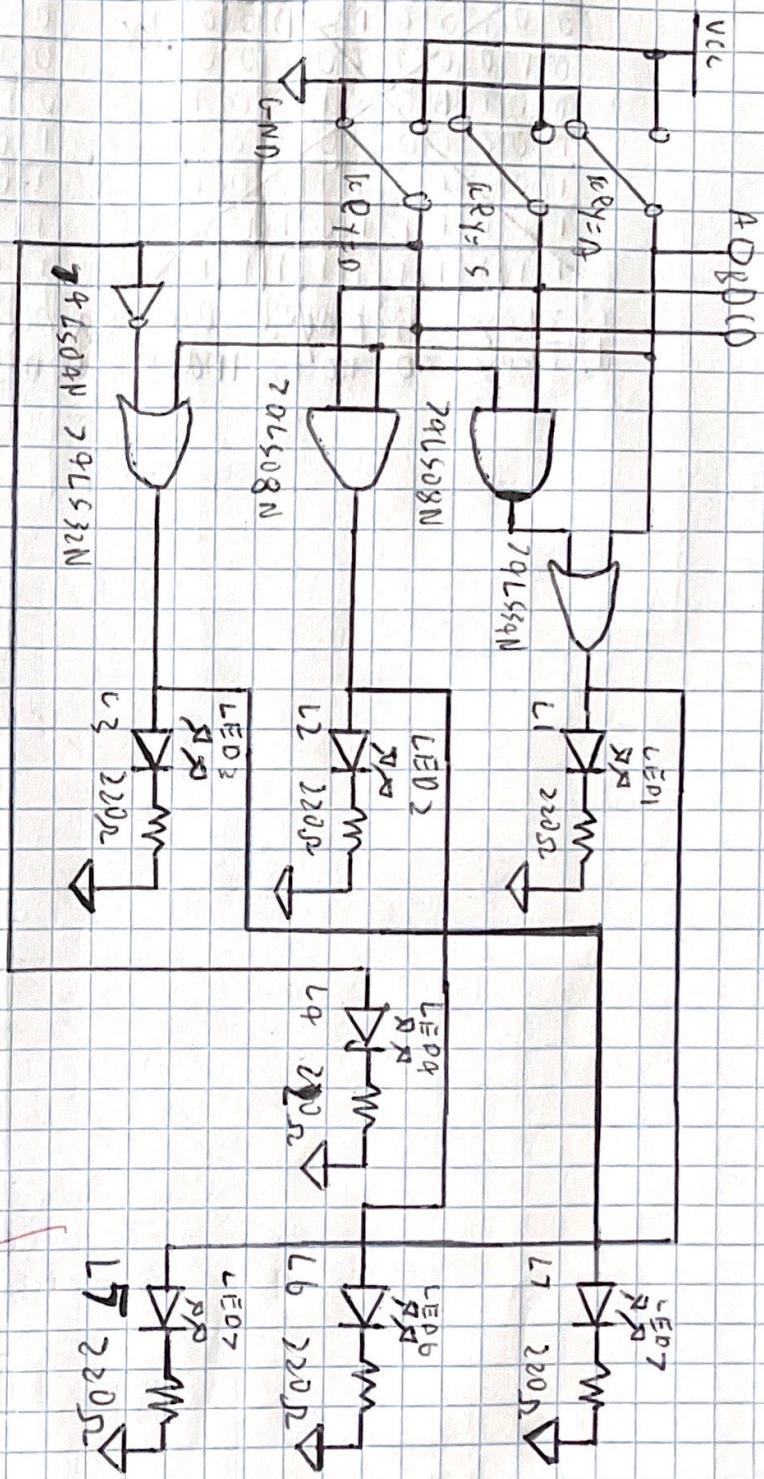


## Project 1.2.7] Understanding Digital Design-Random Number Generator

1.



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DATE 1/28/12 continued on page 69

signature Nelson Vea

DATE 11/26/11

Proprietary Information

Topic 63

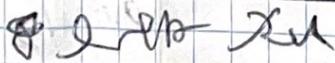
a. On Multisim

A	B	C	L1	L2	L3	L4	L5	L6	L7
0	0	0	0	0	0	1	0	0	0
0	0	1	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	1	0	1
1	0	1	0	1	1	1	0	1	1
1	1	0	1	1	0	1	1	1	1
1	1	1	1	1	1	1	1	1	1

A	B	C	L1	L2	L3	L4	L5	L6	L7
0	0	0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0	0	0
0	1	0	0	0	0	0	0	0	0
0	1	1	0	0	1	1	0	0	0
1	0	0	1	0	1	0	1	0	1
1	0	1	0	1	1	1	0	1	1
1	1	0	1	1	0	1	1	1	1
1	1	1	1	1	1	1	1	1	1

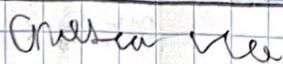
c. They displayed as expected.

d. They do not make sense, and they do not matter.

Signature 

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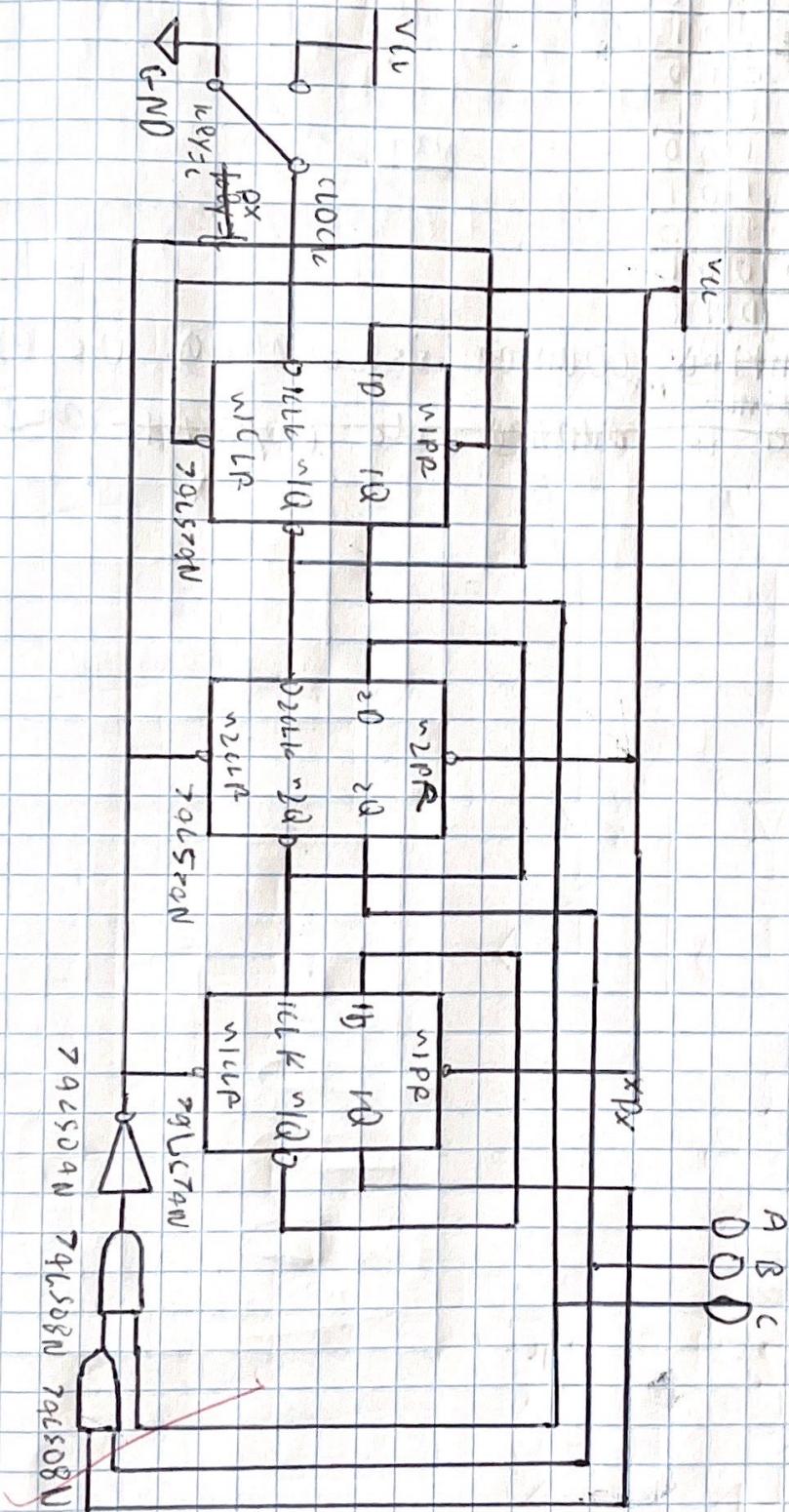
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page 65

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2.



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Date 1/28/12

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a. clock	A	B	C
Initial values	0	0	1
1st cycle	0	1	0
2nd cycle	0	1	1
3rd cycle	1	0	0
4th cycle	1	0	1
5th cycle	1	1	0
6th cycle	0	0	1
7th cycle	0	1	0

- b. The ~~counting~~ counter is counting as expected.  
~~for 0 to 5~~ Multistate  
c. The counter is ~~counting~~ as expected.

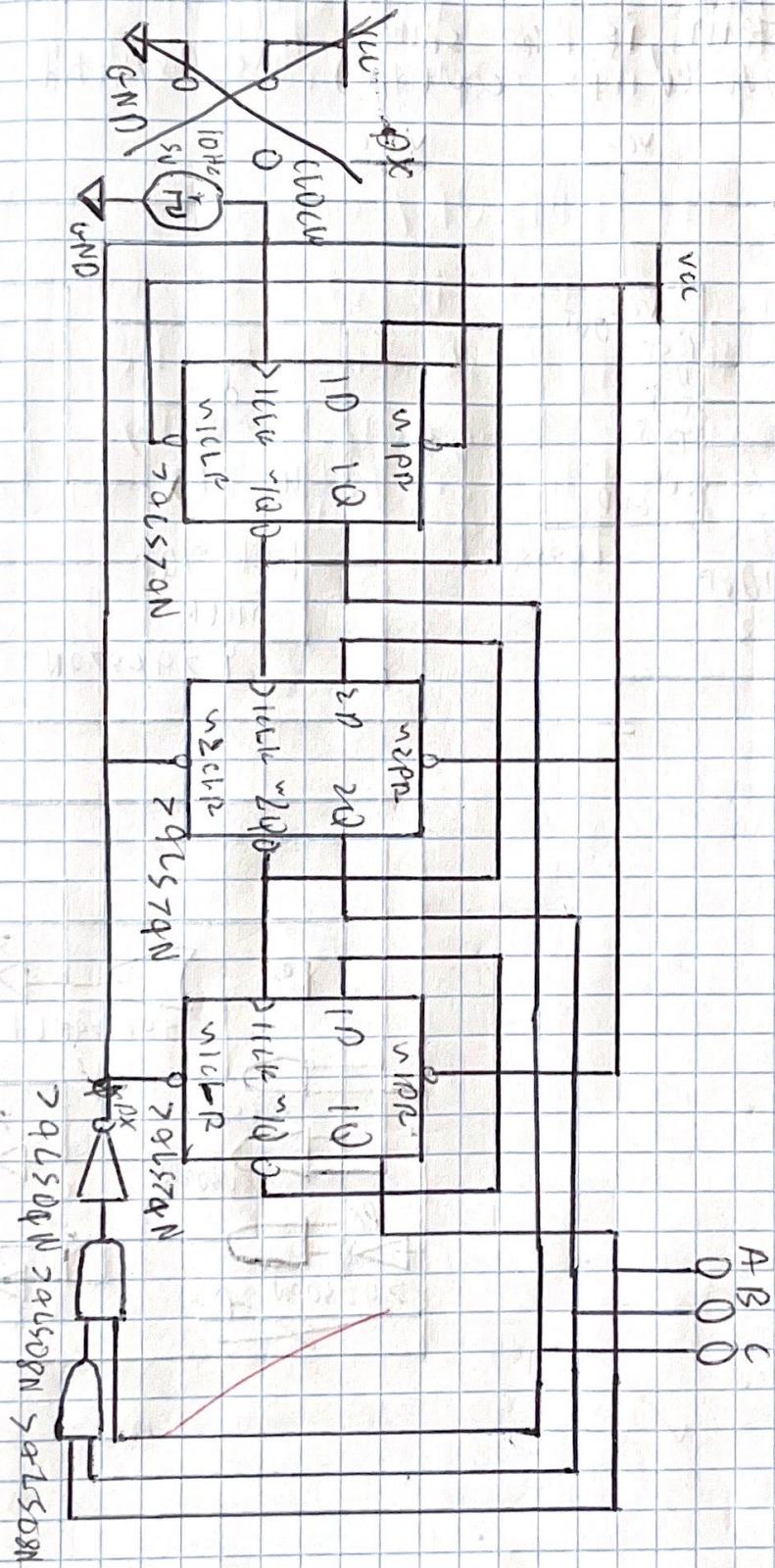
Signature: [Signature]

Signature: [Signature]

Date 1/28/12 | Continued on page 67

Date 1/28/12 Proprietary Information

C.

ABC  
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Date 11/28/12

Continued on  
page 68

Signature

Chesa Lee

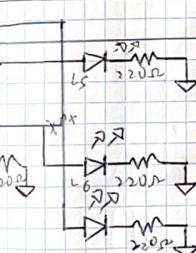
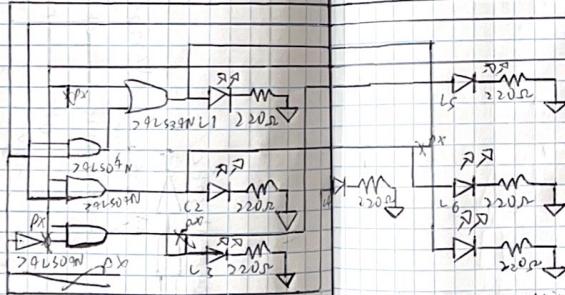
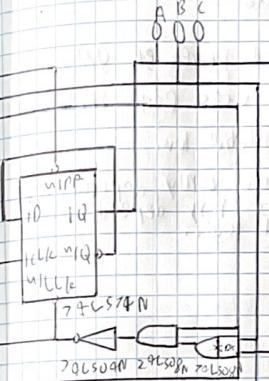
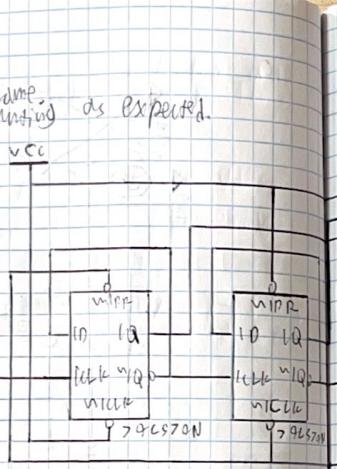
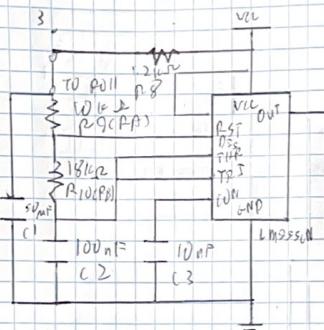
Date 11/28/12

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page 68 79

- d. On ~~Multibit~~ multibit
  - e. The pattern is the same.
  - f. The counter is counting as expected.



- b-c. On Multisim  
d. They are cycling as working as expected.  
e, I added a switch connecting the OUT pin of the  
MAX3232 and the UCLK pin of the leftmost 74LS18N.

Signature	John Doe	Date 1/28/12	Proprietary Information	Signature	John Doe	Date 1/28/12	Proprietary Information
Signature	Chelsea Lee	Date 1/28/12	continued on page 2	Signature	Chelsea Lee	Date 1/28/12	continued on page 20

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5. I predict the circuit will stop and show a random number. However, when I actually open the switch, the LED patterns keep cycling.

Conclusion:

1. They were the AND, OR, and inverter gates.
2. This means the clk input uses edge triggering.
3. This means the input is an active low.
4. In combinational logic, outputs only depend on current inputs, while outputs may depend on previous outputs in sequential logic.



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Continues  
page 2

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