

명령		CU												ALU								W	F
		test	Enable						Select				stack	A	B	cmd	out	Z	DC	C	test	d=1(F)	
			ir	w	rf	tris	stat	PC	w	A	bus	rf											
ADDWF	Q2	0	1	0	0	0	0	1	0	0	0	0	2	1	1	0	2	0	0	0	1	1	1
	Q3	0	0	0	0	0	0	0	0	0	2	0	2	1	1	0	2	0	0	0	1	1	1
	Q4	0	0	0	0	0	1	0	0	0	1	0	2	1	1	0	2	0	0	0	1	1	1
NOP	Q2	1	0	0	0	0	0	0	0	0	0	0	2	0	0	0	0	1	0	0	1	0	1
	Q3	1	0	0	0	0	0	0	0	0	0	0	2	0	0	0	0	1	0	0	1	0	1
	Q4	1	1	0	0	0	0	0	0	0	0	0	2	0	0	0	0	1	0	0	1	0	1
ANDWF	Q2	0	0	0	0	0	0	0	0	0	2	0	2	2	2	0	4	0	0	0	1	2	254
	Q3	0	0	0	0	0	1	0	0	0	1	0	2	2	254	6	255	0	0	0	0	2	254
	Q4	0	0	0	1	0	0	1	0	0	0	0	2	2	255	0	1	0	1	1	0	2	254
CLRF	Q2	1	0	0	0	0	0	0	0	0	0	0	2	6	6	0	12	0	0	0	1	6	6
	Q3	1	0	0	0	0	0	0	0	0	1	0	2	6	6	3	0	1	0	0	1	6	6
	Q4	1	1	0	1	0	0	0	0	0	0	0	2	6	0	0	6	0	0	0	1	6	6
CLRW	Q2	0	0	0	0	0	0	0	0	0	0	0	2	170	170	0	84	0	1	1	1	170	1
	Q3	0	0	0	0	0	1	0	0	0	1	0	2	170	170	3	0	1	0	0	1	170	1
	Q4	1	1	1	0	0	0	0	1	0	0	0	2	170	0	0	170	0	0	0	1	170	1
DECF	Q2	1	0	0	0	0	0	0	0	0	2	0	2	2	2	0	4	0	0	0	1	2	2
	Q3	1	0	0	0	0	1	0	0	0	1	0	2	2	2	4	1	0	0	0	1	2	2
	Q4	1	1	0	1	0	0	0	0	0	0	0	2	2	1	0	3	0	0	0	1	2	2
DEOFSZ	Q2	1	0	0	0	0	0	0	0	0	2	0	2	2	2	0	4	0	0	0	1	2	1
	Q3	1	0	0	0	0	1	0	0	0	1	0	2	2	1	4	0	1	0	0	1	2	1
	Q4	1	0	0	1	0	0	0	0	0	0	0	2	2	0	0	2	0	0	0	1	2	1
	Q5	1	0	0	0	0	0	1	0	0	0	0	2	2	2	0	4	0	0	0	1	2	1
	Q6	1	0	0	0	0	0	0	0	0	0	0	2	2	2	0	4	0	0	0	1	2	0
	Q7	1	0	0	0	0	0	0	0	0	0	0	2	2	2	0	4	0	0	0	1	2	0
	Q8	1	1	0	0	0	0	0	0	0	0	0	2	2	2	0	4	0	0	0	1	2	0

표 1 Control Unit / ALU 동작표 (1)

명령		CU												ALU								W	F
		test	Enable						Select				stack	A	B	cmd	out	Z	DC	C	test	d=1(F)	
			ir	w	rf	tris	stat	PC	w	A	bus	rf											
COMF	Q2	1	0	0	0	0	0	0	0	0	0	0	2	2	2	0	4	0	0	0	1	2	0
	Q3	1	0	0	0	0	1	0	0	0	1	0	2	2	2	5	253	0	0	0	1	2	0
	Q4	1	1	0	1	0	0	0	0	0	0	0	2	2	253	0	255	0	0	0	0	2	0
INCF	Q2	1	0	0	0	0	0	0	0	0	2	0	2	0	0	0	0	1	0	0	1	0	17
	Q3	1	0	0	0	0	1	0	0	0	1	0	2	0	17	6	18	0	0	0	0	0	17
	Q4	0	1	0	1	0	0	0	0	0	0	0	2	0	18	0	18	0	0	0	1	0	17
INCFSZ	Q2	1	0	0	0	0	0	0	0	0	2	0	2	2	2	0	4	0	0	0	1	2	253
	Q3	1	0	0	0	0	1	0	0	0	1	0	2	2	253	6	254	0	0	0	0	2	253
	Q4	0	0	0	1	0	0	1	0	0	0	0	2	2	254	0	0	1	1	1	0	2	253
IORWF	Q2	1	0	0	0	0	0	0	0	0	2	0	2	4	4	0	8	0	0	0	1	4	2
	Q3	1	0	0	0	0	1	0	0	0	1	0	2	4	2	7	6	0	0	0	1	4	2
	Q4	1	1	0	1	0	0	0	0	0	0	0	2	4	6	0	10	0	0	0	1	4	2
MOVF	Q2	1	0	0	0	0	0	0	0	0	2	0	2	4	4	0	8	0	0	0	1	4	6
	Q3	1	0	0	0	0	1	0	0	0	1	0	2	4	6	8	6	0	0	0	1	4	6
	Q4	1	1	1	0	0	0	0	1	0	0	0	2	4	6	0	10	0	0	0	1	4	6
MOWF	Q2	1	0	0	0	0	0	0	0	0	2	0	2	6	6	0	12	0	0	0	1	6	6
	Q3	1	0	0	0	0	0	0	0	0	1	0	2	6	6	9	6	0	0	0	1	6	6
	Q4	1	1	0	1	0	0	0	0	0	0	0	2	6	6	0	12	0	0	0	1	6	6
RLF	Q2	0	0	0	0	0	0	0	0	0	2	0	2	6	6	0	12	0	0	0	1	6	254
	Q3	0	0	0	0	0	1	0	0	0	1	0	2	6	254	10	252	0	0	1	0	6	254
	Q4	0	1	0	1	0	0	0	0	0	0	0	2	6	252	0	2	0	1	1	0	6	254
RRF	Q2	0	0	0	0	0	0	0	0	0	2	0	2	6	6	0	12	0	0	0	1	6	249
	Q3	0	0	0	0	0	1	0	0	0	1	0	2	6	249	11	252	0	0	1	0	6	249
	Q4	0	1	0	1	0	0	0	0	0	0	0	2	6	252	0	2	0	1	1	0	6	249
SUBWF	Q2	0	0	0	0	0	0	0	0	0	2	0	2	6	6	0	12	0	0	0	1	6	127
	Q3	0	0	0	0	0	1	0	0	0	1	0	2	6	127	12	121	0	0	1	0	6	127
	Q4	0	1	0	1	0	0	0	0	0	0	0	2	6	121	0	127	0	0	0	0	6	127

표 2 Control Unit / ALU 동작표 (2)

명령		CU												ALU								W	F
		test	Enable						Select				stack	A	B	cmd	out	Z	DC	C	test	d=1(F)	
			ir	w	rf	tris	stat	PC	w	A	bus	rf											
SWAPF	Q2	0	0	0	0	0	0	0	0	0	2	0	2	6	6	0	12	0	0	0	1	6	121
	Q3	0	0	0	0	0	1	0	0	0	1	0	2	6	121	13	151	0	0	0	0	6	121
	Q4	0	1	0	1	0	0	0	0	0	0	0	2	6	151	0	157	0	0	0	1	6	121
XORWF	Q2	0	0	0	0	0	0	0	0	0	2	0	2	6	6	0	12	0	0	0	1	6	151
	Q3	0	0	0	0	0	1	0	0	0	1	0	2	6	151	14	145	0	0	0	1	6	151
	Q4	1	1	0	1	0	0	0	0	0	0	0	2	6	145	0	151	0	0	0	1	6	151
BCF	Q2	1	0	0	0	0	0	0	0	0	2	0	2	6	6	0	12	0	0	0	1	6	145
	Q3	1	0	0	0	0	0	0	0	1	1	0	2	7	145	15	17	0	0	0	0	6	145
	Q4	1	1	0	1	0	0	0	0	0	0	0	2	6	17	0	23	0	0	0	1	6	145
BSF	Q2	1	0	0	0	0	0	0	0	0	2	0	2	6	6	0	12	0	0	0	1	6	17
	Q3	1	0	0	0	0	0	0	0	1	1	0	2	7	17	16	145	0	0	0	1	6	17
	Q4	1	1	0	1	0	0	0	0	0	0	0	2	6	145	0	151	0	0	0	1	6	17
BTFSC	Q2	1	0	0	0	0	0	0	0	0	2	0	2	6	6	0	12	0	0	0	1	6	17
	Q3	1	0	0	0	0	1	0	0	1	1	0	2	7	17	17	17	0	0	0	1	6	17
	Q4	1	0	0	0	0	0	1	0	0	0	0	2	6	17	0	23	0	0	0	1	6	17
	Q5	1	0	0	0	0	0	0	0	0	0	0	2	6	6	0	12	0	0	0	1	6	17
	Q6	1	0	0	0	0	0	0	0	0	0	0	2	6	6	0	12	0	0	0	1	6	17
	Q7	1	0	0	0	0	0	0	0	0	0	0	2	6	6	0	12	0	0	0	1	6	17
	Q8	1	1	0	0	0	0	0	0	0	0	0	2	6	6	0	12	0	0	0	1	6	17
BTFSS	Q2	68	0	0	0	0	0	0	0	0	0	2	0	2	6	6	0	12	0	0	0	1	6
	Q3	69	0	0	0	0	0	1	0	0	1	1	0	2	7	145	17	145	0	0	0	0	6
	Q4	70	0	0	0	0	0	0	1	0	0	0	0	2	6	145	0	151	0	0	0	1	6
	Q5	71	0	0	0	0	0	0	0	0	0	0	0	2	6	6	0	12	0	0	0	1	6
	Q6	5	0	0	0	0	0	0	0	0	0	0	0	2	6	6	0	12	0	0	0	1	6
	Q7	6	0	0	0	0	0	0	0	0	0	0	0	2	6	6	0	12	0	0	0	1	6
	Q8	7	0	1	0	0	0	0	0	0	0	0	0	2	6	6	0	12	0	0	0	1	6

표 3 Control Unit / ALU 동작표 (3)

명령		cCU												ALU								W	F
		test	Enable						Select				stack	A	B	cmd	out	Z	DC	C	test	d=1(F)	
			ir	w	rf	tris	stat	PC	w	A	bus	rf											
ANDWL	Q2	1	0	0	0	0	0	0	0	0	0	0	2	6	6	0	12	0	0	0	1	6	1
	Q3	1	0	0	0	0	1	0	0	2	1	0	2	255	6	2	6	0	0	0	1	6	1
	Q4	1	1	1	0	0	0	0	1	0	0	0	2	6	6	0	12	0	0	0	1	6	1
CALL	Q2	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	44
	Q3	1	0	0	0	0	0	0	0	0	0	0	2	0	0	0	0	1	0	0	1	0	45
	Q4	1	0	0	0	0	0	0	0	0	0	0	2	0	0	0	0	1	0	0	1	0	45
	Q5	1	0	0	0	0	0	0	0	0	0	0	2	0	0	0	0	1	0	0	1	0	45
	Q6	1	0	0	1	0	0	0	0	0	0	2	2	0	0	0	0	1	0	0	1	0	45
	Q7	1	0	0	0	0	0	0	0	0	0	0	2	0	0	0	0	1	0	0	1	0	45
	Q8	1	1	0	0	0	0	0	0	0	0	0	2	0	0	0	0	1	0	0	1	0	48
RETLW	Q2	0	0	1	0	0	0	0	0	0	0	0	2	170	170	0	84	0	1	1	1	170	55
	Q3	0	0	0	0	0	0	0	0	0	0	0	2	99	170	0	13	0	0	1	0	99	56
	Q4	0	0	0	0	0	0	0	0	0	0	0	2	99	99	0	198	0	0	0	1	99	56
	Q5	0	0	0	0	0	0	0	0	0	0	0	2	99	99	0	198	0	0	0	1	99	56
	Q6	0	0	0	1	0	0	0	0	0	0	1	1	99	99	0	198	0	0	0	1	99	56
	Q7	0	0	0	0	0	0	0	0	0	0	0	2	99	99	0	198	0	0	0	1	99	56
	Q8	0	1	0	0	0	0	0	0	0	0	0	2	99	99	0	198	0	0	0	1	99	45
GOTO	Q2	0	0	0	0	0	0	0	0	0	0	0	2	99	99	0	198	0	0	0	1	99	46
	Q3	0	0	0	0	0	0	0	0	0	0	0	2	99	99	0	198	0	0	0	1	99	47
	Q4	0	0	0	0	0	0	0	0	0	0	0	2	99	99	0	198	0	0	0	1	99	47
	Q5	0	0	0	0	0	0	0	0	0	0	0	2	99	99	0	198	0	0	0	1	99	47
	Q6	0	0	0	1	0	0	0	0	0	0	2	2	99	99	0	198	0	0	0	1	99	47
	Q7	0	0	0	0	0	0	0	0	0	0	0	2	99	99	0	198	0	0	0	1	99	47
	Q8	0	1	0	0	0	0	0	0	0	0	0	2	99	99	0	198	0	0	0	1	99	56

표 4 Control Unit / ALU 동작표 (4)

명령		CU												ALU								W	F
		test	Enable						Select				stack	A	B	cmd	out	Z	DC	C	test	d=1(F)	
			ir	w	rf	tris	stat	PC	w	A	bus	rf											
IORWL	Q2	1	0	0	0	0	0	0	0	0	0	0	2	0	0	0	0	1	0	0	1	0	1
	Q3	1	0	0	0	0	1	0	0	2	1	0	2	255	0	7	255	0	0	0	1	0	1
	Q4	1	1	1	0	0	0	0	1	0	0	0	2	0	255	0	255	0	0	0	0	0	1
XORLW	Q2	1	0	0	0	0	0	0	0	0	0	0	2	255	255	0	254	0	1	1	0	255	1
	Q3	1	0	0	0	0	1	0	0	2	1	0	2	255	255	14	0	1	0	0	0	255	1
	Q4	0	1	1	0	0	0	0	1	0	0	0	2	255	0	0	255	0	0	0	1	255	1
MOVLW	Q2	0	0	0	0	0	0	0	0	0	0	0	2	0	0	0	0	1	0	0	1	0	1
	Q3	0	0	0	0	0	0	0	0	2	1	0	2	170	0	9	170	0	0	0	1	0	1
	Q4	0	1	1	0	0	0	0	1	0	0	0	2	0	170	0	170	0	0	0	1	0	1
TRIS	Q2	0	0	0	0	0	0	0	0	0	0	0	2	170	170	0	84	0	1	1	1	170	1
	Q3	0	0	0	0	1	0	0	0	0	0	0	2	170	170	0	84	0	1	1	1	170	1
	Q4	0	1	0	0	0	0	0	0	0	0	0	2	170	170	0	84	0	1	1	1	170	1

표 5 Control Unit / ALU 동작표 (5)