Design Project: ELE 404
Multistage Amplifier Circuit

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Overview

An amplifier can be simply described as an electronic device/component which increases or decreases the amplitude of an output compared to its input. The amount of amplification of a specific amplifier is measured by its "gain". For the output signal's amplitude to be increased, the amplifier should have an absolute gain larger than 1, whereas a lower powered signal would be produced by an amplifier with an absolute gain between 0 and 1. Transistor amplifiers are being used commonly today, and are of two types: Bipolar Junction Transistors(BJTs) and Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs).

Bipolar Junction Transistors can be set up in 3 ways, namely, Common Emitter Amplifier(CE Amp), Common Base Amplifier(CB Amp), and Common Collector Amplifier(CC Amp). Each type of configuration has its own properties, as shown in Table 1. The objective of this Design Project was to design, simulate, and implement an amplifier circuit which would fulfill a set of specifications.

Amplifier	Voltage Gain	Input Resistance	Output Resistance
Common Emitter (CE)	Moderate to high	Moderate to high	High
Common Collector (CC)	Less than unity	High	Low
Common Base (CB)	High	Low	High

Table 1: BJT properties

Specifications

- Open-circuit (no-load) voltage gain: **$|A_{Vo}|$ = 50 (±10%)**;
- Number of transistors (stages): **no more than 3 BJTs**;
- Power supply: +15V relative to the ground;
- Output resistance: **no larger than 500 Ω**;
- Input resistance: **no less than 80 kΩ**;
- Quiescent current drawn from the power supply**: no larger than 5 mA**;
- Maximum no-load output signal swing: **no less than 8 V peak to peak.**

To meet the aforementioned specifications, an amplifier circuit with 3 BJTs connected as CC-CE-CC will be used.

Design Process

Common Emitter Amplifier

The main purpose of the CE Amplifier is to attain the required no-load voltage gain (A_{Vo}), and contibute for the Input Resistance (R_i). The first step in this portion of the design process was to set the emitter voltage, V_{E1}, to be 2.1V, as the emitter voltage should be roughly 3 times $V_{BE,on}$ (0.7V) for stability purposes. Using that and $V_{CE,sat}$ (0.3V) to find the associated quiscent node voltages V_B, V_C. Using these values and relevant formulas, the currents associated with the transistor and its gain was calculated. After setting R_C to 56 kΩ, R_{E1}, R_{E2}, and R_i' were calculated although they will be adjusted once other amplifiers are in place.

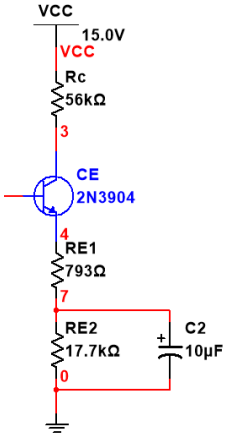


Figure 1:
CE Amp. Schematic

Common Collector Amplifier #1

At this point, although the input resistance condition is met, the output resistance is far too high for the specification, since $R_O = R_C = 56$ kΩ. Hence, a CC Amplifier was introduced to lower the output resistance (R_o) and further increase the input resistance. After doing the appropriate calculations (pleases refer to page XX), the no-load voltage gain was found out to be -46.23 V/V. Since this does not conform with the specifications, R_{E1}, R_{E2}, and R_i' were adjusted for it to -51.26 V/V (extra -1.26 V/V to compensate for the next CC amplifier).

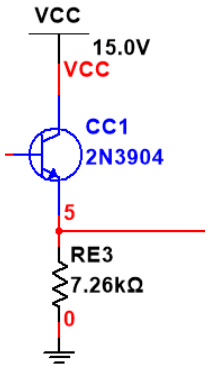


Figure 2:
CC#1 Amp. Schematic

Common Collector Amplifier #2

The third and final BJT amplifier to be added was another CC Amplifier. Much like its predeccessor, its function was to further adjust the input and output resistances to meet specifications. After continuing its calculations, please refer to pages XX-XX, the no-load voltage gain was calculated to be -49.91 V/V, input resistance to be 80 kΩ, and output resistance to be 0.5439 kΩ.

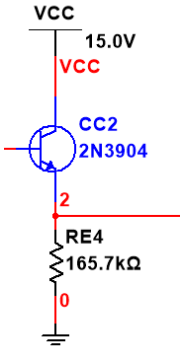


Figure 3:
CC#2 Amp. Schematic

Simulation Results

Simulation Schematic

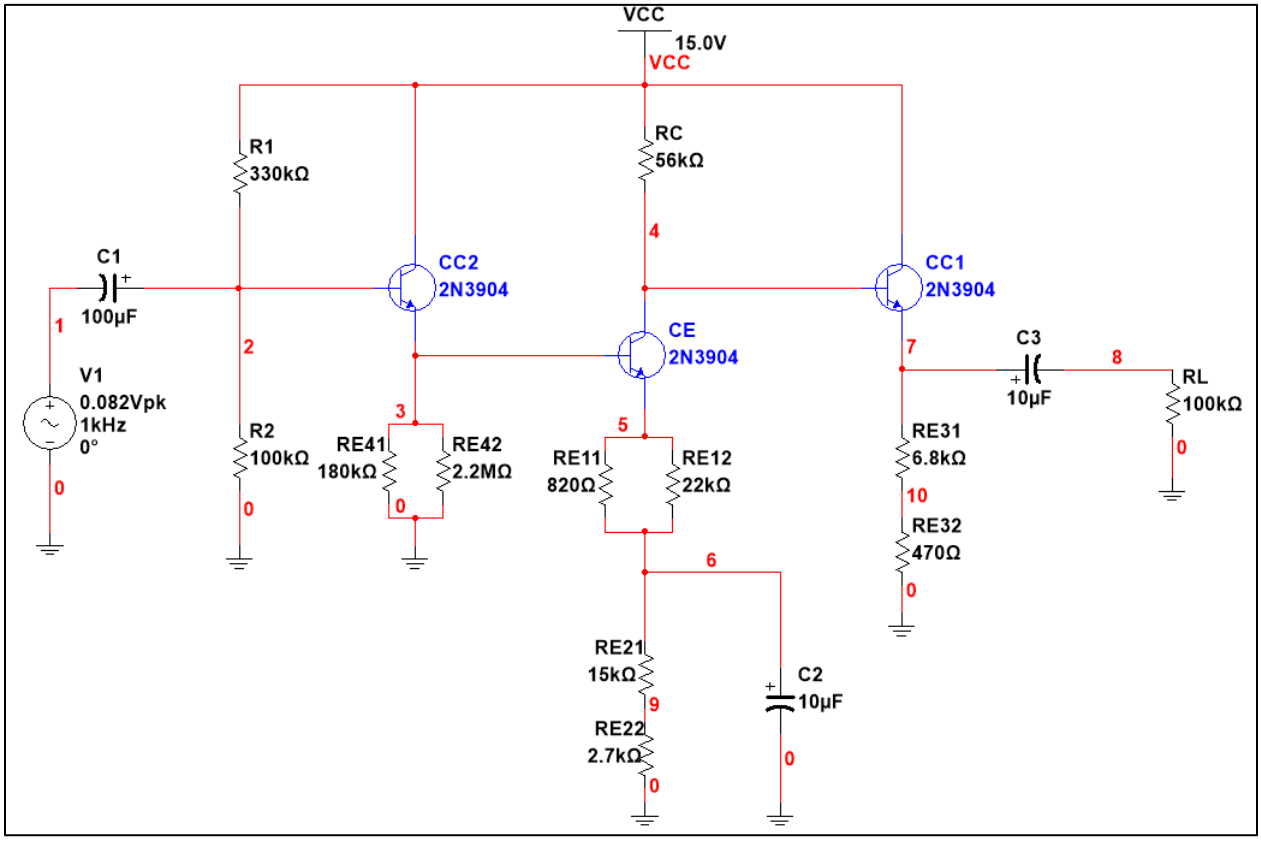
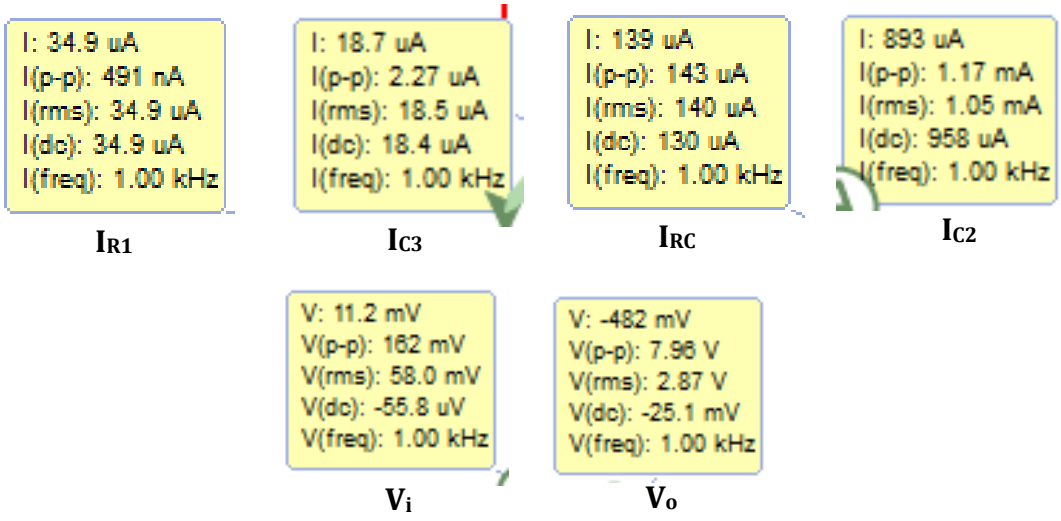


Figure 4: Simulation Schematic



I_{R1} I_{C3} I_{RC} I_{C2}

V_i V_o

Figure 5: Important node voltages and currents

Simulation Waveforms

Note: A load of 100 kΩ was used for no-load condition to simulate infinite resistance (similar to lab 08)

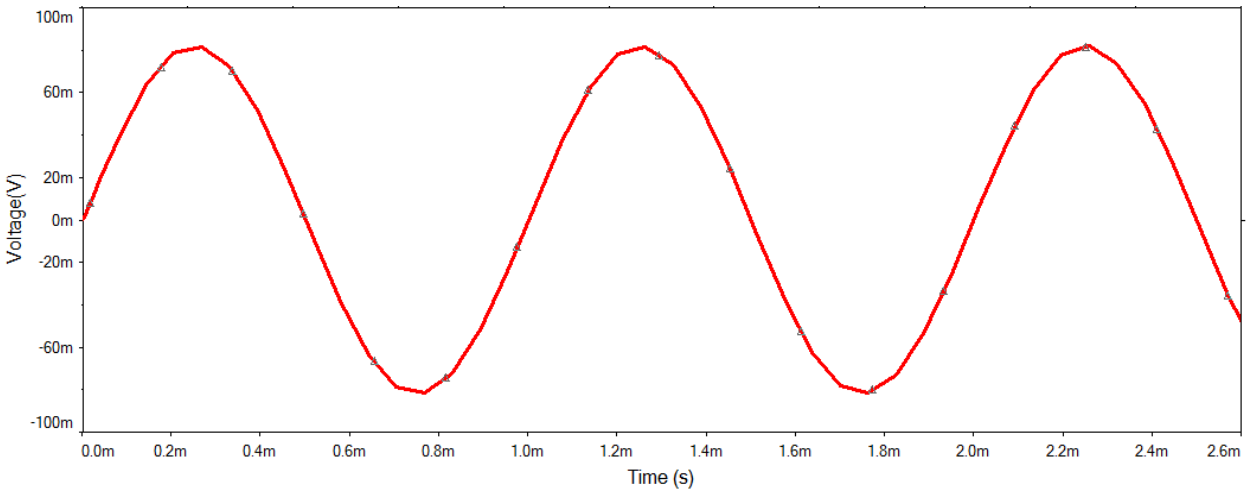


Figure 6: Simulation waveform for V_i vs t (1 kHz)

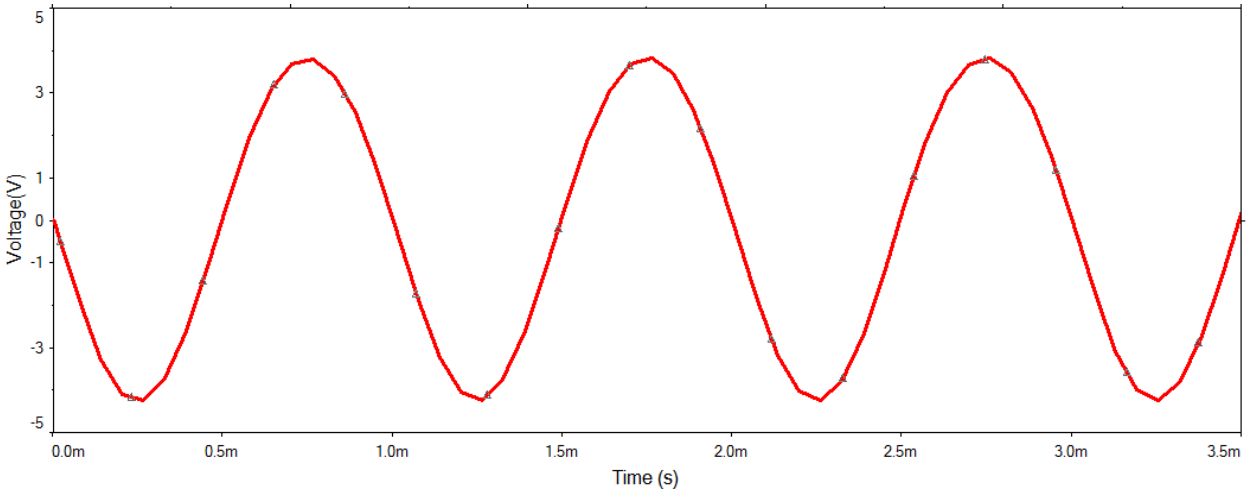


Figure 7: Simulation waveform for V_O vs t (1 kHz)

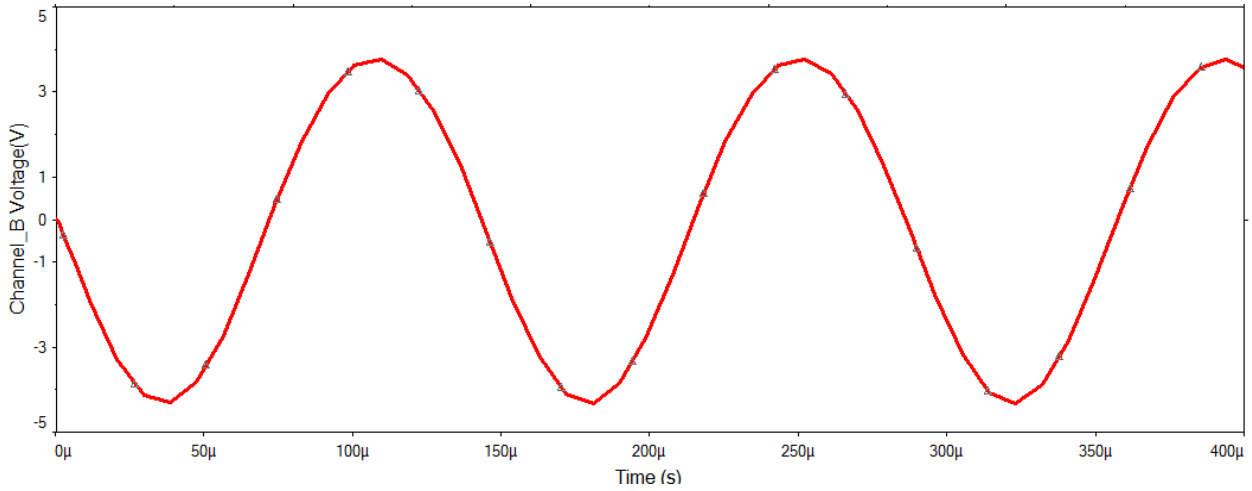


Figure 8: Simulation waveform for V_O vs t (7 kHz)

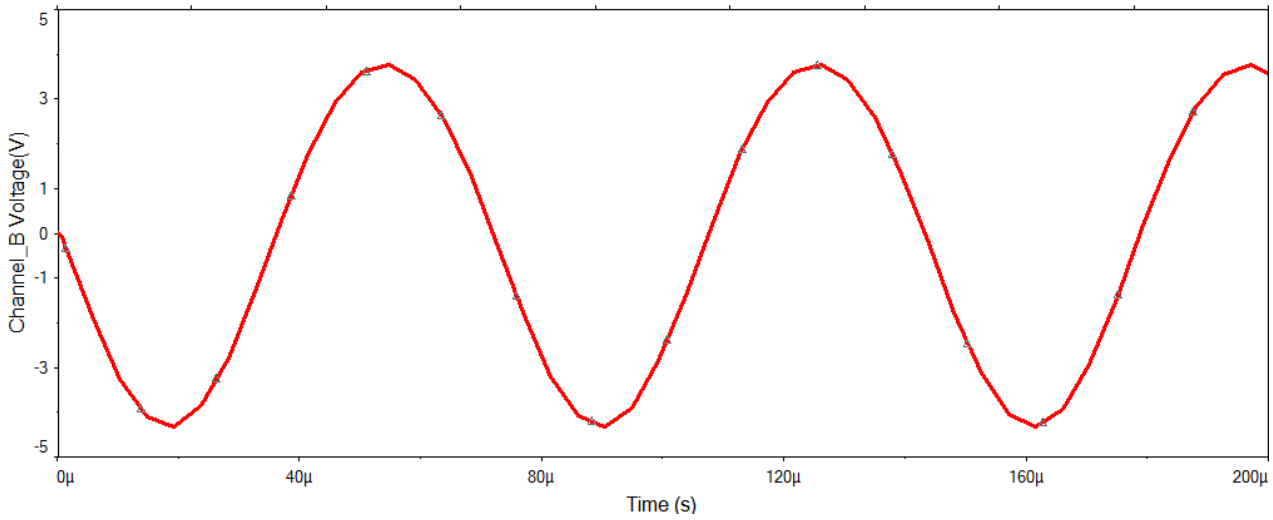


Figure 9: Simulation waveform for V_O vs t (14 kHz)

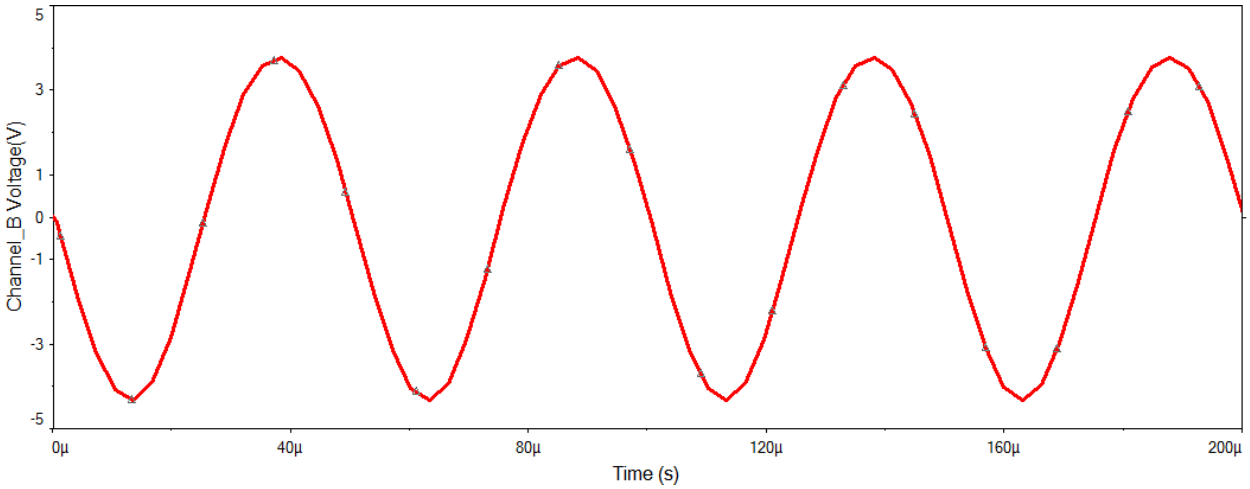


Figure 10: Simulation waveform for V_O vs t (20 kHz)

Manual calculation verifications

	V_i [Vrms]	V_o [Vrms]	$\lvert A_{Vo}\rvert$[V/V]
Simulation	0.058	2.87	49.48
Calculation	--	--	49.91
Percent error	--	--	0. 87%

Table 2: No-load voltage gain comparison

R_i formula from Lab 06:

$$R_i = R_{t,in}\left(\frac{v_i}{v_t - v_i}\right)$$

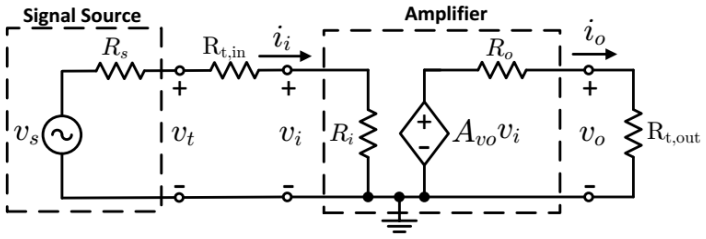


Figure 11: Diagram related to R_i simulation calculation

	V_t [Vrms]	V_i [Vrms]	R_i [kΩ]	I_{Supply} [mA]
Simulation	0.058	0.0282	75.71	1.243
Calculation	--	--	80.0	0.914
Percent error	--	--	5.61%	-26%

Table 3: Input Resistance and Quiescent Current draw comparison

Conclusion

At the end of the simulation, it is shown that the CC-CE-CC multistage amplifier meets the given specifications by having high Gain and Input Resistance while having a lower Output Resistance. The Common-Emitter amplifier supplied around -51V/V while providing a good Input Resistance, although quite not being able to match the 80kΩ mark.

The first Common-Collector amplifier remedied the higher Output Resistance caused by the CE amplifier and helped increase the input resistance although it lowered the gain by a fraction. The second Common-Collector amplifier also functioned alongside the first one, increasing the Input Resistance while decreasing the gain to -49.9V/V.

The minor percent errors are to be expected due to the restrictions on what resistors can be used and real world errors. Other than that, the amplifier worked as intended by providing an Input Resistance of 80kΩ, Output Resistance of 500Ω, and a net Quiescent Current draw under 5mA, all the while falling well within the range of ±50 V/V (±10%) for the voltage gain, for all frequencies ranging from 1 kHz to 20 kHz.