DIGITAL INTEGRATED CIRCUITS DESIGN LAB

PC459EC

Instruction: 2 periods per week *Duration of SEE:- 3hours*
CIE: 25 marks *SEE:- 50 Marks*
Credits: 1

Course Objectives:

1. To develop verilog HDL code for digital circuits using gate level, data flow and behavioral, modeling and Verify the design block using stimulus.
2. To study the VLSI CAD tools.
3. To implement transistor level circuits.

Course Outcomes: On successful completion of the course, the students will be able to

1.write the Verilog HDL programs in gate level and data flow modeling.
2.implement combinational and sequential circuits using Verilog.
3.analyse digital circuits using VLSI CAD tools like Mentor Graphics / Cadence
4.design CMOS circuits like basic gates, adders at the transistor level
5. implement the layout of simple CMOS circuits like inverter and basic gates.

List of Experiments:

Part-A

Write the Code using Verilog and simulate the following:

1. Write structural and dataflow Verilog HDL models for
a) 4-bit ripple carry adder.
b) 4-bit carry Adder – cum Subtractor.
c) 2-digit BCD adder / subtractor.
d) 4-bit carry look ahead adder
e) 4-bit comparator

2. Write a Verilog HDL program in behavioral model for
a) 8:1 multiplexer
b) 3:8 decoder
c) 8:3 encoder
d) 8 bit parity generator and checker

3. Write a Verilog HDL program in Hierarchical structural model for
a) 16:1 multiplexer realization using 4:1 multiplexer
b) 3:8 decoder realization through 2:4 decoder
c) 8-bit comparator using 4-bit comparators and additional logic

4. Write a Verilog HDL program in behavioral model for D,T and JK flip flops, shift registers and counters.

5. Write a Verilog HDL program in structural and behavioral models for
a) 8 bit asynchronous up-down counter b) 8 bit synchronous up-down counter

6.Write a Verilog HDL program for 4 bit sequence detector through Moore state machines

7.Write a Verilog HDL program for 4 bit sequence detector through Mealy state machines

PART-B

Transistor Level implementation of CMOS circuits using VLSI CAD tool

1. Basic Logic Gates: Inverter, NAND and NOR
2. Half Adder and Full Adder
3. 2:1 Multiplexer and 4:1 Multiplexer using 2:1 Multiplexer
4. one bit comparator and four-bit magnitude comparator using one bit comparator
5. Implement the Layout of CMOS Inverter.
6. Implement the Layout of CMOS NAND.

Note:

2. A total of 10 experiments must be completed in the semester.
3. Minimum of 5 experiments from Part-A and 5 from Part-B is compulsory.