Electrical Engineering Department

RFIC

Project

Phase 2

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Spring 2024

Design of LNA

- Assumptions:

$C_{pad} = 50\,fF,\ Q_{wire-bond\ \&\ external} = 50,\ Q_{internal} = 8,\ V_{DD} = 1.8V$

$C_{ox} = 9\frac{fF}{\mu^2}\ ,\ C_{ov} = 0.2\frac{fF}{\mu^2}, E = 0.54\mu, C_j = 1.2\frac{fF}{\mu^2}$

- Requirements from phase 1:

$f_0 = 947.5MHz\ ,\ A_v = 20dB\ ,\ NF = 1.8dB\ ,\ IIP3 = -5dBm,\ f = (935, 960)MHz$

- Design steps:

First, an inductively degenerated cascode common source stage with inductive load was chosen due to the low NF achievable with this setup. Next, using equations from the textbook, the theoretical values of the capacitors and the inductors and the size of the transistors were chosen. In the first iteration $L_g = 45nH$ and $L_s = 5nH$.

$$\frac{1}{(L_G+L_s)(C_{GS1}+C_{pad})} = \omega_0^2 \rightarrow C_{GS1} = 514fF$$

$$\left(\frac{C_{GS1}}{C_{GS1}+C_{pad}}\right)^2 L_1\omega_T = R_s \rightarrow \omega_T = 12.03Grad/s \rightarrow g_m = 6.2mS$$

Then using the plot from mini project 1 for the optimal value of g_m, the width and current of M1 are found as follows: $W = 16.57\mu m\ ,\ I_D = 0.9mA$. The width of M2 is chosen to be the same as M1 and the width and current of the biasing transistor is set to 0.2 times the width and current of M1.

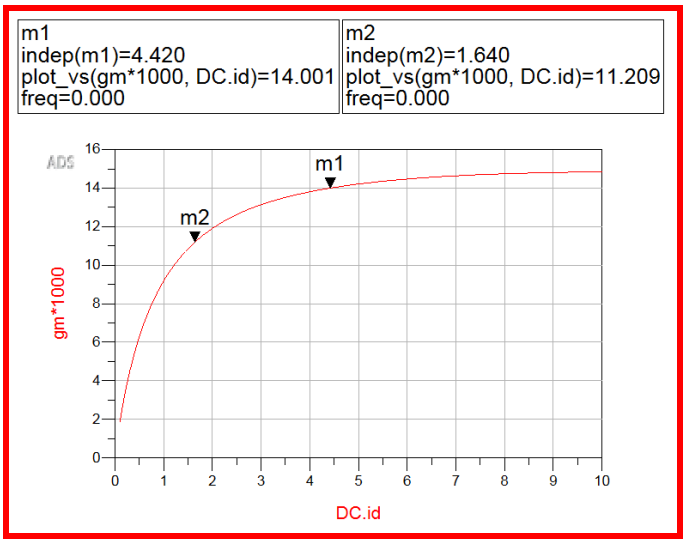


Figure 1: $g_m vs.\ I_D$

Lastly, to choose the value of the drain inductor, the capacitance at the drain of M2 is needed: $C_D = C_{GD2} + C_{DB2} + C_L = 12.15fF + C_L$. Then, to select a reasonable value for the drain inductance, for example, 20nH, an extra capacitor of 1.4 pF is added to the drain of M2.

- Final design:

After some fine-tuning, the final circuit below was reached:

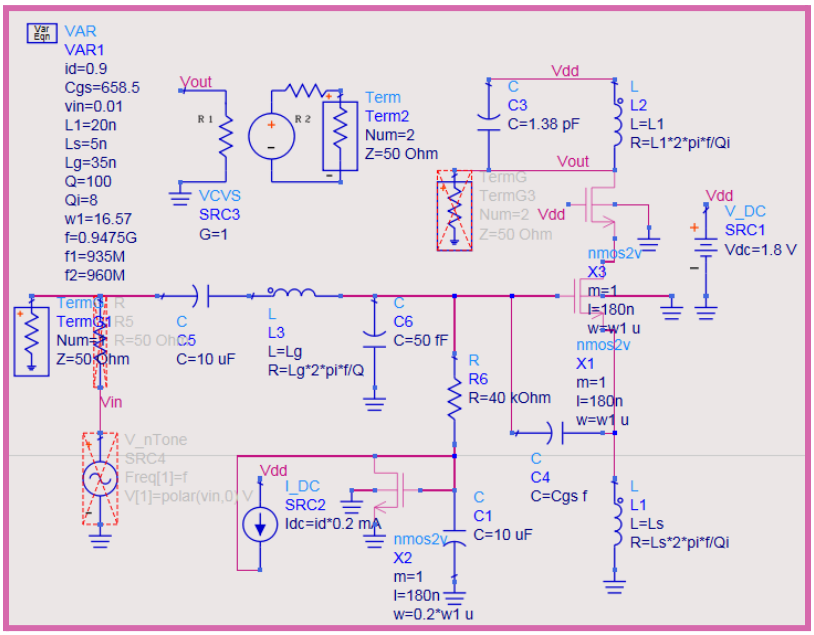
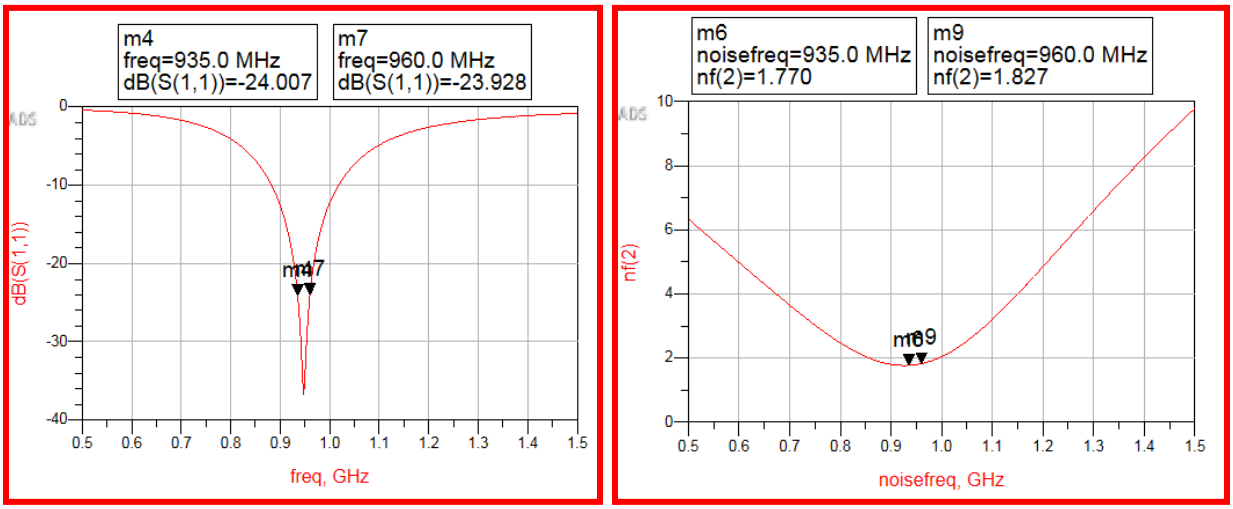


Figure 2: final circuit

- LNA parameters in the GSM receiver bandwidth:



Figures 3 & 4: S_{11} and NF of the final circuit

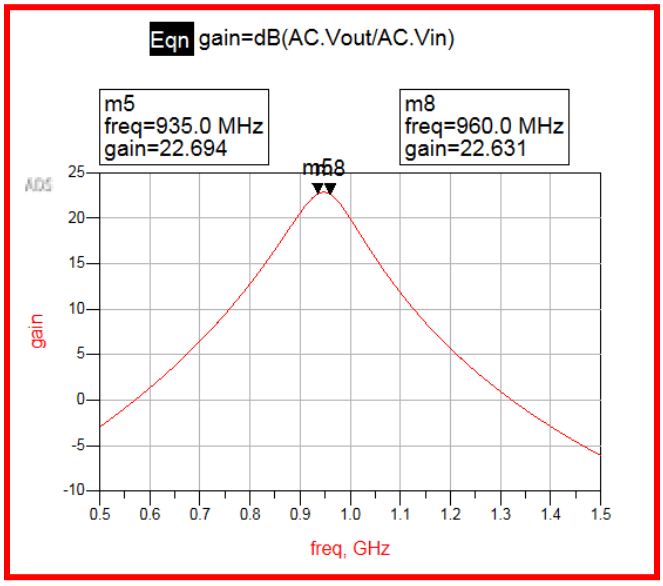


Figure 5: gain of the final circuit

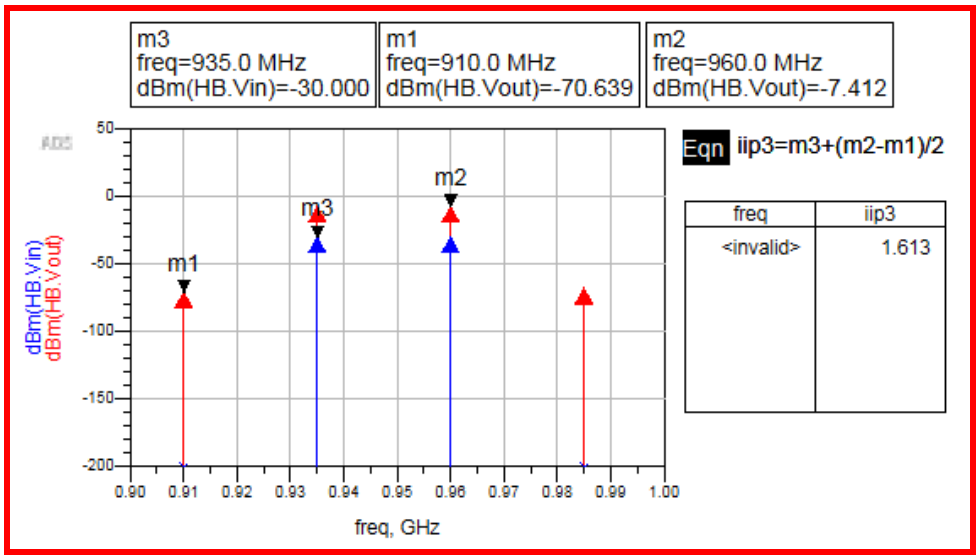


Figure 6: IIP3 of the final circuit

As evident, this circuit satisfies all the requirements.

Table 1: comparison of the theoretical requirements and circuit properties

	$s_{11}(dB)$	NF(dB)	$A_v(dB)$	IIP3(dBm)
Requirement	<-15	<1.8	>20	>-5
Property	-24	1.8	23	0.86

- Gain switching:

  Four switches are used to provide 5 gain steps, each switch lowering the gain by about 5 dB with the lowest gain of 2dB:

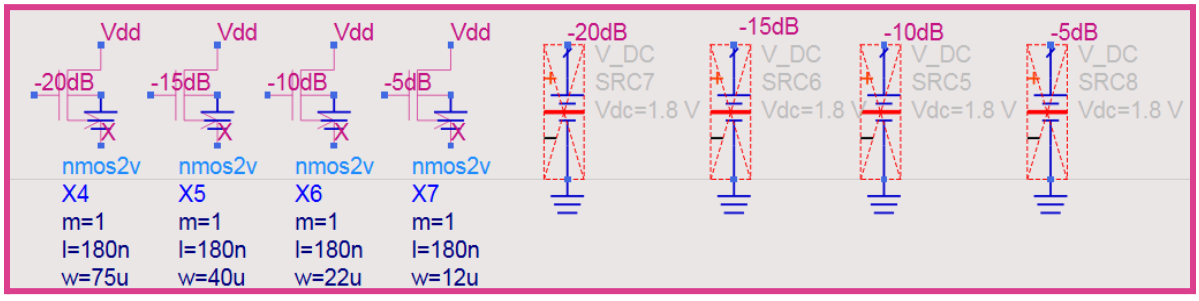


Figure 7: gain switching circuit

Design of mixer

- Requirements from phase 1:

$$f_0 = 947.5MHz\,,\ A_v = 8dB\,,\ NF = 9.6dB\,,\ IIP3 = 25dBm,\ f = (935, 960)MHz$$

- Design steps:

For the design of the mixer, an overdrive voltage of 0.5V for the RF transistor was chosen. Next using these values and the equations from the textbook, other parameters were selected for a gain of 9dB:

$$A_{v,max} = \frac{8}{\pi}\frac{V_{R,max}}{V_{ov1}} = 5 \rightarrow V_{R,max} = 0.98V$$

$$V_{R,max} = V_{DD} - (V_{ov1} + (1 + \frac{\sqrt{2}}{2})V_{ov2}) \rightarrow V_{ov2} = 0.18V$$

$$A_{V,max} = \frac{2}{\pi}g_m R_D \rightarrow g_m R_D = 7.85 \rightarrow if\ R_D = 5k\Omega \rightarrow g_m = 1.57mS$$

$$g_m = K_n'(\frac{W}{L})_1 V_{ov1} \rightarrow W_1 = 2.26\mu m\,,\ I_D = 0.4mA \rightarrow W_2 = 4.3\mu m$$

- Final design:

After a lot of tuning, the final circuit turned out nothing like planned:

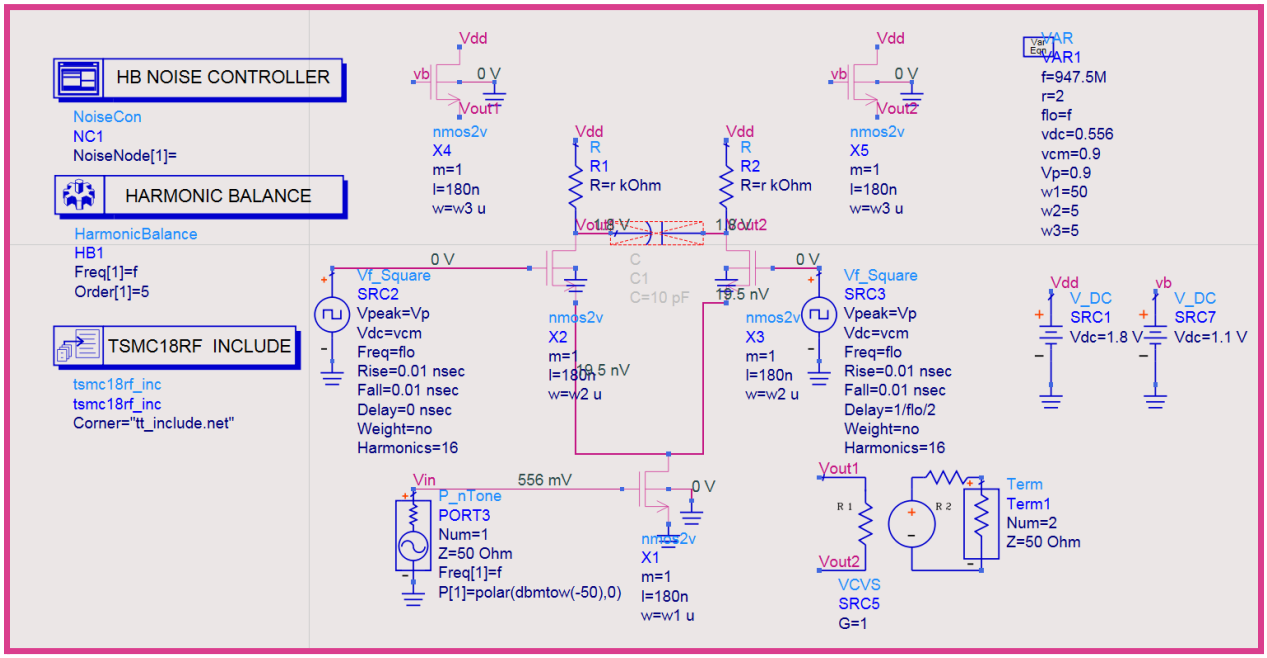


Figure 8: final mixer design

- Mixer properties:

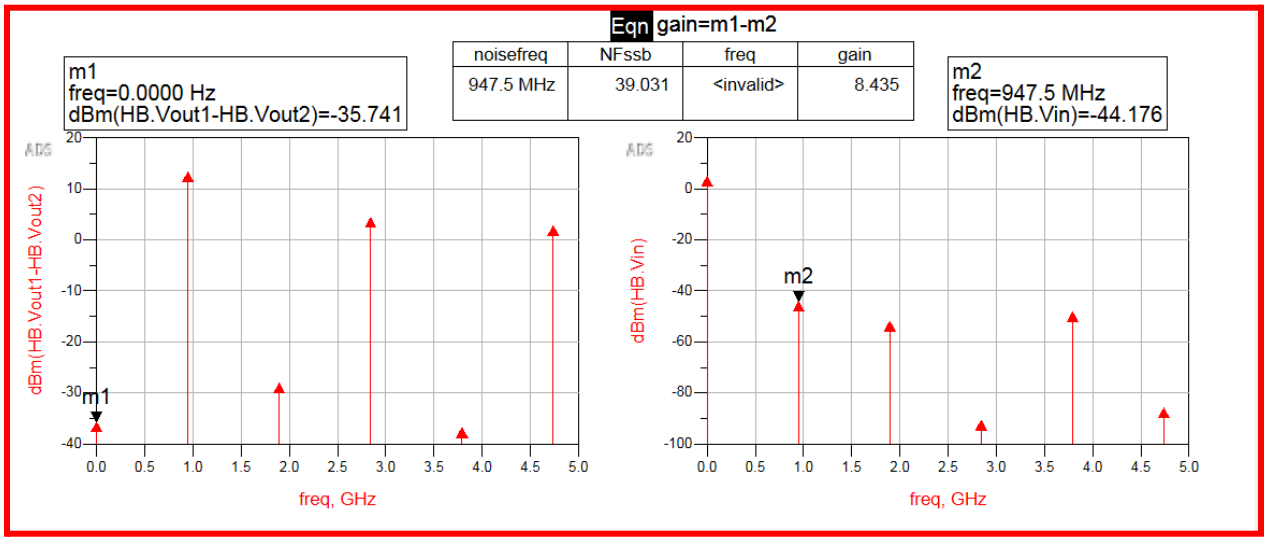


Figure 9: conversion gain and NF of the mixer

The NF of the mixer is terrible but due to limited time it could not be brought any lower.

Mixer and LNA connected

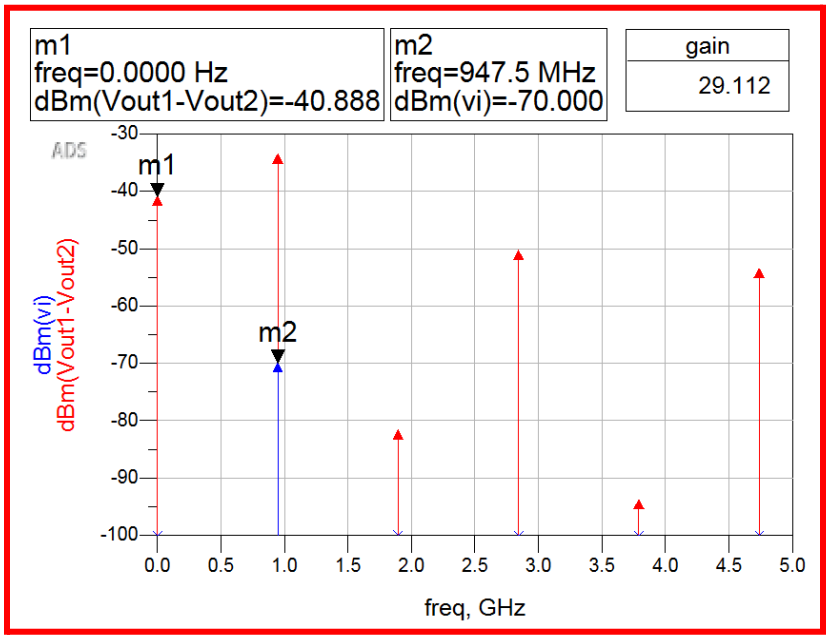


Figure 10: receiver gain

noisefreq	NFssb
947.5 MHz	166.007

Figure 11: NF of the receiver chain

The NF is terrible because the NF of the mixer is too high but I could not bring it any lower. (sorry :()