Electrical Engineering Department

Communications Circuits

Homework 6

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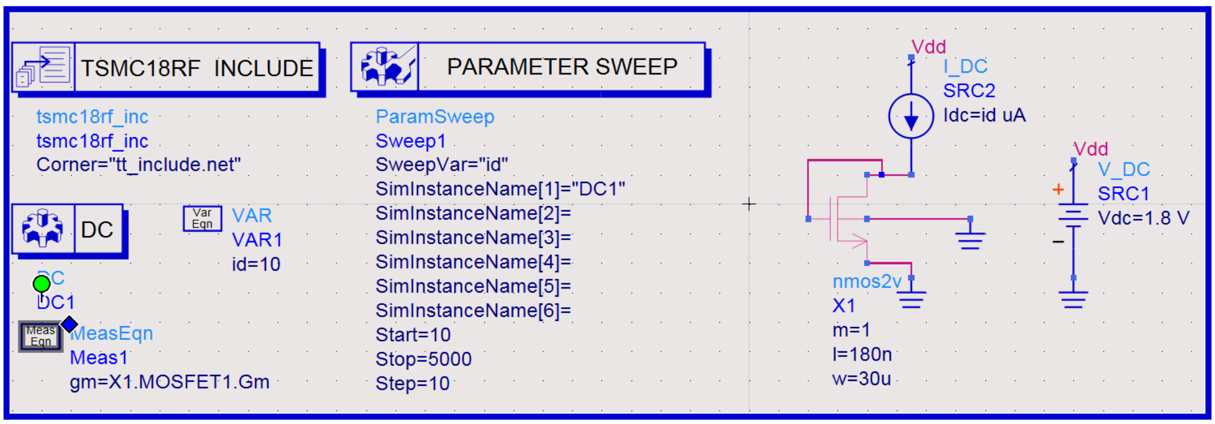
Knowns:

Assume center frequency = 1 GHz, $V_{DD} = 1.8V$, $R_s = 50\Omega$, $L = 180nm$, and $W_0 = 30\mu m$.

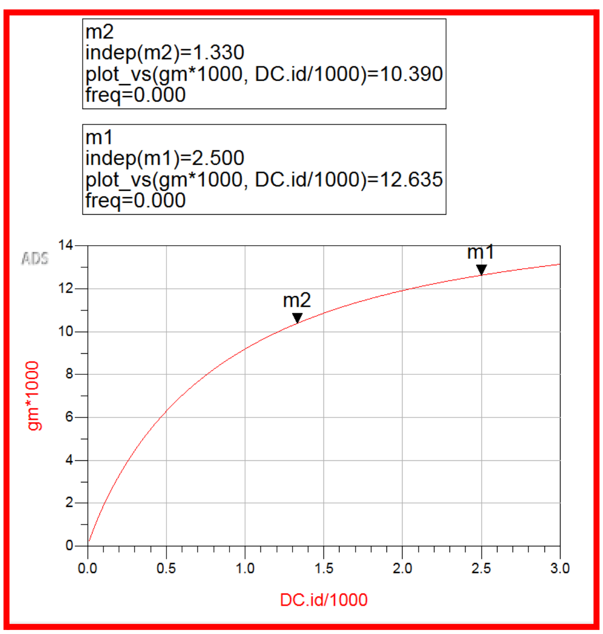
Assuming a typical $g_m = 10mS$ and a wire-bond inductance of $L_s = 1nH$.

Steps:

1. **Plot g_m versus I_D and determine I_D to reach desired g_m.**



Picture 1 - the circuit schematic



Picture 2- g_m vs. drain current

Marker m1 marks the chosen top value and marker m2 shows the gm that is 0.8 times the top value. Using these measurements and gm=10 mS the drain current and the transistor width were scaled by a factor of α=1.039 and the final values were: $I_d = 1.38mA$ and $W = 31.17\mu m$.

2. **Design biasing circuit by choosing the size of transistor MB and Iref.**

   According to the textbook, the width of the bias MOSFET and the reference current can be chosen as 0.1 times the width and current of the M1 to provide the necessary bias and consume less power than the main branch.

3. **Choose C_{gs} and L_G to obtain impedance matching and resonance at working frequency.**

   From DC operating point: $C_{gs_1} = 37.6fF$ and $C_{gb1} = 6.77fF$.

   $$R_s = \frac{g_m L_s}{C_{gs}} \left(\frac{C_{gs}}{C_{gs}+C_{gb1}}\right)^2 = 50\Omega \rightarrow C_{gs} = 186.2fF$$

   Therefore the added capacitance should be 148.6 fF.

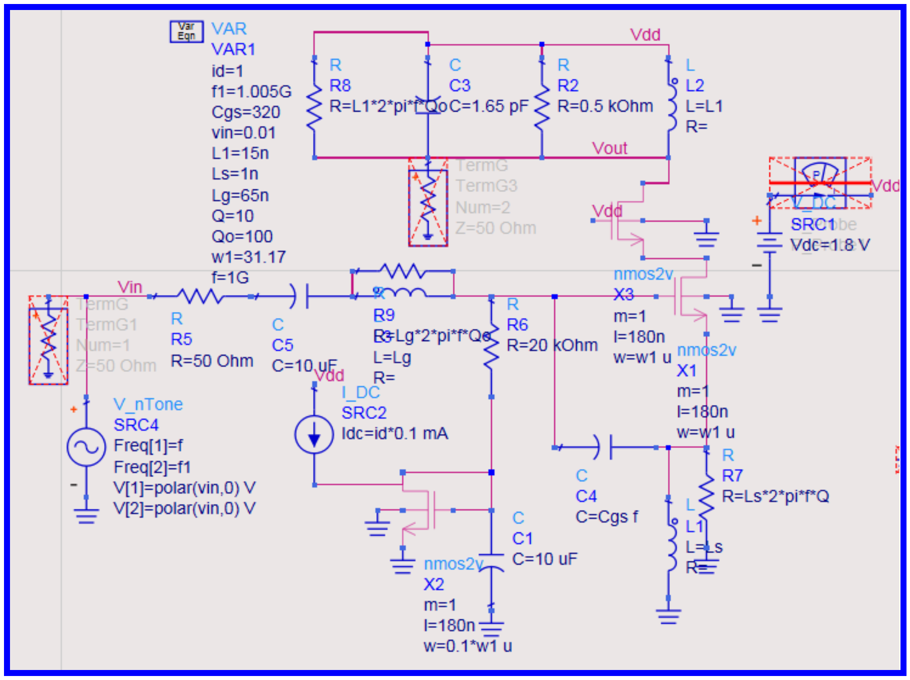
   $f_0 = \frac{1}{2\pi\sqrt{(C_{gs}+C_{gb1})(L_S+L_G)}} \rightarrow L_G = 131.2nH$ which means L_G has to be off-chip.

4. **Choose L_1 and C_d in the drain of the cascode transistor so that they resonate and yield the desired gain.**

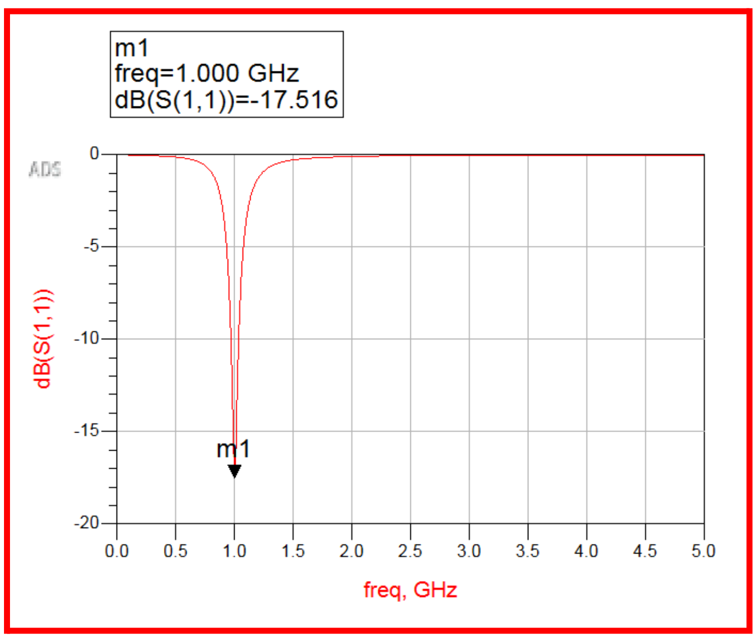
   L_1 was chosen to be 15nH and the drain capacitance was found to be 1.2pF so that they would resonate at the working frequency.

5. **Fine-tune the circuit until the desired S_{11} and NF are reached.**

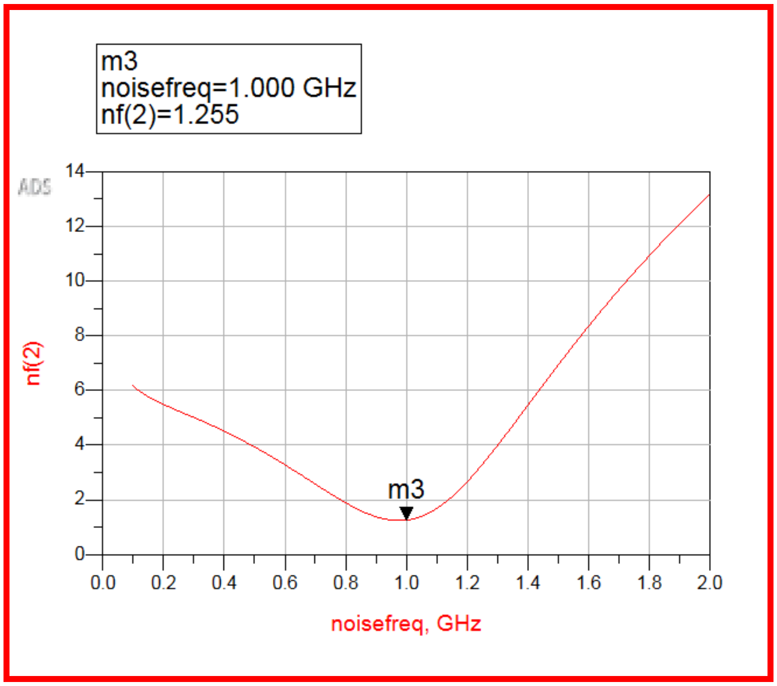
   After sweeping various parameters and simulating to check NF and s11, this circuit was determined to be the optimum design:



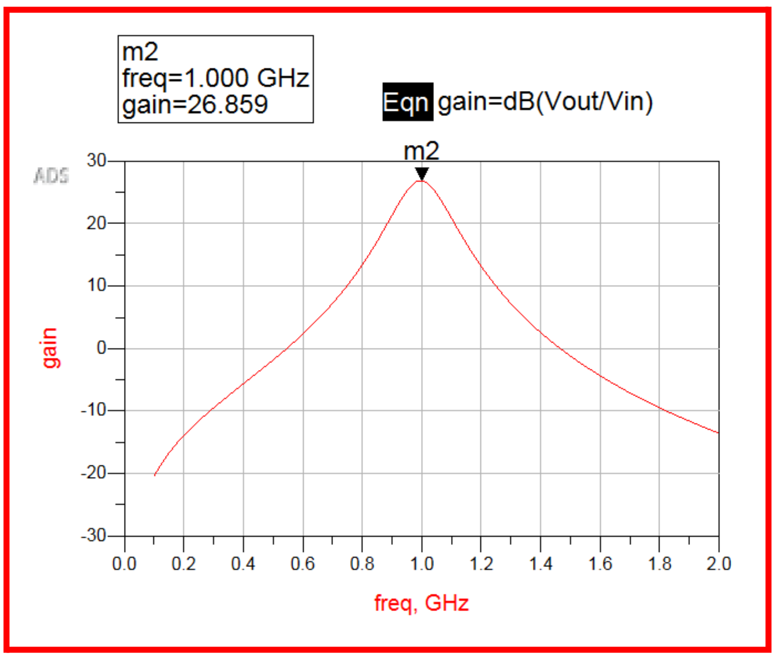
Picture 3- the final circuit schematic



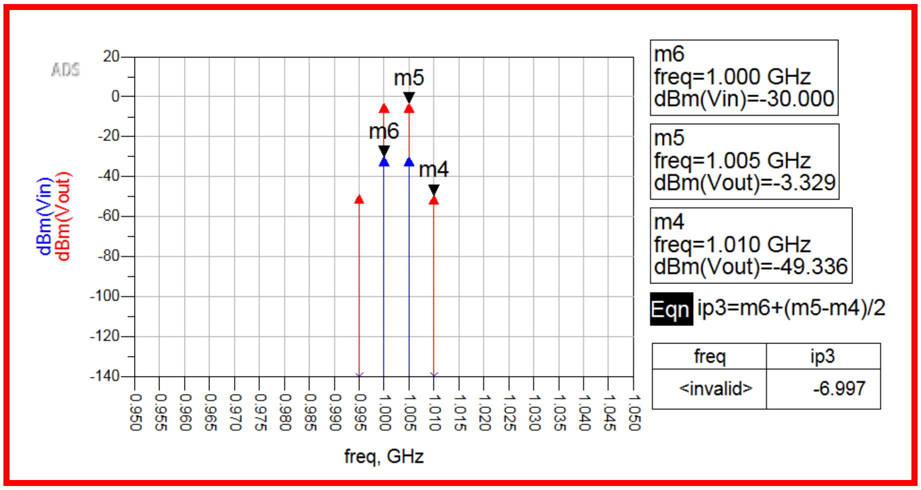
Picture 4- S_{11} vs. frequency



Picture 5- NF vs. frequency



Picture 6- gain vs. frequency



Picture 7- IIP3 calculations

S11 (dB)	NF (dB)	Gain (dB)	IIP3 (dBm)	Power (mW)
-17.51	1.25	26.85	-6.99	2

Knowns:

Assume center f = 20 GHz, $V_{DD} = 1.8V$, $R_s = 50\Omega$, $L = 180nm$, and $W_0 = 30\mu m$.

Assuming a wire-bond inductance of $L_s = 1nH$.

Steps:

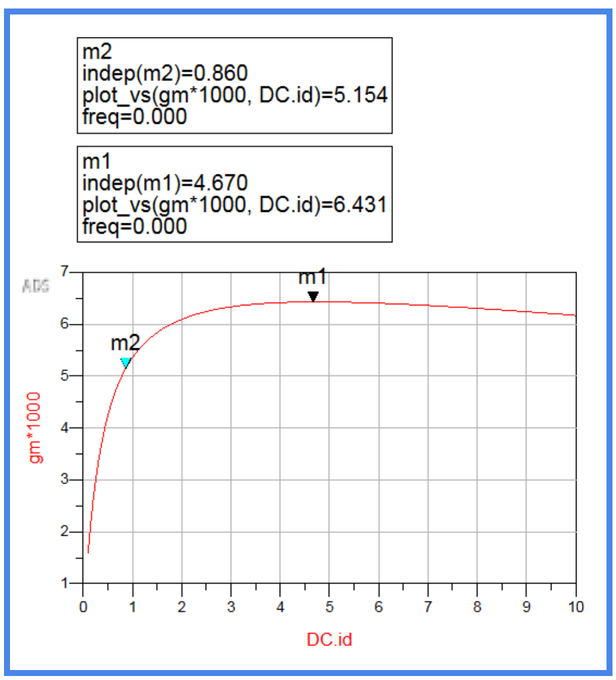
1. **Find L_G so that C_{gs1}, L_s and L_G resonate at $f = 20GHz$.**

   $$f_0 = \frac{1}{2\pi\sqrt{(L_s+L_G)C_{gs}}} \rightarrow L_G = 5nH$$

2. **Find g_m to ensure impedance matching.**

   $$R_s = \frac{g_m L_s}{C_{gs}} \rightarrow g_m = 0.527mS$$

3. **Plot g_m versus I_D and determine I_D to reach desired g_m.**



Picture 8- g_m vs. drain current for smaller width than first one

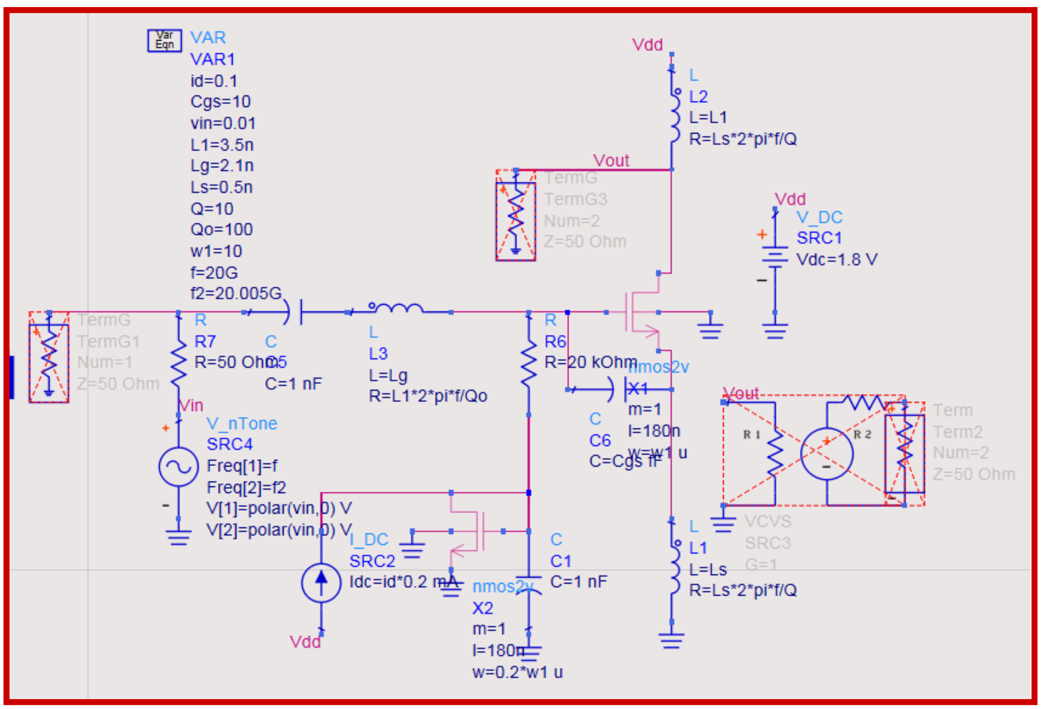
Marker m1 marks the chosen top value and marker m2 shows the gm that is 0.8 times the top value. Using these measurements to achieve the desired g_m the drain current and the transistor width were scaled by a factor of $\alpha = 0.1$ and the final values were: $I_d = 0.088mA$ and $W = 1.3\mu m$.

6. **Choose L_1 in the drain of the cascode transistor so that they yield the desired gain.**

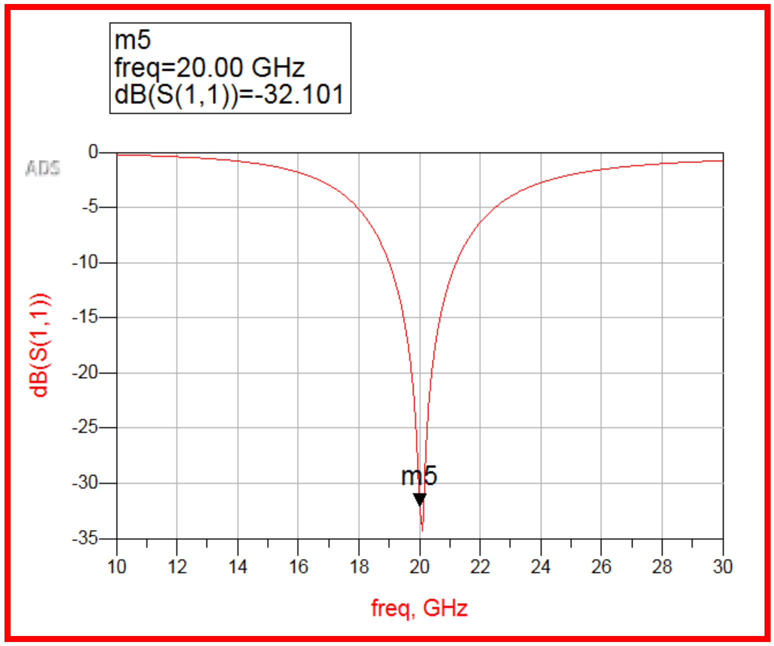
   L_1 was chosen to be 5nH.

7. **Fine-tune the circuit until the desired S_{11} and NF are reached.**

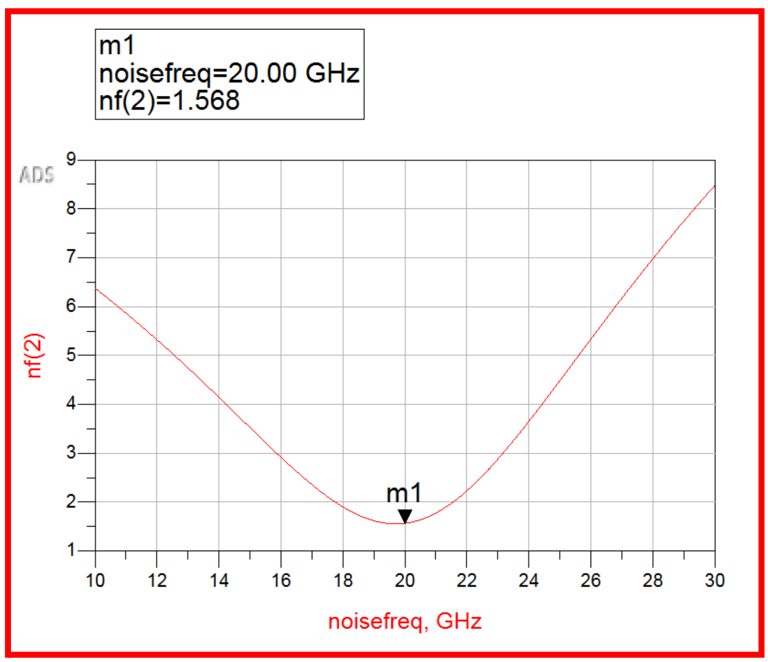
   After sweeping various parameters and simulating to check NF and s11, this circuit was determined to be the optimum design:



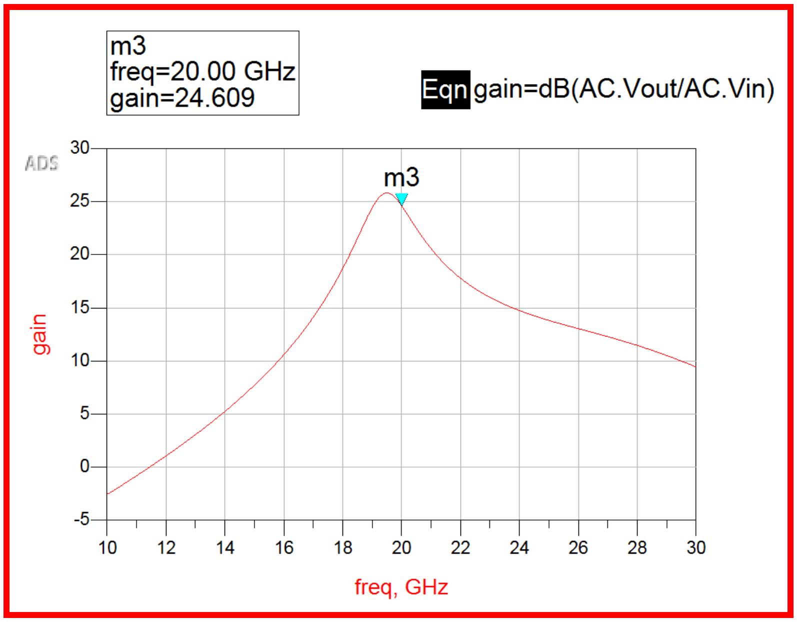
Picture 9- the final circuit schematic



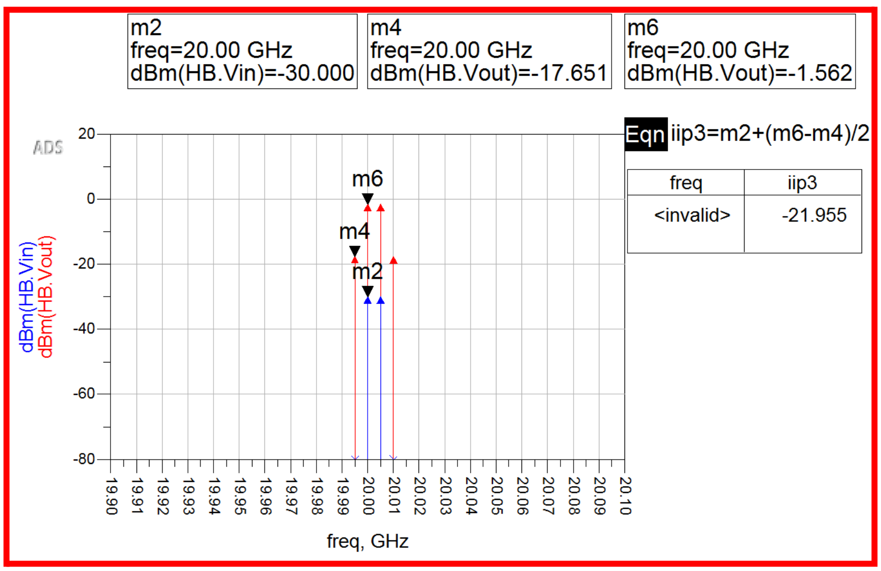
Picture 10- S_{11} vs. frequency



Picture 11- NF vs. frequency



Picture 12- gain vs. frequency



Picture 7- IIP3 calculations

S11 (dB)	NF (dB)	Gain (dB)	IIP3 (dBm)	P (mW)
-32.1	1.56	24.6	-21.9	0.406