Electrical Engineering Department

RFIC

mini-project

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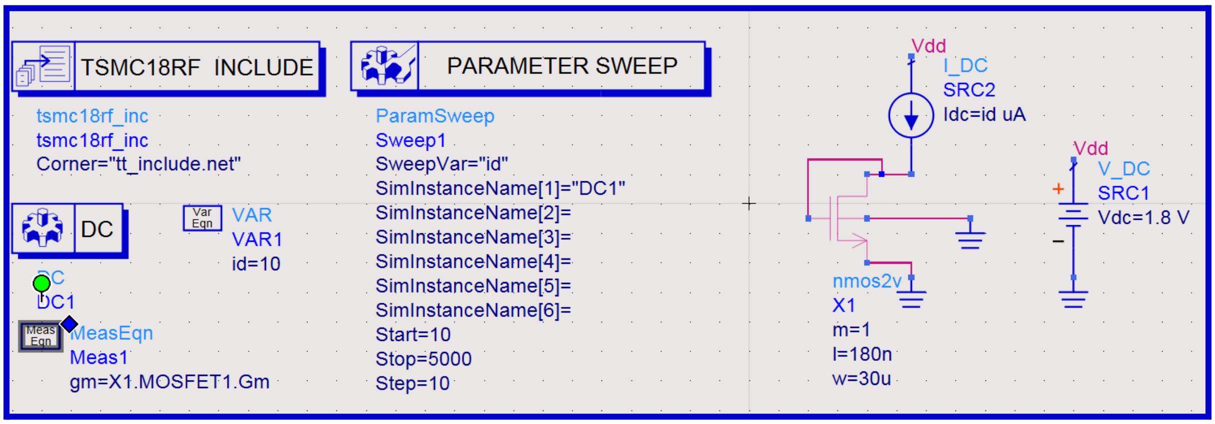
Design Procedure:

Knowns:

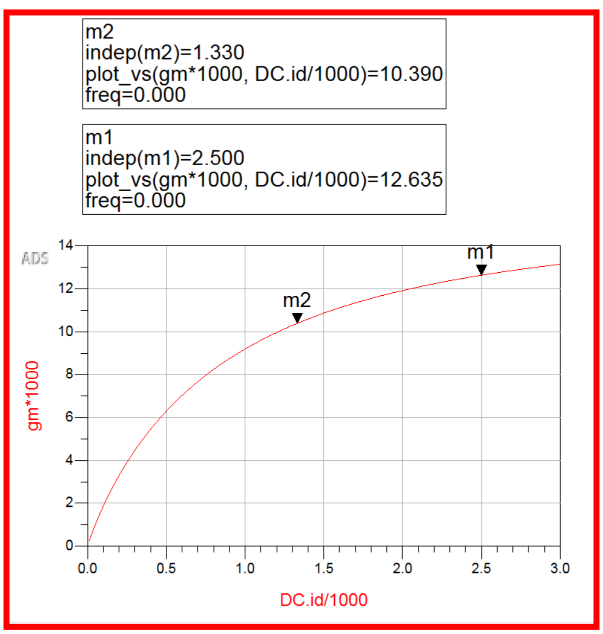
Assume center frequency = 2.4 GHz, VDD = 1.8 V, Rs = 50 Ohm, L = 180 nm, and W1 = 30 um.

Steps:

1. **Plot gm versus ID and determine ID so that gm = 1/Rs.**

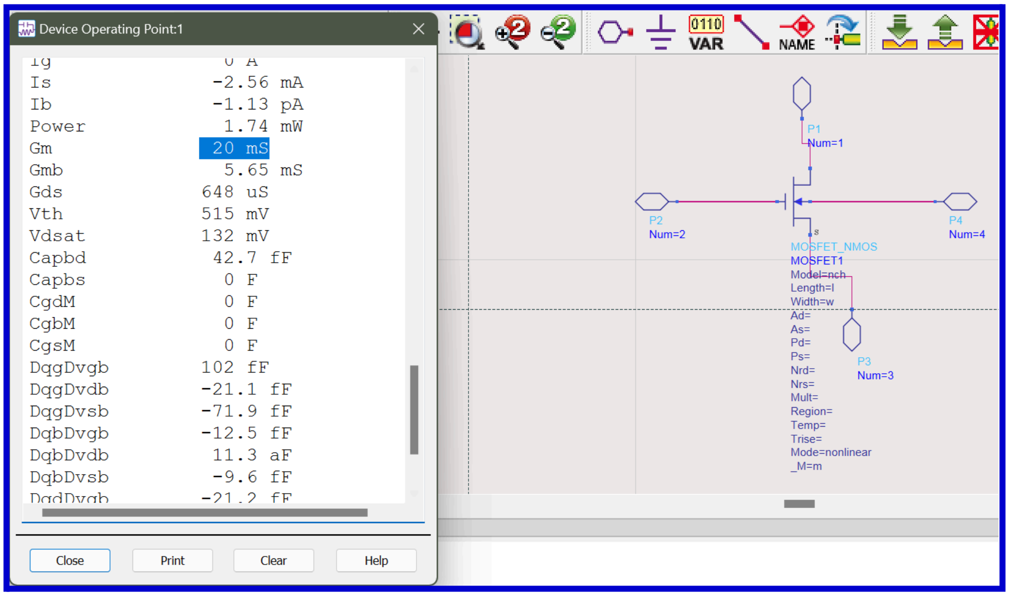


Picture 1 - the circuit schematic



Picture 2- g_m vs. drain current

Marker m1 marks the chosen top value and marker m2 shows the gm that is 0.8 times the top value. Using these measurements and considering the input impedance $R_S = 50\ \Omega$, to achieve $g_m = \frac{1}{50} = 20\ mS$ the drain current and the transistor width were scaled by a factor of $\alpha = 1.92$ and the final values were: $I_d = 2.56\ mA$ and $w = 57.74\ \mu m$.



Picture 3- MOSFET g_m after scaling

2. Determine LB and for Q = 10, determine Rp (parallel resistance of LB).

Using typical values for 180-n MOSFET technology ($C_{ox} = 9\frac{fF}{\mu^2}$, $C_{ov} = 0.2\frac{fF}{\mu^2}$, $E = 0.54\mu$, $C_j = 1.2\frac{fF}{\mu^2}$) the source capacitors were found to be:

$$C_{gs_1} = \frac{2}{3}C_{ox}WL + C_{ov}W = 72.9\ fF$$

$$C_{sb} = EWC_j = 36.9\ fF$$

Assuming a pad capacitance of 50fF, the necessary L_B for resonance at $f = 2.4GHz$ was found to be: $L_B = \frac{1}{\omega^2 C} = 27.52nH$

Therefore $R_p = QL\omega = 4.150k\Omega$.

3. **Design biasing circuit by choosing the size of transistor MB and Iref.**

   According to the textbook, the width of the bias MOSFET and the reference current can be chosen as 0.2 times the width and current of the M1 to provide the necessary bias and consume less power than the main branch.

4. **Determine the size of M2.**

   The width of M2 was chosen to be the same as M1 for the sake of simplicity.

5. **Determine R1 and L1 to obtain the mentioned gain. R1 is the parallel resistance of L1 with Q = 10.**

   For the necessary gain of 18dB or 8, using the simplified gain equation (by disregarding channel length modulation and body effect) $A_v = \frac{1}{2} g_m R_d$, the drain resistance was found to be 800 ohms. The load inductance has to resonate with the load capacitance which is assumed to be 50 fF and $C_{gd_2} + C_{db_2}$ which is calculated as:

   $C_{gd} = C_{ov} W = 11.4fF$, $C_{db} = C_{sb} = 36.9fF$

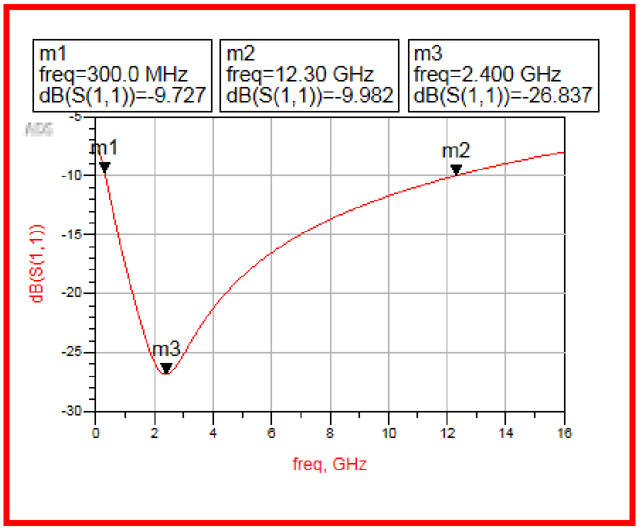
   So the load inductance is found to be: $L_1 = 44.73nH$.

   The parallel resistance with Q=10 is: $R_p = 6.75k\Omega$.

   To achieve the mentioned gain, a resistance of 900 ohms was placed in parallel to the load inductance.

6. **Plot S11 versus frequency and specify BW (S11 < -10 dB).**

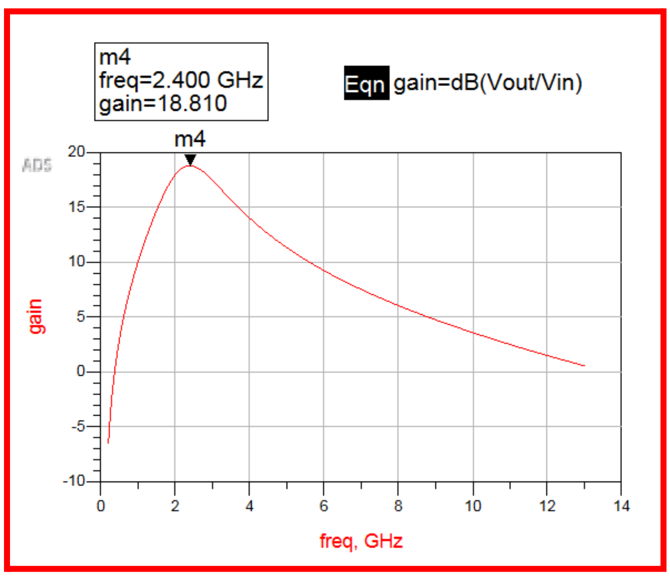
   The s11 plot shows that the bandwidth of the circuit is acceptable but it is not centered at 2.4GHz. The center frequency was corrected by changing the L_B to 25nH. The bandwidth is then equal to 12GHz.



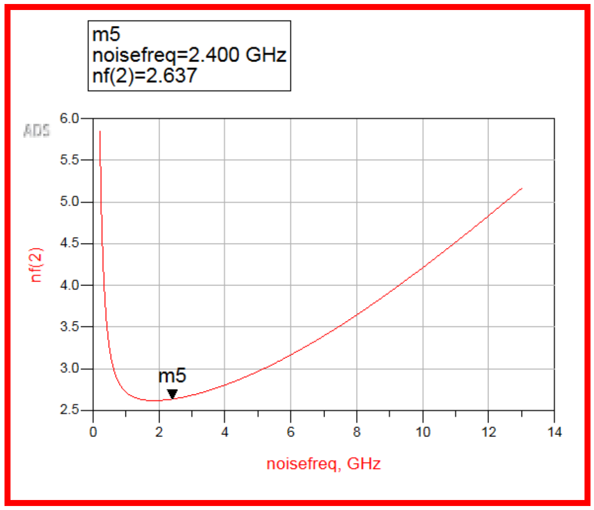
Picture 5- s11 vs frequency, m3 marks the center frequency

7. Plot NF and gain in specified BW.

L1 needed to be tuned a little so that the center frequency of the gain would fall at 2.4 GHz.



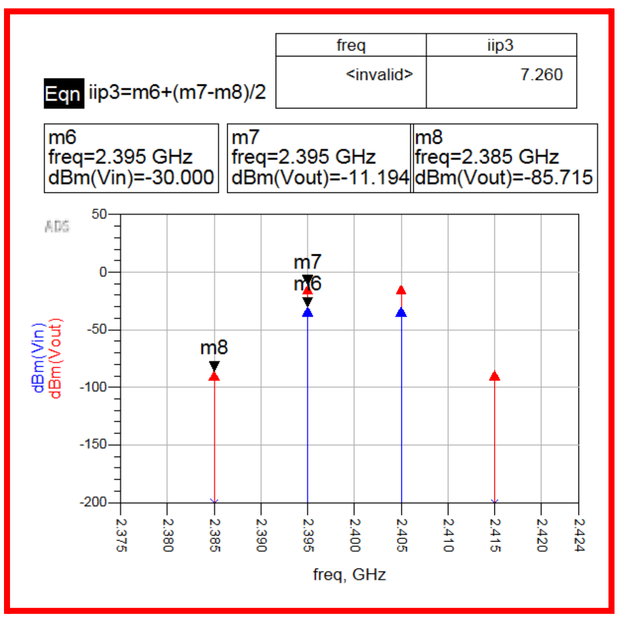
Picture 6- gain vs. frequency



Picture 7- noise figure vs. frequency

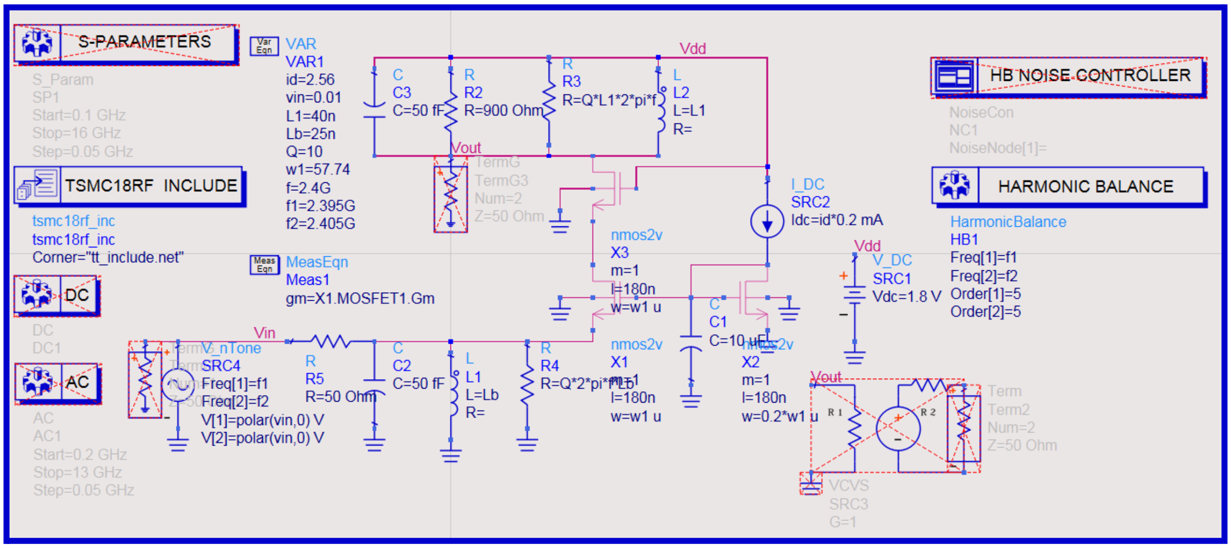
8. Determine IIP3.

To calculate IIP3, 2 tones at frequencies 2.395 and 2.405 GHz with input power of -30dBm were submitted to the circuit and the IIP3 was determined to be 7.26dBm.



Picture 8- IIP3 calculations

Final circuit



Final results

bandwidth	12 GHz
gain	18.8 dB
NF	2.6
IIP3	7.26 dBm