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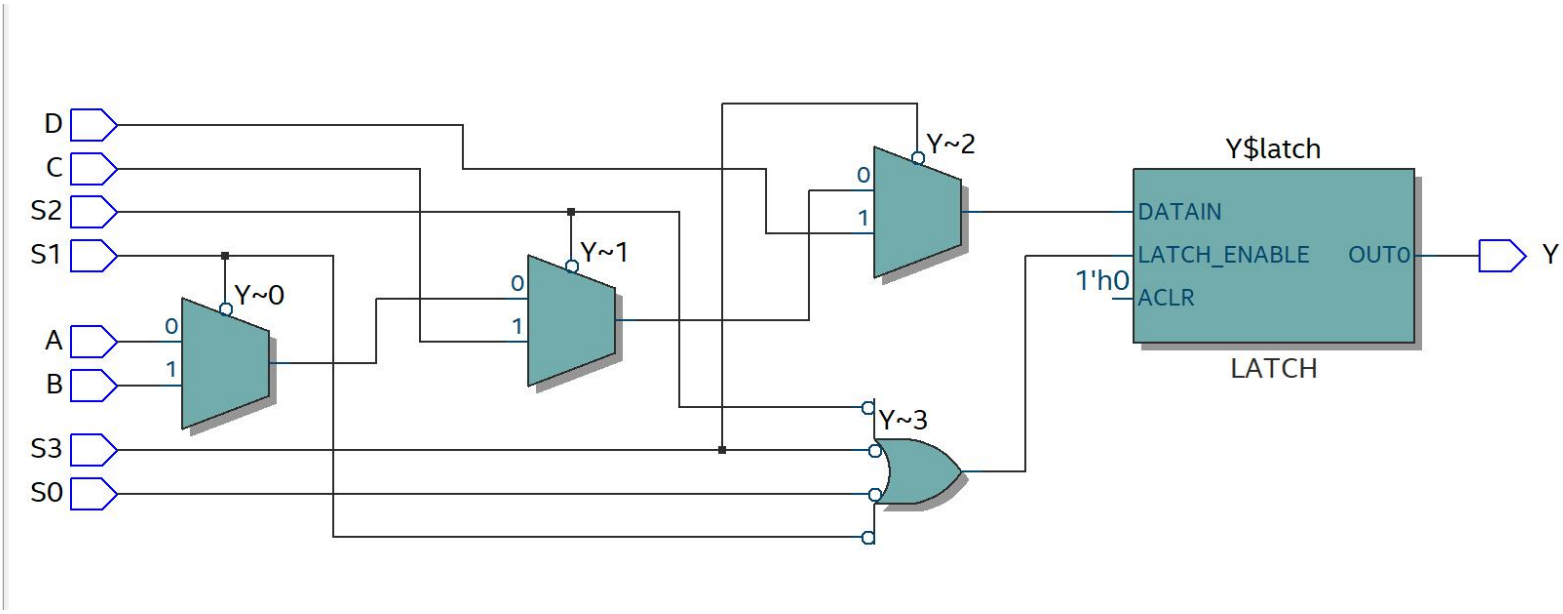
EDA-3-6：

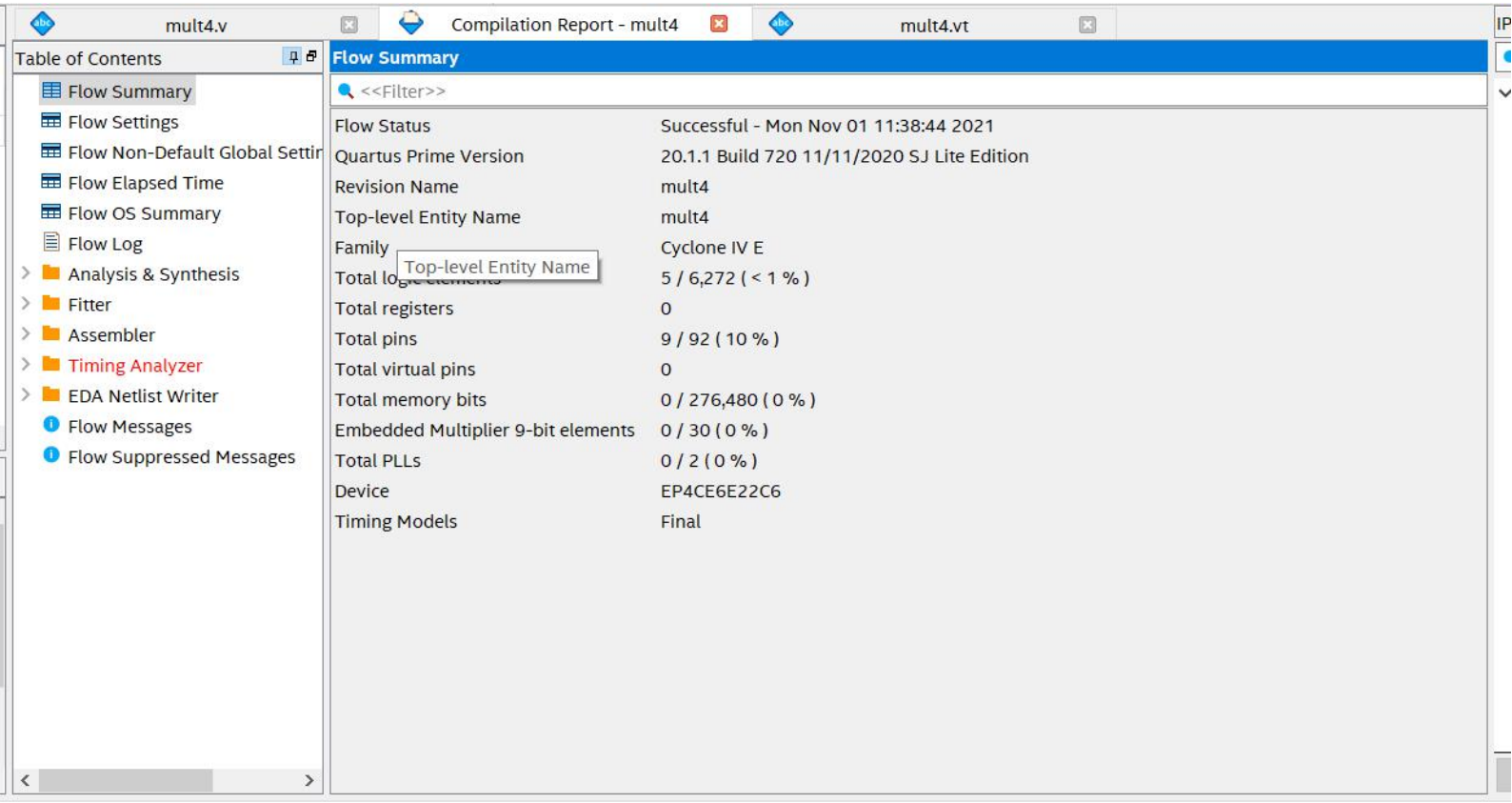
代码文件：

```
module mult4 (S0,S1,S2,S3,A,B,C,D,Y);
    input S0,S1,S2,S3,A,B,C,D;
    output Y;
    reg Y;
    always@(S0,S1,S2,S3,A,B,C,D)
        begin
            if (S0==0) Y=A;
            if (S1==0) Y=B;
            if (S2==0) Y=C;
            if (S3==0) Y=D;
        end
Endmodule
```

网表文件：



资源开销：



仿真文件：

```
`timescale 1 ps/ 1 ps
module mult4_vlg_tst();
// constants
// general purpose registers

reg A;
reg B;
reg C;
reg D;
reg S0;
reg S1;
reg S2;
reg S3;
// wires
wire Y;

// assign statements (if any)
mult4 i1 (
// port map - connection between master ports and signals/registers
	.A(A),
	.B(B),
	.C(C),
	.D(D),
	.S0(S0),
	.S1(S1),
	.S2(S2),
	.S3(S3),
	.Y(Y)
);
initial
begin
```

```
// code that executes only once
// insert code here --> begin
#0 A=1'b0;
#0 B=1'b0;
#0 C=1'b0;
#0 D=1'b0;
#0 S1=1'b0;
#0 S2=1'b0;
#0 S3=1'b0;
#0 S0=1'b0;

// --> end
$display("Running testbench");
end
always #1 A=~A;
always #2 B=~B;
always #3 C=~C;
always #4 D=~D;
always #5 S0=~S0;
always #6 S1=~S1;
always #7 S2=~S2;
always #8 S3=~S3;

always@(Y);
endmodule
```

仿真结果：