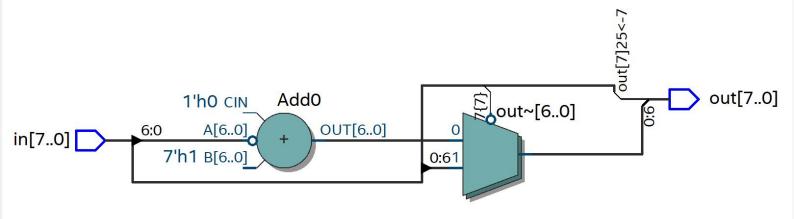
## 崔浩然 <mark>2020302181062</mark>

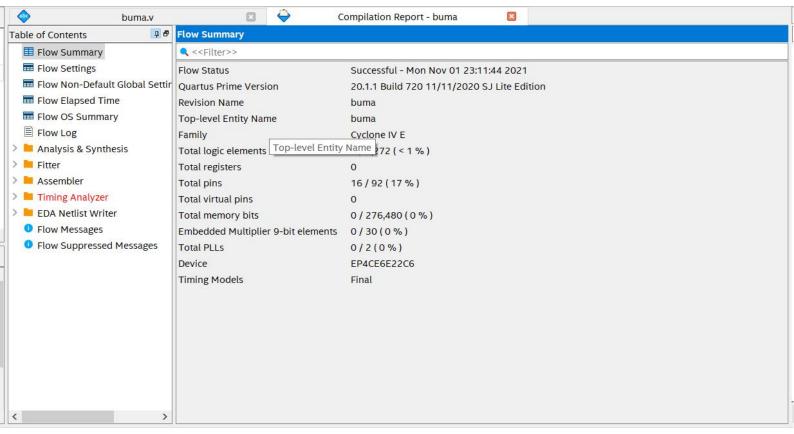
## EDA-3-10

```
代码文件:
module buma (in,out);
   input [7:0] in;
   output[7:0] out;
   reg[7:0] out;
   reg[6:0] a;//a,符号位外的低 7 位
   always@(in)
       begin: bu
           if (in[7]==0) out<=in;
           else begin: bum
               a=(~in[6:0]+1);
               out[7]=in[7];
               out[6:0]=a;//~in[6:0]+1;
                 end
       end
Endmodule
```

## 图表文件:



资源开销:



```
仿真文件:
`timescale 1 ps/ 1 ps
module buma_vlg_tst();
// constants
// general purpose registers
//reg eachvec;
// test vector input registers
reg [7:0] in;
// wires
wire [7:0] out;
// assign statements (if any)
buma i1 (
// port map - connection between master ports and signals/registers
    .in(in),
    .out(out)
);
initial
begin
// code that executes only once
// insert code here --> begin
#0 in=8'b00000000;
// --> end
$display("Running testbench");
end
always #5 in=in+1;
// optional sensitivity list
// @(event1 or event2 or .... eventn)
//begin
// code executes for every event on sensitivity list
```

// insert code here --> begin

//@eachvec; // --> end //end Endmodule

## 仿真结果:

