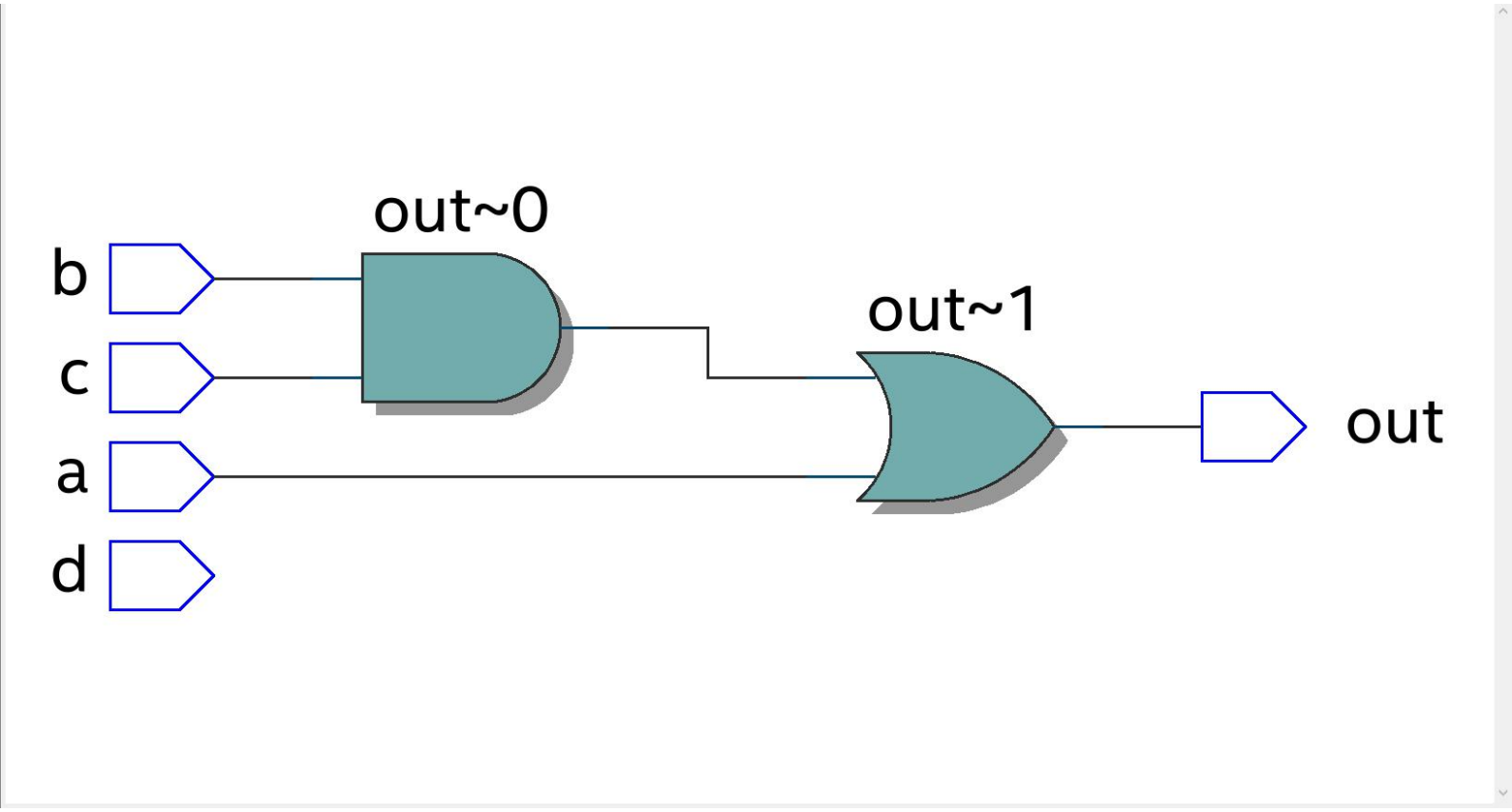
崔浩然
2020302181062

EDA-3-8：

代码文件：

```
module bcd8421 (a,b,c,d,out);
    input a,b,c,d;
    output out;
    assign out=(b&c)|a;
Endmodule
```

图表文件：



资源开销：

bcd8421.v | Compilation Report - bcd8421 | bcd8421.vt

Table of Contents

- Flow Summary
- Flow Settings
- Flow Non-Default Global Settir
- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Fitter
- Assembler
- Timing Analyzer
- EDA Netlist Writer
- Flow Messages
- Flow Suppressed Messages

Flow Summary

<<Filter>>

Flow Status	Successful - Mon Nov 01 17:44:56 2021
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	bcd8421
Top-level Entity Name	bcd8421
Family	Cyclone IV E
Total logic elements	1 / 6,272 (< 1 %)
Total registers	0
Total pins	5 / 92 (5 %)
Total virtual pins	0
Total memory bits	0 / 276,480 (0 %)
Embedded Multiplier 9-bit elements	0 / 30 (0 %)
Total PLLs	0 / 2 (0 %)
Device	EP4CE6E22C6
Timing Models	Final

仿真文件：

```
`timescale 1 ps/ 1 ps
module bcd8421_vlg_tst();
// constants
// general purpose registers
//reg eachvec;
// test vector input registers
reg a;
reg b;
reg c;
reg d;
// wires
wire out;

// assign statements (if any)
bcd8421 i1 (
// port map - connection between master ports and signals/registers
    .a(a),
    .b(b),
    .c(c),
    .d(d),
    .out(out)
);
initial
begin
// code that executes only once
// insert code here --> begin
#0 a=1'b0;
#0 b=1'b0;
#0 c=1'b0;
#0 d=1'b0;
// --> end
```

```
$display("Running testbench");
end
always #1 a=~a;
always #2 b=~b;
always #4 c=~c;
always #8 d=~d;
always@(out);
// optional sensitivity list
// @(event1 or event2 or .... eventn)
//begin
// code executes for every event on sensitivity list
// insert code here --> begin

//@eachvec;
// --> end
//end
endmodule
```

仿真结果：