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2020302181062

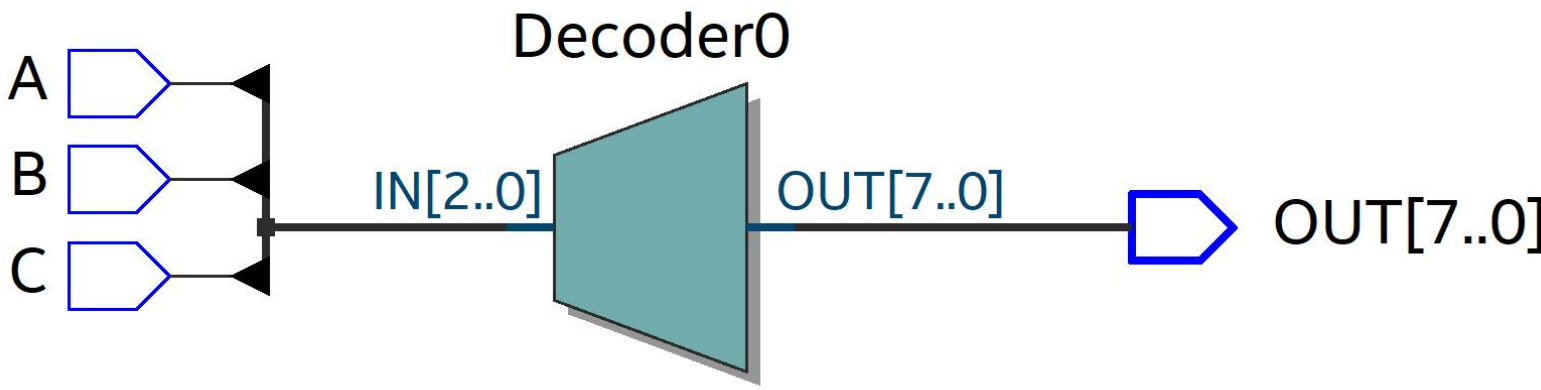
EDA 3-4

Case：

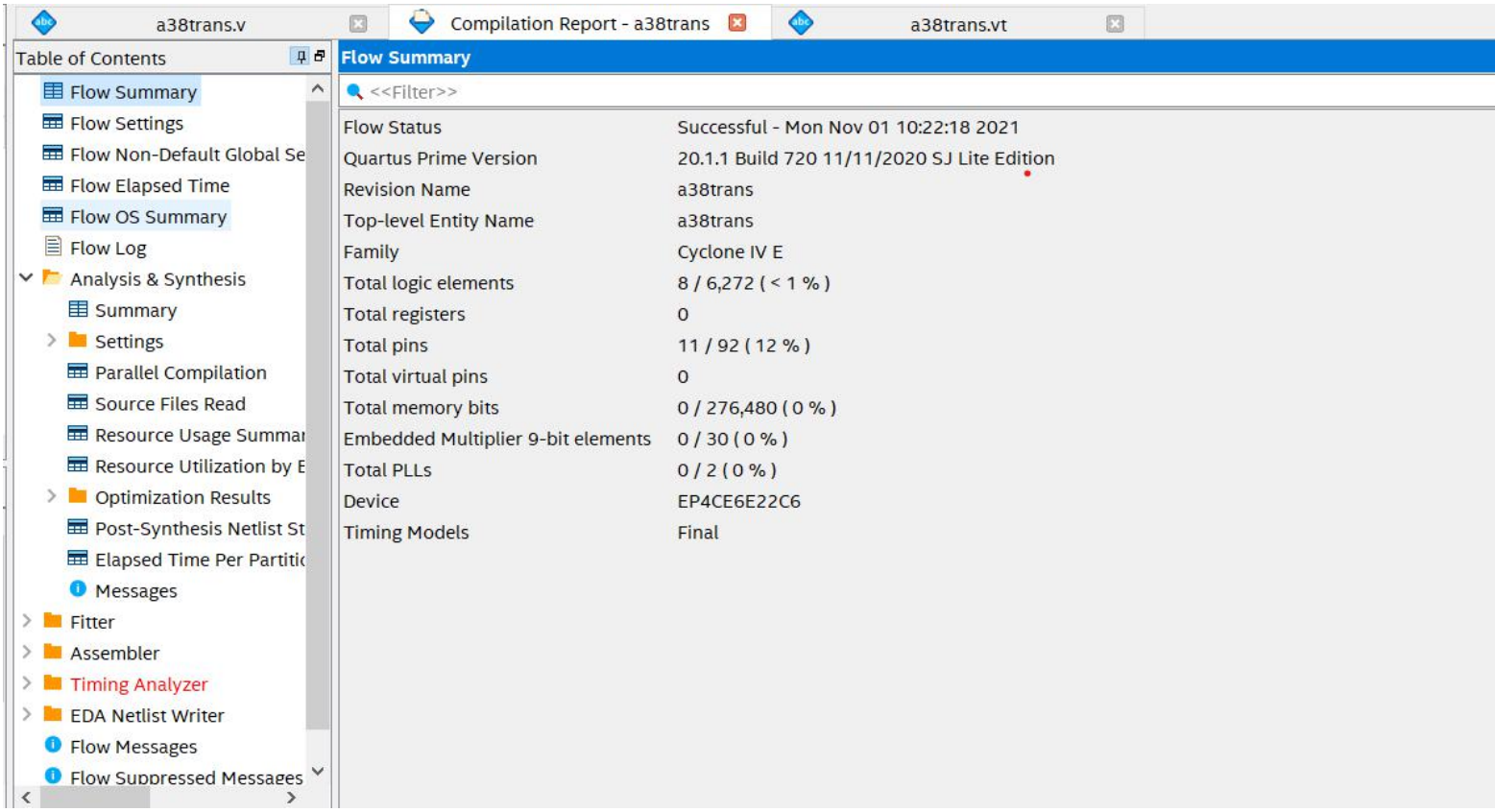
代码文件：

```
module a38trans(A,B,C,OUT);
  input A,B,C;
  output[7:0] OUT;
  reg[7:0] OUT;
  always@(A,B,C,OUT)
     begin:   a38trans
        case({A,B,C})
            3'b000: OUT<=8'b00000001;
            3'b001: OUT<=8'b00000010;
            3'b010: OUT<=8'b00000100;
            3'b011: OUT<=8'b00001000;
            3'b100: OUT<=8'b00010000;
            3'b101: OUT<=8'b00100000;
            3'b110: OUT<=8'b01000000;
            3'b111: OUT<=8'b10000000;
        endcase
     end
Endmodule
```

网表文件：



资源开销：

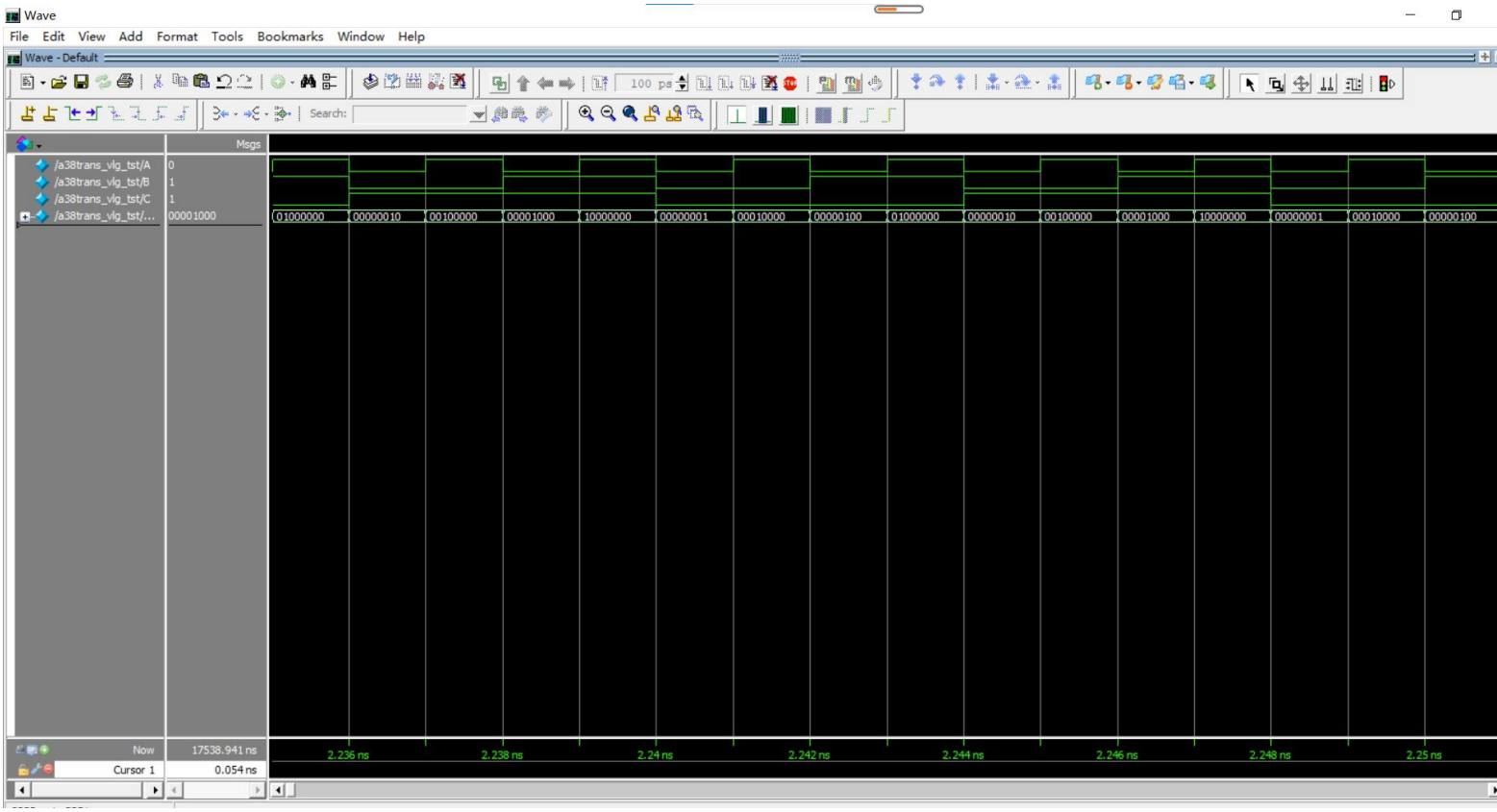


仿真文件：

```
`timescale 1 ns/ 1 ps
module a38trans_vlg_tst();
// constants
// general purpose registers
// test vector input registers
reg A;
reg B;
reg C;
// wires
wire [7:0]  OUT;

// assign statements (if any)
a38trans i1 (
// port map - connection between master ports and signals/registers
  .A(A),
  .B(B),
  .C(C),
  .OUT(OUT)
);
initial
begin
// code that executes only once
// insert code here --> begin
#0 A=1'b0;
#0 B=1'b0;
#0 C=1'b0;
// --> end
$display("Running testbench");
end
```

```
  always #1 A=~A;
  always #2 B=~B;
  always #4 C=~C;

 always @(OUT);
 // optional sensitivity list
 // @(event1 or event2 or .... eventn)
 Endmodule
```

仿真结果：

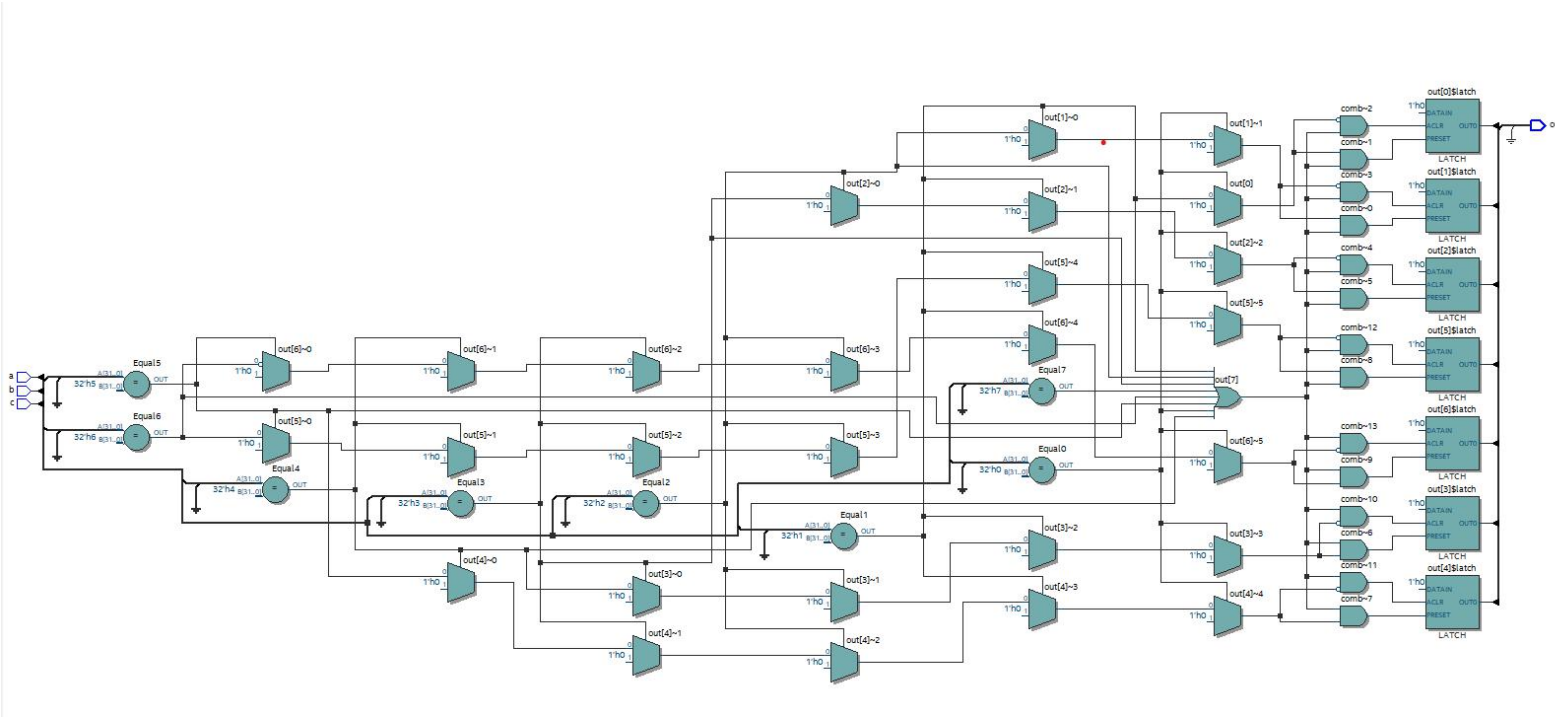


If-else：

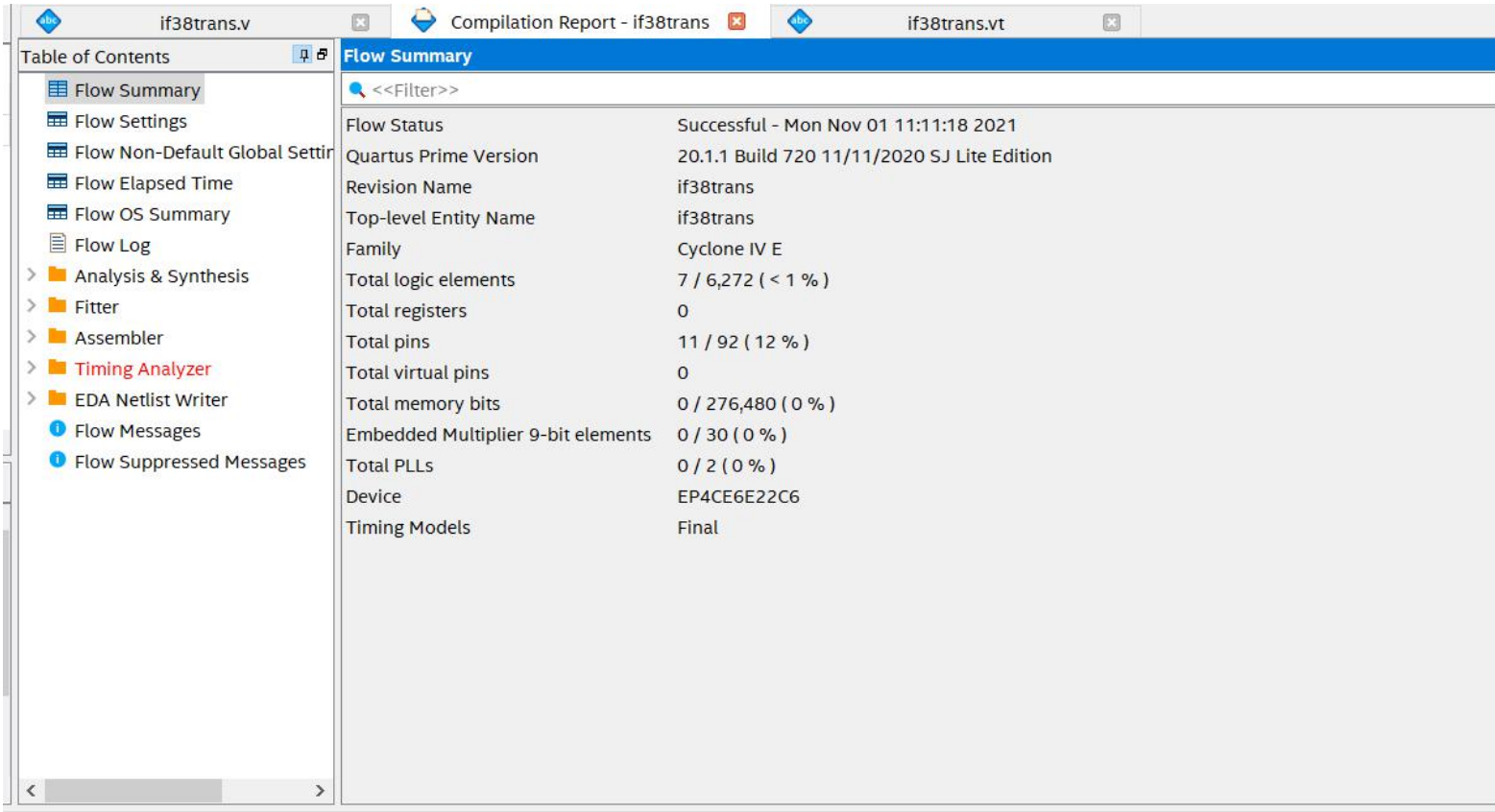
代码文件：

```
 module if38trans (a,b,c,out);
  input a,b,c;
  output[7:0] out;
  reg[7:0] out;
  reg[2:0] sel;
  always@(a,b,c,out)
     begin
         sel={a,b,c};
         if(sel==0) out=8'b00000000;
         else if (sel==1) out<=8'b00000001;
         else if (sel==2) out<=8'b00000010;
         else if (sel==3) out<=8'b00000100;
         else if (sel==4) out<=8'b00001000;
         else if (sel==5) out<=8'b00010000;
         else if (sel==6) out<=8'b00100000;
         else if (sel==7) out<=8'b01000000;
         else if (sel==8) out<=8'b10000000;
     end
 Endmodule
```

网表文件：



资源开销：

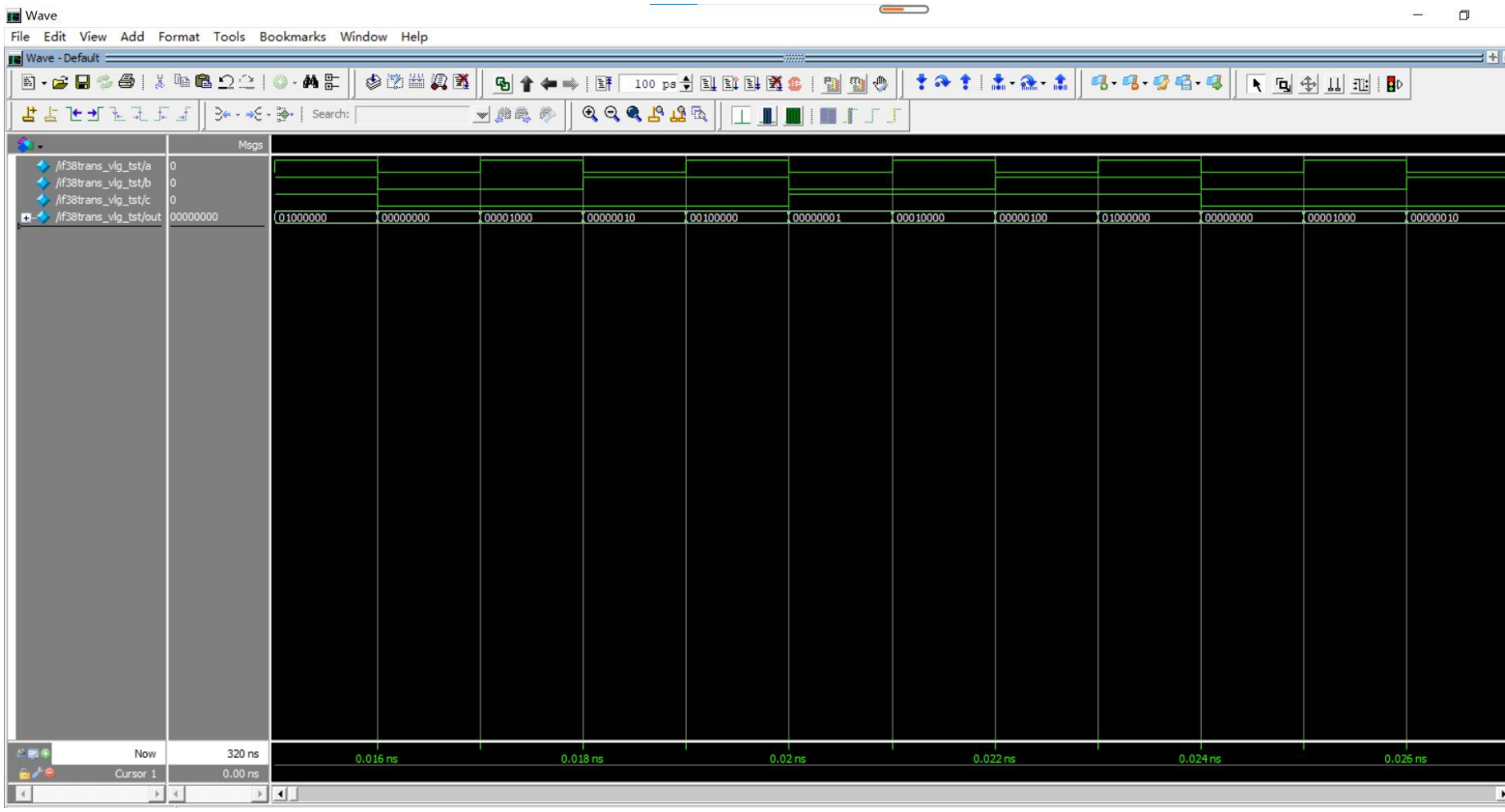


仿真文件：

```
`timescale 1 ps/ 1 ps
module if38trans_vlg_tst();

reg a;
reg b;
reg c;
// wires
wire [7:0]  out;
```

```
// assign statements (if any)
if38trans i1 (
// port map - connection between master ports and signals/registers
  .a(a),
  .b(b),
  .c(c),
  .out(out)
);
initial
begin
// code that executes only once
// insert code here --> begin
#0 a=1'b0;
#0 b=1'b0;
#0 c=1'b0;
// --> end
$display("Running testbench");
end
always #1 a=~a;
always #2 b=~b;
always #4 c=~c;

always@(out);
// --> end
endmodule
```

仿真结果：

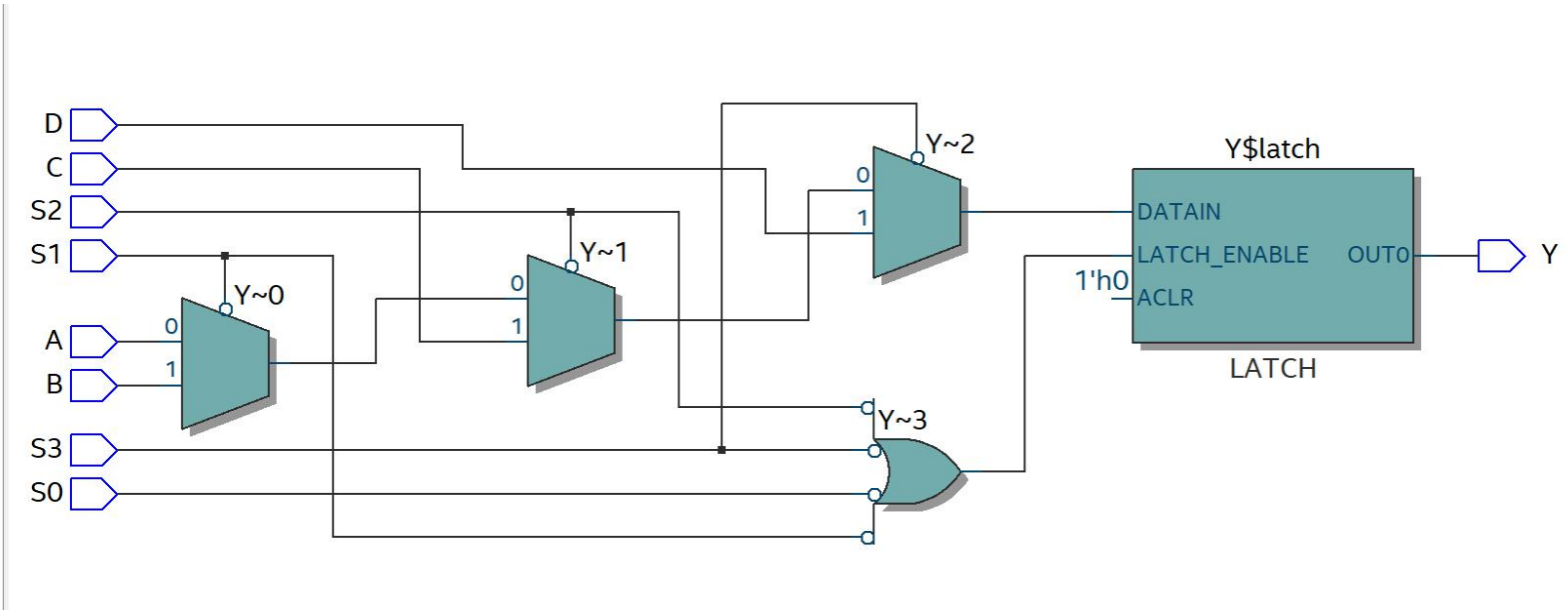


EDA-3-6：

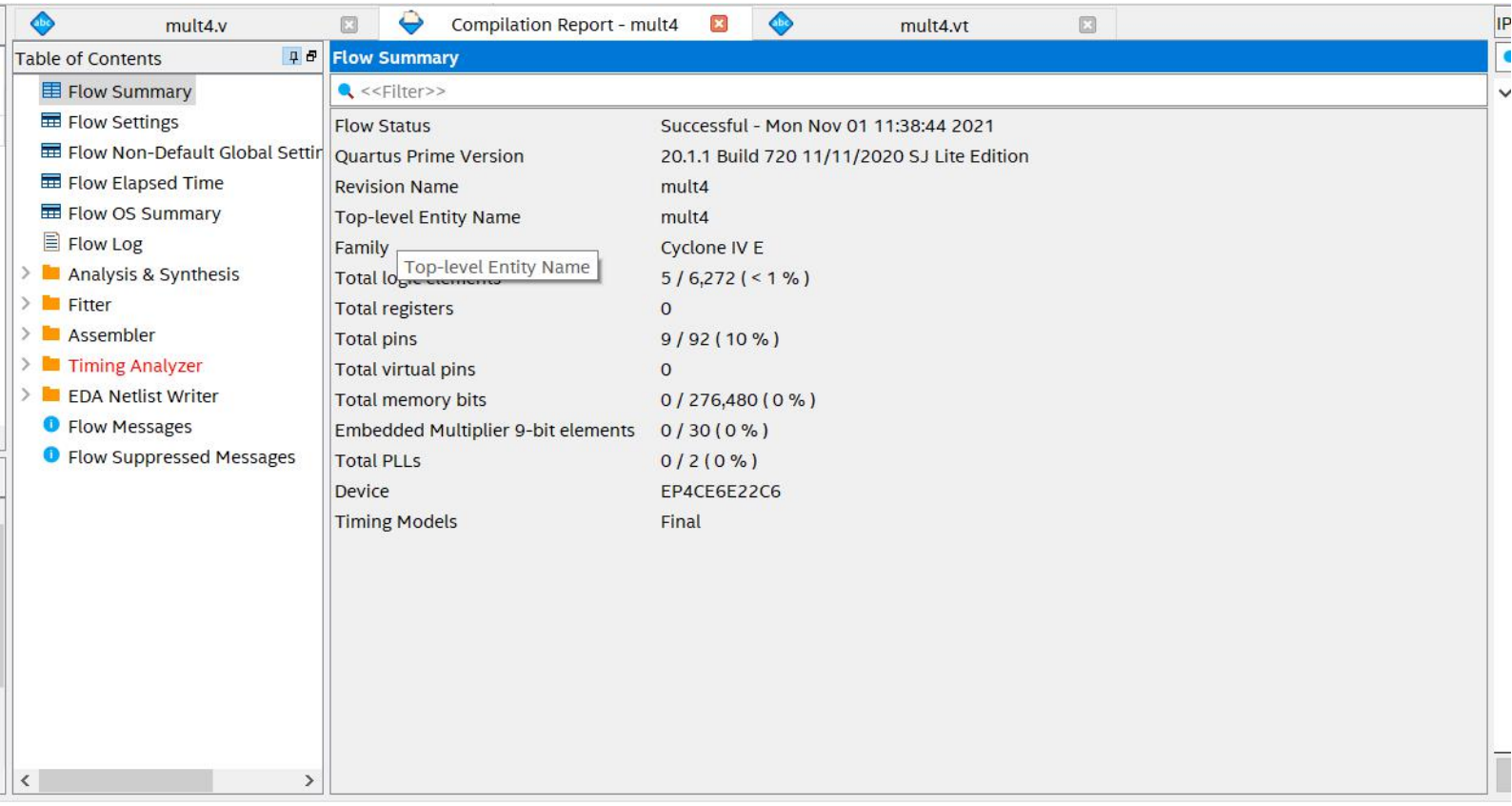
代码文件：

```
module mult4 (S0,S1,S2,S3,A,B,C,D,Y);
    input S0,S1,S2,S3,A,B,C,D;
    output Y;
    reg Y;
    always@(S0,S1,S2,S3,A,B,C,D)
        begin
            if (S0==0) Y=A;
            if (S1==0) Y=B;
            if (S2==0) Y=C;
            if (S3==0) Y=D;
        end
Endmodule
```

网表文件：



资源开销：

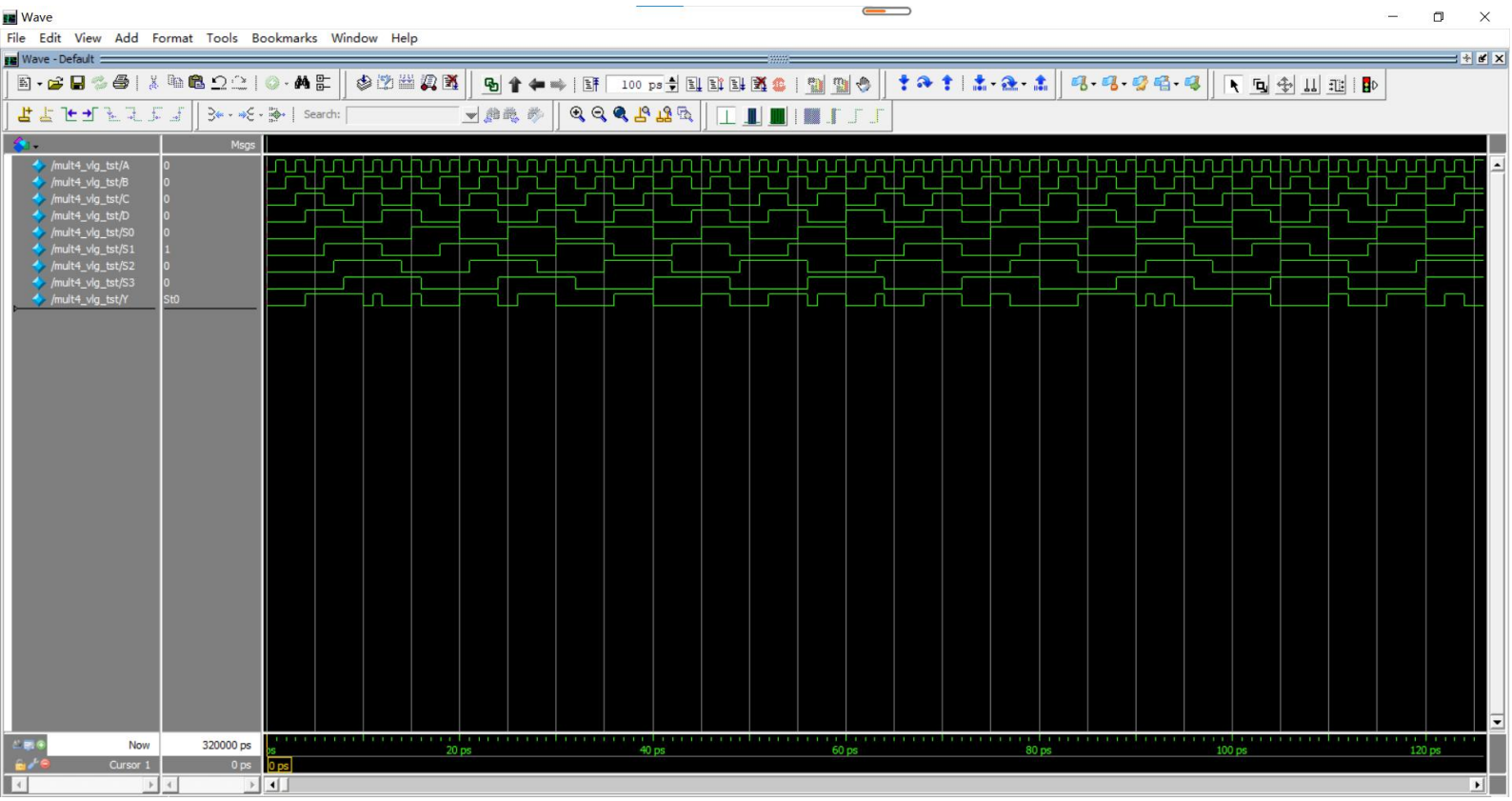


仿真文件：

```
`timescale 1 ps/ 1 ps
module mult4_vlg_tst();
// constants
// general purpose registers

reg A;
reg B;
reg C;
reg D;
reg S0;
reg S1;
reg S2;
reg S3;
// wires
wire Y;

// assign statements (if any)
mult4 i1 (
// port map - connection between master ports and signals/registers
    .A(A),
    .B(B),
    .C(C),
    .D(D),
    .S0(S0),
    .S1(S1),
    .S2(S2),
    .S3(S3),
    .Y(Y)
);
initial
begin
// code that executes only once
// insert code here --> begin
#0 A=1'b0;
#0 B=1'b0;
#0 C=1'b0;
#0 D=1'b0;
#0 S1=1'b0;
#0 S2=1'b0;
#0 S3=1'b0;
#0 S0=1'b0;

// --> end
$display("Running testbench");
end
always #1 A=~A;
always #2 B=~B;
always #3 C=~C;
always #4 D=~D;
always #5 S0=~S0;
always #6 S1=~S1;
always #7 S2=~S2;
```

```
always #8 S3=~S3;

always@(Y);
endmodule
```

仿真结果：

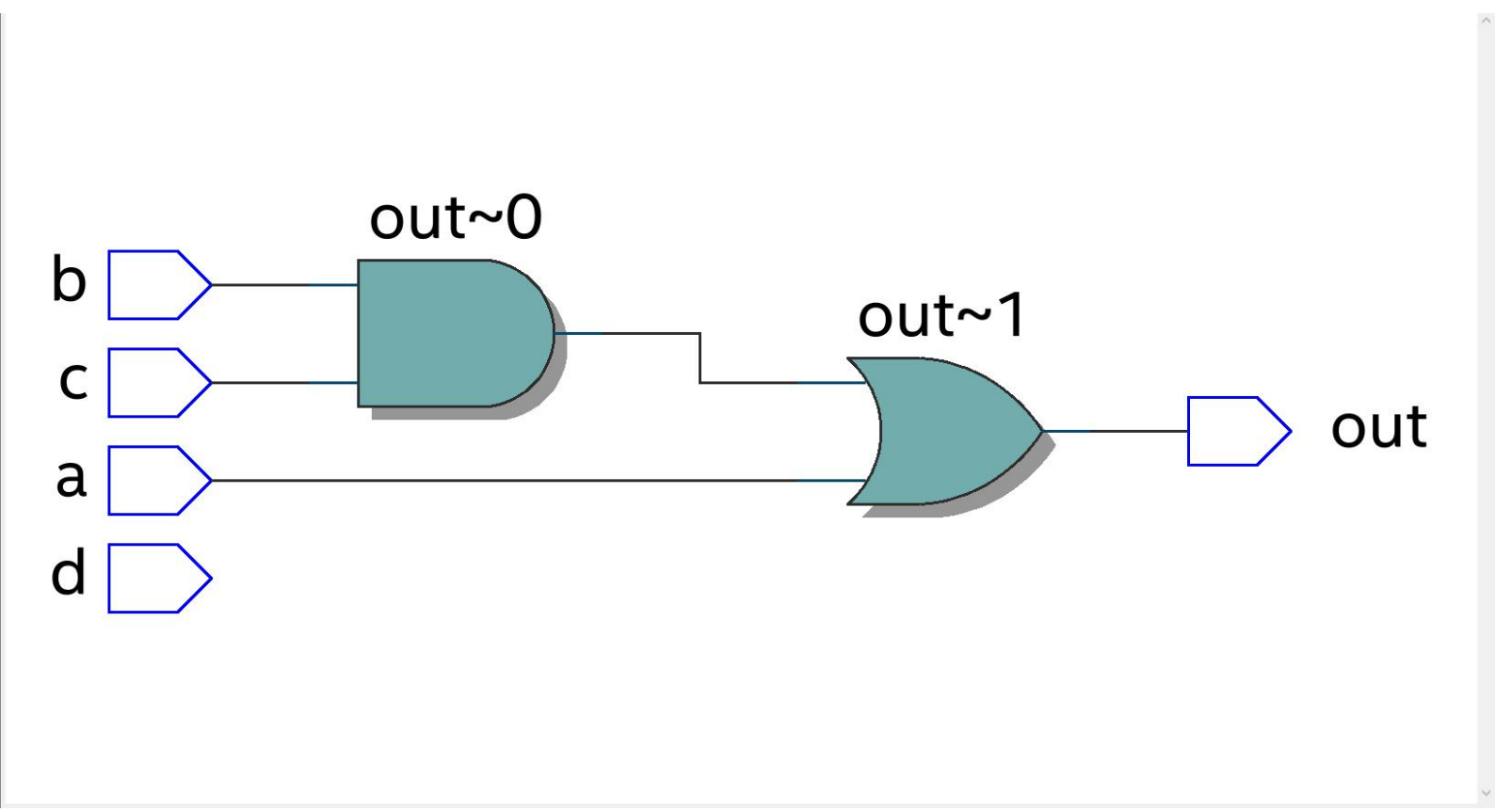


EDA-3-8：

代码文件：

```
module bcd8421 (a,b,c,d,out);
    input a,b,c,d;
    output out;
    assign out=(b&c)|a;
Endmodule
```

图表文件：



资源开销：

bcd8421.v | Compilation Report - bcd8421 | bcd8421.vt

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Flow Summary

<<Filter>>

Flow Status	Successful - Mon Nov 01 17:44:56 2021
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	bcd8421
Top-level Entity Name	bcd8421
Family	Cyclone IV E
Total logic elements	1 / 6,272 (< 1 %)
Total registers	0
Total pins	5 / 92 (5 %)
Total virtual pins	0
Total memory bits	0 / 276,480 (0 %)
Embedded Multiplier 9-bit elements	0 / 30 (0 %)
Total PLLs	0 / 2 (0 %)
Device	EP4CE6E22C6
Timing Models	Final

仿真文件：

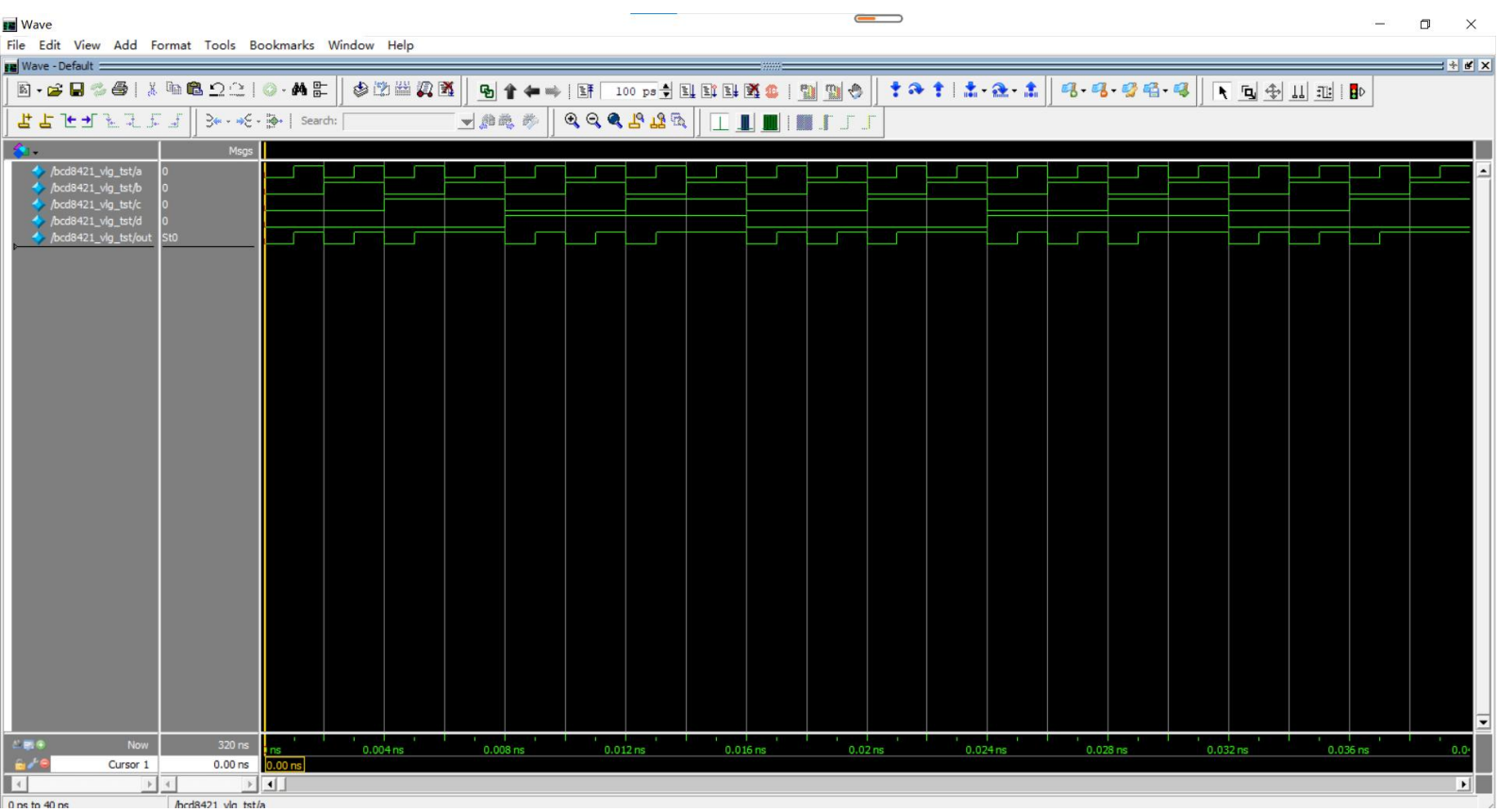
```
`timescale 1 ps/ 1 ps
module bcd8421_vlg_tst();
// constants
// general purpose registers
//reg eachvec;
// test vector input registers
reg a;
reg b;
reg c;
```

```
reg d;
// wires
wire out;

// assign statements (if any)
bcd8421 i1 (
// port map - connection between master ports and signals/registers
    .a(a),
    .b(b),
    .c(c),
    .d(d),
    .out(out)
);
initial
begin
// code that executes only once
// insert code here --> begin
#0 a=1'b0;
#0 b=1'b0;
#0 c=1'b0;
#0 d=1'b0;
// --> end
$display("Running testbench");
end
always #1 a=~a;
always #2 b=~b;
always #4 c=~c;
always #8 d=~d;
always@(out);
// optional sensitivity list
// @(event1 or event2 or .... eventn)
//begin
// code executes for every event on sensitivity list
// insert code here --> begin

//@eachvec;
// --> end
//end
endmodule
```

仿真结果：

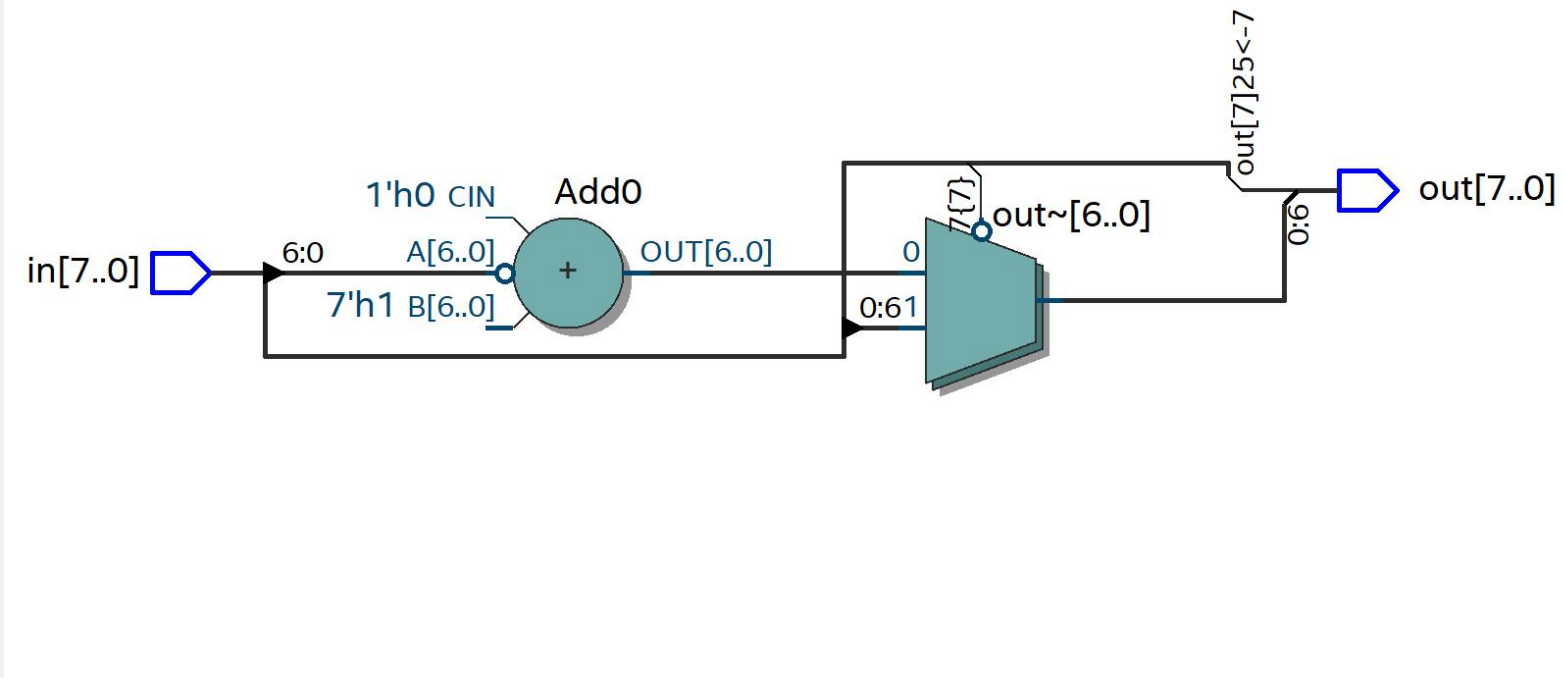


EDA-3-10

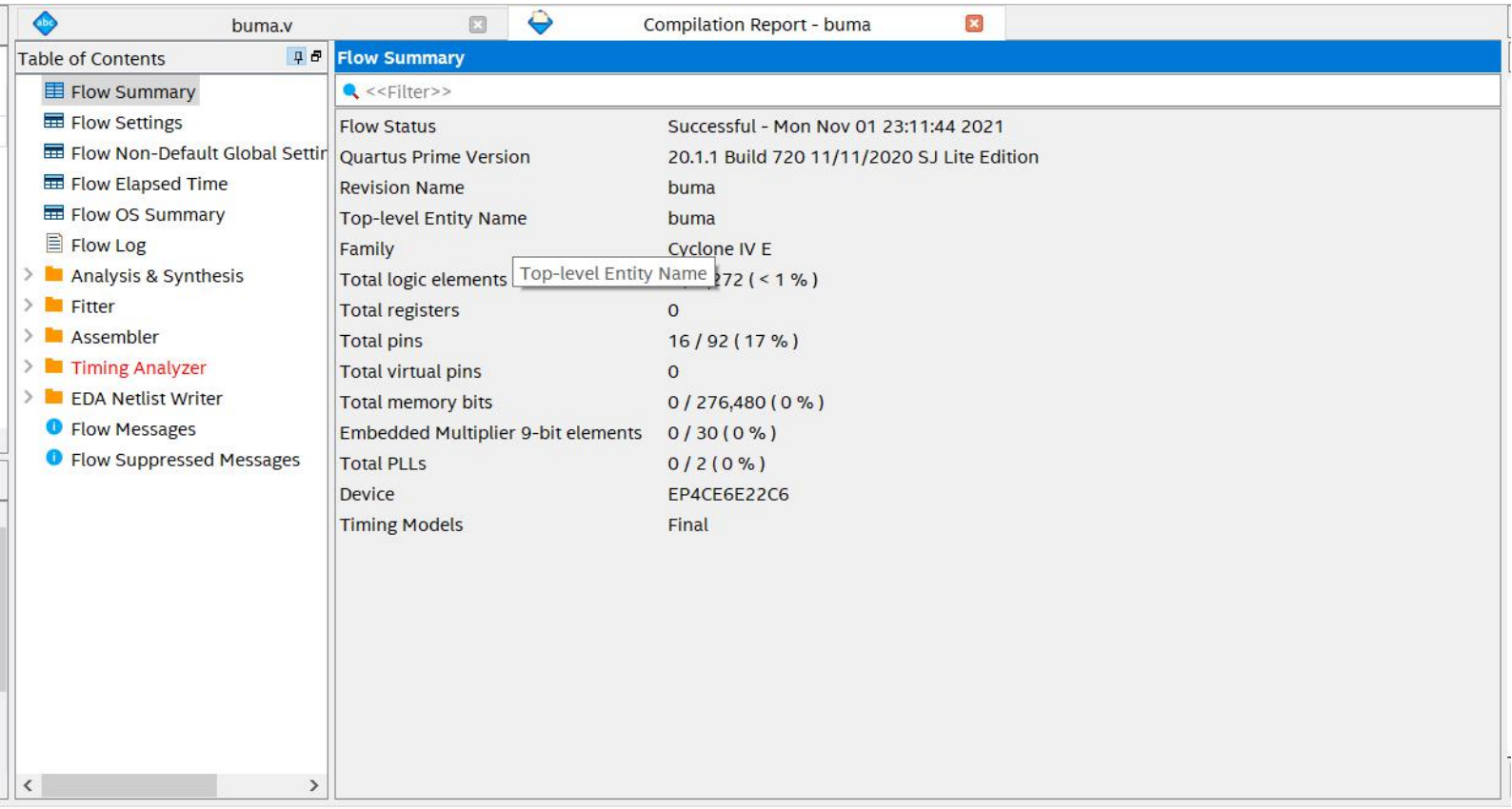
代码文件：

```
module buma (in,out);
    input [7:0] in;
    output[7:0] out;
    reg[7:0] out;
    reg[6:0] a;//a，符号位外的低 7 位
    always@(in)
        begin: bu
            if (in[7]==0) out<=in;
            else begin: bum
                a=(~in[6:0]+1);
                out[7]=in[7];
                out[6:0]=a;//~in[6:0]+1;
                  end
        end
Endmodule
```

图表文件：



资源开销：



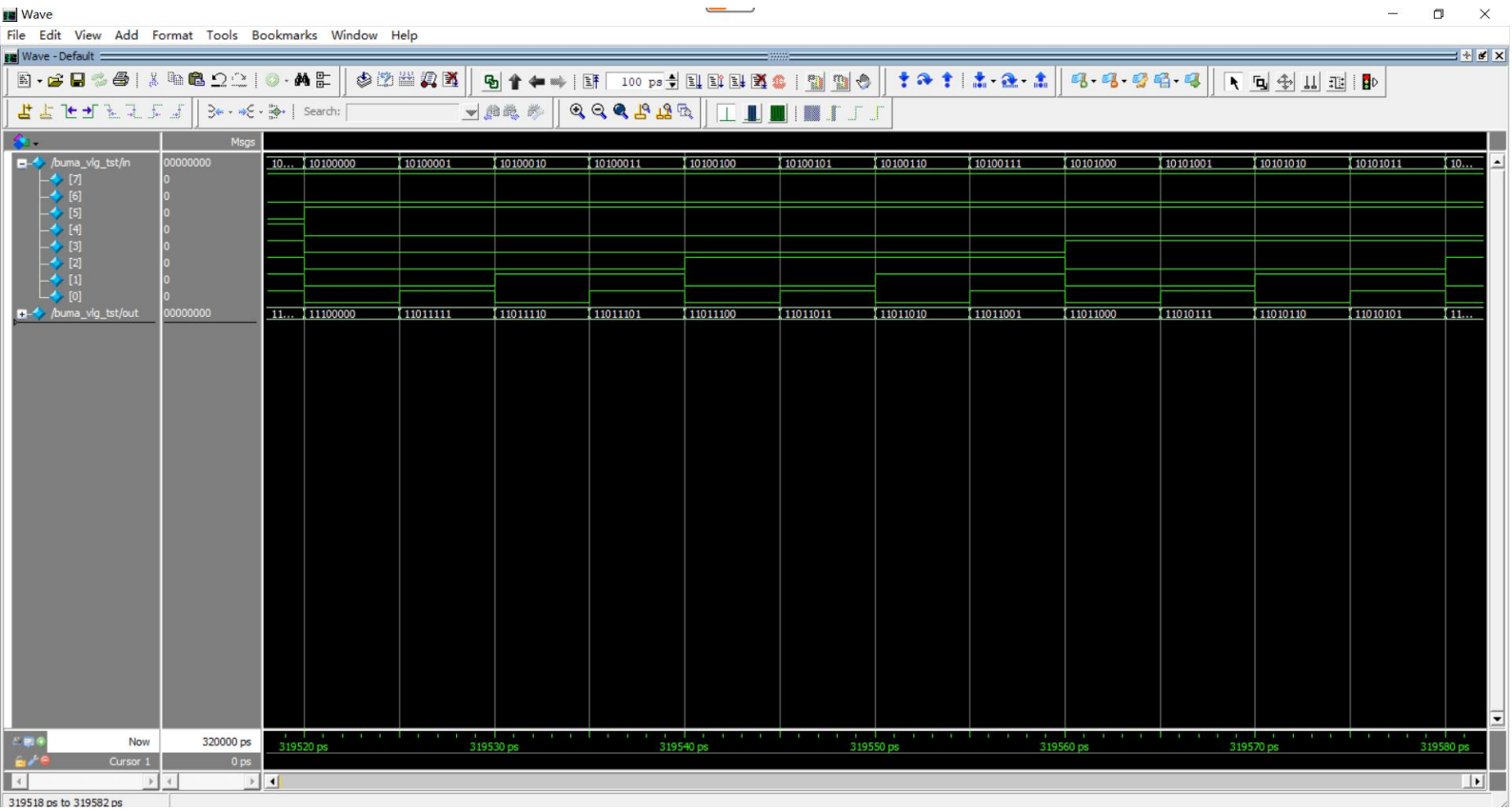
仿真文件：

```
`timescale 1 ps/ 1 ps
module buma_vlg_tst();
// constants
// general purpose registers
//reg eachvec;
// test vector input registers
reg [7:0] in;
// wires
wire [7:0]  out;
```

```
// assign statements (if any)
buma i1 (
// port map - connection between master ports and signals/registers
    .in(in),
    .out(out)
);
initial
begin
// code that executes only once
// insert code here --> begin
#0 in=8'b00000000;
// --> end
$display("Running testbench");
end
always #5 in=in+1;
// optional sensitivity list
// @(event1 or event2 or .... eventn)
//begin
// code executes for every event on sensitivity list
// insert code here --> begin

//@eachvec;
// --> end
//end
Endmodule
```

仿真结果：



数逻

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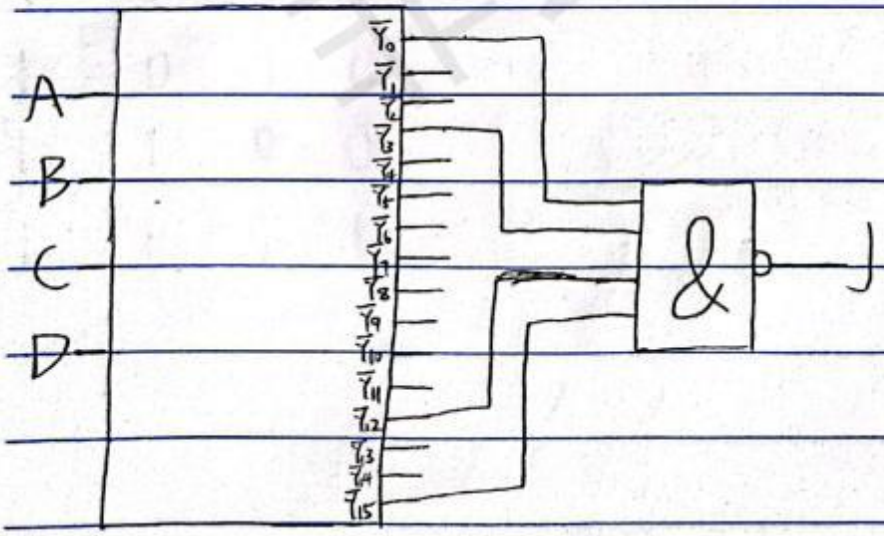
习题七

7.5 设ABCD为一位十进制数2421码，J为奇偶检验位

A B C D	J	A B C D	J
0 0 0 0	1	1 0 0 0	d
0 0 0 1	0	1 0 0 1	d
0 0 1 0	0	1 0 1 0	d
0 0 1 1	1	1 0 1 1	0
0 1 0 0	0	1 1 0 0	1
0 1 0 1	d	1 1 0 1	0
0 1 1 0	d	1 1 1 0	0
0 1 1 1	d	1 1 1 1	1

$\therefore F = m_0 + m_3 + m_{12} + m_{15}$

$= \overline{\overline{m_0} \cdot \overline{m_3} \cdot \overline{m_{12}} \cdot \overline{m_{15}}}$



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7.6 $\bar{I}_0, \bar{I}_4, \bar{I}_6, \bar{I}_7$ 为1, $\bar{I}_1, \bar{I}_2, \bar{I}_3, \bar{I}_5$ 为0

I_5优先级高，故输出为0|0

7.8

$Y = A\bar{B}D_0 + \bar{A}BD_1 + A\bar{B}D_2 + ABD_3$

$= \bar{A}B\bar{C} + ABC$

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

由真值表可知，该电路的功能为判断A.B.C是否相同，相同输出1，不同输出0