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**2020302181062**

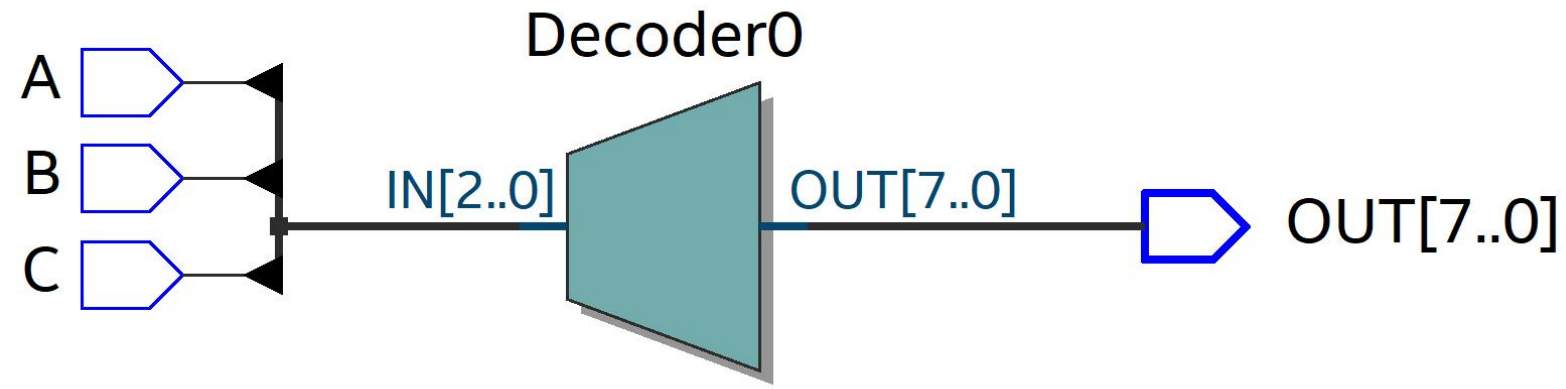
**EDA 3-4**

**Case：**

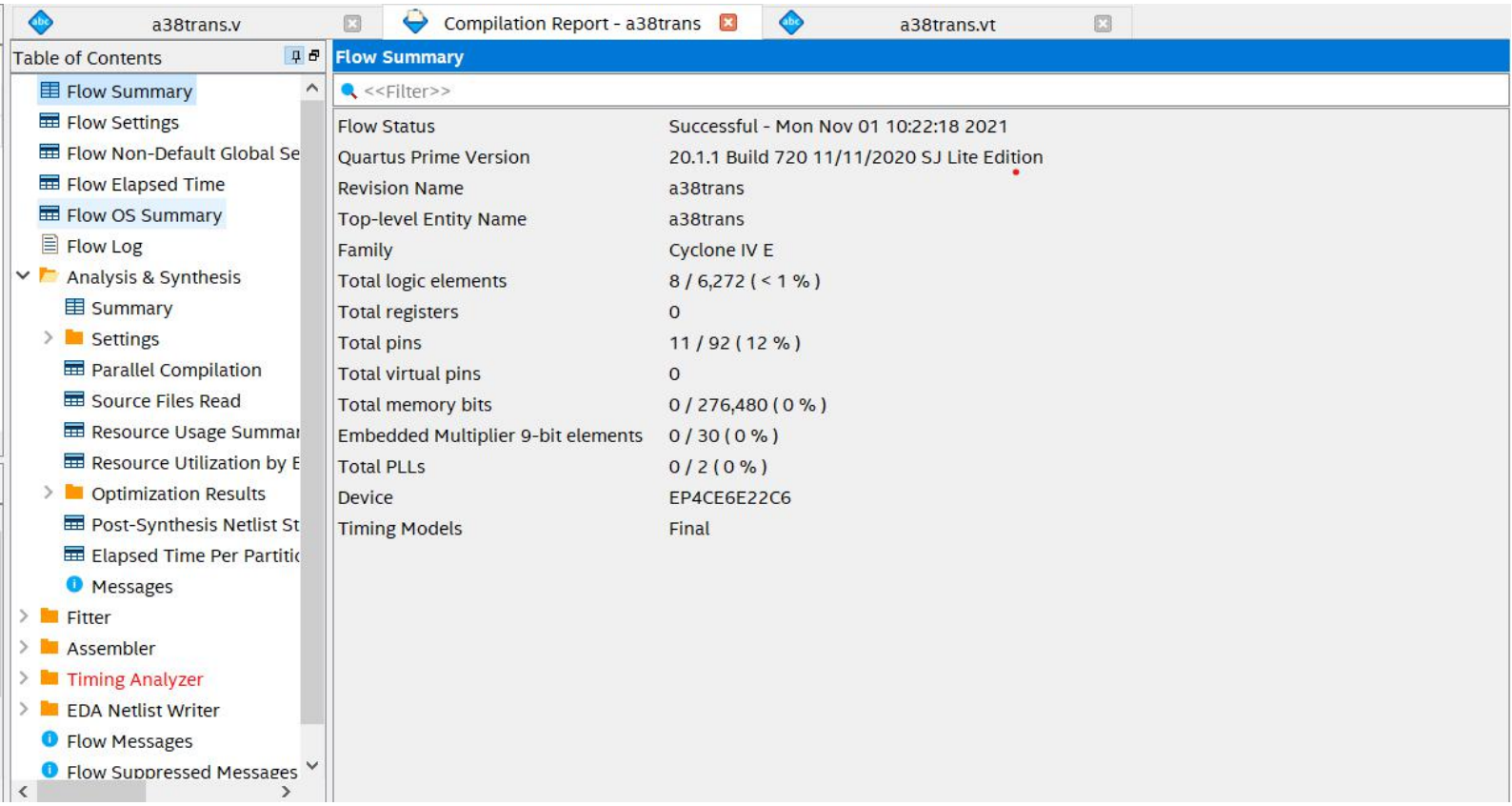
代码文件：

```
module a38trans(A,B,C,OUT);
  input A,B,C;
  output[7:0] OUT;
  reg[7:0] OUT;
  always@(A,B,C,OUT)
      begin:    a38trans
          case({A,B,C})
              3'b000: OUT<=8'b00000001;
              3'b001: OUT<=8'b00000010;
              3'b010: OUT<=8'b00000100;
              3'b011: OUT<=8'b00001000;
              3'b100: OUT<=8'b00010000;
              3'b101: OUT<=8'b00100000;
              3'b110: OUT<=8'b01000000;
              3'b111: OUT<=8'b10000000;
          endcase
      end
Endmodule
```

网表文件：




资源开销：




# 仿真文件：

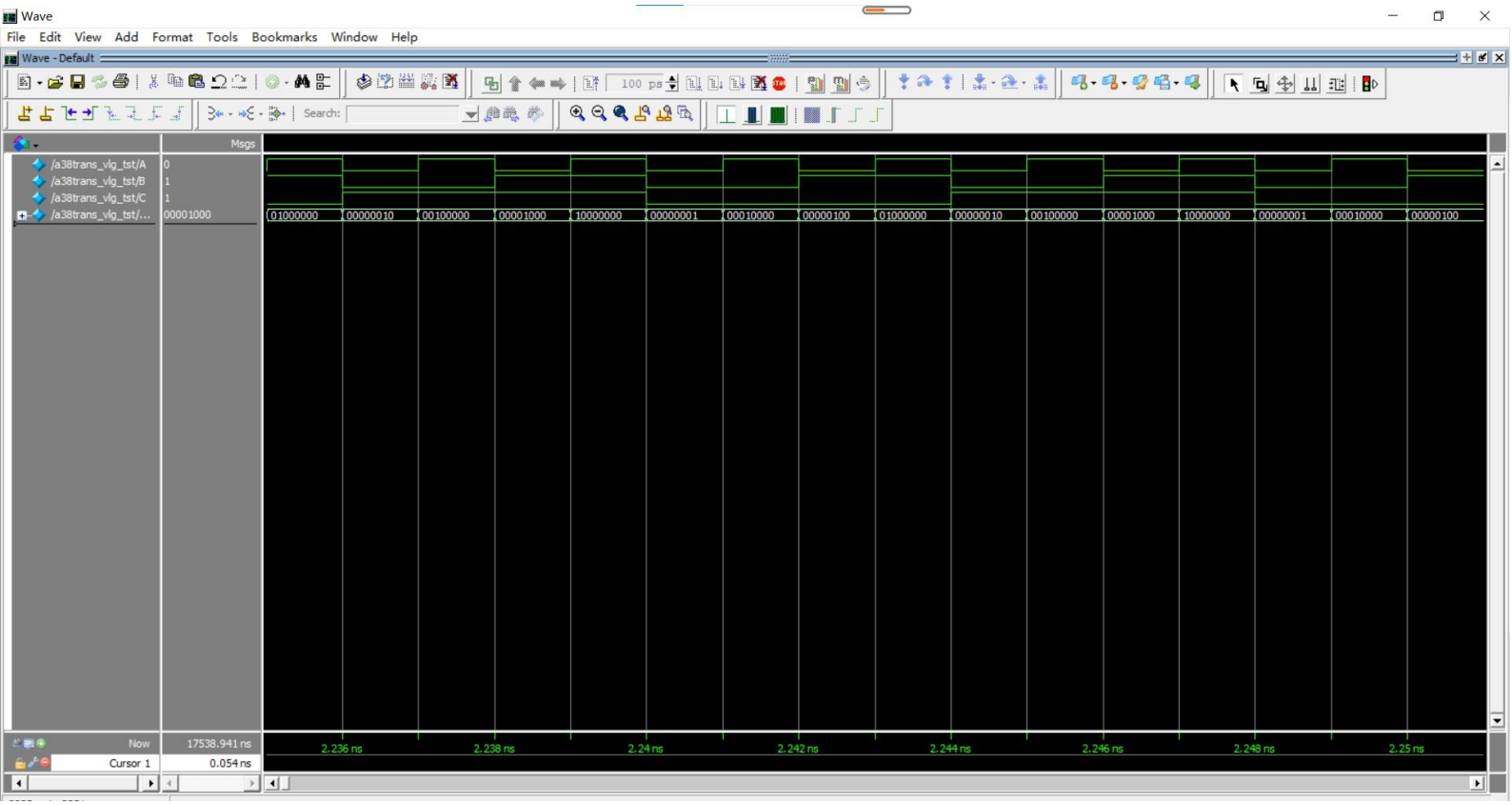
```
`timescale 1 ns/ 1 ps
module a38trans_vlg_tst();
// constants
// general purpose registers
// test vector input registers
reg A;
reg B;
reg C;
// wires
wire [7:0]    OUT;

// assign statements (if any)
a38trans i1 (
// port map - connection between master ports and signals/registers
  .A(A),
  .B(B),
  .C(C),
  .OUT(OUT)
);
initial
begin
// code that executes only once
// insert code here --> begin
#0 A=1'b0;
#0 B=1'b0;
#0 C=1'b0;
// --> end
$display("Running testbench");
end
```

```
  always #1 A=~A;
  always #2 B=~B;
  always #4 C=~C;

always @(OUT);
// optional sensitivity list
// @(event1 or event2 or .... eventn)
Endmodule
```

# 仿真结果：



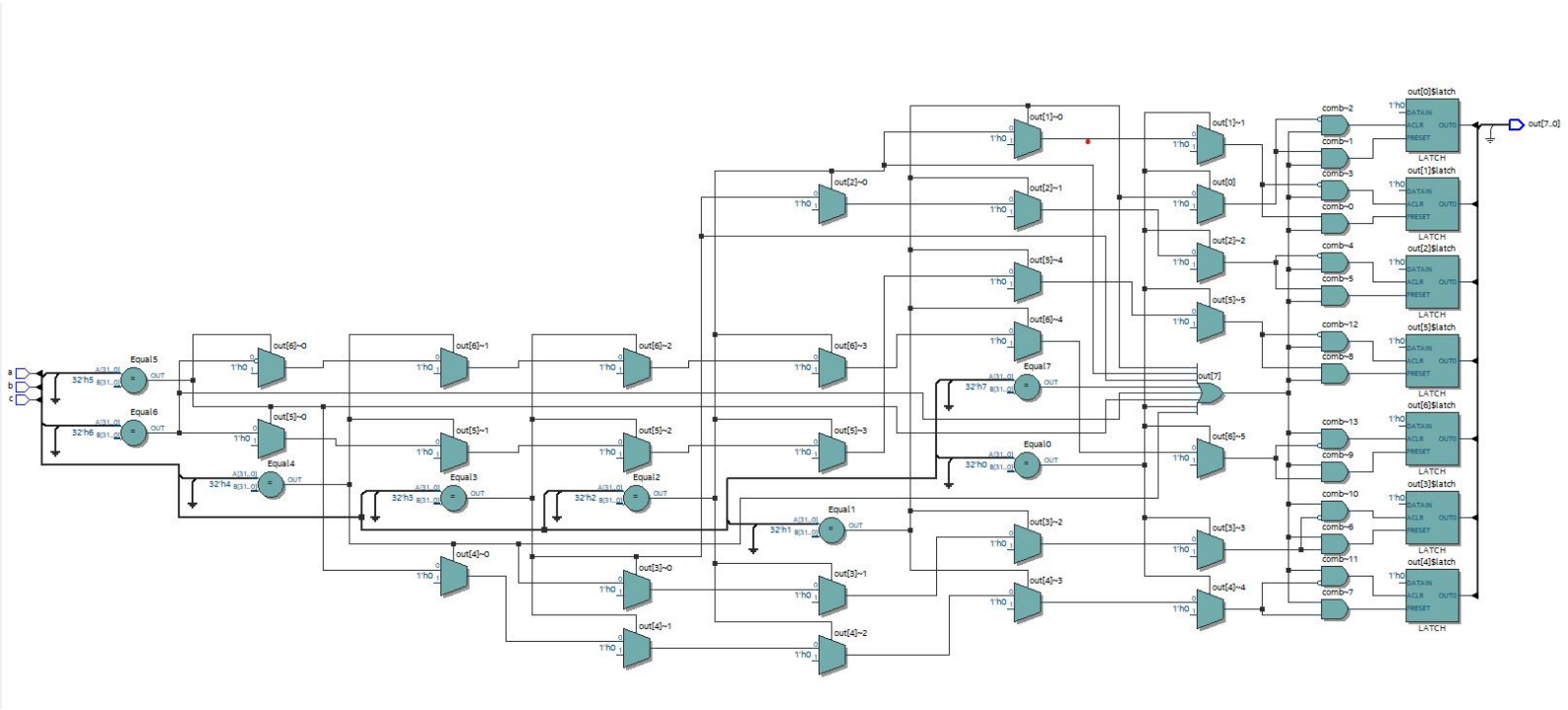

# If-else：

# 代码文件：

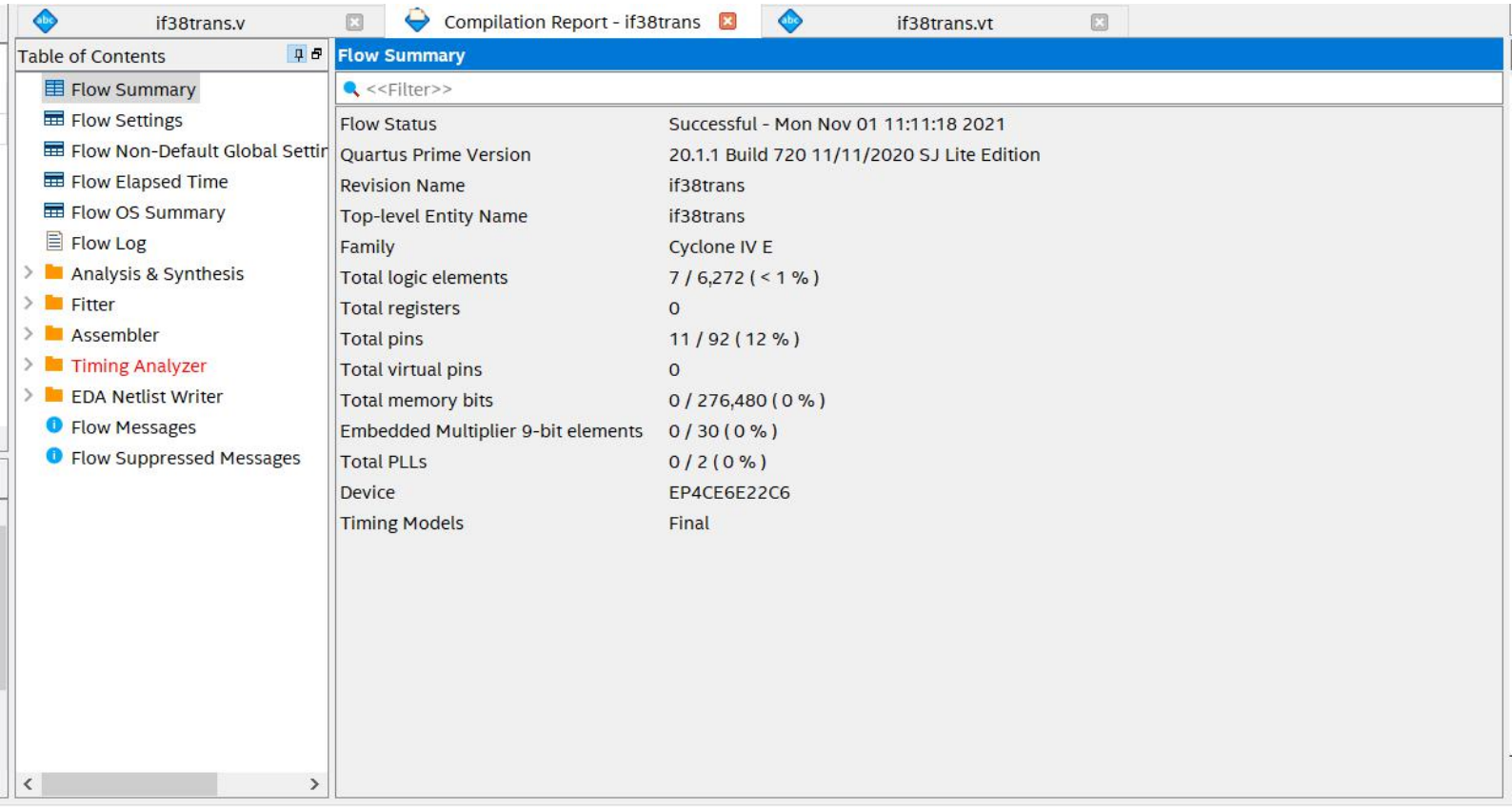
```
module if38trans (a,b,c,out);
  input a,b,c;
  output[7:0] out;
  reg[7:0] out;
  reg[2:0] sel;
  always@(a,b,c,out)
      begin
          sel={a,b,c};
          if(sel==0) out=8'b00000000;
          else if (sel==1) out<=8'b00000001;
          else if (sel==2) out<=8'b00000010;
          else if (sel==3) out<=8'b00000100;
          else if (sel==4) out<=8'b00001000;
          else if (sel==5) out<=8'b00010000;
          else if (sel==6) out<=8'b00100000;
```

```
            else if (sel==7) out<=8'b01000000;
            else if (sel==8) out<=8'b10000000;
        end
Endmodule
```

# 网表文件：



# 资源开销：




# 仿真文件：

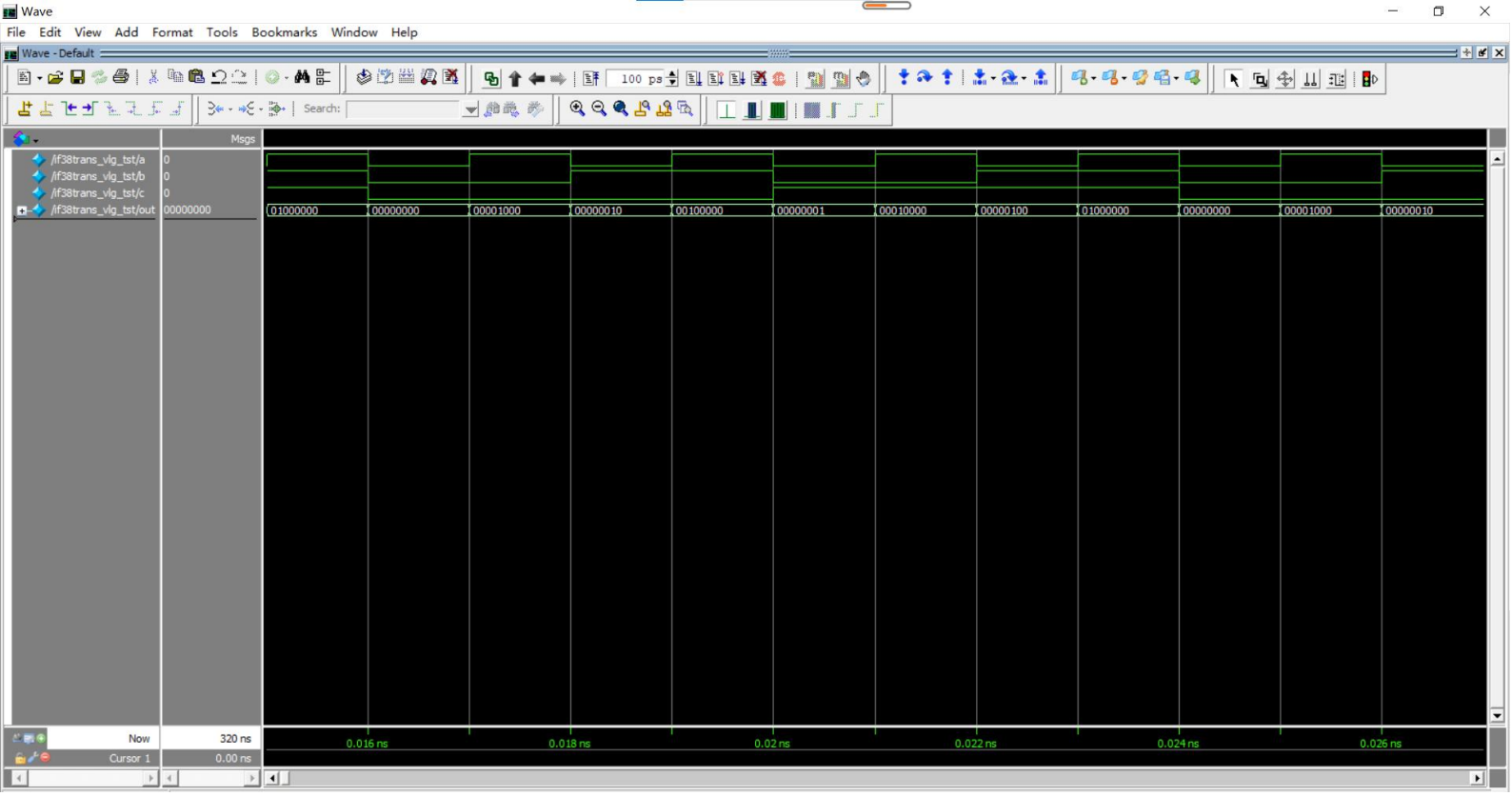
```
`timescale 1 ps/ 1 ps
module if38trans_vlg_tst();
```

```
  reg a;
  reg b;
  reg c;
  // wires
  wire [7:0]    out;

  // assign statements (if any)
  if38trans i1 (
  // port map - connection between master ports and signals/registers
    .a(a),
    .b(b),
    .c(c),
    .out(out)
  );
  initial
  begin
  // code that executes only once
  // insert code here --> begin
  #0 a=1'b0;
  #0 b=1'b0;
  #0 c=1'b0;
  // --> end
  $display("Running testbench");
  end
  always #1 a=~a;
  always #2 b=~b;
  always #4 c=~c;

  always@(out);
  // --> end
  endmodule
```

# 仿真结果：


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Search:
Msgs
/lf38trans_vlg_tst/a
/lf38trans_vlg_tst/b
/lf38trans_vlg_tst/c
/lf38trans_vlg_tst/out
0
0
0
00000000
01000000
00000000
00001000
00000010
00100000
00000001
00010000
00000100
01000000
00000000
00001000
00000010
Now
320 ns
Cursor 1
0.00 ns
0.016 ns
0.018 ns
0.02 ns
0.022 ns
0.024 ns
0.026 ns