

NETWORK

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graph TD; Network[NETWORK] --- Node1[Node]; Network --- Node2[Node]; Network --- Node3[Node]; subgraph Node1 [Node]; direction TB; M1[MEMORY] --- C1_1(Core); M1 --- C1_2(Core); C1_1 --- C1_3(Core); C1_2 --- C1_4(Core); end; subgraph Node2 [Node]; direction TB; M2[MEMORY] --- C2_1(Core); M2 --- C2_2(Core); C2_1 --- C2_3(Core); C2_2 --- C2_4(Core); end; subgraph Node3 [Node]; direction TB; M3[MEMORY] --- C3_1(Core); M3 --- C3_2(Core); C3_1 --- C3_3(Core); C3_2 --- C3_4(Core); end;
```

The diagram illustrates a network architecture. At the top, a green rectangular box labeled "NETWORK" is connected by three black lines to three separate nodes below. Each node is represented by a white rectangular box with a black border. Inside each node box, there is an orange rectangular box at the top labeled "MEMORY". Below the memory box, there are four olive-green oval shapes, each labeled "Core", arranged in a 2x2 grid. Blue wavy lines connect the "MEMORY" box to the "Core" ovals: two wavy lines on the left side connect to the left column of cores, and two wavy lines on the right side connect to the right column of cores. Below each node box, the word "Node" is written in black text.

MEMORY

Core

Core

Core

Core

Node

MEMORY

Core

Core

Core

Core

Node

MEMORY

Core

Core

Core

Core

Node