instruction	Bytes	Cycles	Opcode
ACALL	2	2	aaa10001 address
LCALL	3	2	00010010 address address
RET	1	2	00100010
RET	1	2	00110010
AJMP	2	2	aaa00001 address
LJMP	3	2	00000010 address address
SJMP	2	2	10000000 rel.address
JMP	1	2	01110011
JZ	2	2	01100000 rel.address
JNZ	2	2	01110000 rel.address
CJNE	3	2	10110101 address rel.address
CJNE	3	2	10110100 data rel.address
CJNE	3	2	10111rrr data rel.address
CJNE	3	2	1011011i data rel.address
DNJZ	2	2	11011rrr rel.address
DJNZ	3	2	11010101 address rel.address
NOP	1	1	00000000
ADD	1	1	00101rrr
ADD	2	1	00100101 address
ADD	1	1	0010011i
ADD	2	1	00100100 data
SUBB	1	1	10011rrr
SUBB	2	1	10010101 address
SUBB	1	1	1001011i
SUBB	2	1	10010100 data
ADDC	1	1	00111rrr
ADDC	2	1	00110101 address
ADDC	1	1	0011011i
ADDC	2	1	00110100 data
INC	1	1	00000100
INC	1	1	00001rrr
(DPTR)INC	1	1	10100011
DEC	1	1	00010100
DEC	1	1	00011rrr
MUL	1	4	10100100
DIV	1	4	10000100
CLR	1	1	11100100
CPL	1	1	11110100
RL	1	1	00100011
RLC	1	1	00110011
RR	1	1	00000011
RRC	1	1	00010011
SWAP	1	1	11000100
MOV	1	1	11101rrr
MOV	2	1	11100101 address
MOV	1	1	1110011i
MOV	2	1	01110100 data
(dir)MOV	2	2	1000011i
(dir)MOV	3	2	01110101 address data
(@r)MOV	1	1	1111011i
(@r)MOV	2	2	1010011i address
MOV @r	2	1	0111011i data
PUSH	2	2	11000000 address
POP	2	2	11010000 address
XCH	2	1	11000101 address
XCH	1	1	1100011i
XCHD	1	1	1101011i
ANL	1	1	01011rrr
ANL	2	1	01010101, address
ANL	1	1	0101011i
ANL	2	2	01010100 data
(dir)ANL	2	1	01010010 address
(dir)ANL	2	1	01010011 address data
ORL	1	1	01001rrr
ORL	2	1	01000101, address
ORL	1	1	0100011i
ORL	2	1	01000100 data
(dir)ORL	2	1	01000010 address
(dir)ORL	3	2	01000011 address data
XRL	1	1	01101rrr
XRL	2	1	01100101 address
XRL	1	1	0110011i
XRL	2	1	01100100 data
XRL	2	1	01100010 address
XRL	3	3	01100011 address data

MODE	INFO
register	MOV A,R7=MOV A,7
implied	the address is implied by instruction
direct	address is given
indirect	@R0 or @R1

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