School of Computer Science Engineering and Technology

Course- BTech	Type- Core
Course Code: CSET203	Course Name- Microprocessor & Computer Architecture
Year- 2022	Semester- 3rd
Date-	Batch-

Lab Assignment -2 (Set-5)

Q1. Use a D flip-flop, a 2x1 multiplexer, and an inverter to design a J-K flipflop in Logisim tool.

Q2. Suppose the equation Y = ABC' + BD' + C represents a combinational circuit with 4 inputs and one output. Implement the following combinational circuit using basic gates and verify the output with a truth table. Truth Table can be generated using tool itself.

Q3. Design and derive the expression of full subtractor using 4:1 MUX and verify its truth table on Logisim.

Q4. Create a 4-bit ALU in Logisim that can compute AND, OR, and SUM of two 4-bit numbers. Here, it is noted that only basic gates we can use to design the above ALU circuit.

Q5. Design and simulate an encoder in Logisim that can be used in a domestic burglar alarm that has sensors for each of eight zones. Each sensor signal is 1 when an intrusion is detected in that zone, and 0 otherwise. Include the explanation in the word file. The encoder has three bits of output, encoding the zone as follows:
Zone 1: 000; Zone 2: 001; Zone 3: 010; Zone 4: 011; Zone 5: 100; Zone 6: 101; Zone 7: 110; Zone 8: 111

Submission Instructions:

1. Submit your .circ file from LMS within 2 Hours of lab. Save all the files as per the format
2. RollNo_Lab#_QuestionNo.circ (Example: E19CSE632_Lab1_Q2. circ). Make a .zip file and
3. upload.
4. Write your Name and Roll No in the design itself. Without this you will score zero for
5. that question.
6. Provide labels for all the input and output.
7. Late submission will lead to penalty.