1. Description

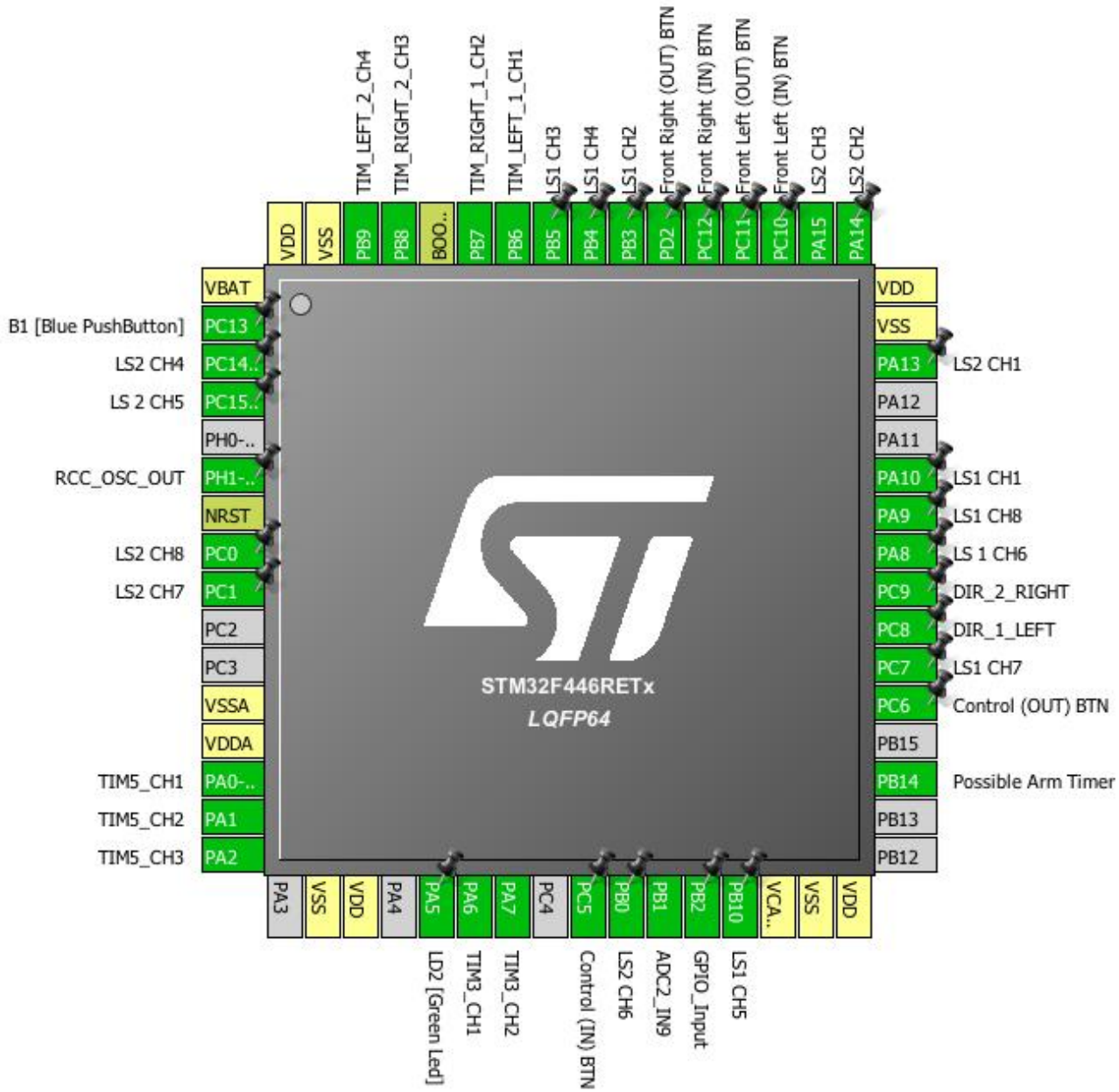
1.1. Project

Project Name	Nucleo
Board Name	NUCLEO-F446RE
Generated with:	STM32CubeMX 4.19.0
Date	04/20/2017

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F446
MCU name	STM32F446RETx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration



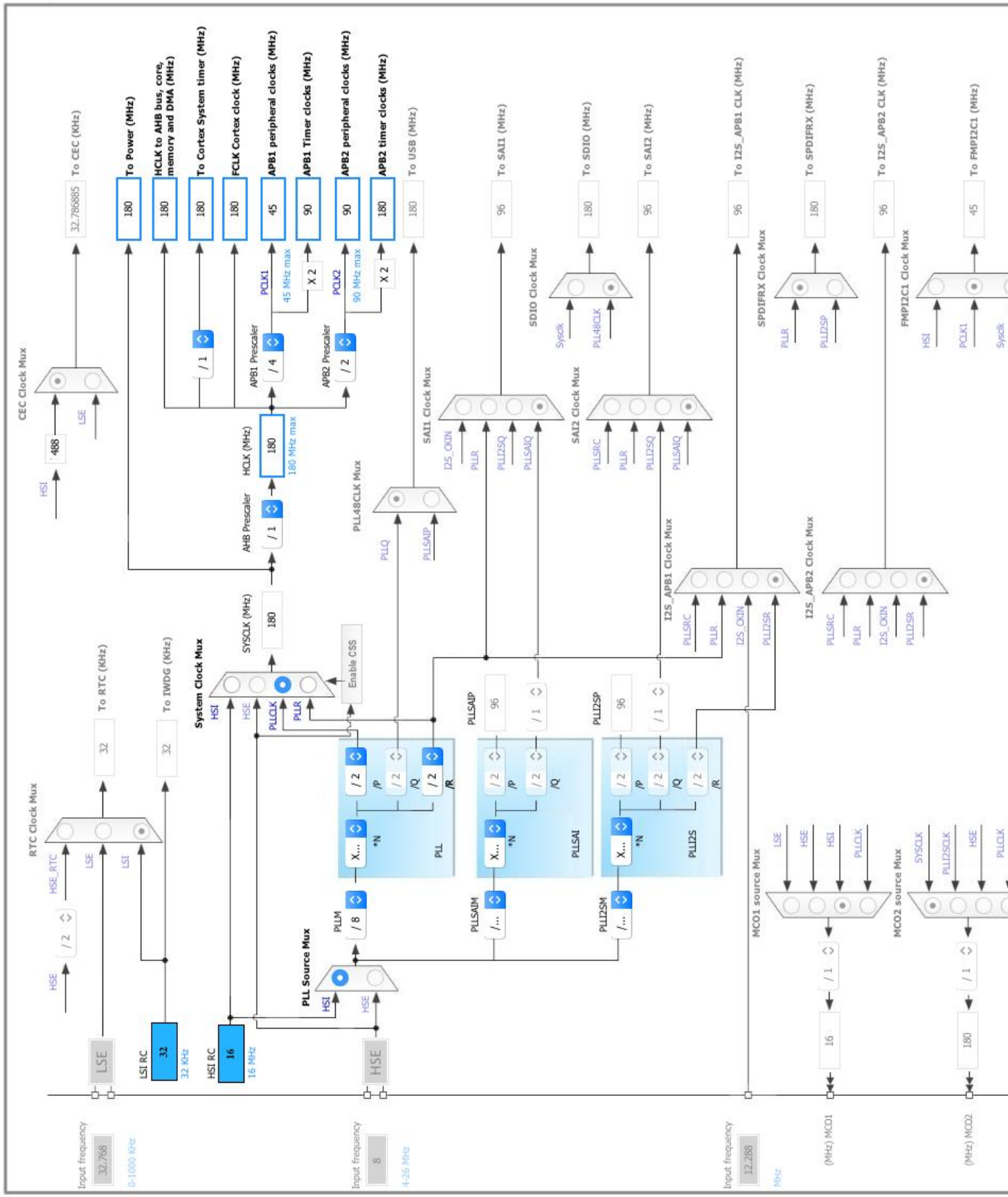
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13	I/O	GPIO_EXTI13	B1 [Blue PushButton]
3	PC14-OSC32_IN *	I/O	GPIO_Input	LS2 CH4
4	PC15-OSC32_OUT *	I/O	GPIO_Input	LS 2 CH5
6	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	PC0 *	I/O	GPIO_Input	LS2 CH8
9	PC1 *	I/O	GPIO_Input	LS2 CH7
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	TIM5_CH1	
15	PA1	I/O	TIM5_CH2	
16	PA2	I/O	TIM5_CH3	
18	VSS	Power		
19	VDD	Power		
21	PA5 *	I/O	GPIO_Output	LD2 [Green Led]
22	PA6	I/O	TIM3_CH1	
23	PA7	I/O	TIM3_CH2	
25	PC5 *	I/O	GPIO_Input	Control (IN) BTN
26	PB0 *	I/O	GPIO_Input	LS2 CH6
27	PB1	I/O	ADC2_IN9	
28	PB2 *	I/O	GPIO_Input	
29	PB10 *	I/O	GPIO_Input	LS1 CH5
30	VCAP_1	Power		
31	VSS	Power		
32	VDD	Power		
35	PB14	I/O	TIM12_CH1	Possible Arm Timer
37	PC6 *	I/O	GPIO_Output	Control (OUT) BTN
38	PC7 *	I/O	GPIO_Input	LS1 CH7
39	PC8 *	I/O	GPIO_Output	DIR_1_LEFT
40	PC9 *	I/O	GPIO_Output	DIR_2_RIGHT
41	PA8 *	I/O	GPIO_Input	LS 1 CH6
42	PA9 *	I/O	GPIO_Input	LS1 CH8
43	PA10 *	I/O	GPIO_Input	LS1 CH1
46	PA13 *	I/O	GPIO_Input	LS2 CH1
47	VSS	Power		

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
48	VDD	Power		
49	PA14 *	I/O	GPIO_Input	LS2 CH2
50	PA15 *	I/O	GPIO_Input	LS2 CH3
51	PC10 *	I/O	GPIO_Input	Front Left (IN) BTN
52	PC11 *	I/O	GPIO_Output	Front Left (OUT) BTN
53	PC12 *	I/O	GPIO_Input	Front Right (IN) BTN
54	PD2 *	I/O	GPIO_Output	Front Right (OUT) BTN
55	PB3 *	I/O	GPIO_Input	LS1 CH2
56	PB4 *	I/O	GPIO_Input	LS1 CH4
57	PB5 *	I/O	GPIO_Input	LS1 CH3
58	PB6	I/O	TIM4_CH1	TIM_LEFT_1_CH1
59	PB7	I/O	TIM4_CH2	TIM_RIGHT_1_CH2
60	BOOT0	Boot		
61	PB8	I/O	TIM4_CH3	TIM_RIGHT_2_CH3
62	PB9	I/O	TIM4_CH4	TIM_LEFT_2_Ch4
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC2

mode: IN9

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 9
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. SYS

Timebase Source: SysTick

5.3. TIM3

Combined Channels: Encoder Mode

5.3.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	Encoder Mode TI1
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

5.4. TIM4

Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3
Channel4: PWM Generation CH4

5.4.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**180 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**100 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**50 ***
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	**50 ***
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	**50 ***
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	**50 ***
Fast Mode	Disable
CH Polarity	High

5.5. TIM5

Channel1: PWM Generation CH1
Channel2: PWM Generation CH2
Channel3: PWM Generation CH3

5.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**360 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**10000 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	**150 ***
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (32 bits value)	**150 ***
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

5.6. TIM12

Channel1: PWM Generation CH1

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**360 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**10000 ***
Internal Clock Division (CKD)	No Division

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**150 ***
Fast Mode	Disable
CH Polarity	High

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC2	PB1	ADC2_IN9	Analog mode	No pull-up and no pull-down	n/a	
TIM3	PA6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PB6	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM_LEFT_1_CH1
	PB7	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM_RIGHT_1_CH2
	PB8	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM_RIGHT_2_CH3
	PB9	TIM4_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM_LEFT_2_Ch4
TIM5	PA0-WKUP	TIM5_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	TIM5_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA2	TIM5_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM12	PB14	TIM12_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	Possible Arm Timer
GPIO	PC13	GPIO_EXTI13	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	n/a	B1 [Blue PushButton]
	PC14-OSC32_IN	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LS2 CH4
	PC15-OSC32_OUT	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LS 2 CH5
	PC0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LS2 CH8
	PC1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LS2 CH7
	PA5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Green Led]
	PC5	GPIO_Input	Input mode	**Pull-up ***	n/a	Control (IN) BTN
	PB0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LS2 CH6
	PB2	GPIO_Input	Input mode	**Pull-up ***	n/a	
	PB10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LS1 CH5
	PC6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Control (OUT) BTN
	PC7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LS1 CH7
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DIR_1_LEFT
	PC9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DIR_2_RIGHT
	PA8	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LS 1 CH6
	PA9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LS1 CH8
	PA10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LS1 CH1
	PA13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LS2 CH1

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PA14	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LS2 CH2
	PA15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LS2 CH3
	PC10	GPIO_Input	Input mode	**Pull-up ***	n/a	Front Left (IN) BTN
	PC11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Front Left (OUT) BTN
	PC12	GPIO_Input	Input mode	**Pull-up ***	n/a	Front Right (IN) BTN
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Front Right (OUT) BTN
	PB3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LS1 CH2
	PB4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LS1 CH4
	PB5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	LS1 CH3

6.2. DMA configuration

nothing configured in DMA service

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
EXTI line[15:10] interrupts	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 interrupts	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM5 global interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F446
MCU	STM32F446RETx
Datasheet	027107_Rev5

7.2. Parameter Selection

Temperature	25
Vdd	null

8. Software Project

8.1. Project Settings

Name	Value
Project Name	Nucleo
Project Folder	/Users/Sean/Workspace/CPRoborodentia/Nucleo
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F4 V1.14.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No