Single Cycle Processor in Logisim

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Screenshots demonstrating working of processor

Control

MemtoReg
ALUOp
MemWrite
ALUSrc
RegWrite

IMem

Addr

Clock

rs1
rs2
rd
WriteData

Data1
Data2

ImmGen

ALU-Ctrl

0
32   8
extend

0
32   8
extend

Addr   DataOut
DataIn
DataMem

MUX

MUX

D   Q
WE
R

IAddr   03 h
Instruction 0200393 h
rs1   00 h
rs2   02 h
rd   07 h
Data1   00000000 h
Data2   EEEEEEEE h
Imm   00000002 h
ALUCtrl   0 h
ALUOut   00000002 h
DataOut   00000000 h
WriteData   00000002 h

Control

IMem
Addr
Clock

D Q
WE
R

03

01

τ in
c out

τ in
c out

0
32   8
extend

MemtoReg
ALUOp
MemWrite
ALUSrc
RegWrite

MUX

rs1   Data1
rs2   Data2
rd
WriteData

MUX

0
32   8
extend

Addr   DataOut
DataIn
DataMem

MUX

ImmGen

ALU-Ctrl

30,14-12

19-15

IAddr   03 h
Instruction 0d0a3030 h
rs1   14 h
rs2   10 h
rd   00 h
Data1   EEEEEEEE h
Data2   EEEEEEEE h
Imm   000000c0 h
ALUCtrl   0 h
ALUOut   EEEEEEEE h
DataOut EEEEEEEE h
WriteData EEEEEEEE h