Datasheet

RF-BM-ND06 BT5.0_MODULE

Version 1.0

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REVISION HISTORY

Version	Date	Notes	Contributor(s)	Approver
1.0	8 August 2018	Initial Production Release	Aroo wang	Aroo wang

1、OVERVIEW AND KEY FEATURES

Every RF-BM-ND06 module is designed to simplify of Bluetooth Low Energy (BLE) v5.0 and Thread (802.15.4) to small, portable. The RF-BM-ND06 provides engineers with considerable design flexibility in both hardware and software programming capabilities. Based on the world-leading Nordic Semiconductor nRF52840 chipset, the RF-BM-ND06 modules provide ultra-low power consumption with outstanding wireless range via +8 dBm of transmit power and the Long Range (CODED PHY) Bluetooth 5 feature.

*smart*BASIC is an event-driven programming language that is highly optimized for memory-constrained systems such as embedded modules. It was designed to make BLE development quicker and simpler, vastly cutting down time to market.

The Nordic SDK, on the other hand, offers developers source code (in C) and precompiled libraries containing BLE and ANT+ device profiles, wireless communication, as well as application examples.

Note: RF-BM-ND06 hardware provides all functionality of the nRF52840 chipset used in the module design. This is a hardware datasheet only – it does not cover the software aspects of the ND06.
For customers using *smart*BASIC, refer to the *smart*BASIC extensions guide (available from the ND06 product page of the RFSTAR website.

For customers using the Nordic SDK, refer to www.nordicsemi.com.

1.1 Features of the benefits

- Bluetooth v5.0 – Single mode
- NFC
- 802.15.4 (Thread) radio support
- External or internal antennas
- Multiple programming options
  - smartBASIC AT command set shim or
  - Nordic SDK in C
- Compact footprint
- Programmable Tx power +8 dBm to -20 dBm, -40dBm
- Rx sensitivity – -95 dBm (1Mbps), - 103dBm (125kbps)
- Ultra-low power consumption
- Tx – 4.8 mA peak (at 0 dBm, DCDC on)
- Rx: 4.6 mA peak (DCDC on)
- Standby Doze – 3.1 uA typical
- Deep Sleep – 0.4 uA
- UART, GPIO, ADC, PWM, FREQ output, timers, I2C, SPI, I2S, PDM, and USB interfaces
- Fast time-to-market
- Full Bluetooth Declaration ID (Full Test report)
- No external components required
- Industrial temperature range (-40° C to +85° C)

1.2 Application Areas

- Medical devices
- IoT Sensors
- Appcessories
- Fitness sensors
- Location awareness
- Home automation

2、SPECIFICATION

2.1 Specification Summary

Categories/Feature	Implementation
Wireless Specification	
Bluetooth®	▪ BT 5.0 -Single mode ▪ 4x Range (CODED PHY support) – BT 5.0 ▪ 2x Speed (2M PHY support) – BT 5.0 ▪ LE Advertising Extensions – BT 5.0 ▪ Concurrent master, slave ▪ BLE Mesh capabilities ▪ Diffie-Hellman based pairing (LE Secure Connections) – BT 4.2 ▪ Data Packet Length Extension – BT 4.2 ▪ Link Layer Privacy (LE Privacy 1.2) – BT 4.2 ▪ LE Dual Mode Topology – BT 4.1 ▪ LE Ping – BT 4.1
Frequency	2.402 - 2.480 GHz
Raw Data Rates	▪ 1 Mbps BLE (over-the-air) ▪ 2 Mbps BLE (over-the-air) ▪ 125 kbps BLE (over-the-air) ▪ 500 kbps BLE (over-the-air)
Maximum Transmit Power Setting	+8 dBm Conducted 451-00001 (Integrated antenna) +8 dBm Conducted 451-00002 (External antenna)
Minimum Transmit Power Setting	-40 dBm, -20 dBm (in 4 dB steps) -16 dBm, -12 dBm, - 8 dBm, - 4 dBm, 0 dBm, 2 dBm, 4 dBm, 5 dBm, 6 dBm, 7 dBm,
	BLE 1 Mbps (BER=1E-3) -95 dBm typical BLE 2 Mbps -92 dBm typical

Receive Sensitivity (≤37byte packet)	BLE 125 kbps -103 dBm typical BLE 500 kbps -99 dBm typical
Link Budget (conducted)	103 dB @ BLE 1 Mbps 111 dB @ BLE 125 kbps
NFC	
NFC-A Listen mode compliant	**Based on NFC forum specification** · 13.56 MHz · Date rate 106 kbps · NFC Type2 and Type 4 emulation **Modes of Operation** · Disable · Sense · Activated **Use Cases** · Touch-to-Pair with NFC · NFC enabled Out-of-Band Pairing
System Wake-On-Field function	Proximity Detection

Categories/Feature	Implementation
Host Interfaces and Peripherals	
Total	48 x multifunction I/O lines
UART	2 UARTs Tx, Rx, CTS, RTS DCD, RI, DTR, DSR Default 115200, n, 8, 1 From 1,200 bps to 1 Mbps
USB	USB 2.0 FS (Full Speed, 12Mbps). CDC driver / Virtual UART (baud rate TBD) Other USB drivers available via Nordic SDK
GPIO	Up to 48, with configurable: I/O direction, O/P drive strength (standard 0.5 mA or high 3mA/5 mA), Pull-up /pull-down Input buffer disconnect
	Eight 8/10/12-bit channels 0.6 V internal reference

ADC	Configurable 4, 2, 1, 1/2, 1/3, 1/4, 1/5 1/6(default) pre-scaling Configurable acquisition time 3uS, 5uS, 10uS (default), 15uS, 20uS One-shot mode
PWM	PWM outputs on 16 GPIO output pins · PWM output duty cycle: 0%-100% · PWM output frequency: Up to 500kHz
FREQ	FREQ outputs on 16 GPIO output pins. · FREQ output frequency: 0 MHz-4MHz (50% duty cycle)
I2C	Two I2C interface (up to 400 kbps)
SPI	Four SPI Master Slave interface (up to 4 Mbps)
QSPI	One 32-MHz QSPI interface. Gives XIP (Execution in Place) capability. External serial flas
Temperature Sensor	One temperature sensor. Temperature range equal to the operating temperature range Resolution 0.25 degrees
RSSI Detector	One RF received signal strength indicator ±2 dB accuracy (valid over -90 to -20 dBm) One dB resolution
I2S	One inter-IC sound interface
PDM	One pulse density modulation interface
Optional (External to the ND06 module)	
External 32.768 kHz crystal	For customer use, connect +/-20ppm accuracy crystal for more accurate protocol timing.

Categories/Feature	Implementation
Profiles	
Services supported	· Central Mo · Peripheral Mode · Mesh (with custom models) · Custom and adopted profiles
Programmability	
smartBASIC	FW upgrade via JTAG or UART Application download via UART or Via Over-the-Air (if SIO_02 pin is pulled high externally)
Nordic SDK	Via JTAG
Operating Modes	

	Self-contained Run mode Selected by nAutoRun pin status: LOW (0V).
smartBASIC	Interactive/Development mode HIGH (VDD). Then runs via at+run (and file name of smartBASIC application script).
Nordic SDK	As per Nordic SDK
Supply Voltage	
Supply (VDD or VDD_HV) options	▪ Normal voltage mode VDD 1.7- 3.6 V – Internal DCDC converter or LDO ▪ High voltage mode VDD_HV 2.5V-5.5V Internal DCDC converter or LDO
Power Consumption	
Active Modes Peak Current (for maximum Tx power +8 dBm) – Radio only	14.8 mA peak Tx (with DCD
Active Modes Peak Current (for Tx power -40 dBm) – Radio only	4.6 mA peak Tx (with DCDC)
Active Modes Average Current	Depends on many factors,
Ultra-low Power Modes	Standby Doze 3.1 uA typical Deep Sleep 0.4 uA
Antenna Options	
Internal	Printed PCB PIFA antenna – on-board

Categories/Feature	Implementation
Physical	
Dimensions	24.0 mm x 20.5 mm x 2.2 mm Pad Pitch – 0.8 mm Bottom pad
Weight	<1 gram
Environmental	
Operating	-40 ˚C to +85 ˚C
Storage	-55 ˚C to +125 ˚C
Miscellaneous (Other)	
Lead Free	Lead-free and RoHS compliant

2、SPECIFICATION

3.1 Block Diagram and Pin-out

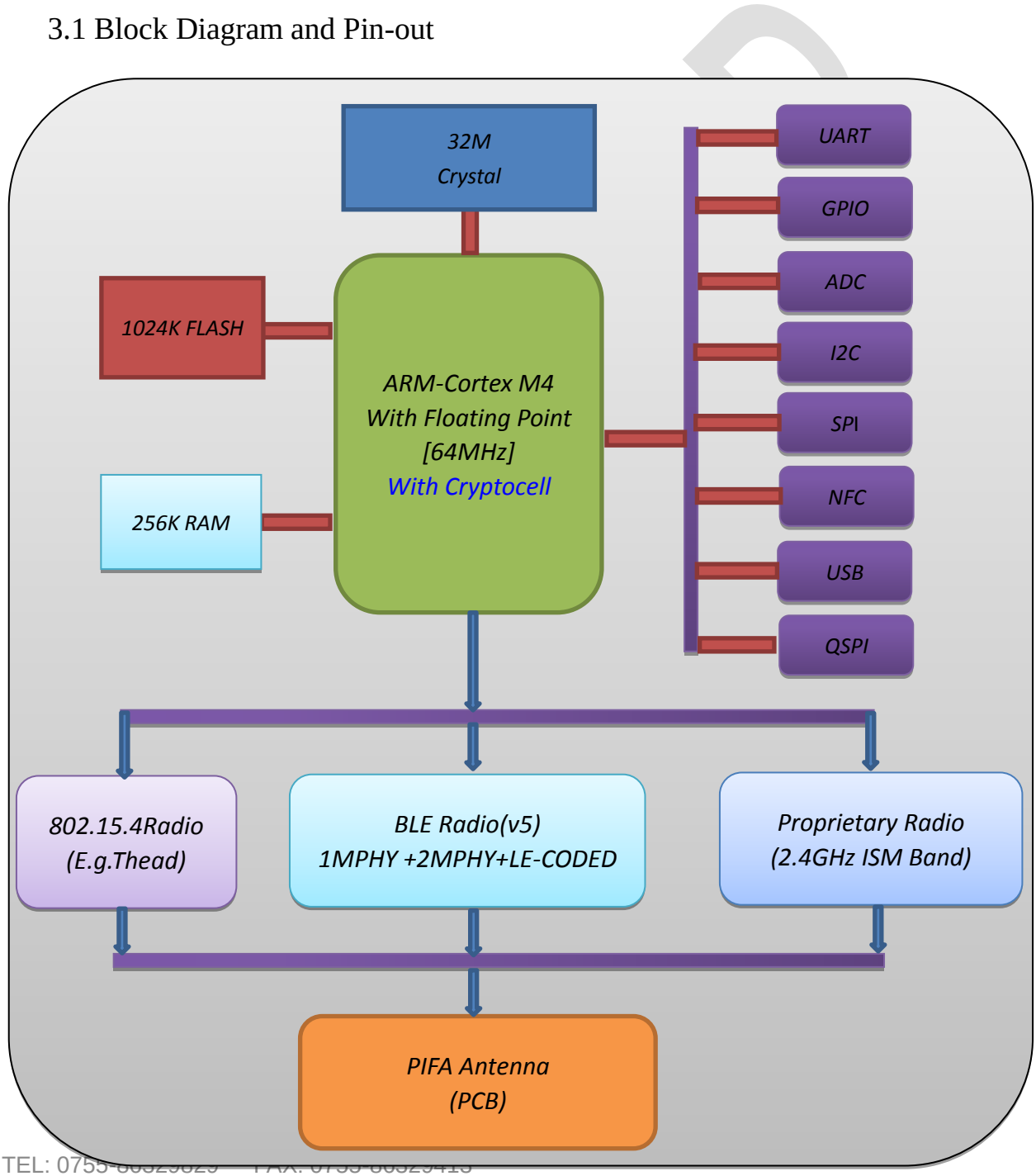


Figure 1: ND06 Block diagram

3.2 Pin Definitions

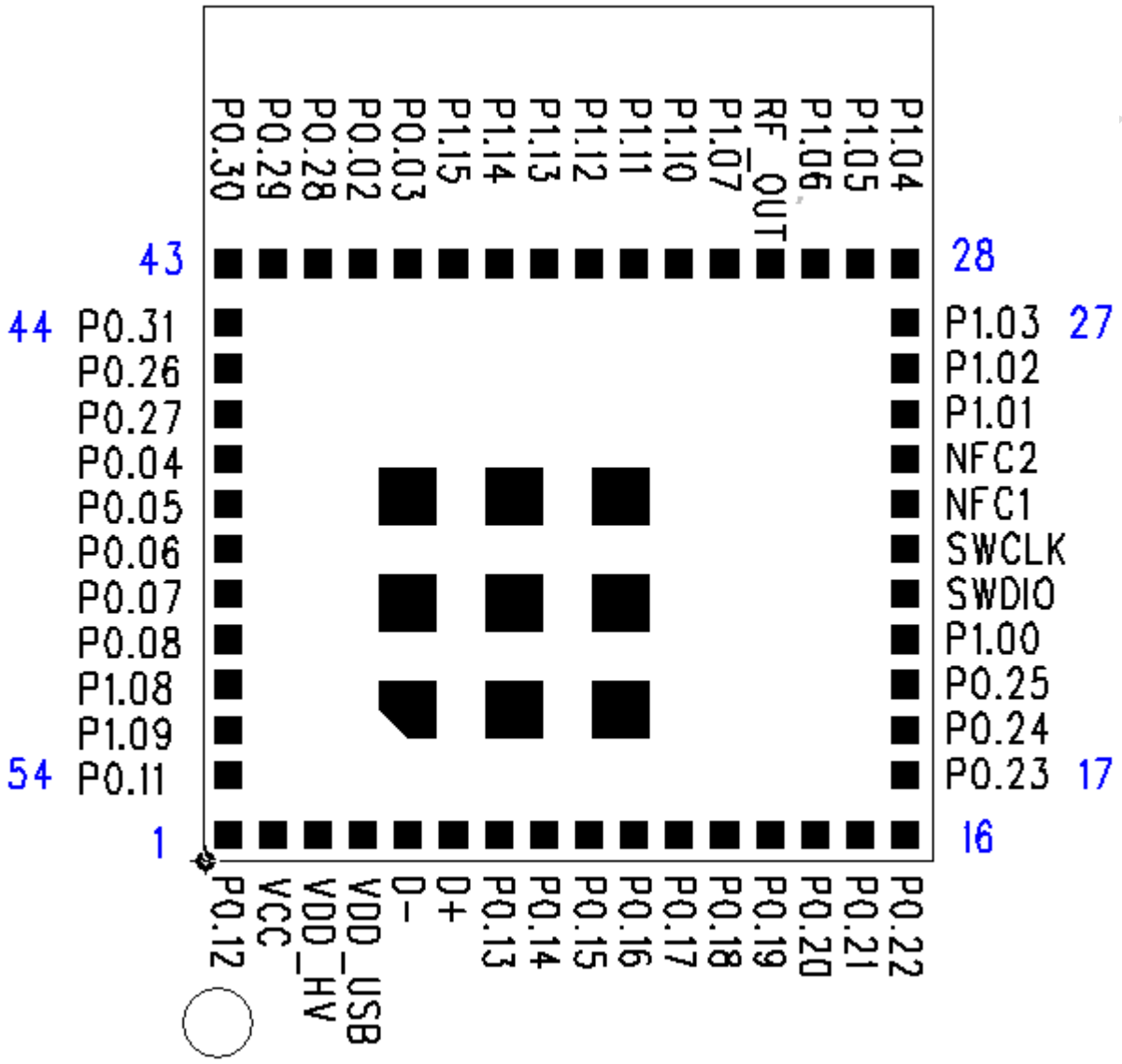


Figure 2: ND06 module pin-out (top view).

Table 1: Pin definitions

Pin #	Pin Name	Default Function	Alternate Function	note
1	P0.12	SIO_12	-	-
2	VCC	Power 1.7V to 3.6V	-	1.7V to 3.6V
3	VDD_HV	Power 2.5V to 5.5V	-	2.5V to 5.5V
4	VDD_USB	4.35V ~5.5V	-	4.35V ~5.5V
5	D-	D-	D-	D-
6	D+	D+	D+	D+
7	P0.13	GPIO_13	-	LED
8	P0.14	GPIO_14	-	LED
9	P0.15	GPIO_15	-	LED
10	P0.16	GPIO_16	-	LED
11	P0.17	GPIO_17	QSPI_CS	LED
12	P0.18	nRESET	-	System Reset (Active Low)
13	P0.19	GPIO_19	QSPI_CLK	-
14	P0.20	GPIO_20	QSPI_DIO0	-
15	P0.21	GPIO_21	QSPI_DIO1	-
16	P0.22	GPIO_22	QSPI_DIO2	-
17	P0.23	GPIO_23	QSPI_DIO3	-
18	P0.24	GPIO_24	-	BUTTON
19	P0.25	GPIO_25	-	BUTTON
20	P1.00	GPIO_1.00	-	-
21	SWDIO	SWDIO	-	Connect to the j - link
22	SWCLK	SWCLK	-	Connect to the j - link
23	NFC1	NFC1/SIO_09	-	SIO_09
24	NFC2	NFC2/SIO_10	-	SIO_10
25	P1.01	GPIO_1.01	-	-
26	P1.02	GPIO_1.02	-	-
27	P1.03	nAutoRUN	nAutoRUN	FTDI USB_DTR via jumper on J12pin1-2.
28	P1.04	GPIO_1.04	-	-
29	P1.05	GPIO_1.05	-	-

30	P1.06	GPIO_1.06	-	-
31	RF_OUT	RF-interface	-	-
32	P1.07	GPIO_1.07	-	-
33	P1.10	GPIO_1.10	-	-
34	P1.11	GPIO_1.11	-	-
35	P1.12	GPIO_1.12	SPI_CS	SPI EEPROM. SPI_Eeprom_CS, Input
36	P1.13	GPIO_1.13	-	-
37	P1.14	GPIO_1.14	-	-
38	P1.15	GPIO_1.15	-	-
39	P0.03	GPIO_0.03	-	Temp Sens Analog
40	P0.02	GPIO_0.02	-	Internal pull-down. Pull High externally to enter VSP (Virtual Serial Port) Service
41	P0.28	GPIO_0.28	-	-
42	P0.29	GPIO_0.29	-	-
43	P0.30	GPIO_0.30	-	-
44	P0.31	GPIO_0.31	-	-
45	P0.26	GPIO_0.26	I2C_SDA	I2C RTC chip. I2C data line
46	P0.27	GPIO_0.27	I2C_SCL	I2C RTC chip. I2C clock line.
47	P0.04	GPIO_0.04	SPI_MISO	SPI EEPROM. SPI_Eeprom_MISO, Input. SPIOPEN in smartBASIC selects SPI function; MOSI and CLK are outputs when in SPI master mode
48	P0.05	GPIO_0.05	UART_RTS	UARTCLOSE() selects DIO functionality. UARTOPEN selects UART COMMS behaviour
49	P0.06	GPIO_0.06	UART_TX	UARTCLOSE() selects DIO functionality. UARTOPEN() selects UART COMMS behaviour
50	P0.07	GPIO_0.07	UART_CTS	UARTCLOSE() selects DIO functionality. UARTOPEN() selects UART COMMS behaviour
51	P0.08	GPIO_0.08	UART_RX	UARTCLOSE() selects DIO functionality. UARTOPEN() selects UART COMMS behavior
52	P1.08	GPIO_1.08	SPI_MOSI	SPI EEPROM. SPI_Eeprom_MOSI,

				Output *SPIOPEN() in smartBASIC selects SPI function, MOSI and CLK are outputs in SPI master*
53	*P1.09*	*GPIO_1.09*	*SPI_CLK*	*SPI EEPROM.* *SPI_Eeprom_CLK,* *Output:* *smartBASIC selects SPI function, MOSI and CLK are outputs when in SPI master mode.*
54	*P0.11*	*GPIO_0.11*	*-*	*BUTTON*

3、POWER CONSUMPTION

Data at VDD of 3.3 V with internal (to chipset) LDO ON or with internal (to chipset) DCDC ON and 25° C.

4.1 Power consumption

Table 2: Power consumption

Parameter	*LDO mode*	*DCDC mode*	*Unit*
Tx only run peak current @ Txpwr = +8 dBm	*32.7*	*14.8*	*mA*
Tx only run peak current @ Txpwr = +4 dBm	*21.4*	*9.6*	*mA*
Tx only run peak current @ Txpwr = 0 dBm	*10.6*	*4.8*	*mA*
Tx only run peak current @ Txpwr = -4 dBm	*8.1*	*3.3*	*mA*
Tx only run peak current @ Txpwr = -8 dBm	*7.2*	*3.1*	*mA*
Tx only run peak current @ Txpwr = -12 dBm	*6.4*	*3.0*	*mA*
Tx only run peak current @ Txpwr = -16 dBm	*6.0*	*2.8*	*mA*
Tx only run peak current @ Txpwr = -20 dBm	*5.6*	*2.7*	*mA*
Tx only run peak current @ Txpwr = -40 dBm	*4.6*	*2.3*	*mA*

Table 3: UART power consumption

Parameter	*Min*	*Typ*	*Max*	*Unit*
UART Run current @ 115200 bps	*-*	*55*	*-*	*μ A*
UART Run current @ 1200 bps	*-*	*55*	*-*	*μ A*
Idle current for UART (no activity)	*-*	*1*	*-*	*μ A*
UART Baud rate	*1.2*	*-*	*1000*	*kbps*

Table 4: power consumption

Parameter	*Min*	*Typ*	*Max*	*Unit*
SPI Master Run current @ 2 Mbps	*-*		*50*	*μ A*
SPI Master Run current @ 8 Mbps	*-*		*50*	*μ A*
Idle current for SPI (no activity)		*<1*		*μ A*
SPI bit rate			*8*	*Mbps*

Table 5: I2C power consumption

Parameter	Min	Typ	Max	Unit
I2C Run current @ 100 kbps	-	*50*	-	*μ A*
I2C Run current @ 400 kbps	-	*50*	-	*μ A*
I2C Bit rate	*100*	-	*400*	*μ A*

Table 6: ADC power consumption

Parameter	Min	Typ	Max	Unit
I2C Run current @ 100 kbps	-	*700*	-	*μ A*

4.2 Radio Frequence（RF）

- 2402 – 2480 MHz Bluetooth Low Energy radio BT5.0 – 1 Mbps, 2 Mbps, and Long-range (125 kbps and 500 kbps) overthe-air data rate.
- Tx output power of +8 dBm programmable down to 7dBm, 6dBm, 5dBm, 4dBm, 2dBm, 0dBm and further down to -20 dBm in steps of 4 dB and final TX power level of -40 dBm.
- Receiver (with integrated channel filters) to achieve maximum sensitivity -95 dBm @ 1 Mbps BLE, -92 dBm @2 Mbps, -103 dBm @ 125 kbps long-range and -99 dBm @500kbps long-range).
- **RF conducted interface available in the following:**
  - RF connected to on-board PCB trace antenna
- Received Signal Strength Indicator (RSSI)
- RSSI accuracy (valid range -90 to -20dBm) is ±2dB typical
- RSSI resolution 1dB typical

4.2 NFC

- Based on the NFC forum specification
  - 13.56 MHz
  - Date rate 106 kbps
  - NFC Type2 and Type4 tag emulation
- Modes of operation:
  - Disable
  - Sense
  - Activated

4.2.1

USE CASES

- Touch-to Pair with NFC
- Launch a smartphone app (on Android)
- NFC enabled Out-of-Band Pairing
- System Wake-On-Field function
  - Proximity Detection

Table 7: NFC interface

Signal Name	Pin Number	I/O	Comments
NFC1/SIO_09	23	IO	The NFC pins are by default NFC pins and an alternate function on each pin is GPIO. Refer to the smartBASIC. User manual.
NFC2/SIO_10	24	IO	

4.2.2

NFC Antenna Coil Tuning Capacitors

From Nordic nRF52840 Objective Product Specification v1.0：

http://infocenter.nordicsemi.com/pdf/nRF52840_PS_v1.0.pdf

The NFC antenna coil must be the connected differential between the NFC1 and NFC2 pins of the ND06.Two external capacitors should be used to tune the resonance of the antenna circuit to 13.56 MHz(Figure 1).

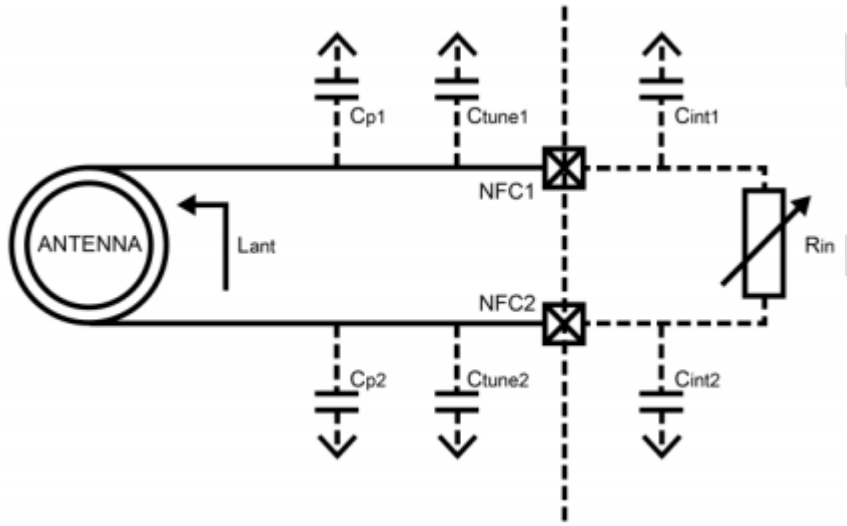


Figure 1: NFC antenna coil tuning capacitors

The required external tuning capacitor value is given by the following equations:

$$C_{tune} = \frac{2}{(2\pi \cdot 13.56\ MHz)^2 \cdot L_{ant}} - C_{tune} - C_{int}$$

An antenna inductance of Lant = 0.72 uH provides tuning capacitors in the range of 300 pF on each pin.The total capacitance on NFC1 and NFC2 must be matched. Cint and Cp are small usually (Cint is 4pF), so can omit from calculation.

4.2.3

UART Interface

Note: The ND06 has two UARTs.

The Universal Asynchronous Receiver/Transmitter (UART) offers fast, full-duplex, asynchronous serial communication with built-in flow control support (UART_CTS, UART_RTS) in HW up to one Mbps baud. Parity checking and generation for the ninth data bit are supported.

UART_TX, UART_RX, UART_RTS, and UART_CTS form a conventional asynchronous serial data port with handshaking. The interface is designed to operate correctly when connected to other UART devices such as the 16550A. The signaling levels are nominal 0 V and 3.3 V (tracks VDD) and are inverted with respect to the signaling on an RS232 cable.

Two-way hardware flow control is implemented by UART_RTS and UART_CTS. UART_RTS is an output and UART_CTS is an input. Both are active low.

These signals operate according to normal industry convention. UART_RX, UART_TX, UART_CTS, UART_RTS are all 3.3 V level logic (tracks VDD). For example, when RX and TX are idle they sit at 3.3 V. Conversely for handshaking pins CTS, RTS at 0 V is treated as an assertion.

The module communicates with the customer application using the following signals:

- Port/TxD of the application sends data to the module’s UART_RX signal line
- Port/RxD of the application receives data from the module’s UART_TX signal line

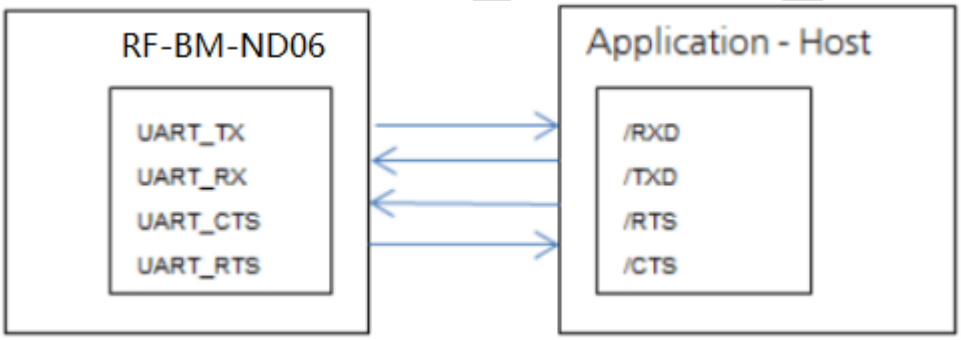


Figure 2: UART signals

Table 8: UART interface

Signal Name	*Pin Number*	*I/O*	*Comments*
P0.06 / UART_Tx	***49***	***O***	***(alternative function UART_Tx) is an output, set high (in firmware)***
P0.08 / UART_Rx	***52***	***I***	***(alternative function UART_Rx) is an input, set with internal pull-up (in firmware).***
P0.05 /UART_RTS	***38***	***O***	***(alternative function UART_RTS) is an output, set low (in firmware)***
P0.07/UART_CTS	***50***	***I***	***(alternative function UART_CTS) is an input, set with internal***

			pull-down (in firmware).

4.2.4

USB interface

ND06 has USB2.0 FS (Full Speed, 12Mbps) hardware capability. There is a CDC driver/Virtual UART as well as other USB drivers available via Nordic SDK – such as: usb_audio, usb_hid, usb_generic, usb_msc (mass storage device)

Table 9: **USB interface**

Signal Name	*Pin Number*	*I/O*	*Comments*
D-	***5***	***I/O***	
D+	***6***	***I/O***	
VBUS	***4***	***When using the ND06 VBUS pin (which is mandatory when USB interface is used), Customer MUST connect externally a 4.7uF capacitor to ground.*** ***Note:*** ***You MUST power the rest of ND06 module circuitry through the VDD pin (OPTION1) or VDD_HV pin (OPTION2).***	

4.2.5

SPI Bus

The module is a master device that uses terminals SPI_MOSI, SPI_MISO, and SPI_CLK. SPI_CS is implemented using any spare GPIO digital output pins to allow for multi-dropping

The SPI interface enables full duplex synchronous communication between devices. It supports a 3-wire (SPI_MOSI, SPI_MISO, SPI_SCK,) bidirectional bus with fast data transfers to and from multiple slaves. Individual chip select signals are necessary for each of the slave devices attached to a bus, but control of these is left to the application through use of SIO signals. I/O data is double-buffered.

Table 10: SPI interfaces

Signal Name	Pin No.	I/O	Comments
P1.08/SPI_MOSI	52	O	This interface is an alternate function configurable by *smart*BASIC. Default in the FW pin 56 and 53 are SIO inputs. SPIOPEN() in *smart*BASIC selects SPI function and changes pin 56 and 53 to outputs (when in SPI master mode).
P0.04/SPI_MISO	47	I	
P1.09/SPI_CLK	53	O	
P1.12 or any/SPI_CS	35	IO	

4.2.6

IIC Interface

The two-wire interface can interface a bi-directional wired-OR bus with two lines (SCL, SDA) and has master /slave topology. The interface is capable of clock stretching. Data rates of 100 kbps and 400 kbps are supported.

IMPORTANT: It is essential to remember that pull-up resistors onboth SCL and SDA lines are not provided in the module and MUST be provided external to the module.

Table 11: I2C interface

Signal Name	Pin No.	I/O	Comments
P0.26/I2C_SDA	45	I/O	This interface is an alternate function on each pin, configurable by *smart*BASIC. I2COPEN() in *smart*BASIC selects I2C function.
P0.27/I2C_SCL	46	I/O	

4.2.7

GPIO

The 19 SIO pins are configurable by smartBASIC application script or Nordic SDK. They can be accessed individually. Each has the following user configured features:

- Input/output direction
- Output drive strength (standard drive 0.5 mA or high drive 5mA)
- Internal pull-up and pull-down resistors (13 K typical) or no pull-up/down or input buffer disconnect
- Wake-up from high or low-level triggers on all pins including NFC pins

4.2.8

Anglog interface(ADC)

The ND06 provides access to 8-channel 8/10/12-bit successive approximation ADC in one-shot mode. This enables sampling up to 8 external signals through a front-end MUX. The ADC has configurable input and reference pre-scaling and sample resolution (8, 10, and 12 bit).

Table 12: Analog interface

Signal Name	Pin No.	I/O	Comments
P0.05– Analog Input	48	I	This interface is an alternate function on each pin, configurable by smartBASIC. AIN configuration selected using GpioSetFunc() function. Configurable 8, 10, 12-bit resolution. Configurable voltage scaling 4, 2, 1/1, 1/3, 1/3, 1/4, 1/5, 1/6(default). Configurable acquisition time 3uS, 5uS, 10uS(default), 15uS, 20uS, 40uS. Full scale input range (VDD)
P0.04 – Analog Input	47	I	
P0.03 – Analog Input	39	I	
P0.02 – Analog Input	40	I	
P0.31 – Analog Input	44	I	
P0.30 – Analog Input	43	I	
P0.29 – Analog Input	42	I	
P0.28 – Analog Input	41	I	

4.2.9

PWM SIGNAL OUTPUT

The **PWM output** signal has a frequency and duty cycle property. Frequency is adjustable (up to 1 MHz) and the duty cycle can be set over a range from 0% to 100%.

PWM output signal has a frequency and duty cycle property. PWM output is generated using dedicated hardware in the chipset. There is a trade-off between PWM output frequency and resolution.

For example:

- PWM output frequency of 500 kHz (2 uS) results in resolution of 1:2.
- PWM output frequency of 100 kHz (10 uS) results in resolution of 1:10.
- PWM output frequency of 10 kHz (100 uS) results in resolution of 1:100.
- PWM output frequency of 1 kHz (1000 uS) results in resolution of 1:1000.

4.3.0

n-RESET PIN

Table 13: nRESET pin

Signal Name	Pin No	I/O	Comments
nRESET	12	I	ND06 HW reset (active low). Pull the nRESET pin low for minimum 100mS for the ND06 to reset.

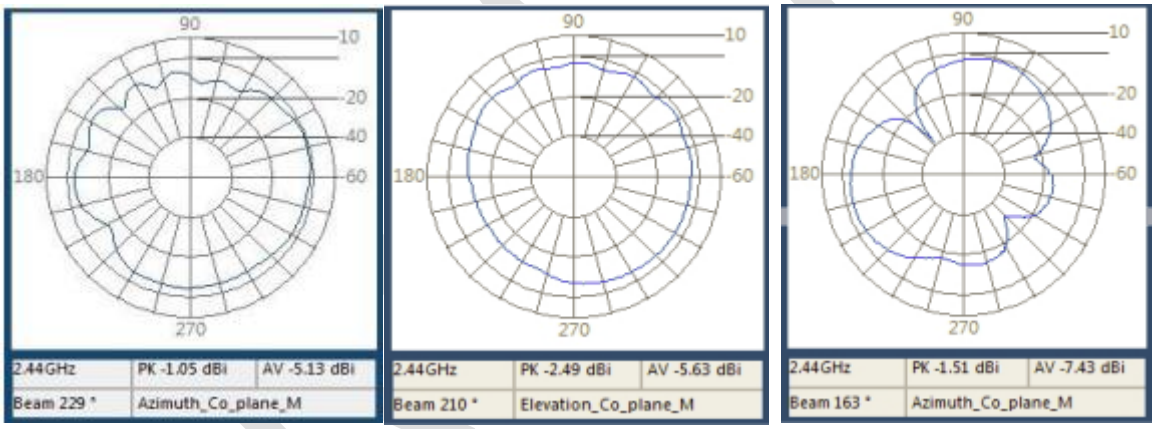
4.2 Antenna data on demo board

Table 14: Antenna gain

Unit in dBi @2440MHz	XY-plane		XZ-plane		YZ-plane	
	Peak	Avg	Peak	Avg	Peak	Avg
451-00001 PCB trace antenna	-1.05	-5.13	-1.51	-7.43	-2.49	-5.63

◆

XY-plane ◆XZ-plan ◆YZ-plane



4、PCB Layout on host PCB-General

Checklist (for PCB):

- MUST locate ND06 module close to the edge of PCB
- For best antenna performance, place the ND06 module on the edge of the host PCB, preferably in the edge center.
- The ND06 development board has the ND06 module on the edge of the board (not in the corner). The antenna keep-out area is defined by the ND06 development board which was used for module development and antenna performance evaluation is shown in **Figure 2**
- Any metal closer than 20 mm will begin to significantly degrade performance (S11, gain, radiation efficiency).

- It is best that you test the range with a mock-up (or actual prototype) of the product to assess effects of enclosure height (and materials, whether metal or plastic).

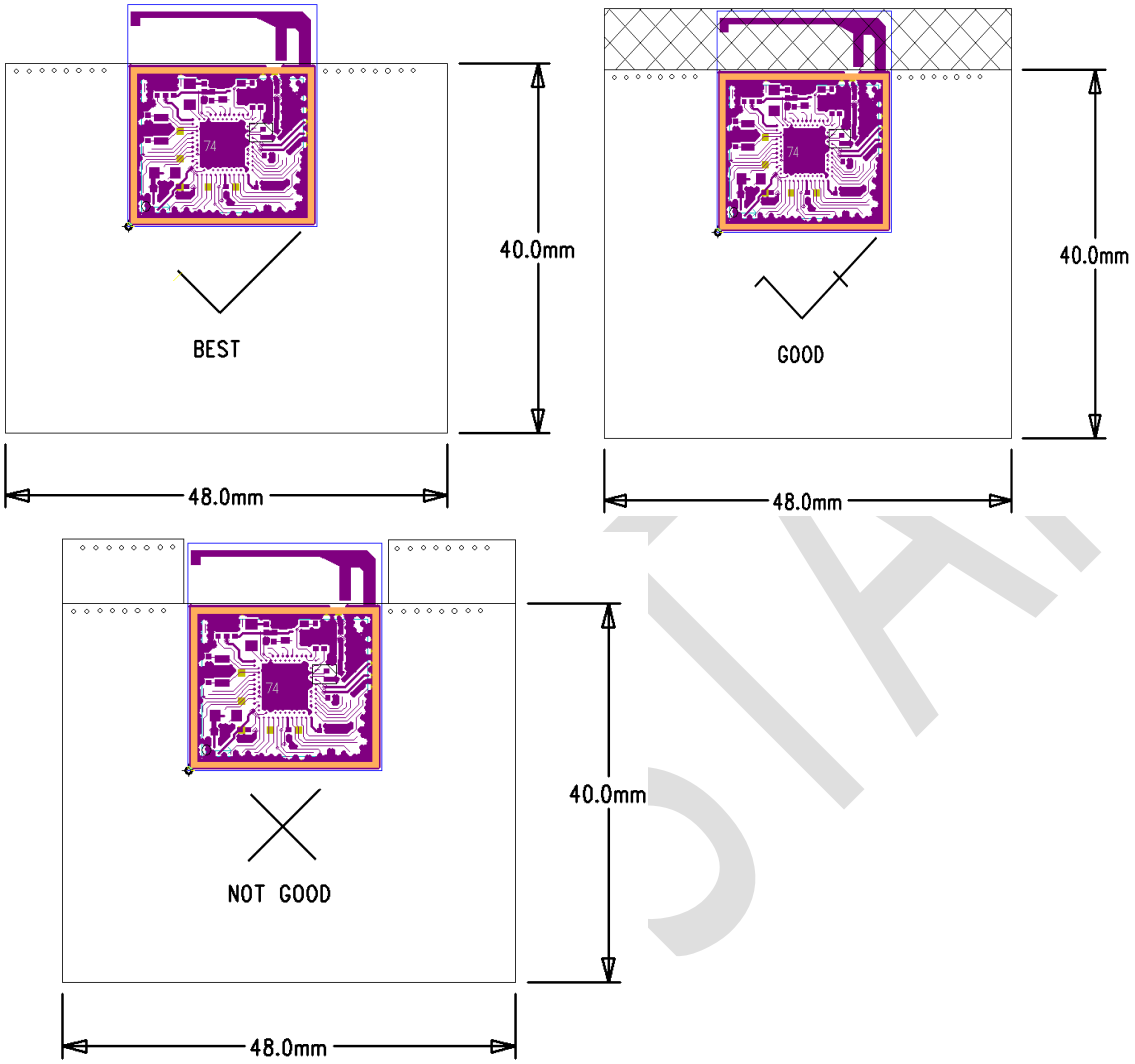
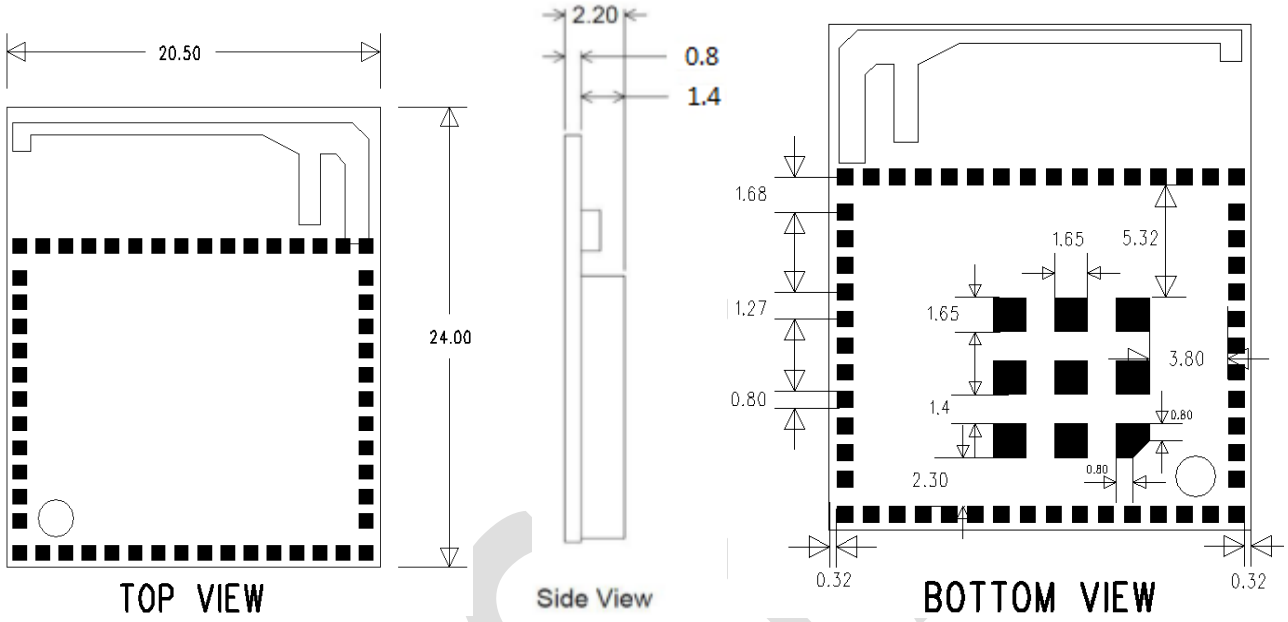


Figure 2: PCB trace Antenna keep-out area

5、MECHANICAL DETAILS

6.1 RF-BM-ND06 Mechanical details(*Unit:mm*)



Unit:mm

Figure 3: ND06 mechanical drawings

6、Recommended baking times and temperatures

***Table 15:** Recommended baking times and temperatures*

MSL	125°C Baking Temp.		90°C/≤ 5%RH Baking Temp.		40°C/ ≤ 5%RH Baking Temp.	
	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%	Saturated @ 30°C/85%	Floor Life Limit + 72 hours @ 30°C/60%
3	9 hours	7 hours	33 hours	23 hours	13 days	9 days

RFSTAR surface mount modules are designed to be easily manufactured, including reflow soldering to a PCB. Ultimately it is the responsibility of the customer to choose the appropriate solder paste and to ensure oven temperatures during reflow meet the requirements of the solder paste. RFSTAR surface mount modules conform to J-STD-020D1 standards for reflow temperatures.

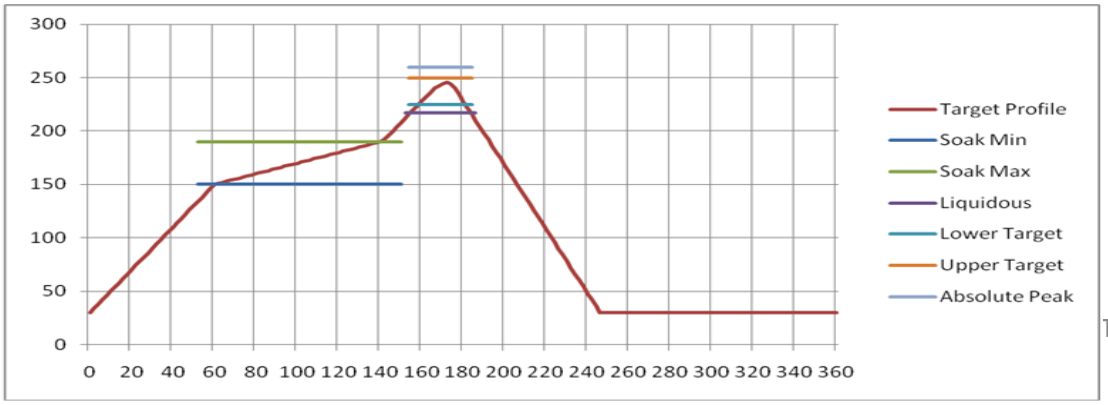


Figure 3: Recommended reflow temperature

Temperatures should not exceed the minimums or maximums presented in Table 16.

Table 16: Recommended maximum and minimum temperatures

Specification	Value	Unit
Temperature Inc./Dec. Rate (max)	1~3	℃ / Sec
Temperature Decrease rate (goal)	2-4	℃ / Sec
Soak Temp Increase rate (goal)	5 - 1	℃ / Sec
Flux Soak Period (Min)	70	Sec
Flux Soak Period (Max)	120	Sec
Flux Soak Temp (Min)	150	℃
Flux Soak Temp (max)	190	℃
Time Above Liquidous (max)	70	Sec
Time Above Liquidous (min)	50	Sec
Time In Target Reflow Range (goal)	30	Sec
Time At Absolute Peak (max)	5	Sec
Liquidous Temperature (SAC305)	218	℃
Lower Target Reflow Temperature	240	℃
Upper Target Reflow Temperature	250	℃
Absolute Peak Temperature	260	℃

7、Schematic reference design

- ***Nordic nRF52840 Reference Schematic***

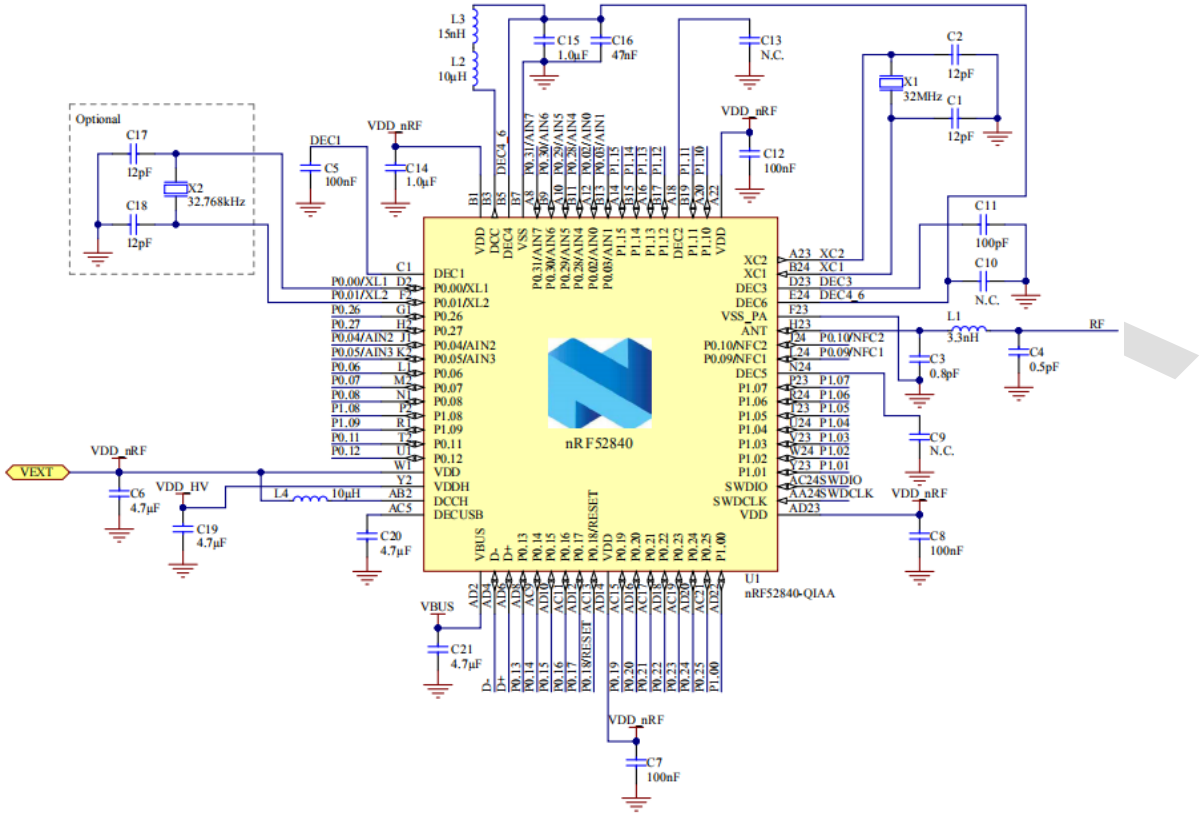


Figure 4: Nordic nRF52840 Reference Schematic

- ***ND06 Modele Reference Schematic***

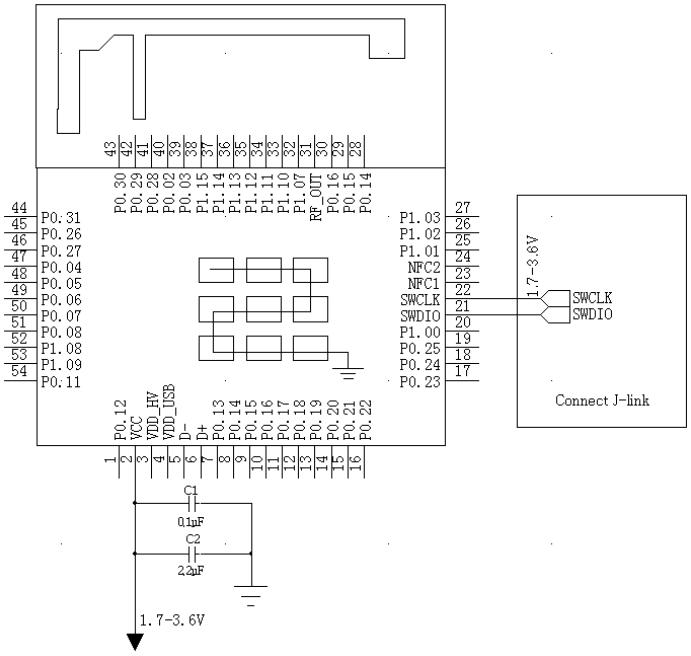


Figure 5: ND06 Modele Reference Schematic

- ***ND06 High voltage mode VDD_HV 2.5V-5.5V Internal DCDC converter or LDO***

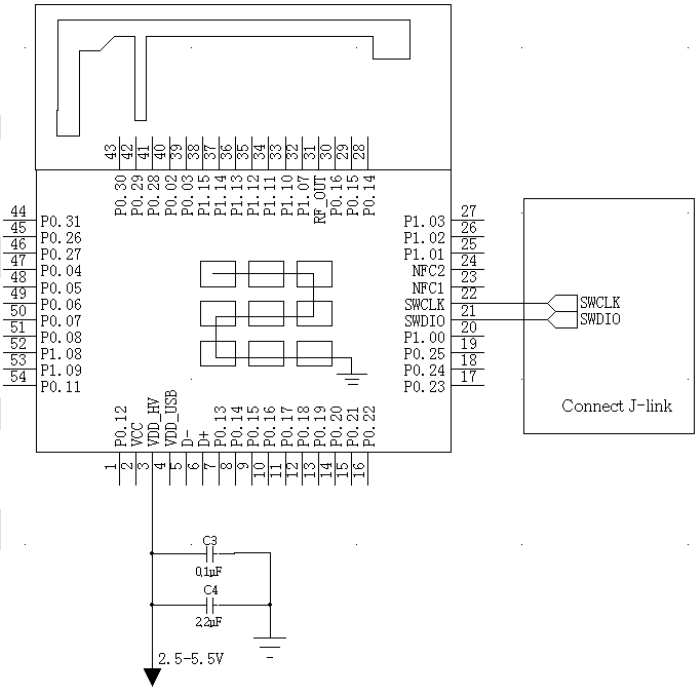


Figure 6: High voltage mode VDD_HV 2.5V-5.5V Internal DCDC converter or LDO

Contact us

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