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ESD & Latch-Up Qualification Report

PART NO.:**NUC972DF62Y**

Version: B

PKG type: LQFP216

Lot No.:E448M003

FUNCTION: ARM926EJ-S Based 32-bit Micro Processor

PROCESS: SMIC 0.11um

PASS/FAIL: PASS

Report Date: Feb./2015

---SUMMARY---

The ESD and Latch-Up test results for NUC972DF62Y are:

- ESD-HBM stress voltage +/- 2KV: Pass
- ESD-MM stress voltage +/- 200V: Pass
- ESD-RCDM stress voltage +/- 500V: Pass
- ESD-SCDM stress voltage +/- 500V: Pass
- Latch-Up stress current +/-100mA: Pass

Note.
ESD: Positive (+) & Negative (-) zap on the same part.
PD & ND zap together on 36ea parts for each mode

Latch-Up: Vdd1max=3.63V, Vdd2max=1.96V, Vdd3max=1.32V,Idd clamp@1A; for all I/O pins, Vt clamped@+5.445V and -1.815V, Overvoltage trigger 5.445V to Vdd1 power pins, overvoltage trigger 2.94V to Vdd2 power pins, overvoltage trigger 1.98V to Vdd3 power pins.

A. Introduction

1. ESD

1.1 SCOPE

ESD test is to evaluate the immunity of device to electrostatic discharge.

1.2 TEST CONDITION

JESD22-A114

JESD22-A115/ EIAJ-IC-121

JESD22-C101

Zapping start voltage : 1 KV (HBM), 100V(MM), 250V (CDM)

Zapping times per pin per voltage : 1

1.3 Stress Mode

PD : Positive pulse zap from test pin in turn to combined Vdd pins,other pins no connection.

ND : Negative pulse zap from test pin in turn to combined Vdd pins,other pins no connection.

PS : Positive pulse zap from test pin in turn to combined Vss pins,other pins no connection.

NS : Negative pulse zap from test pin in turn to combined Vss pins,other pins no connection.

2. Latch-Up

2.1 SCOPE

Latch-Up test is to evaluate the immunity of the devices to latch-up.

2.2 TEST CONDITION

JEDEC-STD 78, Temp = 25 °C, VDD biased @ Max. Operating Voltage.

Current triggers source and clampps @1.5 times max. signal voltage of the test pin

Current triggers source and clampps @ -0.5 times max signal voltage of the test pin

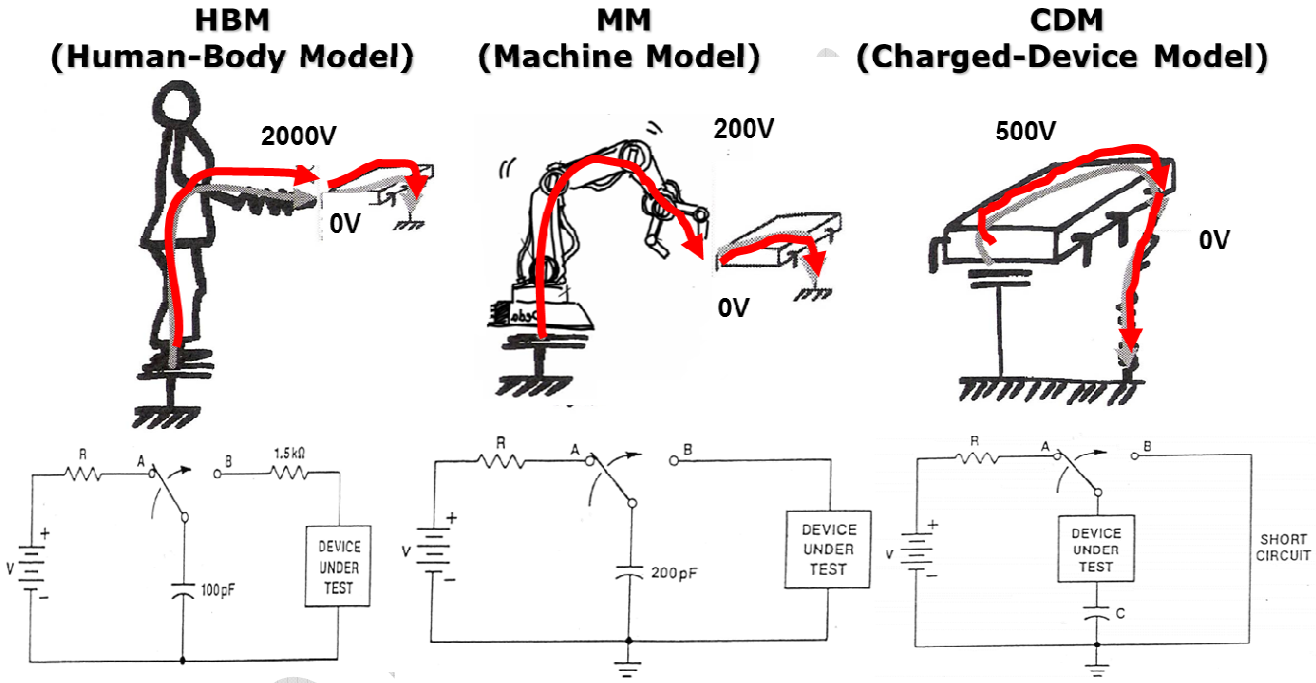
Overvoltage trigger 1.5 times max Vsupply voltage to the Vsupply pins.

Trigger times per pin : 1

B. Application Note (1)

和可靠度相关的电气特性 – Chip ESD

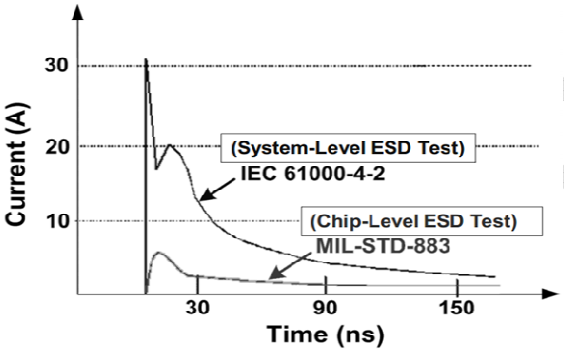
- 3 种不同的 Chip ESD



Application Note (2)

Chip ESD 和 System ESD 是不一样的规格

- 标准不同
  - Chip ESD: HBM MIL-STD-833C, MM: EIA/JESD22-A115-A
  - System ESD: IEC 61000-4-2
- 应用场合不同
  - Chip ESD: 芯片未上电, 应用于生产, 运送中的保护
  - System ESD: 芯片上电, 应用于实际工作状态
- 能量等级不同
  - Chip ESD: HBM 2KV, MM 200V 是一般 IC level
  - System ESD Level 4: Contact Mode 8KV, Air Mode 15KV
  - System ESD 只靠MPU檔不住,需外部保護元件



- **Under 8-kV ESD zapping, the peak current in system-level ESD test is about 5 ~ 6 times larger than that in component-level ESD test**