General Design Recommendation for I2C Interface

This application note is intended to provide general design recommendation for I2C interface to customer. This brief document describes things customer may need to consider when designing I2C interface using Nuvoton's audio product along with external I2C master device.

1 I2C Design Considerations

1.1 MCU I/O type setting for I2C interface

I2C pins of master device are better to be open-drain mode when output, or be high-impedance state when output high. The real output high is driven by pull-high resistors. Normally, hardware I2C has no problem on the I/O output and type change. Programmer has to care about the I/O type change timing when using software.

1.2 Timing

- Latch data on SCL rising edge. Master or slave cannot release the SCL if data is not ready.
- Data preparing after SCL falling edge.
- Meeting the I2C timing specification (described in datasheet).

1.3 Pull-high resistors

These resistors will impact the rising/falling time. Long I2C trace or more I2C slave devices on same I2C bus will have more loading to make slow rising/falling time. Please make sure the data setup and hold time are enough.

1.4 Power on sequence

The setting of the I2C interface of master device should be done first before providing power to audio codec, i.e. NAU8822A, NAU8810, NAU8500, etc. It means the SCL and SDA should be high first before audio codec power on. Otherwise first command to audio codec may fail.

1.5 Voltage Level Translation

There are many I/O standards that have different voltage level requirements for the input voltage and output voltage typically based on the device operating voltage. Based on different operating voltage, bi-directional level shifter may be needed on I2C bus to enable these devices to communicate with each other. We should prevent to use below connections in Figure 1; these connections may cause the communication problem due to different input voltage (VIH or VIL) and output voltage (VOH or VOL).

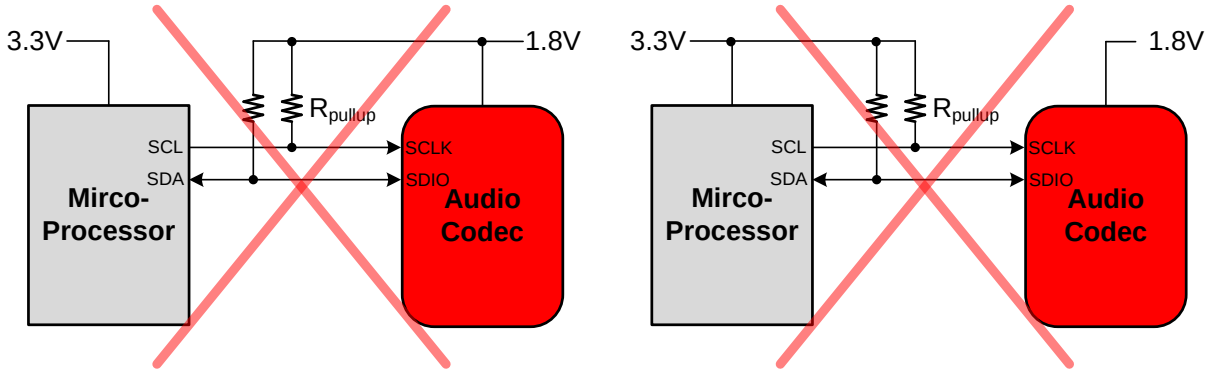

Figure 1. Wrong I2C bus circuit

For I2C-bus bi-directional level shifter design, please refer to Philips Semiconductors (now NXP Semiconductors) Bi-directional level shifter for I2C-bus and other system application note.

1.6 Board noise impact

Large noise on the SCL rising/falling edge has chance to make wrong clock count, also wrong address/data latching or preparing. Following figures show that the noise on the SCL rising and falling edge.

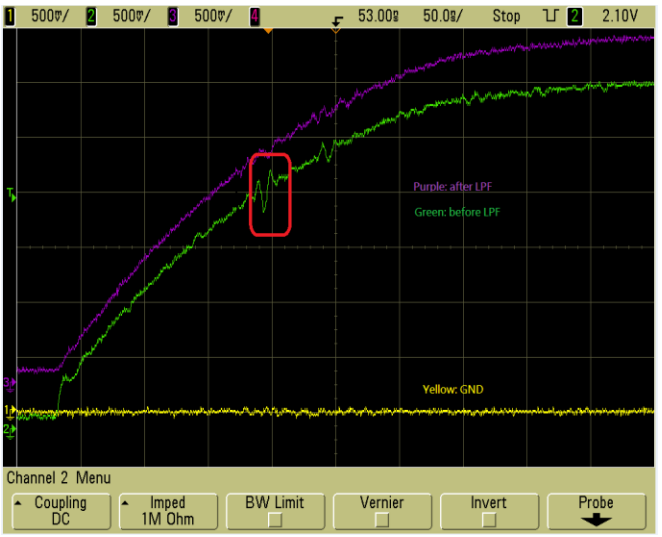

Figure 2. Abnormal SCL rising edge before and after low pass filter

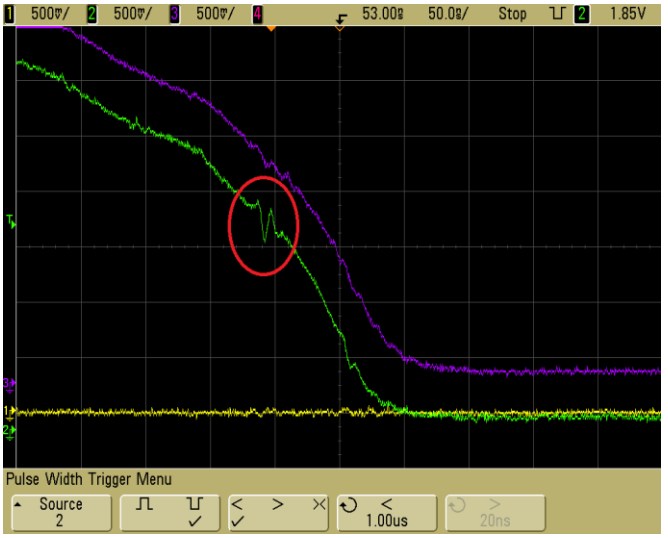

Figure 3. Abnormal SCL falling edge before and after low pass filter

- Wrong clock count may cause I2C bus being locked (SCL is always pulled low by audio codec). Master I2C device can send a dummy clock to release this state.
- Faster rising/falling time will reduce the time duration of wrong count area.
- Be careful on the sampling rate of oscilloscope. In the platform of high frequency system clock, the noise may be megahertz; it needs high resolution oscilloscope (GHz) to sample it out.
- Suitable ferrite bead or RC low pass filter on each input pin may eliminate the noise (Like the purple line in above figures), and the filter should be closed to audio codec, the connection as shown as below.

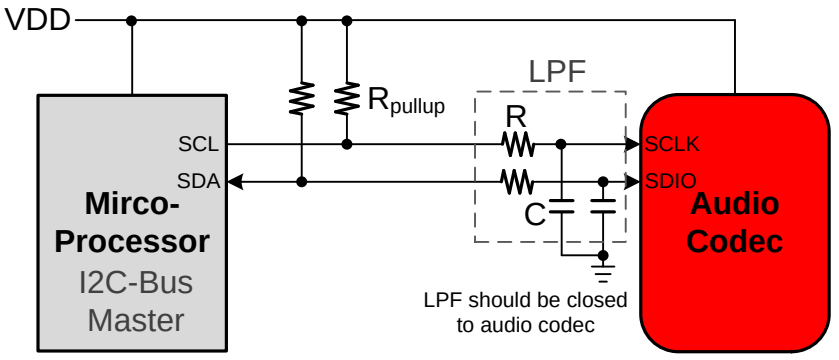

Figure 4. RC Low Pass Filter on I2C Bus

2 Wrong I2C Communication Reference

Audio codec may miss to ACK or drive SDA line low at wrong clock cycle by below reasons.

2.1 Timing Issue

Wrong timing (i.e. setup time and hold time, etc.) can cause the audio codec to get a different data or resulting in a missing acknowledgment.

2.2 Wrong SCL cycle count

Some board noise may appear on SCL line, and audio codec may receive wrong slave device address. Please refer to figure 2 and figure 3. Suggested add low pass filter on I2C path to prevent board noise impact.

2.3 Wrong chip pin configured

Some audio codecs can be controlled by SPI and I2C, please make sure that MODE pin is pulled to ground. In addition, the NAU88L25 I2C has two slave device addresses and can be controlled by GPIO1 pin.

2.4 Pervious incomplete SCL cycles (8-bit block)

When less than eight bits are sent, the audio codec waits for the rest of the SCL clock. Unless the eighth clock is sent, the audio codec will not generate acknowledgment. And the acknowledgment will be generated in next I2C command, and next I2C command will reply non-acknowledgment.

The figure 5 shows that the system power-off and power-on period, the audio codec doesn’t reply the acknowledgment at first I2C command. The figure 6 shows microcontroller stops I2C communication and has incomplete I2C command. Due to the supply voltage doesn’t reach the reset threshold of audio codec’s power-on, so audio codec still waits the rest of SCL clocks at the repower-on period. A way to restart the transmission is starting a new I2C command with Start condition.

Figure 5. The I2C command of power-on and power-off period

Figure 6. Zoom-in 1. The I2C command of power-off period

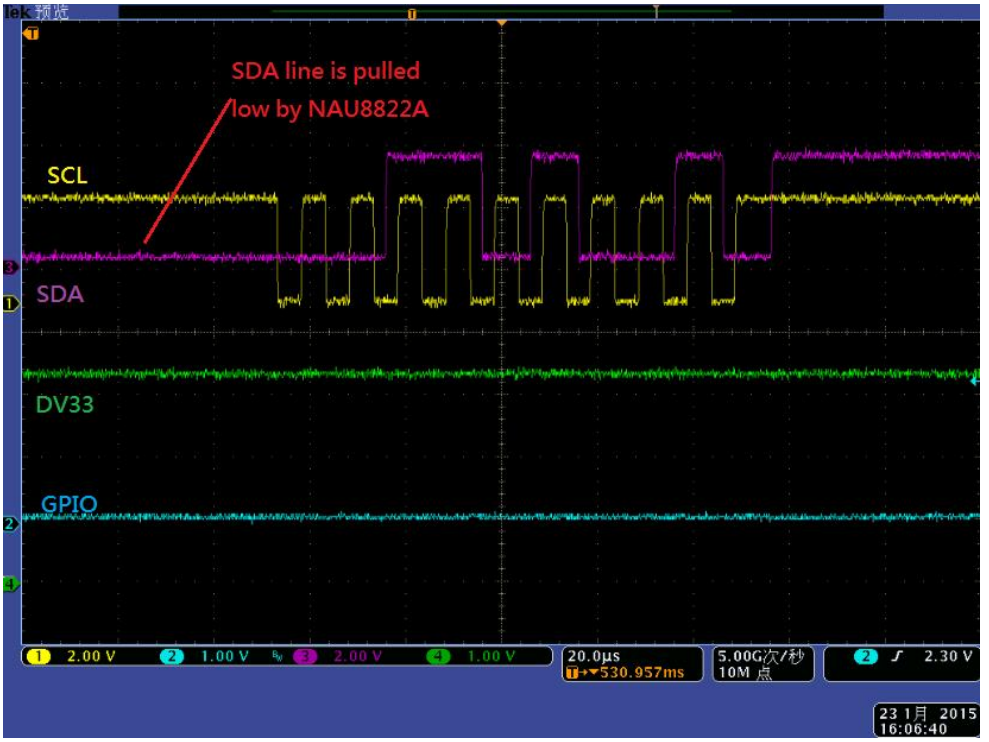

Figure 7. Zoom-in 2. The I2C command of power-on period

3 Revision History

VERSION	DATE	PAGE	DESCRIPTION
0.1	Feb, 2014		Initial Version
0.2	Feb, 2016		Added LPF description in Board Noise Impact section