

NUC972 Development Board

Introduction

Jan. 9th, 2015

Nuvoton Technology Corp.

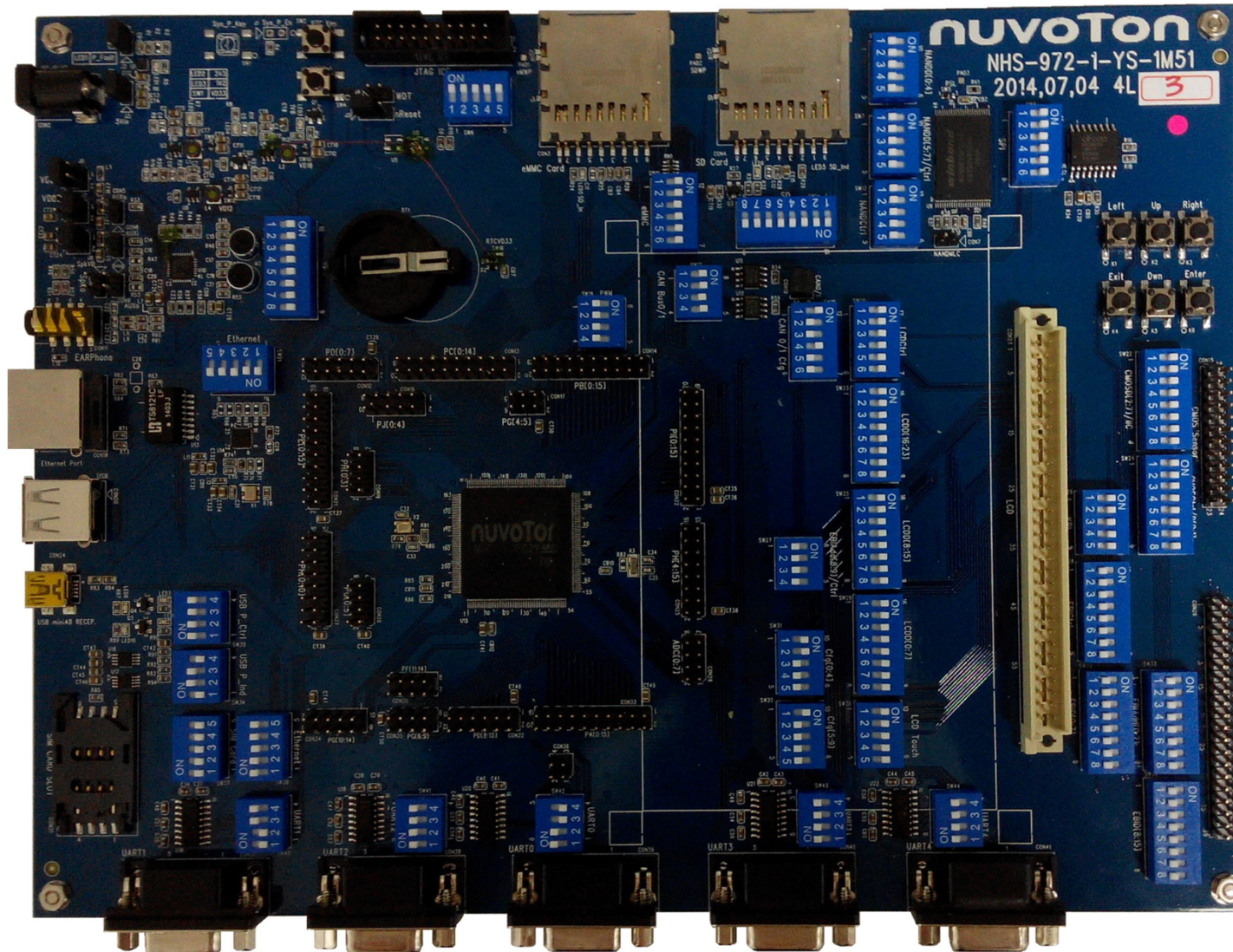
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Overview

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 - **Layout Guideline in Ethernet**



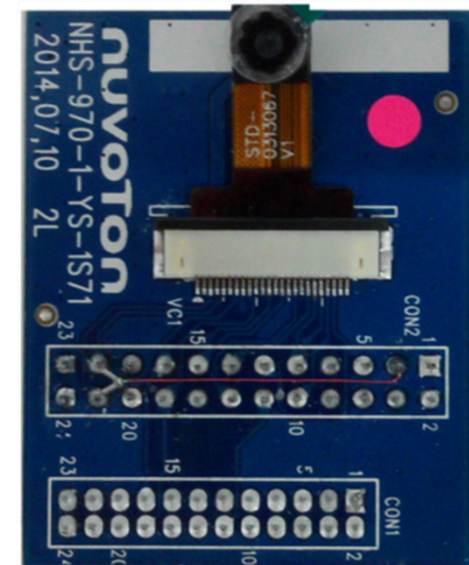
Mainboard Outline



Accessory Board Outline



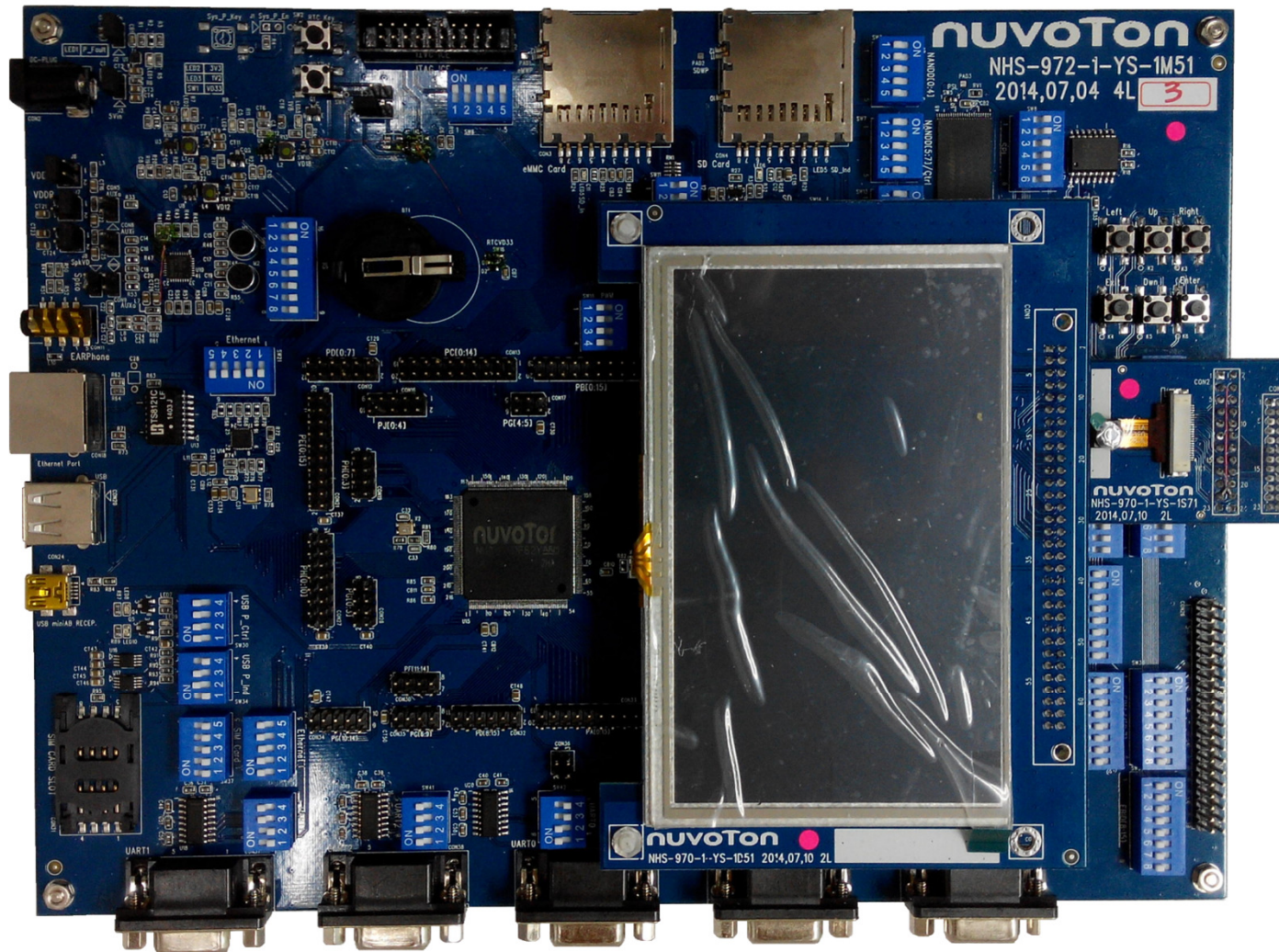
5" 24-bit LCD board



CMOS sensor board

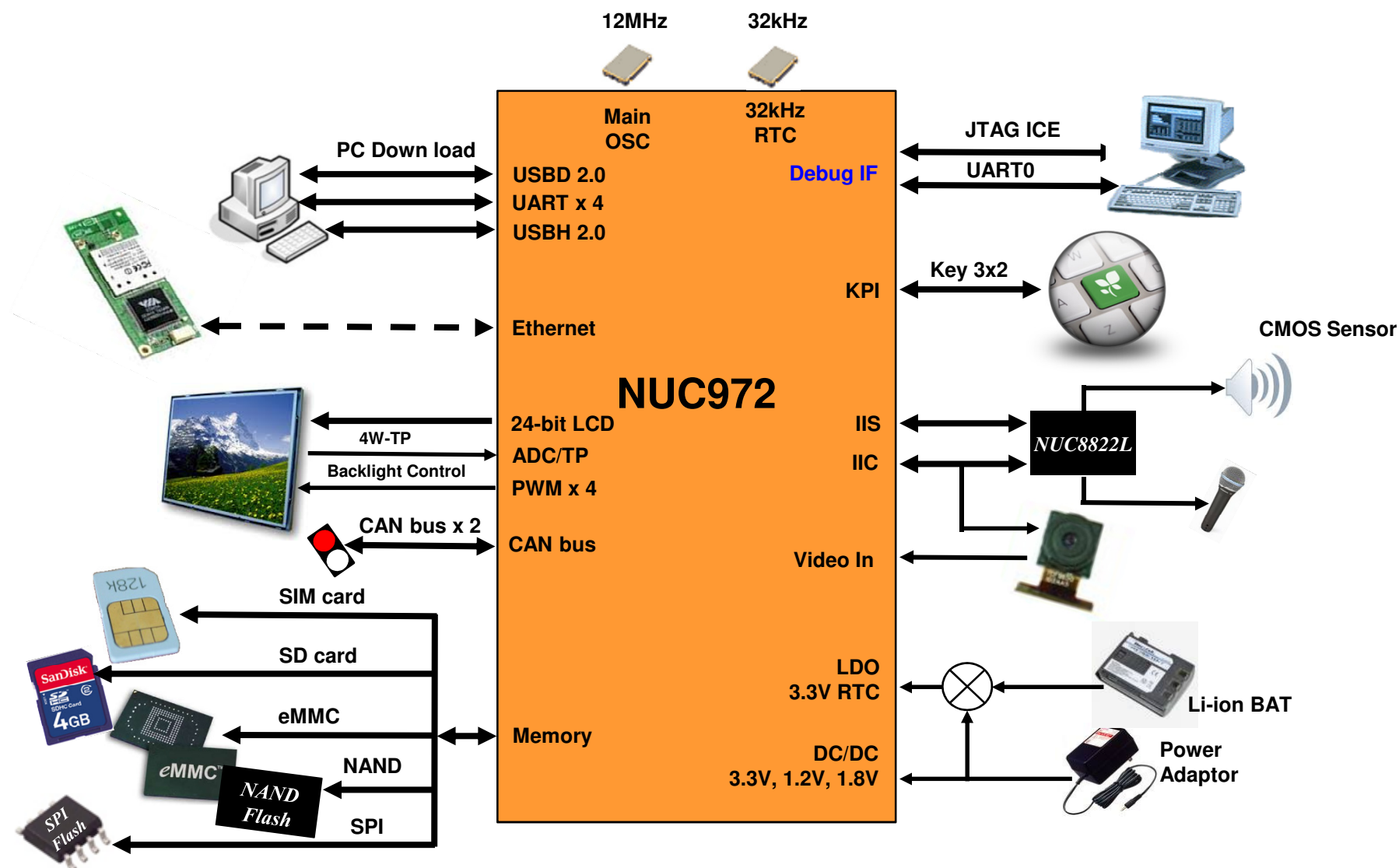
Back to continue

Assembled Board Outline



Back to continue

System Block Diagram



Features I

- **CAN Bus x 2**
- **EBI (External Bus Interface)**
 - 10-bit address bus
 - 16-bit data bus
- **IIS**
 - Audio codec, NUC8822L.
 - Dual microphone.
- **Human Interface:**
 - Power Key x 1, Reset Key x 1
 - 3 x 2 matrix function
 - 5" LCD with 24-bit RGB with resistor type touch panel
 - CMOS sensor

Features II

- **Memory – eMMC card, SD card, NAND flash, SPI flash.**
- **PWM x 4**
- **JTAG ICE**
- **UART x 5**
 - Default is UART 0 for debugging message
- **USB**
 - USB0 is OTG
 - USB1 is Host
- **ADC x 8**
 - ADC0 is for battery detection.
 - ADC [3:7] for touch panel.

NHS-972-1-YS-1M51
2014.07.04 4L

Peripheral Device Port 2

Peripheral Device Port 3

Peripheral Device Port 4

Peripheral Device Port 5

Peripheral Device Port 6

Power Block

JTAG ICE Port

NUC 972

Peripheral Device Port 1

Board Description I

● Power Block

- System power control by RTCWkUp & RTCPWREn.
- RTC power input
 - ◆ LDO – NUC3705
 - ◆ Battery paddle – CR2032.
- JTAG ICE port
 - ◆ U-Link – Not to system reset.

● Peripheral Device 1

- eMMC – bus is shared with NAND flash.
- SD
- NAND – bus is conflicted with eMMC.
- SPI flash – 4-bit.

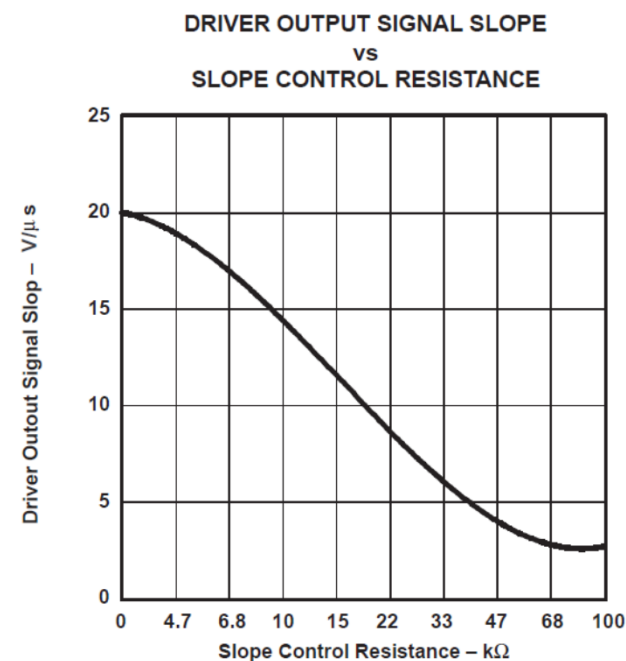
Dev. Board Description II

● Peripheral Device 3

- CAN Bus x 2
 - ◆ Slew rate setting by SW19.
- PWM x 4

● Peripheral Device 2

- IIS – NUC8822L
- Ethernet – RMII
- USB
 - ◆ USB OTG – Control power chip by GPIO.
 - ◆ USB host
- SIM card



Dev. Board Description III

- Peripheral Device 4
 - 3 x 2 matrix Keypads.
 - CMOS sensor.
 - LCD – 5” RGB888.
 - ◆ Touch panel – ADC[3:7].
 - ◆ PWM – Backlight control.
 - EBI pin header.
- Peripheral Device 6
 - UART0 – Debugging message
 - UART[1:4]

Dev. Board Description IV

● Peripheral Device 5

■ Power On Setting

◆ PA[0:9] (= Cfg[0:9])

◆ Setting pin has to be pulled low with a 10KΩ.

Cfg[1:0] =	00 : Boot from USB. 01 : Boot from eMMC. 10 : Boot from NANA Flash. 11 : Boot from SPI Flash.
Cfg2 =	0 : System clock is from 12 MHz crystal. 1 : System clock is from UPLL output.
Cfg3 =	0 : WDT is OFF after power-on. 1 : WDT is ON after power-on.
Cfg4 =	0 : Pin PJ[4:0] used as GPIO pin. 1 : Pin PJ[4:0] used as JTAG interface.

Cfg[7:6] =	00 : NAND Flash page size is 2KB. 01 : NAND Flash page size is 4KB. 10 : NAND Flash page size is 8KB. 11 : Ignore Power-On Setting.
Cfg[9:8] =	00 : NAND Flash ECC type is BCH T12. 01 : NAND Flash ECC type is BCH T15. 10 : NAND Flash ECC type is BCH T24. 11 : Ignore Power-On Setting.

Phenomenon I

● Power Block

■ ICE port reset

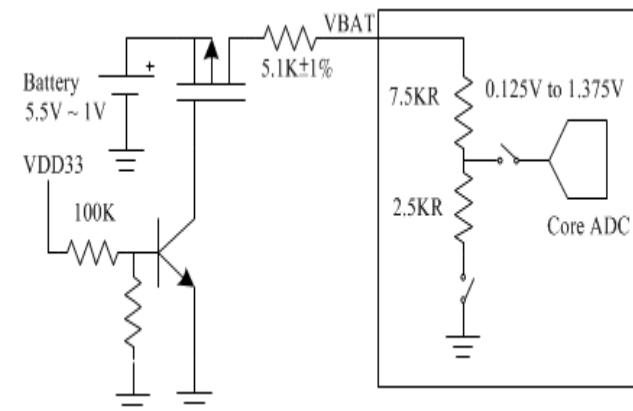
- ◆ U-Link – Not to system reset. Open J4 on 2nd Dev. Board.
- ◆ JTAG - 1st version is traced to system reset. 2nd one adds one switch (J4) for shorting to system reset.

■ USB 0

- ◆ Recognize device and host by software driver.
- ◆ Power is controlled by software.

Phenomenon II

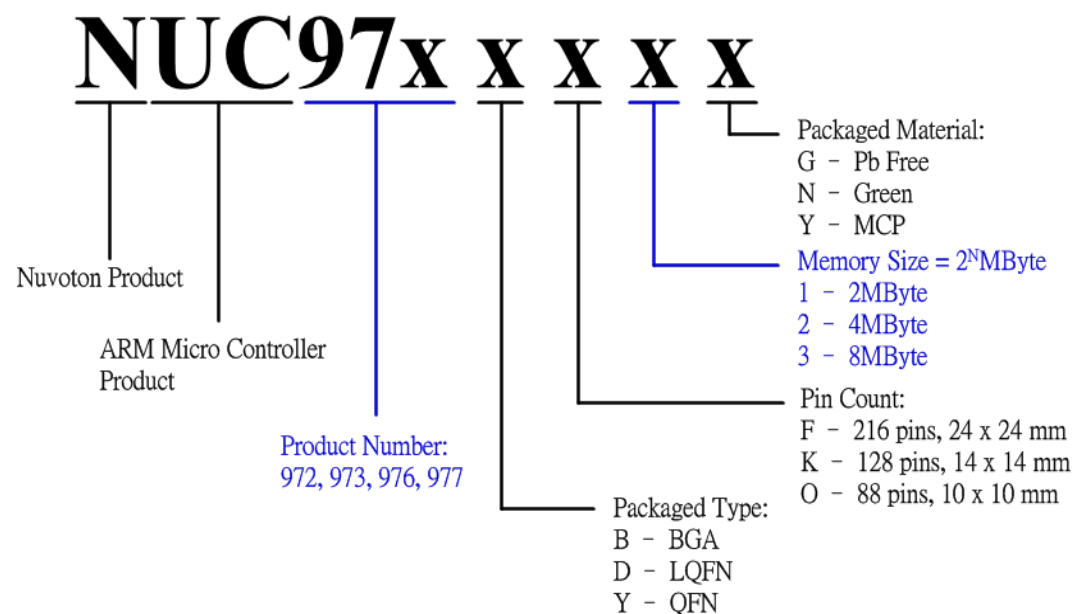
- ICE Link
 - 1st to Turbo writer connection, link to ICE
 - Install WinUSB4NuCom
- IIC
 - Use PG[3:2], PH[3:2]
- ADC
 - Vref – tied with band gap.
 - ADC0
 - ◆ Battery detection
 - ◆ Leakage current → 0.5mA.
 - ◆ Add one switch circuit for detection.



Packaged Item & Naming Rule

● Packaged Item:

- NUC972DF62Y
- NUC973DF62Y
- NUC976DK51Y
- NUC976DK52Y
- NUC976DK62Y
- NUC977DK62Y



FAQ

- Pin Header
 - VD33 is at the first 2-pin, VS is at the last 2-pin.
- UART0
 - No message
 - SW31.1 must be turned on.
- NAND fail
 - Bus is shared with eMMC.
 - Turn off SW11.
- SIM card fail
 - Is shared with IIS.
 - Turn off SW15.

RTC Power Control

- RTC's register setting

- PCLR_TIME –

- ◆ the period of the power core will be cleared after the power key is pressed. Its time scalar is 1S and the default is 5 second.
 - ◆ $\text{Key_Pressed_Period_To_Power_Off} = (\text{PCLR_TIME} + 3) \text{ sec.}$

- EDGE_TRIG –

- ◆ 1 = Edge trigger
 - ◆ 0 = Level trigger (\geq programming time).

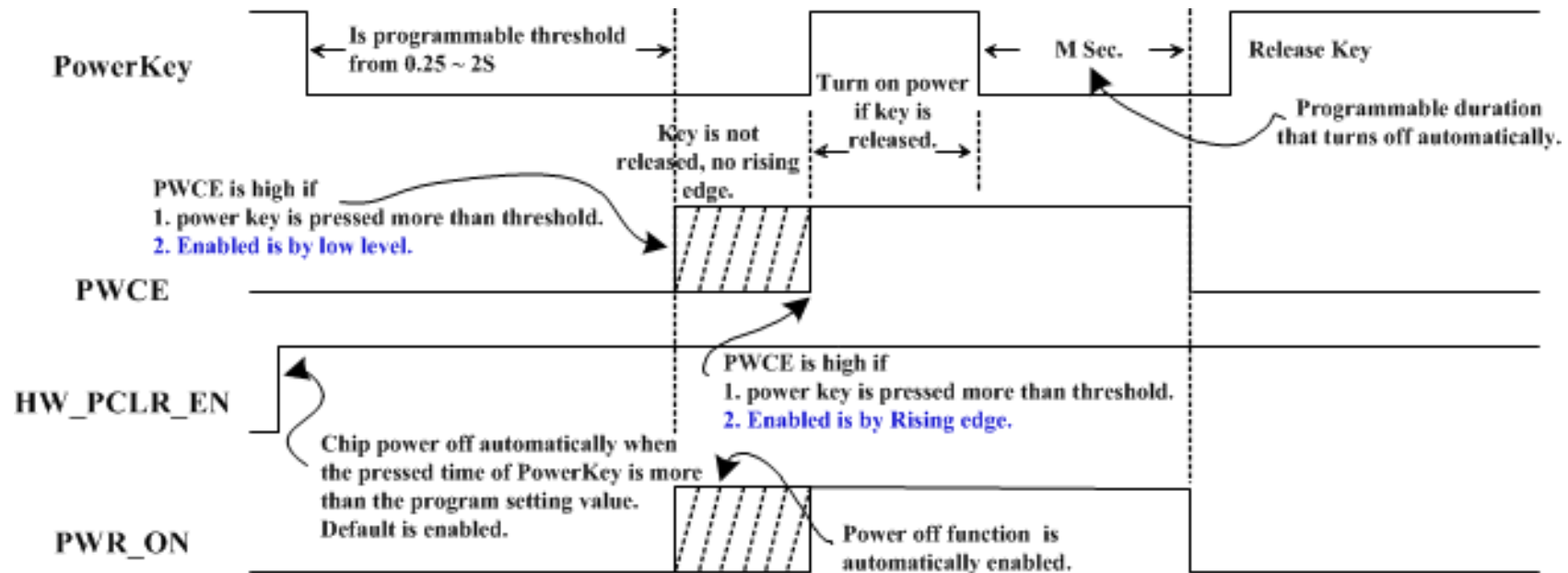
- HW_PCLR_EN

- ◆ = 1, the RPWR pin will clear to low when the power key is pressed over the PCLR_TIME second.
 - ◆ = 0, the RPWR pin isn't influenced by the pressed time of power key.

- PWR_ON

- ◆ $\text{PWRCE} = 1$ when $\text{PWR_ON} = 1$.
 - ◆ $\text{PWRCE} = 0$ when $\text{PWR_ON} = 0$, $\text{HW_PCLR_EN} = 1$ and PowerKey is pressed over setting time.

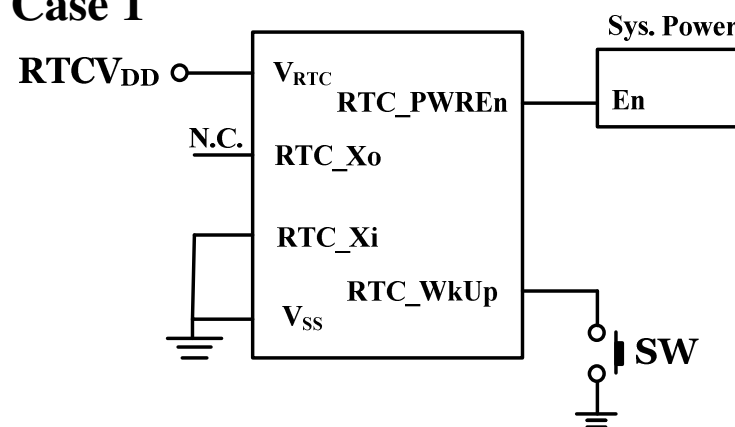
RTC Control Waveform



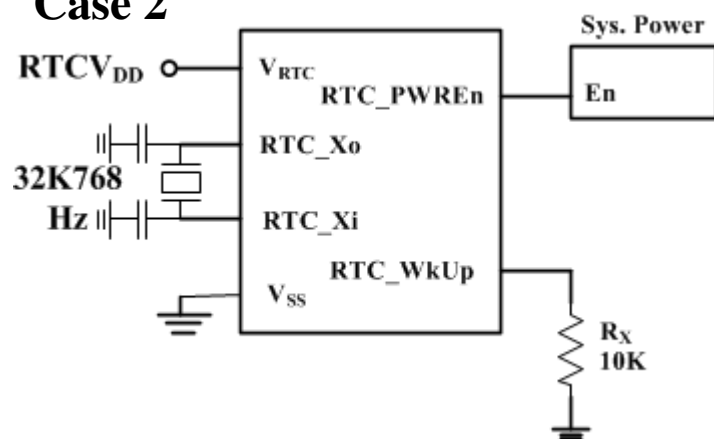
RTC Checking List

Part No.	Ext. RTC OSC.	Int. RC for RTC	V _{RTC}
N3290x	√	×	1.8V
N3291x	√	√	3.3V
N3292x	√	√	3.3V
NUC97x	√	×	3.3V

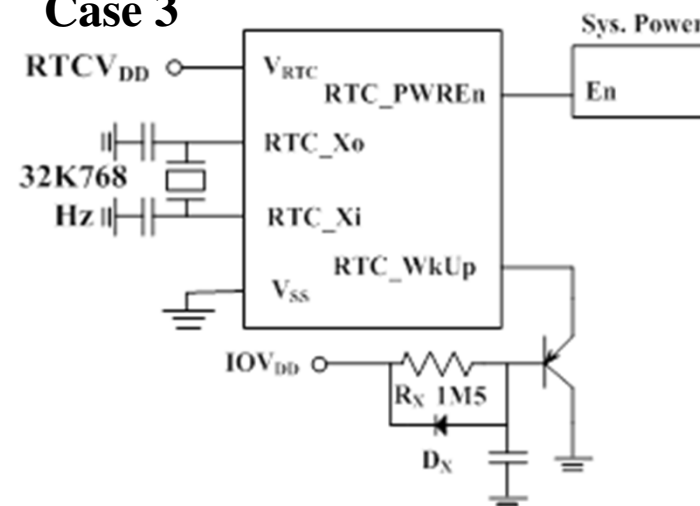
Case 1



Case 2



Case 3



Layout Guideline in Ethernet Phy

- The trace impedance (Tx+/Tx-, Rx+/Rx-) should be 100Ω, as short as possible between phy and transformer.
- The signal traces (red line) of Tx/Rx should be symmetry.
- The trace of Tx/Rx (red line) is not longer than 12 cm.
- Surround with ground
 - Tx+/Tx-, Rx+/Rx- Iset, Crystal
 - If necessary the trace routing is under transformer, $D2 \geq 60\text{mil}$.
- The distance is 30mil bet
- $D1 \geq 60\text{mil}$, $D2 \geq 80\text{mil}$

