N3292xUxDN
N3292xO1DN
N3292xO2DN

Data Sheet

ARM9-S Based Media Processor with

H.264 Codec and MCP

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1. GENERAL DESCRIPTION

The N3292x includes H.264 codec, MJPEG codec, AAC accelerator and the sound processor and is specially designed for accelerating video/audio streaming performance in the cloud multimedia stream application. H.264 codec and MJPEG codec have a very broad application range that covers all forms of recording, compression and distribution of video content. AAC accelerator can dramatically reduce the amount of data needed to represent high-quality digital audio and the sound processor can improve sound quality; both of them are mainly used for corresponding audio stream. The embedded video codec engines and audio compression/decompression accelerator enhance the application performance to save power consumption while off-loading the CPU.

The N3292x is built on the ARM926EJ-S CPU core and is integrated with video codec (H.264), Ethernet MAC, JPEG codec, CMOS sensor interface, 32-channel SPU (Sound Processing Unit), ADC, DAC and TV encoder for saving the BOM cost in various kinds of application needs. The combination of ARM926 @ 240MHz, DDR2, H.264 codec, AAC accelerator, SDIO host controller and USB2.0 HS Host/Device makes the N3292x be the best choice for video/audio streaming devices.

The N3292x could also be ported under Linux OS to leverage the driver availability of emerging functionalities such as Wi-Fi, browser, etc. On the other hand, the open source code environment provides the product development more flexibility and Nuvoton's continuous optimizations in Linux provide customers with a cost-effective video/audio streaming solution. Moreover, the 3rd parties USB and SDIO Wi-Fi modules are introduced to best utilize Wi-Fi streaming application devices such as smartphones, tablets, notebooks, smart TV, etc.

Maximum resolutions for N3292x are D1 (720x480) @ TV output and 1024x768 @ TFT LCD panel. With the increasing popularity of video streaming resolutions, H.264 is the best fit for limited bandwidth application that requires smaller data rate for high-resolution video. The N3292x is well designed in terms of cost/performance for the video/audio streaming market where Wi-Fi, Ethernet or proprietary RF is extensively used. For 2.4GHz proprietary applications, the hardware CRC generator and checking engines will off-load CPU loading to save the power consumption. Moreover, the hardware channel coding engines including scrambler, inter-leaver, Reed-Solomon outer codec and convolutional inner codec engines are used for more reliable wireless video/audio data streaming in the crowd 2.4GHz ISM band environment.

To reduce system complexity while cutting the BOM cost, the N3292x also provides versatile options of MCP (Multi-Chip Package). The 32Mbx16 or 16Mbx16 DDR2 is stacked inside the MCP to ensure higher performance and to minimize the system design efforts, such as EMI, noise coupling. Total BOM cost could be cut by employing 2-layer PCB along with the elimination of damping resistors, EMI prevention components and less board space.

1.1 Applications

- IP Camera
- Smartphone/Tablet Accessories
- Video Baby Monitor
- HMI
- Home Appliance
- Advertisement

2. FEATURES

- **CPU**
  - ARM926EJ-S 32-bit RISC CPU with 8KB I-Cache & 8KB D-Cache
  - Frequency up to 240MHz@1.2V for typical operation condition
  - JTAG interface supported for development and debugging

- **Internal SRAM & ROM**
  - 16KB IBR internal booting ROM supported
  - IBR booting messages displayed by UART console for debugging supported
  - Different system booting modes supported:
    - Memory Card
      - SD card
      - SD-to-NAND flash bridge
    - NAND Interface
      - Raw NAND Flash
      - OTP ROM (N23512T / N231GT, MXIC ExtraROM)
    - SPI Flash
    - USB Mass Storage

- **DRAM MCP**
  - 4Mbx16 DDR MCP for N32923UxDN
  - 16Mbx16 DDR2 MCP for N32925UxDN
  - 32Mbx16 DDR2 MCP for N32926UxDN/ N32926OxDN

- **EDMA (Enhanced DMA)**
  - Totally 11 DMA channels supported
    - 8 peripheral DMA channels for transfer between memory and on-chip peripherals, such as ADC, UART and SPI
    - 3 dedicated channels for memory-to-memory transfer
  - Byte, half-word and word data width types supported
  - Single and burst transfer modes supported
  - Block transfer supported in memory-to-memory transfer channel
  - Color format transformation supported in memory-to-memory transfer channel
    - Source color format could be RGB555, RGB565 and YCbCr422
    - Destination color format could be RGB555, RGB565 and YCbCr422
  - Auto reload supported for continuous data transfer
  - Interrupt generation supported in the half-of-transfer or end-of-transfer

- **Capture (CMOS Image Sensor I/F)**
  - CCIR601 & CCIR656 interfaces supported for connection to CMOS image sensor
  - Resolution up to 3M pixels
  - YUV422 and RGB565 color format supported for data-in from CMOS sensor
  - YUV422, RGB565, RGB555 and Y-only color format supported for data storing to system memory
  - Planar and packet data formats supported for data storing to system memory
  - Image cropping supported with the cropping window up to 4096x2048
  - Image scaling-down supported
    - Vertical and horizontal scaling-down for preview mode supported
      - The scaling factor is N/M
      - Two pairs of configurable 16-bit N and 16-bit M for vertical and horizontal scaling-down
      - The value of N has to equal to or less than M
    - Frame rate control supported
  - Combines two interlace fields to a single frame supported for data in from TV-decoder

- Supports 1280x1024@15fps CIS (PCLK up to 48MHz)
- Supports 1280x720@30fps CIS (PCLK up to 67.5MHz)
- Supports 640x480@60fps CIS (PCLK up to 48MHz)

- **JPEG Codec**
  - Baseline sequential mode JPEG codec function compliant with ISO/IEC 10918-1 international JPEG standard supported.
  - Planar Format
  - Support to encode interleaved YCbCr 4:2:2/4:2:0 and gray-level (Y only) format image
  - Support to decode interleaved YCbCr 4:4:4/4:2:2/4:2:0/4:1:1 and gray-level (Y only) format image
  - Support to decode YCbCr 4:2:2 transpose format
  - Support arbitrary width and height image encode and decode
  - Support three programmable quantization-tables
  - Support standard default Huffman-table and programmable Huffman-table for decode
  - Support arbitrarily 1X~8X image up-scaling function for encode mode
  - Support down-scaling function for encode and decode modes
  - Support specified window decode mode
  - Support quantization-table adjustment for bit-rate and quality control in encode mode
  - Support rotate function in encode mode
  - Packet Format
  - Support to encode interleaved YUYV format input image, output bitstream 4:2:2 and 4:2:0 format
  - Support to decode interleaved YCbCr 4:4:4/4:2:2/4:2:0 format image
  - Support decoded output image RGB555, RGB565 and RGB888 formats.
  - The encoded JPEG bit-stream format is fully compatible with JFIF and EXIF standards
  - Support arbitrary width and height image encode and decode
  - Support three programmable quantization-tables
  - Support standard default Huffman-table and programmable Huffman-table for decode
  - Support arbitrarily 1X~8X image up-scaling function for encode mode
  - Support down-scaling function 1X~ 16X for Y422 and Y420, 1X~ 8X for Y444 for decode mode
  - Support specified window decode mode
  - Support quantization-table adjustment for bit-rate and quality control in encode mode

- **AES (Advance Encryption Standard) Engine**
  - Support both encryption and decryption.
  - Support only CBC (Cipher Block Chaining) mode.
  - All three kinds of key length: 128, 192, 256 bits are supported.
  - Built-in DMA supported.

- **H.264 Codec**
  - Supports ITU-T Recommendation H.264|ISO/IEC 14496-10 Advance Video Coding(AVC) Standard (MPEG-4 part 10) baseline profile Level 3.1 standard
  - Supports up to the 720p @25fps video resolution
  - Supports YUV 4:2:0 video input format (MB base)
  - Hardware block-base rate-control (CBR/VBR)
  - Pure hardware engine

- **Video Data Processor(VPE)**
  - Video Data Processor
    - Image/Video data format conversion
      - Source

- Planar: YUV/YCbCr 444/422/420
- Packet: YUV 422

- Destination
  - Packet: YUV 422, RGB 555/565/888

- Image/video 2-D rotation and coordinate transforming
  - Left/Right with 90/180 degrees, mirror, up-side-down, and flip/flop.
- Arbitrary scaling up/down with the bilinear filter
- Supports MMU DMA

FEC (Forward Error Correction) Engine

- Reed-Solomon Encoder/Decoder
- Inter-leaver
- Scrambler
- Convolutional Encoder
- Viterbi Decoder

CRC Generator/Checking Hardware Engine

- CRC16: x^16+x^15+x^2+1 or x^16+x^15+x^5+1 (CRC-CCITT)
- CRC32: x^32+x^26+x^23+x^22+x^16+x^12+x^11+x^10+x^8+x^7+x^5+x^4+x^2+x+1

VPOST

- 8/16/18/24-bit SYNC type and 8/9/16/18/24-bit MPU type TFT LCD supported
- Color format supported:
  - YCbCr422, RGB565, RGB555, and RGB888 color formats supported for data in
  - YCbCr422, RGB565, RGB555, and RGB888 color formats supported for data out
- SVGA (800x600), WVGA (800x480), D1 (720X480), VGA (640x480), WQVGA (480x272), QVGA (320x240) and HVGA (640x240) resolution supported
  - The maximum resolution is up to D1 (720X480) for TV output
  - The maximum resolution is up to 1024x768 for TFT LCD panel
- Display scaling to fit different size of LCD panels
  - Horizontal: At most 4.0x scale
  - Vertical: At most 3.0x scale
- For SYNC type LCD:
  - For 8-bit bus
    - CCIR601 YCbCr422 packet mode (NTSC/PAL) supported
    - CCIR601 RGB Dummy mode (NTSC/PAL) supported
    - CCIR656 interface supported
    - RGB Through mode supported
  - For 16/18/24-bit bus
    - Parallel pixel data output mode (1-pixel/1-clock)
- NTSC/PAL interlace & non-interlace output supported
- Color format transform supported:
  - Color format transform between YCbCr422 and RGB565
  - Color format transform from YCbCr422 to RGB888
- TV encoder supported
- Dual screen, outputs to TV and LCD simultaneously with same content, supported
  - LCD panel should be 320X240 MPU-type, or 8-bit SYNC-type LCD panel with TV timing
- Support OSD functions to overlap system information like battery life, brightness tuning, volume tuning or muting, etc.

SPU (Sound Processing Unit)

- 7-bit volume control supported for each of 32 channels
- 5-bit pan control supported for each L/R of 32 channels
- 10-band equalizer supported
- Special code supported for loop playing and event detection

- **AAC accelerator**
  - MDCT/IMDCT engine
- **I2S Controller**
  - I2S interface supported to connect external audio codec
  - 16/18/20/24-bit data format supported
- **Storage Interface Controller**
  - Interface to NAND Flash:
    - 8-bit data bus width supported
    - SLC and MLC type NAND Flash supported
    - 512B, 2KB, 4KB, and 8KB page size NAND Flash supported
    - ECC24 algorithm supported for ECC generation, error detection and error correction
    - PBA-NAND flash supported
  - Interface to SD/MMC/SDIO/SDHC/micro-SD cards supported
    - SD-to-NAND flash bridge supported
  - DMA function supported to accelerate the data transfer between system memory and NAND Flash or SD/MMC/SDIO/SDHC/micro-SD
- **USB Device Controller**
  - USB2.0 HS (High-Speed) x 1 port
  - 6 configurable endpoints supported
  - Control, Bulk, Interrupt and Isochronous transfers supported
  - Suspend and remote wakeup supported
- **USB Host Controllers**
  - One USB 1.1 Host port
  - One USB 2.0 Host port
  - Over Current detection required
  - Fully compliant with USB Revision 1.1 and 2.0 specifications
  - Open Host Controller Interface (OHCI) Revision 1.0 compatible
  - High-speed (480Mbps), Full-speed (12Mbps) and low-speed (1.5Mbps) USB devices supported
  - Control, Bulk, Interrupt and Isochronous transfers supported
- **Timer & Watch-Dog Timer**
  - Four 32-bit with 8-bit pre-scalar timers supported
  - One programmable 24-bit Watch-Dog Timer supported
- **PWM**
  - 4 PWM channel outputs supported
  - 16-bit counter supported for each PWM channel
  - Two 8-bit pre-scalars supported and each pre-scalar shared by two PWM channels
  - Two clock-dividers supported and each divider shared by two PWM channels
  - Two Dead-Zone generators supported and each generator shared by two PWM channels
  - Auto reloaded mode and one-shot pulse mode supported
  - Capture function supported
- **UART**
  - A high speed UART supported:
    - Baud rate is up to 1M bps
    - 4 signals TX, RX, CTS and RTS supported
  - A normal UART supported:
    - Baud rate is up to 115.2K bps
    - 2 signals TX and RX supported only

- **SPI**
  - Two SPI interfaces are supported
    - Both master and slave mode are supported in SPI interface 0
    - Only master mode is supported in SPI interface 1
      - Byte transfer with configurable stop interval supported
  - Supports 1/2/4 bit SPI NOR Flash interface timing specification

- **I2C**
  - One I2C channel supported
  - Compatible with Philips's I^2C standard and only master mode supported
  - Multi-master operation supported

- **Advanced Interrupt Controller**
  - Total 32 interrupt source supported
  - Configurable interrupt type:
    - Low-active level triggered interrupt
    - High-active level triggered interrupt
    - Low-active edge (falling edge) triggered interrupt
    - High-active edge (rising edge) triggered interrupt
  - Individual interrupt mask bit for each interrupt source
  - 8 different priority levels supported
  - Low priority interrupt automatic masking supported for interrupt nesting

- **Internal SRAM**
  - 8KB embedded SRAM
  - Co-work with Fast Booting (<3 seconds) for reducing system power consumption.

- **RTC**
  - Independent power plane supported
  - 32.768 KHz crystal oscillation circuit supported
  - Build-in 32KHz RC oscillator
  - Time counter (second, minute, hour) and Calendar counter (day, month, year) supported
  - Alarm supported (second, minute, hour, day, month and year)
  - 12/24-hour mode and Leap year supported
  - Alarm to wake chip up from Standby mode or from Power-down mode supported
  - Wake chip up from Power-down mode by input pin supported
  - Power-off chip by register setting supported
  - Power-on timeout is supported for low battery protection

- **GPIO**
  - 80 programmable general purpose I/Os supported and separated into 5 groups
  - Individual configuration supported for each I/O signal
  - Configurable interrupt control functions supported
  - Configurable de-bounce circuit supported for interrupt function

- **Audio DAC**
  - 16-bit stereo DAC supported with headphone driver output
  - H/W volume control supported

- **Audio ADC**
  - 16-bit Sigma-Delta ADC supported

- **General-Purpose ADC (SAR ADC)**
  - Multi-channel, 12-bit ADC supported

- 4 channels dedicated for 4-wire resistive touch sensor inputs
- 3 channels reserved for various purposes, like LVD (Low Voltage Detection), keypad input, and light sensor
- 5-wire resistive touch sensor interface is also supported
- Input voltage range from 0V ~ 3.3V supported

- Maximum 16MHz input clock supported
- Maximum 200K/s conversion rate supported
- One high-speed channel for 1M SPS sampling rate
- LVR (Low Voltage Reset) supported

Power Management

- Advanced power management including Power Down, Deep Standby, CPU Standby, and Normal Operating modes
  - Normal Operating Mode
    - Core power is 1.2V and chip is in normal operation
  - CPU Standby Mode
    - Core power is 1.2V and only ARM CPU clock is turned OFF
  - Deep Standby Mode
    - Core power is 1.2V and all IP clocks are turned OFF
  - Power Down Mode
    - Only the RTC power is ON. Other 3.3V and 1.2V power are OFF

Operating Voltage

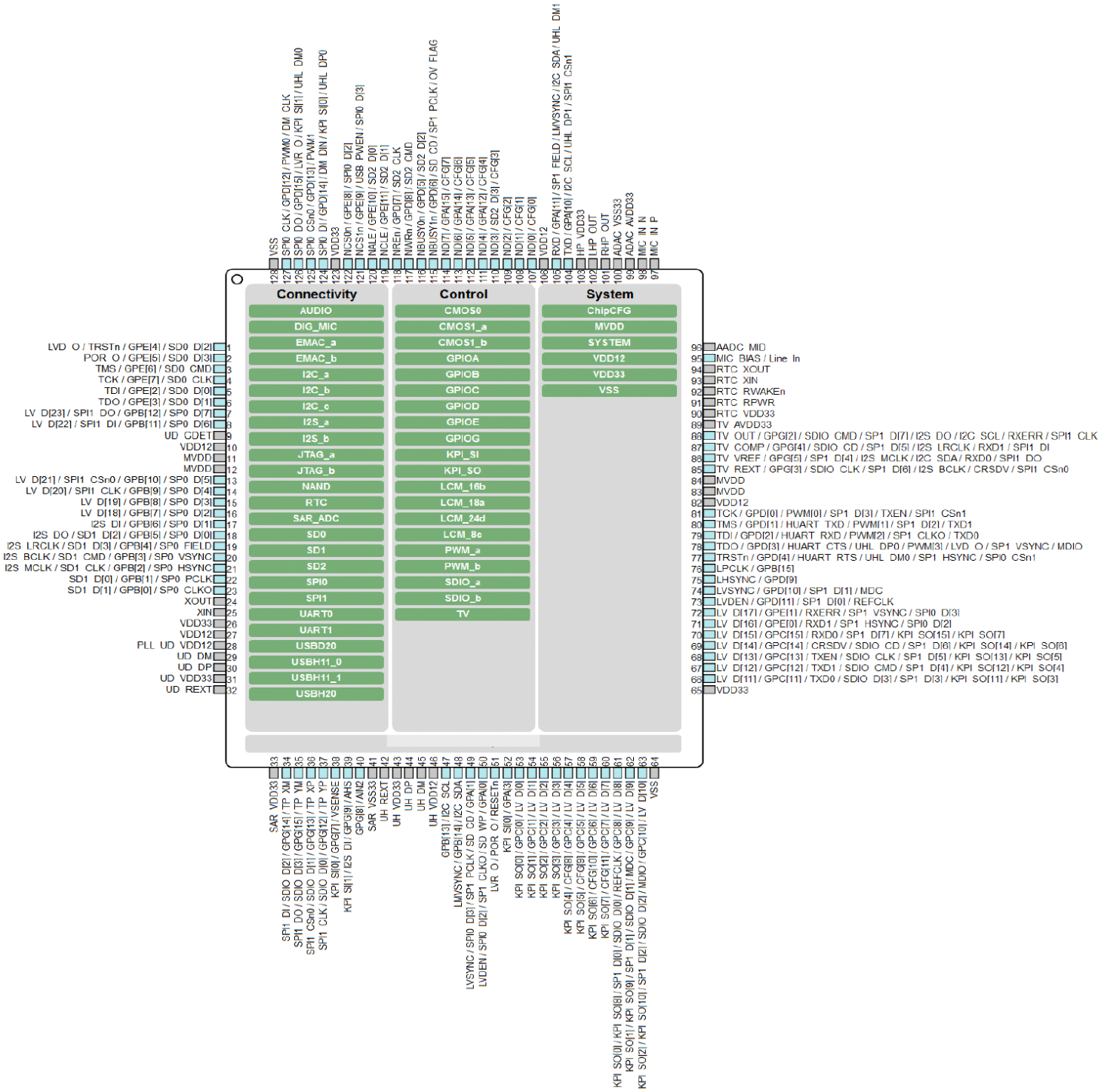
- I/O: 3.3V
- Core: 1.2V
- DDR2: 1.9V

Package

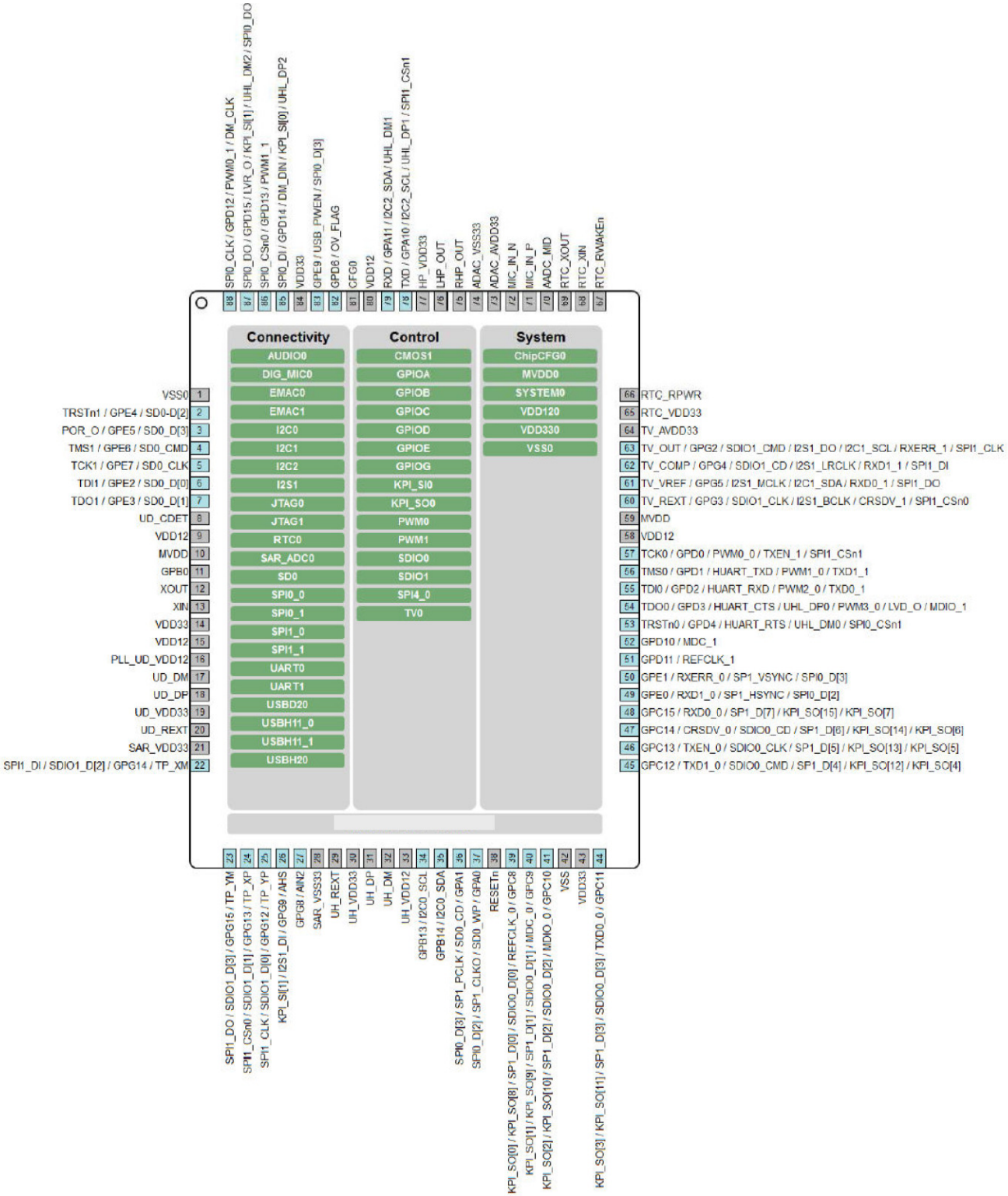
- LQFP-128
- QFN-88

3. PIN DIAGRAM

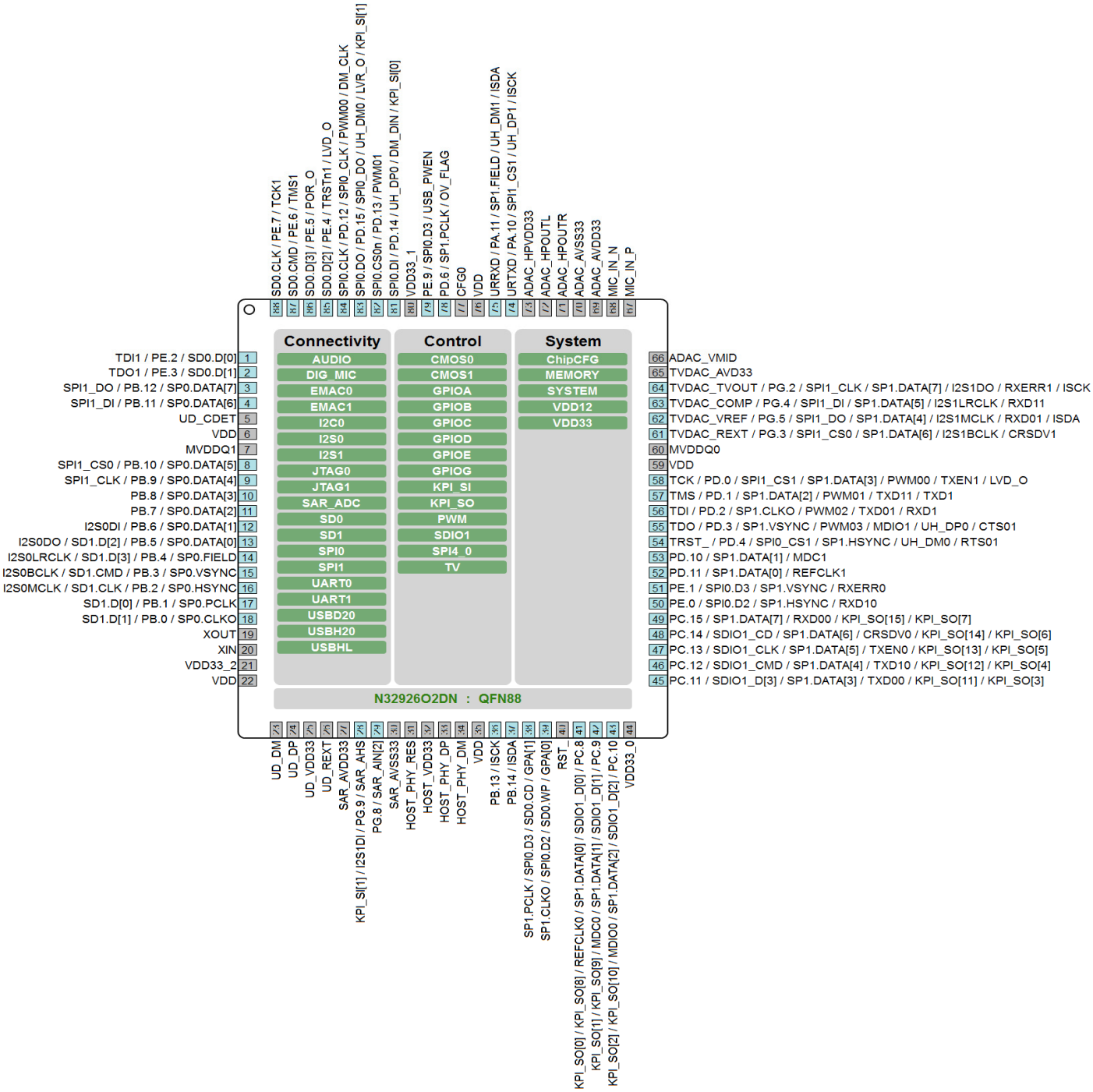
3.1 N3292xUxDN



3.2 N3292xO1DN



3.3 N3292xO2DN



4. PIN DESCRIPTION

4.1 Pin Description

Name	I/O Type	Brief	N329x Pin No.		
			UxDN	O1DN	O2DN
			LQFP128	QFN88	QFN88
XIN	I	12MHz Crystal Input	25	13	20
XOUT	O	12MHz Crystal Output	24	12	19
RST_	ISU	System Reset, Input, Low Active	51	38	40
TCK	IOD	JTAG Interface Test Clock, Input	81	57	58
SPI1_CS1_		SPI Port 1 Device Select 1, Output, Low Active			
PWM0		PWM Channel 0			
S2DATA[3]		Sensor Interface Device 2 Pixel Data 3			
TXEN		LAN RMII Interface TXEN			
GPD[0]		GPIO Port D Bit 0			
TMS	IOU	JTAG Interface Test Mode Select, Input	80	56	57
HUR_TXD		High-Speed UART TX Data, Output			
PWM1		PWM Channel 1			
S2DATA[2]		Sensor Interface Device 2 Pixel Data 2			
TXD1		LAN RMII Interface TXD1			
GPD[1]		GPIO Port D Bit 1			
TDI	IOU	JTAG Interface Test Data In, Input	79	55	56
HUR_RXD		High-Speed UART RX Data, Input			
PWM2		PWM Channel 2			
S2CLKO		Sensor Interface Device 2 System Clock, Output			
TXD0		LAN RMII Interface TXD0			
GPD[2]		GPIO Port D Bit 2			
TDO	IOU	JTAG Interface Test Data Out, Output	78	54	55
HUR_CTS		High-Speed UART Clear-To-Send, Input, Low Active			

PWM3		PWM Channel 3			
S2VSYNC		Sensor Interface Device 2 Vertical Sync, Input			
UHL_DP0		USB Host Like Port 0, D+			
LVD_O		Low Voltage Detected, Output, Low Active			
MDIO		LAN RMII Interface MDIO			
GPD[3]		GPIO Port D Bit 3			
TRST_	IOU	JTAG Interface Test Reset, Input, Low Active	77	53	54
HUR_RTS		High-Speed UART Reset-To-Send, Output, Low Active			
SPI0_CS1_		SPI Port 0 Device Select 1, Output, Low Active			
S2HSYNC		Sensor Interface Device 2 Horizontal Sync, Input			
UHL_DM0		USB Host Like Port 0, D-			
GPD[4]		GPIO Port D Bit 4			
NCS0_	IOU	NAND Interface Chip Select 0, Output, Low Active	122	--	--
SPI0_D2		SPI Interface Port 0 Data 2 Inout			
GPE[8]		GPIO Port E Bit 8			
NCS1_	IOU	NAND Interface Chip Select 1, Output, Low Active	121	83	79
SPI0_D3		SPI Interface Port 0 Data 3 Inout			
USB_PWEN		USB High Side Power Switch for Over Current			
GPE[9]		GPIO Port E Bit 9			
NALE	IOU	NAND Interface Address-Latch-Enable, Output, High Active	120	--	--
SDDATA2[0]		SD Interface Port 2 Data Bit 0			
GPE[10]		GPIO Port E Bit 10			
NCLE	IOU	NAND Interface Command-Latch-Enable, Output, High Active	119	--	--
SDDATA2[1]		SD Interface Port 2 Data Bit 1			
GPE[11]		GPIO Port E Bit 11			
NBUSY0_	IOU	NAND Interface Busy 0, Input, Low Active	116	--	--
SDDAT2[2]		SD Interface Port 2 Data Bit 2			
GPD[5]		GPIO Port D Bit 5			
NBUSY1_	IOU	NAND Interface Busy 1, Input, Low Active	115	82	78
SD_CD		SD Interface Card Detect			

S2PCLK		Sensor Interface Device 2 Pixel Clock, Input			
OV_FLAG		USB High Side Over Current Flag			
GPD[6]		GPIO Port D Bit 6			
NRE_	IOU	NAND Interface Read Enable, Output, Low Active	118	--	--
SDCLK2		SD Interface Port 2 Clock, Output			
GPD[7]		GPIO Port D Bit 7			
NWR_	IOU	NAND Interface Write Enable, Output, Low Active	117	--	--
SDCMD2		SD Interface Port 2 Command/Response			
GPD[8]		GPIO Port D Bit 8			
ND[0]	IOU	NAND Interface Data Bit 0	107	81	77
CHIPCFG[0]		Chip Power-On Configuration Bit 0, Input			
ND[1]	IOU	NAND Interface Data Bit 1	108	--	--
CHIPCFG[1]		Chip Power-On Configuration Bit 1, Input			
ND[2]	IOU	NAND Interface Data Bit 2	109	--	--
CHIPCFG[2]		Chip Power-On Configuration Bit 2, Input			
ND[3]	IOU	NAND Interface Data Bit 3	110	--	--
SDDATA2[3]		SD Interface Port 2 Data Bit 3			
CHIPCFG[3]		Chip Power-On Configuration Bit 3, Input			
ND[4]	IOU	NAND Interface Data Bit 4	111	--	--
GPA[12]		GPIO Port A Bit 12			
CHIPCFG[4]		Chip Power-On Configuration Bit 4, Input			
ND[5]	IOU	NAND Interface Data Bit 5	112	--	--
GPA[13]		GPIO Port A Bit 13			
CHIPCFG[5]		Chip Power-On Configuration Bit 5, Input			
ND[6]	IOU	NAND Interface Data Bit 6	113	--	--
GPA[14]		GPIO Port A Bit 14			
CHIPCFG[6]		Chip Power-On Configuration Bit 6, Input			
ND[7]	IOU	NAND Interface Data Bit 7	114	--	--
GPA[15]		GPIO Port A Bit 15			
CHIPCFG[7]		Chip Power-On Configuration Bit 7, Input			

SCLKO	IOD	Clock to Sensor Module, Output	23	11	18
SDDAT1[1]		SD Interface Port 1 Data Bit 1			
GPB[0]		GPIO Port B Bit 0			
SPCLK	IOD	Sensor Interface Pixel Clock, Input	22	--	17
SDDAT1[0]		SD Interface Port 1 Data Bit 0			
GPB[1]		GPIO Port B Bit 1			
SHSYNC	IOD	Sensor Interface Horizontal Sync, Input	21	--	16
I2S_MCLK		Clock to I2S Codec, Output			
SDCLK1		SD Interface Port 1 Clock, Output			
GPB[2]		GPIO Port B Bit 2			
SVSYNC	IOD	Sensor Interface Vertical Sync, Input	20	--	15
I2S_BCLK		I2S Interface Clock, Input			
SDCMD1		SD Interface Port 1 Command/Response			
GPB[3]		GPIO Port B Bit 3			
SFIELD	IOD	Sensor Interface Even/ODD Field Indicator, Input	19	--	14
I2S_WS		I2S Interface Word Select, Output			
SDDAT1[3]		SD Interface Port 1 Data Bit 3			
GPB[4]		GPIO Port B Bit 4			
SPDATA[0]	IOD	Sensor Interface Data Bit 0, Input	18	--	13
I2S_DOUT		I2S Interface Data Output			
SDDAT1[2]		SD Interface Port 1 Data Bit 2			
GPB[5]		GPIO Port B Bit 5			
SPDATA[1]	IOD	Sensor Interface Data Bit 1, Input	17	--	12
I2S_DIN		I2S Interface Data Input			
GPB[6]		GPIO Port B Bit 6			
SPDATA[2]	IOD	Sensor Interface Data Bit 2, Input	16	--	11
LVDATA[18]		LCD Interface Data Bit 18			
GPB[7]		GPIO Port B Bit 7			
SPDATA[3]	IOD	Sensor Interface Data Bit 3, Input	15	--	10
LVDATA[19]		LCD Interface Data Bit 19			

GPB[8]		GPIO Port B Bit 8			
SPDATA[4]	IOD	Sensor Interface Data Bit 4, Input	14	--	9
SPI1_CLK		SPI Interface Port 1 Clock, Output (Master), Input (Slave)			
LVDATA[20]		LCD Interface Data Bit 20			
GPB[9]		GPIO Port B Bit 9			
SPDATA[5]	IOD	Sensor Interface Data Bit 5, Input	13	--	8
SPI1_CS0_		SPI Interface Port 1 Device Select 0, Low Active, Output (Master), Input (Slave)			
LVDATA[21]		LCD Interface Data Bit 21			
GPB[10]		GPIO Port B Bit 10			
SPDATA[6]	IOD	Sensor Interface Data Bit 6, Input	8	--	4
SPI1_DI		SPI Interface Port 1 Data Input			
LVDATA[22]		LCD Interface Data Bit 22			
GPB[11]		GPIO Port B Bit 11			
SPDATA[7]	IOD	Sensor Interface Data Bit 7, Input	7	--	3
SPI1_DO		SPI Interface Port 1 Data Output			
LVDATA[23]		LCD Interface Data Bit 23			
GPB[12]		GPIO Port B Bit 12			
ISCK	IOU	I2C Interface Clock, Output	47	34	36
GPB[13]		GPIO Port B Bit 13			
ISDA	IOU	I2C Interface Data	48	35	37
LMVSYNC		LCD MPU Mode Vertical Sync, Output			
GPB[14]		GPIO Port B Bit 14			
LPCLK	IOU	LCD Interface Pixel Clock, Output	76	--	--
GPB[15]		GPIO Port B Bit 15			
LHSYNC	IOU	LCD Interface Horizontal Sync, Output, High Active	75	--	--
GPD[9]		GPIO Port D Bit 9			
LVSYNC	IOU	LCD Interface Vertical Sync, Output, High Active	74	52	53
S2DATA[1]		Sensor Interface Device 2 Pixel Data 1			
MDC		LAN RMII Interface MDC			
GPD[10]		GPIO Port D Bit 10			

LVDEN	IOU	LCD Interface Data Enable, Output, High Active	73	51	52
S2DATA[0]		Sensor Interface Device 2 Pixel Data 0			
REFCLK		LAN RMII Interface REFCLK			
GPD[11]		GPIO Port D Bit 11			
LVDATA[0]	IOU	LCD Interface Data Bit 0	53	--	--
KPI_SO[0]		KPI Scan Out Data Bit 0			
GPC[0]		GPIO Port C Bit 0			
LVDATA[1]	IOU	LCD Interface Data Bit 1	54	--	--
KPI_SO[1]		KPI Scan Out Data Bit 1			
GPC[1]		GPIO Port C Bit 1			
LVDATA[2]	IOU	LCD Interface Data Bit 2	55	--	--
KPI_SO[2]		KPI Scan Out Data Bit 2			
GPC[2]		GPIO Port C Bit 2			
LVDATA[3]	IOU	LCD Interface Data Bit 3	56	--	--
KPI_SO[3]		KPI Scan Out Data Bit 3			
GPC[3]		GPIO Port C Bit 3			
LVDATA[4]	IOU	LCD Interface Data Bit 4	57	--	--
KPI_SO[4]		KPI Scan Out Data Bit 4			
GPC[4]		GPIO Port C Bit 4			
CHIPCFG[8]		Chip Power-On Configuration Bit [8], Input			
LVDATA[5]	IOU	LCD Interface Data Bit 5	58	--	--
KPI_SO[5]		KPI Scan Out Data Bit 5			
GPC[5]		GPIO Port C Bit 5			
CHIPCFG[9]		Chip Power-On Configuration Bit [9], Input			
LVDATA[6]	IOU	LCD Interface Data Bit 6	59	--	--
KPI_SO[6]		KPI Scan Out Data Bit 6			
GPC[6]		GPIO Port C Bit 6			
CHIPCFG[10]		Chip Power-On Configuration Bit [10], Input			
LVDATA[7]	IOU	LCD Interface Data Bit 7	60	--	--
KPI_SO[7]		KPI Scan Out Data Bit 7			

GPC[7]		GPIO Port C Bit 7			
CHIPCFG[11]		Chip Power-On Configuration Bit [11], Input			
LVDATA[8]	IOU	LCD Interface Data Bit 8	61	39	41
KPI_SO[8/0]		KPI Scan Out Data Bit 8 or Bit 0			
S2PDATA[0]		Sensor Interface Device 2 Data Bit 0, Input			
SDIO_D0		SDIO Interface Data 0			
REFCLK		LAN RMII Interface REFCLK			
GPC[8]		GPIO Port C Bit 8			
LVDATA[9]	IOU	LCD Interface Data Bit 9	62	40	42
KPI_SO[9/1]		KPI Scan Out Data Bit 9 or Bit 1			
S2PDATA[1]		Sensor Interface Device 2 Data Bit 1, Input			
SDIO_D1		SDIO Interface Data 1			
MDC		LAN RMII Interface MDC			
GPC[9]		GPIO Port C Bit 9			
LVDATA[10]	IOU	LCD Interface Data Bit 10	63	41	43
KPI_SO[10/2]		KPI Scan Out Data Bit 10 or Bit 2			
S2PDATA[2]		Sensor Interface Device 2 Data Bit 2, Input			
SDIO_D2		SDIO Interface Data 2			
MDIO		LAN RMII Interface MDIO			
GPC[10]		GPIO Port C Bit 10			
LVDATA[11]	IOU	LCD Interface Data Bit 11	66	44	45
KPI_SO[11/3]		KPI Scan Out Data Bit 11 or Bit 3			
S2PDATA[3]		Sensor Interface Device 2 Data Bit 3, Input			
SDIO_D3		SDIO Interface Data 3			
TXD0		LAN RMII Interface TXD0			
GPC[11]		GPIO Port C Bit 11			
LVDATA[12]	IOU	LCD Interface Data Bit 12	67	45	46
KPI_SO[12/4]		KPI Scan Out Data Bit 12 or Bit 4			
S2PDATA[4]		Sensor Interface Device 2 Data Bit 4, Input			
SDIO_CMD		SDIO Interface CMD			

TXD1		LAN RMII Interface TXD1			
GPC[12]		GPIO Port C Bit 12			
LVDATA[13]	IOU	LCD Interface Data Bit 13	68	46	47
KPI_SO[13/5]		KPI Scan Out Data Bit 13 or Bit 5			
S2PDATA[5]		Sensor Interface Device 2 Data Bit 5, Input			
SDIO_CLK		SDIO Interface CLK			
TXEN		LAN RMII Interface TXEN			
GPC[13]		GPIO Port C Bit 13			
LVDATA[14]	IOU	LCD Interface Data Bit 14	69	47	48
KPI_SO[14/6]		KPI Scan Out Data Bit 14 or Bit 6			
S2PDATA[6]		Sensor Interface Device 2 Data Bit 6, Input			
SDIO_CD		SDIO Interface Card Detect			
CRSDV		LAN RMII Interface CRSDV			
GPC[14]		GPIO Port C Bit 14			
LVDATA[15]	IOU	LCD Interface Data Bit 15	70	48	49
KPI_SO[15/7]		KPI Scan Out Data Bit 15 or Bit 7			
S2PDATA[7]		Sensor Interface Device 2 Data Bit 7, Input			
RXD0		LAN RMII Interface RXD0			
GPC[15]		GPIO Port C Bit 15			
LVDATA[16]	IOU	LCD Interface Data Bit 16	71	49	50
S2HSYNC		Sensor Interface Device 2 Horizontal Sync, Input			
SPI0_D2		SPI Interface Port 0 Data 2 Inout			
RXD1		LAN RMII Interface RXD1			
GPE[0]		GPIO Port E Bit 0			
LVDATA[17]	IOU	LCD Interface Data Bit 17	72	50	51
S2VSYNC		Sensor Interface device 2 Vertical Sync, Input			
SPI0_D3		SPI Interface Port 0 Data 3 Inout			
RXERR		LAN RMII RXERR			
GPE[1]		GPIO Port E Bit 1			
URTXD	IOU	UART TX Data, Output	104	78	74

UHL_DP1		USB Host Like Port 1, D+			
ISCK		I2C Interface Clock			
SPI1_CS1_		SPI Port 1 Device Select 1, Output, Low Active			
GPA[10]		GPIO Port A Bit 10			
URRXD	IOU	UART RX Data, Input	105	79	75
UHL_DM1		USB Host Like Port 1, D-			
ISDA		I2C Interface Data			
LMVSYNC		LCD MPU Mode Vertical Sync, Output			
S2FIELD		Sensor Interface Device 2 Even/ODD Field Indicator, Input			
GPA[11]		GPIO Port A Bit 11			
SPI0_CLK	IOD	SPI Interface Port 0 Clock, Output (Master), Input (Slave)	127	88	84
PWM0		PWM Channel 0			
DM_CLK		Digital Microphone Interface CLK			
GPD[12]		GPIO Port D Bit 12			
SPI0_CS0_	IOU	SPI Interface Port 0 Device Select 0, Low Active, Output (Master), Input (Slave)	125	86	82
PWM1		PWM Channel 1			
GPD[13]		GPIO Port D Bit 13			
SPI0_DI	IOD	SPI Interface Port 0 Data Input	124	85	81
UHL_DP0		USB Host Like Port 0, D+			
KPI_SI[0]		KPI Scan In Data Bit 0			
DM_DIN		Digital Microphone Interface Data Input			
GPD[14]		GPIO Port D Bit 14			
SPI0_DO	IOD	SPI Interface Port 0 Data Output	126	87	83
UHL_DM0		USB Host Like Port 0, D-			
KPI_SI[1]		KPI Scan In Data Bit 1			
LVR_O		Low Voltage Reset, Output			
GPD[15]		GPIO Port D Bit 15			
SDCLK	IOD	SD Interface Port 0 Clock, Output	4	5	88
TCK		JTAG Interface Test Clock, Input			

GPE[7]		GPIO Port E Bit 7			
SDCMD	IOU	SD Interface Port 0 Command/Response	3	4	87
TMS		JTAG Interface Test Mode Select, Input			
GPE[6]		GPIO Port E Bit 6			
SDDAT[0]	IOU	SD Interface Port 0 Data Bit 0	5	6	1
TDI		JTAG Interface Test Data In, Input			
GPE[2]		GPIO Port E Bit 2			
SDDAT[1]	IOU	SD Interface Port 0 Data Bit 1	6	7	2
TDO		JTAG Interface Test Data Out, Output			
GPE[3]		GPIO Port E Bit 3			
SDDAT[2]	IOU	SD Interface Port 0 Data Bit 2	1	2	85
TRST_		JTAG Interface Test Reset, Input, Low Active			
GPE[4]		GPIO Port E Bit 4			
LVD_O		Low Voltage Detect, Output, Low Active			
SDDAT[3]	IOU	SD Interface Port 0 Data Bit 3	2	3	86
GPE[5]		GPIO Port E Bit 5			
POR_O		Power On Reset, Output, Low Active			
S2CLKO	IOU	Sensor Interface device 2 System Clock, Output	50	37	39
SPI0_D2		SPI Interface Port 0 Data 2 Inout			
LVDEN		LCD Interface Data Enable, Output, High Active			
SD_WP		SD Interface Write Protect			
GPA[0]		GPIO Port A Bit 0			
S2PCLK	IOU	Sensor Interface Device 2 Pixel Clock, Input	49	36	38
SPI0_D3		SPI Interface Port 0 Data 3 Inout			
LVSYNC		LCD Interface Vertical Sync, Output, High Active			
SD_CD_		SD Interface Card Detect, Input, Low Active			
GPA[1]		GPIO Port A Bit 1			
KPI_SI[0]	IOU	Key Matrix Scan Input Data Bit 0	52	--	--
GPA[3]		GPIO Port A Bit 3			
RTC_XIN	I	32768Hz Crystal Input	93	68	--

RTC_XOUT	O	32768Hz Crystal Output	94	69	--
RTC_RWAKE_	IU	Wakeup Enable, Input, Low Active	92	67	--
RTC_RPWR	O	Power Enable, Output, High Active	91	66	--
UD_CDET	I (Hi Z)	USB Device Connect Detect, Input, High Active	9	8	5
UD_DP	IO	USB 2.0 Device D+	30	18	24
UD_DM	IO	USB 2.0 Device D-	29	17	23
UD_REXT	I	External Resistor Connected, This pin is to connect a 12.1Kohm resistor to ground for USB 2.0 PHY	32	20	26
UH_DP	IO	USB 2.0 HOST D+	44	31	33
UH_DM	IO	USB 2.0 HOST D-	45	32	34
UH_REXT	I	External Resistor Connected, This pin is to connect a 12.1Kohm resistor to ground for USB HOST2.0 PHY	42	29	31
TVDAC_TVOUT	IO	Composite/Chroma Output	88	63	64
I2S_DOUT		I2S Interface Data Output			
ISCK		I2C Interface Clock			
SPI1_CLK		SPI Interface Port 1 Clock			
SDIO_CMD		SDIO Interface CMD			
S2DATA[7]		Sensor Interface Device 2 Data Bit 7, Input			
RXERR		LAN RMII Interface RXERR			
GPG[2]		GPIO Port G Bit 2			
TVDAC_REXT	IO	External Resistor Connection	85	60	61
I2S_BCLK		I2S Interface Clock, Input			
SPI1_CS0_		SPI Interface Port 1 Device Select 0, Output, Active Low			
SDIO_CLK		SDIO Interface CLK			
S2DATA[6]		Sensor Interface Device 2 Data Bit 6, Input			
CRSDV		LAN RMII Interface CRSDV			
GPG[3]		GPIO Port G Bit 3			
TVDAC_COMP	IO	External Capacitor Connection	87	62	63
I2S_WS		I2S Interface Word Select, Output			

SPI1_DI		SPI Interface Port 1 Data Input			
SDIO_CD		SDIO Interface Card Detect			
S2DATA[5]		Sensor Interface Device 2 Data Bit 5, Input			
RXD1		LAN RMII Interface RXD1			
GPG[4]		GPIO Port G Bit 4			
TVDAC_VREF	IO	Reference Voltage Output	86	61	62
I2S_MCLK		Clock to I2S Codec, Output			
ISDA		I2C Interface Data			
SPI1_DO		SPI Interface Port 1 Data Output			
S2DATA[4]		Sensor Interface Device 2 Data Bit 4, Input			
RXD0		LAN RMII Interface RXD0			
GPG[5]		GPIO Port G Bit 5			
ADC_VSENSE	IO	5W Touch Screen Input detection	38	--	--
ADC_AIN[3]		ADC Analog Input Channel 3			
KPI_SI[0]		Key Matrix Scan Input Data Bit 0			
GPG[7]		GPIO Port G Bit 7			
ADC_AHS (ADC_AIN[1])	IO	ADC Analog (High Speed) Input Channel 1	39	26	28
I2S_DI		I2S Interface Data Input			
KPI_SI[1]		Key Matrix Scan Input Data Bit 1			
GPG[9]		GPIO Port G Bit 9			
ADC_AIN[2]	IO	ADC Analog Input Channel 2 (HW analog scan key)	40	27	29
GPG[8]		GPIO Port G Bit 8			
MIC_IN_M	I	Microphone Negative Input	98	72	68
MIC_IN_P	I	Microphone Positive Input	97	71	67
MIC_BIAS	IO	Microphone Bias Power Supply. (MIC_BIAS=0.75 * ADAC_AVDD33)	95	--	--
Line_In		Analog Audio In			
ADC_TP_YP	IO	Touch Panel YP	37	25	--
SPI1_CLK		SPI Interface Port 1 Clock			
SDIO_D0		SDIO Interface Data 0			
GPG[12]		GPIO Port G Bit 12			

ADC_TP_XP	IO	Touch Panel XP	36	24	--
SPI1_CS0_		SPI Interface Port 1 Device Select 0, Output, Active Low			
SDIO_D1		SDIO Interface Data 1			
GPG[13]		GPIO Port G Bit 13			
ADC_TP_XM	IO	Touch Panel XM	34	22	--
SPI1_DI		SPI Interface Port 1 Data Input			
SDIO_D2		SDIO Interface Data 2			
GPG[14]		GPIO Port G Bit 14			
ADC_TP_YM	IO	Touch Panel YM	35	23	--
SPI1_DO		SPI Interface Port 1 Data Output			
SDIO_D3		SDIO Interface Data 3			
GPG[15]		GPIO Port G Bit 15			
ADAC_HPOUT_R	O	Audio Headphone Right Channel Output	101	75	71
ADAC_HPOUT_L	O	Audio Headphone Left Channel Output	102	76	72
VMID	I	DAC Mid-rail Reference Decoupling Point, Connect a 1uF to ADAC_HPVSS33.(VMID=1/2 * ADAC_AVDD33)	96	70	66
MVDD	P	SDRAM I/F Power VDD & VDDQ	11,12,83,84	10,59	7,60
RTC_VDD	P	RTC Core, I/F & 32768Hz Crystal Power (3.3V)	90	65	--
UD_VDD33	P	USB 2.0 PHY Power (3.3V)	31	19	25
UD_PLL_VDD12	P	USB 2.0 PHY & PLL Power (1.2V)	28	16	22
UH_VDD33	P	USB HOST 2.0 PHY Power (3.3V)	43	30	32
UH_VDD12	P	USB HOST 2.0 PHY Power (1.2V)	46	33	35
TVDAC_VDD33	P	TV DAC Power (3.3V)	89	64	65
ADC_VDD33	P	ADC Power (3.3V)	33	21	27
ADC_VSS33	G	ADC Ground (0V)	41	28	30
ADAC_HPVDD33	P	Audio DAC Headphone Driver Power (3.3V)	103	77	73
ADAC_HPVSS33	G	Audio DAC & Headphone Driver Ground (0V)	100	74	70
ADAC_AVDD33	P	Audio DAC Power (3.3V)	99	73	69
VDD33	P	I/O Power (3.3V)	26,65,123	14,43,84	21,44,80
VDD12	P	Core Logic Power (1.2V)	10,27,82,106	9,15,58,80	6,59,76

VSS	G	Ground (0V)	64,128	1,42,EPAD	EPAD

4.2 Pin Type Description

TYPE	DESCRIPTION
I	Input
O	Output
OD	Open Drain output
IO	Input / Output
IOD	Input with pull-Down / Output
IOU	Input with pull-Up / Output
IOSU	Input with Schmitt trigger & pull-Up/ Output
P	Power
G	Ground

5. ELECTRICAL SPECIFICATION

5.1 Absolute Maximum Rating

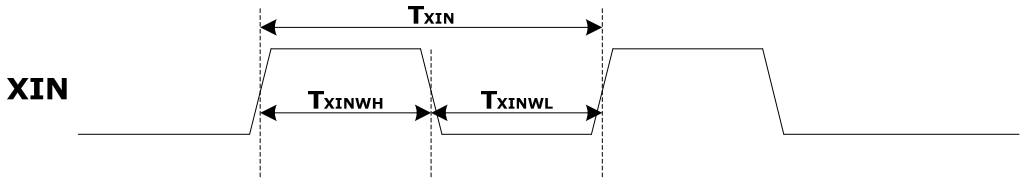
Parameters	Values
Ambient Temperature	-20 ℃ ~ 85 ℃
Storage Temperature	-40 ℃ ~ 125 ℃
Voltage On Any Pin	-0.3V ~ 3.6V
Power Supply Voltage (Core Logic)	-0.5V ~ 1.8V
Power Supply Voltage (I/O Buffer)	-0.5V ~ 4.6V
Injection Current (Latch-Up Testing)	100mA
Crystal Frequency	1MHz ~ 20MHz

5.2 DC Characteristics (Normal I/O)

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
VDD33	I/O Buffer Post-Driver Voltage			2.97	3.30	3.63	V
VDD12	Core Logic Voltage	240MHz		1.14	1.20	1.32	V
MVDD	DRAM DDR2 Power Voltage	360MHZ		1.80	1.90	2.0	V
RTC_VDD	RTC Power Supply			2.0		3.6	V
I_{RTC_VDD}	RTC Supply Current				10		uA
V_{IH}	Input High Voltage			2.0		VDD33+0.3	V
V_{IL}	Input Low Voltage					0.8	V
V_T	Threshold Point				1.65		V
V_{T+}	Schmitt Trigger Low to High Threshold Point			1.7		1.96	V
V_{T-}	Schmitt Trigger High to Low Threshold Point			0.87		1.11	V
I_{CC}	Supply Current		F_{CPU} = 240MHz		230		mA
I_L	Input Leakage Current			-10		10	uA
I_{OZ}	Tri-State Output Leakage Current			-10		10	uA
R_{PU}	Pull-Up Resistor			53	66	120	kohm
R_{PD}	Pull-Down Resistor			37	50	120	kohm
V_{OL}	Output Low Voltage					0.4	V
V_{OH}	Output High Voltage			2.4			V
I_{OL}	Low Level Output Current	4mA I/O	V_{OL} = 0.4V	4.2	6.5	8	mA
		8mA I/O	V_{OL} = 0.4V	8.4	13	16	mA
I_{OH}	High Level Output Current	4mA I/O	V_{OH} = 2.4V	4.7	9.6	14.9	mA
		8mA I/O	V_{OH} = 2.4V	9.4	19.2	29.8	mA

5.3 AC Characteristics (Digital Interface)

5.3.1 Clock Input Characteristics

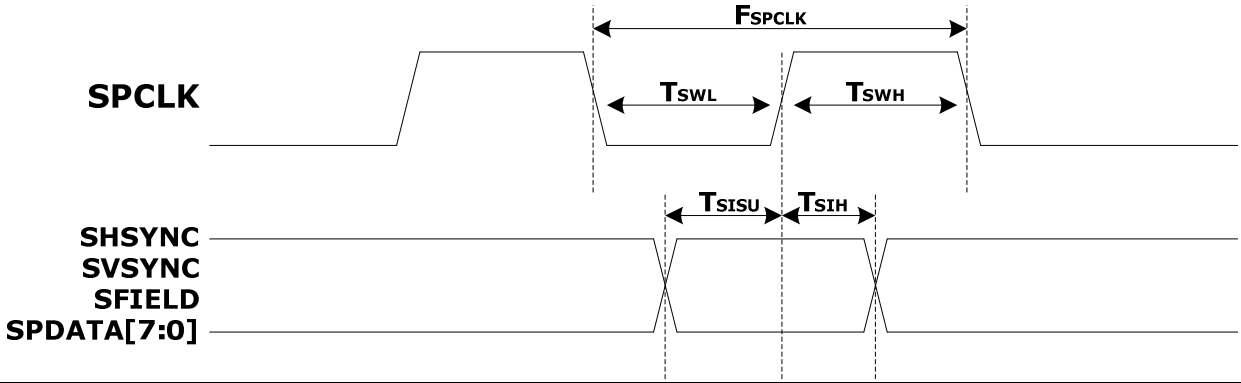


$F_{XIN} = 1 / T_{XIN}$

$XIN_{DUTY} = T_{XINWH} / (T_{XINWH} + T_{XINWL})$

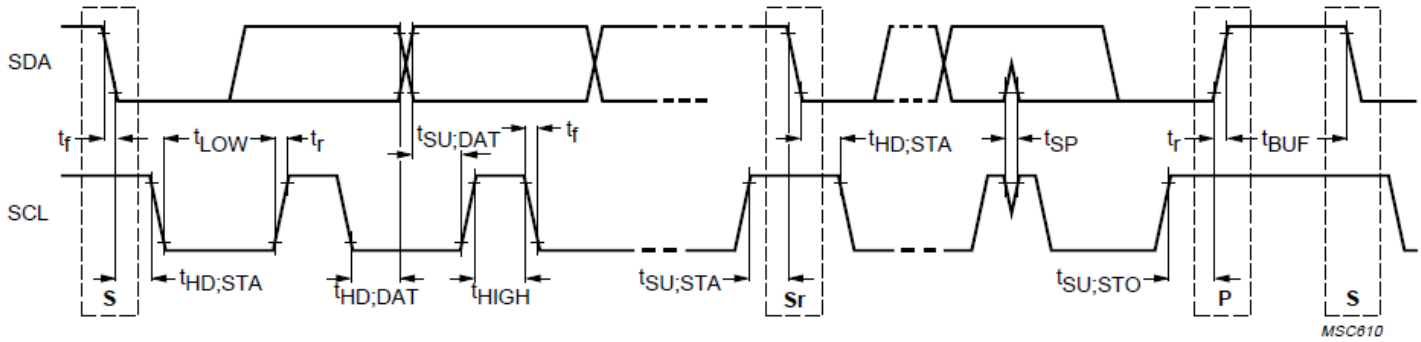
SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
F_{XIN}	Clock Input Frequency	-	12	-	MHz
XIN_{DUTY}	Clock Input Duty Cycle	45	50	55	%

5.3.2 Sensor/Video-In Interface



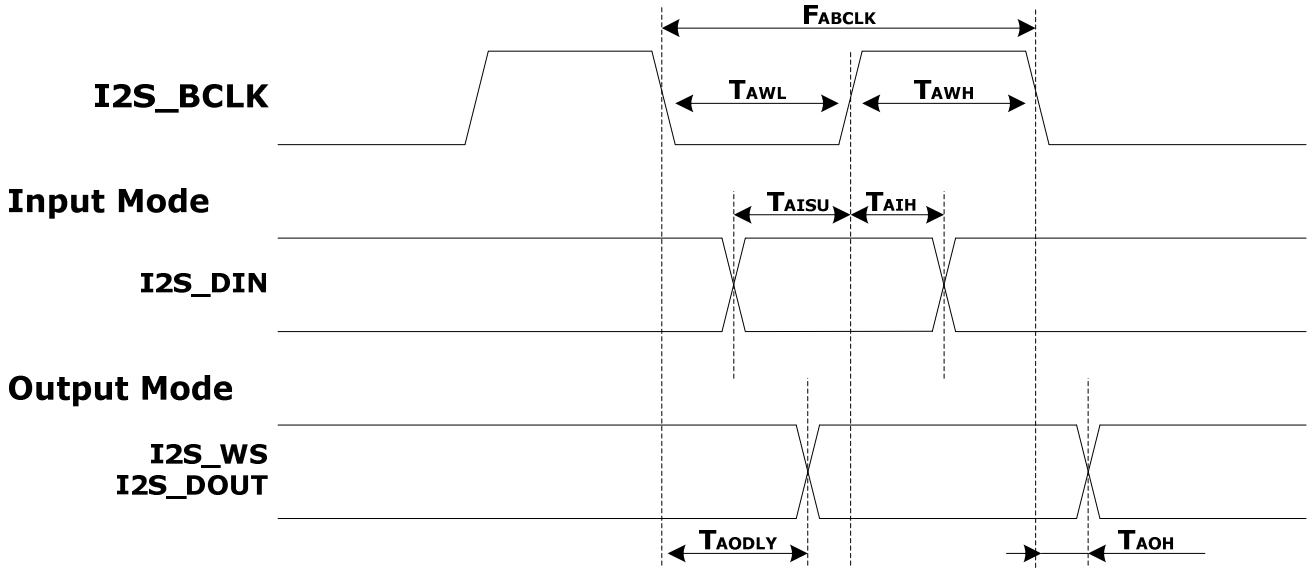
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{SPCLK}	SPCLK Clock Frequency		-	-	72M	MHz
T_{SWL}	SPCLK Clock Low Time		10	-	-	ns
T_{SWH}	SPCLK Clock High Time		10	-	-	ns
T_{SISU}	SHSYNC, SVSYNC, SFIELD, SPDATA[7:0] Setup Time		1.0	-	-	ns
T_{SIH}	SHSYNC, SVSYNC, SFIELD, SPDATA[7:0] Hold Time		1.0	-	-	ns

5.3.3 I2C Interface



PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	–	0.6	–	µs
LOW period of the SCL clock	t_{LOW}	4.7	–	1.3	–	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	–	0.6	–	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	–	0.6	–	µs
Data hold time: for CBUS compatible masters (see NOTE, Section 10.1.3) for I^2C-bus devices	$t_{HD;DAT}$	 5.0 0(2)	 – 3.45(3)	 – 0(2)	 – 0.9(3)	 µs µs
Data set-up time	$t_{SU;DAT}$	250	–	100(4)	–	ns
Rise time of both SDA and SCL signals	t_r	–	1000	$20 + 0.1C_b$(5)	300	ns
Fall time of both SDA and SCL signals	t_f	–	300	$20 + 0.1C_b$(5)	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	–	0.6	–	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	1.3	–	µs
Capacitive load for each bus line	C_b	–	400	–	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	$0.1V_{DD}$	–	$0.1V_{DD}$	–	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	$0.2V_{DD}$	–	$0.2V_{DD}$	–	V

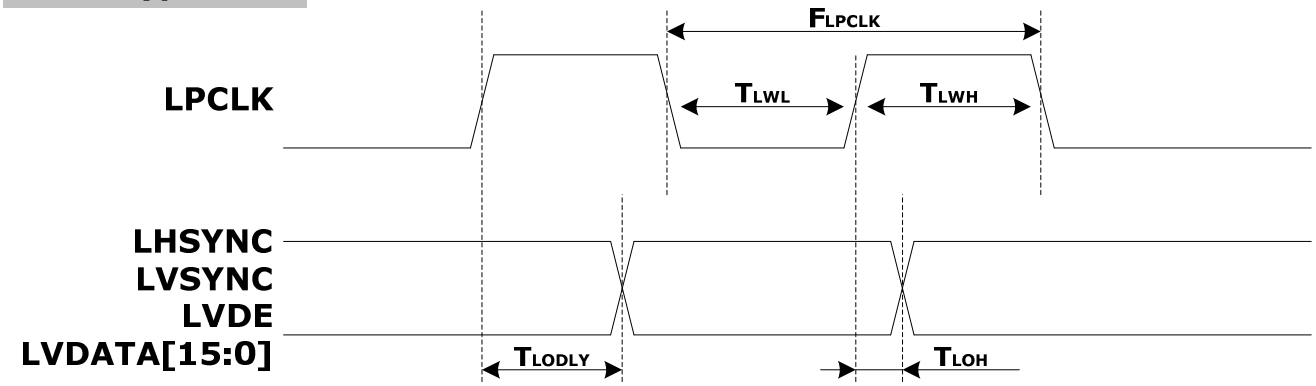
5.3.4 I2S Interface



Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{ABCLK}	I2S_BCLK Clock Frequency		-	-	16	MHz
T_{AWL}	I2S_BCLK Clock Low Time		31.25	-	-	ns
T_{AWH}	I2S_BCLK Clock High Time		31.25	-	-	ns
T_{AISU}	I2S_DIN Setup Time		10	-	-	ns
T_{AIH}	I2S_DIN Hold Time		10	-	-	ns
T_{AODLY}	I2S_DOUT Output Delay Time		-	-	0.5	ns
T_{AOH}	I2S_DOUT Output Hold Time		0.1	-	-	ns

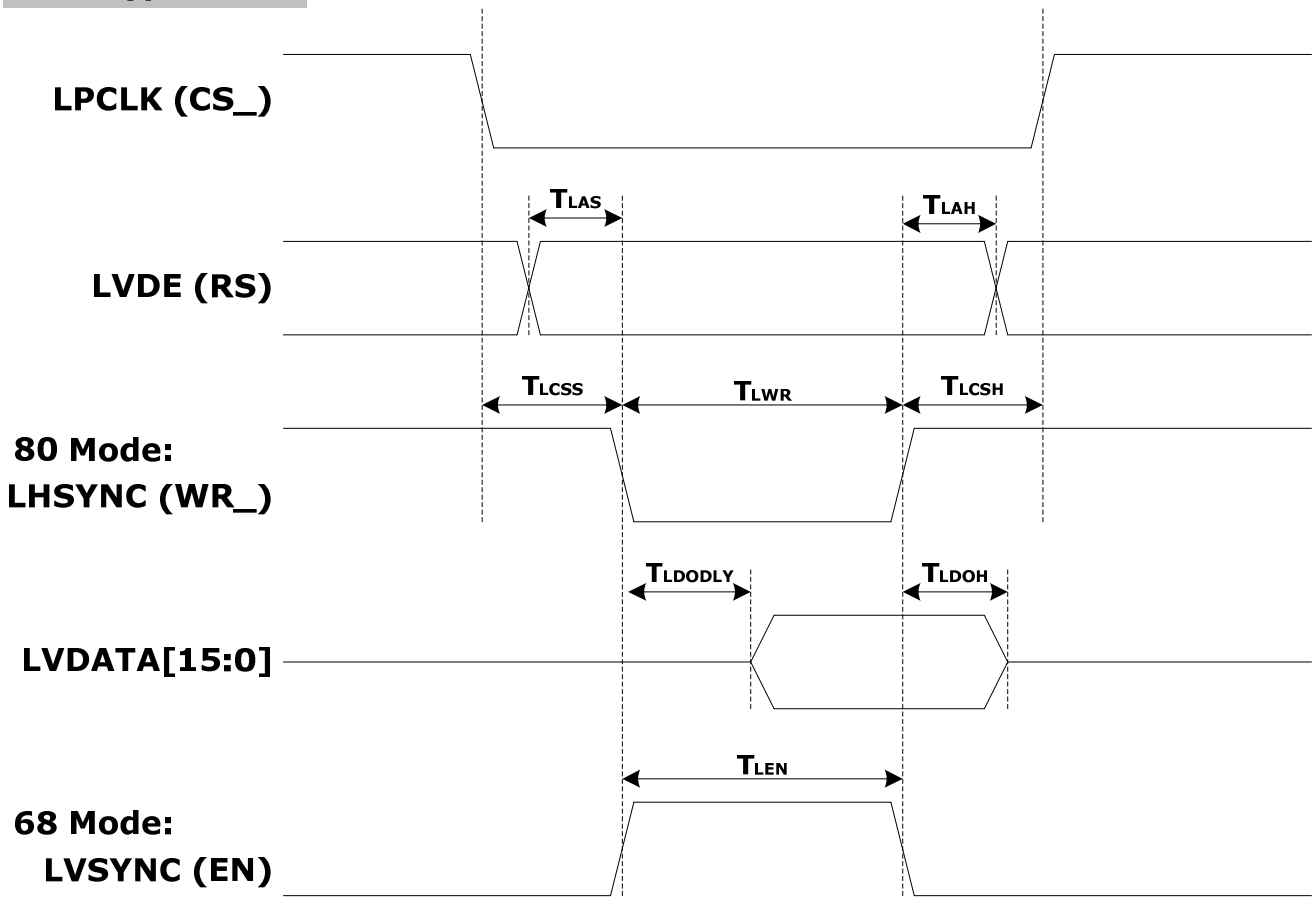
5.3.5 LCD/Display Interface

SYNC Type LCD



Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{LPCLK}	LPCLK Clock Frequency		-	-	120	MHz
T_{LWL}	LPCLK Clock Low Time		18.5	-	-	ns
T_{LWH}	LPCLK Clock High Time		18.5	-	-	ns
T_{LODLY}	LHSYNC, LVSYNC, LVDE and LVDATA Output Delay Time		-	-	1.3	ns
T_{LOH}	LHSYNC, LVSYNC, LVDE and LVDATA Output Hold Time		0.67	-	-	ns

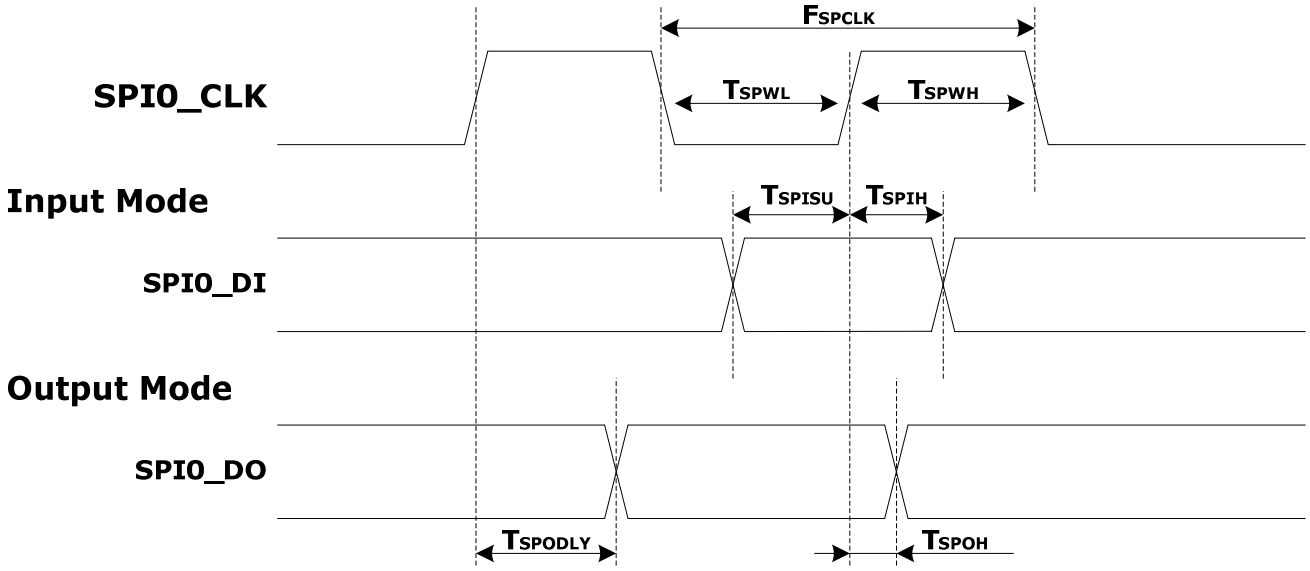
MPU Type LCD



Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{LCSS}	CS_ to WR_ Setup Time		2	-	-	PCLK
T_{LCSH}	CS_ to WR_ Hold Time		1	-	-	PCLK
T_{LAS}	RS to WR_ Setup Time		1	-	-	PCLK
T_{LAH}	RS to WR_ Hold Time		1	-	-	PCLK
T_{LDODLY}	LVDATA Output Delay Time		-	-	1	PCLK
T_{LDOH}	LVDATA Output Hold Time		1	-	-	PCLK
T_{LWR}	WR_ Pulse Width	80 Mode	1	-	-	PCLK
T_{LEN}	EN Pulse Width	68 Mode	1	-	-	PCLK

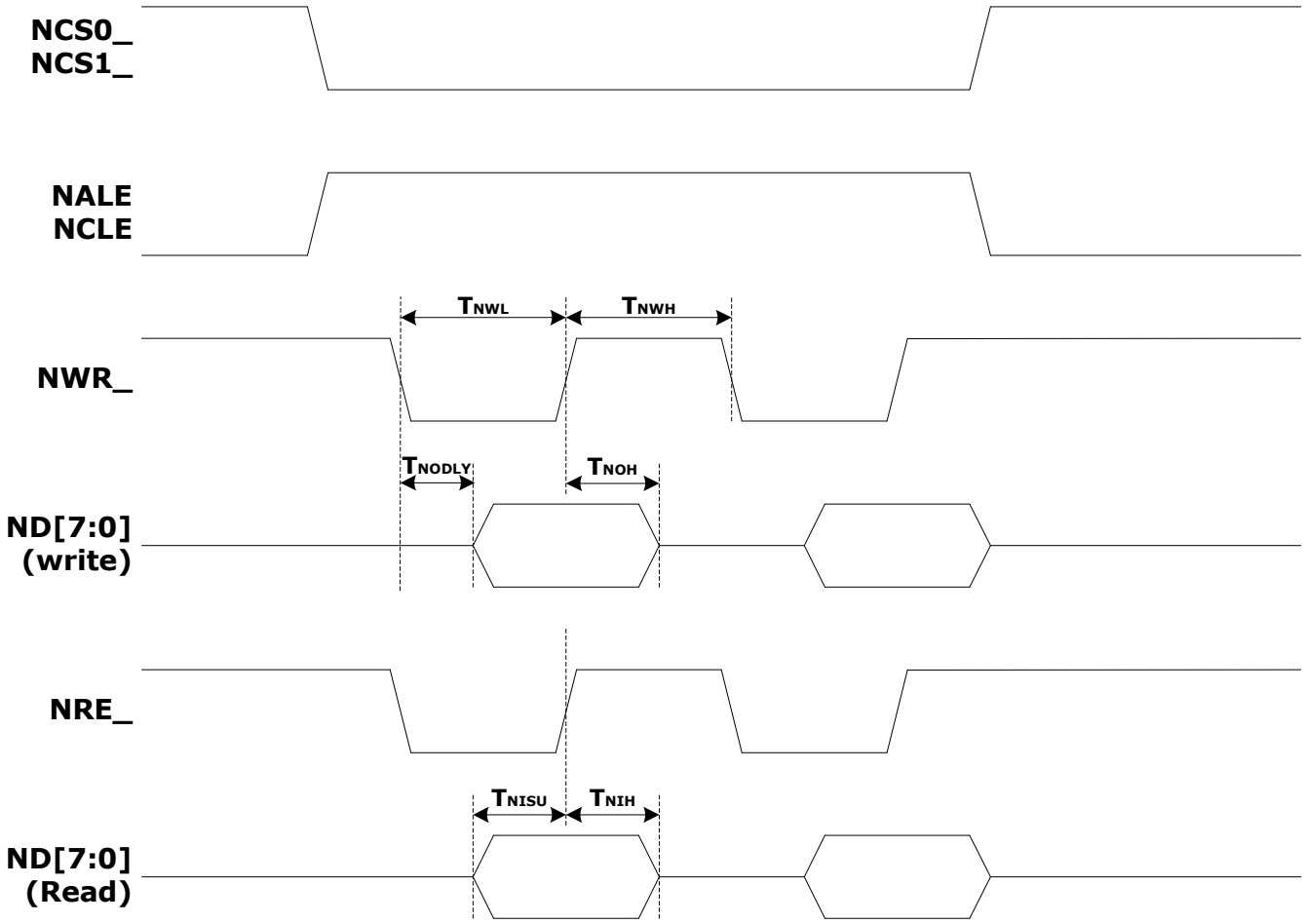
Note: Where PCLK is APB bus clock.

5.3.6 SPI Interface



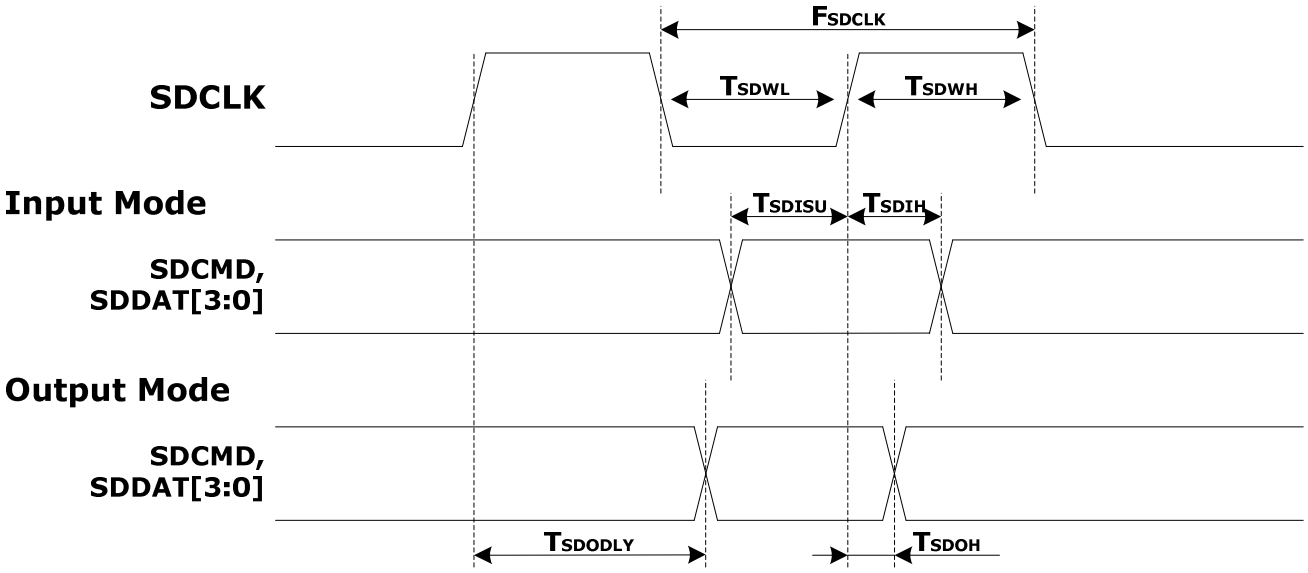
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{SPCLK}	SPI0_CLK Clock Frequency		-	-	25	MHz
T_{SPWL}	SPI0_CLK Clock Low Time		20	-	-	ns
T_{SPWH}	SPI0_CLK Clock High Time		20	-	-	ns
T_{SPISU}	SPI0_DI Setup Time		10	-	-	ns
T_{SPIH}	SPI0_DI Hold Time		10	-	-	ns
T_{SPODLY}	SPI0_DO Output Delay Time		-	-	1	ns
T_{SPOH}	SPI0_DO Output Hold Time		0.2	-	-	ns

5.3.7 NAND Interface



Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{NWL}	Write Pulse Low Width		10	-	-	ns
T_{NWH}	NWR_ High Hold Time		10	-	-	ns
T_{NODLY}	ND[7:0] Output Delay Time		-	-	2.5	ns
T_{NOH}	ND[7:0] Output Hold Time		10	-	-	ns
T_{NISU}	ND[7:0] Data in Setup Time		3.2	-	-	ns
T_{NIH}	ND[7:0] Data in hold time		1	-	-	ns

5.3.8 SD Card Interface

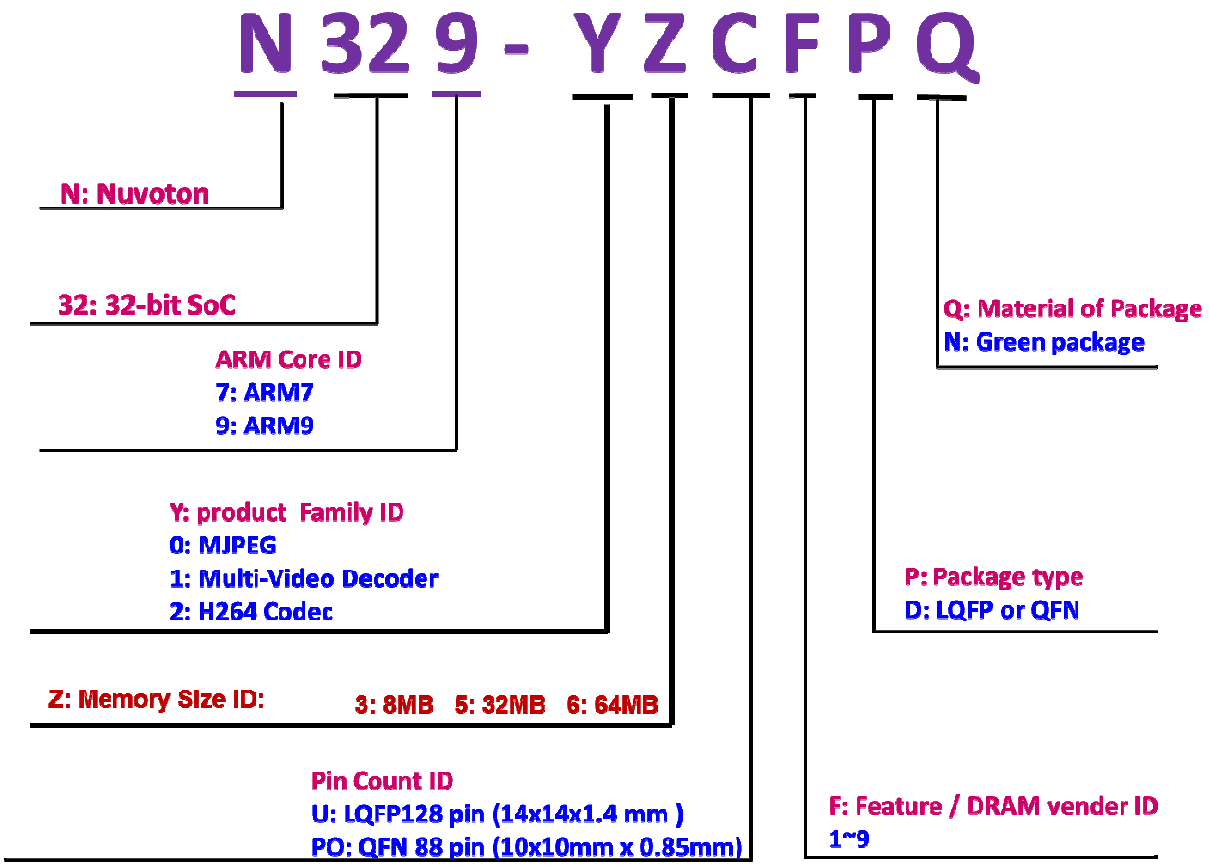


Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Clock SDCLK						
F_{SDCLK}	Clock Frequency in Data Transfer Mode		-	-	50	MHz
F_{SDCLK}	Clock Frequency in Identification Mode		100	-	400	KHz
T_{SDWL}	Clock Low Time		10	-	-	ns
T_{SDWH}	Clock High Time		10	-	-	ns
Input SDCMD, SDDAT[3:0] (referenced to SDCLK)						
T_{SDISU}	Input Setup Time		6	-	-	ns
T_{SDIH}	Input Hold Time		2	-	-	ns
Output SDCMD, SDDAT[3:0] (referenced to SDCLK)						
T_{SDODLY}	Output Delay Time		-	-	14	ns
T_{SDOH}	Output Hold Time		2.5	-	-	ns

6. ORDERING INFORMATION

PART NO.	PACKAGE TYPE	DESCRIPTION
N32926U1DN	LQFP-128, MCP[1]	Stacked 32Mbit x16 SDR MCP with LCD interface.
N32925U3DN	TQFP-64, MCP	Stacked 16Mbit x 16 DDR MCP with LCD interface
N32923U1DN	LQFP-128, MCP	Stacked 4Mbit x16 DDR MCP with LCD interface.
N32926O1DN	QFN88, MCP	Stacked 32Mbit x16 DDR MCP without LCD (2nd CAP)
N32926O2DN	QFN88,MCP	Stacked 32Mbit x16 DDR MCP without LCD & RTC (Dual CAP)

6.1 Part Number Definition



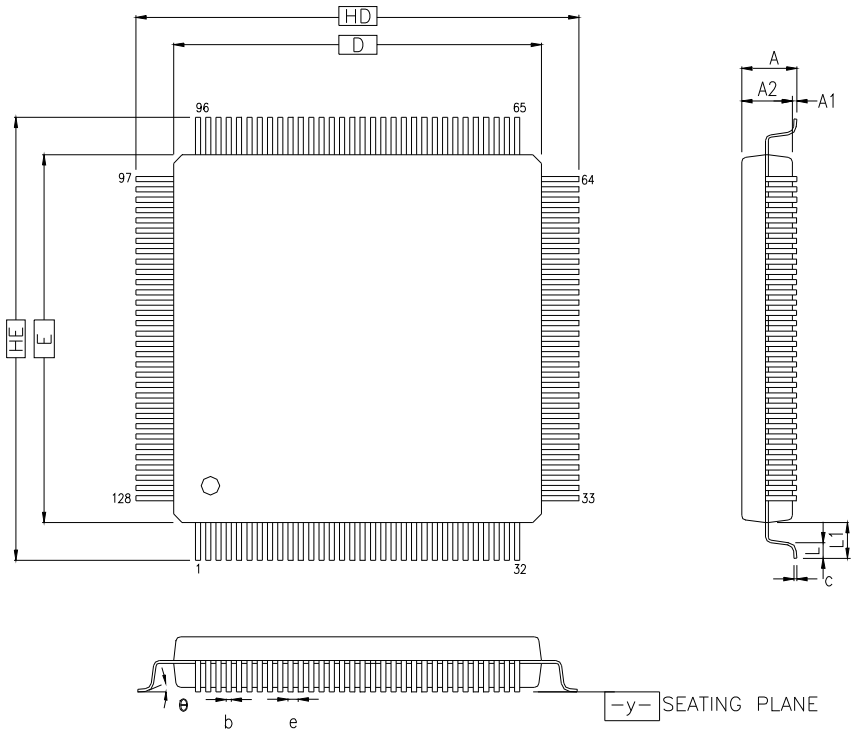
[1] MCP stands for Multi-Chip Package.

6.2 Difference between N3292x series

	DRAM Type/ Capacity	LCD & NAND	CAP Interface	RMII&SDIO	RTC
N32926U1DN	DDR2/ 64MBytes	V	1st + 2nd	V	V
N32925U3DN	DDR2/ 32MBytes	V	1st + 2nd	V	V
N32923U1DN	DDR/ 8Mbytes	V	1st + 2nd	V	V
N32926O1DN	DDR2/ 64MBytes	--	2nd	Either	V
N32926O2DN	DDR2/ 64MBytes	--	1st + 2nd	V	--

7. PACKAGE SPECIFICATIONS

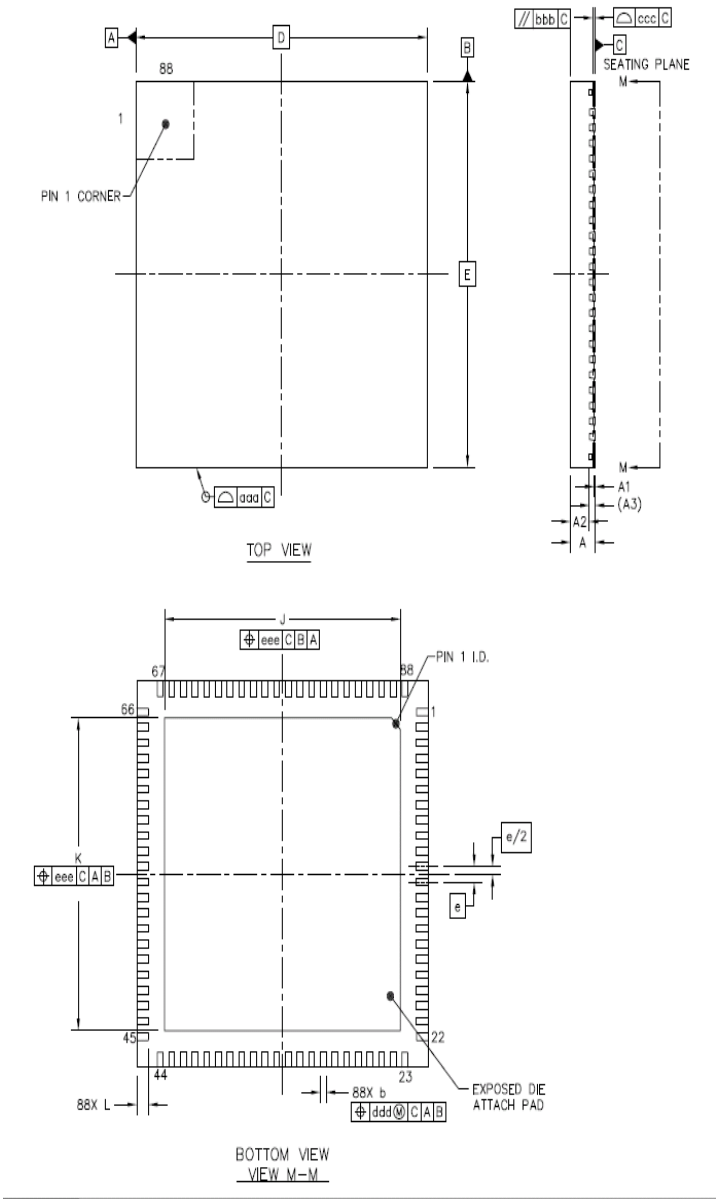
7.1 LQFP-128 Package Outline Drawing



COTROL DIMENSIONS ARE IN MILLIMETERS.

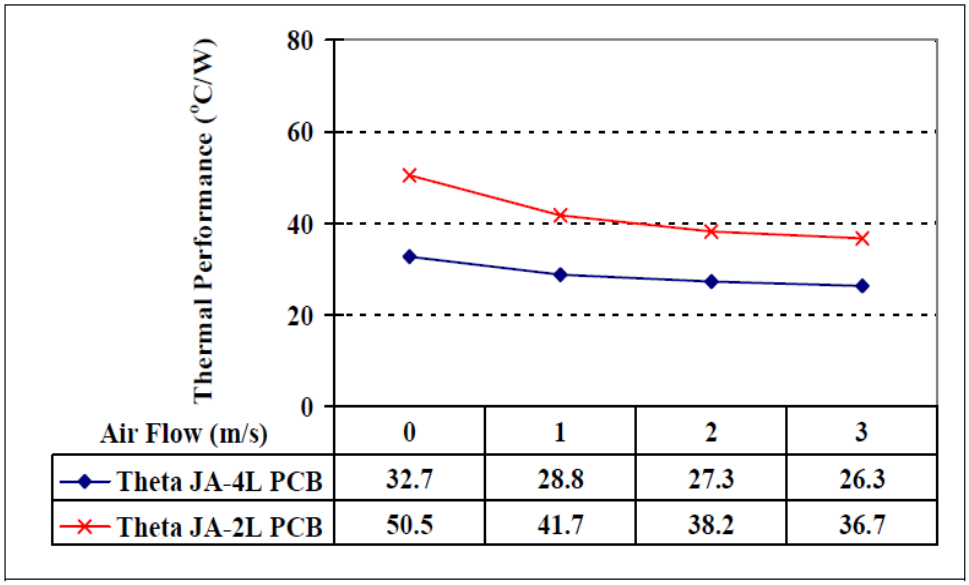
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
HD	16.00 BSC.			0.630 BSC.		
D	14.00 BSC.			0.551 BSC.		
HE	16.00 BSC.			0.630 BSC.		
E	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
y	–	–	0.1	–	–	0.004

7.2 QFN-88 Package Outline Drawing



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		10 BSC	
	Y	E		10 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	8	8.1	8.2
	Y	K	8	8.1	8.2
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

7.3 Thermal Characteristics



Air Flow (m/s)	0	1	2	3
Theta JA-4L PCB	32.7	28.8	27.3	26.3
Theta JA-2L PCB	50.5	41.7	38.2	36.7

The relationship between junction temperature, T_j, ambient temperature, T_A, thermal resistance, θja, and chip power consumption, P,

$$\theta_{JA} = \frac{T_J - T_A}{P}$$

8. REVISION HISTORY

Version	Date	Description
A0	Nov. 01, 2013	● Initial release.
A1	Dec. 10, 2013	● Correct SAR ADC channels. ● Update ambient temperature from -20 ℃ ~ 80 ℃. ● Change VDD power supply to 1.14V ~ 1.32V. ● Unify symbol of pin 11, 12, 83, 84 to MVDD. ● Change MVDD power supply to 1.8V ~ 2.0V.
A2	Dec. 26, 2013	● Add multi-function LVD_O on Pin 1. ● Add multi-function POR_O on Pin 2. ● Add multi-function Line_In on Pin 95. ● Revise ADC information and correct some mistake of IO type
A3	Feb. 21, 2014	● Revise general description ● Change ambient temperature of operation to -20°C~85°C
A4	Apr. 10, 2014	● Include N3292xPxDN and N3292xOxDN ● Include 8MB DDR MCP option
A5	Jun. 12, 2014	● Add N3292xO2DN PKG ● Remove N3292xPxDN PKG
A5.1	Aug. 22, 2014	● Revise pin description typo of page 26 that N32926O1DN pin 15 should be VDD12 not VDD33.

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