NUC970 Series Hardware Design Guide

Application Note for ARM926EJ-S Based

Rev.1.5 — Sept. 10, 2015

Document Information

Abstract	NUC970 hardware development guide is intended for hardware system designers who require a hardware implementation overview for NUC970 base system. The feature included an embedded basic 12MHZ external crystal, 32.768K RTC backup power circuitry with power on/off control, USB Host reference circuitry, USB2.0 Hi Speed device reference circuitry, SARADC reference schematic for BAT voltage detection, IIC, IIS for audio codec, Ethernet, Smart Card Interface, CMOS sensor and 24-bit LCD interface, scan key application and UART (universal asynchronous receiver/transmitter). By the way, NUC970 have various memories interface, SD, eMMC, NAND flash, SPI flash and EBI interface for system storage and data accesses. This document shows how to use the NUC970 series MPU and describes the minimum hardware resources required to develop a basic system. This design guide can be adapted to others NUC970 series MPU with others package.
Apply to	NUC970 Series.

Table of Contents

1 Power Supplies

This section describes design considerations related to the NUC970 series MPU's power supply scheme and power operating modes.

1.1 Power Supply Scheme

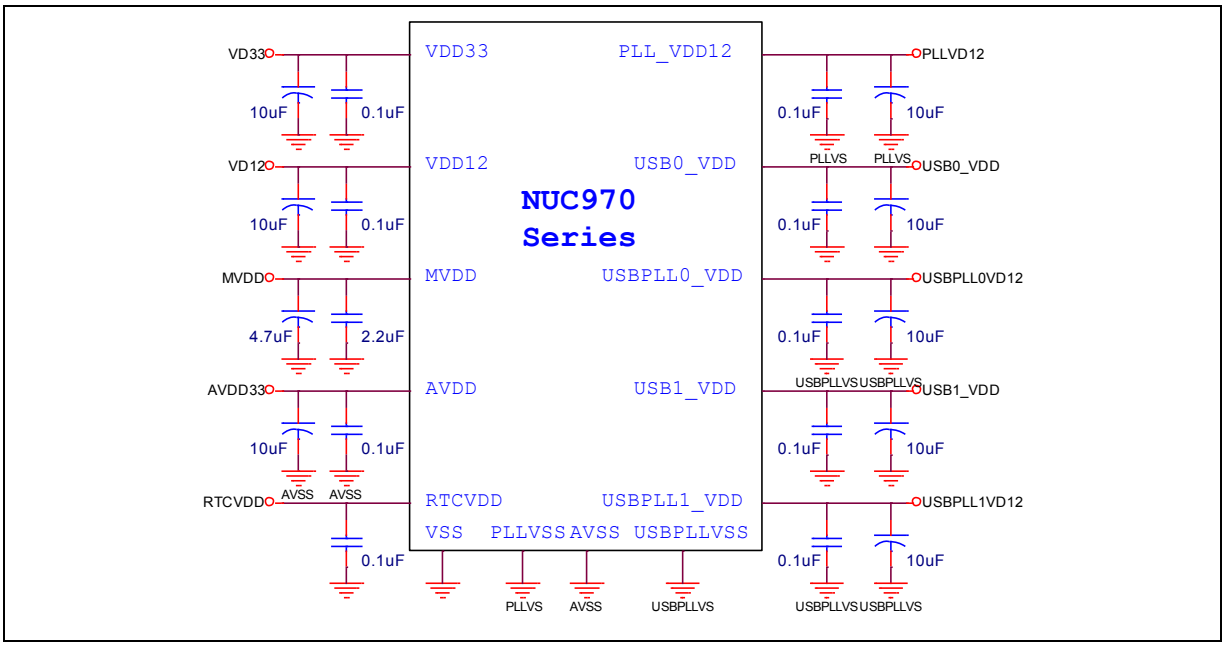
The NUC970 series MPU should be supplied by a stabilized power; VDD (Digital IO 3.3V), VDD12 (Core 1.2V), MVDD (DDRII 1.8V), AVDD (Analog 3.3V), USB0_VDD/ USB1_VDD (Universal Serial Bus 3.3V) and PLLVDD (Phase Lock Loop 1.2V), USBPLL (USB Phase Lock loop 1.2V).

Some precautions need to be taken when using these powers:

- The VDD33 pins must be connected to 3.0V~3.6V voltage supply with external decoupling capacitors (a 0.1uf capacitor and a 10uf capacitor for each VDD pin).
- The VDD12 pins must be supplied by 1.2V±5% with the decoupling capacitors (a 0.1uf and a 10uf for each one of the VDD12 pin.
- The MVDD pins must by supplied by 1.8V±5% with the decoupling capacitors (a 2.2uf and a 4.7uf for each one of the MVDD).
- The AVDD pin must be connected to 3.0V~3.6V voltage supply with external decoupling capacitors (a 0.1uf capacitor and a 10uf capacitor for each AVDD pin).
- The RTCVDD is a RTC power pin which should be provide a 3.3V±10% with a decoupling capacitor 0.1uf.
- The PLLVDD is a phase lock loop power pin which should be supplied by a 3.3V±10%, and connected with a 10uf and 0.1uf for decoupling.
- The USB0VDD pin should be supplied by a 3.3V with a decoupling capacitor, 10uF for USB0 port.
- The USBPLL0 VDD pin should be supplied a 1.2V with a decoupling capacitor, 10uf and 0.1uf for USBPLL0.
- The USB1VDD pin should be provided by a 3.3V with a decoupling capacitor, 10uF for USB1 port.
- The USBPLL0 VDD pin should be supplied a 1.2V with a decoupling capacitor, 10uf and 0.1uf for USBPLL0.

Additional precautions need to be taken to filter analog noise. The following is suggestion for designing the board level system for AVDD can be connected to VDD through a ferrite bead.

Figure 1-1 Power Supply Scheme



1.2 RESET

Hardware Reset Conditions:

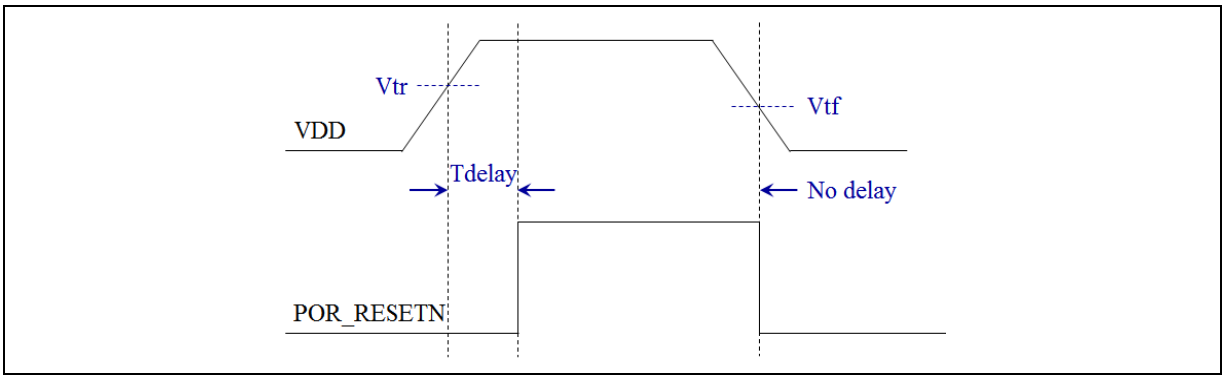
- Power-on Reset (POR).
- Low level on the nRESET Pin (nRST).
- Watch-dog time-out reset (WDT).
- Low voltage reset (LVR).

The internal Power On Reset (POR) circuit without any external resistor or capacitor. It supports a power on ratio within 1V/0.1us~1V/100ms. The reset signal may not be available if the power rises too fast or too slow and the ratio goes beyond the range 1V/01us~1V/100ms.

Table 1.2-1 Internal Power-On Characteristics

CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
Power Supply	VDD	2	3.3	3.6	V	Ramp raio 1.0V/100ms
Reset Trigger Level	Vtr	1.05	1.57	1.98	V	Ramp raio 1.0V/0.11us
	Vtf	1	1.64	1.98	V	
Reset Delay Time	Tdelay	85	150	7500	us	

Figure 1.2-1 POR Waveform



The Watchdog Timer is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Power-down mode and Deep Power-down mode.

The purpose of Watchdog Timer (WDT) is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

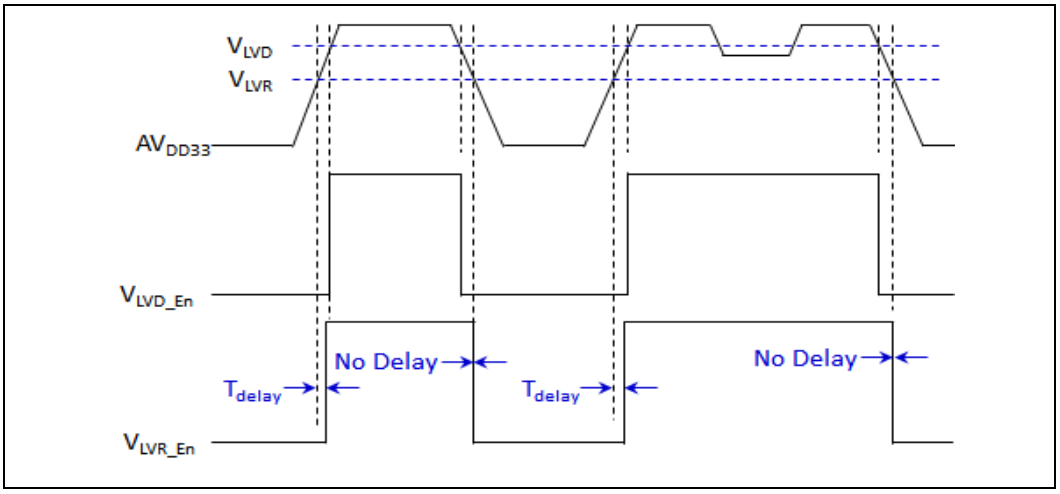
- 18-bit free running up counter for WDT time-out interval
- Selectable time-out interval (2^4 ~ 2^{18}) and the time-out interval is 0.48828125 ms ~ 8 s if WDT_CLK = 32.768 kHz
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1024+2、128+2、16+2 or 1+2 WDT_CLK reset delay period
- Supports WDT time-out wake-up function only if WDT clock source is selected as 32 kHz low-speed oscillator.
- Supports to force WDT enabled after chip powered on or reset by setting WDTON in PWRON register

The Low Voltage Reset (LVR) and the Low Voltage Detector (LVD) both will generate logic high or logic low output for digital core once the monitored power, VDD, surpasses or falls below their detection level. The block diagram as Figure

Table 1.2-2 Internal LVR/LVD Characteristics

CHARATERISTICS	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
Analog Power	AVDD	2.97	3.3	3.63	V	
Core Power	VDD12	1.14	1.2	1.26	V	
LVD Detect Levels	VDET_LVD1	2.34	2.6	2.86	V	LVD_SEL=0, VDD rises
	VDET_LVD2	2.295	2.55	2.805	V	LVD_SEL=0, VDD falls
	VDET_LVD3	2.52	2.8	3.08	V	LVD_SEL=1, VDD rises
	VDET_LVD4	2.475	2.75	3.025	V	LVD_SEL=1, VDD falls
LVR Detect Levels	VDET_LVR1	2.16	2.4	2.64	V	VDD rises
	VDET_LVR2	2.115	2.35	2.585	V	VDD falls
LVR Output Delay	Tdelay	100	320	600	uS	VDD rises @ 3V/10us

Figure 1-2 LVR and LVD Timing Waveform



Note:

1. When testing the features of LVD/LVR detect levels, the power-up or power-down speed of VDD should be slower than 500mS/2V.

2. When testing the output delay of LVR, the power-up speed of VDD should be faster than 10uS/3V.

Table 1.2-3 Power-On Reset at POR33

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
AVDD	3.3V power		3.3		V	-
T_r	Power Rising Rate Voltage	1V/1uS	-	-	V	AVDD rising from 0V to 3.3V
V_{rr}	Active level	1.65	1.82	2.0	V	Power slew rate is 3.3V/20mS.
Tpor	POR output low duration		5.2		uS	-

Figure 1-3 Power-On Reset at POR33

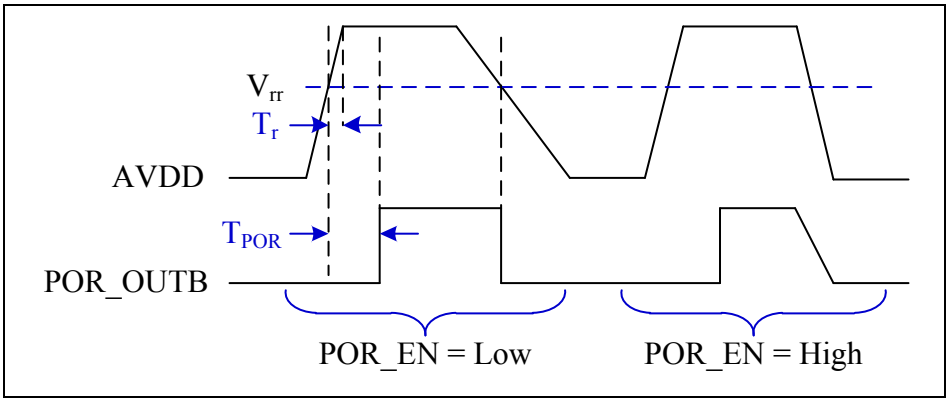
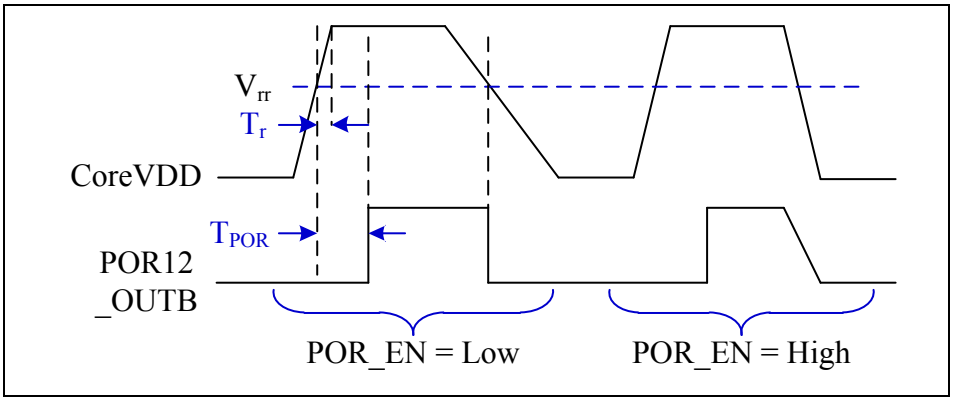


Table 1.2-3 Power-On Reset at POR12

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
CoreVDD	1.2V power		1.2		V	-
T_r	Power Rising Rate Voltage	1V/1uS	-	-	V	-
V_{rr}	Active level	0.63	0.76	0.86	V	Power slew rate is 1.2V/20mS.
Tpor	POR output low duration		4.25		uS	-

Figure 1-5 Power-On Reset at POR12



1.3 Power on setting

The power-on setting is used to configure the chip to enter the specified state when the chip is powered up or reset. Since each pin of power on setting has an internal pulled-up resistor when in reset period. If the application needs to set the configuration to “0”, the proper pull-down must be added resisters for corresponding configuration pins.

The entire configuration table is listed as below:

Note:

a. 1 = open, 0 = pulled down.

b. PA [9:0] = CFG [9:0]

Table 1.3-1 System Power-On Setting Guide for booting mode.

PA.1	PA.0	Booting From
0	0	USB.
0	1	eMMC Flash.
1	0	NAND Flash.
1	1	SPI Flash.

Table 1.3-2 System Power-On Setting Guide for system clock source.

PA2	System Clock Source
0	12MHz crystal.
1	PLL output.

Table 1.3-3 System Power-On Setting Guide for booting mode.

PA3	Watch Dog Setting
0	Disable after power on.
1	Enable after power on.

Table 1.3-4 System Power-On Setting Guide for booting mode.

PA4	Setting PJ[4:0]
0	As GPIO pin.
1	As JTAG interface.

Table 1.3-5 System Power-On Setting Guide for booting mode.

PA5	UART Debug Message
0	Output turn on.
1	Output turn off.

Table 1.3-6 System Power-On Setting Guide for NAND flash page size.

PA7	PA6	NAND Flash Page Size
0	0	2K page.
0	1	4K page.
1	0	8K page.
1	1	None.

Table 1.3-7 System Power-On Setting Guide for NAND flash ECC type.

PA9	PA8	NAND Flash ECC Type
0	0	BCH 12T.
0	1	BCH 15T.
1	0	BCH 24T.
1	1	None.

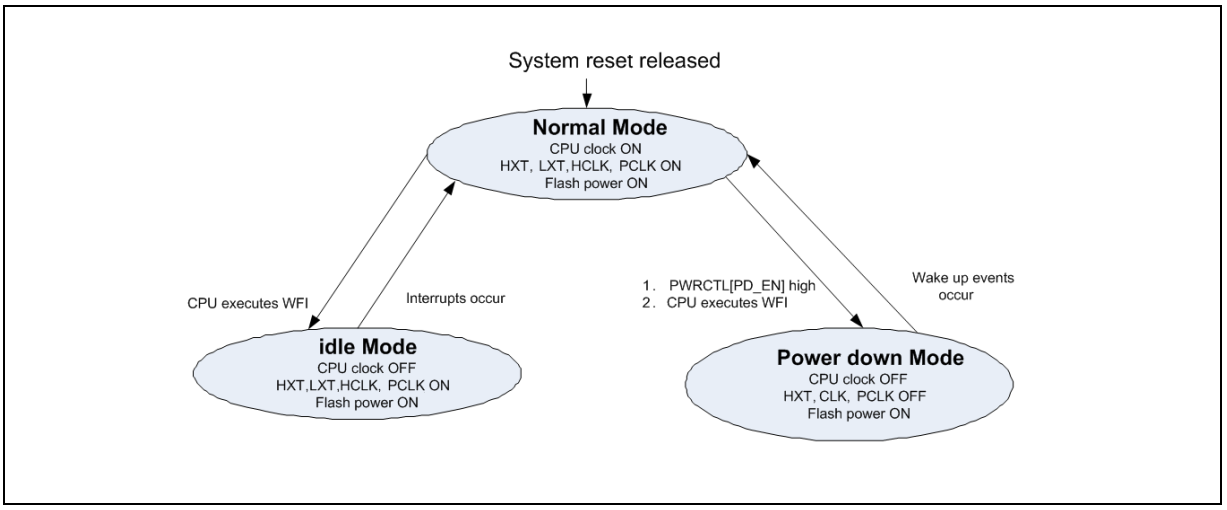
1.4 Power Operating Modes

The NUC970 series MPU has four kinds of operating modes:

- Normal mode: CPU runs normally and all clocks are ON.
- Idle mode: CPU entering Sleep mode while CPU clock stops and other clocks are ON.
- Power-down mode: All clocks stop, except LXT and SRAM retention.
- Deep Power-down mode:

As the control flow chart below, under Normal mode the CPU and the peripheral device works normally; under Idle mode the CPU stops to work and the peripheral device works normally; under Power-down mode both the CPU and the peripheral device stop, the high frequency crystal and oscillator input will be disabled to reduce power consumption. While low frequency crystal and oscillator can be enabled by program control to support the peripheral functions (e.g. RTC, Watchdog Timer) to work in Power-down mode, which is the best power saving mode.

Figure 1-4 Power Operating Modes



2 Clock Circuitry

This section describes design considerations related to the NUC972 series MPU's clock oscillation module.

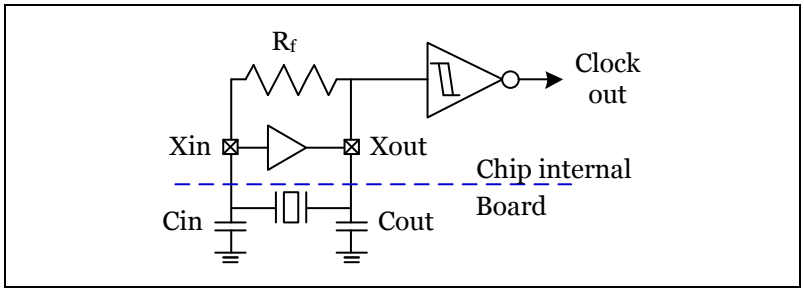
2.1 External Crystal Sources

Two external clock sources are used for the NUC970 series MPUs:

- Main clock: 12MHz high speed crystal for the microcontroller.
- Sub-clock: 32.768KHz low speed crystal is for RTC operation.

The oscillators of main clock and sub-clock which are connected with a quartz X'tal and two capacitors externally.

Figure 2-1 Crystal Oscillator Circuit



Cin, Cout: External capacitors

Rf: Built-in feedback resistor

X'tal: External X'tal

The external crystal oscillator and two capacitors are connected to the pad "Xin" and pad "Xout". The capacitance value of the two capacitors may be changed for differential crystal oscillator from different vender.

Main Clock: 12MHz High Speed Crystal

For Cin and Cout is recommended to use high-quality ceramic capacitors in the 5 pF-to-20 pF range (typ.), designed for high-frequency applications and selected to meet the requirements of the crystal or resonator. Cin and Cout are usually the same value. The crystal manufacturer typically specifies a load capacitance that is the series combination of Cin and Cout. The PCB and MPU pin capacitances must be included when sizing Cin and Cout (10pF can be used as a rough estimation of the combined pin and board capacitance).

Table 2.1-1 12MHz Cin, Cout & Rf Recommend Value

Board Parameter	Symbol	Value

XIN, XOUT Capacitance	Cin, Cout	5~20pF

RTC Clock: 32.768 KHz Low Speed Crystal

For Cin and Cout is recommended to use high-quality ceramic capacitors in the 15pf-to-33pf range (typ.), designed for RTC applications and selected to meet the requirements of the crystal or resonator. Cin and Cout, are usually the same value. The crystal manufacturer typically specifies a load capacitance that is the series combination of Cin and Cout. The PCB and MPU pin capacitances must be included when sizing Cin and Cout (10pf can be used as a rough estimation of the combined pin and board capacitance).

Table 2.1-2 32.768KHz Cin, Cout & Rf Recommend Value

Board Parameter	Symbol	Value
RTC_IN, RTC_OUT Capacitance	Cin, Cout	15~33pf

2.2 PCB Design Guide

Applications requiring low power oscillators on NUC970 series MPUs must take PCB layout into consideration. The oscillators on NUC970 series MPUs consume very little current, and it sometimes makes the oscillator circuit sensitive to neighboring circuits. The following lists some PCB design guidelines:

1. Keep PCB trace as short as possible because the longer trace leads will increase parasitic capacitance and might induce coupling issue.

2. Reduce power supply noise; connect a de-coupling capacitor between VDD and VSS will suppress from system power traces.

3. Place oscillator module correctly to prevent noise source from influencing of oscillator block and Xin/ Xout pins.

4. The load capacitors Cin/ Cout should be placed close to the crystal pins, and the trace length should be as short as possible.

3 SAR_ADC

This section describes design considerations related to the NUC970 series MPU's ADC module.

3.1 Analog Signals

The analog-to-digital converter contains one 12-bit Successive Approximation Register analog-to-digital converter (SAR A/D converter) with eight input channels. The A/D converter supports two operation modes: 4-wire or 5-wire mode. The ADC is especially suitable to act as touch screen controller. Battery voltage detection could be easily accomplished by the SAR ADC. It has keypad interrupt signal generator.

3.2 Features

- Resolution: 12-bit resolution.
- DNL: +/-1.5 LSB, INL: +/-3 LSB.
- Dual Data Rates: 1MSPS/200KSPS.
- Analog Input Range: VREF to AGND, could be rail-to-rail.
- Analog Supply: 2.97-3.63V.
- Digital Supply: 1.2V.
- 8 Single-Ended Analog inputs.
- Compatible with 4-wire or 5-wire Touch Screen Interface.
- Touch Pressure Measurement for 4-wire touch screen application.
- Direct Battery Measurement.
- Keypad Interrupt Generator.
- Auto Power Down.
- Low Power Consumption: 4850uW(@1MSPS) / 2170uW(@200KSPS), < 1uA

3.3 Block Diagram

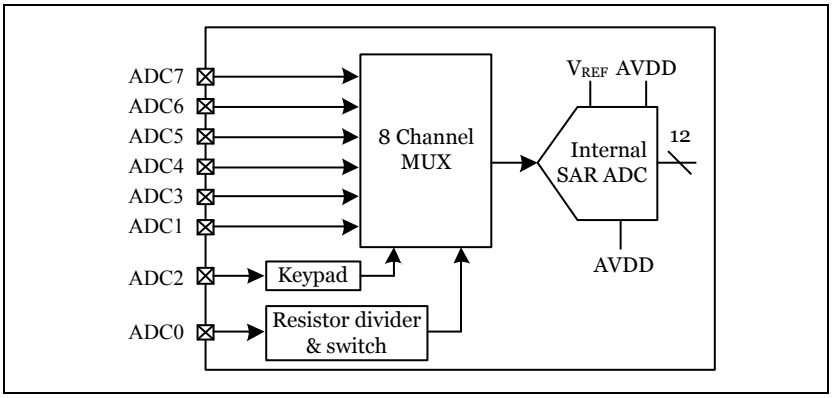
Figure 3-1 is the whole ADC function block diagram. The SAR-ADC supports 8 input channels. The channel selection is controlled by the IN_SEL[2:0]. ADC.0 can support battery voltage detection. Therefore, it includes the block “Resistor Divider & Switch”. ADC.1 is for high speed sampling rate (1MSPS). ADC2 are for low speed sampling rate (200KSPS), and ADC.0 needs lengthy sampling time because it entrains 10 kΩ resistances. ADC.2 is also for keypad application. Remaining channel of ADC[7:3] is for touch panel application.

Table 3.3 ADC input channel selection table

IN_SEL[2:0]	ADC Input Channel	Description
000 (ADC0)	VBT	Intended for battery voltage detection. It includes an inherent resistor divider and a switch.
001 (ADC1)	VHS	ADC high speed input port. VHS = 1, it supports 1MS/S. VHS = 0, it supports 200KS/S.
010 (ADC2)	A_2	A low speed input which could support 200KS/S; Keypad signal input pin.
011 (ADC3)	VSENSE	The input port is intended for 5-wire touch screen detection.
100 (ADC4)	YM	ADC analog input. If used in touch screen, it should connect to the negative end of Y axis. If used in 5-wire touch screen, it could connect to lower-left electrode.
101 (ADC5)	YP	ADC analog input. If used in touch screen, it should connect to the positive end of Y axis. If used in 5-wire touch screen, it could connect to upper-right electrode.
110 (ADC6)	XM	ADC analog input. If used in touch screen, it should connect to the negative end of X axis. If used in 5-wire touch screen, it could

		connect to lower-right electrode.
111 (ADC7)	XP	ADC analog input. If used in 4-wire touch screen, it should connect to the positive end of X axis. If used in 5-wire touch screen, it could connect to upper-left electrode.

Figure 3-1 ADC Functional Block Diagram



3.4 SAR ADC reference voltage

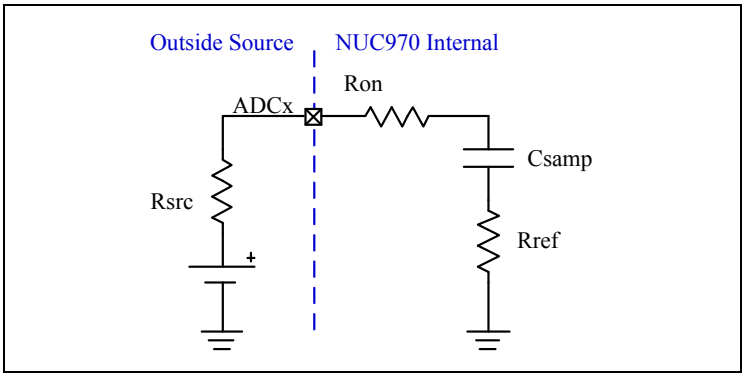
The VREF is an analog referent input for SAR ADC, one external decoupling capacitor at this pin to ground is must.

3.5 Input Signal Impedance (Excluding ADC 0)

Figure 3-2 is the whole simplified sampling diagram. The input current on analog input pins depends on analog input voltage and sampling rate. In the sampling mode, the input current charges the internal sampling capacitor. After the capacitor is fully charged, the current will be off. The internal sampling capacitor must be charged to 12-bit settling level at sampling time, under afore mentioned condition.

The signal source impedance connected to analog input needs to satisfy the following expression:

Figure 3-2 Simplified Sampling Diagram



0.69*(12+1)*Csamp*1.1*(Rsrc+Ron+Rref) < (1/Fclk)*3

Rref: The equivalent resistance value from the ADC input end.

Csamp: On chip sample and hold capacitance.

Ron: On chip 8 channels input resistance.

Rsrc: Signal source resistance.

Vsrc: Signal source voltage level.

Fclk: ADC clock (Fclk = Sample rate * 16)

3.5.1 High Speed Mode (1MSPS)

Csamp = 25.6pF

Fclk = 16MHz

Rref: 300Ω

Ron: 20Ω

0.69*(12+1)*Csamp*1.1*(Rsrc+Ron+Rref) < (1/Fclk)*3

→ Rsrc < 422Ω

3.5.2 Low Speed Mode (200KSPS)

Csamp = 25.6pF

Fclk = 3.2MHz

Rref: 300Ω

Ron: 20Ω

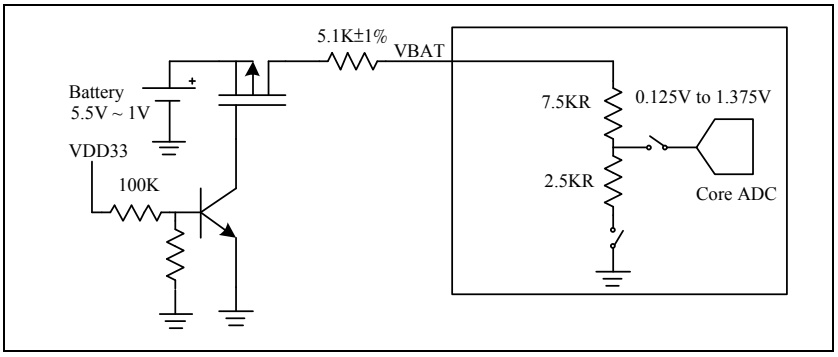
0.69*(12+1)*Csamp*1.1*(Rsrc+Ron+Rref) < (1/Fclk)*3

→ Rsrc < 2111Ω

3.5.3 Application Circuit for Battery Voltage Detection

Figure 3.4-1 is the battery voltage detection application circuit, the analog input is from V_{BAT} and the external discrete components are prevent battery leakage from V_{BAT} when system under power off states.

Figure 3.3 Battery Voltage Detection Application Circuit



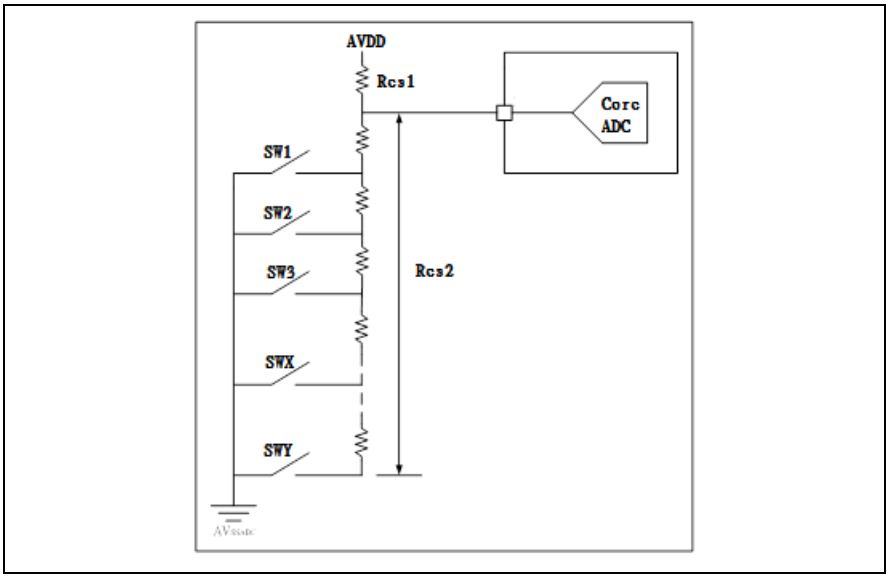
Note: This IP entails 10K resistance, so lengthy sampling time is needed.

3.5.4 Key Pad Scan

This signal designed for Key Pad Scan from A_2

The figure 3.4-3 is the key pads detection diagram.

Figure 3-3 Key Pads Detection Diagram



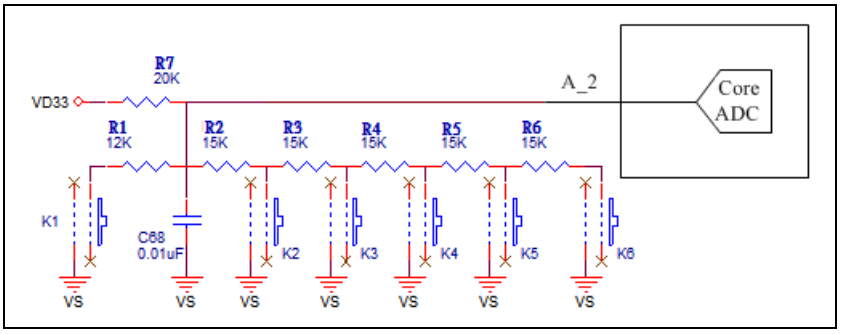
Note: If a user applies the keypad using this structure and meanwhile, he/she needs the interrupt

generator, please make sure Res1≦ 20Kohm and Res2＜ 5.6*Res1. Moreover a 0.01uF cap is recommended at A_2 on board.

If a user doesn't need the interrupt generator, please ignore the requirement for Res1 and Res2.

3.5.5 Application Circuit for Key Pad Scan

Figure 3-4 Key Pad Scan Application Circuit



A_2 = 0.825V When K1 + K2 switch be press.

A_2 = 0.99V When K1 + K3 switch be press.

A_2 = 1.0607V When K1 + K4 switch be press.

A_2 = 1.1V When K1 +K5 switch be press.

A_2 = 1.125V When K1 + S6 switch be press.

A_2 = 1.2375V When K1 switch be press.

A_2 = 1.4143V When K2 switch be press.

A_2 = 1.98V When K3 switch be press.

A_2 = 2.2846V When K4 switch be press.

A_2 = 2.475V When K5 switch be press.

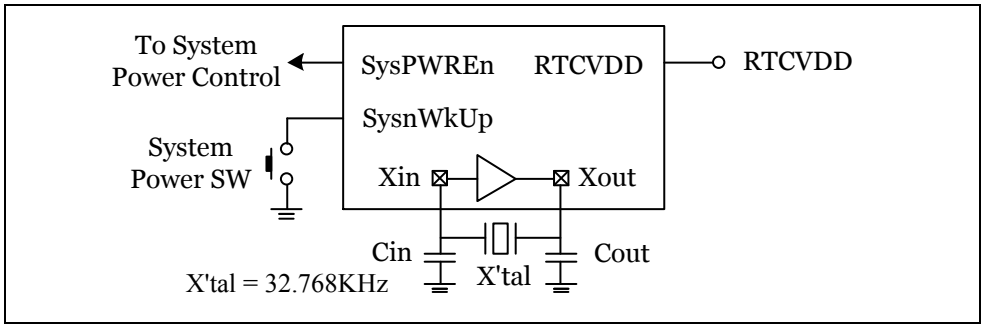
A_2 = 2.6053V When K6 switch be press.

4 RTC

NUC970 series is built-in a Real Time Clock (RTC) which is operated by the independent power supply while the system power is off. The RTC uses a 32.768 KHz external crystal.

This section will describe that design considerations related to the NUC970 RTC block.

Figure 4-1 RTC Internal Block



4.1 RTC Power Backup & Power Saving

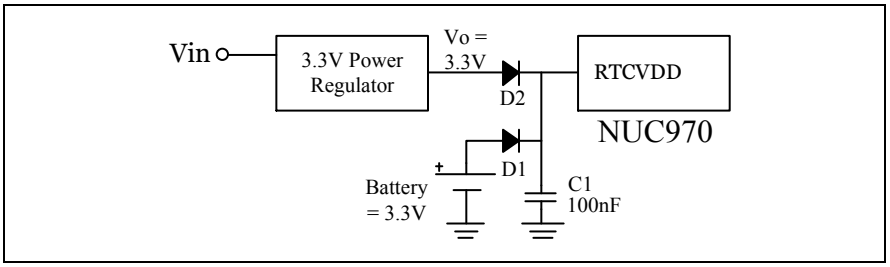
For some applications requiring operation with either an external power supply or a battery backup, it is recommend to implement with a simple diode OR circuitry as figure 4-2 shown below. The diode D1 prevents current from flowing into the CR2032 (3V) battery from LDO when the external power is supplied. Low forward voltage Schottky diodes are used to minimize the voltage dropout from the diode and ensure that the LDO output will be a little higher than CR2032 (3V). This solution can save CR2302 BAT power life time and provided proper powered to RTC_VDD.

When external power is removed and the voltage is dropping lower than VBAT, the CR2032 (3V) battery will start supplying power to NUC970.

To avoid RTC VDD power dropping causes RTC data loss by different power supply switching through diodes, at least place a 100nF capacitance to VBAT with C1.

The following shows the RTC backup power block diagram for design reference.

Figure 4-2 RTC Power Backup Block



4.2 RTC Power & Control Flow

Power On, when RTC_WKUP power key pressed to low, it will induce RTC_PWEN pin output high to enable external power chip.

If RTC_PWR_ON bit not be set =1 (IBR booting may not ready yet) that RTC_PWEN pin output will back to low when power key was released then system powered off.

If RTC PWR_ON bit be set =1 (IBR booting is successful) that RTC_PWEN can keep output high for enabling power on even if the power key be released or no pressing.

Power Off, while system with normal operation and power key is pressed again, RTC will get an interrupt for system. System program can follow this event to clear RTC_PWR_ON bit=0 that RTC_PWEN will output low soon to disable power chip let system turned off.

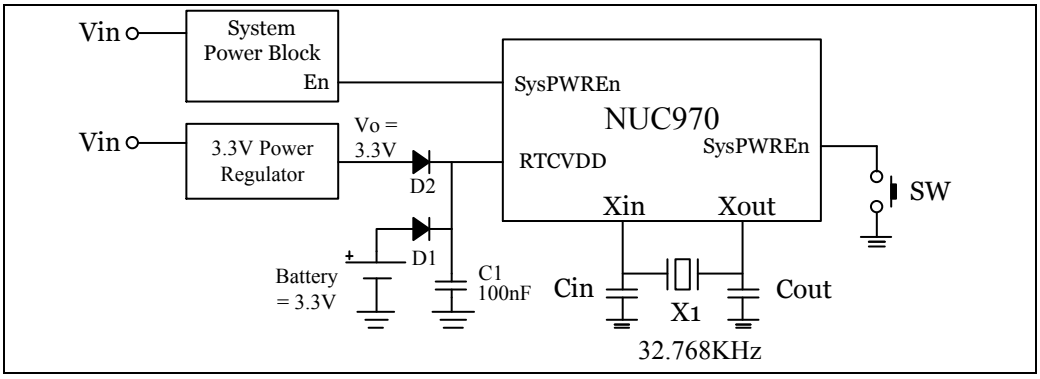
4.3 Force System Power OFF Control Flow

NUC970's RTC except for supporting a software power off function also supports a hardware automatic power off function like Notebook. For hardware power off function, it can be enable and disable in the RTC_PWRCTL's PWR_ON bit, or the user can presses the power button for a few seconds to force power off. The time to press power the button to power on/off could be configured in the PWRON and PWROFF of RTC_PWRCTL.

4.4 Reference Connections for Different Application

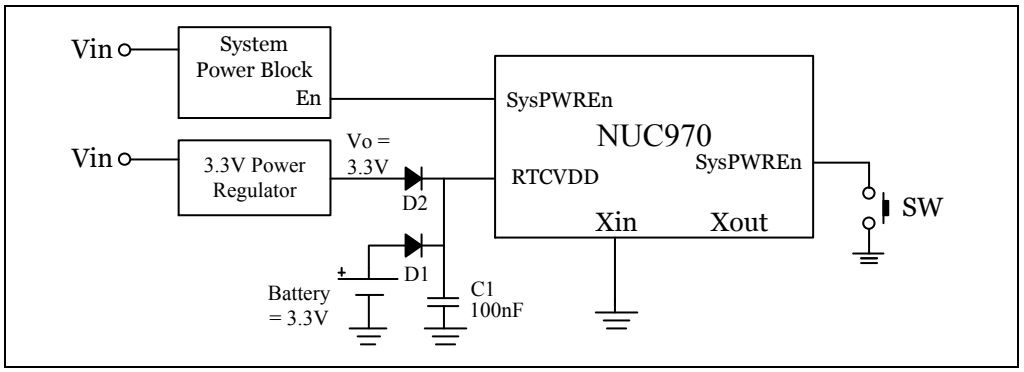
The typical connection of RTC block is as follow:

Figure 4-3 RTC Typical Application Circuitry



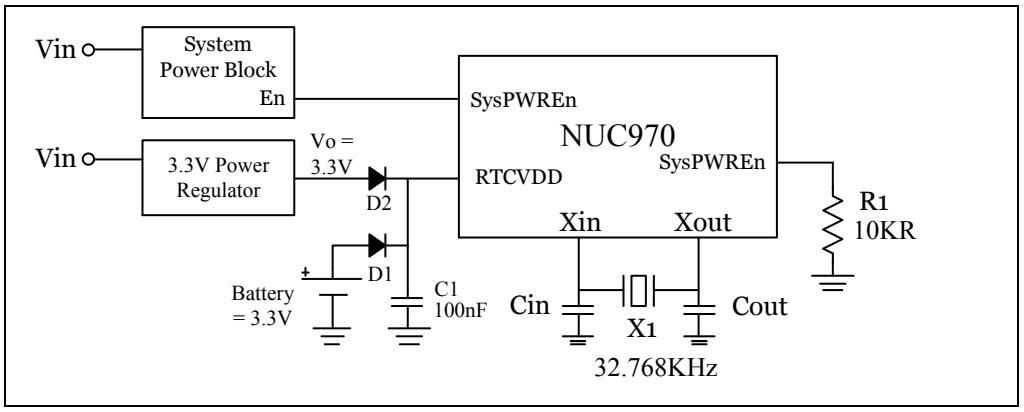
Sometimes, the sub-crystal (32.768KHz) is unnecessary for the some of application, the sub-crystal could be removed for saving cost. The figure is shown in detail as below:

Figure 4-4 RTC Power control without RTC crystal



In the hot pulg-in to power on system without power switch control for the system, the hardware designeer can remove the power switch and poull one 10KΩ to ground at the RTC_WkUp pin.

Figure 4-5 RTC Only Without Power CTL Method (1)



Note.

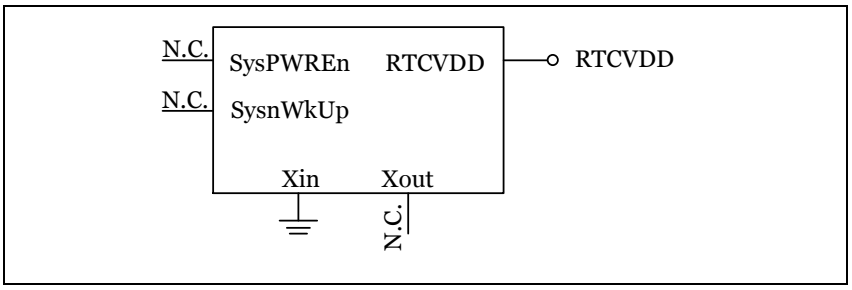
1. For RTC counter only, placed one R with 10K to RTC_WKUP then pull down to GND.

2. This application will have a penalty of leakage current by the R@10K pull down.

3. The bits of SW_PCLR and PWR_ON should be set in the control register of RTC_PWRCTL which to prevent RTC be forced off.

If the RTC isn't used in the system, the sub-crystal-in (Xin, 32.768KHz crystal) should be pulled to low, the SysPWREn and RTCVDD could be no connection. By the way, the RTCVDD should be tied to VDD33, too.

Figure 4-6 Without RTC Function



5 USB Bus

NUC970 integrated with two USB ports which 1st port (USB0) support with USB 1.1 /2.0 device and USB1.1/2.0 Host, the 2nd one (USB1) is only supported with USB2.0 Host.

USB host function compliant to Enhanced Host Controller Interface (EHCI) 1.0 specification to connect with USB 2.0 High-Speed (HS) device and compliant to Open Host Controller Interface (OHCI) 1.0 specification to connect with USB 1.1 Full-Speed (FS) and Low-Speed (LS) devices,

The following guidelines provide PCB design considerations, such as PCB stack up, component placement, routing concern etc.

5.1 USB Device

The USB device controller interfaces the AHB bus and the UTMI bus. It is compliant to USB Specification reversion 2.0. It supports USB Hi Speed performance up to 480Mbps.

The USB device controller interfaces the AHB bus and the UTMI bus. The USB controller contains both the AHB master interface and AHB slave interface. CPU programs the USB controller registers through the AHB slave interface. It is complaint with USB 2.0 specification and it contains 12 configurable endpoints in addition to control endpoint. In which the high speed performance up to 480Mbps.

5.1.1 High Speed USB Termination

To get a good signals quality and the Eye-Diagram waveform, the 90 Ω impedance for the DP/DM trace should be considerate when the PCB is routing. Normally, the resistor and capacitor need to be reserved on the DP/DM pin for impedance correction which should be closed to USB connector.

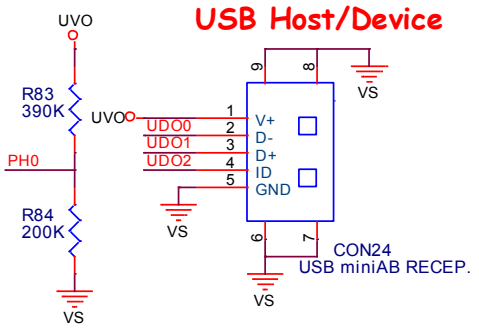
NUC970 USB device controller can get USB VBUS status or interrupt from the pin of USB_Det, when USB_Det is high it indicated VBUS status bit is 1, related reference design please see the Figure 5-1.

Power-On Setting Pin	Description	Power-On Setting Register Bit
USB0_ID	**USB Port 0 Role Selection** 0 = USB Port 0 act as a USB host. 1 = USB Port 0 act as a USB device.	PWRON[16]

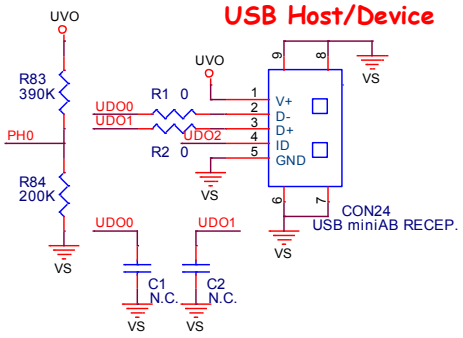
Register	Offset	R/W	Description	Reset Value
SYS_PWRON	SYS_BA+0x004	R/W	Power-On Setting Register	Undefined

[16]	**USBID**	**USB ID Pin Status** 0= USB port 0 used as a USB device. 1= USB port 0 used as a USB host.

Figure 5-1 Example of USB Device Connection



No reserving R/C component if impedance is matching.



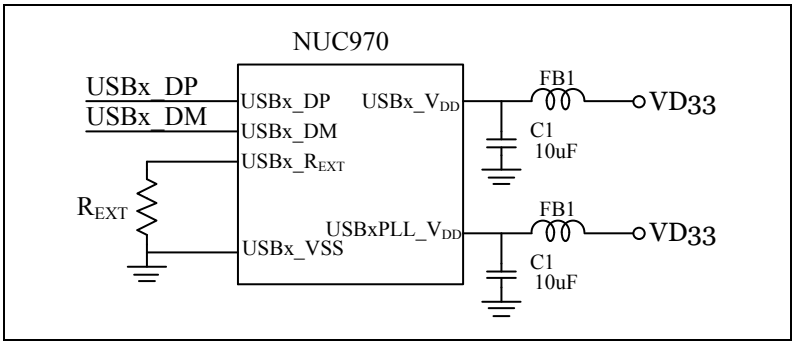
The value of R1/R2 and C1/C2 depends on the impedance matching.

5.1.2 REXT and USB Power

The REXT, an external resistor with precision 12.1K ohm ± 10%, to prevent any noise interference for the reference bias, the REXT which should be placed close to the pins of USBx_Rext and USB_VSS as figure 5.1-1 shown.

To get good USB signals quality, the PCB design also need take care of USB power and ground as the as the figure 5.1-1 shown the USBVDD33, USBVDD12 & USBVSS they be isolated with ferrite bead and 0 ohm resistor for reducing possible power noise from system.

Figure 5.1-1 Example of NUC970 USBVDD & REXT Connection



5.2 USB PCB Layout Guideline

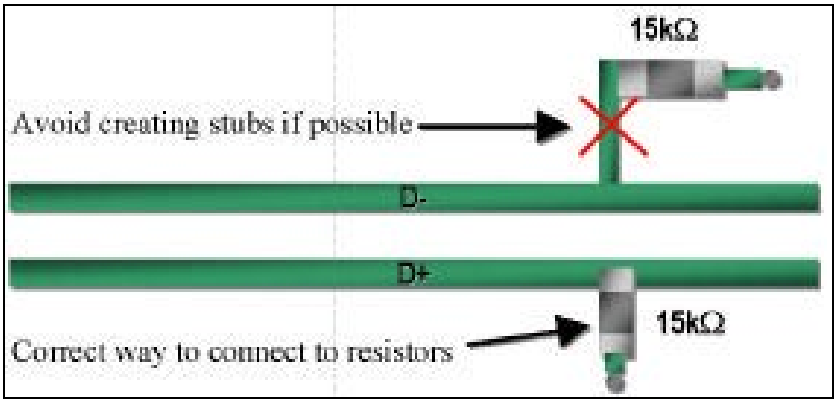
Traces the DP/DM to the connector, the signal swing during high-speed operation on the DP/DM line is relatively a small waveform about 400mV. So, if there is any differential noise picked up will effect transceiver signal on the pair traces. When the DP/DM traces are not shield, the traces behave like an antenna to pick up noise by the surrounding components.

To lower the interference effect:

shield Use the following general routing and placement guidelines when laying out a new design. These guidelines will help to minimize signal quality and EMI problems. The high speed USB validation efforts focused on a four-layer PCB where the first layer is a signal layer, the second layer is power, the third layer is ground and the fourth is a signal layer. This results in placing most of the routing on the fourth layer closest to the ground layer, and allowing a higher component density on the first layer.

1. DP/DM traces should be length matched and as close as possible to the connector.
2. Route DP/DM traces should be close together for noise rejection on the differential signals, parallel to each other and the length difference within 200-mil.
3. If the common chock is necessary, it should be as close as to the connector.
4. No extra components at DP/DM pair traces to maintain signal integrity.
5. No de-coupled caps on the DP/DM.
6. The characteristic of matching impedance 90Ω on the DP/DM is necessary.
7. Stubs on high speed USB signals should be avoided, as stubs will cause signal reflections and affect signal quality. If a stub is unavoidable in the design, no stub should be greater than 200 mils.

Figure 5-2 Avoid BUS Stubs



7. Route all traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces as much as practical. It is preferable to change layers to avoid crossing a plane split.

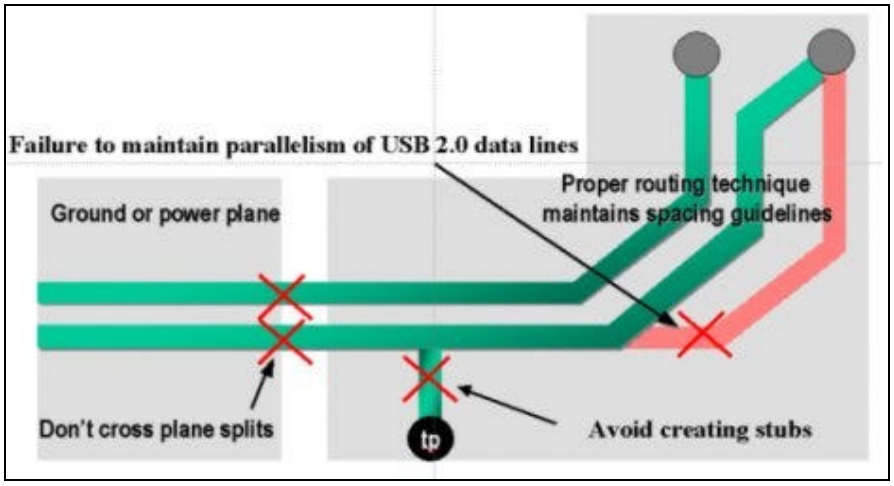
8. Use the following guidelines for the VCC OR GND plane.
   a. Traces should not cross anti-etch, for it greatly increases the return path for those signal traces. This applies to High Speed USB signals, high-speed clock and signal traces as well as slower signal traces, which might be coupling to them. USB signaling is not purely differential in all speeds (i.e. the FS Single Ended Zero is common mode)
   b. Avoid routing of USB signals within 25 mils of any anti-etch to avoid coupling to the next split or radiating from the edge of the PCB.

9. Separate signal traces into similar categories and route similar signal traces together (such as routing differential pairs together).

10. Keep high-speed USB signals clear of the core logic set. High current transients are produced during internal state transitions and can be very difficult to filter out.

11. Follow the 20*h thumb rule by keeping traces at least 20*(height above the plane) away from the edge of the plane (VCC or GND, depending on the plane the trace is over). For the suggested stack up the height above the plane are 4.5 mils. This calculates to a 90-mil spacing requirement from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.

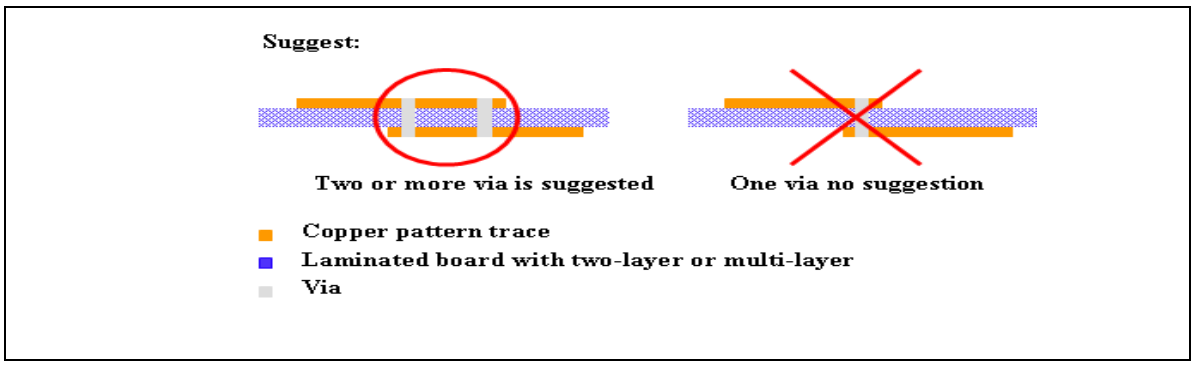
Figure 5-3 Maintain Parallelism USB BUS



5.2.1 Through Hole Consideration for D+ and D-

For the two-layer or multi-layer of PCB, when the signals of D+ and D- need to be through another layer, in which the resistively of through hole should be concerned. To lower the resistively issue for the sensitivity case, the two-via or multi-via should be adapted, as shown in the following figure.

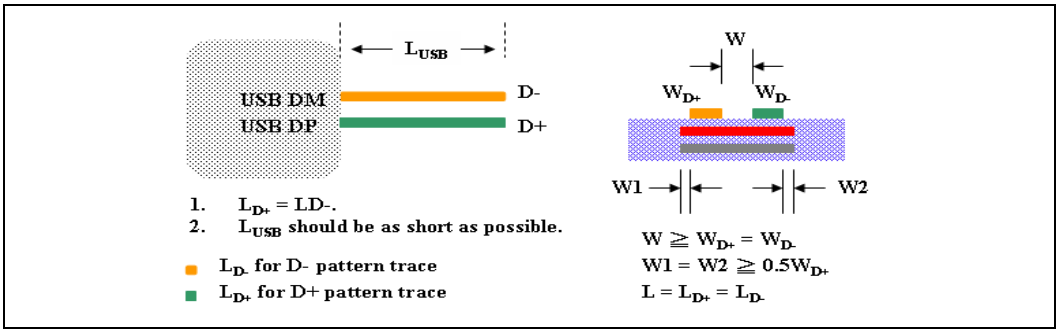
Figure 5-4 Through Hole for D+ and D-



5.2.2 Signal Trace for D+ and D-

To avoid the trace effect signal for the eye diagram, the trace length should be almost the same of D+ and D-. Then, the characteristic impedance should be a symmetrical path for the differential end of the USB port. The characteristic impedance should be 50 Ω for full speed USB1.1. For reducing the trace length, the USB terminal should be as close as the USB port of NUC970 series MPUs.

Figure 5-5 Signal Trace for D+ and D-



5.2.3 High Speed USB Trace Spacing

Below figure provides an illustration of the recommended trace spacing for multi-layer and 2-layer PCB. Please use the following separation guidelines to your design.

1. Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90ohms differential impedance. Deviations will normally occur due to package breakout and routing to connector pins. Just ensure the amount and length of the deviation is kept to the minimum possible.
2. Use an impedance calculator to determine the trace width and spacing required for the specific board stack up being used. For the board stack up parameters referred to in Layer Stacking, 7.5-mil traces with 7.5-mil spacing results in approximately 90 ohms differential trace impedance.
3. Minimize the length of high-speed clock and periodic signal traces that run parallel to high speed USB signal lines, to minimize crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50 mils.
4. Based on simulation data, use 20-mil minimum spacing between high-speed USB signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.
5. If PCB is 2-layer design, for signals quality request that USB signal pairs should have GND plane closely to traces side for shielding as the illustration of figure 6.3-6

Figure 5-6 Multi-Layer PCB USB Bus Trace Space Recommendation

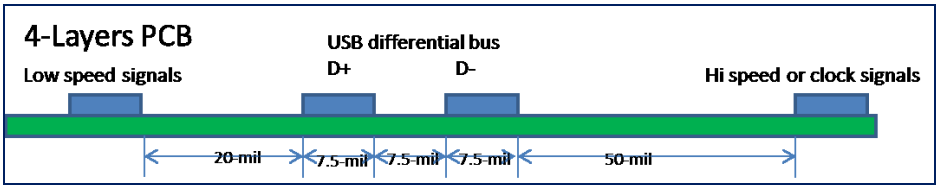
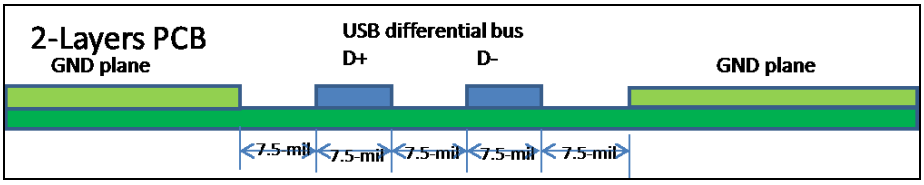


Figure 5-7 Layer PCB USB Bus Trace Space Recommendation



5.2.4 High Speed USB Trace Length Matching

Use the following trace length matching guidelines.

High-Speed USB signal pair traces should be trace-length matched. Max trace-length mismatch between High-Speed USB signal pairs (such DM0 and DP0) should be no greater than 150 mils.

5.2.5 High Speed USB Trace Length Guidelines

Use the following trace length guidelines.

Main board's USB signal pairs total trace length should be less than or equal 18 inches.

5.2.6 Layout Stacking

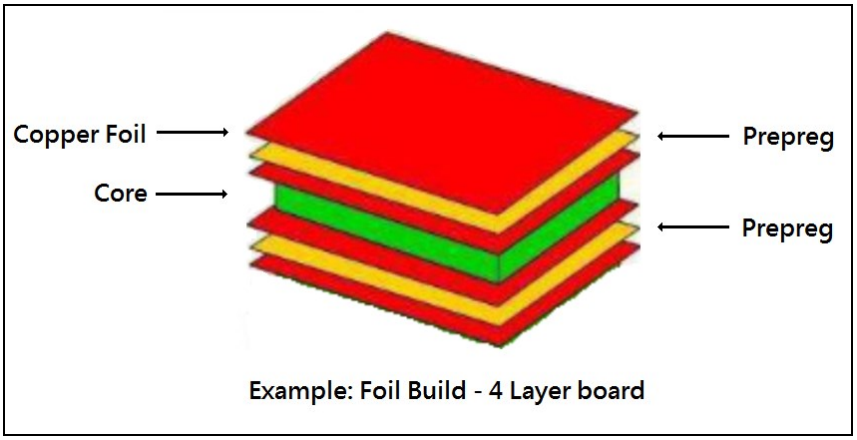
The following guidelines apply to PCB stack-up reference.

4-Layer Stack-Up
1. Signal 1 (top)
2. VCC
3. GND
4. Signal 2 (bottom)

The high speed USB validation PCB used 7.5-mil traces with 7.5-mil spacing between differential pairs to obtain 90 Ohm differential impedance. The PCB specific board stack up used is as follows:

- 1 oz. copper
- Prepreg @4.5 mils
- Core @53 mils
- Board thickness @ 63 mils (1.6mm)
- FR4

Figure 5-8 4-Layer PCB structures



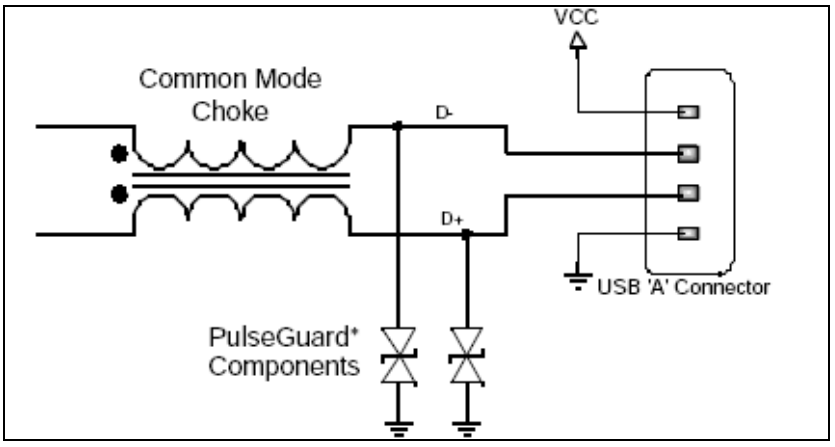
5.2.7 EMI/ESD Considerations

The following guidelines apply to the selection and placement of common mode chokes and ESD protection devices.

5.2.8 EMI - Common Mode Chokes

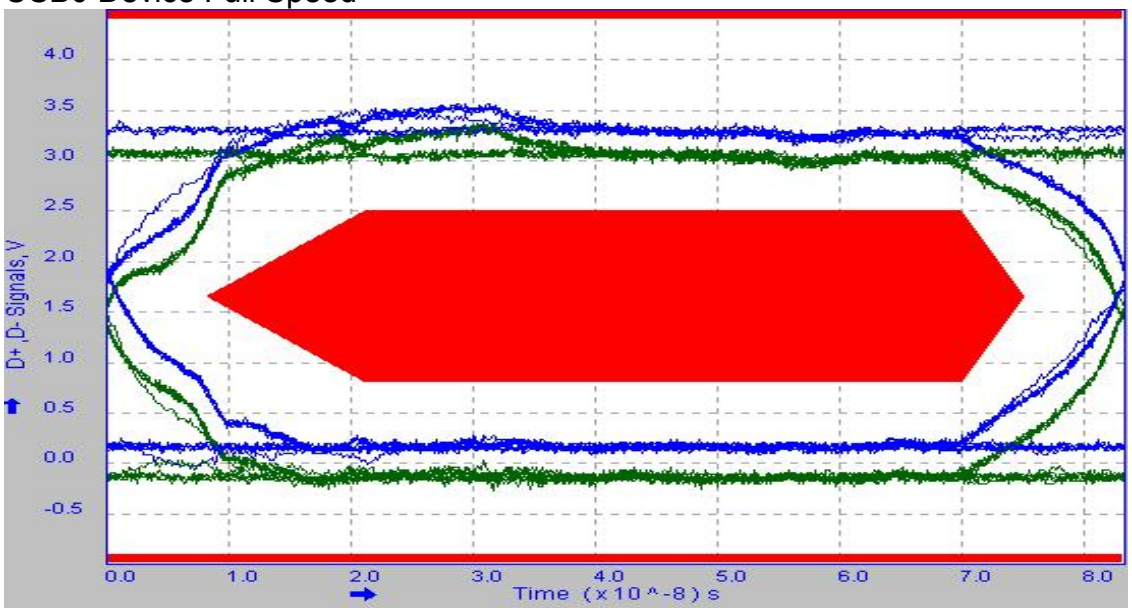
Testing has shown that common mode chokes can provide required noise attenuation. A design may include a common mode choke footprint to provide a stuffing option in the event the choke is needed to pass EMI testing. Below figure shows the schematic of a typical common mode choke and ESD suppression components. The choke should be placed as close as possible to the USB connector signal pins.

Figure 5-9 Common mode choke

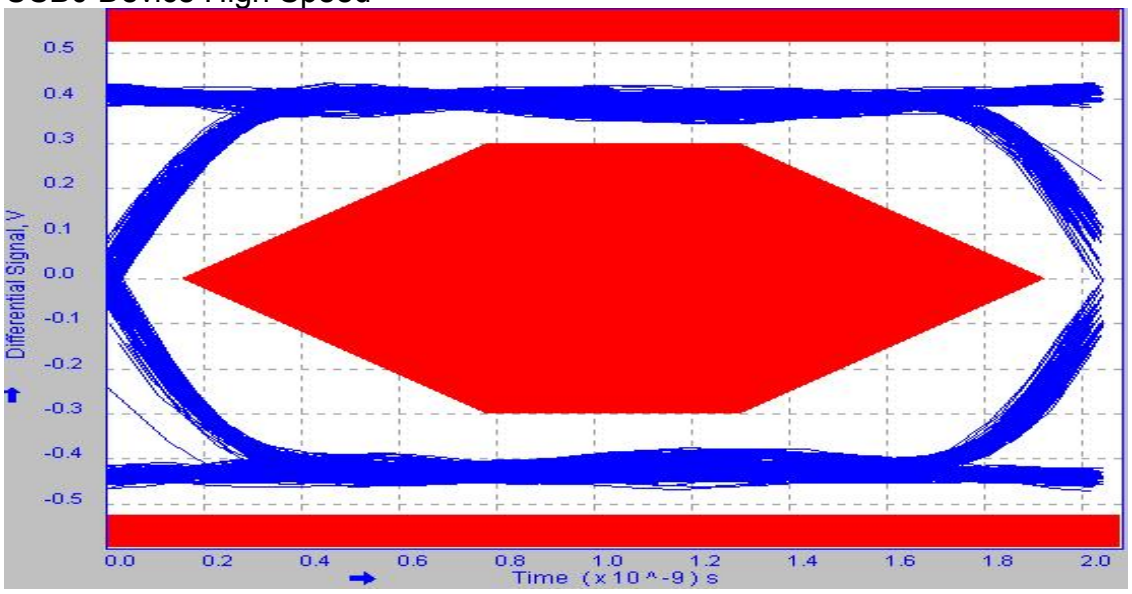


Examples of specific common mode chokes that were tested for signal quality and EMI with passing results are given in Table. Other vendors make similar parts that may provide the same results but due to limited time and resources they were not tested.

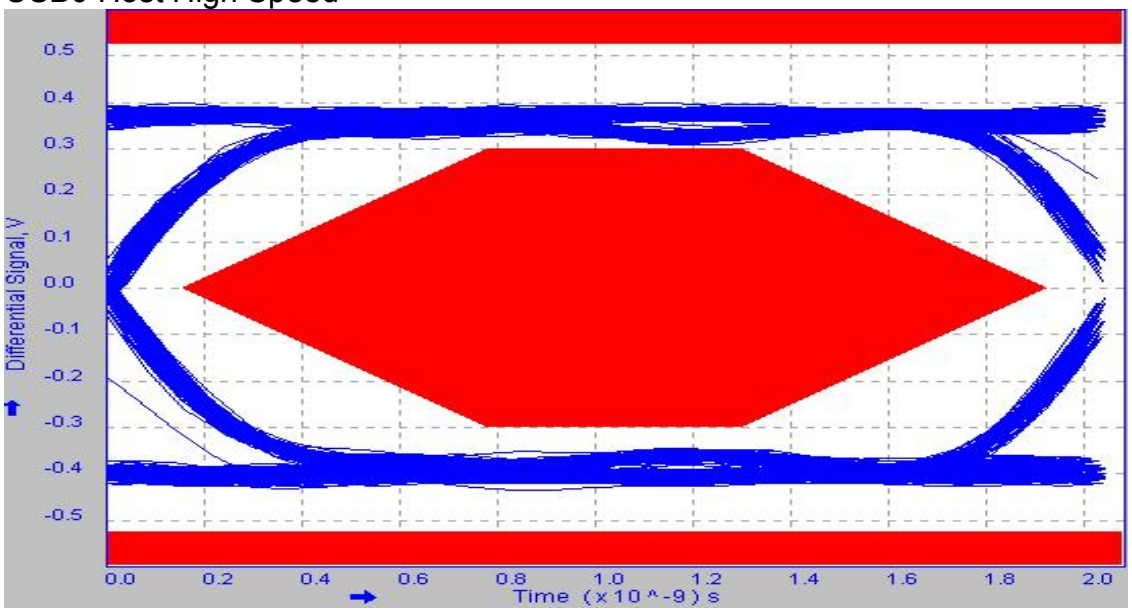
USB0 Device Full Speed



USB0 Device High Speed



USB0 Host High Speed



USB1 Host High Speed

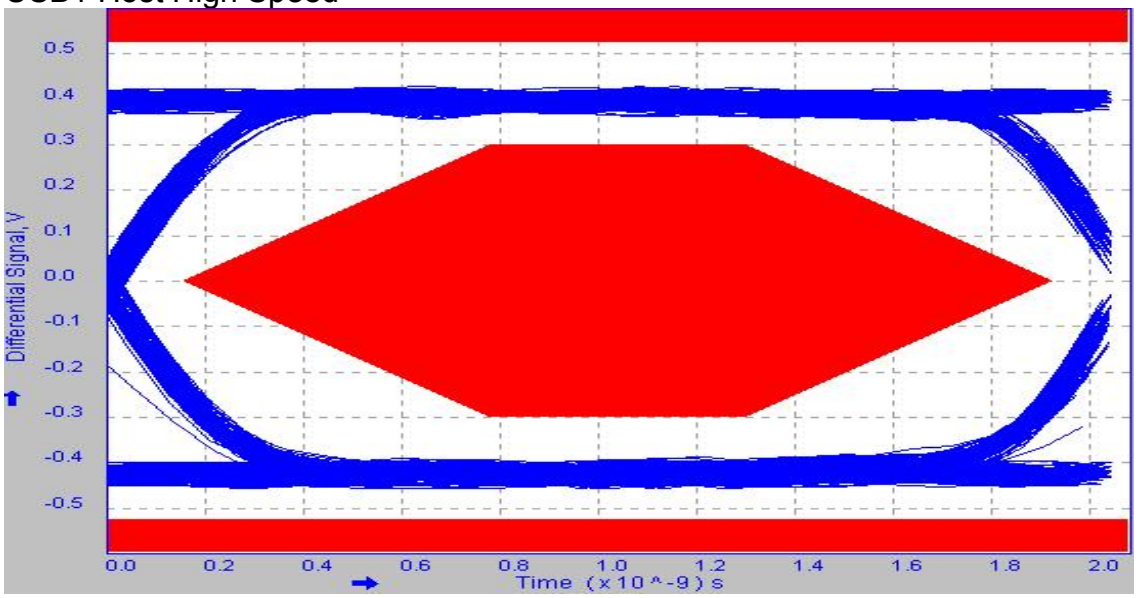


Figure 5-10 USB High Speed Eye-Diagram

The eye diagram above shows high speed signal quality, as the common mode impedance increases, this distortion will increase, so you should test the effects of the common mode choke on full speed and high-speed signal quality.
Finding a common mode choke that meets the designer's needs is a two-step process.
1. A part must be chosen with the impedance value that provides the required noise attenuation. This is a function of the electrical and mechanical characteristics of the part chosen, and the frequency and strength of the noise present on the USB traces

that the designer is trying to suppress.
2. Once the designer has a part that gives passing EMI results, the second step is to test the effect this part has on signal quality. Higher impedance common mode chokes generally have a greater damaging effect on signal quality, so be careful about increasing the impedance without doing thorough testing.
Thorough testing means that the signal quality must be checked for Low speed, Full speed and High speed USB operation.

5.2.9 ESD

Low-speed and full-speed USB provide ESD suppression using in-line ferrites and capacitors that formed a low pass filter. This technique doesn't work for high speed USB due to the much higher signal rate of HS data.
A device that has been tested successfully is based on spark gap technology. The specific device tested is a Little-Fuse component, Pulse-Guard* PGB0010603 (0603 package size). Proper placement of the device is on the data lines between the common mode choke and the USB connector data pins as shown in above Common mode choke figure. Other low-capacitance ESD protection devices may work as well.
As with the common mode choke solution, we recommend including the footprints for this device, or some other proven solution, as a stuffing option in case it is needed to pass ESD testing.
ESD protection and common mode chokes are only needed if the design does not pass EMI or ESD testing. Footprints for common mode chokes and/or ESD suppression components should be included in the event that a problem occurs (General routing and placement guidelines should be followed).

6 Ether Net PHY & RJ45 port layout note:

- Make a Stable & Low-Noise environment for Ether Net PHY working
- Make a better circuit for Ether Net PHY by simplifying signal trace
- Reduce EMI & EMC
- Make better ESD protecting

6.1 Placement

Block A and B may be better placed as close to magnetic as possible. Let the trace between ETHERNET PHY and magnetic as short as possible, and keep the Tx+/-(So as Rx+/-) signal traces to be symmetry. The traces should not be too long and 12cm will be the maximum of path's length. When Tx, ETHER NET PHY will sink current from Block A (When Auto-MDIX working, Tx<->Rx direction switch). When Rx, ETHER NET PHY will take differential voltage signal from Block B

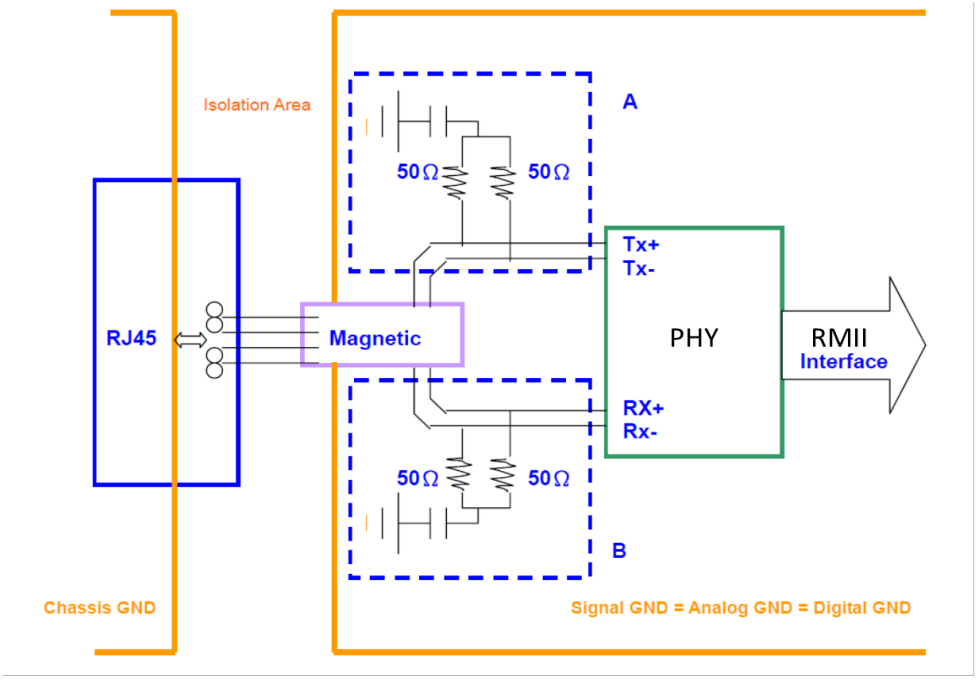
(When Auto-MDIX working, Rx<->Tx direction switch). Besides, the distance between RJ-45 and magnetic should be as short as possible. If these 2 requirements couldn't be met at the same time, the distance between ETHERNET PHY and transformer might be scarified to keep the distance between RJ-45 and magnetic as short as possible.

A).The termination resistors (50Ω in block A & B) may be better placed as close to magnetic as possible. For better impedance matching, the termination resistors and caps should pay more attention to take care.

B).ISET of ETHER NET PHY (pin28) should be placed as close to ETHERNET PHY as possible. Furthermore, it should not be affected by other signals such as TX+/-, RX+/- and clock signal traces.

C).Crystal shouldn't be placed close to: Input /Output ports, edge of PCB board and magnetic devices. The most important thing is that crystal should not be placed close to high-frequency devices or traces, such as MII interface signals, Tx+/-, Rx+/- and Power signals.

D).High current on the trace will induce the higher EMI noise, so it will be better to reduce the trace length to the power source when we placing the high current devices. The magnetic device with magnetic field should be separated (Isolation) and mounted at 90° to each other.



6.2 Power and Ground

It is better that do not try to partition GND at all.

A).Never use right angle for all partition on power plane or GND plane, so as each signal trace should be.

B).No power and GND planes can be underneath the isolated area for the RJ-45 connector and magnetic. Also RJ-45 connector has its isolated GND (Chassis GND) to connect to RJ-45's case.

C).Try to keep the GND plane as large as possible, and do not partition the GND plane for good GND return path.

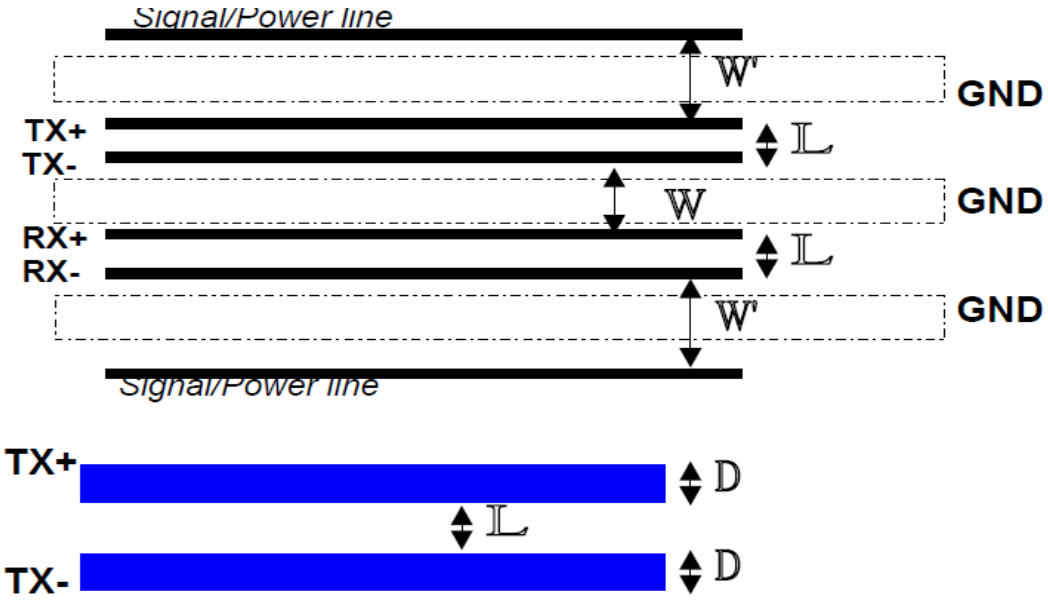
6.3 Trace Routing

To reduce the propagation delay, frequency noise, cross-talk and improve the signal quality that ETHER NET PHY received, and reduce the loss from transmit signals.

6.3.1 Avoid right angle signal trace:

6.3.2 For Tx+/−, Rx+/− traces:

- Avoid signal noise or loss on these traces.
- Tx+ & Tx- should be equal length to each other.
- Rx+ & Rx- should be equal length to each other.
- The line width and distance between Tx+/− and Rx+/−



Note.

D: Line width is as wide as possible in the range of (6mil ~ 12 mil), ex: 8mil.
L: Width between differential pair should be small, ex: 4mil.
W: Isolation width between TX+/- and RX+/- is as wide as possible, ex: 30mil. GND used as isolation is recommended.
W': Isolation width between TX/RX and noisy signal/power is as wide as possible, ex: 30mil. GND used as isolation is recommended.

6.3.3 For W & W' need better isolation, ex: shielding with GND.

Try to avoid via for TX+/-, RX+/- traces. Via will degrade signal quality.
Try to avoid digital signals (like Clocks or MII signal traces) interfere with analog signals (like Tx+/-, Rx+/-, or ISET [Pin28] traces) and power lines.

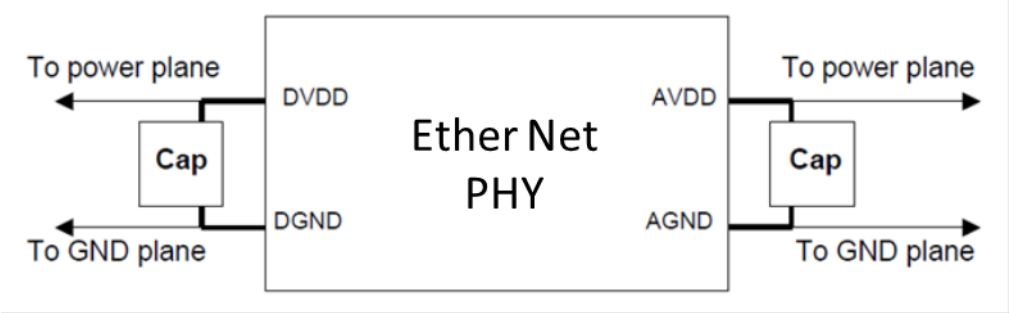
6.3.4 Never running noisy digital signals in parallel with TX+/- and RX+/-.

The traces of power, ground, and those need de-couple cap should be shorter and wider. If vias are not eliminated on the trace for de-couple cap, try to enlarge the diameter of these vias.

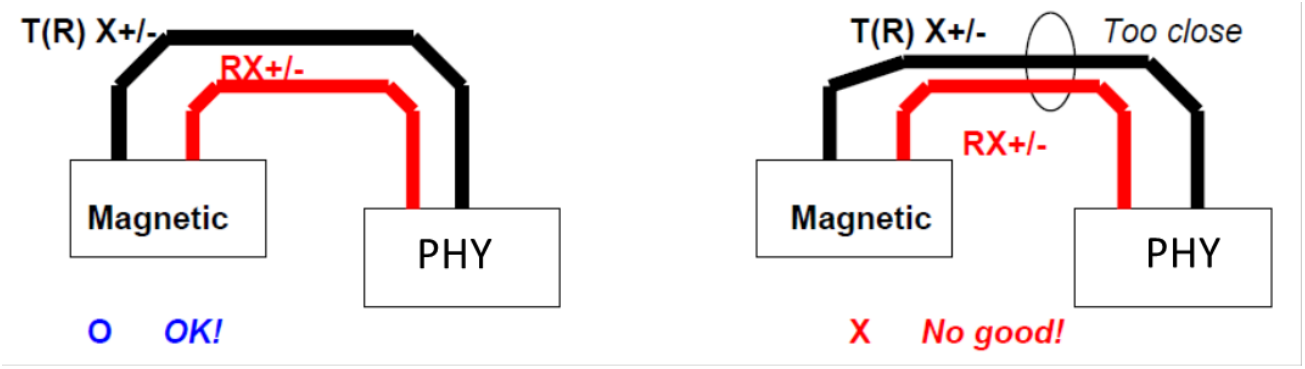
A) For some critical signals, clock and the other high speed signal traces should be as short and wide as possible. (Surely that is compared with normal signal traces.) And it's better having the GND plane under them, and it is even better with the GND plane around it.

B) The length of each signal trace shouldn't exceed 1/20 of the highest harmonic wavelength. For example, for the 25M clock trace shouldn't exceed 30cm and for the 125M signal trace shouldn't exceed 12cm (Tx+/-, Rx+/-).

C) De-couple cap should be placed as close to IC as possible, and the traces should be short. Every ETHERNET PHY analog/digital power needs de-couple cap and keeps the analog power close to analog GND pin, digital power close to digital GND pin. (See the diagram below)



Try to keep the distance between Tx+/- & Rx+/- differential pairs for good isolation. When these two pair of traces runs together in parallel, don't place them too close for unwanted interference. Shielding by GND planes can get a better isolation to these two differential pairs.



A) The signal trace length difference between Tx+ and Tx- (Same as Rx+ and Rx-) should be kept as small as possible, better within 1 inch.

B) Ferrite Beads should be as close to IC pins and let it on the rating of 100Ω@100MHz. The ferrite bead between DVDD and AVDD of ETHERNET PHY pins should be placed as close to ETHERNET PHY as possible, and at the same side as ETHERNET PHY, not opposite side.

C) The ferrite bead between REGOUT and REGIN of ETHERNET PHY pins should be placed as close to ETHERNET PHY as possible, and at the same side as ETHERNET PHY, not opposite side.

D) Magnetic: Any Magnetic with Tx/Rx turn ration of 1:1/1:1 are suitable for IP101, such as SINKA LS518/LS502, Bothhand TS8121C/TS6121C. Transformer supports Automdix function is recommended for better EMI performance.

6.4 Better Analog Performance

A) When using regulator such as 5V to be 3.3V, the rated current of the regulator should be at least 300mA.

B) Both Analog GND pins and Digital GND pins must maintain a good GND return path (One GND plane is recommended. Avoid using single ended GND or making the GND plane discrete. Keep the circuit's return path back to the system's real GND as short as possible. This is especially important for 2 layers PCB layout.

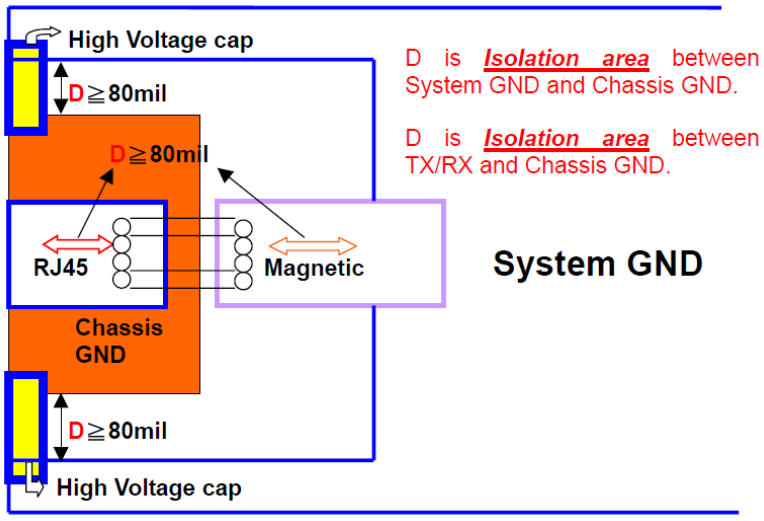
C) When using 25MHz crystal as ETHERNET PHY's clock source, the spec of crystal is under 50ppm better. Two caps attached to X1 and X2 should be close to 20pf.

D) Avoid placing cap in the clock path when using oscillator as clock source.

E) If EMI of the system couldn't pass, add some de-couple caps (such as 0.1uf, 10nf, 1nf, 390pf.., etc.) between systems Power to GND.

6.5 ESD Protecting

For ESD protection, we suggest to keep a distance at least 80mil for good isolation, which avoid ESD energy jumping by traces nearby IC. (See the diagram below)



7 NUC970 B ver. Limitation Notification

By NUC970 B version design issue, there are the following limitations please follow the engineering change order (ECO) application notes to stable that functions to system.

Issue-1, NUC970 B version has random power up failure issue that is power-on latch miss by a little probability when powered is directly. This issue can be avoided with NUC970 power-on/off control by RTC_WKUP & RTC_PWREN signals.

If powered-on/off directly still is necessary by system design demand, Nuvoton provided applicable solutions for reference, about the detail please refer to the application note of "NUC970B Application CKT for Random Power up Fail Issue_EN.pdf".

Issue-2, NUC970 B version RTC internal reset function may enter unknown state when core power is not ready yet. If this issue occurred that RTC_WKUP & RTC_PWREN will be out of control and caused system powered break down.
For preventing the symptom occurrence, please refer to the application note of "NUC970 RTC application CKT.pdf" to add proper circuitry for RTC power control design.

8 Reference Design

This section shows the whole chip reference design circuit which is the same as the NUC970 development board.

Figure 8-1 NUC972 Development Board Schematic Block Diagram

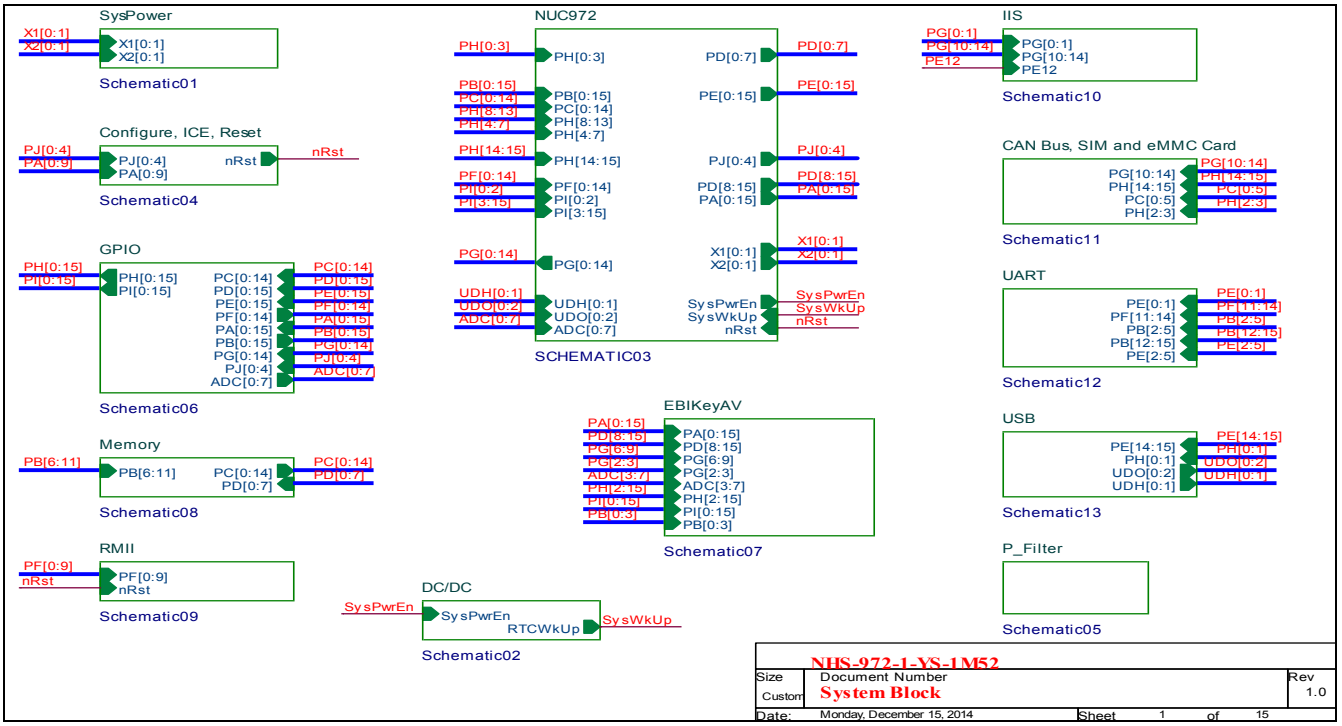


Figure 8-2 Power Input, Crystal

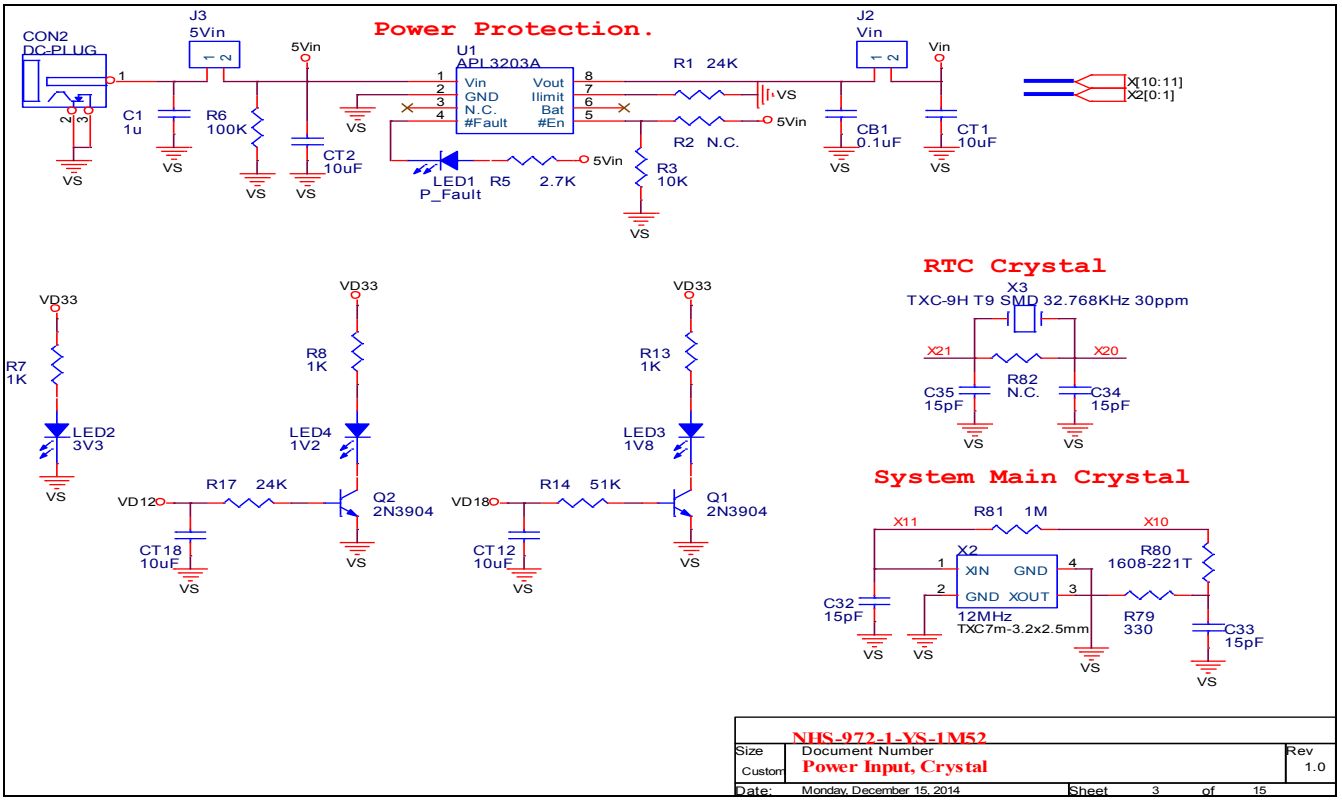


Figure 8-3 System Power

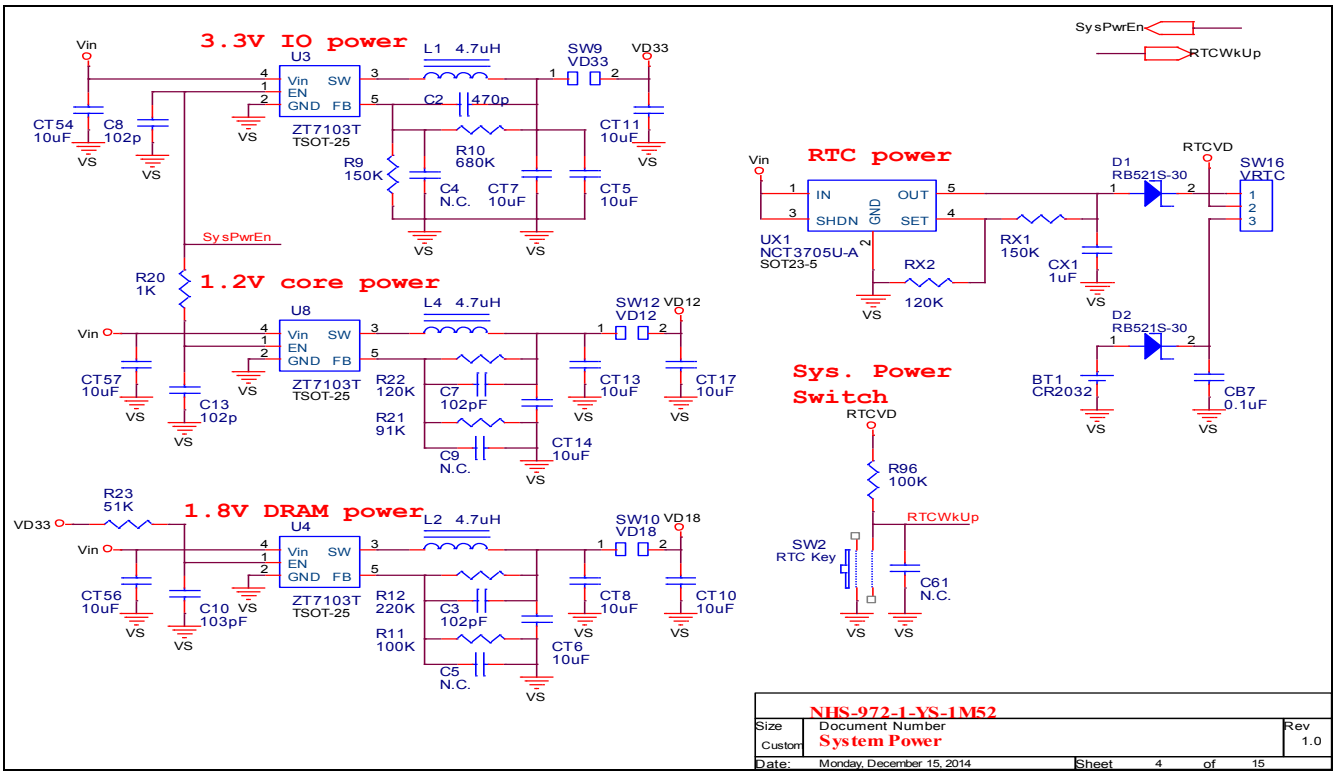


Figure 8-4 NUC970

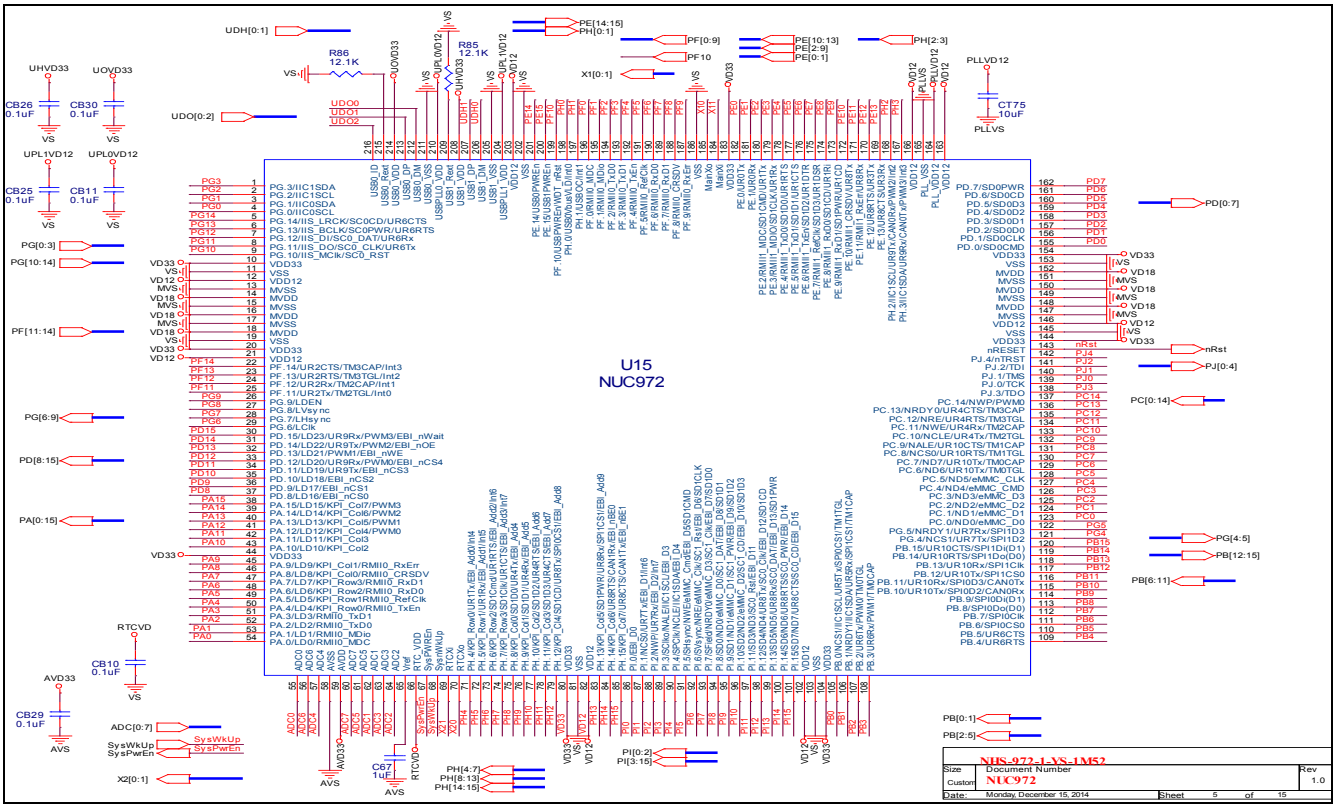
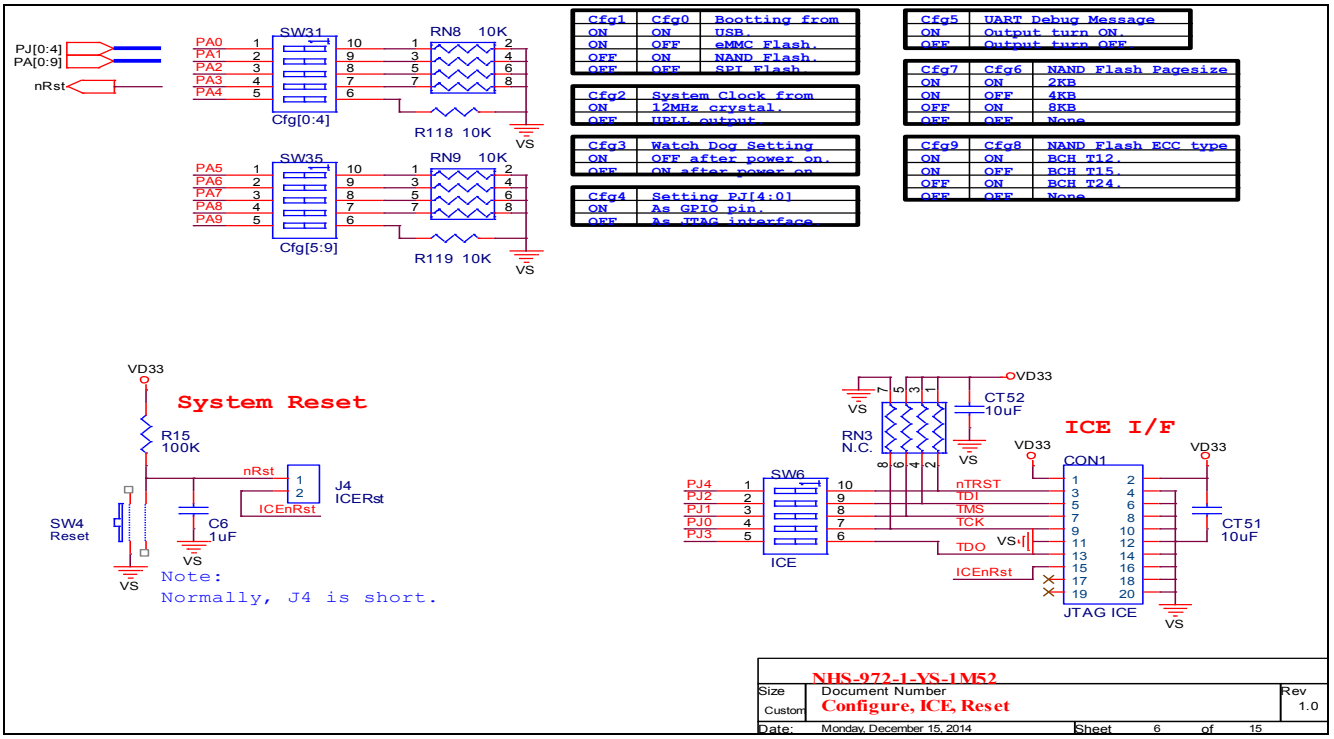


Figure 8-5 Configure, ICE, Reset



Cfg1	Cfg0	Bootting from
ON	ON	USB.
ON	OFF	eMMC Flash.
OFF	ON	NAND Flash.
OFF	OFF	SPI Flash.

Cfg2	System Clock from
ON	12MHz crystal.
OFF	UPLL output.

Cfg3	Watch Dog Setting
ON	OFF after power on.
OFF	ON after power on.

Cfg4	Setting PJ[4:0]
ON	As GPIO pin.
OFF	As JTAG interface.

Cfg5	UART Debug Message
ON	Output turn ON.
OFF	Output turn OFF.

Cfg7	Cfg6	NAND Flash Pagesize
ON	ON	2KB
ON	OFF	4KB
OFF	ON	8KB
OFF	OFF	None

Cfg9	Cfg8	NAND Flash ECC type
ON	ON	BCH T12.
ON	OFF	BCH T15.
OFF	ON	BCH T24.
OFF	OFF	None

Figure 8-6 Power Filter

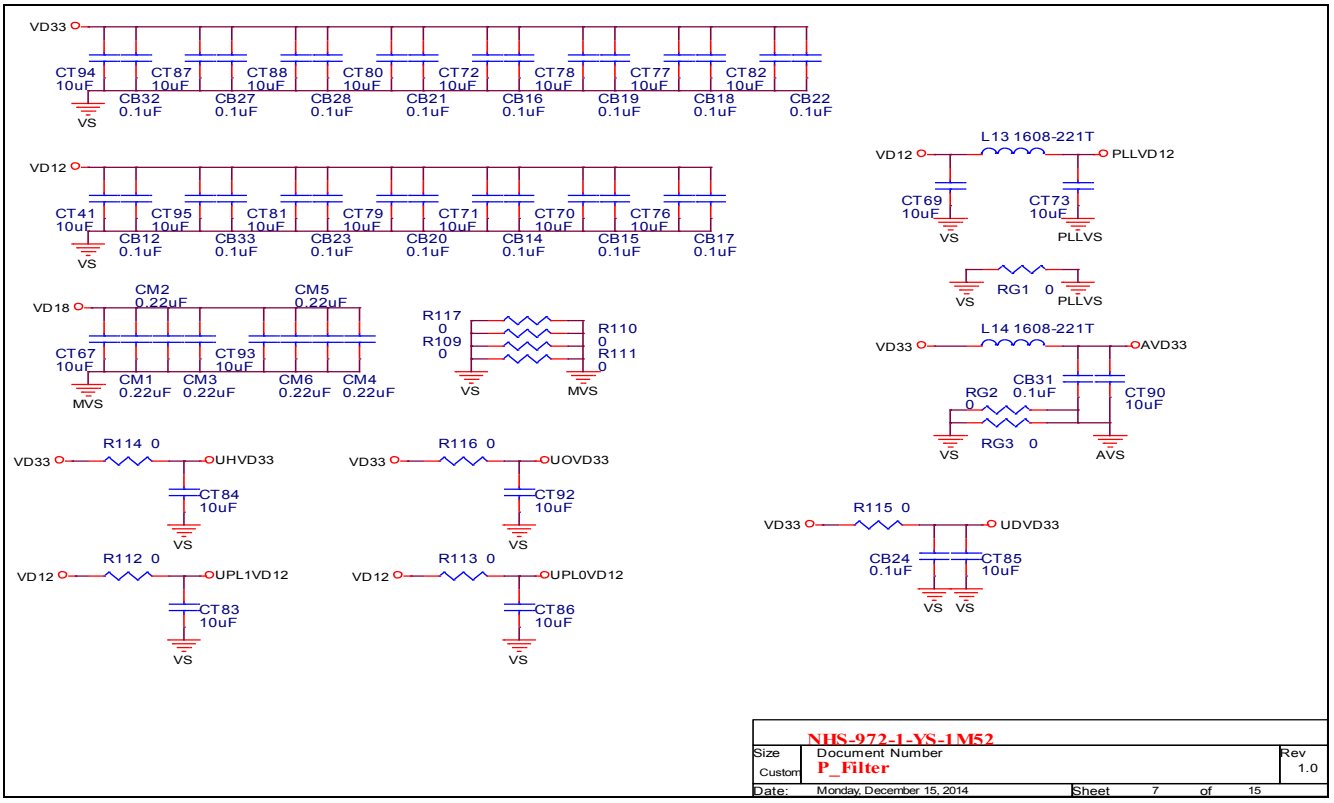


Figure 8-7 GPIO

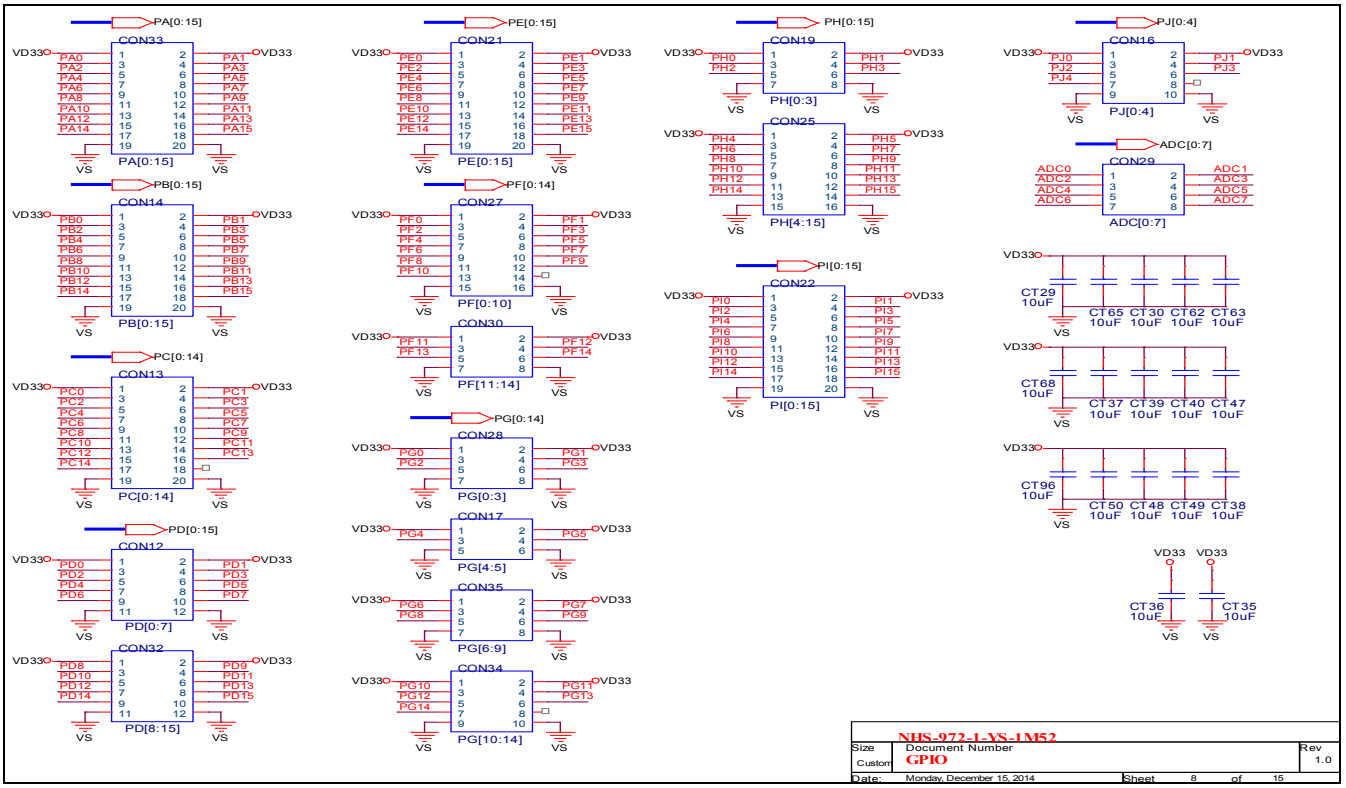


Figure 8-8 EBI, Keypad, LCD and CMOS sensor

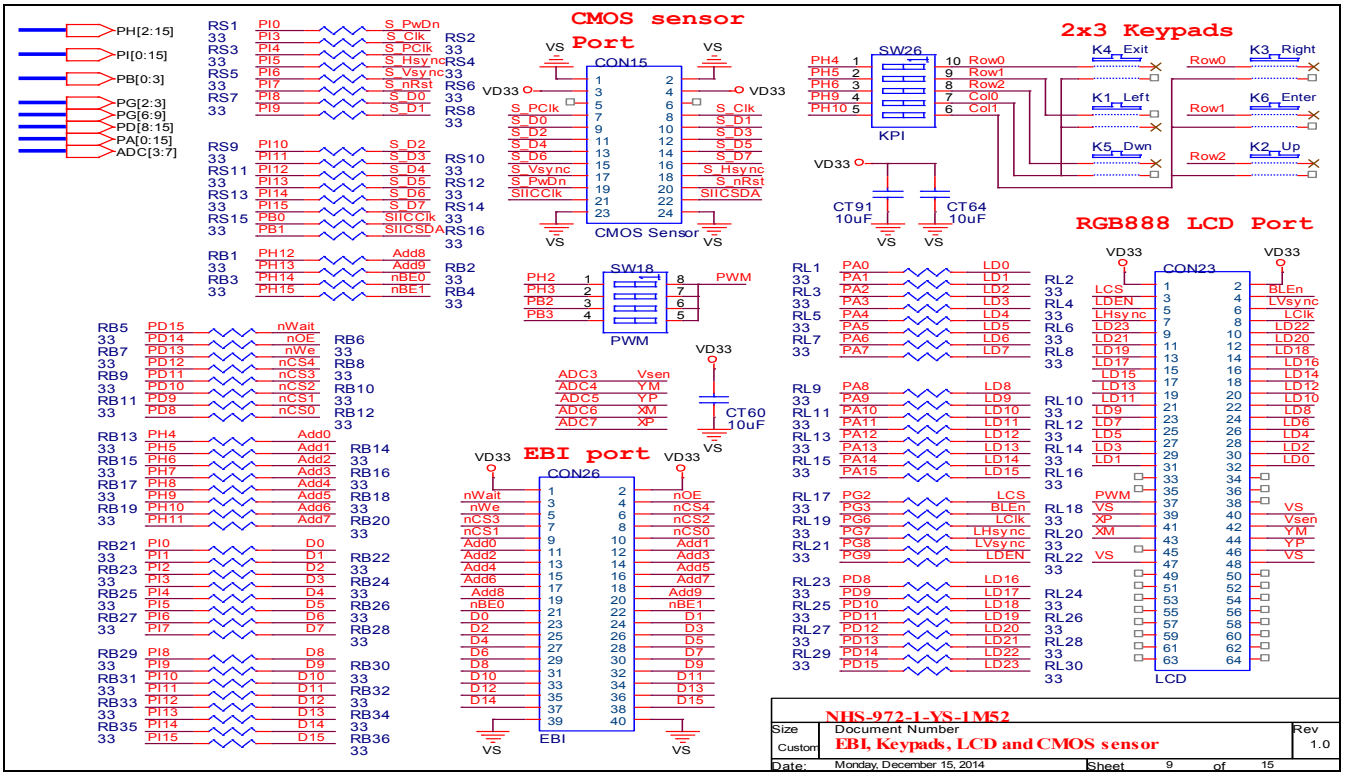


Figure 8-9 Memory

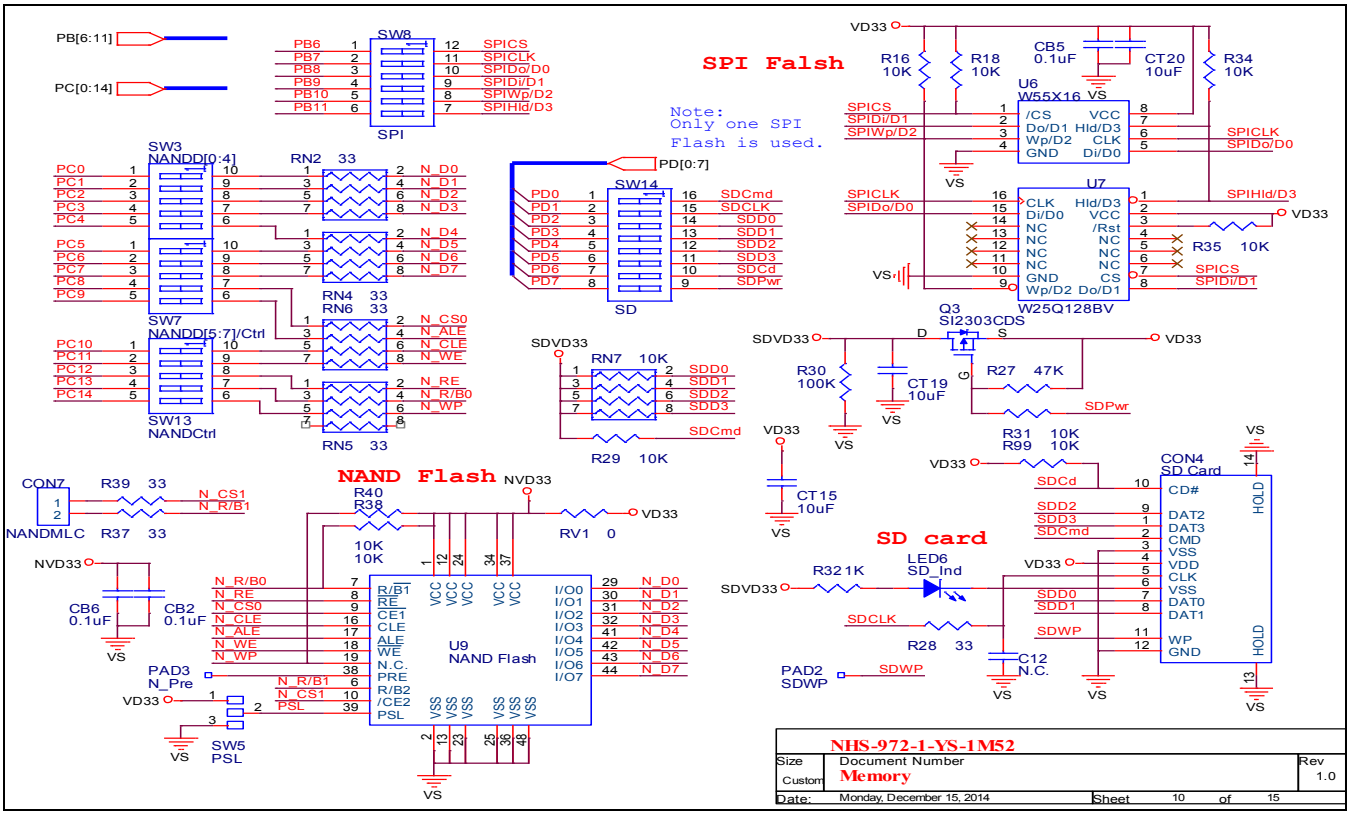


Figure 8-10 Ethernet

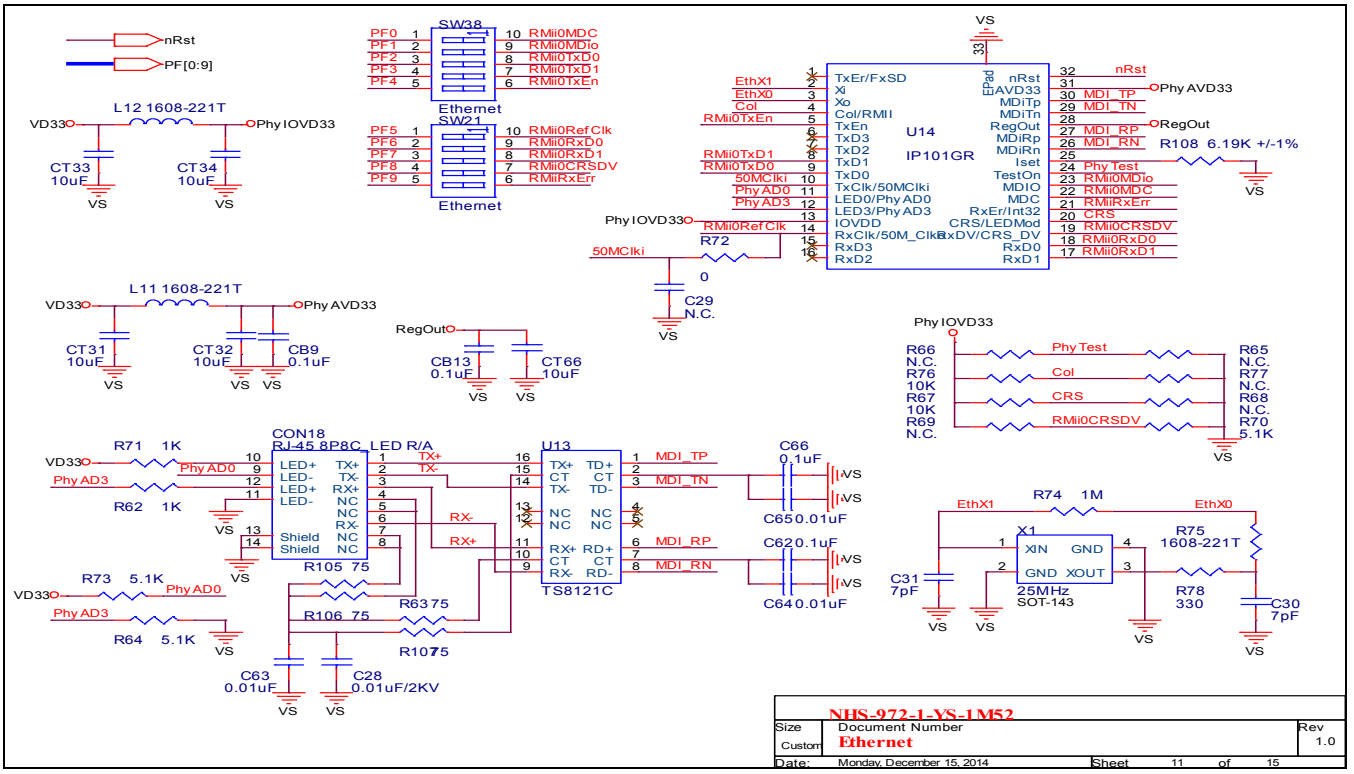


Figure 8-11 IIS

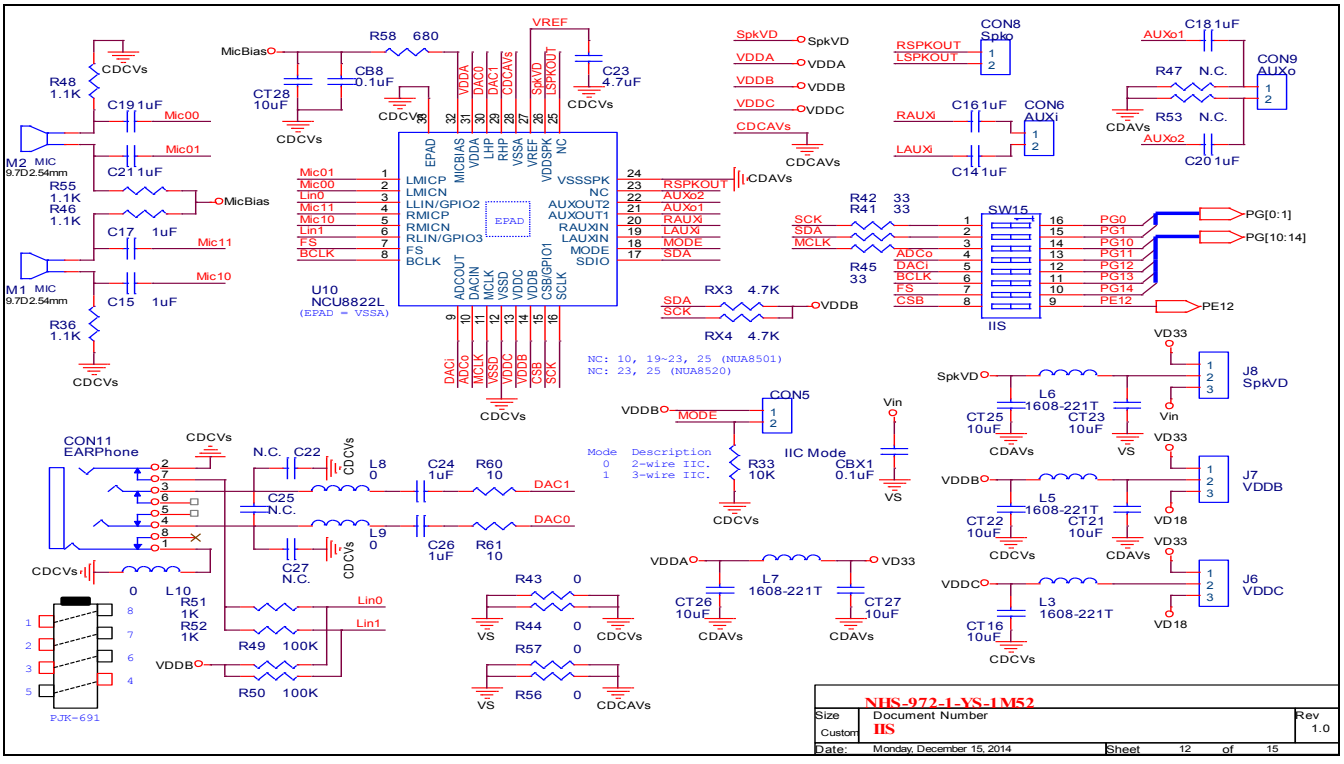


Figure 8-12 CAN Bus, SIM and eMMC card

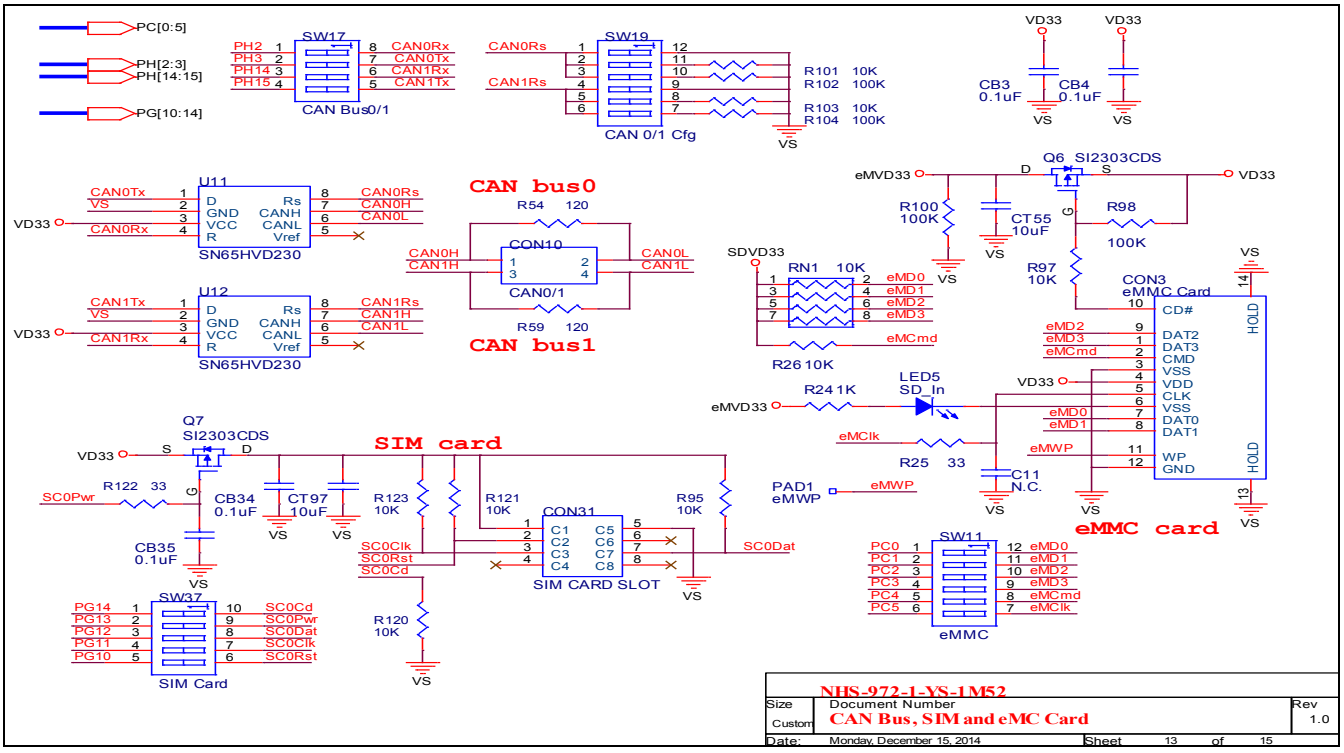


Figure 8-13 UART

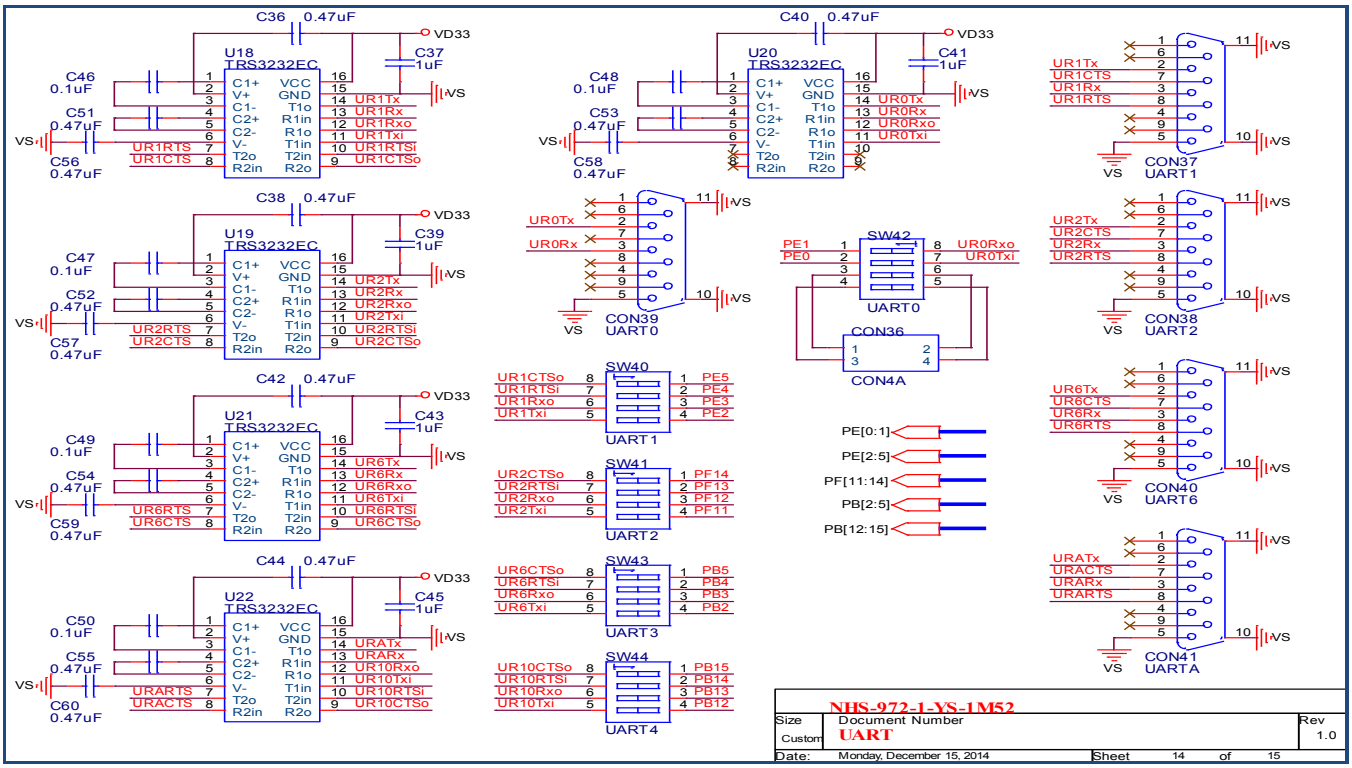
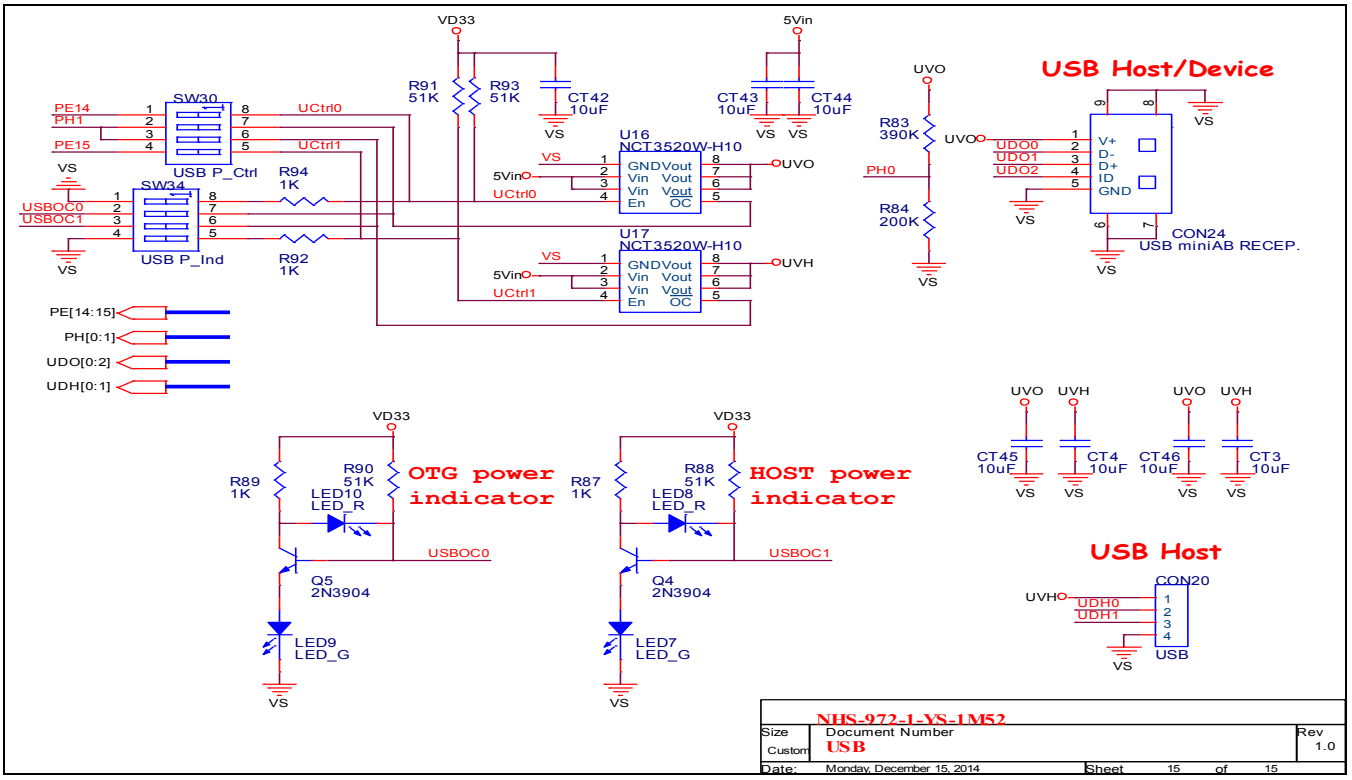


Figure 8-14 USB



Revision History

Rev.	Date	Description
1.0	Mar., 10, 2015	Release version
1.1	June 10, 2015	Added Ethernet design note
1.5	Sept. 10, 2015	Added NUC970B ECO CKT notification

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