NUC977 Development Board
User's Manual

Rev. A1.0

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1 General Description

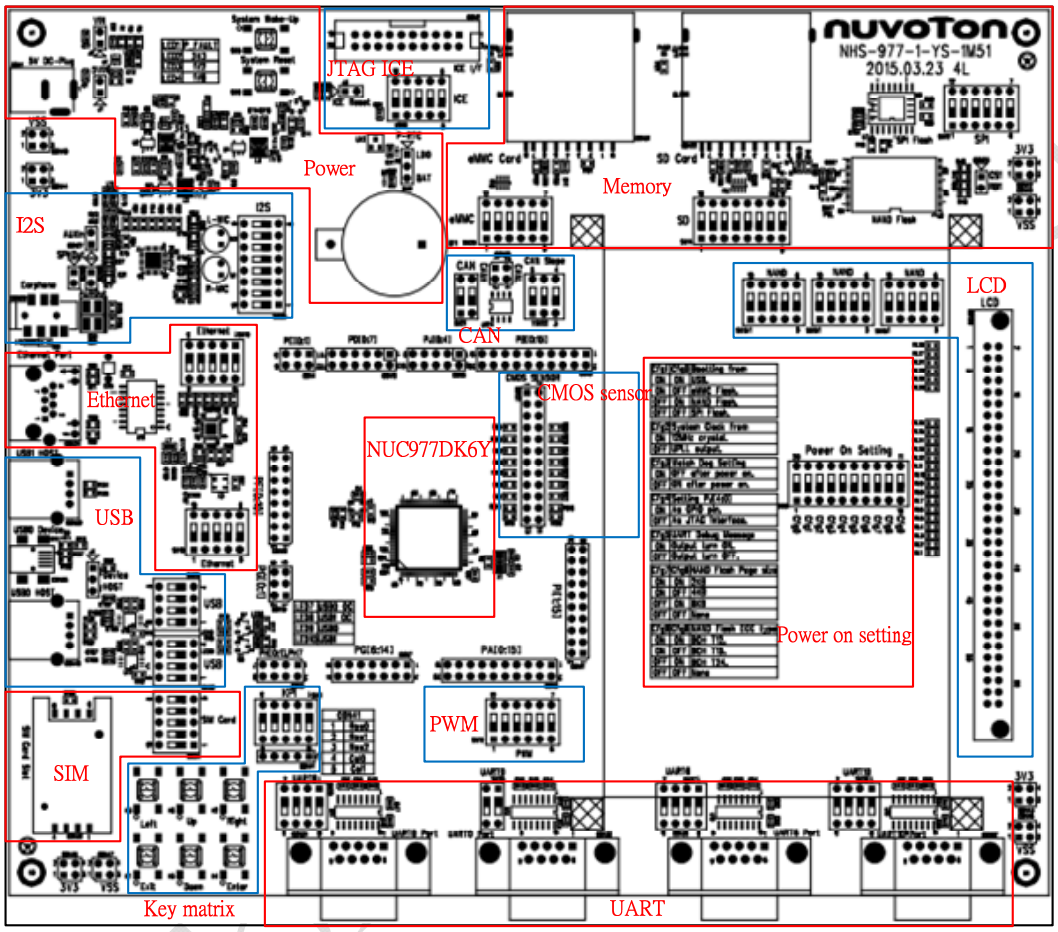
The user's guide describes the operation and use of the NHS-977-1-YS-1M51 development board, The board places NUC977DK62Y's almost of the functions, which includes the peripheral interfaces as memory (NAND flash, SPI flash, SD x 2), UART x 4, I2S, CAN bus, 2 x 3 Key matrix, 16-bit LCD interface, Ethernet, USB host, USB device, CMOS sensor, and SIM card.

In order to easier-check for user, the description is based on the functional block with the sheet of schematic. User can check out what the function port is they would like to design on their system. The schematic is attached for the system reference design.

On the NUC977DK6Y development board, almost of the GPIO pin headers are traced to peripheral device via the dip switches. In which the system designer can easier to verify their module circuit by wire out from the pin header if the corresponding peripheral devices are turned off.

Meanwhile, the board reserves a JTAG ICE port for program development and a UART0 for debugging message. In which is convenient for the designer to develop their system.

2 Peripheral Device



3 Board Description

3.1 Power Block –

CON1 is 5V DC power adaptor input jack terminal which provides the system power for the DC/DC converters, 3.3V is for system I/O and peripheral devices, 1.2V is for CPU's core power, 1.8V is for CPU's internal RAM.

Plug the 5V DC adaptor into the CON1, in which will supply RTC power and system power DC/DC convertors input. Toggle the System Wake-Up key; system power control key, the RTCWkUp will go low, and then the RTCPWREn output Hi to enable DC/DC convertor U2 (3.3V for IO power), U3 (1.2V for core power), U4 (1.8V for RAM power). Mine while, the power LED2 (3.3V), LED3 (1.2V) and LED4 (1.8V) are light, too.

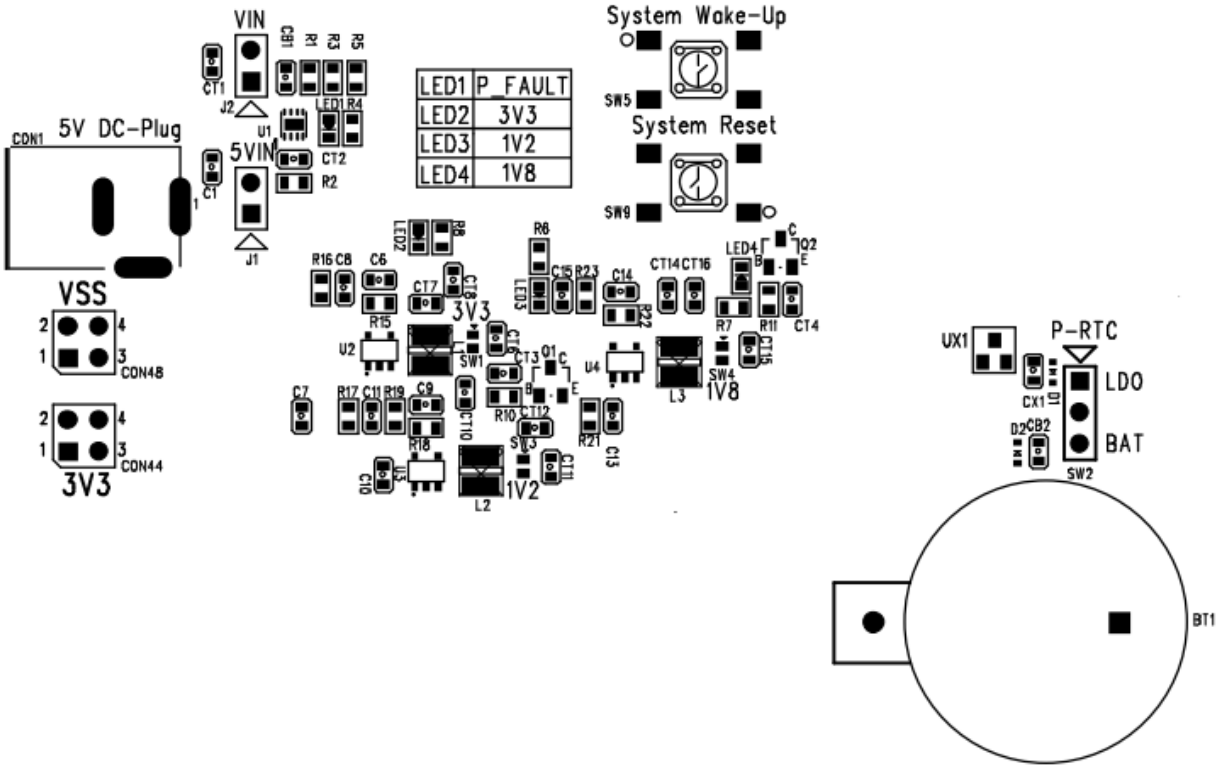
To prevent the input power is over the development board specification, the system board adds a power protection device U1 (APL3203A). The system power will be terminated and LED1 lighting when the input voltage is over 5.85V (APL3203A) or the current is over 1A.

For the over current protection defines formula is as below:

$$I_{OCP} = \frac{K_{ILim}}{R_{ILim}} \qquad K_{ILim} = 25000AK \quad , \quad R_{ILim} = 24K\Omega$$

CON1, 5V power adaptor input terminal, polarity as below:

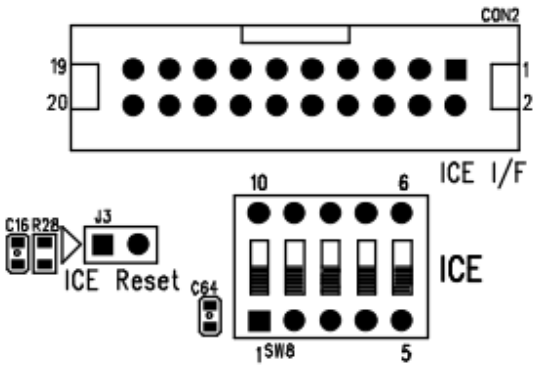
	1: Center hole is positive for 5V+ 2: External ring is negative for ground.
SW5	System Wake-Up key for system power control on/off.
SW9	System Reset key.
BT1	Battery socket is for CR2032.
SW2	1-2: RTC power from LDO
	2-3: RTC power from BT1



3.2 JTAG ICE Block –

CON2 is a connector for JATG ICE port which function has to turn on SW8.

ICE port	PJ[0:4]	SW8	CON2	J3
Note: J3 1-2 ICE reset connector to CPU system reset				

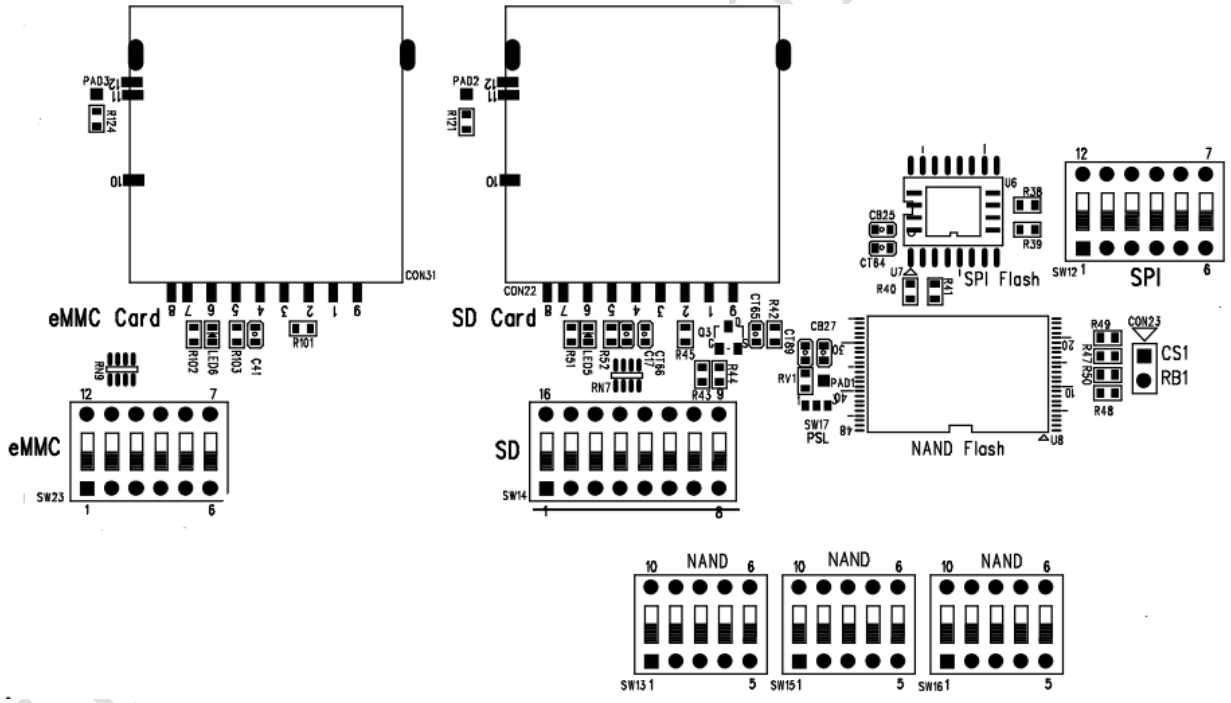


3.3 Memory Block –

Memory block includes eMMC socket, SD socket, NAND flash and SPI flash.

Each one of the device has to be turned on by the corresponding switch which all of the GPIO and DIP switched are listed as below:

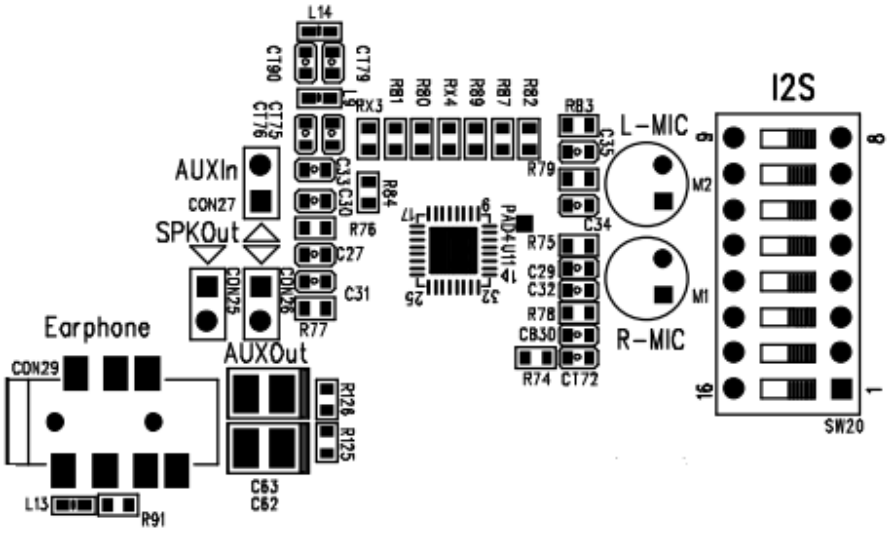
eMMC	PI[5:10]	SW23	CON31
SD	PD[0:7]	SW14	CON22
NAND Flash	PI[1:15]	SW13, SW15, SW16	U8
SPI Flash	PB[6:11]	SW12	U6/U7
Note: 1. The PI[5:10] of eMMC conflicts with NAND flash. 2. Only one (U6 or U7) SPI flash can be used.			



3.4 I2S Block –

Add one CODEC chip (NAU8822L) to I2S port which is easier to verify.

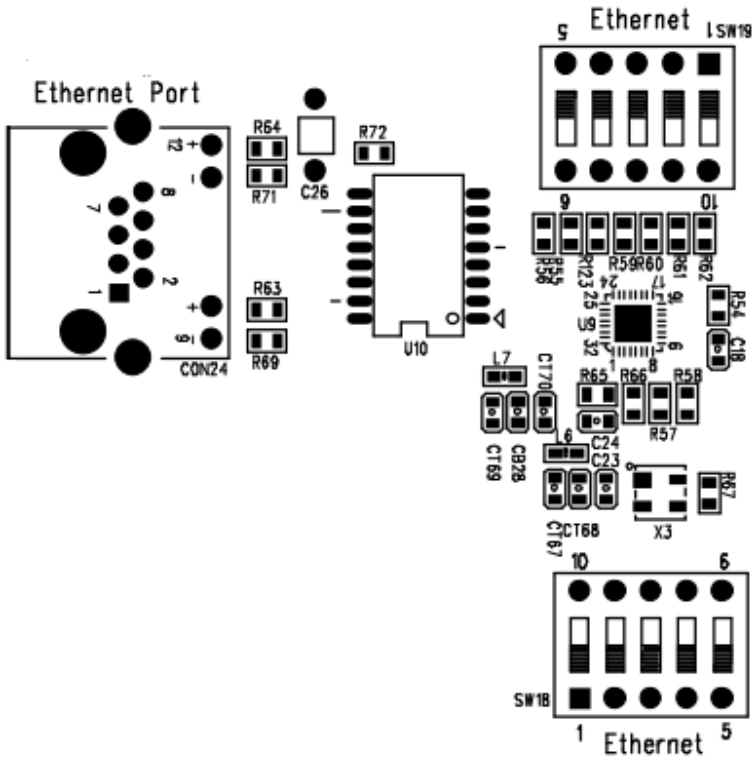
I2S	PG[0:1], PG[10:14], PH7	SW20	U11



3.5 Ethernet Block –

For Ethernet port, the NUC977 support RMII interface which add one Ethernet PHY (IP101GR) to RJ45.

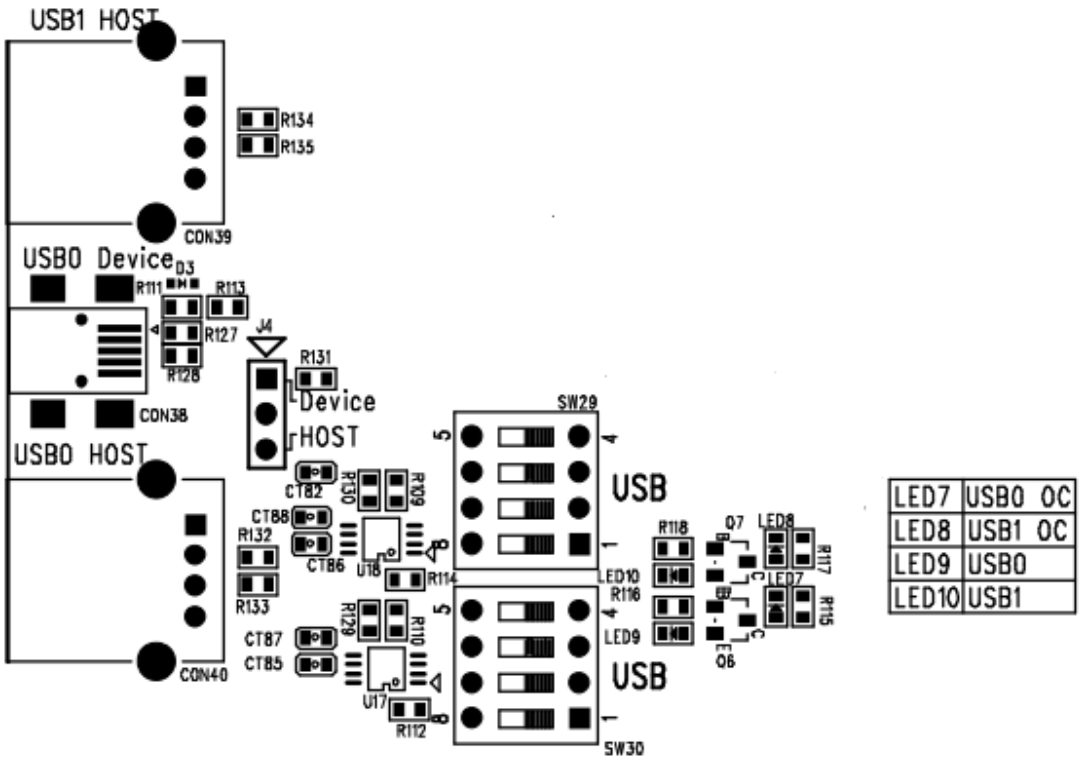
Ethernet	PF[0:9]	SW18, SW19	U9, U10, CON24



3.6 USB Block –

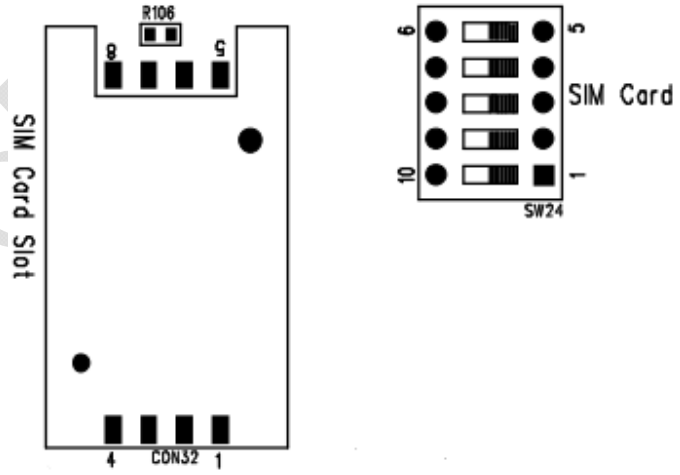
The corresponding DIP switches have to be turned on for the power control. If the USB power control chip isn't control by GPIO, the system is reserved a switch for manual control. The OC pin will active low when the USB power is fault, the fault LED will be turned to red from green.

USB0 Device/HOST	UDO0/UDO1/UDO2, PF10, PH0, PH1	J4, SW29.1/2, SW30.1/2	U17, CON38/CON40
USB1 HOST	UDH0/UDH1, PF10, PH1	SW29.3/4, SW30.3/4	U18, CON39
Note: 1. SW30 is USB power chip enable by hardware force and fault LED setting. 2. J4 1-2: USB0 for Device (CON38) J4 2-3 USB0 for HOST (CON40)			



3.7 SIM Block –

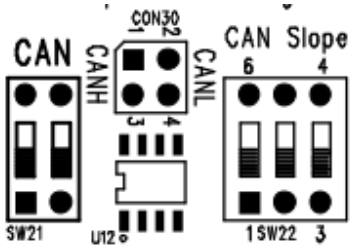
SIM card	PG[10:14]	SW24	CON32



3.8 CAN Block –

Add one CAN transceivers chip (SN65HVD230) to CAN bus.

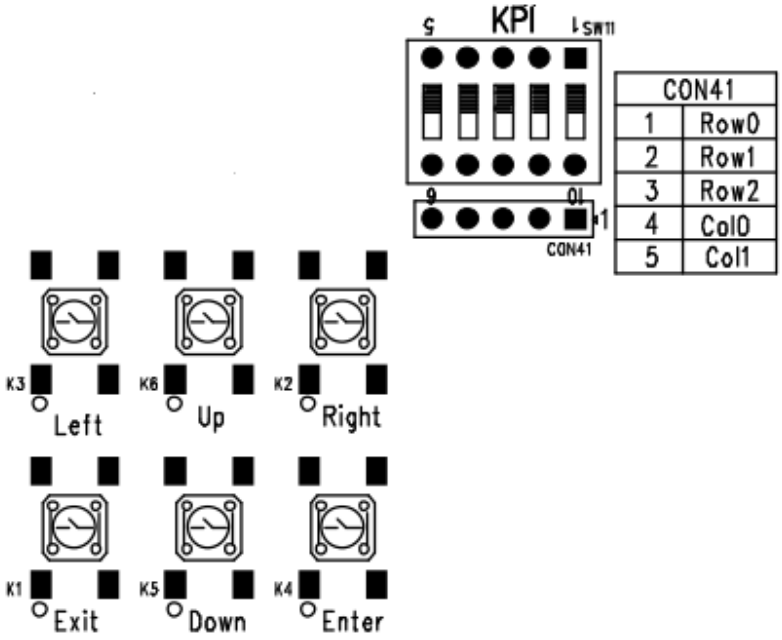
CAN bus 0	CON30.1/2	PI[3:4]	U12, SW21, SW22
Note: SW22 for CAN slope control			



3.9 Key Matrix Block –

2x3 matrix keypads.

Key pads	PA[4:6]: Row[0:2] PA[8:9]: Col[0:1]	SW11	K[1:6]

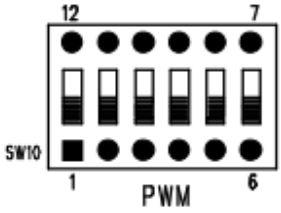


CON41	
1	Row0
2	Row1
3	Row2
4	Col0
5	Col1

3.10 PWM Block –

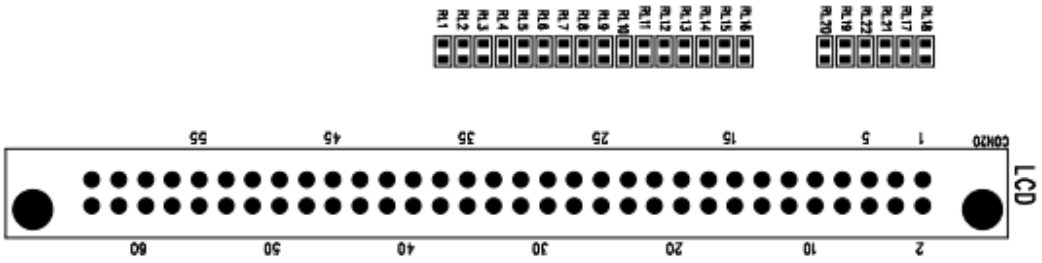
PWM is only reserved with pin header. The LCD backlight could be controlled by the PWM if one of the PWM switch is switched on.

PWM	PA[12:15], PB[2:3]	SW10	CON3, CON9, CON20



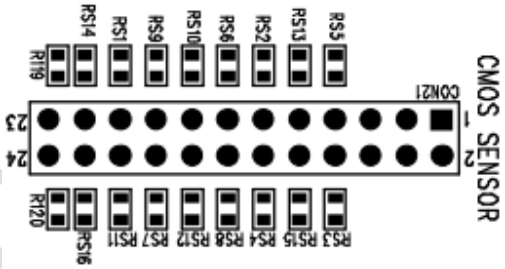
3.11 LCD Block –

LCD	PG[6:9], PB[2:3], PA[0:15]	CON20



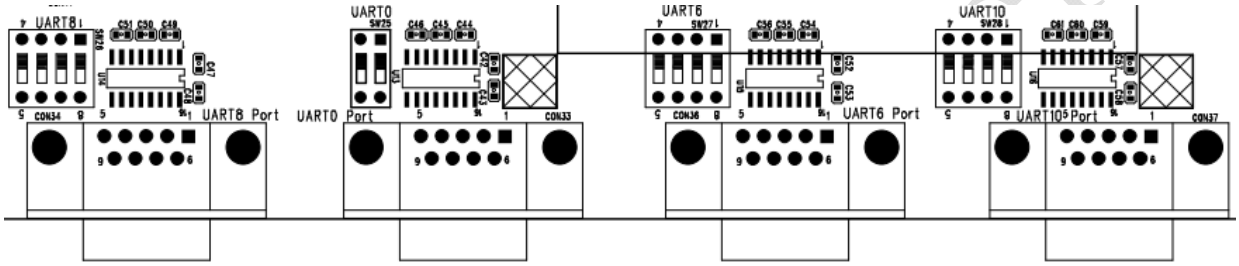
3.12 CMOS Sensor Block –

CMOS Sensor	PI[0:15], PB[0:1]	CON21



3.13 UART Block –

UART8	PI[2:5]	SW26	CON34
UART0	PE[0:1]	SW25	CON33
UART6	PB[2:5]	SW27	CON36
UART10	PB[12:15]	SW28	CON37



3.14 Power On Setting Block –

CPU will recognize the state as the port setting in power on initial. The system designer has to know which one of the state want to use by oneself. Causing there is a scanning time; these pins are in input mode. If possible, the system designer should prevent to use these pins as input mode in this period. All of the configuration setting is listed as below.

Configure Bit	Configured Function	SW
Cfg[1:0] =	00 : Boot from USB. 01 : Boor from eMMC. 10 : Boot from NANA Flash. 11 : Boot from SPI Flash.	SW6.2, SW6.1
Cfg2 =	0 : System clock is from 12 MHz crystal. 1 : System clock is from UPLL output.	SW6.3
Cfg3 =	0 : WDT is OFF after power-on. 1 : WDT is ON after power-on.	SW6.4
Cfg4 =	0 : Pin PJ[0:4] used as GPIO pin.	SW6.5

	1 : Pin PJ[0:4] used as JTAG interface.	
Cfg5 =	0 : UART0 debug message output ON. 1 : UART0 debug message output OFF	SW6.6
Cfg[7:6] =	00 : NAND Flash page size is 2KB. 01 : NAND Flash page size is 4KB. 10 : NAND Flash page size is 8KB. 11 : Ignore Power-On Setting.	SW6.8, SW6.7
Cfg[9:8] =	00 : NAND Flash ECC type is BCH T12. 01 : NAND Flash ECC type is BCH T15. 10 : NAND Flash ECC type is BCH T24. 11 : Ignore Power-On Setting.	SW6.10, SW6.9

Note: The configured pin should be pulled low with a 10KΩ.

Cfg1	Cfg0	Bootting from
ON	ON	USB.
ON	OFF	eMMC Flash.
OFF	ON	NAND Flash.
OFF	OFF	SPI Flash.

Cfg2	System Clock from
ON	12MHz crystal.
OFF	UPLL output.

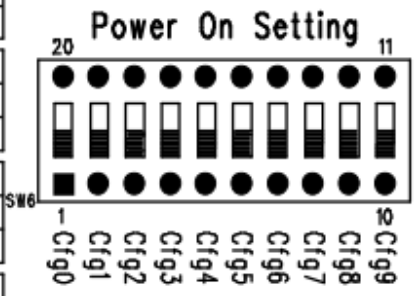
Cfg3	Watch Dog Setting
ON	OFF after power on.
OFF	ON after power on.

Cfg4	Setting PJ[4:0]
ON	As GPIO pin.
OFF	As JTAG interface.

Cfg5	UART Debug Message
ON	Output turn ON.
OFF	Output turn OFF.

Cfg7	Cfg6	NAND Flash Page size
ON	ON	2KB
ON	OFF	4KB
OFF	ON	8KB
OFF	OFF	None

Cfg9	Cfg8	NAND Flash ECC type
ON	ON	BCH T12.
ON	OFF	BCH T15.
OFF	ON	BCH T24.
OFF	OFF	None



4 Pin Function assignment

Pin No.	NUC977	1st Function	2nd Function	3rd Function
1	USB0_ID			
2	PG.1	I2C0SDA		
3	PG.0	I2C0SCK		
4	PG.14	I2S LRCk	SIMC0 CD	
5	PG.13	I2S BClk	SIMC0 PWR	
6	PG.12	I2S Di	SIMC0 DAT	
7	PG.11	I2S Do	SIMC0 CLK	
8	PG.10	I2S MClk	SIMC0 RST	
9	VDD33			
10	VDD12			
11	MVDD18			
12	MVDD18			
13	VDD12			
14	PG.9	LCD DEN		
15	PG.8	LCD Vsync		
16	PG.7	LCD Hsync		
17	PG.6	LCD CLK		
18	PA.15	PWM3	LCD D15	
19	PA.14	PWM2	LCD D14	
20	PA.13	PWM1	LCD D13	
21	PA.12	PWM0	LCD D12	
22	PA.11		LCD D11	
23	PA.10		LCD D10	
24	VDD33			
25	PA.9	Power on setting 9	LCD D9	Key Col1
26	PA.8	Power on setting 8	LCD D8	Key Col0
27	PA.7	Power on setting 7	LCD D7	
28	PA.6	Power on setting 6	LCD D6	Key Row2
29	PA.5	Power on setting 5	LCD D5	Key Row1

30	PA.4	Power on setting 4	LCD D4	Key Row0
31	PA.3	Power on setting 3	LCD D3	
32	PA.2	Power on setting 2	LCD D2	
33	PA.1	Power on setting 1	LCD D1	
34	PA.0	Power on setting 0	LCD D0	
35	RTC_VDD33			
36	SYS_PWREn			
37	SYS_nWkUp			
38	X32_IN			
39	X32_OUT			
40	PH.7	I2S CSB		
41	VDD12			
42	PI.1		NCS0	
43	PI.2		NWP	
44	PI.3	VCAP SCLKo	NALE	CAN0Rx
45	PI.4	VCAP SPCLK	NCLE	CAN0Tx
46	PI.5	VCAP SHsync	NWE	eMMC CMD
47	PI.6	VCAP SVsync	NRE	eMMC CLK
48	PI.7	VCAP SField	NRB0	eMMC D3
49	PI.8	VCAP SD0	ND0	eMMC D0
50	PI.9	VCAP SD1	ND1	eMMC D1
51	PI.10	VCAP SD2	ND2	eMMC D2
52	PI.11	VCAP SD3	ND3	
53	PI.12	VCAP SD4	ND4	UR8Tx
54	PI.13	VCAP SD5	ND5	UR8Rx
55	PI.14	VCAP SD6	ND6	UR8RTS
56	PI.15	VCAP SD7	ND7	UR8CTS
57	VDD33			
58	PB.0	I2C1 SCL		
59	PB.1	I2C1 SDA		
60	PB.2	LCD CS	PWM0	UR6Tx
61	PB.3	LCD BLEn	PWM1	UR6Rx

62	PB.4			UR6RTS
63	PB.5			UR6CTS
64	VSS			
65	PB.6	SPI0 CS0		
66	PB.7	SPI0 CLK		
67	PB.8	SPI0 DoD0		
68	PB.9	SPI0 DiD1		
69	PB.10	SPI0 D2		
70	PB.11	SPI0 D3		
71	PB.12			UR10Tx
72	PB.13			UR10Rx
73	PB.14			UR10RTS
74	PB.15			UR10CTS
75	PJ.3	TDO		
76	PJ.0	TCK		
77	PJ.1	TMS		
78	PJ.2	TDI		
79	PJ.4	nTRST		
80	nRESET			
81	VDD33			
82	VDD12			
83	MVDD18			
84	MVDD18			
85	VDD33			
86	PD.0	SD0 CMD		
87	PD.1	SD0 CLK		
88	PD.2	SD0 D0		
89	PD.3	SD0 D1		
90	PD.4	SD0 D2		
91	PD.5	SD0 D3		
92	PD.6	SD0 CD		
93	PD.7	SD0 PWR		

94	VDD12			
95	PLL_VSS			
96	PE.1			UR0Rx
97	PE.0			UR0Tx
98	VDD33			
99	MainXi			
100	MainXo			
101	VSS			
102	PF.9	RMII0 RxErr		
103	PF.8	RMII0 CRSDV		
104	PF.7	RMII0 RxD1		
105	PF.6	RMII0 RxD0		
106	PF.5	RMII0 RefCLK		
107	PF.4	RMII0 TxEn		
108	PF.3	RMII0 TxD1		
109	PF.2	RMII0 TxD0		
110	PF.1	RMII0 MDio		
111	PF.0	RMII0 MDC		
112	PH.1	USB0/1 OC		
113	PH.0	USB0 VbusDet		
114	PF.10	USB0/1 PWREn		
115	VDD12			
116	VDD12			
117	USBPLL1_VD12			
118	USB1 DM			
119	USB1 DP			
120	USB1_VDD33			
121	USB1 REXT			
122	USBPLL0_VD12			
123	USB0_VSS			
124	USB0 DM			
125	USB0 DP			

126	USB0_VDD33			
127	USB0 REXT			
128	VSS			

5 Document Revision History

Date	Revision	Remarks
08/06/2015	A1.0	Release version A1.0.

Important Notice

NuvoTon products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Furthermore, NuvoTon products are not intended for applications wherein failure of NuvoTon products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

NuvoTon customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify NuvoTon for any damages resulting from such improper use or sales.

6 Schematics

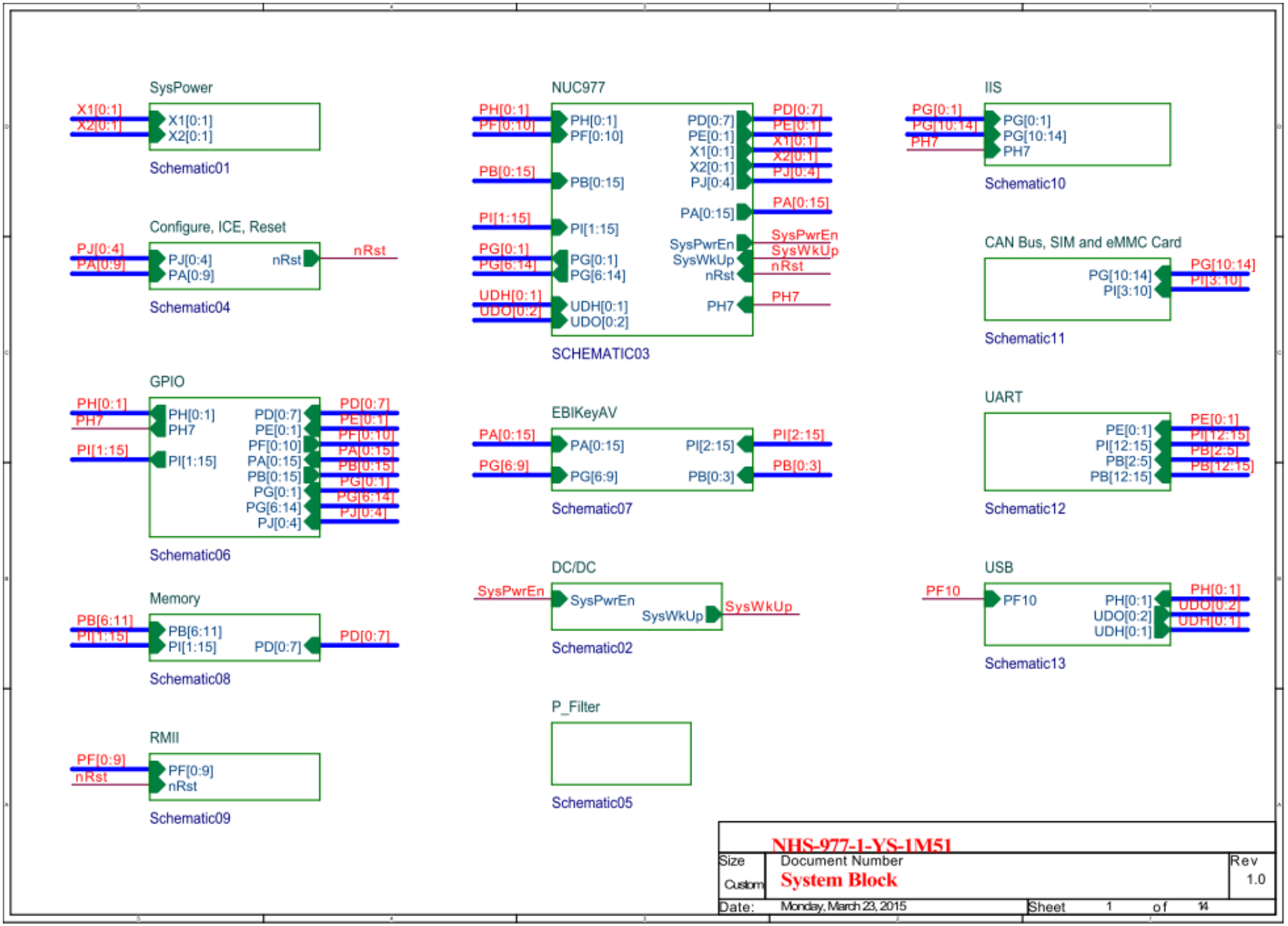


Figure 6-1Block Diagram

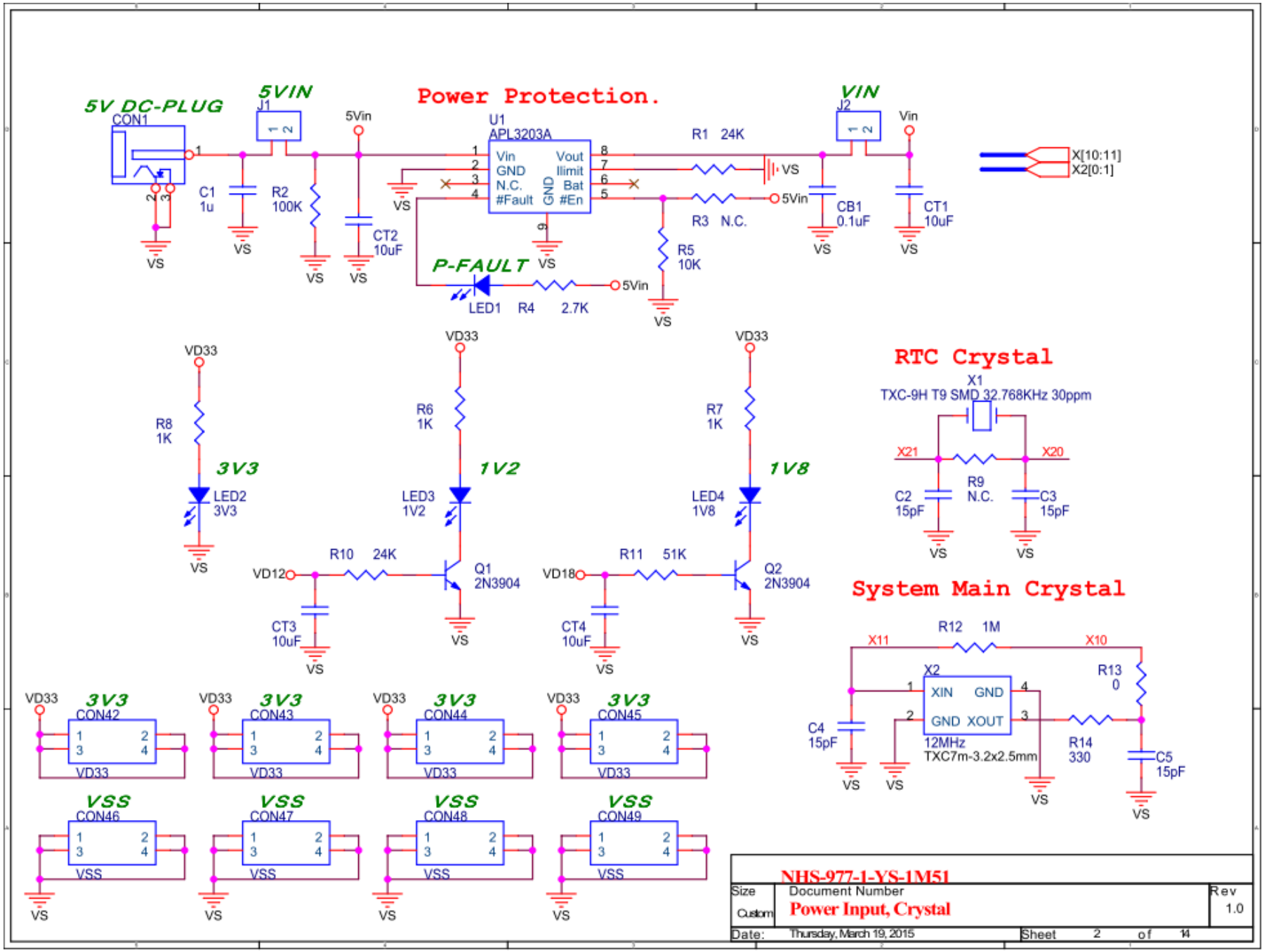


Figure 6-2 System Power

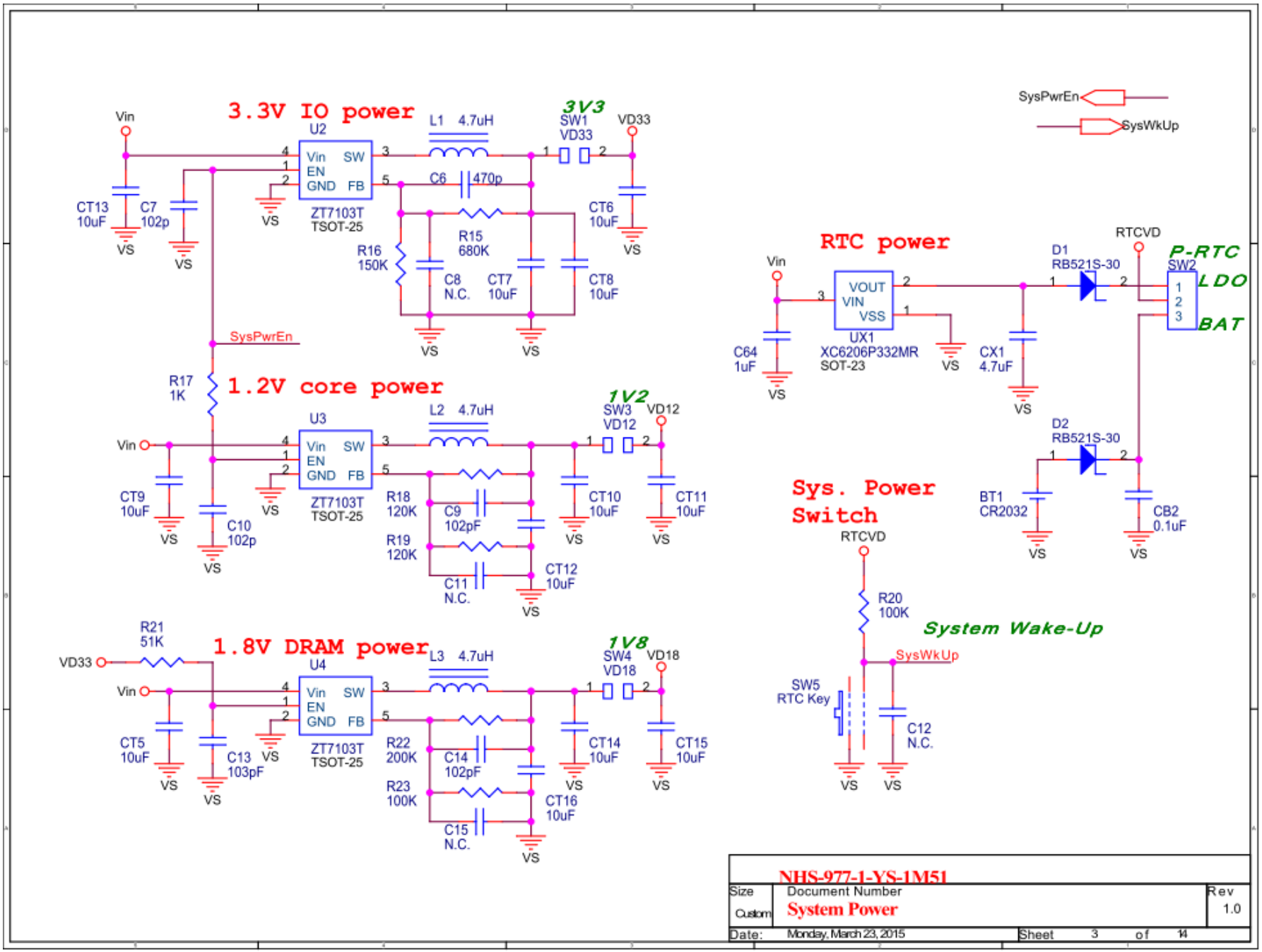


Figure 6-3 DC/DC

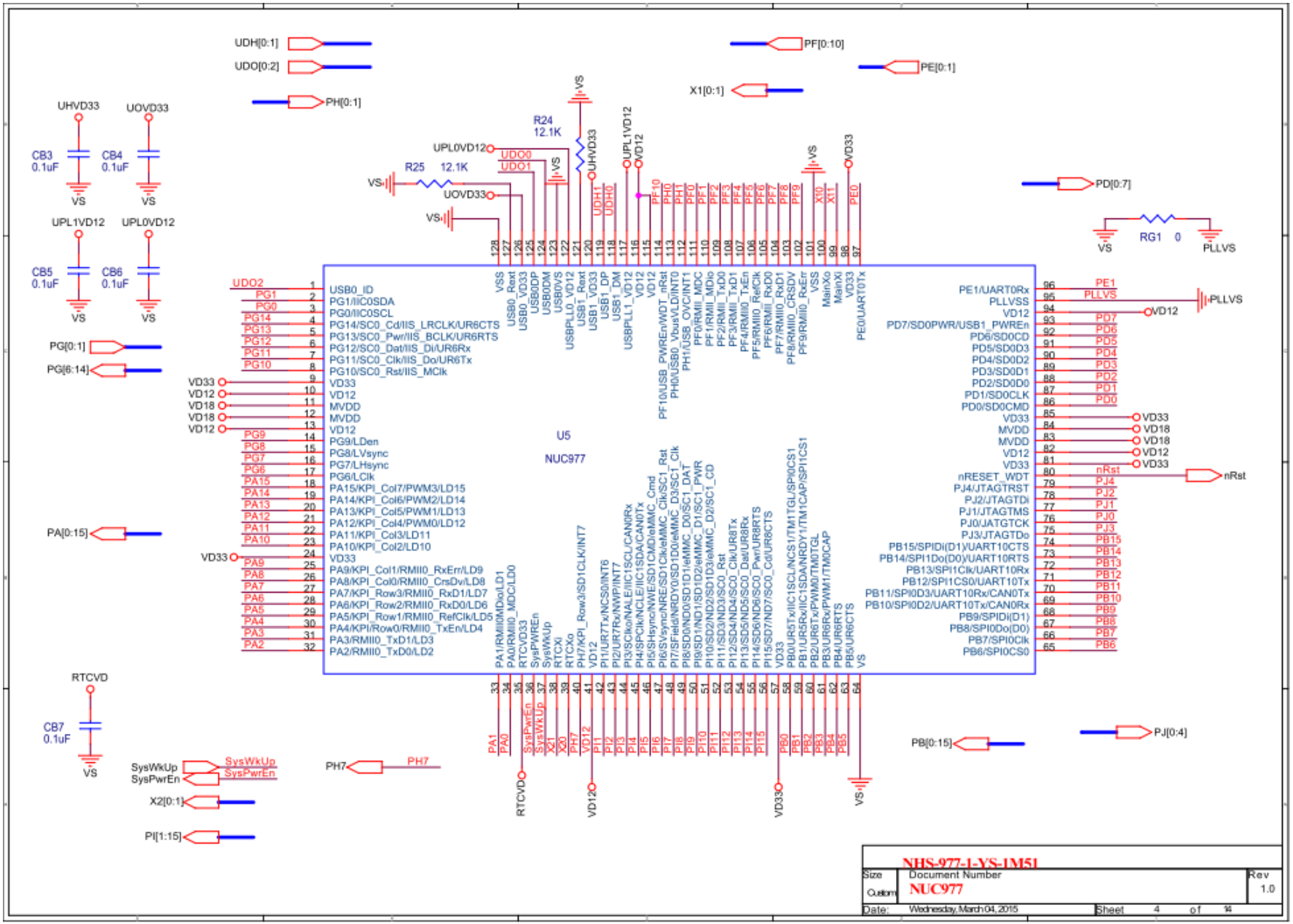


Figure 6-4 NUC977

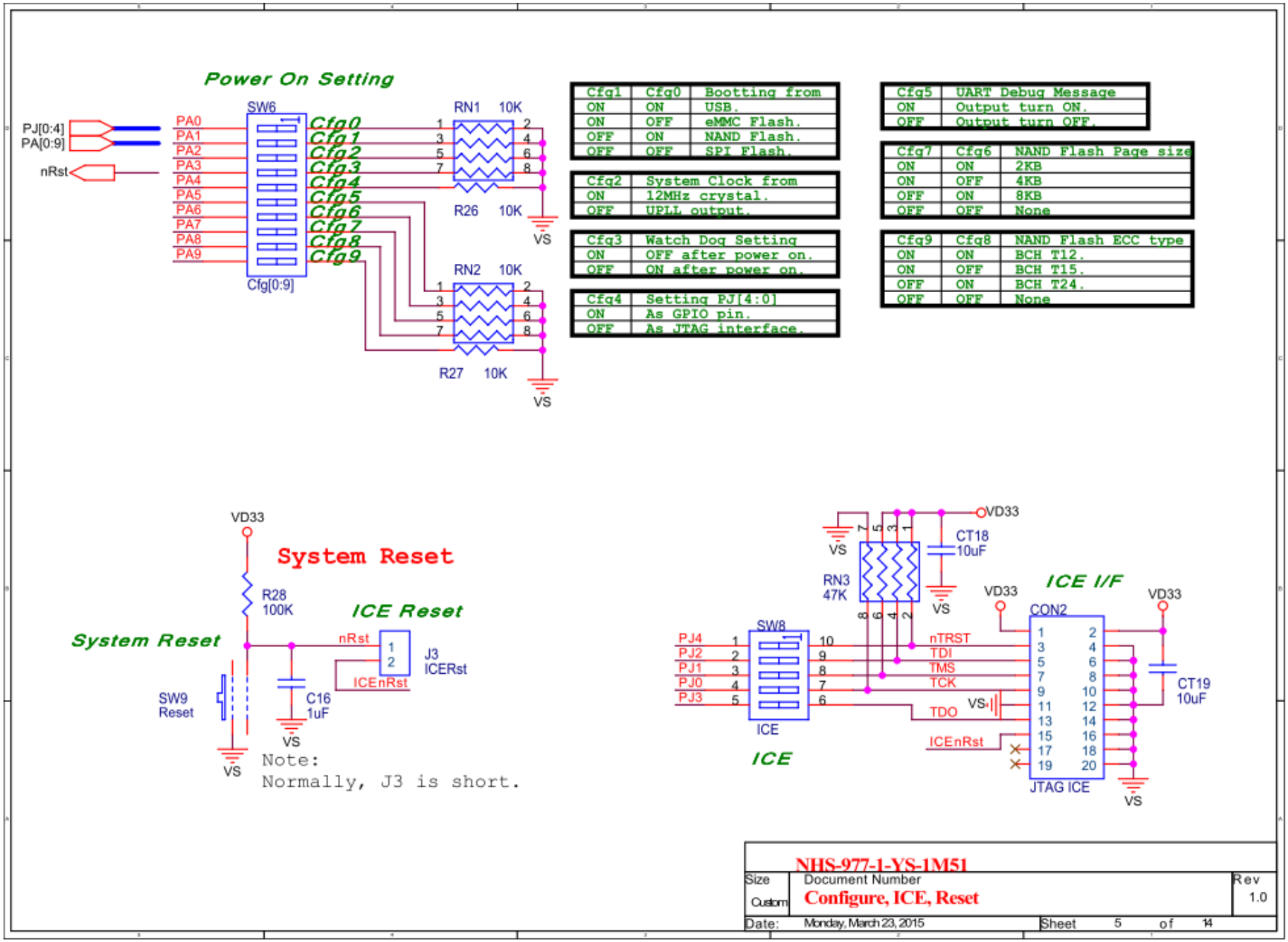


Figure 6-5 Configure, ICE Reset

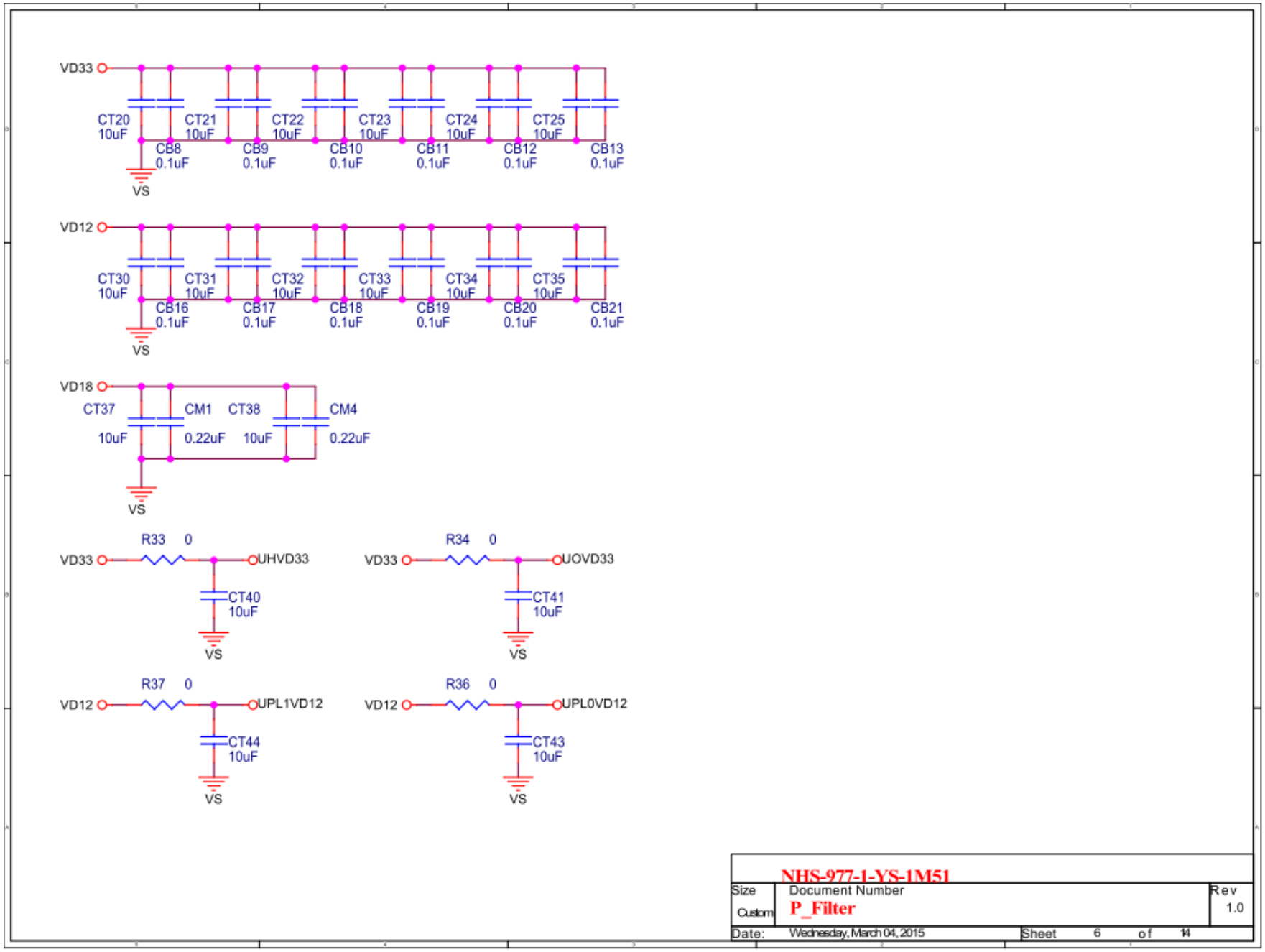


Figure 6-6 P_Filter

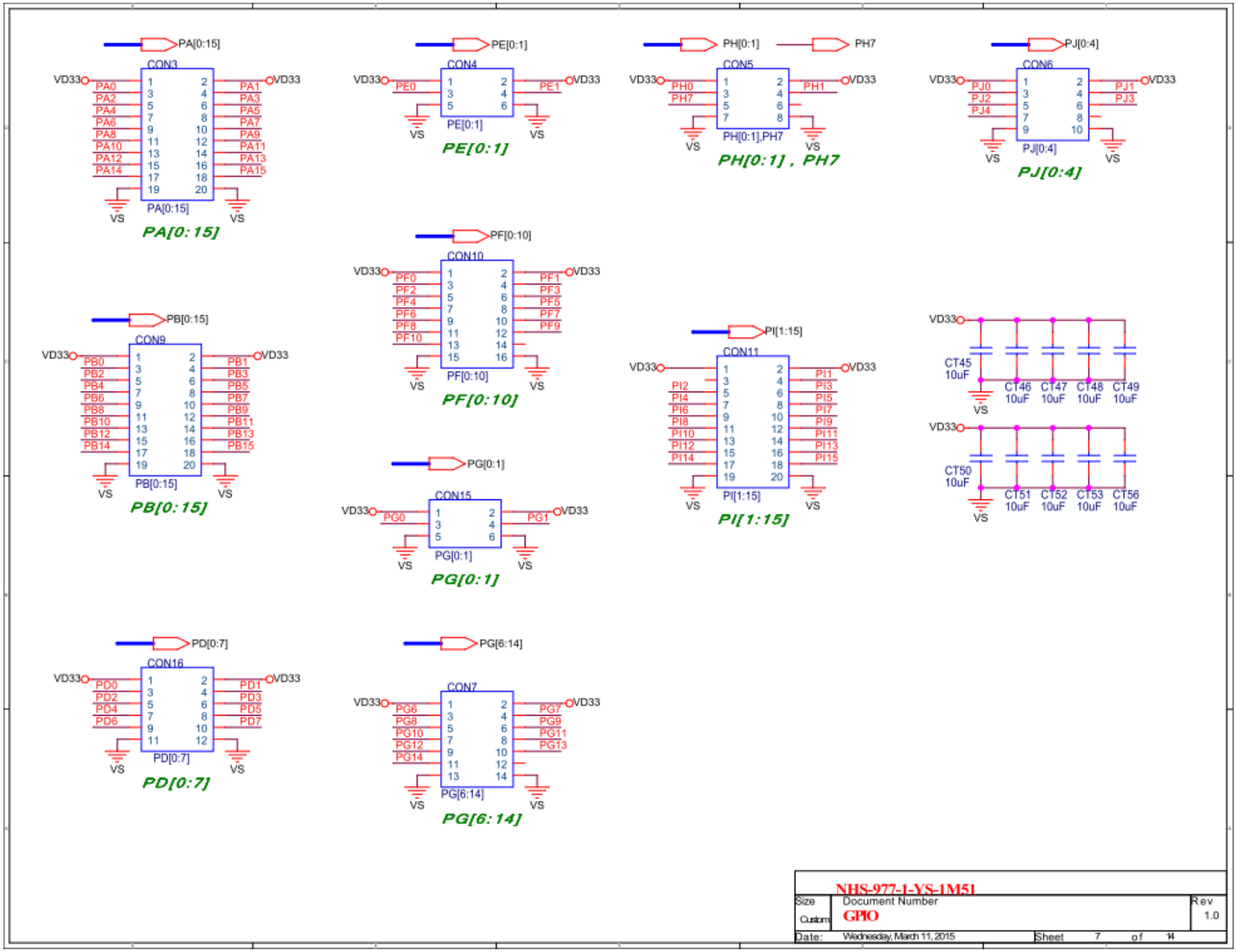


Figure 6-7 GPIO

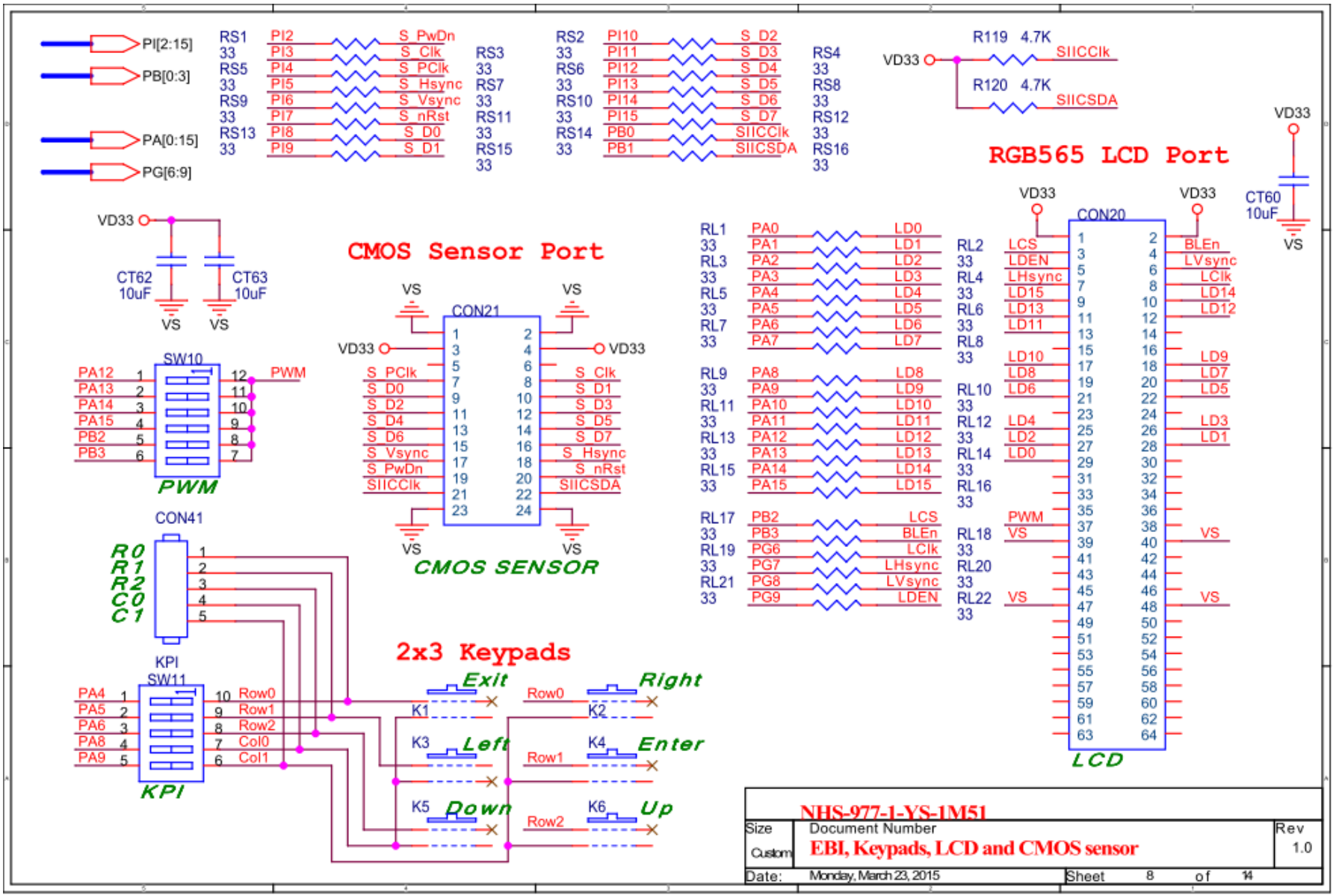


Figure 6-8 Keys, AV

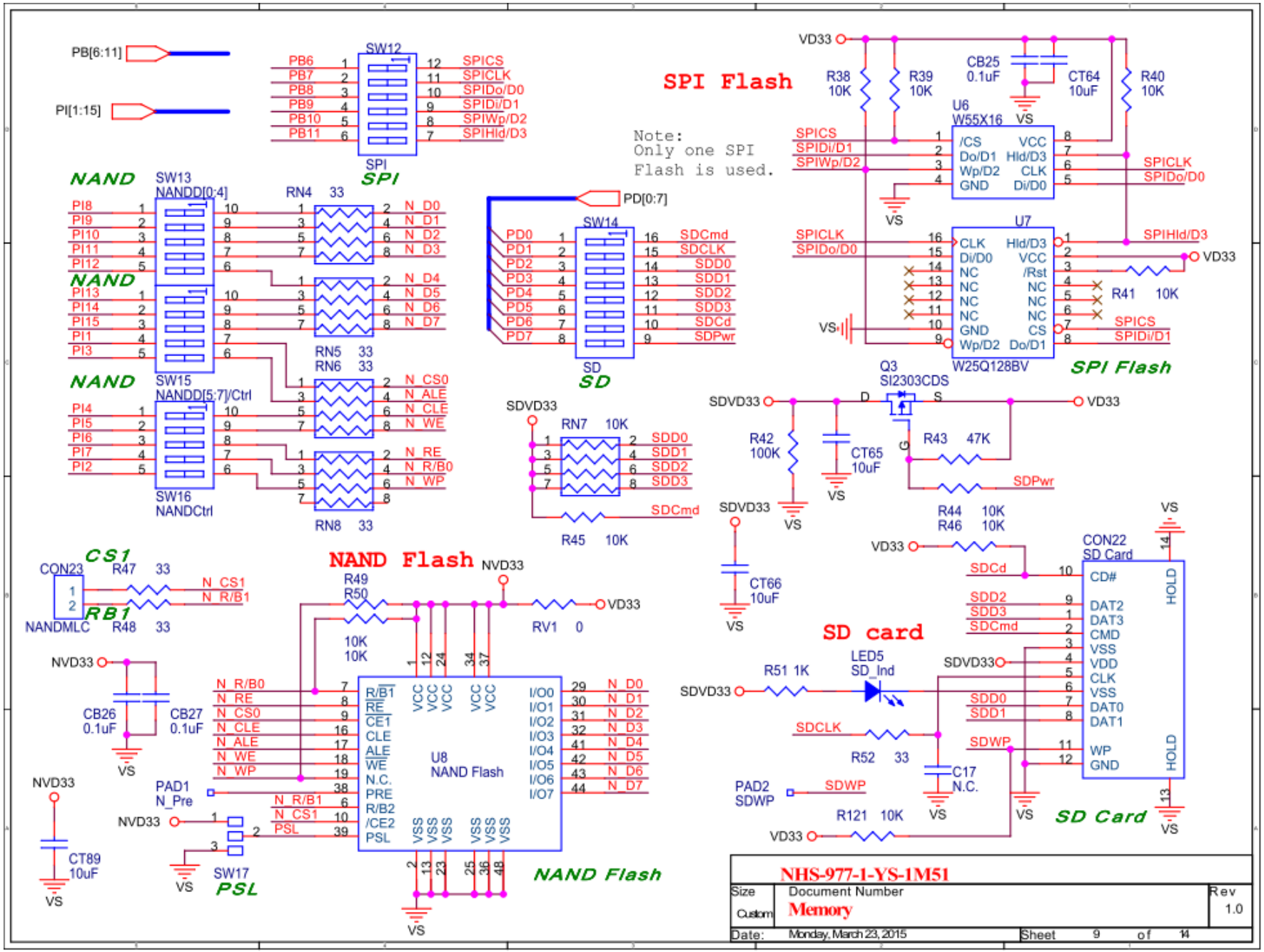


Figure 6-9 Memory

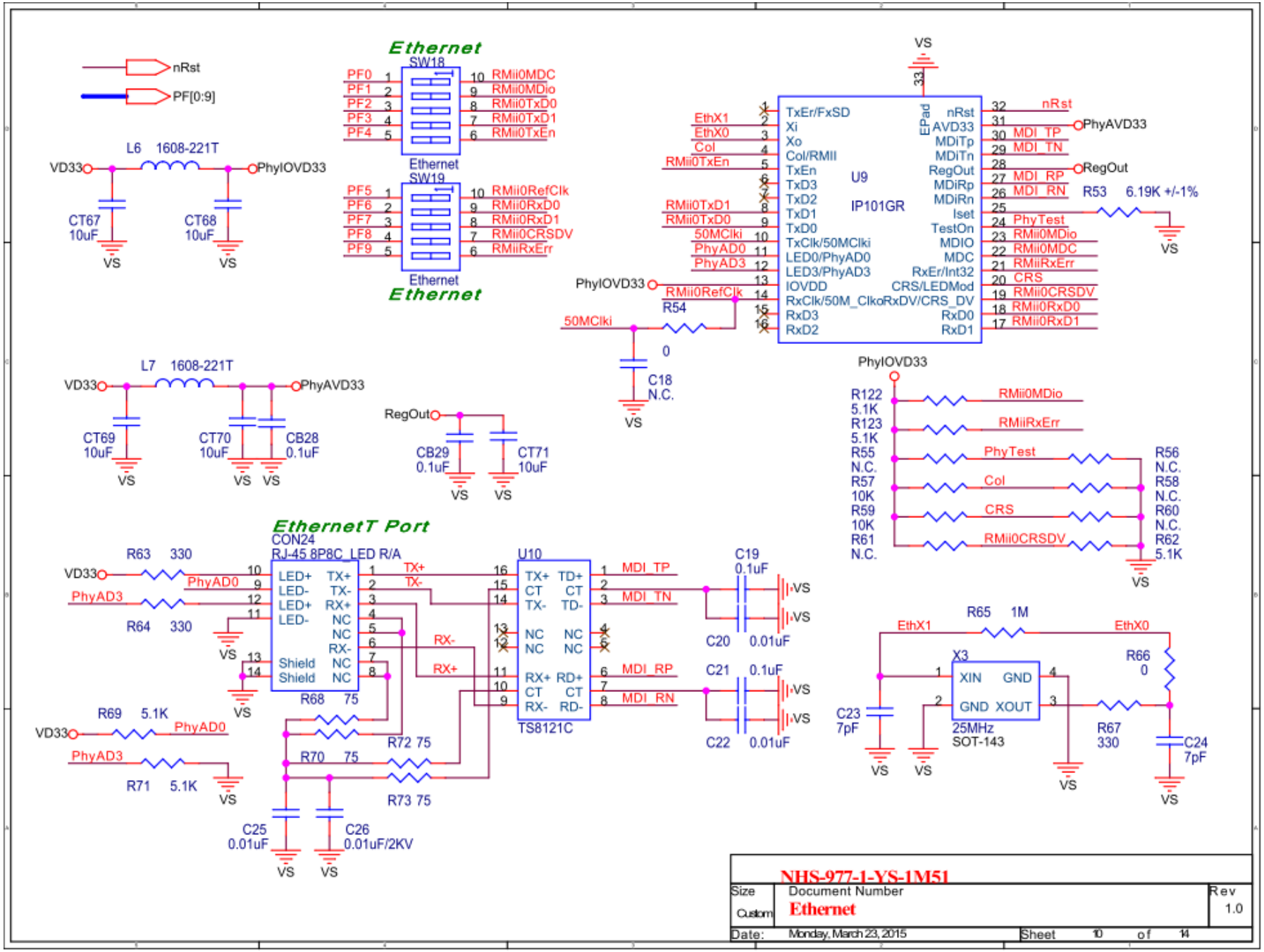


Figure 6-10 RMII

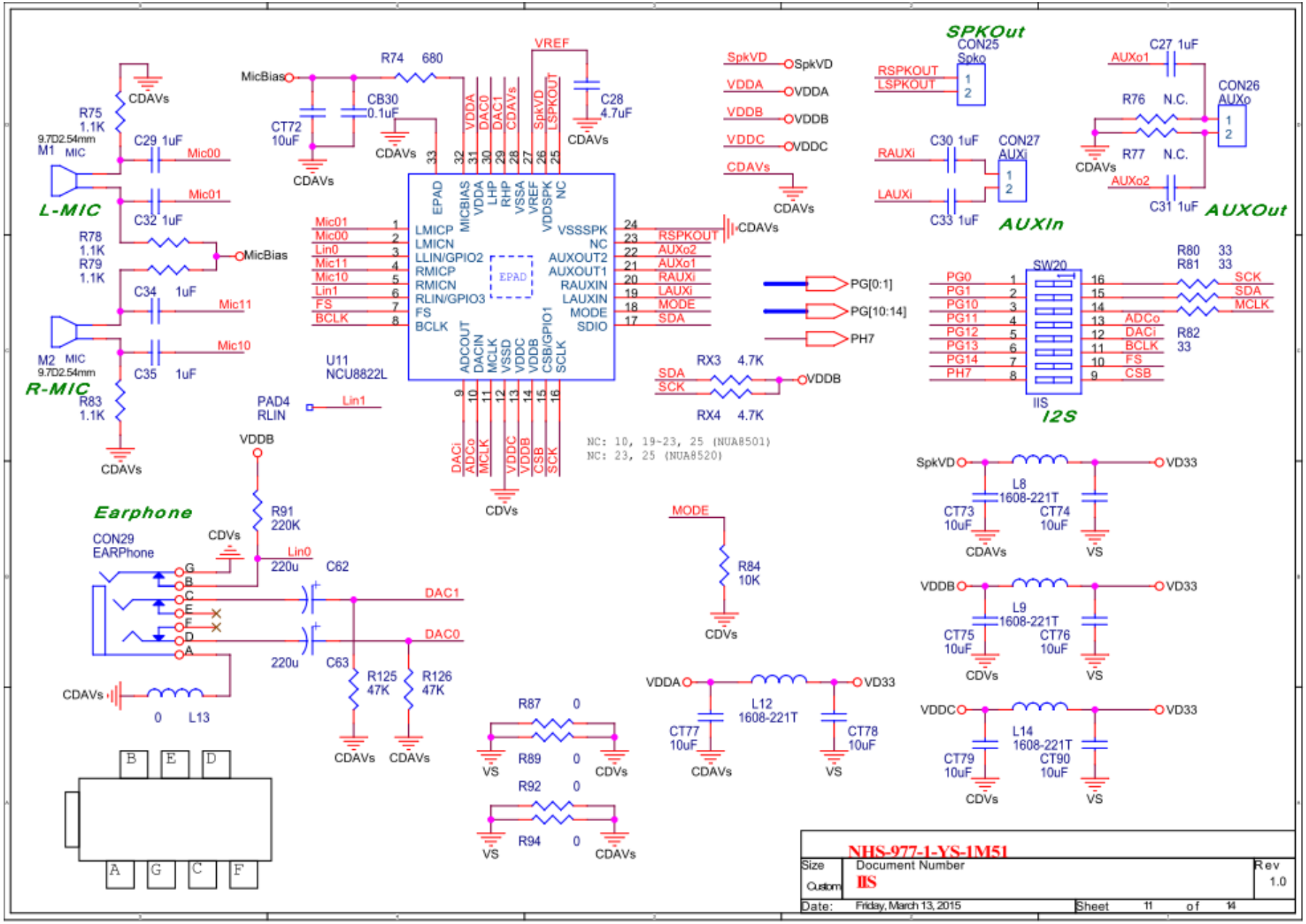


Figure 6-11 I2S

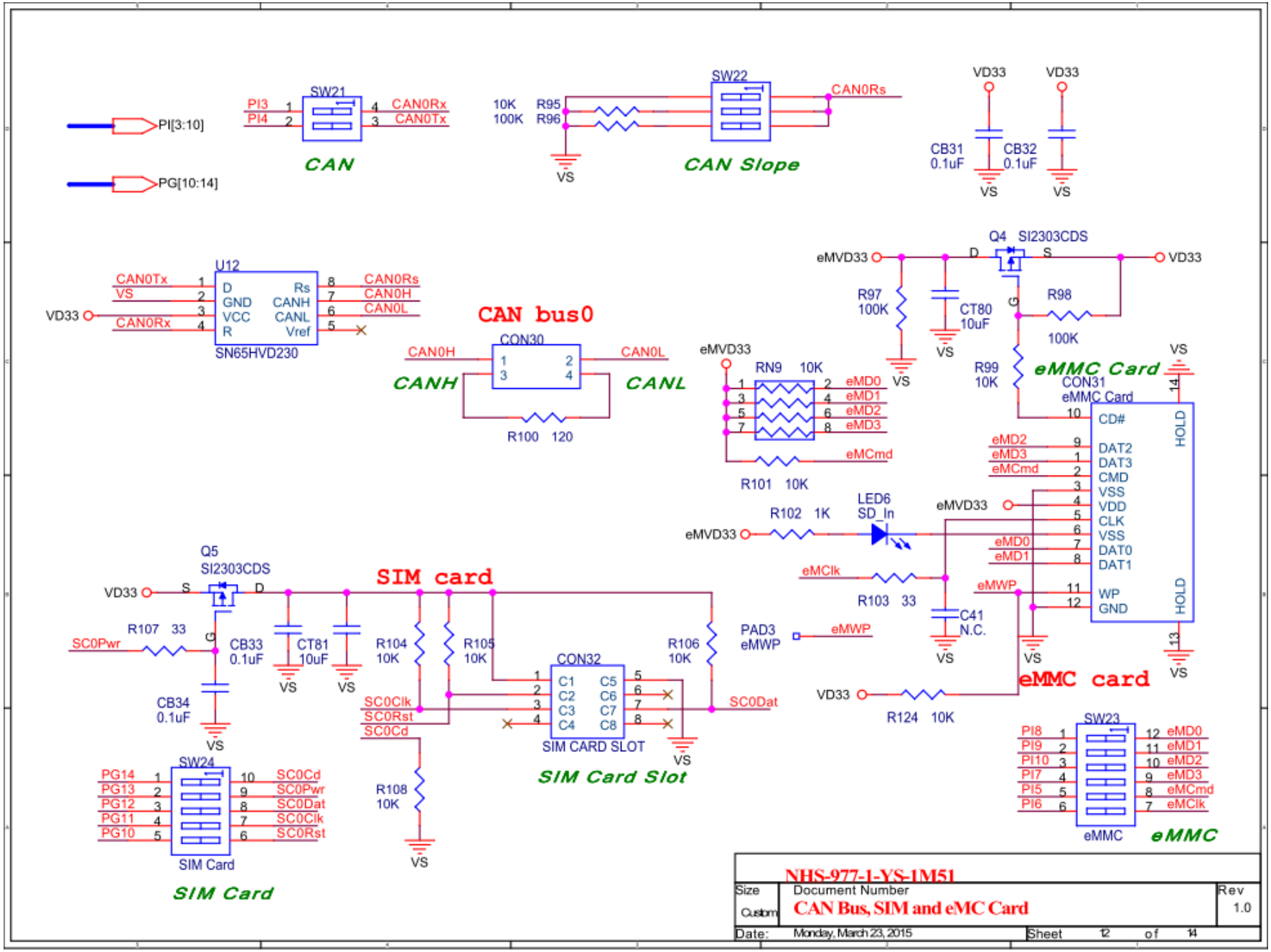


Figure 6-12 CAN Bus, SIM card and eMMC

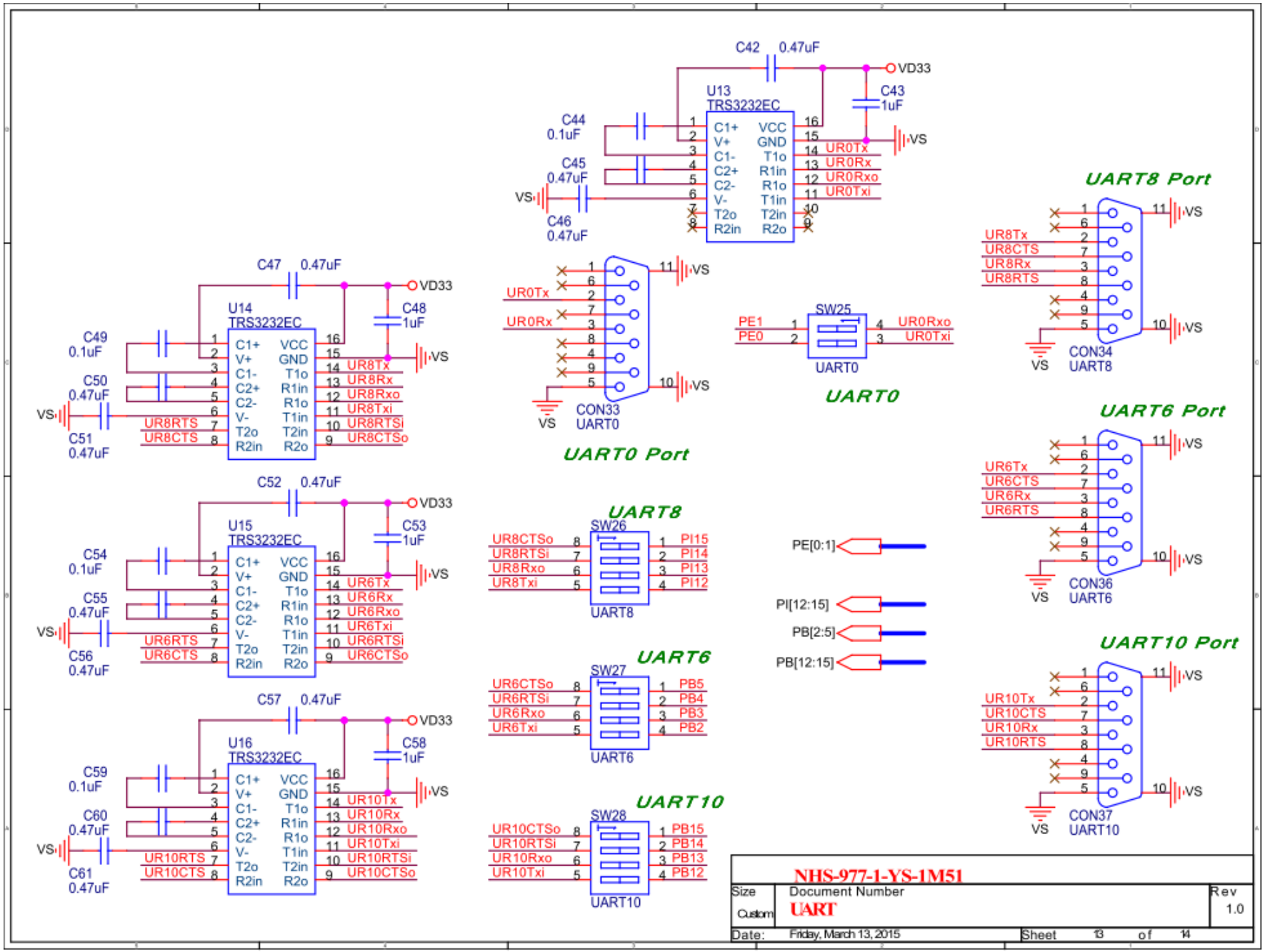


Figure 6-13 UART

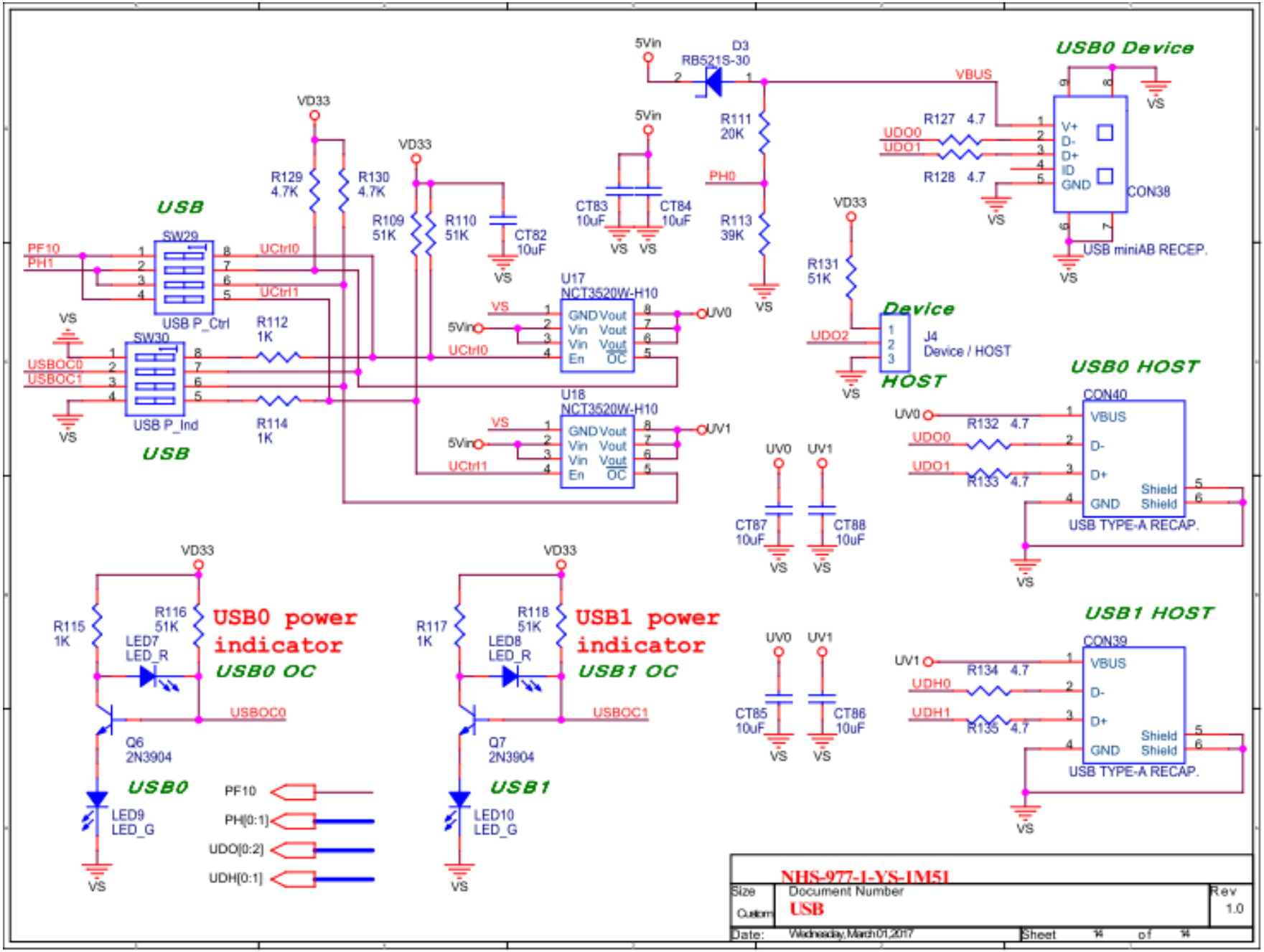


Figure 6-14 USB