

# **NUC970 SAR ADC Application Note**

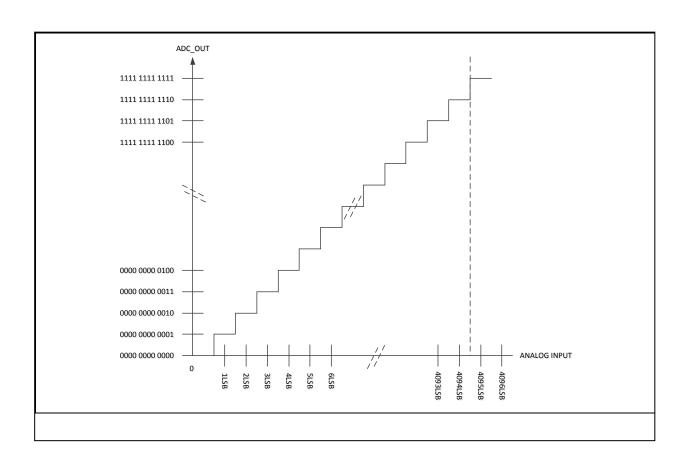
Nuvoton Technology Corp.

#### **NUC970 SAR ADC Features**

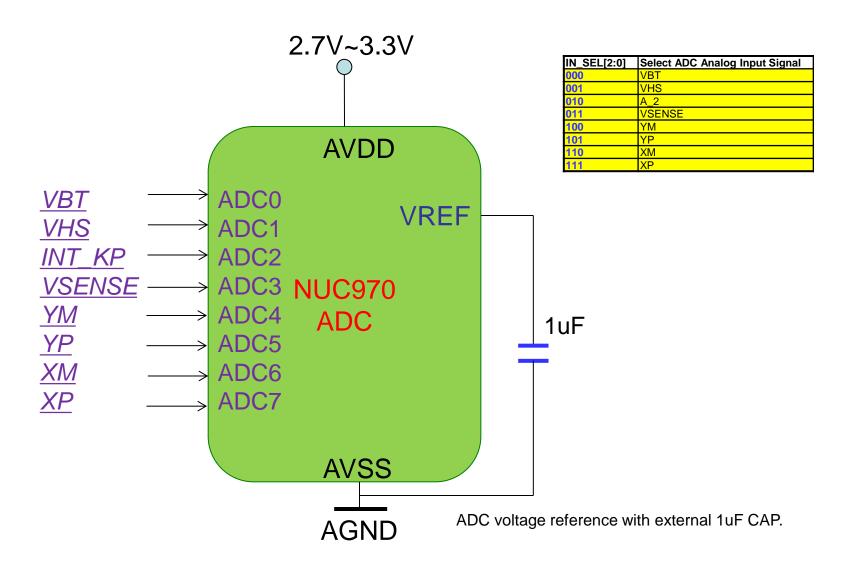
- Resolution: 12-bit resolution
- **DNL**: +/-1.5 LSB, **INL**: +/-3 LSB
- Dual Data Rates: 1MSPS/ 200KSPS (ADC1 only)
- Power Supply (AVDD) range: 2.7-3.6V
- ADC0 (VBT), for Direct Battery Measurement
- ADC1 (VHS), could support 1MS/S
- ADC2 (INT\_KP), could support 200KS/S or Keypad signal input
- ADC3 (VSENSE), ADC analog input or for 5-wire touch detection
- ADC4 (YM), ADC analog input or touch negative end of Y axis
- ADC5 (YP), ADC analog input or touch positive end of Y axis
- ADC6 (XM), ADC analog input or touch negative end of X axis
- ADC7 (XP), ADC analog input or touch positive end of X axis
- NUC972, supports 4-wire or 5-Wires resistive touch screen.
- NUC973 & NUC976, just supported 4-Wires resistive touch screen
- NUC977, doesn't support touch function
- Touch Pressure Measurement, it just for 4-wire touch screen application

#### **ADC Transfer Function**

➤ The ADC output coding is offset in binary, 1LSB=VREF/4096, the transfer characteristic is shown in the following graph:

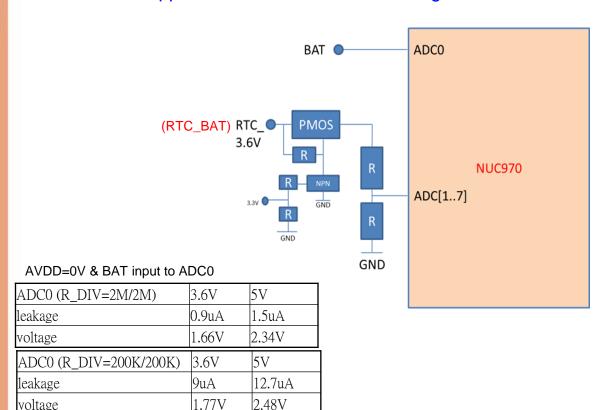


# **Typical Connection**



# ADC0 & ADC[1:7] Application for **Voltage Detection**

For avoiding leakage occurred by ADC pad when AVDD not powered yet, that recommend voltage detection application should use the following connection as the figure illustrated



5V

5V

0.1uA

3.6V

0uA

3.6V

voltage

leakage

voltage

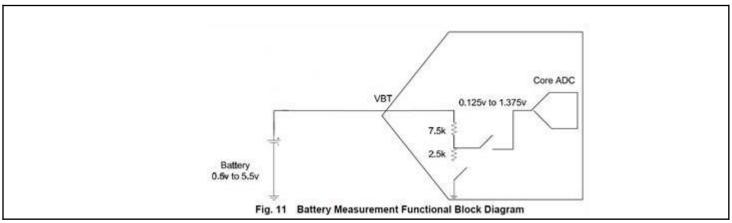
ADC0 (direct connect)

#### AVDD=0V & RTC BAT input to ADC[1..7]

ADC[17] (R_DIV=2M/2M)	3.6V	5V				
Leakage	1.7uA	2.4V				
Voltage	302mV	332mV				
ADC[17] (R_DIV=200K/200K)	3.6V	5V				
leakage	15.4uA	22uA				
Voltage	505mV	645mV				
ADC[17] (direct connect)	3.6V	5V				
leakge	117.4mA	illegal				
voltage	3.6V	illegal				

# ADC0 (VBT) for Direct Battery Measurement

➤ Take VBT as input, and select internal buffer's output as the reference For ADC configure register VBAT\_EN (ADC\_CONF[8]) should be set to 1.



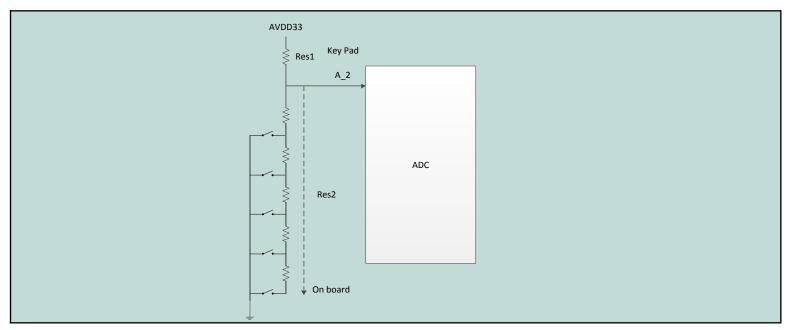
ADC Battery Voltage Detection Diagram

VBT in(v)	ADC0 output code/ V	Power Consumption (uA) /per time		
0.5	196/ 0.119V	44		
1	404/0.245V	90		
2	820/0.5V	183		
3	1236/0.754V	276		
4	1648/1.006V	368		
5	2062/1.258V	460		
5.5	2265/1.382V	505		

# ADC1 (VHS)

- ADC high speed input, could support 1MS/S or 200KS/S.
- When HSPEED is set to high, it supports1MS/S
  - ADC Configure (ADC\_CONF[22]=1)
- When HSPEED is set to low, it supports 200KS/S
  - ADC Configure (ADC\_CONF[22]=0)

## ADC2 (INT\_KP)

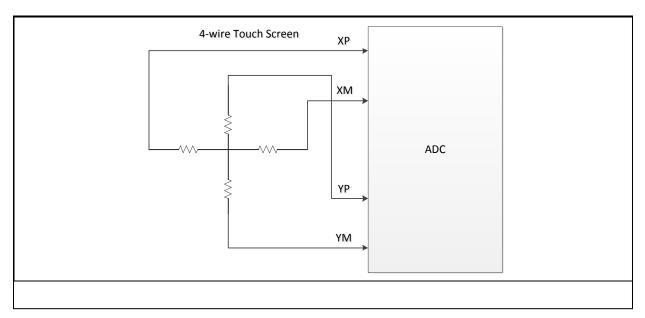


Key Pad Detection Diagram

- For ADC configure register KPC\_EN (ADC\_CONF[9]) should be set to 1.
- Take ADC2 as input, and select AVDD33 and AGND33 as the reference.
- Res1 ≤ 20K ohm and Res2 < 5.6 \* Res1.</p>
- A 0.01uF cap is at ADC2 on board.
- If doesn't need the interrupt, please ignore the requirement for Res1 and Res2.
- This kind of series R scheme can not support multi-key function

#### Interface for 4-wire

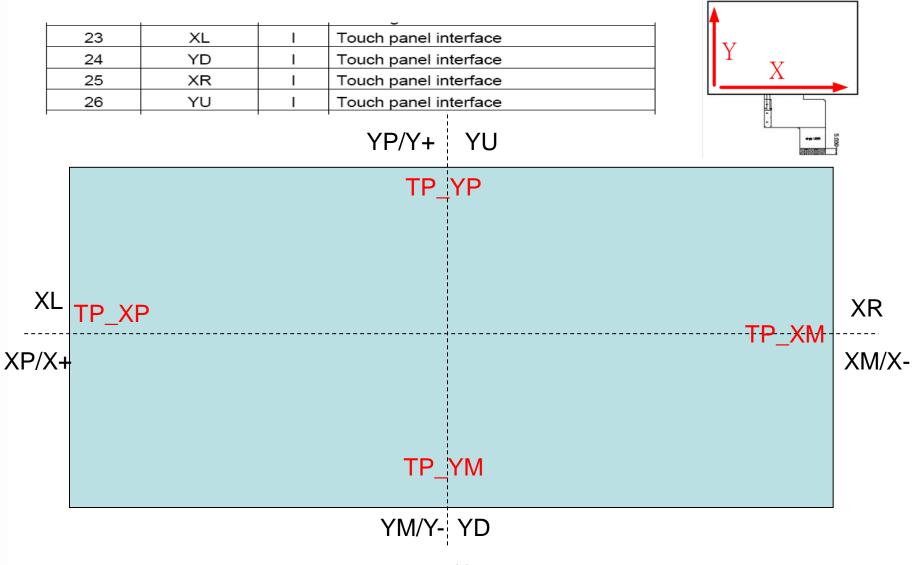
- ➤ For ADC configure register T\_EN (ADC\_CONF[0]) should be set to 1.
- ➤ ADC control register WMSWCH (ADC\_CTL[16]=0) (Wire Mode Switch) for 4-wire configuration.
- ➤ The following figures show the interface for 4-wire touch screen.



4-wire Touch Screen Connection Diagram

Note that 4 switches to bias XP, XM, YP, YM have conduction resistance under 5 ohm. And the pull up PMOS have 200K ohm typically.

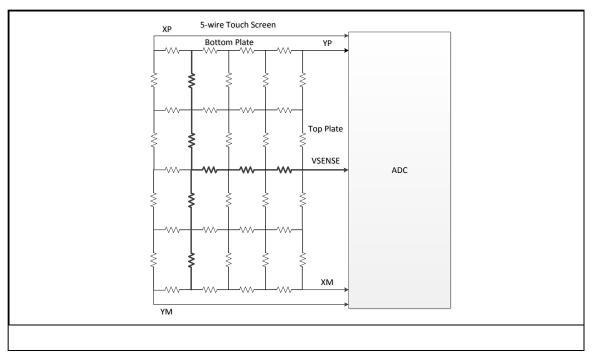
### **4-W TP Connection**



Front

#### Interface for 5-wire

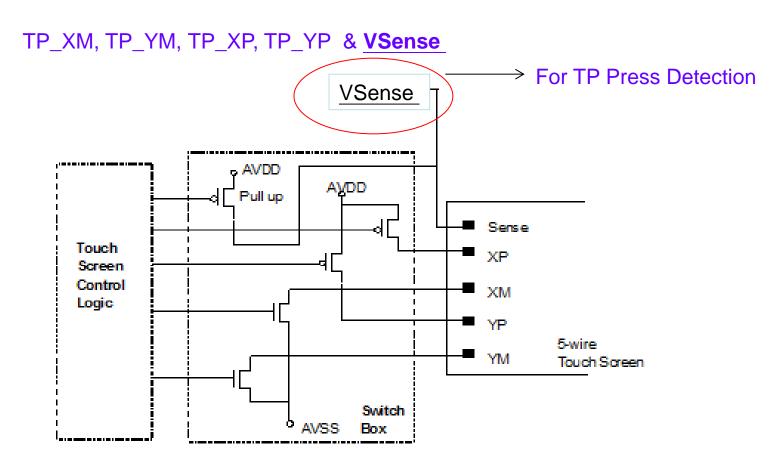
- ➤ For ADC configure register T\_EN (ADC\_CONF[0]) should be set to 1.
- > ADC control register WMSWCH (ADC\_CTL[16]=1) (Wire Mode Switch) for 5-wire configuration.
- > The following figures show the interface for 5-wire touch screen.



5-wire Touch Screen Connection Diagram

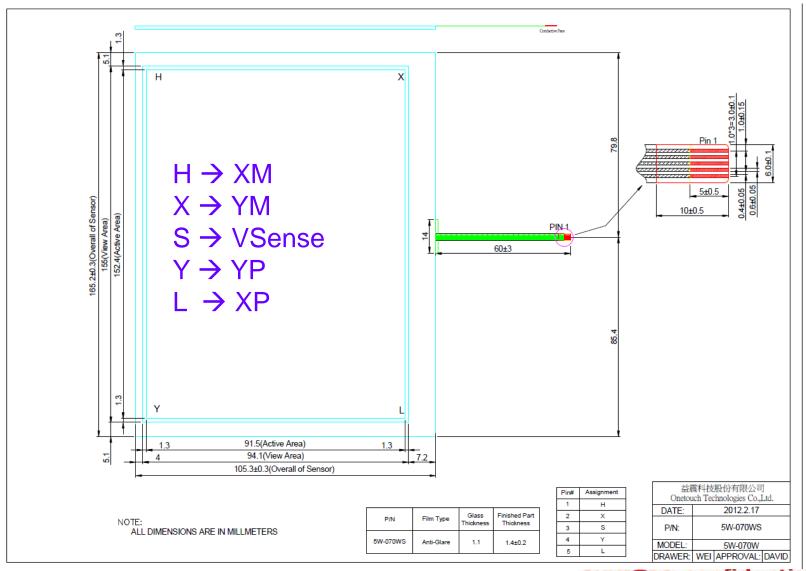
Note that 4 switches to bias XP, XM, YP, YM have conduction resistance under 5 ohm. And the pull up PMOS have 200K ohm typically.

### 5-W Touch Connection



Advantage: Reliability & life time are good than 4W

#### 5-W TP Reference Data



# **Analog Characteristics**

Symbol	Parameter	Min.	Тур.	Max.	Unit	Test Conditions
-	Resolution	-	12	-	Bit	
DNL	Differential Nonlinearity Error	•	±1	-	LSB	V <sub>REF</sub> is external AVREF pin
INL	Integral Nonlinearity Error	1	-1.2	-	LSB	V <sub>REF</sub> is external AVREF pin
Eo	Offset Error	•	+3.7	-	LSB	V <sub>REF</sub> is external AVREF pin
Eg	Gain Error (Transfer Gain)	-	-6.6	-	LSB	V <sub>REF</sub> is external AVREF pin
EA	Absolute Error	-	4.2	-	LSB	V <sub>REF</sub> is external AVREF pin
-	Monotonic		Guaranteed			
F <sub>ADC</sub>	ADC Clock Frequency	•	-	16	MHz	
T <sub>CAL</sub>	Calibration Time	-	3	\	Clock	
Ts	Sample Time	•	17	-	Clock	
T <sub>ADC</sub>	Conversion Time	1	20		Clock	
Fs	Sample Rate	1	-	800[1]	k SPS	
V <sub>AVDD</sub>	Supply Voltage	2.7	3.3	3.6	V	
I <sub>DDA1</sub>	Supply Current (Avg.)		1.2		mA	ADC1 channel high speed mode
I <sub>DDA2</sub>	Supply Current (Avg.)	-)	1.0		mA	ADC1 channel low speed mode
I <sub>DDA3</sub>	Supply Current (Avg.)	-	0.4		mA	
I <sub>LK</sub>	Leakage Current	-	0.1	-	uA	
V <sub>REF</sub>	Reference Voltage	2	-	V <sub>AVDD</sub>	٧	
V <sub>IN</sub>	Analog Input Voltage	0	-	V <sub>REF</sub>	٧	
R <sub>IN</sub>	Analog Input Impedance	-	-	2	MΩ	
C <sub>IN</sub>	Capacitance	-	25.6		pF	

Note. ADC1 channel supports sample rate higher than 200 kSPS. Other ADC channels support sampel rate up to 200 kSPS.