NUC972
Power Sequence

Nuvoton Technology Corp.

Process concerns

- In standard IO, different voltages are supplied to the pre-driver (lower voltage) and post-driver (higher voltage).
- Because of the multi-power ESD (Electro Static Discharge) structure, there is a parasitic forward diode path from core power rail.
- I/O power rail (VD33) as shown in Fig.3 the diode in red, if the core (lower) voltage is powered up earlier than the I/O (higher) voltage without care, there will be current flowing through the parasitic diode that may trigger latch-up.
- So user should to avoid this problem occurring, when system power up/down.

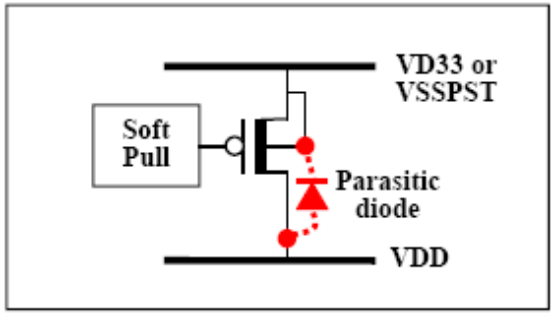


Fig. 3 Parasitic diode between core and I/O power rails

Power Up/Down Sequence

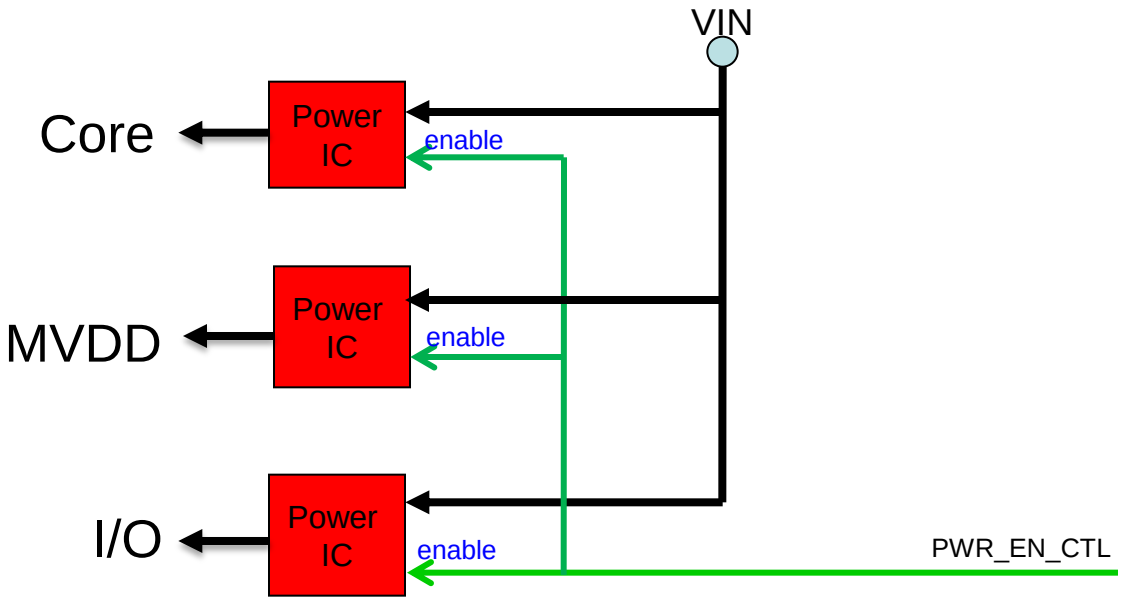
- Power Up sequence
  - Higher Voltage (3.3V) is early than MVDD (1.8V) and Core(1.2V)
  - Sequence: $T_{33} \geq T_{18} \geq T_{12}$
  - The time delay gap T_{33} with T_{12}, 0mS is recommend
  - The time delay gap T_{18} with T_{12}, 0mS is recommend

- Power Down Sequence
  - The lower voltage (1.2V) should be powered down first and then the higher one (3.3V)
  - Sequence: $T_{12} \geq T_{18} \geq T_{33}$

Note.

- T_{12} means 1.2V powered time for Core & PLL
- T_{18} means 1.8V powered time for MVDD
- T_{33} means 3.3V powered time for digital IO and analog IO

Recommended Connection for Power IC enable CTL of IO, MVDD & Core



Power Sequence Relationship