REVISION HISTORY

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Revision	Description	Date	Drawn	Checked
Ver 0.5	Initial Version	2016-12-26	HJ	
Ver 0.8		2017-02-23	HJ	
Ver 0.9		2017-03-22	HJ	
Ver 1.0	1.增加电阻,连通VCC18-RTC 和 VDD18-LPDDR	2018-03-20		

2. 将HDMI和CAMERA处的SDA SCK网络进行调整,H6分两组来控制HDMI和CAMERA.

3.将H6 的PG14脚悬空。

4.主控处的电压改接成BLD01,之前是与DDR3共用。 5.将CAMERA与HDMI_IN处复用的网络用0R电阻分开接出,PCB中绕线更短。

6.将之前40PIN座子修改成26PIN 7.新增USB3.0_HUB功能

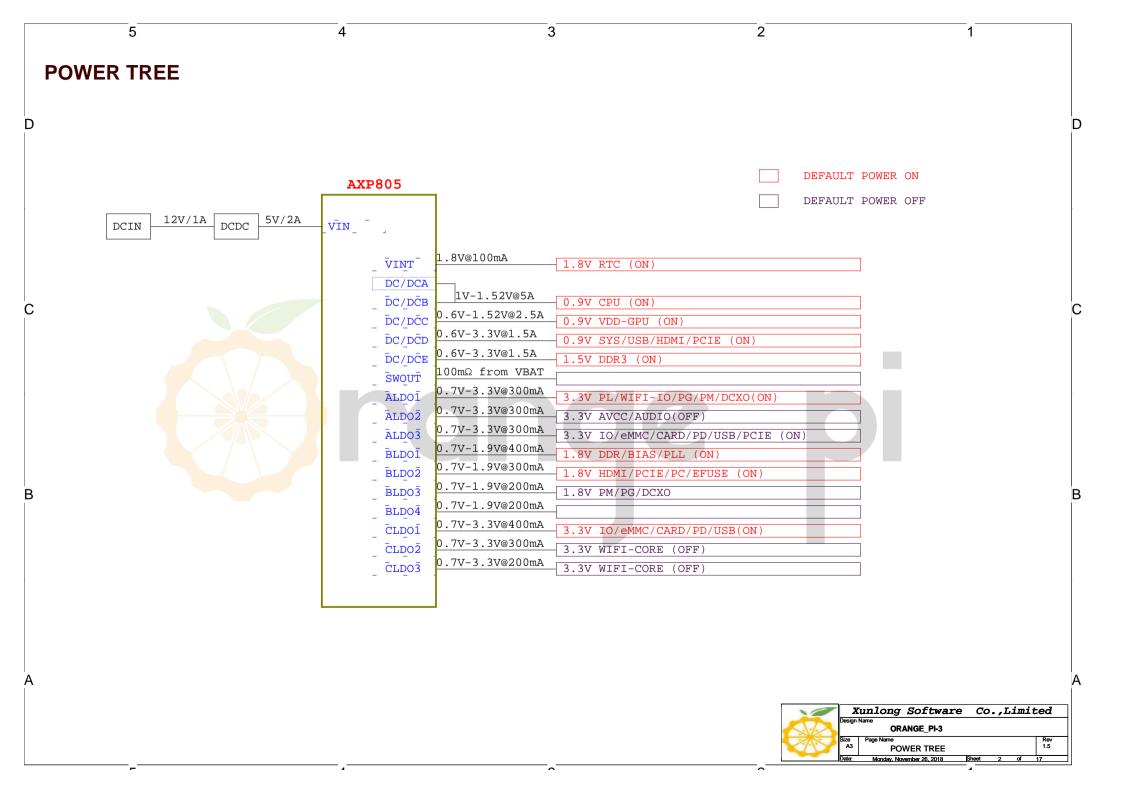
8.新增千兆网口模块

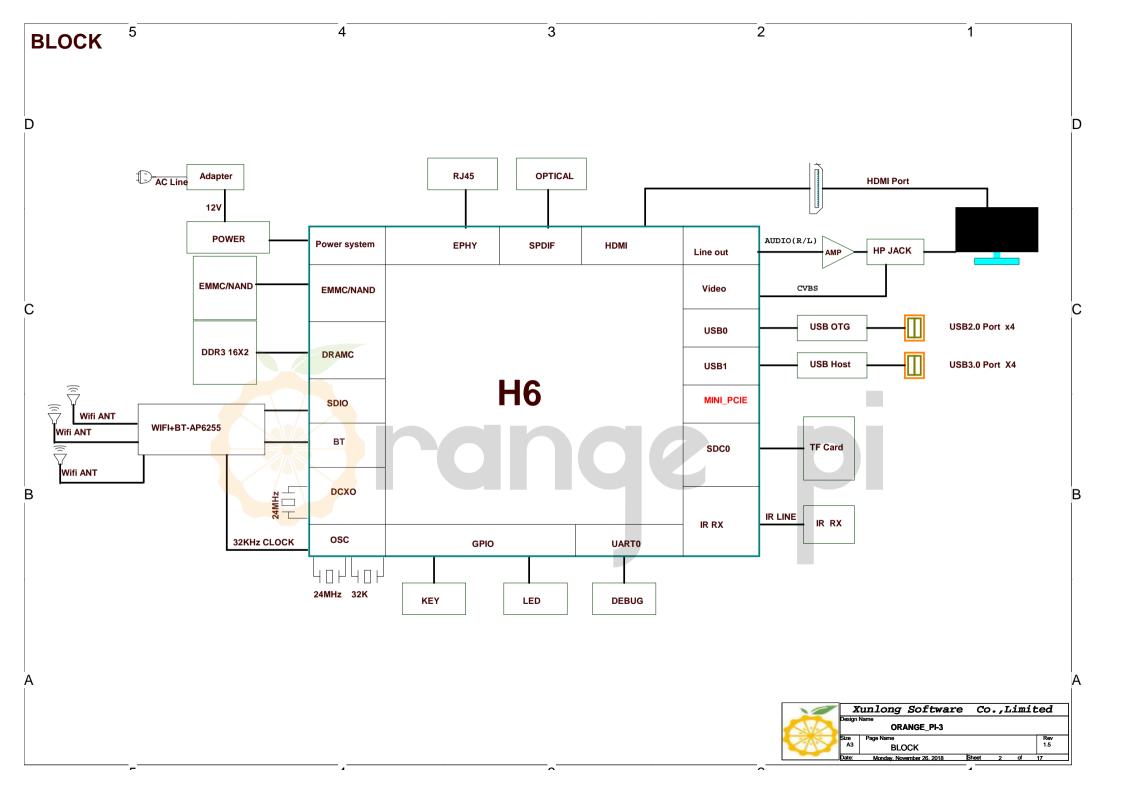
9. 12页去掉AUDIO部分的放大电路模块,左右声道各加一个电阻和电容 10.13页 USB3.0去掉EERPOM模块

Ver 1.1

11.13页 USB3.0接口处的OR电阻去掉,修改TX->RX网络,ESD器件预留0402的封装,VCC18-RTC与VDD18-LPDDR网络通过OR电阻连接

Xunlong Software Co., Limited ORANGE PI-3 Rev 1.5 REVISION HISTORY Monday, November 26, 2018





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3		

PIN	Define	CFG	Function
PC0	NAND_WE	2	
PC1	NAND_ALE/SDC2_DS	2/3	
PC2	NAND_CLE	2	
PC3	NAND_CE0	2	
PC4	NAND_RE/SDC2_CLK	2/3	
PC5	NAND_RB0/SDC2_CMD	2/3	
PC6	NAND_DQ0/SDC2_D0	2/3	
PC7	NAND_DQ1/SDC2_D1	2/3	NAND/eMMC
PC8	NAND_DQ2/SDC2_D2	2/3	
PC9	NAND_DQ3/SDC2_D3	2/3	
PC10	NAND_DQ4/SDC2_D4	2/3	
PC11	NAND_DQ5/SDC2_D5	2/3	
PC12	NAND_DQ6/SDC2_D6	2/3	
PC13	NAND_DQ7/SDC2_D7	2/3	
PC14	NAND_DQS/SDC2_RST	2/3	
PC15	NAND_CE1	2	
PC16	NAND_RB1	2	

PD0		Function
100		
PD1		
PD2		
PD3		
PD4		
PD5		
PD6		
PD7		
PD8		
PD9		
PD10		
PD11		
PD12		
PD13		
PD14		

PIN	Define	CFG	Function
PD15			
PD16			
PD17			
PD18			1
PD19			
PD20			
PD21			
PD22			
PD23			
PD24			
PD25			
PD26			

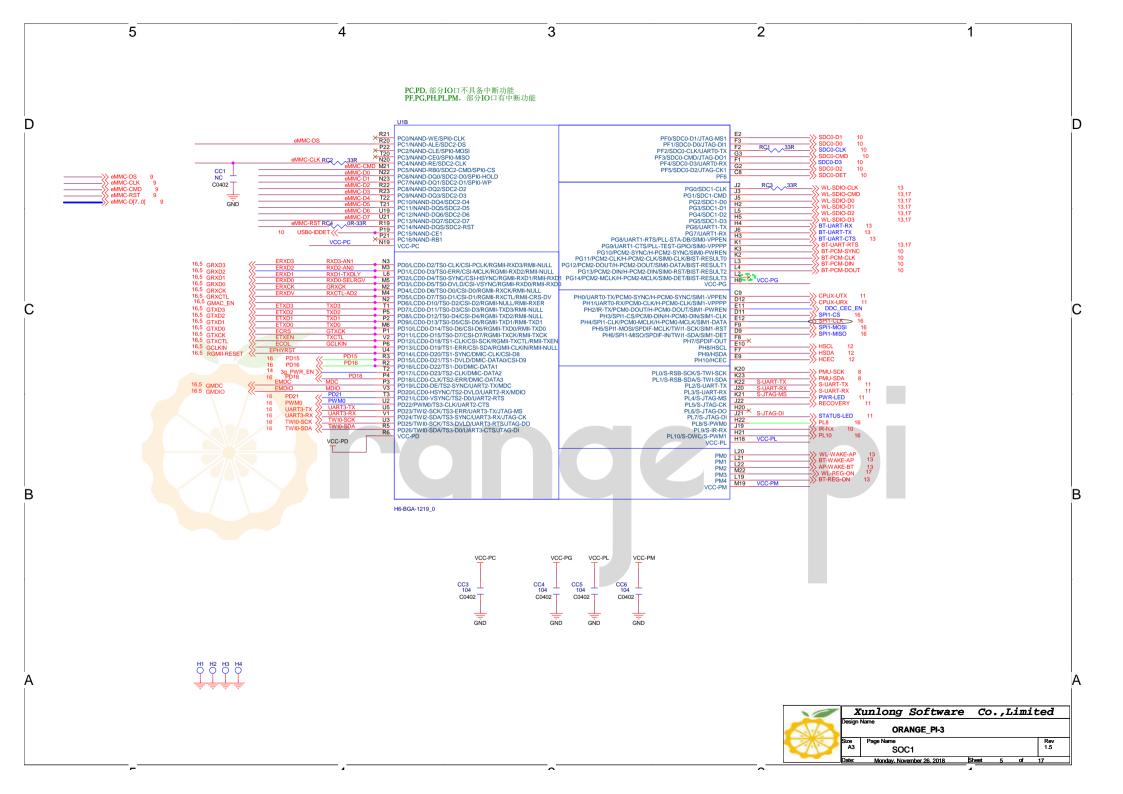
PIN	Define	CFG	Function
PG0	SDC1_CLK	2	
PG1	SDC1_CMD	2	
PG2	SDC1_D0	2	
PG3	SDC1_D1	2	
PG4	SDC1_D2	2	
PG5	SDC1_D3	2	
PG6	UART1_TX	2	WIFI+BT
PG7	UART1_RX	2	WIFI+BI
PG8	UART1_RTS	2	
PG9	UART1_CTS	2	
PG10	PCM2_SYNC	2	
PG11	PCM2_CLK	2	
PG12	PCM2_DOUT	2	1
PG13	PCM2_DIN	2	1
PG14			

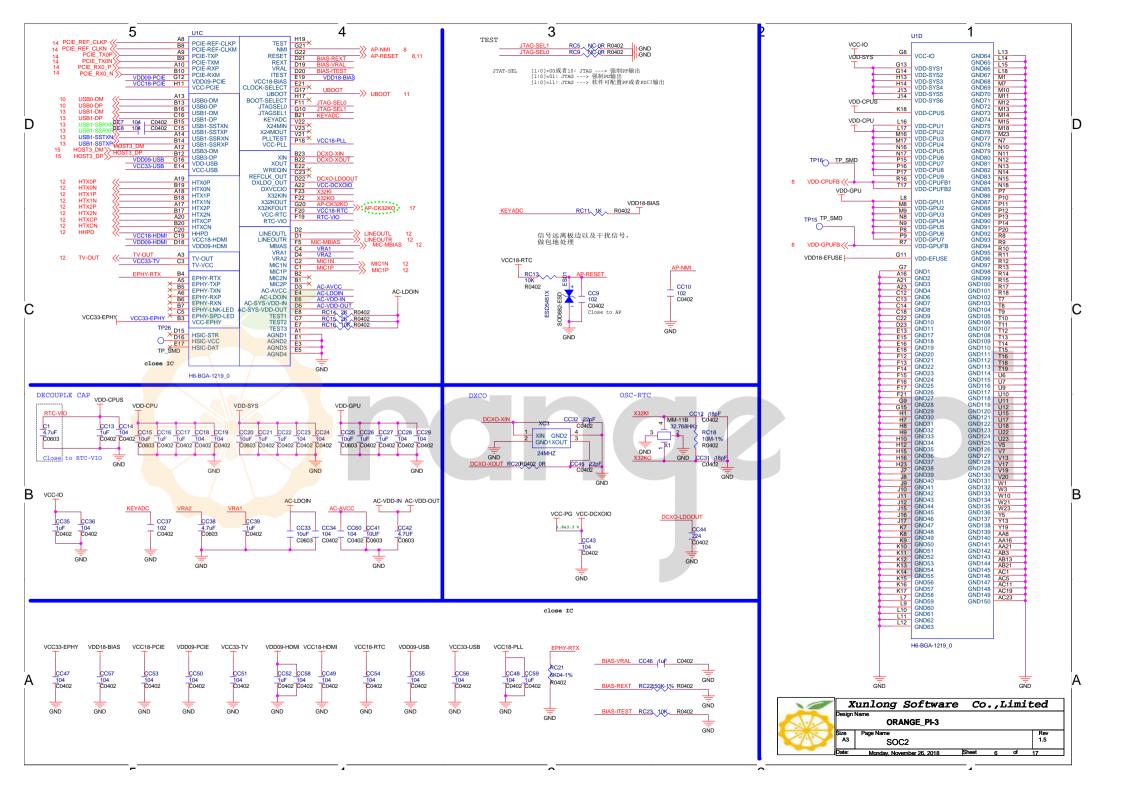
PIN	Define	CFG	Function
PF0	SDC0_D1	2	
PF1	SDC0_D0	2	
PF2	SDC0_CLK/UART0_TX	2/3	
PF3	SDC0_CMD	2	CARD0
PF4	SDC0_D3/UART0_RX	2/3	
PF5	SDC0_D2	2	
PF6	SDC0-DET	2	

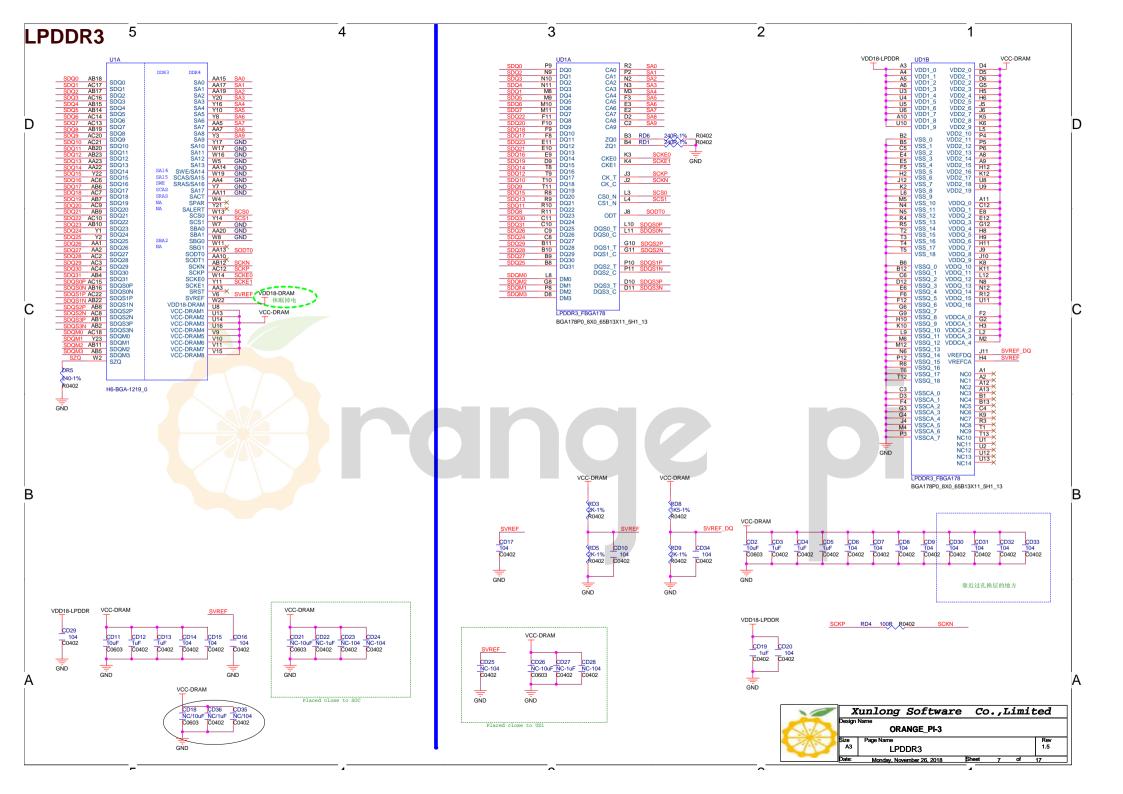
PIN Define CFG Function PH0 CPUX-UTX 2 PH1 CPUX-URX 2 PH2				
PH1 CPUX-URX 2 PH2 PH3 PH4 PH5 PH6 PH7 SPDIF_OUT 3 PH8 HSCL 2 PH9 HSDA 2 HDMI	PIN	Define	CFG	Function
PH2 PH3 PH4 PH5 PH6 PH7 SPDIF_OUT 3 PH8 HSCL 2 PH9 HSDA 2 HDMI	PH0	CPUX-UTX	2	
PH3 PH4 PH5 PH6 PH7 SPDIF_OUT 3 PH8 HSCL 2 PH9 HSDA 2 HDMI	PH1	CPUX-URX	2	
PH4 PH5 PH6 PH7 SPDIF_OUT 3 PH8 HSCL 2 PH9 HSDA 2 HDMI	PH2			
PH5 PH6 PH7 SPDIF_OUT 3 PH8 HSCL 2 PH9 HSDA 2 HDMI	PH3			
PH6	PH4			
PH7 SPDIF_OUT 3 PH8 HSCL 2 PH9 HSDA 2 HDMI	PH5			
PH8 HSCL 2 PH9 HSDA 2 HDMI	РНб			
PH9 HSDA 2 HDMI	PH7	SPDIF_OUT	3	
	PH8	HSCL	2	
PH10 HCEC 2	PH9	HSDA	2	HDMI
	PH10	HCEC	2	

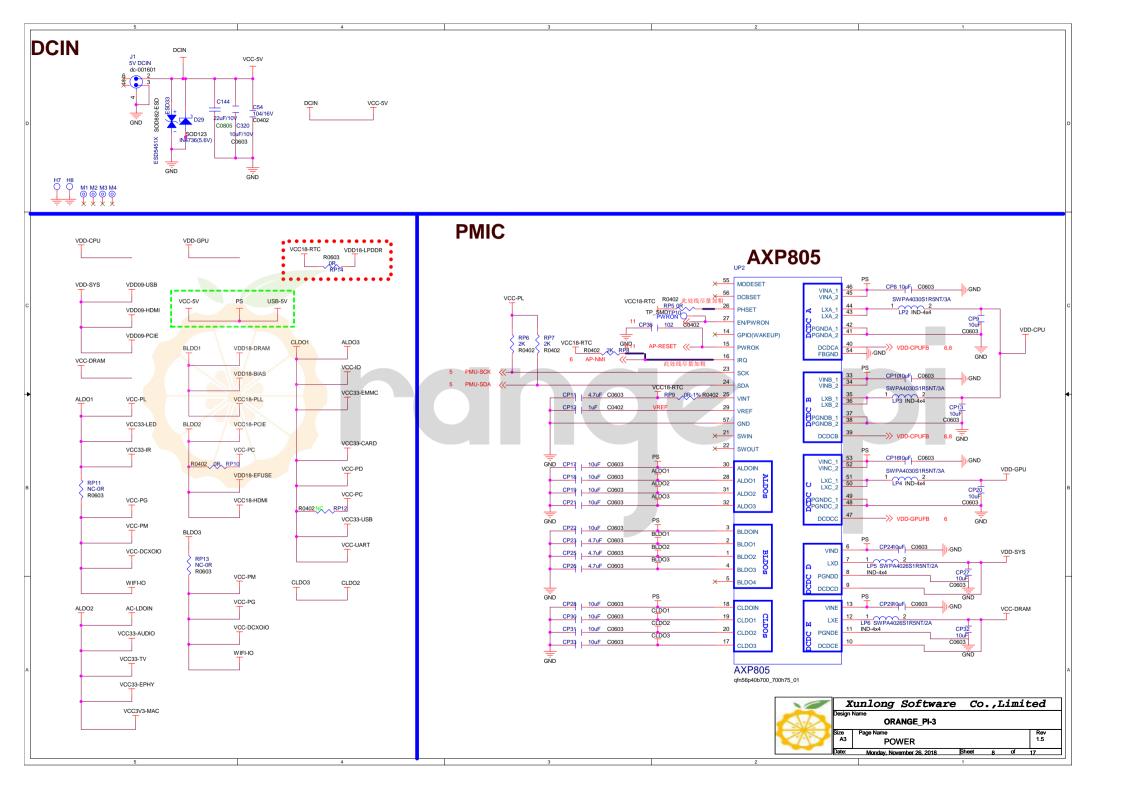
PIN	Define		CFG	Function
PL0	PMU-SCK		3	
PL1	PMU-SDA		3	
PL2	RECOVERY		2	
PL3	LINK-LED		1	
PL4	PWR-LED		1	
PL5	USB0-DRVVBUS		1	
PL6	MUTE		1	
PL7	STATUS-LED		1	
PL8				
PL9	IR-RX		2	
PL10	BT-WIFI-ON		1	
PM0	WL-WAKE-AP		0	
PM1	BT-WAKE-AP		0	
PM2	AP-WAKE-BT		1	WIFI+BT
PM3	WL-REG-ON		1	MILITEI
PM4	BT-REG-ON		1	

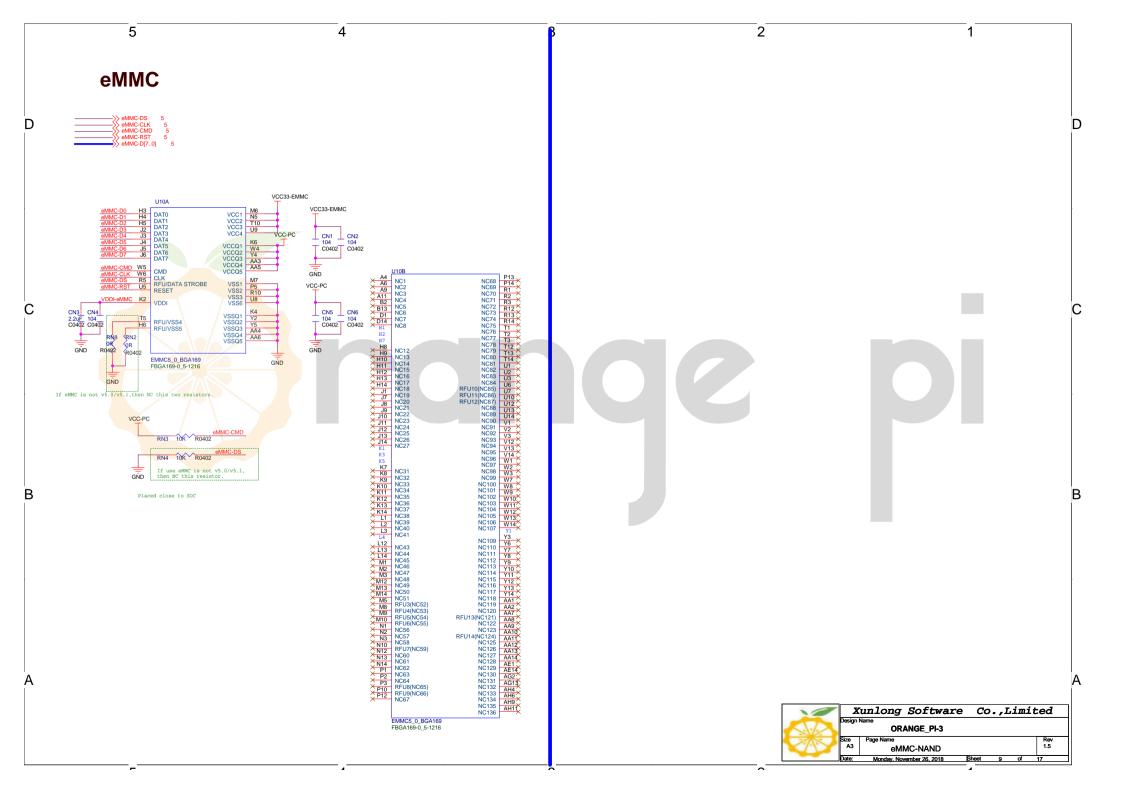
Xunlong Software Co., Limited ORANGE_PI-3 GPIO

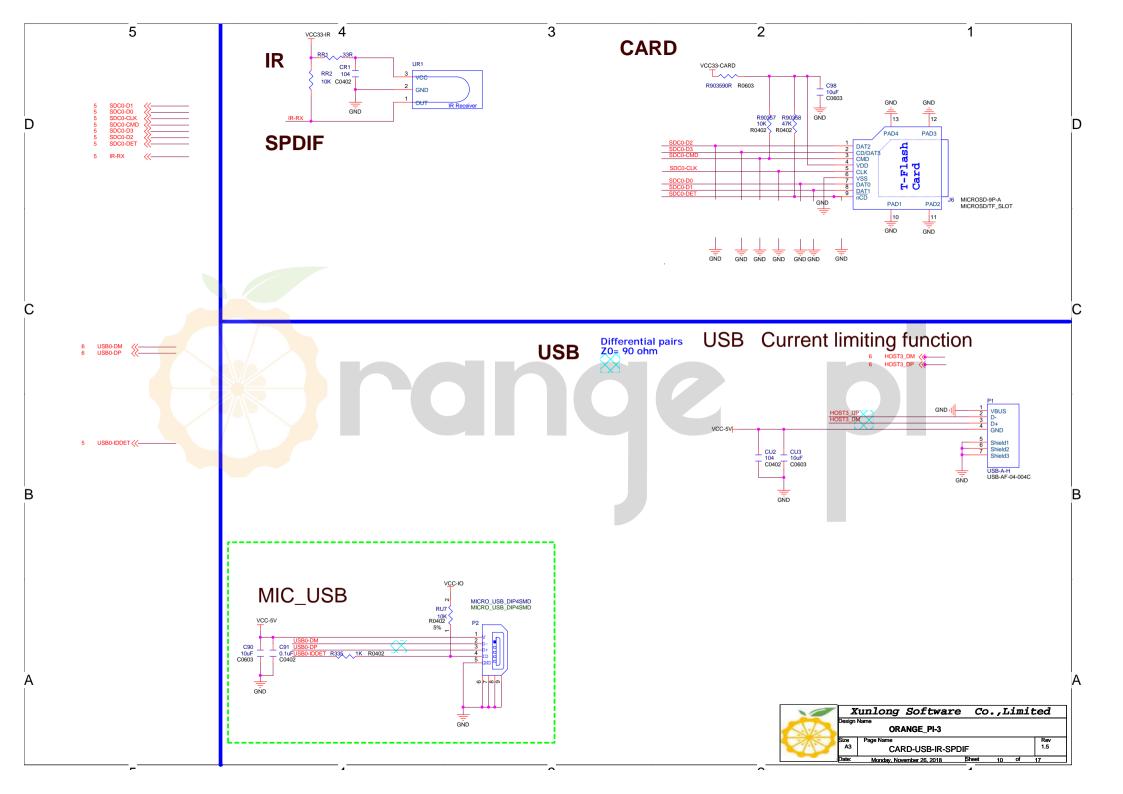


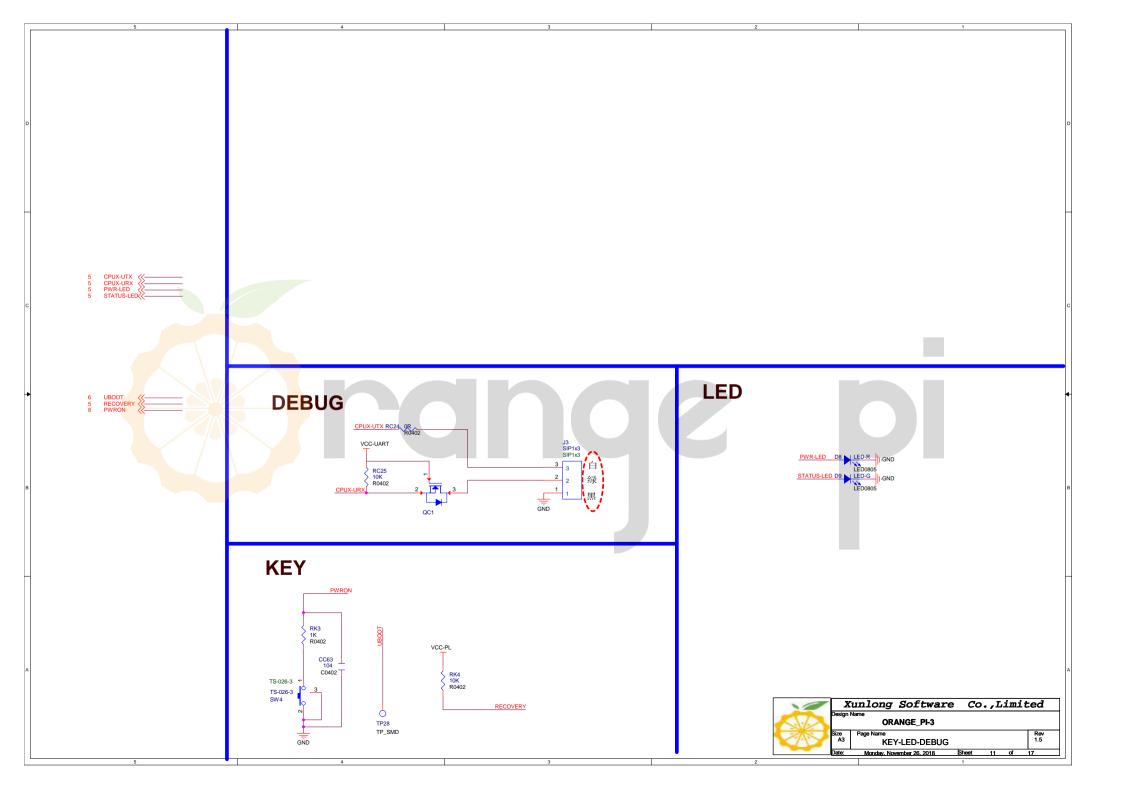


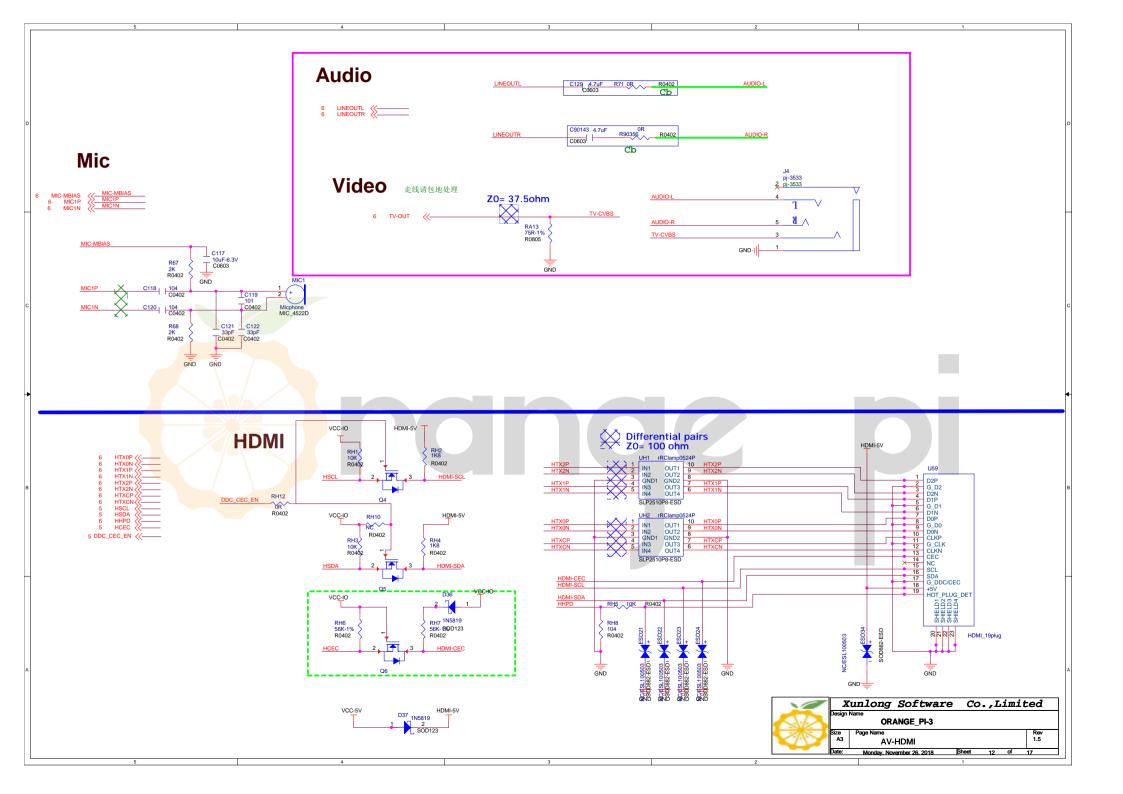


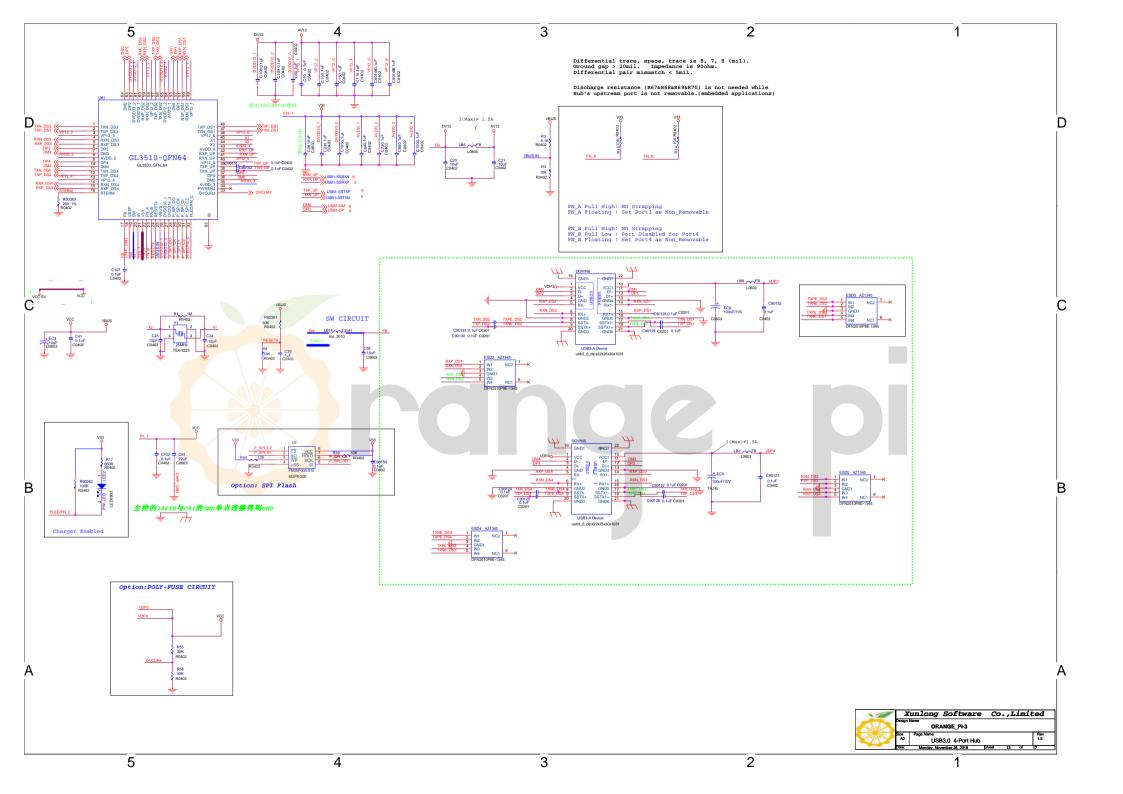


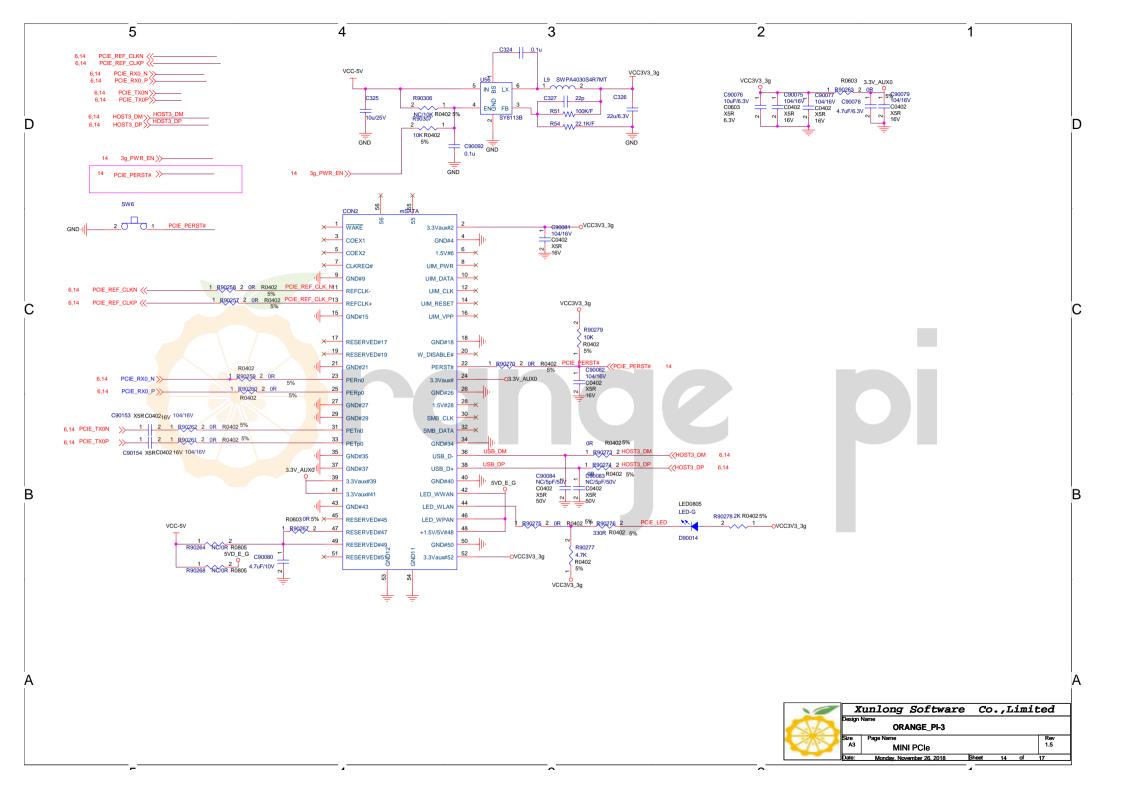


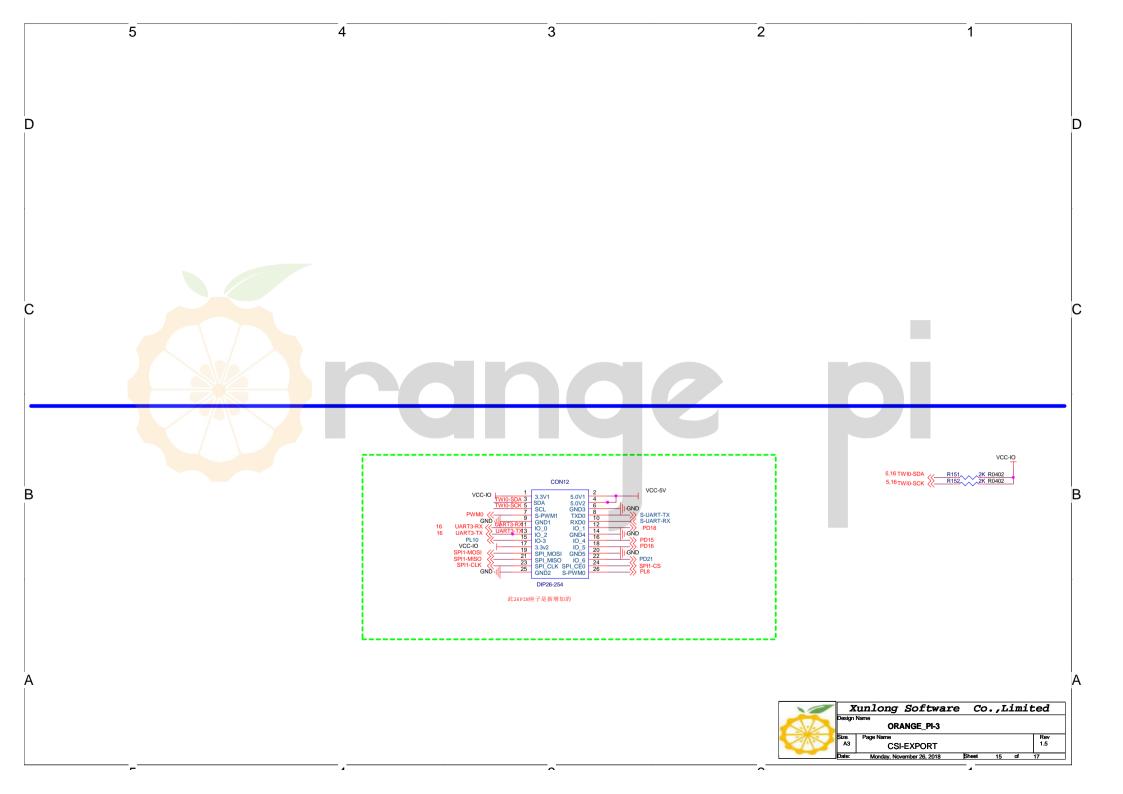


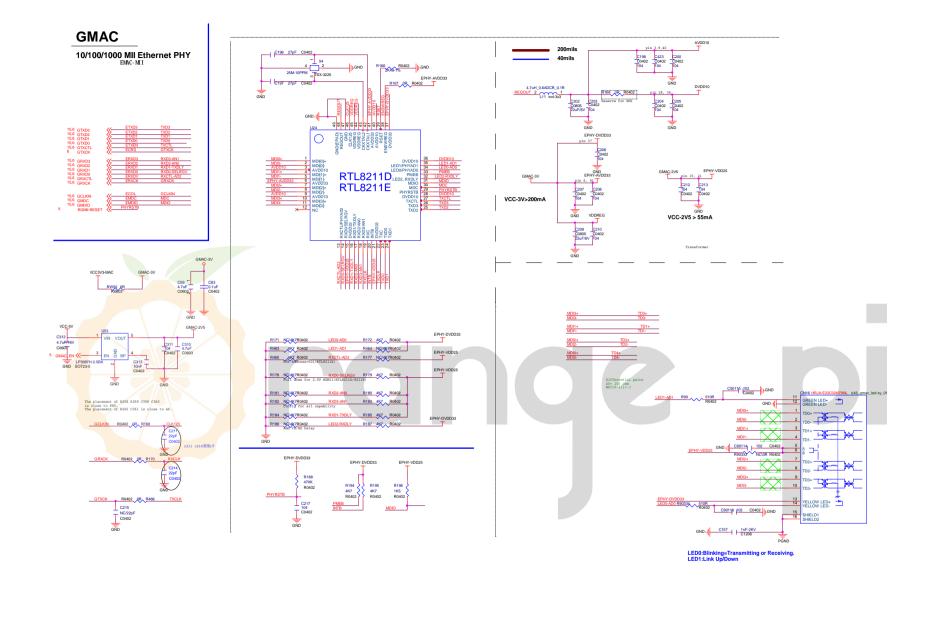


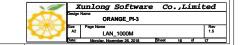


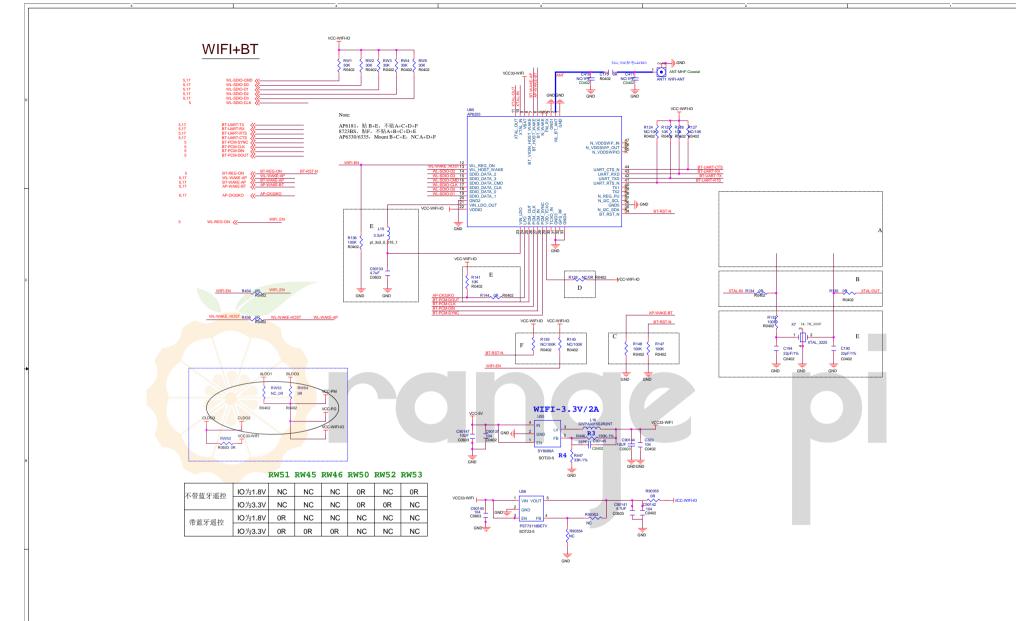












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	Size	Rev 1.5
Street, Square, Square	Date: Monday, November 26, 2018 Sheet 17	of 17