REVISION HISTORY

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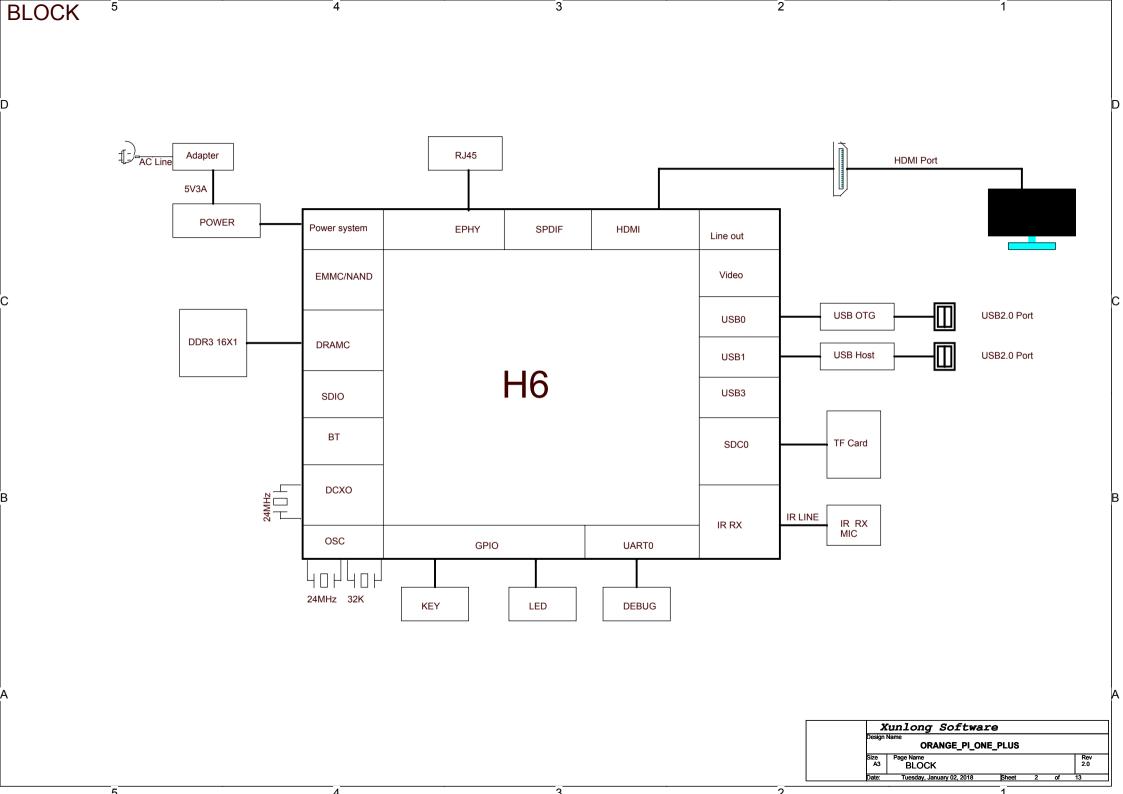
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Ver 0.5 Initial Version 2016-12-26 Ver 2.0 2017-11-27 P01: REVISION HISTORY P02: BLOCK

Revision Description Checked Date Drawn НJ НJ

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POWER TREE

DEFAULT POWER ON AXP805 DEFAULT POWER OFF 12V/1A 5V/2A DCIN VIN .8V@100mA VINT 1.8V RTC (ON) DC/DCA 1V-1.52V@5A DC/DCB 0.9V CPU (ON) 0.6V-1.52V@2.5A 0.9V VDD-GPU (ON) DC/DCC 0.6V-3.3V@1.5A DC/DCD 0.9V SYS/USB/HDMI/PCIE (ON) 0.6V-3.3V@1.5A .5V DDR3 (ON) DC/DCE $100m\Omega$ from VBAT SWOUT 0.7V-3.3V@300mA ALD01 3.3V PL/WIFI-IO/PG/PM/DCXO(ON) 0.7V-3.3V@300mA ALDO2 3.3V AVCC/AUDIO(OFF) 0.7V-3.3V@300mA 3.3V IO/eMMC/CARD/PD/USB/PCIE (ON) ALD03 0.7V-1.9V@400mA BLD01 .8V DDR/BIAS/PLL (ON) 0.7V-1.9V@300mA 1.8V HDMI/PCIE/PC/EFUSE (ON) BLD02 0.7V-1.9V@200mA BLD03 1.8V PM/PG/DCXO 0.7V-1.9V@200mA BLD04 0.7V-3.3V@400mA 3.3V IO/eMMC/CARD/PD/USB(ON) CLD01 0.7V-3.3V@300mA CLD02 3.3V WIFI-CORE (OFF) 0.7V-3.3V@200mA CLD03 3.3V WIFI-CORE (OFF)

 Xunlong Software

 Design Name
 ORANGE_PI_ONE_PLUS

 Size A3
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GPIO ASSIGNMENT

PIN Define CFG Function PCO NAND WE PC1 NAND ALE/SDC2 DS 2/3 PC2 NAND CLE PC3 NAND CE0 PC4 NAND RE/SDC2 CLK 2/3 PC5 NAND RB0/SDC2 CMD 2/3 PC6 NAND DQ0/SDC2 D0 2/3 PC7 NAND DQ1/SDC2 D1 2/3 NAND/eMMC PC8 NAND DQ2/SDC2 D2 2/3 PC9 NAND DQ3/SDC2 D3 2/3 PC10NAND DQ4/SDC2 D4 2/3 PC11 NAND DQ5/SDC2 D5 2/3 PC12NAND DQ6/SDC2 D6 2/3 PC13NAND_DQ7/SDC2_D7 2/3 PC14NAND DQS/SDC2 RST 2/3 PC15NAND CE1 PC16NAND RB1

| PIN | Define | CFG | Function |
|------|--------|-----|----------|
| PD0 | | | |
| PD1 | | | |
| PD2 | | | |
| PD3 | | | |
| PD4 | | | |
| PD5 | | | |
| PD6 | | | |
| PD7 | | | |
| PD8 | | | |
| PD9 | | | |
| PD10 | | | |
| PD11 | | | |
| PD12 | | | |
| PD13 | | | |
| PD14 | | | |
| | | | |

| PIN | Define | CFG | Function |
|------|--------|-----|----------|
| PD15 | | | |
| PD16 | | | 1 |
| PD17 | | | 1 |
| PD18 | | | 1 |
| PD19 | | | 1 |
| PD20 | | | |
| PD21 | | | |
| PD22 | | | |
| PD23 | | | 1 |
| PD24 | | | 1 |
| PD25 | | | 1 |
| PD26 | | | |

| PIN | Define | CFG | Function |
|------|-----------|-----|----------|
| PG0 | SDC1_CLK | 2 | |
| PG1 | SDC1_CMD | 2 | |
| PG2 | SDC1_D0 | 2 | |
| PG3 | SDC1_D1 | 2 | |
| PG4 | SDC1_D2 | 2 | |
| PG5 | SDC1_D3 | 2 | |
| PG6 | UART1_TX | 2 | WIFT+BT |
| PG7 | UART1_RX | 2 | WILITEL |
| PG8 | UART1_RTS | 2 | |
| PG9 | UART1_CTS | 2 | |
| PG10 | PCM2_SYNC | 2 | |
| PG11 | PCM2_CLK | 2 | |
| PG12 | PCM2_DOUT | 2 | |
| PG13 | PCM2_DIN | 2 | |
| PG14 | l | | 1 |

| PIN | Define | CFG | Function |
|-----|-------------------|-----|----------|
| PF0 | SDC0_D1 | 2 | |
| PF1 | SDC0_D0 | 2 | |
| PF2 | SDC0_CLK/UART0_TX | 2/3 | |
| PF3 | SDC0_CMD | 2 | CARD0 |
| PF4 | SDC0_D3/UART0_RX | 2/3 | |
| PF5 | SDC0_D2 | 2 | |
| PF6 | SDC0-DET | 2 | |

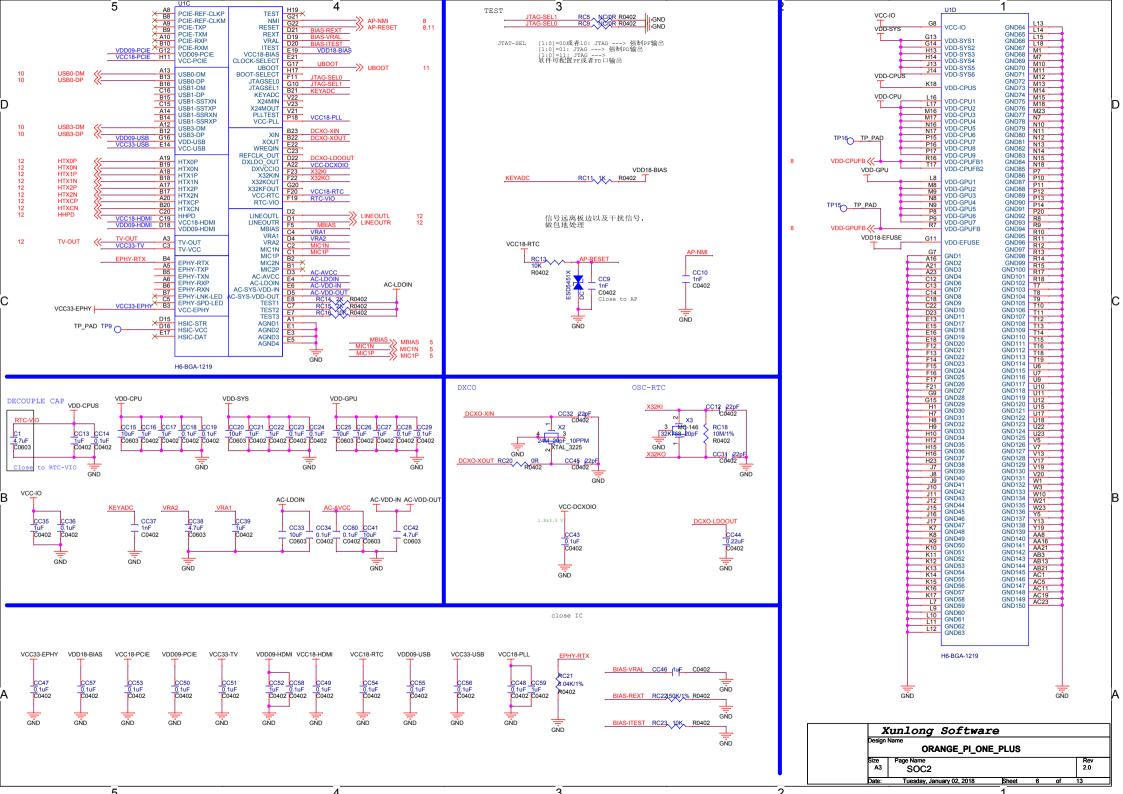
| PIN | Define | CFG | Function |
|------|-----------|-----|----------|
| PH0 | CPUX-UTX | 2 | |
| PH1 | CPUX-URX | 2 | |
| PH2 | | | |
| PH3 | | | |
| PH4 | | | |
| PH5 | | | |
| PH6 | | | |
| PH7 | SPDIF_OUT | 3 | |
| PH8 | HSCL | 2 | |
| PH9 | HSDA | 2 | HDMI |
| PH10 | HCEC | 2 | |

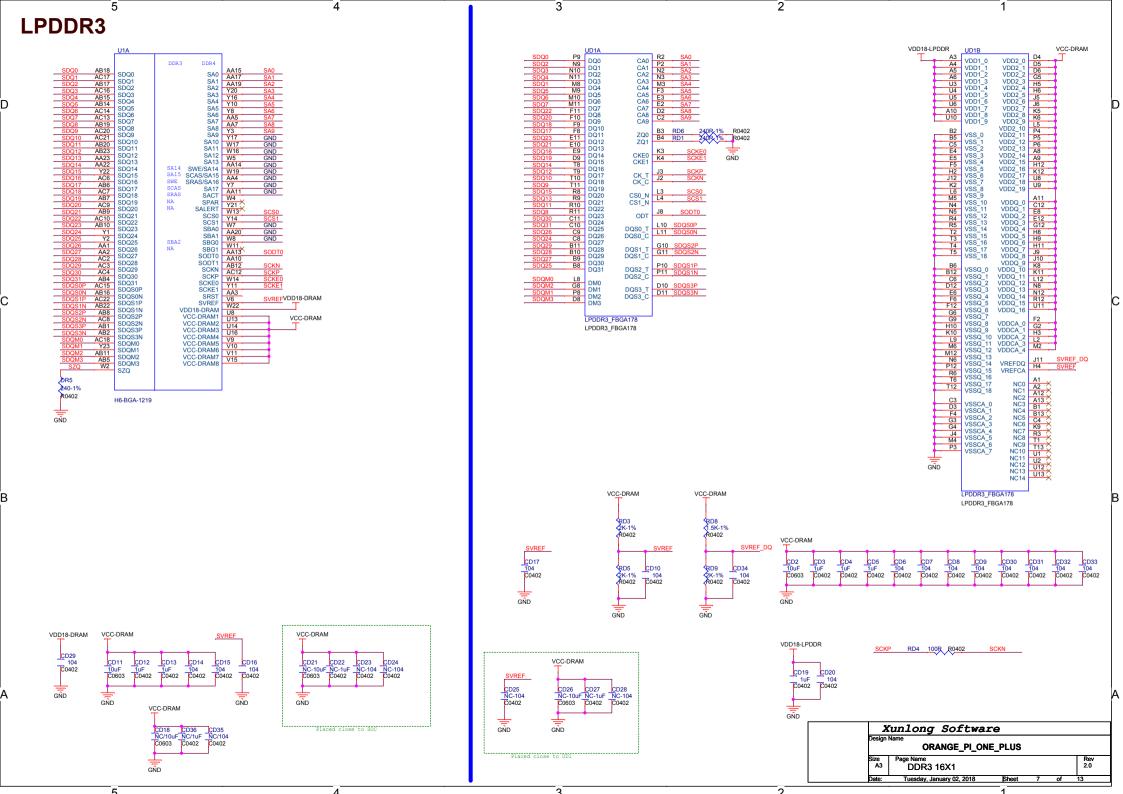
| PIN | Define | CFG | Function |
|------|--------------|-----|----------|
| PL0 | PMU-SCK | 3 | |
| PL1 | PMU-SDA | 3 | |
| PL2 | RECOVERY | 2 | |
| PL3 | LINK-LED | 1 | |
| PL4 | PWR-LED | 1 | |
| PL5 | USB0-DRVVBUS | 1 | |
| PL6 | MUTE | 1 | |
| PL7 | STATUS-LED | 1 | |
| PL8 | | | |
| PL9 | IR-RX | 2 | |
| PL10 | BT-WIFI-ON | 1 | |
| PM0 | WL-WAKE-AP | 0 | |
| PM1 | BT-WAKE-AP | 0 | WIFI+BT |
| PM2 | AP-WAKE-BT | 1 | |
| РМ3 | WL-REG-ON | 1 | MILILDI |
| PM4 | BT-REG-ON | 1 | |
| | | | |

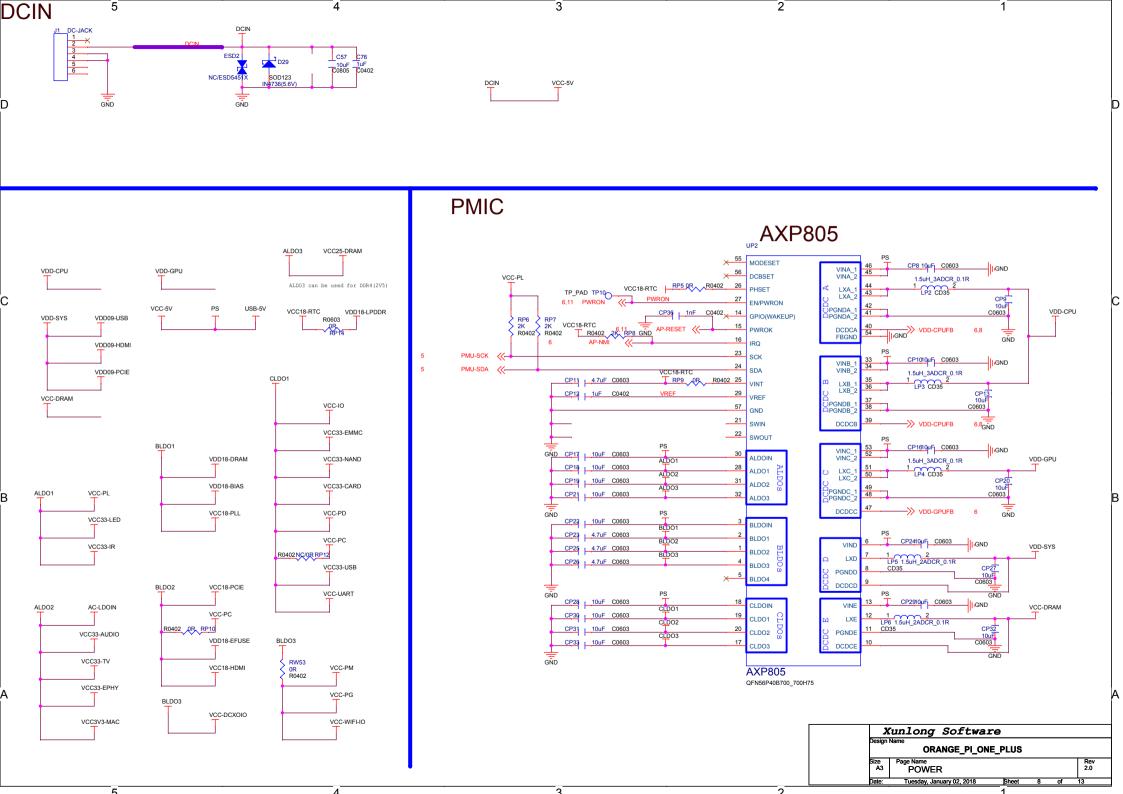
Xunlong Software ORANGE_PI_ONE_PLUS Page Name GPIO ASSIGNMENT Rev 2.0

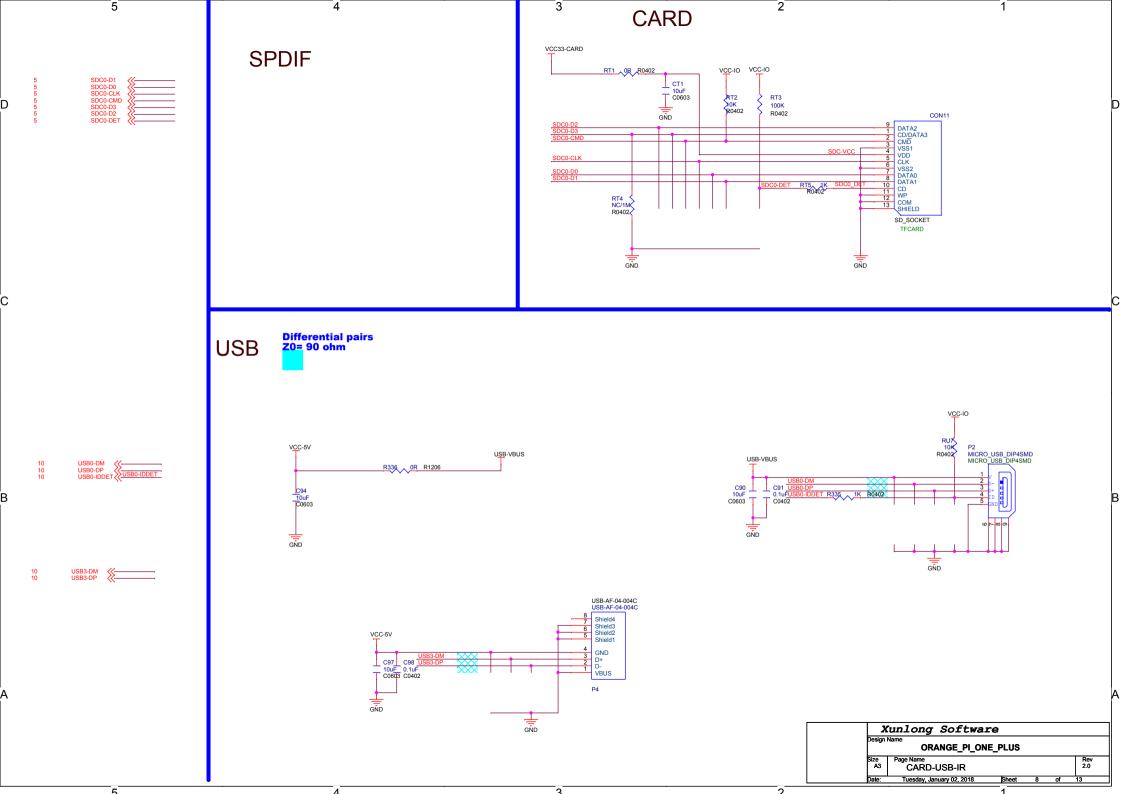
Tuesday, January 02, 2018

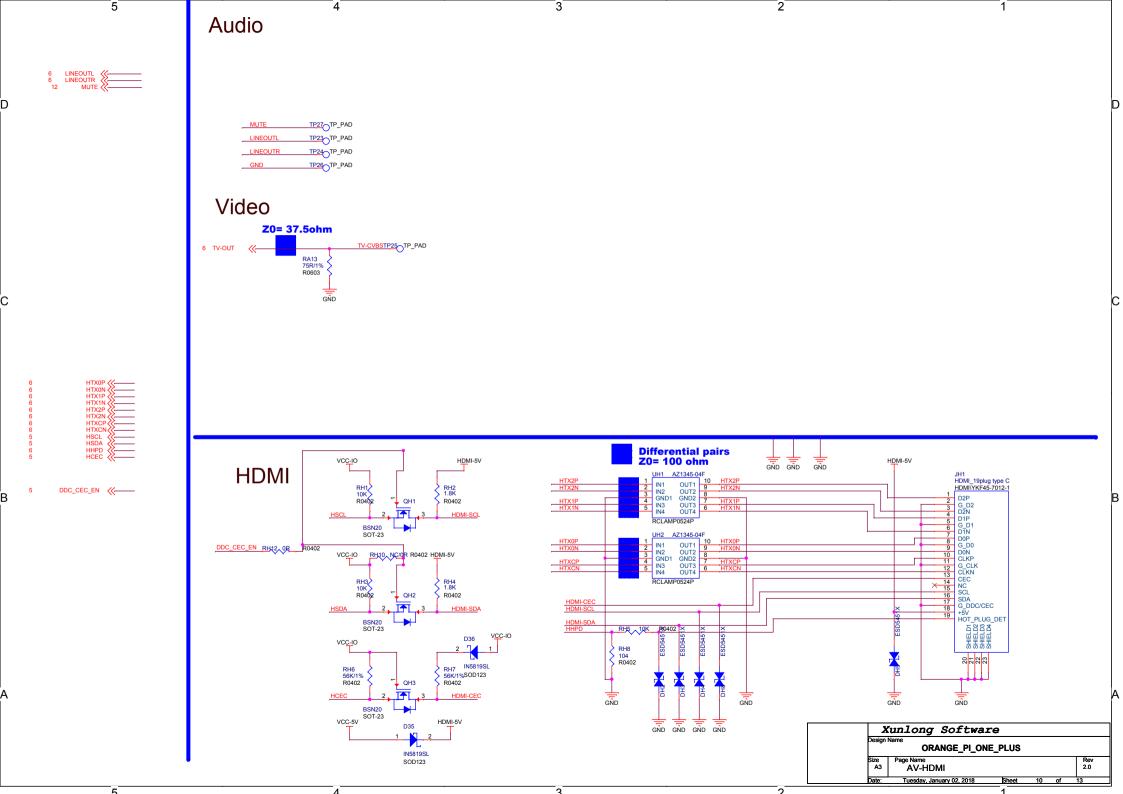
5 PC,PD, 部分IO口不具备中断功能 PF,PG,PH,PL,PM,部分IO口有中断功能 SPIO_CLK << PC0/NAND-WE/SPI0-CLK PE0/SDC0-D1/JTAG-MS1 PC1/NAND-ALE/SDC2-DS PC2/NAND-CLE/SPI0-MOSI PF1/SDC0-D0/JTAG-DI1 SDC0-D0 RC1 33R R0402 PE2/SDC0-CLK/LIART0-TX SPIO_MISO -PC3/NAND-CE0/SPI0-MISO PF3/SDC0-CMD/JTAG-DO1 SS SDC0-CMD 10 10 PC4/NAND-RE/SDC2-CLK PC5/NAND-RB0/SDC2-CMD/SPI0-CS PE4/SDC0-D3/LIARTO-RX SPI0_CS0 USB0-IDDET PF5/SDC0-D2/JTAG-CK1 PC6/NAND-DQ0/SDC2-D0/SPI0-HOLD PC7/NAND-DQ1/SDC2-D1/SPI0-WP N22 N23 R22 R23 T22 T21 U19 U21 R19 PF6 PC8 PC8/NAND-DQ2/SDC2-D2 PC9/NAND-DQ3/SDC2-D3 PG0/SDC1-CLK PG1/SDC1-CMD PC9 PC10/NAND-DQ3/3DC2-D3 PC10/NAND-DQ4/SDC2-D4 PC11/NAND-DQ5/SDC2-D5 PG2/SDC1-D0 PG3/SDC1-D1 PC12/NAND-DQ6/SDC2-D6 PG4/SDC1-D2 PC13/NAND-DQ7/SDC2-D7 PC14/NAND-DQS/SDC2-RST PG5/SDC1-D3 H5 H4 PG6/UART1-TX PC15/NAND-CF1 PG7/UART1-RX PC16/NAND-RB1 PG8/UART1-RTS/PLL-STA-DB/SIM0-VPPEN VCC-PC PG9/UART1-CTS/PLL-TEST-GPIO/SIM0-VPPPP PG10/PCM2-SYNC/H-PCM2-SYNC/SIM0-PWREN VCC-PC PG11/PCM2-CLK/H-PCM2-CLK/SIM0-CLK/BIST-RESULT1
PG12/PCM2-DOUT/H-PCM2-DOUT/SIM0-DATA/BIST-RESULT1 15,6 GRXD3 15,6 GRXD2 15,6 GRXD1 PD0/LCD0-D2/TS0-CLK/CSI-PCLK/RGMII-RXD3/RMII-NULL PD1/LCD0-D3/TS0-ERR/CSI-MCLK/RGMII-RXD2/RMII-NULL PG13/PCM2-DIN/H-PCM2-DIN/SIM0-RST/BIST-RESULT2 PD2/LCD0-D4/TS0-SYNC/CSI-HSYNC/RGMII-RXD1/RMII-RXD1 PG14/PCM2-MCLK/H-PCM2-MCLK/SIM0-DET/BIST-RESULT3 H6 × VCC-PG 15,6 GRXD0 15,6 GRXCK PD2ICLOU-04150-SYNCICSI-HSYNCI/RGMII-RXD1/RMII-RXD1 PD3ICLOD-D5/TS0-DVLO/CSI-VSYNCI/RGMII-RXD0/RMII-RXD0 PD4ICD0-D6/TS0-D0/CSI-D0/RGMII-RXCK/RMII-NULL PD5/ICD0-D1/TS0-D1/CSI-D1/RGMII-RXCTI/RMII-CRS-DV PD6/ICD0-D10/TS0-D2/CSI-D2/RGMII-NULL/RMII-RXER 15,6 GRXCK 15,6 GRXCTL GMAC_EN 15,6 GTXD3 15,6 GTXD2 ∴ CPUX-UTX PH0/UART0-TX/PCM0-SYNC/H-PCM0-SYNC/SIM1-VPPEN PH1/UART0-RX/PCM0-CLK/H-PCM0-CLK/SIM1-VPPPE 11 CPUX-URX
DDC_CEC_EN PD6/LCD0-D10/150-D2/CS1-D2/RGMII-TXD3/RMII-TXER PD7/LCD0-D11/TS0-D3/CSI-D3/RGMII-TXD3/RMII-NULL PD8/LCD0-D12/TS0-D4/CSI-D4/RGMII-TXD1/RMII-NULL PD9/LCD0-D13/TS0-D5/CSI-D5/RGMII-TXD1/RMII-TXD1 PH2/IR-TX/PCM0-DOUT/H-PCM0-DOUT/SIM1-PWREN 12 PH3/SPI1-CS/PCM0-DIN/H-PCM0-DIN/SIM1-CLK 15,6 GTXD1 PH4/SPI1-CLK/PCM0-MCLK/H-PCM0-MCLK/SIM1-DATA PWM1 15,6 GTXD1 15,6 GTXD0 6 GTXCK 15,6 GTXCTL TWI1-SCK PD10/LCD0-D14/TS0-D6/CSI-D6/RGMII-TXD0/RMII-TXD0
PD11/LCD0-D15/TS0-D7/CSI-D7/RGMII-TXCK/RMII-TXCK PH5/SPI1-MOSI/SPDIE-MCLK/TWI1-SCK/SIM1-RST PH6/SPI1-MISO/SPDIF-IN/TWI1-SDA/SIM1-DET S TWI1-SDA PD12/LCD0-D18/TS1-CLK/CSI-SCK/RGMII-TXCTL/RMII-TXEN PD13/LCD0-D19/TS1-ERR/CSI-SDA/RGMII-CLKIN/RMII-NULL PH7/SPDIF-OUT PH8/HSCL → HSCL HSDA 12 12 GCI KIN PD14/LCD0-D20/TS1-SYNC/DMIC-CLK/CSI-D8 PD15/LCD0-D21/TS1-DVLD/DMIC-DATA0/CSI-D9 PH9/HSDA S HCEC PH10/HCEC PD16/LCD0-D22/TS1-D0/DMIC-DATA1 PD17/LCD0-D23/TS2-CLK/DMIC-DATA2 → PMU-SCK PL0/S-RSB-SCK/S-TWI-SCK PD17/LCD0-CLK/TS2-ERR/DMIC-DATA3
PD19/LCD0-DE/TS2-SYNC/JVART2-TX/MDC
PD20/LCD0-HSYNC/TS2-DVLD/JVART2-RX/MDIO PL1/S-RSB-SDA/S-TWI-SDA 15,6 GMDC S RECOVERY PI 2/S-UART-TX PL3/S-UART-RX ->> PWR-LED 11 PD21 PD21/LCD0-VSYNC/TS2-D0/UART2-RTS PD22/PWM0/TS3-CLK/UART2-CTS PL4/S-JTAG-MS PD22 PL5/S-JTAG-CK UART3_TX PD23/TWI2-SCK/TS3-ERR/UART3-TX/JTAG-MS PD24/TWI2-SDA/TS3-SYNC/UART3-RX/JTAG-CK PL6/S-JTAG-DO PL7/S-JTAG-DI UART3_RX UART3_RTS STATUS-LED PD25/TWI0-SCK/TS3-DVLD/UART3-RTS/JTAG-DO PD26/TWI0-SDA/TS3-D0/UART3-CTS/JTAG-DI PL8/S-PWM0 PL9/S-IR-RX IR-RX UART3_CTS -≫IR-RX R6 PL10/S-OWC/S-PWM1 VCC-PL L20 L21 PM0 L22 M22 PM2 РМЗ PM4 M19 VCC-PM H6-BGA-1219 VCC-PC VCC-PG VCC-PL VCC-PM TP1 TP_PAD TP_PAD CC3 CC4 CC5 CC6 C0402 C0402 C0402 C0402 H2 H1 H1 H1 H1 GND GND GND GND Xunlong Software Design Name ORANGE_PI_ONE_PLUS ize A3 Page Nan Rev 2.0 SOC1 Tuesday, January 02, 2018 Sheet 5 of

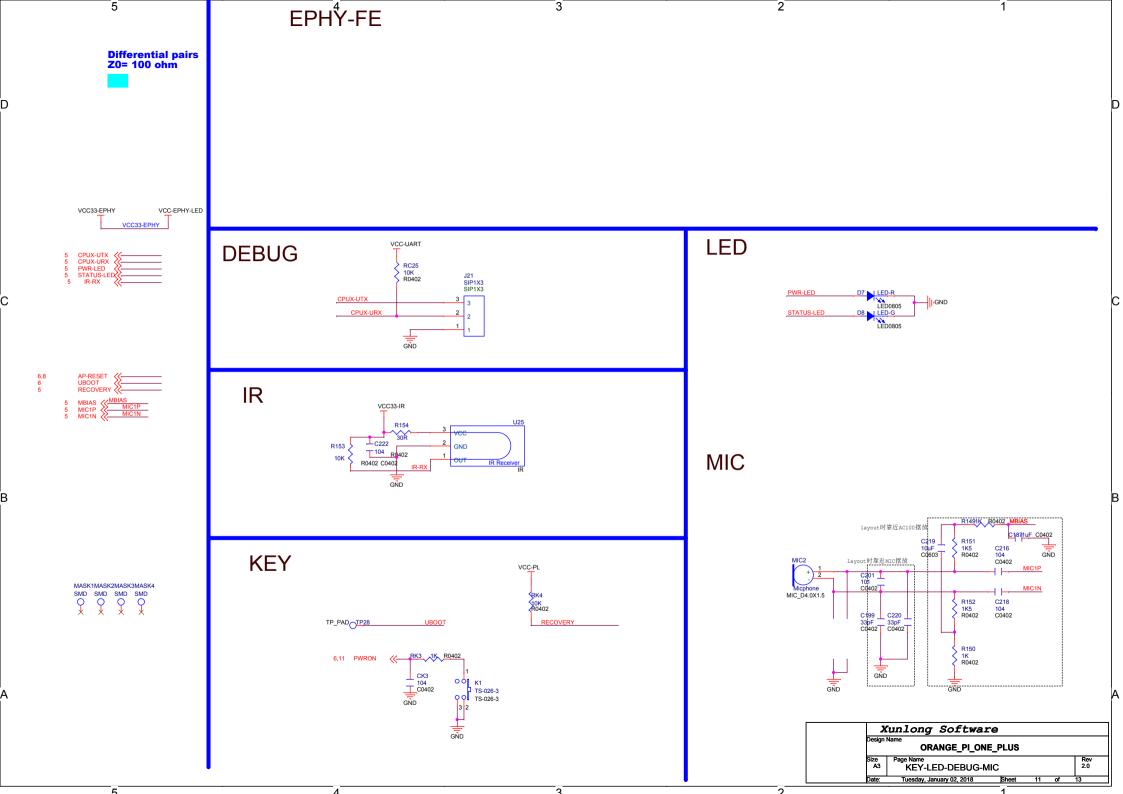


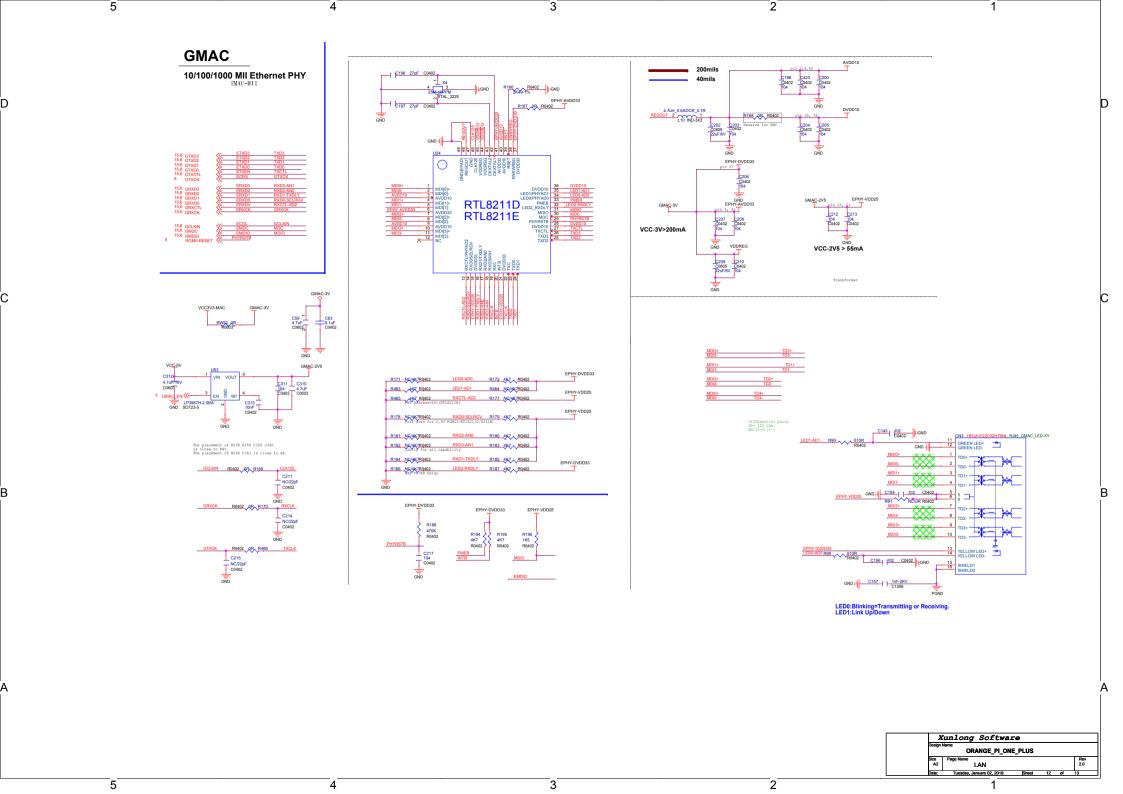












Ext Port Ext VCC-IO CON12 CON12

3 3 3V1 5.0V1 4
5 5DA 5.0V2 6
7 SCL GND3 8
9 10_GCLK TXD0 10
11 GND1 RXD0 12
13 10_0 10_1 13
10_0 10_1 15
15 10_2 GND4 18
15 10_2 GND4 16
15 10_2 GND4 16
15 10_2 GND4 16
15 10_2 GND4 18
15 10_2 GND4 16
15 10_2 GND4 16
15 10_2 GND5 22
23 SPI_MISO 10_5 22
23 SPI_MISO 10_6 24
25 SPI_CLK SPI_CE0
DIP26-254 TWI1-SDA R158 2K R0402
TWI1-SCK R155 2K R0402 VCC-IO TWI1-SDA TWI1-SCK PWM1 PD21
PD22
PC8
PC8
PC7
UART3_RTS
SPI0_CS0
PH3 PWM1
GND:
UART3_RX
UART3_TX
UART3_TX
VCC-IO
SPI0_MOSI
SPI0_MISO
SPI0_CLK
GND: Xunlong Software
Design Name ORANGE_PI_ONE_PLUS