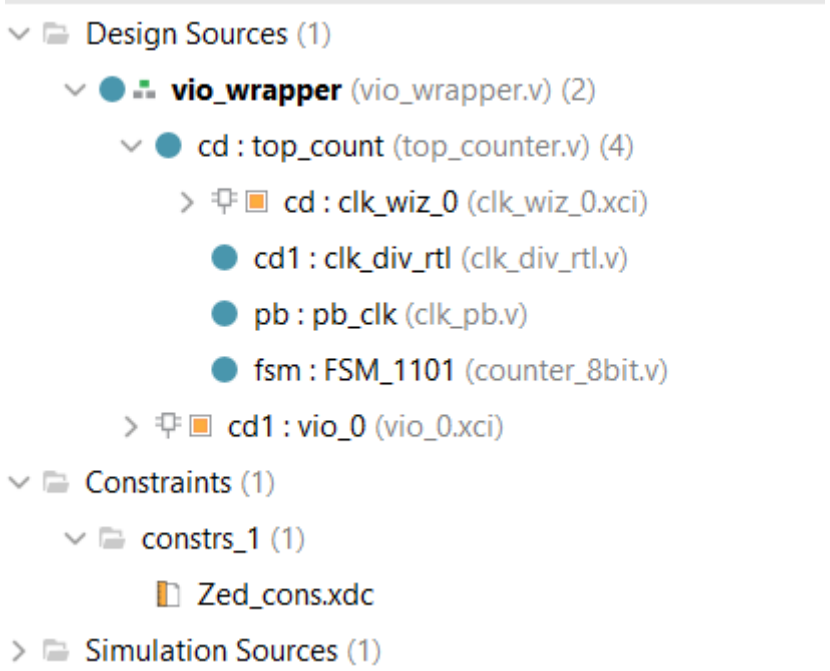
Lab 5 - Lab

Things done in lab to make 1101 sequence detector in next slides:



Code

1111_LAB5HW - [C:/Users/anant/1111_LAB5HW/1111_LAB5HW.xpr] - Vivado 2019.1

File Edit Flow Tools Reports Window Layout View Help Quick Access write_bitstream Complete

Default Layout

Flow Navigator

- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
    - Constraints Wizard
    - Edit Timing Constraints
    - Report Timing Summary
    - Report Clock Networks
    - Report Clock Interaction
    - Report Methodology
    - Report DRC
    - Report Noise
    - Report Utilization
    - Report Power
    - Schematic
- PROGRAM AND DEBUG
  - Generate Bitstream
  - Open Hardware Manager
    - Open Target
    - Program Device

IMPLEMENTED DESIGN - xc7z020clg484-1

Implemented Design is out-of-date. Implementation is running. Reload Close Design

Properties

Sources | Netlist

- Design Sources (1)
  - **vio_wrapper** (vio_wrapper.v) (2)
    - cd : top_count (top_counter.v) (4)
      - cd : clk_wiz_0 (clk_wiz_0.xci)
      - cd1 : clk_div_rtl (clk_div_rtl.v)
      - pb : pb_clk (clk_pb.v)
      - fsm : FSM_1101 (counter_8bit.v)
    - cd1 : vio_0 (vio_0.xci)
- Constraints (1)
  - constrs_1 (1)
    - Zed_cons.xdc
- Simulation Sources (1)
- Utility Sources

Hierarchy | IP Sources | Libraries | Compile Order

Project Summary | vio_wrapper.v | top_counter.v | clk_pb.v | counter_8bit.v | Zed_cons.xdc

C:/Users/anant/1111_LAB5HW/1111_LAB5HW.srcs/sources_1/new/vio_wrapper.v

```
16  // Revision:
17  // Revision 0.01 - File Created
18  // Additional Comments:
19  //
20  //////////////////////////////////////////////////////////////////////////////////


23  module vio_wrapper(
24      input clk_100M
25      );
26      wire in1;
27      wire in0;
28      wire clear;
29      wire [2:0] fsm_state;
30      wire detect;
31     top_count cd ( .clk_100M(clk_100M), .in0(in0), .in1(in1), .clear(clear), .fsm_state(fsm_state),
32      .detect(detect));


35  vio_0 cd1 (
36    .clk(clk_100M),                // input wire clk
37    .probe_in0(fsm_state),     // input wire [2 : 0] probe_in0
38    .probe_in1(detect),     // input wire [0 : 0] probe_in1
39    .probe_out0(in1),  // output wire [0 : 0] probe_out0
40    .probe_out1(in0),  // output wire [0 : 0] probe_out1
41    .probe_out2(clear)  // output wire [0 : 0] probe_out2
42  );
43  endmodule
44
```

Tcl Console | Messages | Log | Reports | Design Runs | Power | DRC | Methodology | Timing

43:9 Insert Verilog

ENG IN 18:44 23-09-2024

1111_LAB5HW - [C:/Users/anant/1111_LAB5HW/1111_LAB5HW.xpr] - Vivado 2019.1

File Edit Flow Tools Reports Window Layout View Help Quick Access write_bitstream Complete

Default Layout

Flow Navigator

SYNTHESIS
- Run Synthesis
- Open Synthesized Design

IMPLEMENTATION
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  - Report Noise
  - Report Utilization
  - Report Power
  - Schematic

PROGRAM AND DEBUG
- Generate Bitstream
- Open Hardware Manager
  - Open Target
  - Program Device

IMPLEMENTED DESIGN - xc7z020clg484-1

Implemented Design is out-of-date. Implementation is running. Reload Close Design

Properties

Sources Netlist

- Design Sources (1)
  - vio_wrapper (vio_wrapper.v) (2)
    - cd : top_count (top_counter.v) (4)
      - cd : clk_wiz_0 (clk_wiz_0.xci)
      - cd1 : clk_div_rtl (clk_div_rtl.v)
      - pb : pb_clk (clk_pb.v)
      - fsm : FSM_1101 (counter_8bit.v)
    - cd1 : vio_0 (vio_0.xci)
- Constraints (1)
  - constrs_1 (1)
    - Zed_cons.xdc
- Simulation Sources (1)
- Utility Sources

Hierarchy IP Sources Libraries Compile Order

Project Summary | vio_wrapper.v | top_counter.v | clk_pb.v | counter_8bit.v | Zed_cons.xdc

C:/Users/anant/1111_LAB5HW/1111_LAB5HW.srcs/sources_1/new/top_counter.v

```
16  // Revision:
17  // Revision 0.01 - File Created
18  // Additional Comments:
19  //
20  //////////////////////////////////////////////////////////////////////////////////
21
22
23
24  module top_count(
25      input clk_100M,
26      input in0,
27      input in1,
28      input clear,
29      output detect,
30      output [2:0] fsm_state
31      );
32      wire clk_8M, clk_1Hz, clk_pb;
33      clk_wiz_0 cd
34     (
35      // Clock out ports
36      .clk_8M(clk_8M),     // output clk_8M
37     // Clock in ports
38      .clk_100M(clk_100M));
39
40      clk_div_rtl cd1( .clk_8M(clk_8M),  .clk_1Hz(clk_1Hz));
41      pb_clk pb(.clk_1hz(clk_1Hz), .in0(in0), .in1(in1), .clk_pb(clk_pb));
42      FSM_1101 fsm (.in1(in1), .clear(clear), .detect(detect), .fsm_state(fsm_state)
43      , .clk_pb(clk_pb));
44  endmodule
```

Tcl Console | Messages | Log | Reports | Design Runs | Power | DRC | Methodology | Timing

ENG IN 18:44 23-09-2024

1111_LAB5HW - [C:/Users/anant/1111_LAB5HW/1111_LAB5HW.xpr] - Vivado 2019.1

File Edit Flow Tools Reports Window Layout View Help Quick Access write_bitstream Complete

Default Layout

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- PROGRAM AND DEBUG
  - Generate Bitstream
  - Open Hardware Manager
    - Open Target
    - Program Device

IMPLEMENTED DESIGN - xc7z020clg484-1

Implemented Design is out-of-date. Implementation is running. Reload Close Design

Source File Properties

Sources | Netlist

- Design Sources (1)
  - vio_wrapper (vio_wrapper.v) (2)
    - cd : top_count (top_counter.v) (4)
      - cd : clk_wiz_0 (clk_wiz_0.xci)
      - cd1 : clk_div_rtl (clk_div_rtl.v)
      - pb : pb_clk (clk_pb.v)
      - fsm : FSM_1101 (counter_8bit.v)
    - cd1 : vio_0 (vio_0.xci)
- Constraints (1)
  - constrs_1 (1)
    - Zed_cons.xdc
- Simulation Sources (1)
- Utility Sources

Hierarchy | IP Sources | Libraries | Compile Order

Project Summary | vio_wrapper.v | top_counter.v | clk_pb.v | counter_8bit.v | Zed_cons.xdc | **clk_div_rtl.v**

C:/Users/anant/Downloads/clk_div_rtl.v

```
14  // Dependencies:
15  //
16  // Revision:
17  // Revision 0.01 - File Created
18  // Additional Comments:
19  //
20  //////////////////////////////////////////////////////////////////////////////////
21
22
23  module clk_div_rtl(
24      input clk_8M,
25      output clk_1Hz
26      );
27
28      reg [22:0] Count_reg = 0; // Initialization of FFs during FPGA configuration
29      reg [22:0] Count_next; // output of combinational circuit...can not be initialized
30      always@(posedge clk_8M)
31          begin
32                  Count_reg <= Count_next; // D-FF
33          end
34
35      always@(*) // Comb. ckt to find out next state
36          Count_next = Count_reg+1;
37
38      assign clk_1Hz = Count_reg[22];
39
40  endmodule
41
42
```

Tcl Console | Messages | Log | Reports | Design Runs | Power | DRC | Methodology | Timing

23:0 Insert Verilog

ENG IN 18:44 23-09-2024

1111_LAB5HW - [C:/Users/anant/1111_LAB5HW/1111_LAB5HW.xpr] - Vivado 2019.1

File Edit Flow Tools Reports Window Layout View Help Quick Access write_bitstream Complete

Default Layout

Flow Navigator

- SYNTHESIS
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  - Open Synthesized Design
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  - Run Implementation
  - Open Implemented Design
    - Constraints Wizard
    - Edit Timing Constraints
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    - Report Noise
    - Report Utilization
    - Report Power
    - Schematic
- PROGRAM AND DEBUG
  - Generate Bitstream
  - Open Hardware Manager
    - Open Target
    - Program Device

IMPLEMENTED DESIGN - xc7z020clg484-1

Implemented Design is out-of-date. Implementation is running. Reload Close Design

Source File Properties

Sources | Netlist

- Design Sources (1)
  - **vio_wrapper** (vio_wrapper.v) (2)
    - cd : top_count (top_counter.v) (4)
      - cd : clk_wiz_0 (clk_wiz_0.xci)
      - cd1 : clk_div_rtl (clk_div_rtl.v)
      - pb : pb_clk (clk_pb.v)
      - fsm : FSM_1101 (counter_8bit.v)
    - cd1 : vio_0 (vio_0.xci)
- Constraints (1)
  - constrs_1 (1)
    - Zed_cons.xdc
- Simulation Sources (1)
- Utility Sources

Hierarchy | IP Sources | Libraries | Compile Order

Project Summary | vio_wrapper.v | top_counter.v | clk_pb.v | counter_8bit.v | Zed_cons.xdc | clk_div_rtl.v

C:/Users/anant/1111_LAB5HW/1111_LAB5HW.srcs/sources_1/new/clk_pb.v

```
6  // Create Date: 17.09.2024 10:26:06
7  // Design Name:
8  // Module Name: clk_pb
9  // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////////////////////////////////////


23 module pb_clk(
24     input clk_1hz,
25     input in0,
26     input in1,
27     output reg clk_pb
28     );
29     wire in_pulse;
30     assign in_pulse = in0 | in1;
31     always @(posedge clk_1hz)
32         clk_pb <=in_pulse;
33 endmodule
34
```

Tcl Console | Messages | Log | Reports | Design Runs | Power | DRC | Methodology | Timing

ENG IN 18:45 23-09-2024

1101_lab5 - [C:/Users/anant/1101_lab5/1101_lab5.xpr] - Vivado 2019.1

File Edit Flow Tools Reports Window Layout View Help Quick Access write_bitstream Complete

Default Layout

Flow Navigator

- PROJECT MANAGER
  - Settings
  - Add Sources
  - Language Templates
  - IP Catalog
- IP INTEGRATOR
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
  - Run Simulation
- RTL ANALYSIS
  - Open Elaborated Design
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
- PROGRAM AND DEBUG

PROJECT MANAGER - 1101_lab5

Sources

- Design Sources (1)
  - vio_wrapper (vio_wrapper.v) (2)
    - cd : top_count (top_counter.v) (4)
      - cd : clk_wiz_0 (clk_wiz_0.xci)
      - cd1 : clk_div_rtl (clk_div_rtl.v)
      - pb : pb_clk (clk_pb.v)
      - fsm : FSM_1101 (counter_8bit.v)
    - cd1 : vio_0 (vio_0.xci) (1)
      - vio_0 (vio_0.v) (1)
        - inst : vio_v3_0_20_vio
- Constraints (1)

Hierarchy IP Sources Libraries Compile Order

Source File Properties

counter_8bit.v

Enabled

Location:	C:/Users/anant/1101_lab5/1101_lab5.srcs/sources_
Type:	Verilog
Library:	xil_defaultlib
Size:	1.6 KB
Modified:	Today at 17:49:56 PM

General Properties

Tcl Console Messages Log Reports Design Runs

Project Summary | counter_8bit.v *

C:/Users/anant/1101_lab5/1101_lab5.srcs/sources_1/new/counter_8bit.v

```
22  module FSM_1101(
23      input clk_pb,
24      input in1,
25      input clear,
26      output [2:0] fsm_state,
27      output reg detect
28      );
29      parameter s0 = 3'b000, s1 = 3'b001, s2 = 3'b010, s3 = 3'b011, s4 = 3'b100;
30      reg [2:0] ps = s0;
31      reg [2:0] ns;
32      always @(posedge clk_pb or posedge clear)
33          begin
34           if(clear)
35               ps <= s0;
36           else
37               ps <= ns;
38           end
39
40       always @(*)
41       begin
42          if(ps == s4)
43              detect = 1;
44          else
45              detect = 0;
46       end
47
48       always @(*)
49       begin
50          case(ps)
51          s0: if(in1 == 1)
52                  ns = s1;
53              else
```

32:4 Insert Verilog

ENG IN 18:47 23-09-2024

1101_lab5 - [C:/Users/anant/1101_lab5/1101_lab5.xpr] - Vivado 2019.1

File Edit Flow Tools Reports Window Layout View Help Quick Access write_bitstream Complete

Default Layout

Flow Navigator

- PROJECT MANAGER
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  - Generate Block Design
- SIMULATION
  - Run Simulation
- RTL ANALYSIS
  - Open Elaborated Design
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
- PROGRAM AND DEBUG

PROJECT MANAGER - 1101_lab5

Sources

- Design Sources (1)
  - vio_wrapper (vio_wrapper.v) (2)
    - cd : top_count (top_counter.v) (4)
      - cd : clk_wiz_0 (clk_wiz_0.xci)
      - cd1 : clk_div_rtl (clk_div_rtl.v)
      - pb : pb_clk (clk_pb.v)
      - fsm : FSM_1101 (counter_8bit.v)
    - cd1 : vio_0 (vio_0.xci) (1)
      - vio_0 (vio_0.v) (1)
        - inst : vio_v3_0_20_vio
- Constraints (1)

Hierarchy IP Sources Libraries Compile Order

Source File Properties

counter_8bit.v

Enabled

Location:	C:/Users/anant/1101_lab5/1101_lab5.srcs/sources_
Type:	Verilog
Library:	xil_defaultlib
Size:	1.6 KB
Modified:	Today at 17:49:56 PM

General Properties

Tcl Console Messages Log Reports Design Runs

Project Summary | counter_8bit.v *

C:/Users/anant/1101_lab5/1101_lab5.srcs/sources_1/new/counter_8bit.v

```
48      always @(*)
49      begin
50         case(ps)
51         s0: if(in1 == 1)
52                ns = s1;
53             else
54                ns = s0;
55         s1: if(in1 == 1)
56                ns = s2;
57             else
58                ns = s0;
59         s2: if(in1 == 0)
60                ns = s3;
61             else
62                ns = s2;
63         s3: if(in1 == 1)
64                ns = s4;
65             else
66                ns = s0;
67         s4: if(in1 == 1)
68                ns = s2;
69             else
70                ns = s0;
71         default ns = s0;
72
73      endcase
74      end
75
76     assign fsm_state = ps;
77  endmodule
78
```

32:4 Insert Verilog

ENG IN 18:48 23-09-2024

Simulation

1101_lab5 - [C:/Users/anant/1101_lab5/1101_lab5.xpr] - Vivado 2019.1

File Edit Flow Tools Reports Window Layout View Help Quick Access write_bitstream Complete

Dashboard Default Layout

Flow Navigator

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- PROGRAM AND DEBUG
  - Generate Bitstream
  - Open Hardware Manager
    - Open Target
    - Program Device
    - Add Configuration Memory

HARDWARE MANAGER - 192.168.226.142/xilinx_tcf/Digilent/210248A39C93

Hardware

Name	Status
arm_dap_0 (0)	N/A
xc7z020_1 (2)	Programmed
XADC (System Monit	
hw_vio_1 (cd1)	OK

Debug Probe Properties

in0

Source: NETLIST

Type: VIO_OUTPUT

Width: 1

General Properties

vio_wrapper.v | top_counter.v | clk_pb.v | counter_8bit.v | Zed_cons.xdc | hw_vios

Dashboard Options

hw_vio_1

Name	Value	Activity	Direction	VIO
detect	[B] 0		Input	hw_vio_1
fsm_state[2:0]	[H] 1		Input	hw_vio_1
clear	[B] 0		Output	hw_vio_1
in0	[B] 0		Output	hw_vio_1
in1	[B] 1		Output	hw_vio_1

Tcl Console | Messages | Serial I/O Links | Serial I/O Scans

```
set_property OUTPUT_VALUE 0 [get_hw_probes in0 -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
commit_hw_vio [get_hw_probes {in0} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
set_property OUTPUT_VALUE 0 [get_hw_probes in1 -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
commit_hw_vio [get_hw_probes {in1} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
set_property OUTPUT_VALUE 1 [get_hw_probes in1 -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
commit_hw_vio [get_hw_probes {in1} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
```

Type a Tcl command here

ENG IN 18:13 23-09-2024

1101_lab5 - [C:/Users/anant/1101_lab5/1101_lab5.xpr] - Vivado 2019.1

File Edit Flow Tools Reports Window Layout View Help Quick Access write_bitstream Complete

Dashboard Default Layout

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    - Report Power
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    - Open Target
    - Program Device
    - Add Configuration Memory

HARDWARE MANAGER - 192.168.226.142/xilinx_tcf/Digilent/210248A39C93

Hardware

Name	Status
arm_dap_0 (0)	N/A
xc7z020_1 (2)	Programmed
XADC (System Monit	
hw_vio_1 (cd1)	OK

Debug Probe Properties

clear

Source: NETLIST

Type: VIO_OUTPUT

Width: 1

General Properties

vio_wrapper.v | top_counter.v | clk_pb.v | counter_8bit.v | Zed_cons.xdc | hw_vios

Dashboard Options

hw_vio_1

Name	Value	Activity	Direction	VIO
detect	[B] 0		Input	hw_vio_1
fsm_state[2:0]	[H] 0		Input	hw_vio_1
clear	[B] 1		Output	hw_vio_1
in0	[B] 0		Output	hw_vio_1
in1	[B] 1		Output	hw_vio_1

Tcl Console | Messages | Serial I/O Links | Serial I/O Scans

```
set_property OUTPUT_VALUE 0 [get_hw_probes in0 -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
commit_hw_vio [get_hw_probes {in0} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
set_property OUTPUT_VALUE 1 [get_hw_probes in1 -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
commit_hw_vio [get_hw_probes {in1} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
set_property OUTPUT_VALUE 1 [get_hw_probes clear -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
commit_hw_vio [get_hw_probes {clear} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
```

Type a Tcl command here

ENG IN 18:12 23-09-2024

1101_lab5 - [C:/Users/anant/1101_lab5/1101_lab5.xpr] - Vivado 2019.1

File Edit Flow Tools Reports Window Layout View Help Quick Access write_bitstream Complete

Dashboard Default Layout

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    - Program Device
    - Add Configuration Memory

HARDWARE MANAGER - 192.168.226.142/xilinx_tcf/Digilent/210248A39C93

Hardware

Name	Status
xilinx_tcf/Digilent/21024	Open
arm_dap_0 (0)	N/A
xc7z020_1 (2)	Programmed
XADC (System Monit	

Debug Probe Properties

in0

Source: NETLIST

Type: VIO_OUTPUT

Width: 1

General Properties

vio_wrapper.v | top_counter.v | clk_pb.v | counter_8bit.v | Zed_cons.xdc | hw_vios

Dashboard Options

hw_vio_1

Name	Value	Activ...	Directi...	VIO
detect	[B] 0		Input	hw_vio_1
fsm_state[2:0]	[H] 1		Input	hw_vio_1
clear	[B] 0		Output	hw_vio_1
in0	[B] 0		Output	hw_vio_1
in1	[B] 1		Output	hw_vio_1

Tcl Console | Messages | Serial I/O Links | Serial I/O Scans

```
set_property OUTPUT_VALUE 0 [get_hw_probes in1 -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
commit_hw_vio [get_hw_probes {in1} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
set_property OUTPUT_VALUE 0 [get_hw_probes in0 -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
commit_hw_vio [get_hw_probes {in0} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
set_property OUTPUT_VALUE 1 [get_hw_probes in1 -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
commit_hw_vio [get_hw_probes {in1} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
```

Type a Tcl command here

ENG IN 18:17 23-09-2024

1101_lab5 - [C:/Users/anant/1101_lab5/1101_lab5.xpr] - Vivado 2019.1

File Edit Flow Tools Reports Window Layout View Help Quick Access write_bitstream Complete

Dashboard Default Layout

Flow Navigator

- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
    - Constraints Wizard
    - Edit Timing Constraints
    - Report Timing Summary
    - Report Clock Networks
    - Report Clock Interaction
    - Report Methodology
    - Report DRC
    - Report Utilization
    - Report Power
    - Schematic
- PROGRAM AND DEBUG
  - Generate Bitstream
  - Open Hardware Manager
    - Open Target
    - Program Device
    - Add Configuration Memory

HARDWARE MANAGER - 192.168.226.142/xilinx_tcf/Digilent/210248A39C93

Hardware

Name	Status
xilinx_tcf/Digilent/210248	Open
arm_dap_0 (0)	N/A
xc7z020_1 (2)	Programmed
XADC (System Monit	

Debug Probe Properties

in1

Source: NETLIST

Type: VIO_OUTPUT

Width: 1

General Properties

vio_wrapper.v | top_counter.v | clk_pb.v | counter_8bit.v | Zed_cons.xdc | hw_vios

Dashboard Options

hw_vio_1

Name	Value	Activ...	Directi...	VIO
detect	[B] 0		Input	hw_vio_1
fsm_state[2:0]	[H] 2		Input	hw_vio_1
clear	[B] 0		Output	hw_vio_1
in0	[B] 0		Output	hw_vio_1
in1	[B] 1		Output	hw_vio_1

Tcl Console | Messages | Serial I/O Links | Serial I/O Scans

```
set_property OUTPUT_VALUE 0 [get_hw_probes in0 -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
commit_hw_vio [get_hw_probes {in0} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
set_property OUTPUT_VALUE 0 [get_hw_probes in1 -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
commit_hw_vio [get_hw_probes {in1} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
set_property OUTPUT_VALUE 1 [get_hw_probes in1 -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
commit_hw_vio [get_hw_probes {in1} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
```

Type a Tcl command here

ENG IN 18:17 23-09-2024

1101_lab5 - [C:/Users/anant/1101_lab5/1101_lab5.xpr] - Vivado 2019.1

File Edit Flow Tools Reports Window Layout View Help Quick Access write_bitstream Complete

Dashboard Default Layout

Flow Navigator

- SYNTHESIS
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  - Open Hardware Manager
    - Open Target
    - Program Device
    - Add Configuration Memory

HARDWARE MANAGER - 192.168.226.142/xilinx_tcf/Digilent/210248A39C93

Hardware

Name	Status
xilinx_tcf/Digilent/210248	Open
arm_dap_0 (0)	N/A
xc7z020_1 (2)	Programmed
XADC (System Monit	

Debug Probe Properties

in0

Source: NETLIST

Type: VIO_OUTPUT

Width: 1

General Properties

vio_wrapper.v | top_counter.v | clk_pb.v | counter_8bit.v | Zed_cons.xdc | hw_vios

Dashboard Options

hw_vio_1

Name	Value	Activ...	Directi...	VIO
detect	[B] 0		Input	hw_vio_1
fsm_state[2:0]	[H] 3		Input	hw_vio_1
clear	[B] 0		Output	hw_vio_1
in0	[B] 1		Output	hw_vio_1
in1	[B] 0		Output	hw_vio_1

Tcl Console | Messages | Serial I/O Links | Serial I/O Scans

```
set_property OUTPUT_VALUE 0 [get_hw_probes in0 -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
commit_hw_vio [get_hw_probes {in0} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
set_property OUTPUT_VALUE 0 [get_hw_probes in1 -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
commit_hw_vio [get_hw_probes {in1} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
set_property OUTPUT_VALUE 1 [get_hw_probes in0 -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
commit_hw_vio [get_hw_probes {in0} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
```

Type a Tcl command here

ENG IN 18:18 23-09-2024

1101_lab5 - [C:/Users/anant/1101_lab5/1101_lab5.xpr] - Vivado 2019.1

File Edit Flow Tools Reports Window Layout View Help Quick Access write_bitstream Complete

Dashboard Default Layout

Flow Navigator

- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design
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  - Run Implementation
  - Open Implemented Design
    - Constraints Wizard
    - Edit Timing Constraints
    - Report Timing Summary
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    - Report Clock Interaction
    - Report Methodology
    - Report DRC
    - Report Utilization
    - Report Power
    - Schematic
- PROGRAM AND DEBUG
  - Generate Bitstream
  - Open Hardware Manager
    - Open Target
    - Program Device
    - Add Configuration Memory

HARDWARE MANAGER - 192.168.226.142/xilinx_tcf/Digilent/210248A39C93

Hardware

Name	Status
xilinx_tcf/Digilent/210248	Open
arm_dap_0 (0)	N/A
xc7z020_1 (2)	Programmed
XADC (System Monit	

Debug Probe Properties

in1

Source: NETLIST

Type: VIO_OUTPUT

Width: 1

General Properties

vio_wrapper.v | top_counter.v | clk_pb.v | counter_8bit.v | Zed_cons.xdc | hw_vios

Dashboard Options

hw_vio_1

Name	Value	Activ...	Directi...	VIO
detect	[B] 1		Input	hw_vio_1
fsm_state[2:0]	[H] 4		Input	hw_vio_1
clear	[B] 0		Output	hw_vio_1
in0	[B] 0		Output	hw_vio_1
in1	[B] 1		Output	hw_vio_1

Tcl Console | Messages | Serial I/O Links | Serial I/O Scans

```
set_property OUTPUT_VALUE 0 [get_hw_probes in0 -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
commit_hw_vio [get_hw_probes {in0} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
set_property OUTPUT_VALUE 0 [get_hw_probes in1 -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
commit_hw_vio [get_hw_probes {in1} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
set_property OUTPUT_VALUE 1 [get_hw_probes in1 -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
commit_hw_vio [get_hw_probes {in1} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
```

Type a Tcl command here

ENG IN 18:18 23-09-2024

Lab Homework

The lab homework that is to make a 1111 sequence detector for that I have to just change some things in FSM_1101.

Edited Code

1111_LAB5HW - [C:/Users/anant/1111_LAB5HW/1111_LAB5HW.xpr] - Vivado 2019.1

File Edit Flow Tools Reports Window Layout View Help Quick Access write_bitstream Complete

Default Layout

Flow Navigator

- SYNTHESIS
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  - Open Synthesized Design
- IMPLEMENTATION
  - Run Implementation
  - Open Implemented Design
    - Constraints Wizard
    - Edit Timing Constraints
    - Report Timing Summary
    - Report Clock Networks
    - Report Clock Interaction
    - Report Methodology
    - Report DRC
    - Report Noise
    - Report Utilization
    - Report Power
    - Schematic
- PROGRAM AND DEBUG
  - Generate Bitstream
  - Open Hardware Manager
    - Open Target
    - Program Device

IMPLEMENTED DESIGN - xc7z020clg484-1

Implemented Design is out-of-date. Implementation is running. Reload Close Design

Source File Properties

Sources | Netlist

- Design Sources (1)
  - vio_wrapper (vio_wrapper.v) (2)
    - cd : top_count (top_counter.v) (4)
      - cd : clk_wiz_0 (clk_wiz_0.xci)
      - cd1 : clk_div_rtl (clk_div_rtl.v)
      - pb : pb_clk (clk_pb.v)
      - fsm : FSM_1101 (counter_8bit.v)
    - cd1 : vio_0 (vio_0.xci)
- Constraints (1)
  - constrs_1 (1)
    - Zed_cons.xdc
- Simulation Sources (1)
- Utility Sources

Hierarchy | IP Sources | Libraries | Compile Order

Project Summary | vio_wrapper.v | top_counter.v | clk_pb.v | counter_8bit.v * | Zed_cons.xdc | clk_div_rtl.v

C:/Users/anant/1111_LAB5HW/1111_LAB5HW.srcs/sources_1/new/counter_8bit.v

```
48      always @(*)
49      begin
50         case(ps)
51         s0: if(in1 == 1)
52                ns = s1;
53             else
54                ns = s0;
55         s1: if(in1 == 1)
56                ns = s2;
57             else
58                ns = s0;
59         s2: if(in1 == 1)
60                ns = s3;
61             else
62                ns = s2;
63         s3: if(in1 == 1)
64                ns = s4;
65             else
66                ns = s0;
67         s4: if(in1 == 1)
68                ns = s1;
69             else
70                ns = s0;
71         default ns = s0;
72
73      endcase
74      end
75      assign fsm_state = ps;
76  endmodule
77
```

Tcl Console | Messages | Log | Reports | Design Runs | Power | DRC | Methodology | Timing

41:15 Insert Verilog

ENG IN 18:53 23-09-2024

Simulation

Lab home work simulation

1111_LAB5HW - [C:/Users/anant/1111_LAB5HW/1111_LAB5HW.xpr] - Vivado 2019.1

File Edit Flow Tools Reports Window Layout View Help Quick Access write_bitstream Complete

Dashboard Default Layout

Flow Navigator

- SYNTHESIS
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    - Report Clock Interaction
    - Report Methodology
    - Report DRC
    - Report Utilization
    - Report Power
    - Schematic
- PROGRAM AND DEBUG
  - Generate Bitstream
  - Open Hardware Manager
    - Open Target
    - Program Device
    - Add Configuration Memory

HARDWARE MANAGER - 192.168.226.142/xilinx_tcf/Digilent/210248A39C7D

Hardware

Name	Status
arm_dap_0 (0)	N/A
xc7z020_1 (2)	Programmed
XADC (System Monit	
hw_vio_1 (cd1)	OK

Debug Probe Properties

in0

Source: NETLIST

Type: VIO_OUTPUT

Width: 1

General Properties

vio_wrapper.v | top_counter.v | clk_pb.v | counter_8bit.v | Zed_cons.xdc | hw_vios

Dashboard Options

hw_vio_1

Name	Value	Activ...	Directi...	VIO
detect	[B] 0		Input	hw_vio_1
fsm_state[2:0]	[H] 1		Input	hw_vio_1
clear	[B] 0		Output	hw_vio_1
in0	[B] 0		Output	hw_vio_1
in1	[B] 1		Output	hw_vio_1

Tcl Console | Messages | Serial I/O Links | Serial I/O Scans

```
INFO: [Labtools 27-3164] End of startup status: HIGH
refresh_hw_device [lindex [get_hw_devices xc7z020_1] 0]
INFO: [Labtools 27-2302] Device xc7z020 (JTAG device index = 1) is programmed with a design that has 1 VIO core(s).
INFO: [Labtools 27-1889] Uploading output probe values for VIO core [hw_vio_1]
set_property OUTPUT_VALUE 1 [get_hw_probes in1 -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
commit_hw_vio [get_hw_probes {in1} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
```

Type a Tcl command here

ENG IN 18:32 23-09-2024

1111_LAB5HW - [C:/Users/anant/1111_LAB5HW/1111_LAB5HW.xpr] - Vivado 2019.1

File Edit Flow Tools Reports Window Layout View Help Quick Access write_bitstream Complete

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    - Report DRC
    - Report Utilization
    - Report Power
    - Schematic
- PROGRAM AND DEBUG
  - Generate Bitstream
  - Open Hardware Manager
    - Open Target
    - Program Device
    - Add Configuration Memory

HARDWARE MANAGER - 192.168.226.142/xilinx_tcf/Digilent/210248A39C7D

Hardware

Name	Status
arm_dap_0 (0)	N/A
xc7z020_1 (2)	Programmed
XADC (System Monit	
hw_vio_1 (cd1)	OK

Debug Probe Properties

in1

Source: NETLIST

Type: VIO_OUTPUT

Width: 1

General Properties

vio_wrapper.v | top_counter.v | clk_pb.v | counter_8bit.v | Zed_cons.xdc | hw_vios

Dashboard Options

hw_vio_1

Name	Value	Activ...	Directi...	VIO
detect	[B] 0		Input	hw_vio_1
fsm_state[2:0]	[H] 2		Input	hw_vio_1
clear	[B] 0		Output	hw_vio_1
in0	[B] 0		Output	hw_vio_1
in1	[B] 1		Output	hw_vio_1

Tcl Console | Messages | Serial I/O Links | Serial I/O Scans

```
set_property OUTPUT_VALUE 0 [get_hw_probes in1 -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
commit_hw_vio [get_hw_probes {in1} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
set_property OUTPUT_VALUE 0 [get_hw_probes in0 -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
commit_hw_vio [get_hw_probes {in0} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
set_property OUTPUT_VALUE 1 [get_hw_probes in1 -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
commit_hw_vio [get_hw_probes {in1} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
```

Type a Tcl command here

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1111_LAB5HW - [C:/Users/anant/1111_LAB5HW/1111_LAB5HW.xpr] - Vivado 2019.1

File Edit Flow Tools Reports Window Layout View Help Quick Access write_bitstream Complete

Dashboard Default Layout

Flow Navigator

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HARDWARE MANAGER - 192.168.226.142/xilinx_tcf/Digilent/210248A39C7D

Hardware

Name	Status
arm_dap_0 (0)	N/A
xc7z020_1 (2)	Programmed
XADC (System Monit	
hw_vio_1 (cd1)	OK

Debug Probe Properties

in1

Source: NETLIST

Type: VIO_OUTPUT

Width: 1

General Properties

vio_wrapper.v | top_counter.v | clk_pb.v | counter_8bit.v | Zed_cons.xdc | hw_vios

Dashboard Options

hw_vio_1

Name	Value	Activ...	Directi...	VIO
detect	[B] 0		Input	hw_vio_1
fsm_state[2:0]	[H] 3		Input	hw_vio_1
clear	[B] 0		Output	hw_vio_1
in0	[B] 0		Output	hw_vio_1
in1	[B] 1		Output	hw_vio_1

Tcl Console | Messages | Serial I/O Links | Serial I/O Scans

```
set_property OUTPUT_VALUE 0 [get_hw_probes in1 -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
commit_hw_vio [get_hw_probes {in1} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
set_property OUTPUT_VALUE 0 [get_hw_probes in0 -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
commit_hw_vio [get_hw_probes {in0} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
set_property OUTPUT_VALUE 1 [get_hw_probes in1 -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
commit_hw_vio [get_hw_probes {in1} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
```

Type a Tcl command here

ENG IN 18:32 23-09-2024

1111_LAB5HW - [C:/Users/anant/1111_LAB5HW/1111_LAB5HW.xpr] - Vivado 2019.1

File Edit Flow Tools Reports Window Layout View Help Quick Access write_bitstream Complete

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    - Open Target
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HARDWARE MANAGER - 192.168.226.142/xilinx_tcf/Digilent/210248A39C7D

Hardware

Name	Status
arm_dap_0 (0)	N/A
xc7z020_1 (2)	Programmed
XADC (System Monit	
hw_vio_1 (cd1)	OK

Debug Probe Properties

in1

Source: NETLIST

Type: VIO_OUTPUT

Width: 1

General Properties

vio_wrapper.v | top_counter.v | clk_pb.v | counter_8bit.v | Zed_cons.xdc | hw_vios

Dashboard Options

hw_vio_1

Name	Value	Activ...	Directi...	VIO
detect	[B] 1		Input	hw_vio_1
fsm_state[2:0]	[H] 4		Input	hw_vio_1
clear	[B] 0		Output	hw_vio_1
in0	[B] 0		Output	hw_vio_1
in1	[B] 1		Output	hw_vio_1

Tcl Console | Messages | Serial I/O Links | Serial I/O Scans

```
set_property OUTPUT_VALUE 0 [get_hw_probes in1 -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
commit_hw_vio [get_hw_probes {in1} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
set_property OUTPUT_VALUE 0 [get_hw_probes in0 -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
commit_hw_vio [get_hw_probes {in0} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
set_property OUTPUT_VALUE 1 [get_hw_probes in1 -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
commit_hw_vio [get_hw_probes {in1} -of_objects [get_hw_vios -of_objects [get_hw_devices xc7z020_1] -filter {CELL_NAME=~"cd1"}]]
```

Type a Tcl command here

ENG IN 18:33 23-09-2024