T4 Datasheet MSP430FR2355 Sistemas Empotrados 1

Héctor Lacueva Sacristán 869637

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Vector reset

- Se encuentra en la dirección **0FFFEh**.
- Si el micro no está programado, se escribe en el vector reset FFFFh y el micro entra en LPM4 (low power mode 4).
- Tiene la mayor prioridad dentro del vector de interrupciones (63).
- Se encuentra dentro de la FRAM.
- Puede ser provocado por las siguientes razones:
  - Power up
  - Brownout (BOR)
  - Supply supervisor
  - External reset RST
  - Watchdog time-out
  - Key violation
  - FRAM uncorrectable bit error detection
  - Software POR, BOR
  - FLL unlock error
- Salta si se activan los siguientes Flags:
  - SVSHIFG
  - PMMRSTIFG
  - WDTIFG
  - PMMPORIFG
  - PMMBORIFG
  - SYSRSTIV
  - FLLULPUC

Estado de los pines del GPIO tras Reset

Todos los pines están en alta-impedancia, con las funciones de módulo deshabilitadas (desactivados). Requieren inicialización explícita.

"After a BOR reset, **all port pins are high-impedance with Schmitt triggers and their module functions disabled to prevent any cross currents**. The application must initialize all port pins including unused ones (Section 8.3.2) as input high impedance, input with pulldown, input with pullup, output high, or output low according to the application needs by configuring PxDIR, PxREN, PxOUT, and PxIES accordingly. This initialization takes effect as soon as the LOCKLPM5 bit in the PM5CTL register (described in the PMM chapter) is cleared; until then, the I/Os remain in their high-impedance state with Schmitt trigger inputs disabled. Note that this is usually the same I/O initialization that is required after a wakeup from LPMx.5. After clearing LOCKLPM5, all interrupt flags should be cleared (note, this is different from the flow for wakeup from LPMx.5). Then port interrupts can be enabled by setting the corresponding PxIE bits. After a POR or PUC reset, all port pins are configured as inputs with their module function disabled. To prevent floating inputs, all port pins

including unused ones (Section 8.3.2) should be configured according to the application needs as early as possible during the initialization procedure.

Note that the same I/O initialization procedure can be used for all reset cases and wakeup from LPMx.5, except for PxIFG:

1. Initialize Ports: PxDIR, PxREN, PxOUT, and PxIES
2. Clear LOCKLPM5
3. If not waking up from LPMx.5: clear all PxIFGs to avoid erroneous port interrupts
4. Enable port interrupts in PxIE"

Max mA por gpio y total del chip (disipar/suministrar)

El max de mA por GPIO está en ± 5 mA y el límite total del chip es de ± 48 mA en total.

Table 5-12. Digital Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	DEVICE GRADE	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –3 mA(1)	T	2.0 V	1.4		2.0	V
		$I_{(OHmax)}$ = –5 mA(1)	T	3.0 V	2.4		3.0	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 3 mA(1)	T	2.0 V	0.0		0.60	V
		$I_{(OLmax)}$ = 5 mA(1)	T	3.0 V	0.0		0.60	
f_{Port_CLK}	Clock output frequency	Applicable to all IO ports, C_L = 20 pF(2)	T	2.0 V	16			MHz
			T	3.0 V	16			
		IOs multiplexed with MCLK and SMCLK, C_L = 10 pF(2)	T	2.0 V	24			
			T	3.0 V	24			
$t_{rise,dig}$	Port output rise time, digital only port pins	C_L = 20 pF	T	2.0 V		10		ns
			T	3.0 V		7		
$t_{fall,dig}$	Port output fall time, digital only port pins	C_L = 20 pF	T	2.0 V		10		ns
			T	3.0 V		5		

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The port can output frequencies at least up to the specified limit and might support higher frequencies.

Figure 1: Tabla de referencia