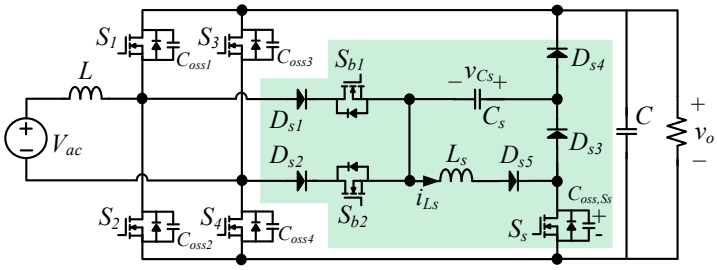
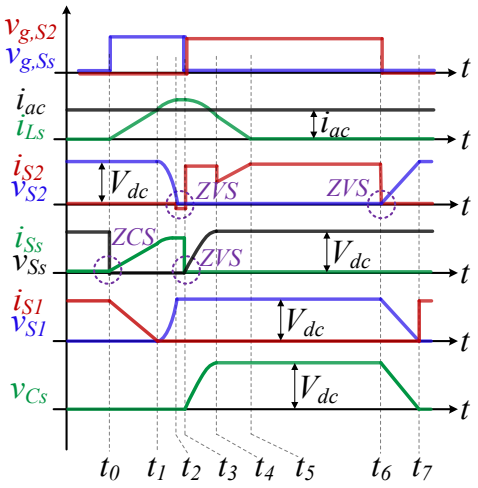
This is a brief overview of my Master's thesis project, "**Analysis and Design of a High-Efficiency Totem-Pole PFC Rectifier with an Integrated Zero-Voltage Transition (ZVT) Cell (11 kW)**." All of the work shown here was completed by me independently, from studying the theory and running simulations to building and testing the prototype.

The simulation files, source code, schematics, and PCB layouts are available here: https://github.com/hectorha-pc/PFC_ZVT

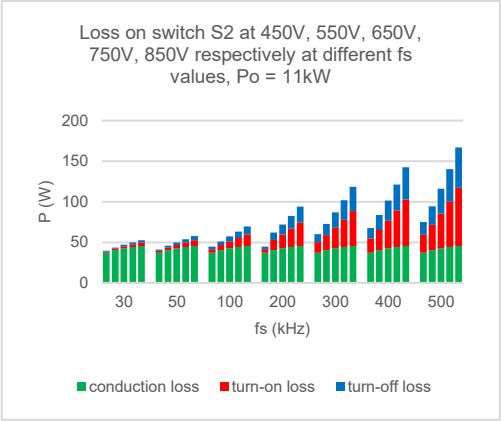
For more information, you can contact me at: hectorha0501@gmail.com



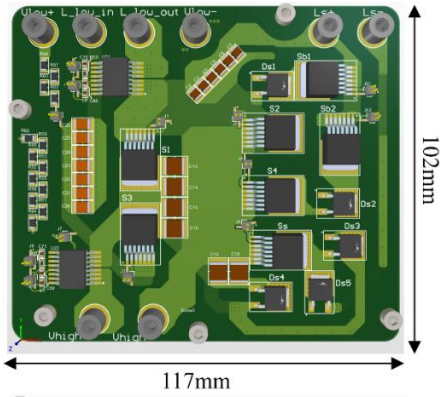
Totempole PFC with ZVT cell (green shaded)

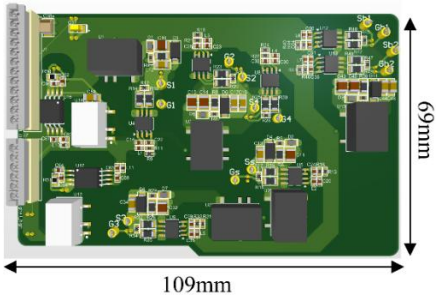


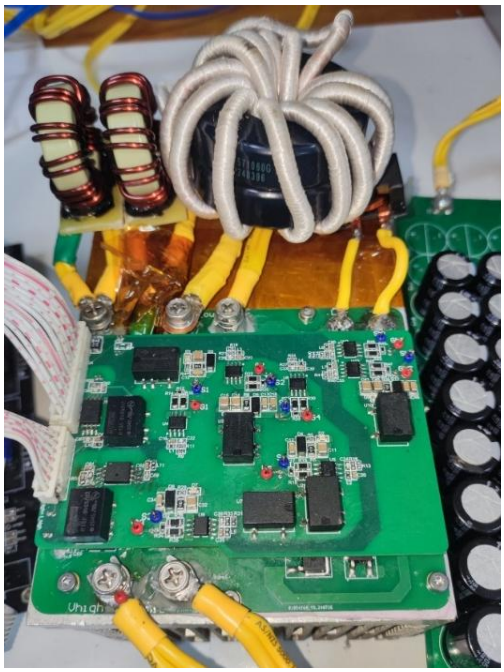
Simulation result (redrawn in Visio)



Beside this text is the loss-breakdown graph of the main switch without the ZVT cell. I researched how to calculate the switching losses based on the MOSFET datasheet specs and the operating conditions. This took me a few months because I needed to derive a formula that matches the switching waveform from my PSIM simulation and I was able to get a perfect match.

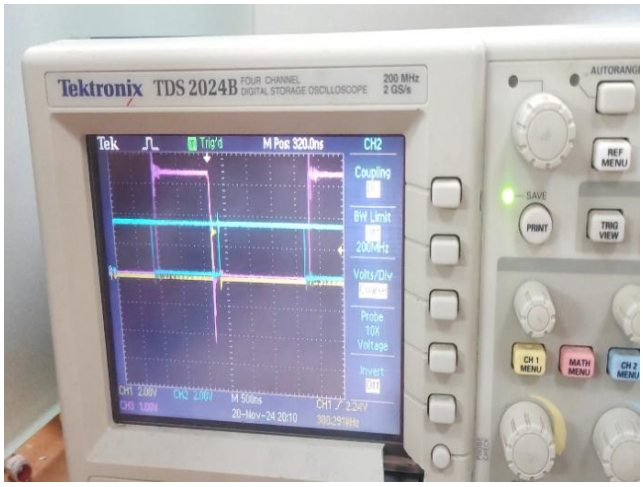




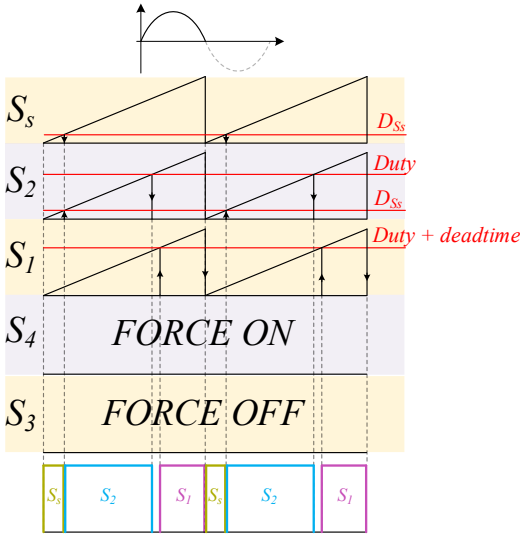


The PCB layout was challenging because my professor required a very compact board. I went through at least 8 PCB layout revisions to meet the size constraint and placement requirements. In terms of hardware integration, the power board is pressed against the heatsink, and the gate-drive board mounts on top and connects through 2-pin headers. The TMS320F28377D and its

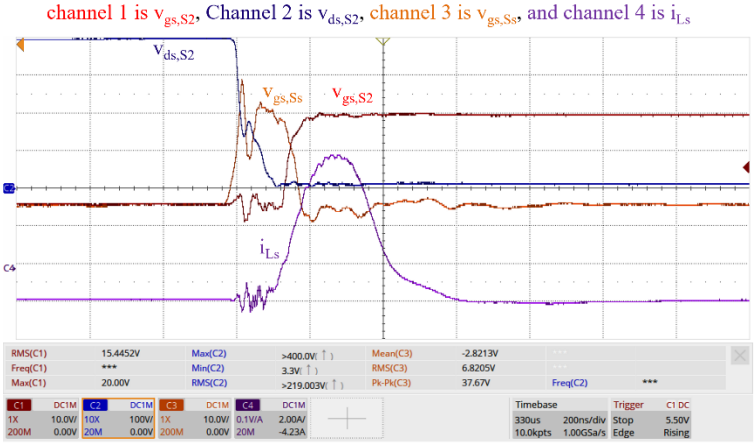
analog front-end circuits are on a separate board (the last image on shows my test setup and the black board mentioned). My work here was tuning the op-amp stage so the scaling fits the ADC input range.



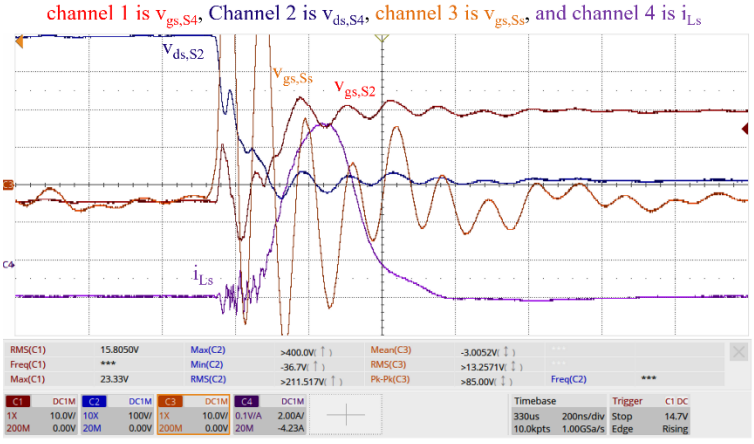
I also programmed the TMS320F28377D to validate the prototype. It took me a few months to go from learning the MCU architecture to implementing the firmware and writing the functions needed for my control algorithm. Shown beside are the PWM waveforms and the logic behind them (under).



The two oscilloscope screenshots below show test results with a positive DC source and a negative DC source. I ran into an issue in the negative DC case (significant noise on the gate-drive signals), and before I could resolve it, my funding ended. Even so, the results still support the ZVT cell concept and confirm that it works in this circuit.



Duty 0.5, positive DC input 200V, Load 100 Ω



Duty 0.5, negative DC input 200V, Load 100 Ω