

500 mA, Very Low Dropout Bias Rail CMOS Voltage Regulator

NCP133

The NCP133 is a 500 mA VLDO equipped with NMOS pass transistor and a separate bias supply voltage (V_{BIAS}). The device provides very stable, accurate output voltage with low noise suitable for space constrained, noise sensitive applications. In order to optimize performance for battery operated portable applications, the NCP133 features low I_Q consumption. The XDFN6 1.2 mm x 1.2 mm package is optimized for use in space constrained applications.

Features

- Input Voltage Range: 0.8 V to 5.5 V
- Bias Voltage Range: 2.4 V to 5.5 V
- Adjustable and Fixed Voltage Versions Available
- Output Voltage Range: 0.8 V to 2.1 V (Fixed) and 0.8 V to 3.6 V (Adjustable)
- ±1.5% Accuracy over Temperature, 0.5% V_{OUT} @ 25°C
- Ultra-Low Dropout: Typ. 140 mV at 500 mA
- Very Low Bias Input Current of Typ. 80 μA
- Very Low Bias Input Current in Disable Mode: Typ. 0.5 μA
- Logic Level Enable Input for ON/OFF Control
- Output Active Discharge Option Available
- Stable with a 2.2 μF Ceramic Capacitor
- Available in XDFN6 1.2 mm x 1.2 mm x 0.4 mm Package
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Battery-powered Equipment
- Smartphones, Tablets
- Cameras, DVRs, STB and Camcorders

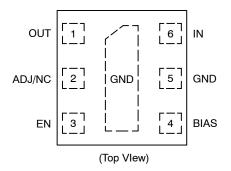


MARKING DIAGRAM



XX = Specific Device Code M = Date Code

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 9.

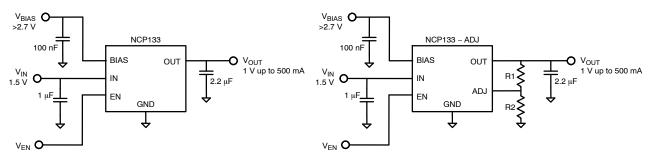
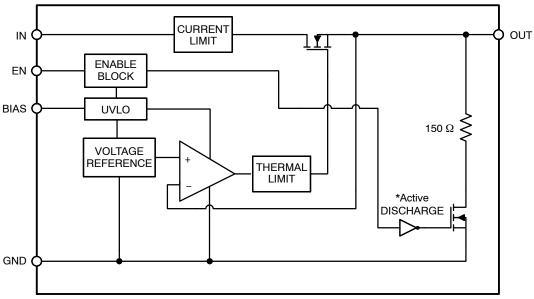


Figure 1. Typical Application Schematics



^{*}Active output discharge function is present only in NCP133AMXyyyTCG devices. yyy denotes the particular output voltage option.

Figure 2. Simplified Schematic Block Diagram - Fixed Version

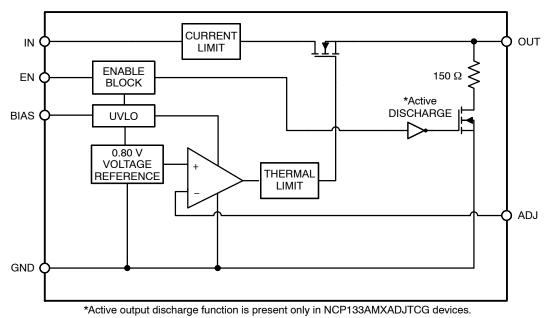


Figure 3. Simplified Schematic Block Diagram - Adjustable Version

PIN FUNCTION DESCRIPTION

Pin No. XDFN6	Pin Name	Description
1	OUT	Regulated Output Voltage pin
2 (Fixed)	N/C	Not internally connected (Note 1)
2 (Adj)	ADJ	Adjustable Regulator Feedback Input. Connect to output voltage resistor divider central node.
3	EN	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode.
4	BIAS	Bias voltage supply for internal control circuits. This pin is monitored by internal Under-Voltage Lockout Circuit.
5	GND	Ground
6	IN	Input Voltage Supply pin
Pad		Should be soldered to the ground plane for increased thermal performance.

^{1.} True no connect. Printed circuit board traces are allowable

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 2)	V _{IN}	-0.3 to 6	V
Output Voltage	V _{OUT}	-0.3 to $(V_{IN}+0.3) \le 6$	V
Chip Enable, Bias and Adj Input	V _{EN,} V _{BIAS,} V _{ADJ}	-0.3 to 6	V
Output Short Circuit Duration	t _{SC}	unlimited	s
Maximum Junction Temperature	T _J	150	°C
Storage Temperature	T _{STG}	-55 to 150	°C
ESD Capability, Human Body Model (Note 3)	ESD _{HBM}	2000	V
ESD Capability, Machine Model (Note 3)	ESD _{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

- 3. This device series incorporates ESD protection (except OUT pin) and is tested by the following methods:

 - ESD Human Body Model tested per EIA/JESD22-A114
 ESD Machine Model tested per EIA/JESD22-A115
 Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

THERMAL CHARACTERISTICS (Note 4)

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction-to-Air	R _{thJA}	110	°C/W
Thermal Resistance, Junction-to-Case (top)	R _{thJCt}	167	
Thermal Resistance, Junction-to-Case (bottom)	R _{thJCb}	33	
Thermal Resistance, Junction-to-Board (top)	R _{thJBt}	44	
Thermal Characterization Parameter, Junction-to-Case (top)	Psi _{JCt}	4.8	
Thermal Characterization Parameter, Junction-to-Board [FEM]	Psi _{JB}	42	

^{4.} Measured according to JEDEC board specification (board 2S2P, Cu layer thickness 1 oz, Cu area 1 in², no airflow). Detailed description can be found in JESD51-7, MIL-STD-883E, JESD51-8

ELECTRICAL CHARACTERISTICS $-40^{\circ}C \le T_J \le 85^{\circ}C$; $V_{BIAS} = 2.7 \text{ V or } (V_{OUT} + 1.6 \text{ V})$, whichever is greater, $V_{IN} = V_{OUT(NOM)} + 0.3 \text{ V}$, $I_{OUT} = 1 \text{ mA}$, $V_{EN} = 1 \text{ V}$, unless otherwise noted. $I_{EN} = 1 \text{ M}$, $I_{EN} = 1 \text{ V}$, unless otherwise noted. (Note 6)

Parameter	Test Conditions	Symbol	Min	Тур	Max	Unit
Operating Input Voltage Range		V _{IN}	V _{OUT} + V _{DO}		5.5	V
Operating Bias Voltage Range		V _{BIAS}	(V _{OUT} + 1.40) ≥ 2.4		5.5	V
Undervoltage Lock-out	V _{BIAS} Rising Hysteresis	UVLO		1.6 0.2		V
Reference Voltage (Adj devices only)	$T_J = +25^{\circ}C$	V _{REF}		0.800		V
Output Voltage Accuracy	(Note 5)	V _{OUT}		±0.5		%
Output Voltage Accuracy (Note 5)	$\begin{array}{l} -40^{\circ}C \leq T_{J} \leq 85^{\circ}C, \ V_{OUT(NOM)} + 0.3 \ V \leq V_{IN} \leq \\ V_{OUT(NOM)} + 1.0 \ V, \ 2.7 \ V \ or \ (V_{OUT(NOM)} + \\ 1.6 \ V), \ whichever \ is \ greater < V_{BIAS} < 5.5 \ V, \\ 1 \ mA < I_{OUT} < 500 \ mA \end{array}$	V _{OUT}	-1.5		+1.5	%
V _{IN} Line Regulation	$V_{OUT(NOM)} + 0.3 \text{ V} \le V_{IN} \le 5.0 \text{ V}$	Line _{Reg}		0.01		%/V
V _{BIAS} Line Regulation	2.7 V or (V _{OUT(NOM)} + 1.6 V), whichever is greater < V _{BIAS} < 5.5 V	Line _{Reg}		0.01		%/V
Load Regulation	I _{OUT} = 1 mA to 500 mA	Load _{Reg}		1.5		mV
V _{IN} Dropout Voltage	I _{OUT} = 150 mA (Note 7)	V _{DO}		37	75	mV
	I _{OUT} = 500 mA (Note 7)	V_{DO}		140	250	
V _{BIAS} Dropout Voltage	I _{OUT} = 500 mA, V _{IN} = V _{BIAS} (Notes 7, 8)	V _{DO}		1.1	1.5	V
Output Current Limit	V _{OUT} = 90% V _{OUT} (NOM)	I _{CL}	550	800	1000	mA
ADJ Pin Operating Current (ADJ devices only)		I _{ADJ}		0.1	0.5	μΑ
Bias Pin Operating Current	V _{BIAS} = 2.7 V	I _{BIAS}		80	110	μΑ
Bias Pin Disable Current	V _{EN} ≤ 0.4 V	I _{BIAS(DIS)}		0.5	1	μΑ
Vinput Pin Disable Current	V _{EN} ≤ 0.4 V	I _{VIN(DIS)}		0.5	1	μΑ
EN Pin Threshold Voltage	EN Input Voltage "H"	V _{EN(H)}	0.9			V
	EN Input Voltage "L"	V _{EN(L)}			0.4	
EN Pull Down Current	V _{EN} = 5.5 V	I _{EN}		0.3	1	μΑ
Turn-On Time	From assertion of V_{EN} to V_{OUT} = 98% $V_{OUT(NOM)}$. $V_{OUT(NOM)}$ = 1.0 V	t _{ON}		150		μs
Power Supply Rejection Ratio	V_{IN} to V_{OUT} , f = 1 kHz, I_{OUT} = 150 mA, $V_{IN} \ge V_{OUT}$ +0.5 V	PSRR(V _{IN})		70		dB
	V_{BIAS} to V_{OUT} , f = 1 kHz, I_{OUT} = 150 mA, $V_{IN} \ge V_{OUT}$ +0.5 V	PSRR(V _{BIAS})		80		dB
Output Noise Voltage (Fixed Volt.)	V _{IN} = V _{OUT} +0.5 V, V _{OUT} (NOM) = 1 V, f = 10 Hz to 100 kHz	V _N		40		μV_{RMS}
Output Noise Voltage (Adj devices)	V _{IN} = V _{OUT} +0.5 V, f = 10 Hz to 100 kHz	V _N		50 x V _{OUT}		μV_{RMS}
Thermal Shutdown	Temperature increasing			160		°C
Threshold	Temperature decreasing			140		
Output Discharge Pull-Down	$V_{EN} \leq 0.4$ V, V_{OUT} = 0.5 V, NCP133A options only	R _{DISCH}		150		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

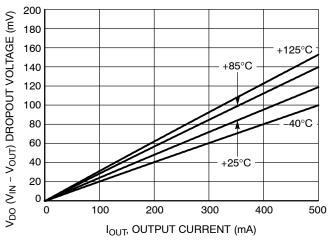
- 5. Adjustable devices tested at 0.8 V; external resistor tolerance is not taken into account.
- 6. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_A = 25°C. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.

 7. Dropout voltage is characterized when V_{OUT} falls 3% below V_{OUT}(NOM).

 8. For output voltages below 0.9 V, V_{BIAS} dropout voltage does not apply due to a minimum Bias operating voltage of 2.4 V.

TYPICAL CHARACTERISTICS

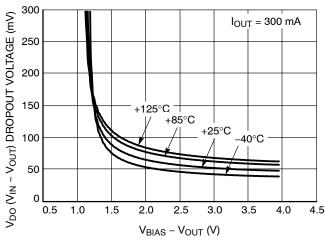
 $AT~T_J = +25^{\circ}C,~V_{IN} = V_{OUT(TYP)} + 0.3~V,~V_{BIAS} = 2.7~V,~V_{EN} = V_{BIAS},~V_{OUT(NOM)} = 1.0~V,~I_{OUT} = 500~MA,\\ C_{IN} = 1~MF,~C_{BIAS} = 0.1~MF,~AND~C_{OUT} = 2.2~MF~(EFFECTIVE~CAPACITANCE),~UNLESS~OTHERWISE~NOTED.$



V_{DO} (V_{IN} - V_{OUT}) DROPOUT VOLTAGE (mV) 200 $I_{OUT} = 100 \text{ mA}$ 180 160 140 120 100 80 +125°C 60 +25°C -40°C 40 20 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0 4.5 V_{BIAS} - V_{OUT} (V)

Figure 4. V_{IN} Dropout Voltage vs. I_{OUT} and Temperature T_J

Figure 5. V_{IN} Dropout Voltage vs. (V_{BIAS} – V_{OUT}) and Temperature T_J



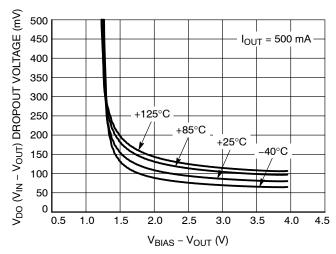
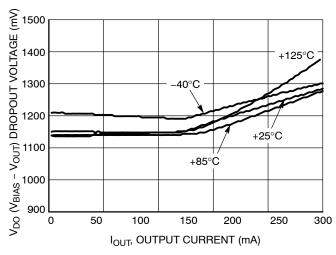


Figure 6. V_{IN} Dropout Voltage vs. (V_{BIAS} – V_{OUT}) and Temperature T_J

Figure 7. V_{IN} Dropout Voltage vs. (V_{BIAS} – V_{OUT}) and Temperature T_J



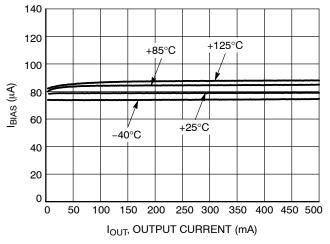


Figure 8. V_{BIAS} Dropout Voltage vs. I_{OUT} and Temperature T_{.I}

Figure 9. BIAS Pin Current vs. I_{OUT} and Temperature T_J

TYPICAL CHARACTERISTICS (continued)

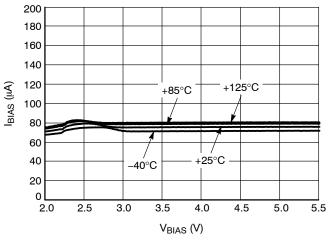
 $AT\ T_J = +25^{\circ}C,\ V_{IN} = V_{OUT(TYP)} + 0.3\ V,\ V_{BIAS} = 2.7\ V,\ V_{EN} = V_{BIAS},\ V_{OUT(NOM)} = 1.0\ V,\ I_{OUT} = 500\ MA,$ $C_{IN} = 1\ MF,\ C_{BIAS} = 0.1\ MF,\ AND\ C_{OUT} = 2.2\ MF\ (EFFECTIVE\ CAPACITANCE),\ UNLESS\ OTHERWISE\ NOTED.$

1000

900

800

700



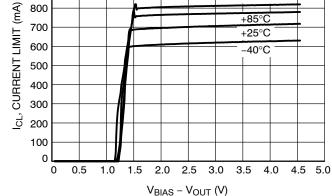


Figure 10. BIAS Pin Current vs. $V_{\mbox{\footnotesize BIAS}}$ and Temperature $T_{\mbox{\footnotesize J}}$

Figure 11. Current Limit vs. (V_{BIAS} - V_{OUT})

+125°C

+85°C

+25°C

APPLICATIONS INFORMATION

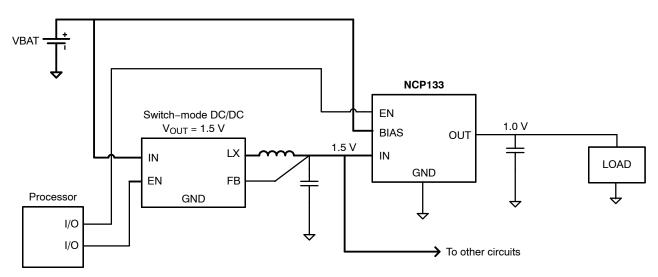


Figure 12. Typical Application: Low-Voltage DC/DC Post-Regulator with ON/OFF Functionality

The NCP133 dual-rail very low dropout voltage regulator is using NMOS pass transistor for output voltage regulation from $V_{\rm IN}$ voltage. All the low current internal control circuitry is powered from the $V_{\rm BIAS}$ voltage.

The use of an NMOS pass transistor offers several advantages in applications. Unlike PMOS topology devices, the output capacitor has reduced impact on loop stability. Vin to Vout operating voltage difference can be very low compared with standard PMOS regulators in very low Vin applications.

The NCP133 offers smooth monotonic start-up. The controlled voltage rising limits the inrush current.

The Enable (EN) input is equipped with internal hysteresis. NCP133 Voltage linear regulator Fixed and Adjustable version is available.

Output Voltage Adjust

The required output voltage of Adjustable devices can be adjusted from 0.8 V to 3.6 V using two external resistors.

Typical application schematics is shown in Figure 13.

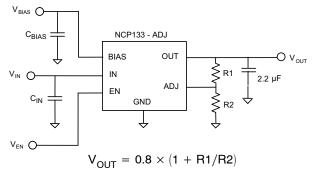


Figure 13. Typical Application Schematics

It is recommended to keep the total serial resistance of resistors (R1 + R2) no greater than 100 k Ω .

Recommended resistor values for programming the frequently used voltages can be found in the Table 1.

Dropout Voltage

Because of two power supply inputs V_{IN} and V_{BIAS} and one V_{OUT} regulator output, there are two Dropout voltages specified.

The first, the V_{IN} Dropout voltage is the voltage difference ($V_{IN}-V_{OUT}$) when V_{OUT} starts to decrease by percent specified in the Electrical Characteristics table. V_{BIAS} is high enough; specific value is published in the Electrical Characteristics table.

The second, V_{BIAS} dropout voltage is the voltage difference ($V_{BIAS} - V_{OUT}$) when V_{IN} and V_{BIAS} pins are joined together and V_{OUT} starts to decrease.

Input and Output Capacitors

The device is designed to be stable for ceramic output capacitors with Effective capacitance in the range from 2.2 μF to 10 μF . The device is also stable with multiple capacitors in parallel, having the total effective capacitance in the specified range.

In applications where no low input supplies impedance available (PCB inductance in V_{IN} and/or V_{BIAS} inputs as example), the recommended C_{IN} = 1 μF and C_{BIAS} = 0.1 μF or greater. Ceramic capacitors are recommended. For the best performance all the capacitors should be connected to the NCP133 respective pins directly in the device PCB copper layer, not through vias having not negligible impedance.

When using small ceramic capacitor, their capacitance is not constant but varies with applied DC biasing voltage, temperature and tolerance. The effective capacitance can be much lower than their nominal capacitance value, most importantly in negative temperatures and higher LDO output voltages. That is why the recommended Output capacitor capacitance value is specified as Effective value in the specific application conditions.

Enable Operation

The enable pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this data sheet. If the enable function is not to be used then the pin should be connected to $V_{\rm IN}$ or $V_{\rm BIAS}$.

Current Limitation

The internal Current Limitation circuitry allows the device to supply the full nominal current and surges but protects the device against Current Overload or Short.

Thermal Protection

Internal thermal shutdown (TSD) circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When TSD activated , the regulator output turns off. When cooling down under the low temperature threshold, device output is activated again. This TSD feature is provided to prevent failures from accidental overheating.

Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heatsinking. For reliable operation, junction temperature should be limited to +125°C maximum.

Table 1. RESISTOR VALUES FOR PROGRAMMING THE OUTPUT VOLTAGE

V _{OUT} (V)	R ₁ (kΩ)	R_2 (k Ω)
0.8	Short	Open
0.9	10.0	80.6
1.0	19.6	78.7
1.05	24.3	78.7
1.1	24.9	66.5
1.2	33.2	66.5
1.5	43.2	49.9
1.8	41.2	33.2
2.5	42.2	20.0
3.3	61.9	20.0

NOTE: $V_{OUT} = 0.8 \times (1 + R_1/R_2)$

Resistors in the table are standard 1% types

ORDERING INFORMATION

Device	Nominal Output Voltage	Marking	Marking Rotation	Option	Package	Shipping [†]
NCP133AMX090TCG	0.90 V	D	90°	Output Active Discharge	XDFN6 (Pb-Free)	3000 or 5000 / Tape & Reel (Note 9)
NCP133AMX105TCG	1.05 V	4	0°	Output Active Discharge	XDFN6 (Pb-Free)	3000 or 5000 / Tape & Reel (Note 9)
NCP133AMX115TCG	1.15 V	Т	90°	Output Active Discharge	XDFN6 (Pb-Free)	3000 or 5000 / Tape & Reel (Note 9)
NCP133AMX120TCG	1.20 V	6	0°	Output Active Discharge	XDFN6 (Pb-Free)	3000 or 5000 / Tape & Reel (Note 9)
NCP133AMX125TCG	1.25 V	E	90°	Output Active Discharge	XDFN6 (Pb-Free)	3000 or 5000 / Tape & Reel (Note 9)
NCP133AMXADJTCG	ADJ	K	90°	Output Active Discharge	XDFN6 (Pb-Free)	3000 or 5000 / Tape & Reel (Note 9)

DISCONTINUED (Note 10)

NCP133AMX090TAG	0.90 V	D	90°	Output Active Discharge	XDFN6 (Pb-Free)	3000 or 5000 / Tape & Reel (Note 9)
NCP133AMX100TCG	1.00 V	3	0°	Output Active Discharge	XDFN6 (Pb-Free)	3000 / Tape & Reel
NCP133AMX110TCG	1.10 V	5	0°	Output Active Discharge	XDFN6 (Pb-Free)	3000 / Tape & Reel
NCP133AMX130TCG	1.30 V	F	90°	Output Active Discharge	XDFN6 (Pb-Free)	3000 / Tape & Reel
NCP133AMX150TCG	1.50 V	J	90°	Output Active Discharge	XDFN6 (Pb-Free)	3000 / Tape & Reel
NCP133AMX180TCG	1.80 V	Q	90°	Output Active Discharge	XDFN6 (Pb-Free)	3000 / Tape & Reel
NCP133BMXADJTCG	ADJ	Р	90°	Non-Active Discharge	XDFN6 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

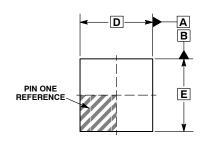
To order other package and voltage variants, please contact your onsemi sales representative

^{9.} Product processed after October 1, 2022 are shipped with quantity 5000 units / Tape & Reel.
10. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

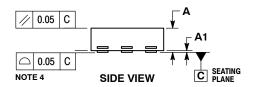


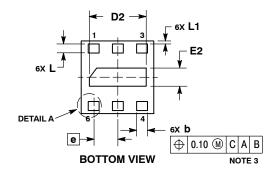
XDFN6 1.20x1.20, 0.40P CASE 711AT ISSUE C

DATE 04 DEC 2015











DETAIL A OPTIONAL CONSTRUCTION

- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
- DIMENSION b APPLIES TO THE PLATED TERMINALS.
- COPLANARITY APPLIES TO THE PAD AS WELL AS THE TERMINALS.

	MILLIMETERS						
DIM	MIN TYP MAX						
Α	0.30	0.37	0.45				
A1	0.00	0.03	0.05				
b	0.13	0.18	0.23				
D	1.15	1.20	1.25				
D2	0.84	0.94	1.04				
E	1.15	1.20	1.25				
E2	0.20	0.30	0.40				
е	0.40 BSC						
L	0.15	0.20	0.25				
L1	0.00	0.05	0.10				

GENERIC MARKING DIAGRAM*

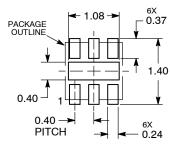


XX = Specific Device Code = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "

", may or may not be present.

RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	XDFN6, 1.20 X 1.20, 0.40P		PAGE 1 OF 1		

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