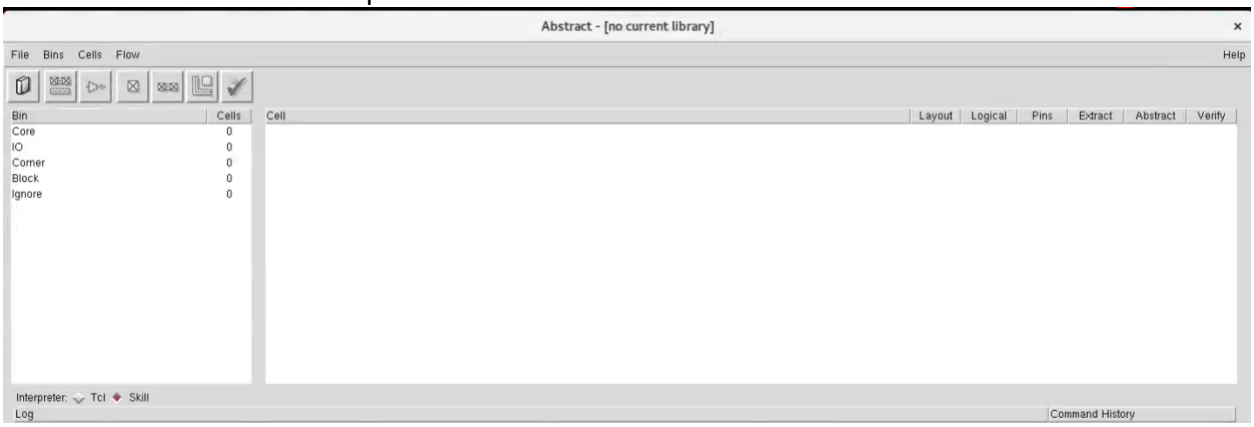
Abstract View Generation

Example shown is for inverter. It's better if you generate Abstract view after you are done drawing all layouts of project 4.

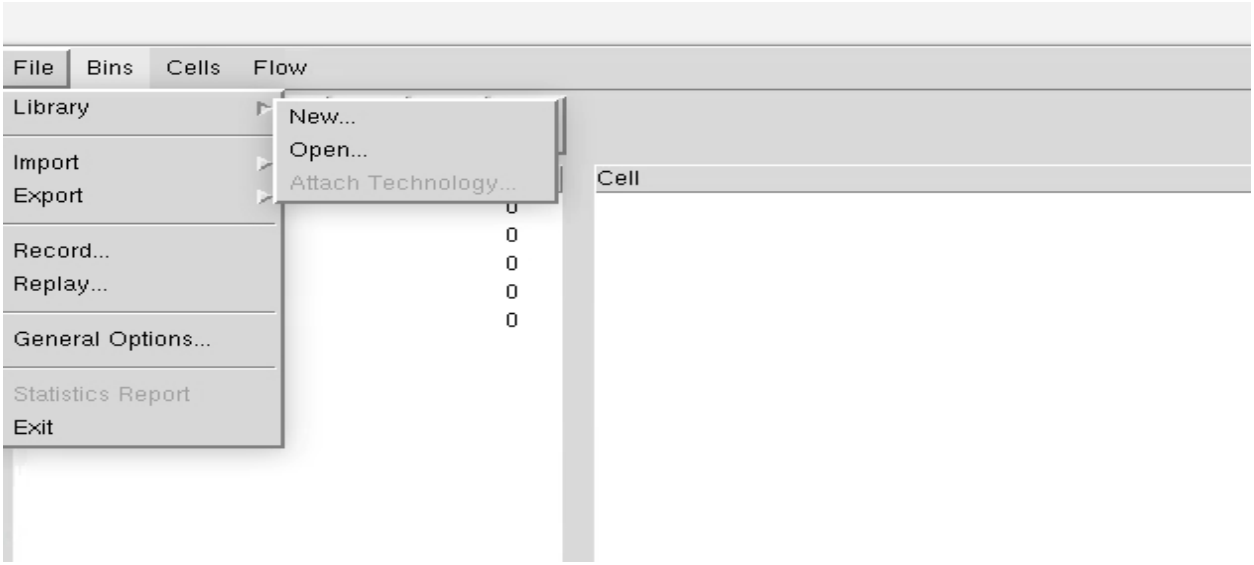
1) After opening Virtuoso in your terminal, type "abstract &" in the same terminal.

```
{engnx10:~/cad/gf65} virtuoso &
[1] 20225
{engnx10:~/cad/gf65} WARNING: HOST <engnx10.utdallas.edu> DOES NOT APPEAR TO BE A CADENCE SUPPORTED LINUX CONFIGURATION.
         For More Info,  Please Run '<cdsroot>/tools.lnx86/bin/checkSysConf' <productId>.

*WARNING* file /home/eng/v/vks160030/CDS.log cls: Unable to connect to clsbd on host "engnx01.utdallas.edu".
Check if clsbd is running on the host. If the host is not valid remove
the ".cdslck" lock file. The connect timeout length can be set using
the CLS_CLSBD_CONNECT_TIMEOUT environment variable.

abstract &
```

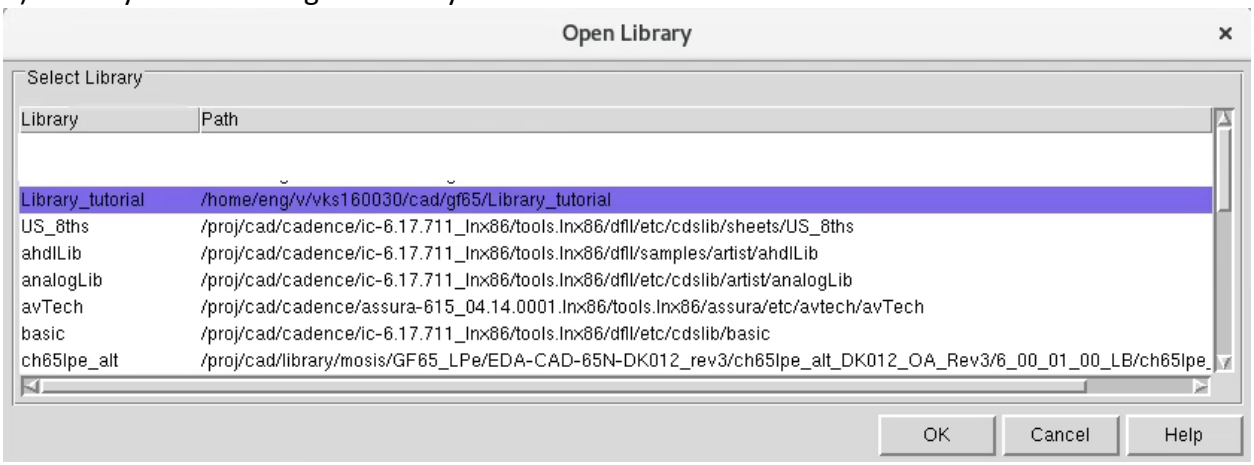
The window shown below opens



2) Click on **File** -> **Open**

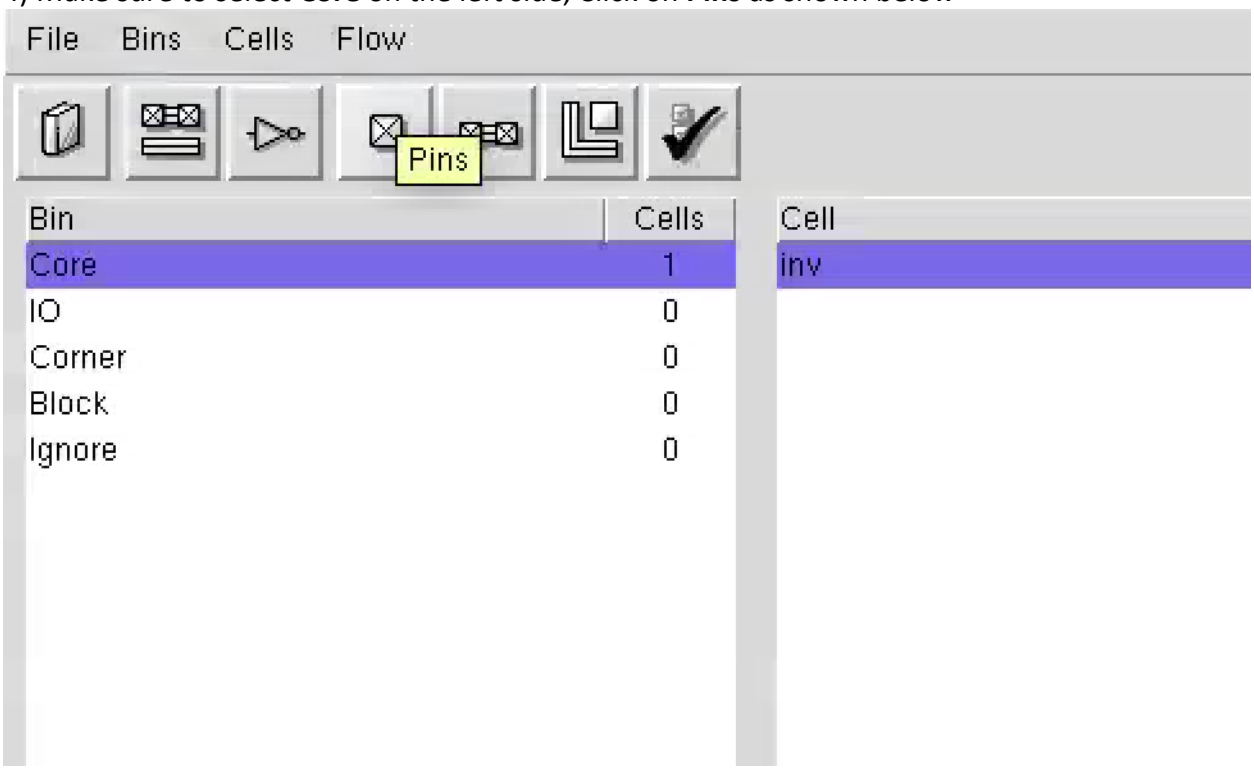


3) Select your own designed library

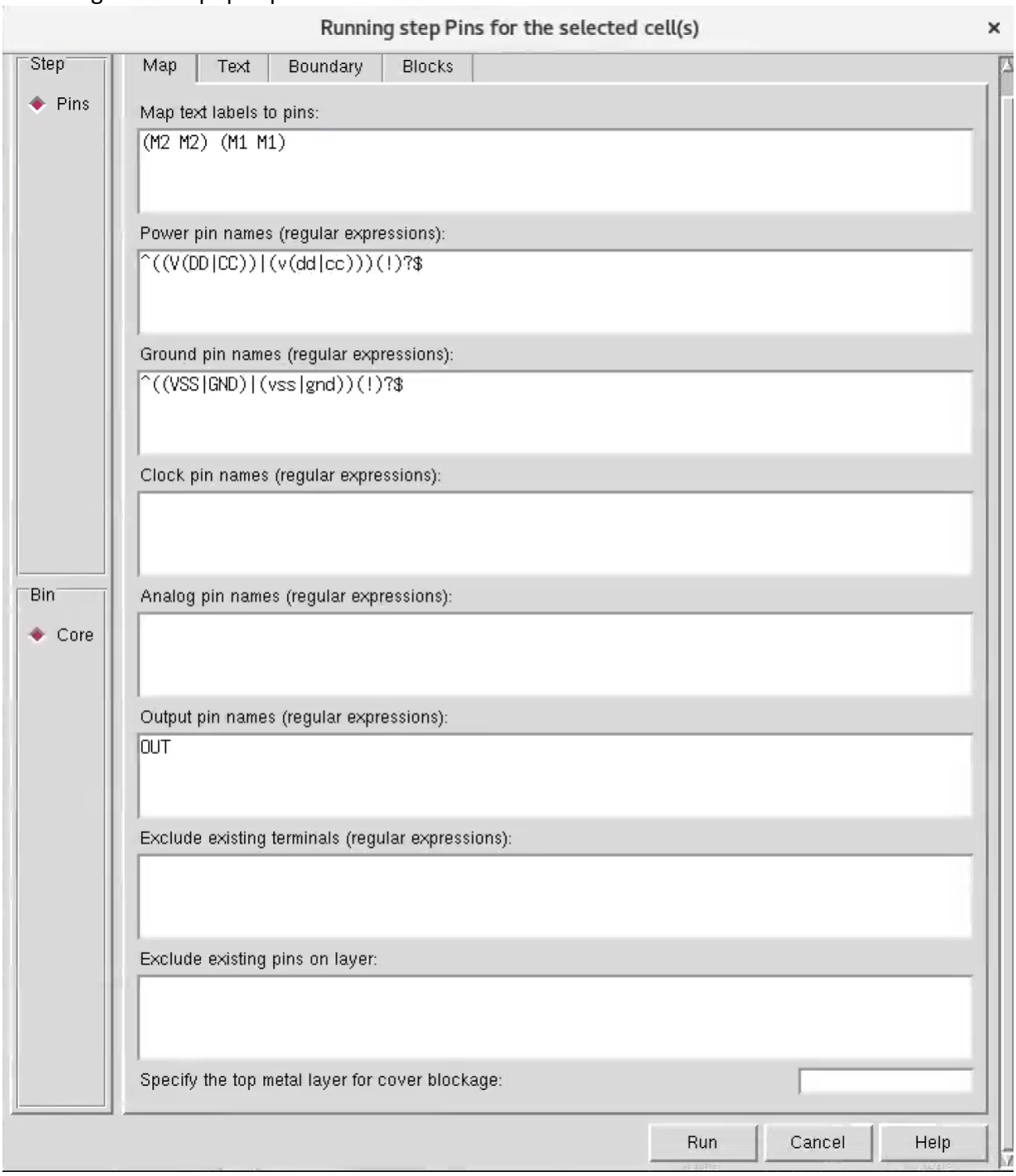


Click **OK**

4) Make sure to select **Core** on the left side, Click on **Pins** as shown below



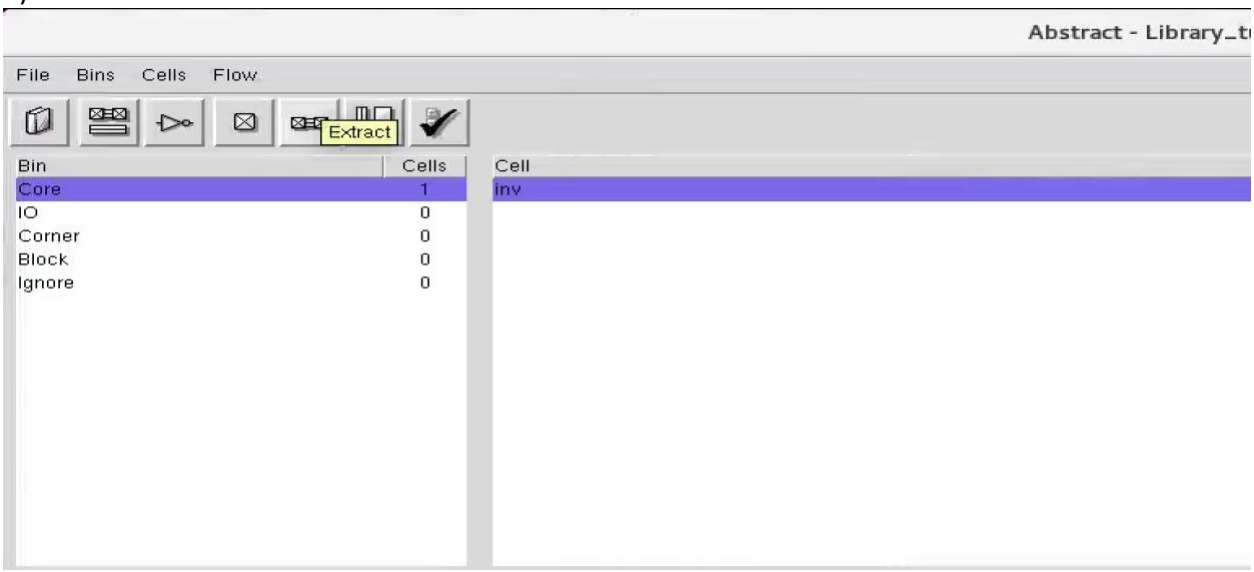
Following window pops up

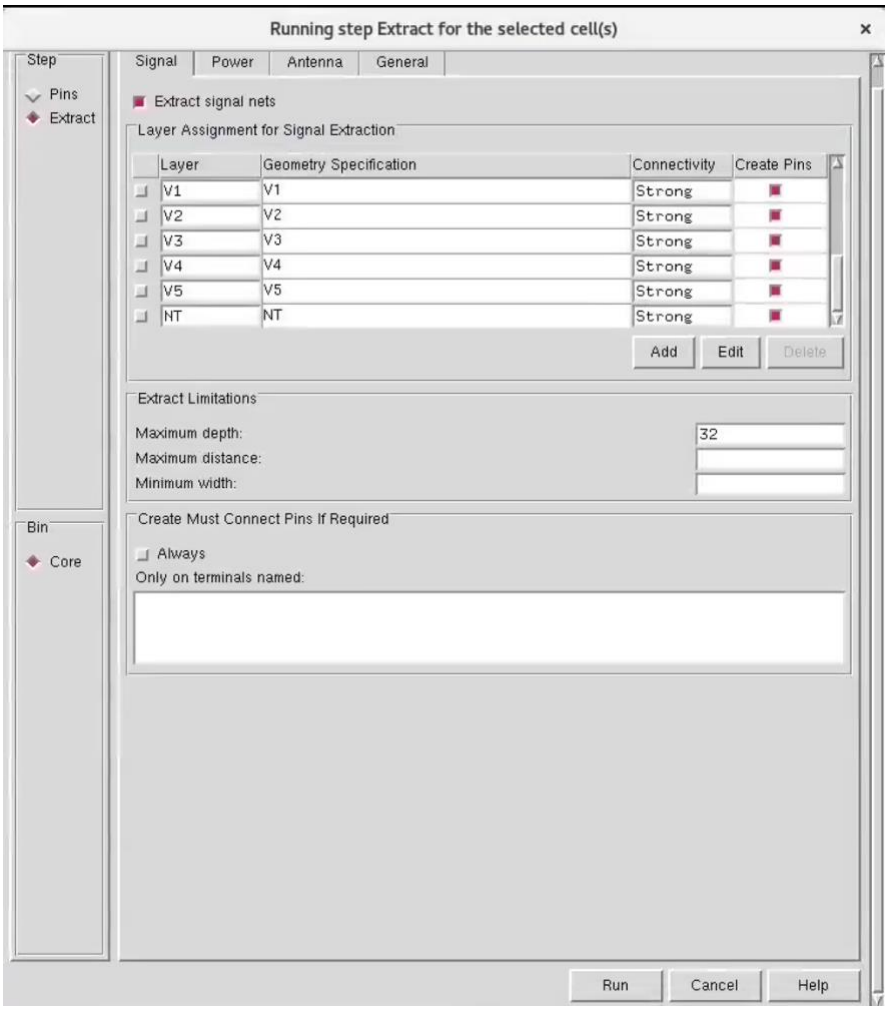


Click **Run**

Ignore the warnings.

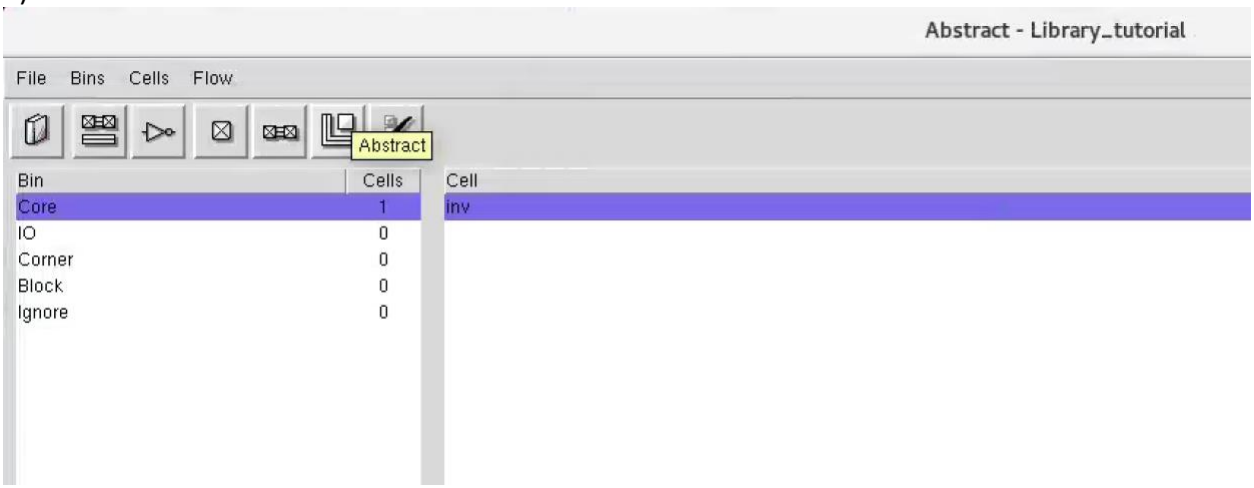
5) Click on **Extract**

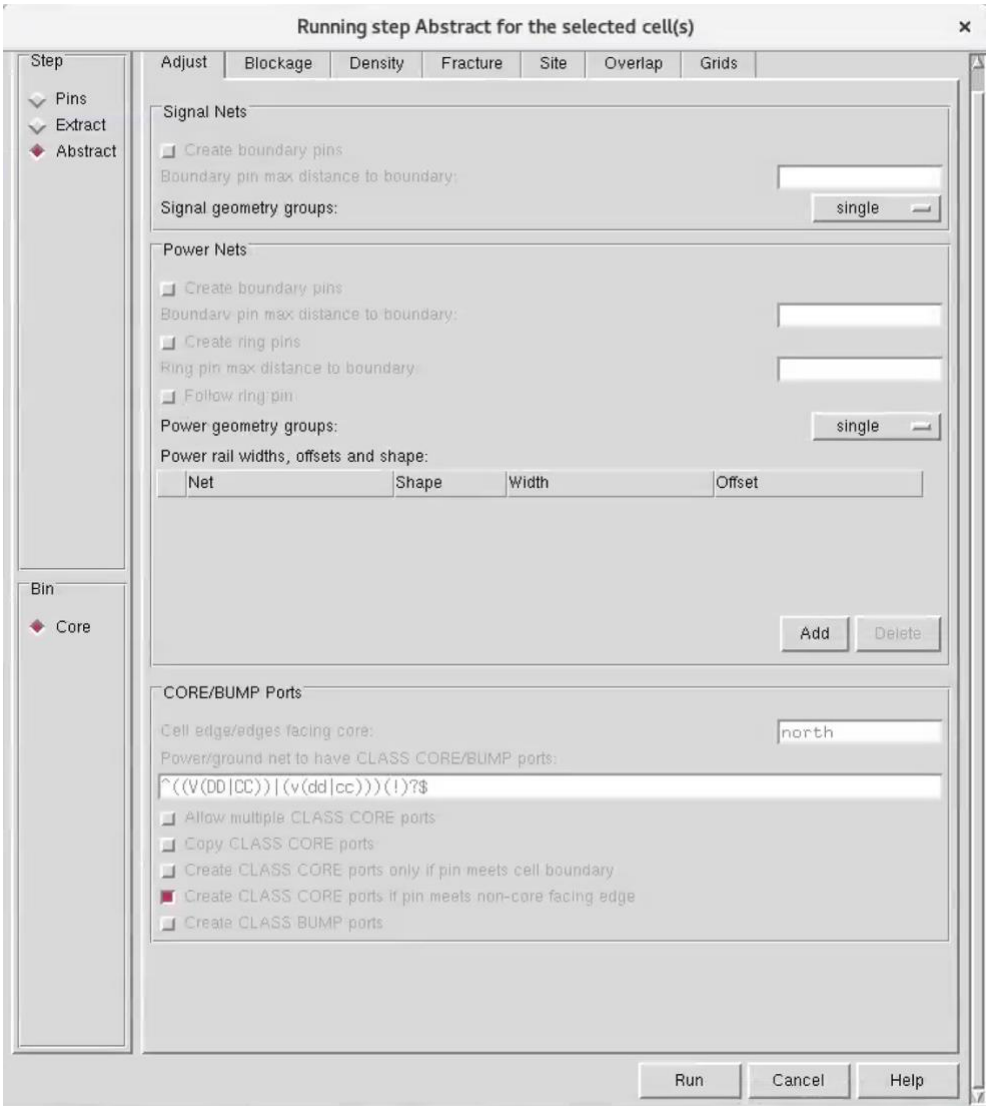




Click **Run**

6) Click on **Abstract**



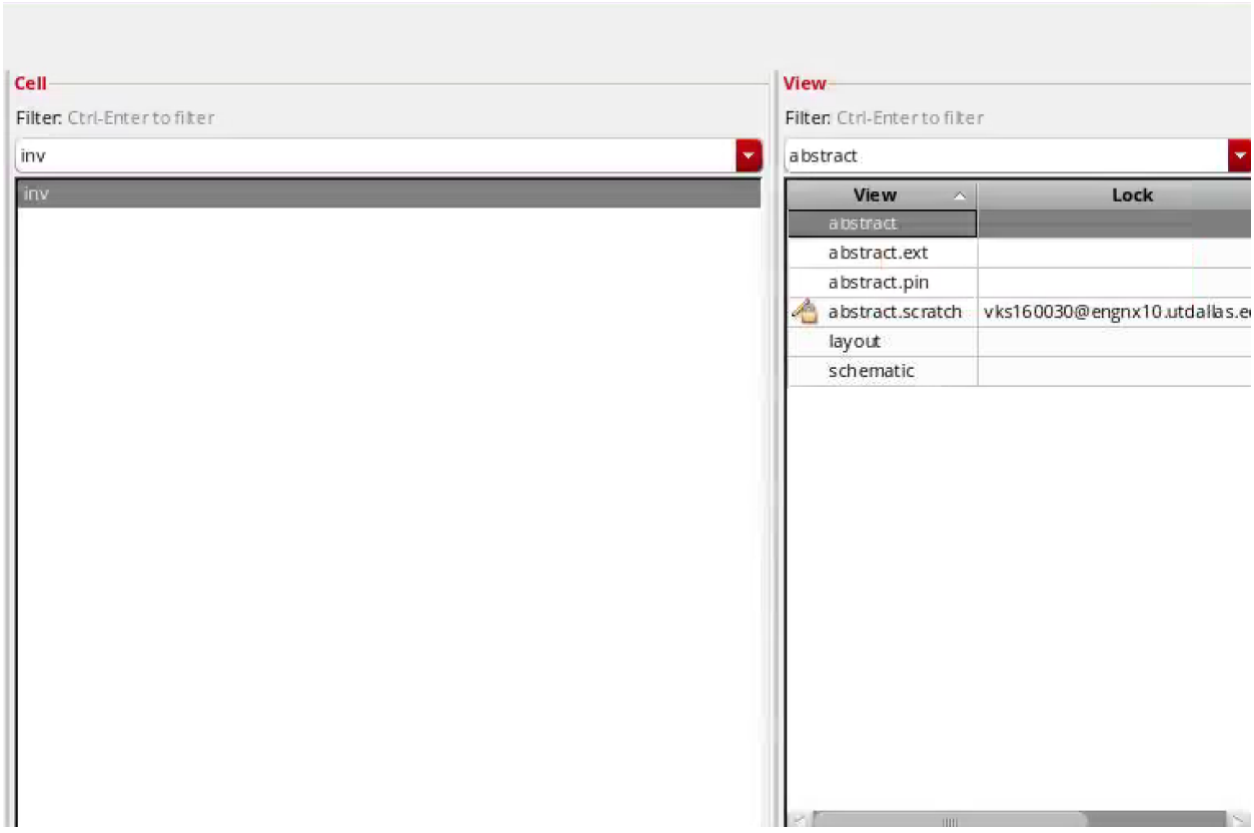


Click **Run**

After completing Abstract generation, this is how the window looks:

Ignore all warnings.

7) Go to **Library Manager** in your Virtuoso window and check the abstract view.



8) Your abstract should look similar to the one shown below