

# **PROJECT 4**

**CE 6325.001 VLSI DESIGN**

**PROJECT :**

**CELL LIBRARY DESIGN AND LAYOUT**  
**(INV, NAND2, NOR2, XOR2, MUX2:1,**  
**AOI21, OAI22, AOI211)**

**TEAM MEMBERS:**

- 1) ALEXANDRA EDWINRAJ (NET ID: AXE210023)**
- 2) HEENISHA REDDY BACHUGUDEM (NET ID: HXR210022)**
- 3) KANUPRIYA SHARMA (NET ID: KXS220016)**

## **OBJECTIVE**

In this project, the below-mentioned cells are designed and laid out to form a cell library,

- INVERTER
- NAND2
- NOR2
- XOR2
- MUX2:1
- OAI211
- OAI22
- AOI21

All the cells mentioned above were placed next to each other with their boundaries touching each other. There were no DRC errors when we checked the cells individually and when they were put together.

# INVERTER

## INVERTER SCHEMATIC:

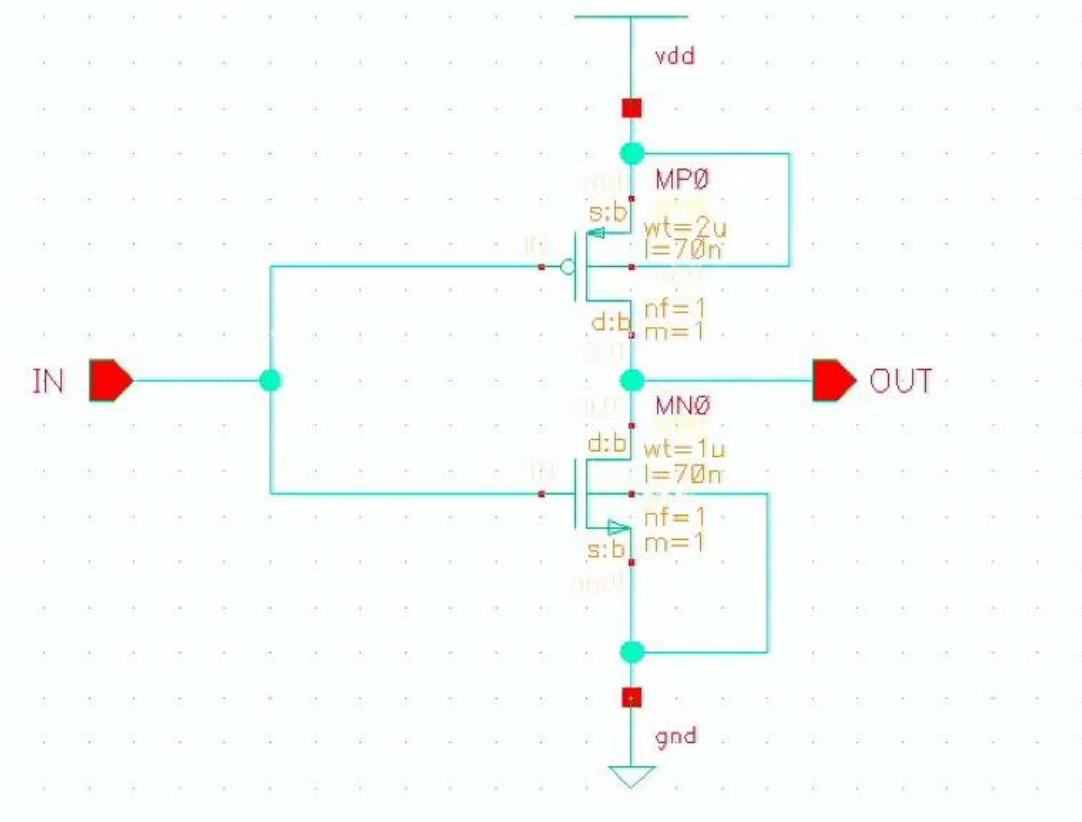
We generated a schematic view of the inverter using the cmos10lpe and analogLib libraries on the Cadence Virtuoso and set the width and length of the MOSFETs as follows:

### P-MOS

- Width of a single finger and all finger - 2um
- Length of the channel - 70nm

### N-MOS

- Width of a single finger and all finger - 1um
- Length of the channel - 70nm

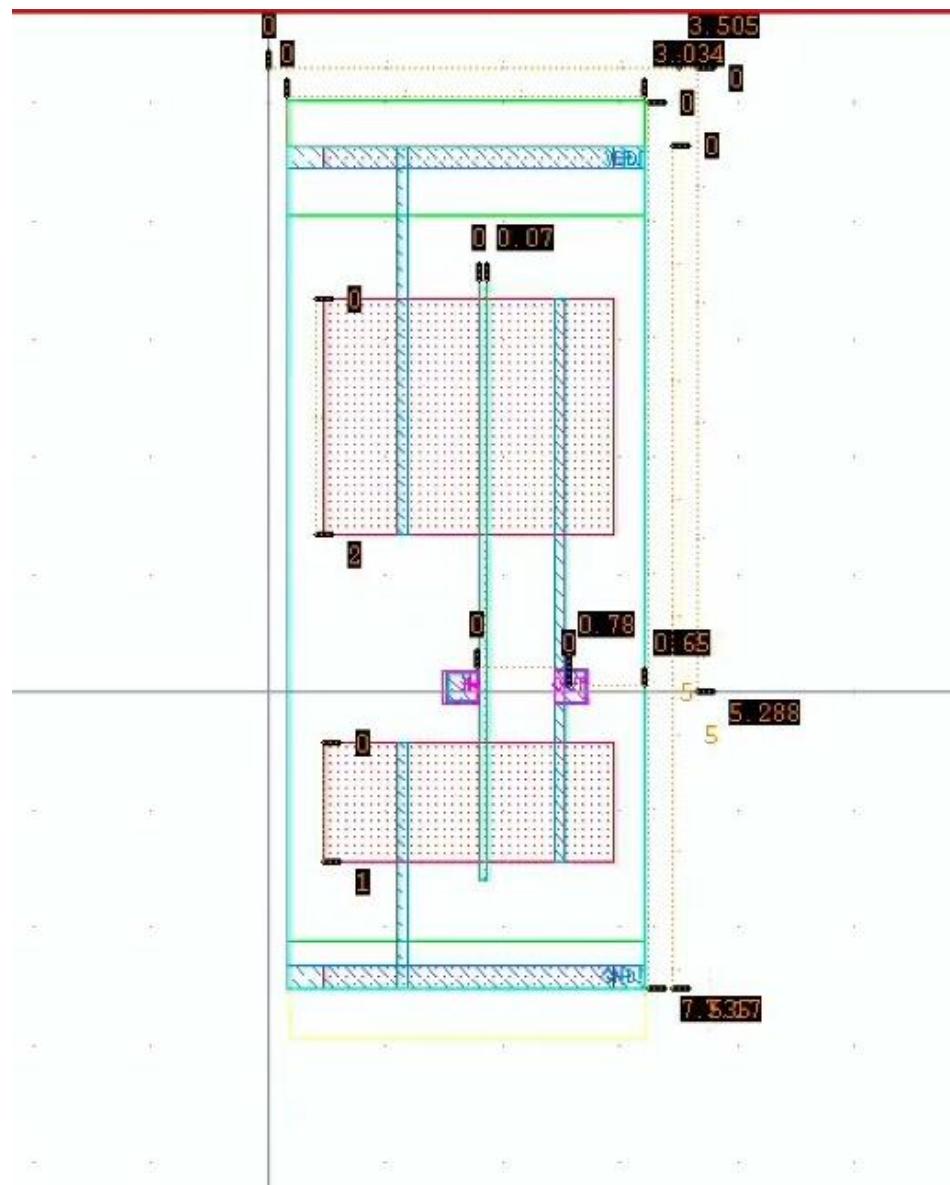


## INVERTER LAYOUT:

Using Cadence Virtuoso, we designed a layout view of the inverter using different cells. We measured each cell with extreme accuracy and connected them together in such a way that they performed their function perfectly.

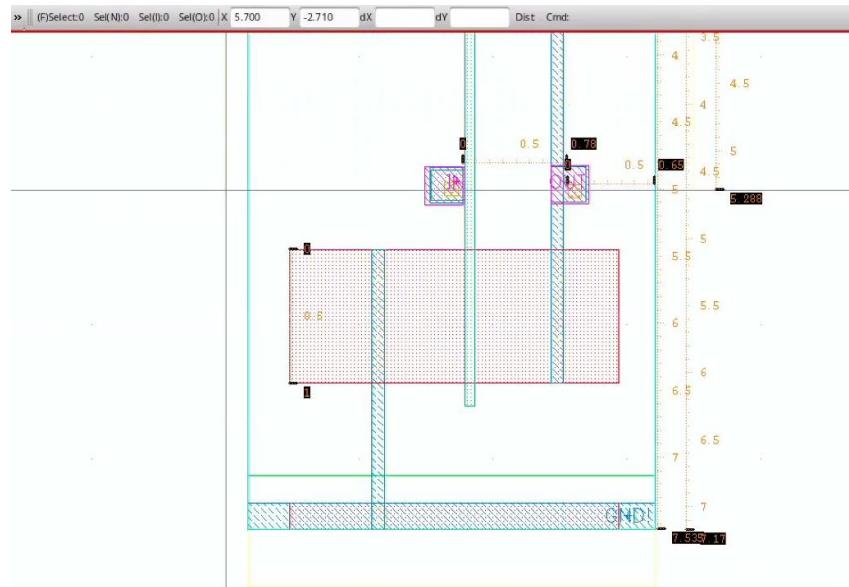
Every contact in the layout has a dimension=  $0.09 \times 0.09 square.$

- P-MOS has 6 contacts (in pairs)
- N-MOS has 4 contacts (in pairs)

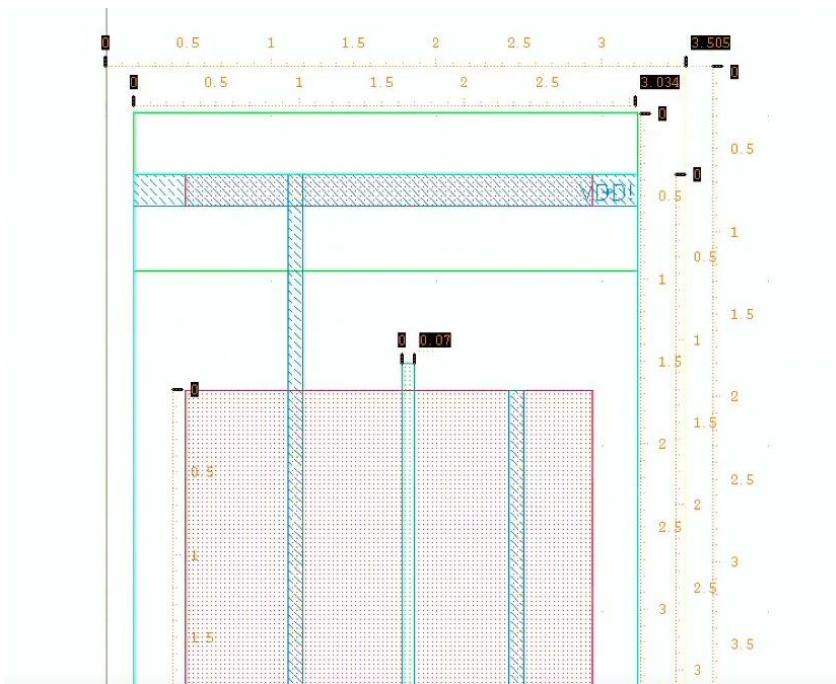


## Dimensions of cell

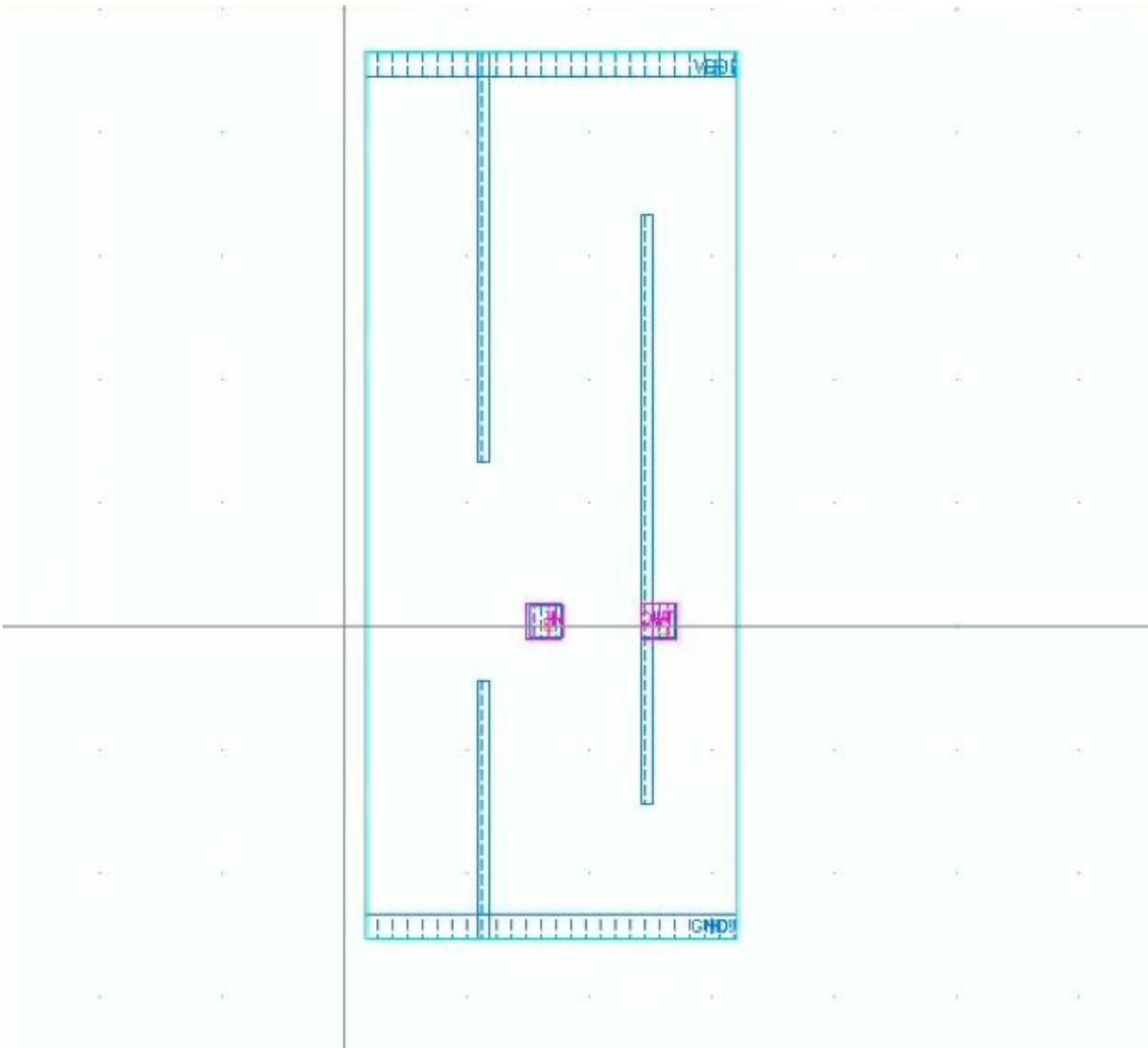
- Height of the cell: 7.535  $\mu\text{m}$



- Width of the cell: 3.034  $\mu\text{m}$

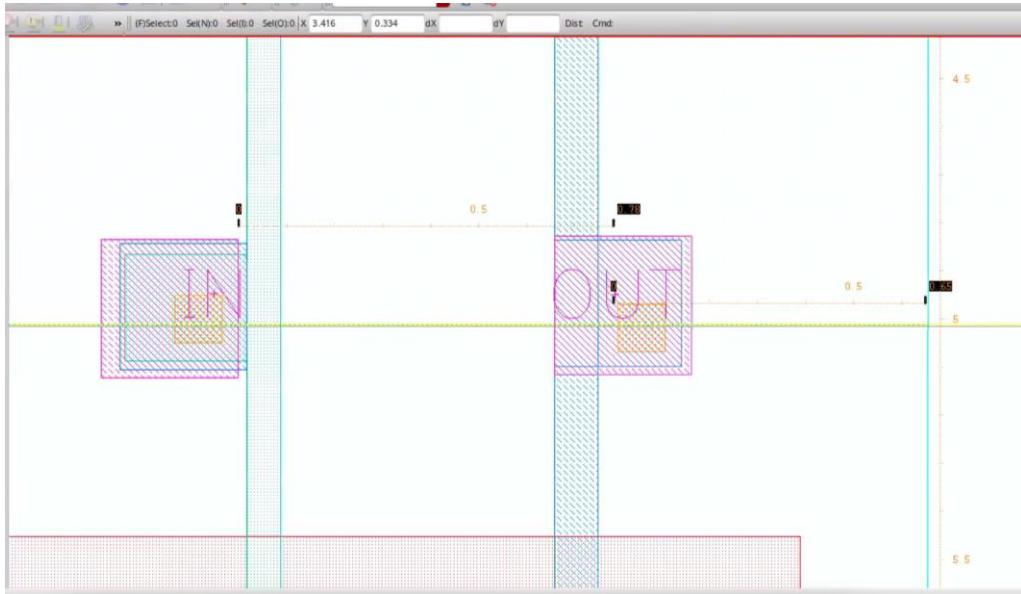


## **INVERTER ABSTRACT:**



## **INVERTER PIN PITCH & OFFSET:**

The pin pitch measurement condition is satisfied, i.e, it has to be in the multiples of 0.26. In this layout the pin pitch is 0.78 as shown in the picture. Offset measurement, on the other hand, should be  $0.13 + 0.26 \times n$  and the layout satisfies that condition. The offset value for the inverter layout is 0.65 as shown in the picture below:



## INVERTER NETLIST:

```

Calibre Interactive - PEX v2013.2_18.13
File Transcript Setup Help
Rules Inputs Outputs Run Control Transcript Run PEX Start RVE
non-top-level nets = 0
degenerate nets = 0
merged nets = 0
error nets = 0

=====
CALIBRE xRC WARNING / ERROR Summary
-----
xRC Warnings = 0
xRC Errors = 0
=====

--- CALIBRE xRC : FORMATTER COMPLETED - Thu Oct 20 16:10:28 2022
--- TOTAL CPU TIME = 1 REAL TIME = 2 LVHEAP = 39/81/467 MALLOC = 29

3 Warnings }

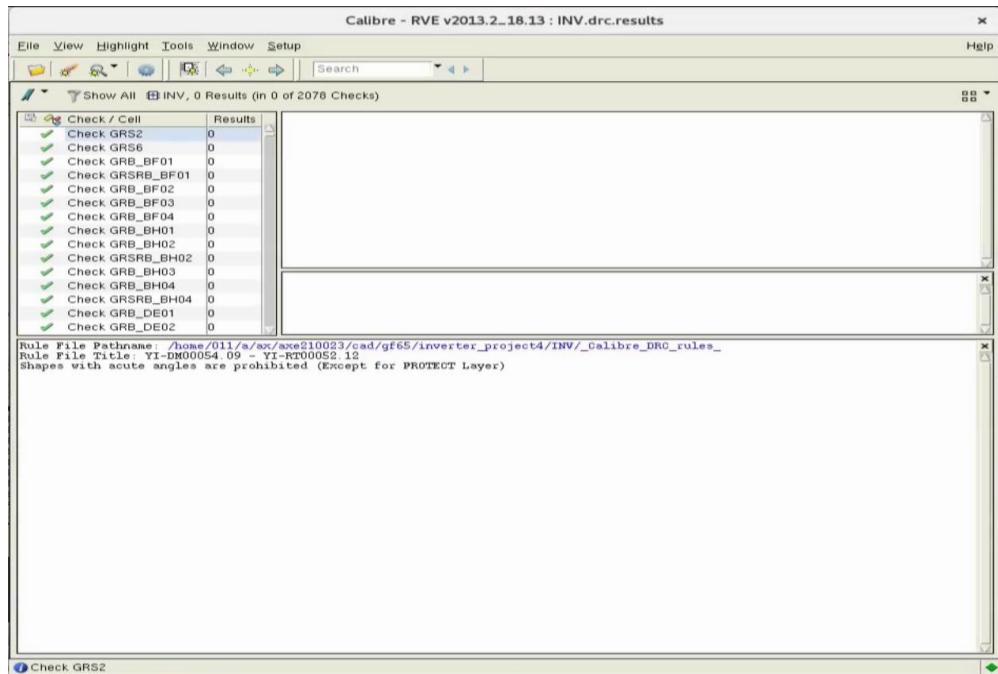
This Linux release is not supported for use with Calibre products.
This Linux release is not supported for use with Calibre products.
This Linux release is not supported for use with Calibre products.

PEX Netlist File - INV.pex.netlist
File Edit Options Windows
+ File: INV.pex.netlist
+ Created: Thu Oct 20 16:10:26 2022
+ Program "Calibre xRC"
+ Version "v2013.2_18.13"
+
include "INV.pex.netlist.pex"
subckt INV GND! OUT VDD! IN
*
* IN IN
* VDD! VDD!
* OUT OUT
* GND! GND!
X00 noxref N_GND!_D0_noxref_pos N_VDD!_D0_noxref_neg DIODENX AREA=1.85396e-1
+ PERIM=1.7592e-05
XMM0 N_OUT MM0N d N_IN MM0N g N_GND!_D0_noxref_pos NFET L=7e-08
+ V=1e-05 AD=1.082e-12 AS=1.31e-12 PD=4.164e-06 PS=4.62e-06 NR=0.16 NRS=0.65
+ M=1 NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.31e-06 SB=1.082e-06 SD=0
+ PANW1=0 PANW2=0 PANW3=0 PANW4=7e-16 PANW5=3.5e-15 PANW6=1e-15 PANW7=1.4e-14
+ PANW8=1.4e-14 PANW9=2.8e-14 PANW10=2.8e-15
XMP0 N_OUT MP0 d N_IN MP0 g N_VDD!_D0_noxref_neg PFET L=7e-08
+ V=2e-05 AD=2.164e-12 AS=2.62e-12 PD=6.164e-06 PS=6.62e-06 NR=0.303 NRS=0.32
+ M=1 NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=1.31e-06 SB=1.082e-06 SD=0
+ PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0 PANW7=0 PANW8=0 PANW9=4.48e-13
+ PANW10=3.2494e-13
+
.include "INV.pex.netlist INV.pxi"
+
.ends
+
```

## INVERTER DRC CHECK :

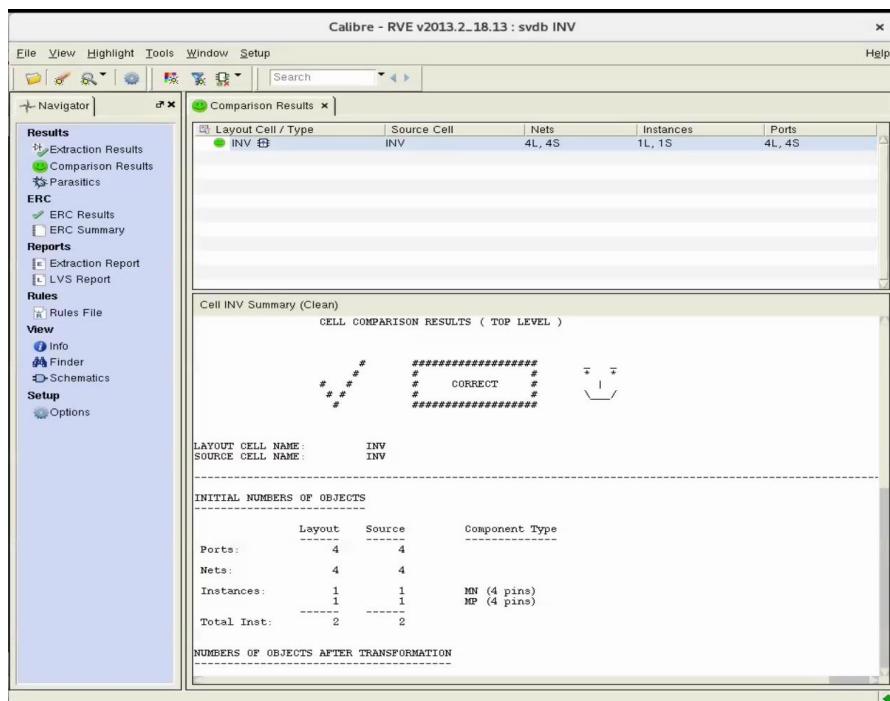
0 DRC errors - Successfully ran the DRC check for INV Layout and the is 0 errors after 2078

## Checks.



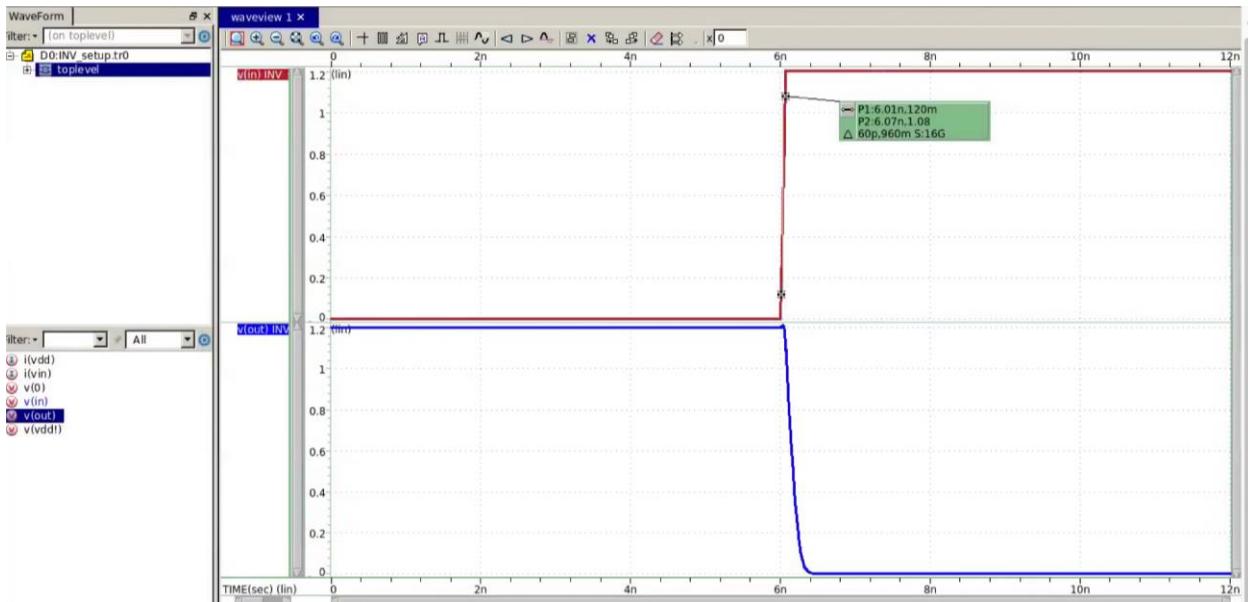
## INVERTER LVS CHECK:

0 LVS errors - Layout and Schematic of the Invertor Gate is **CORRECT**



## INVERTER SIMULATION:

The waveform is generated using the INV netlist and the input slew rate is 60 ps and a 70 fF load capacitance is given to the netlist when simulating.



### INVERTER TRUTH TABLE:

Input	Output
0	1
1	0

### NAND2

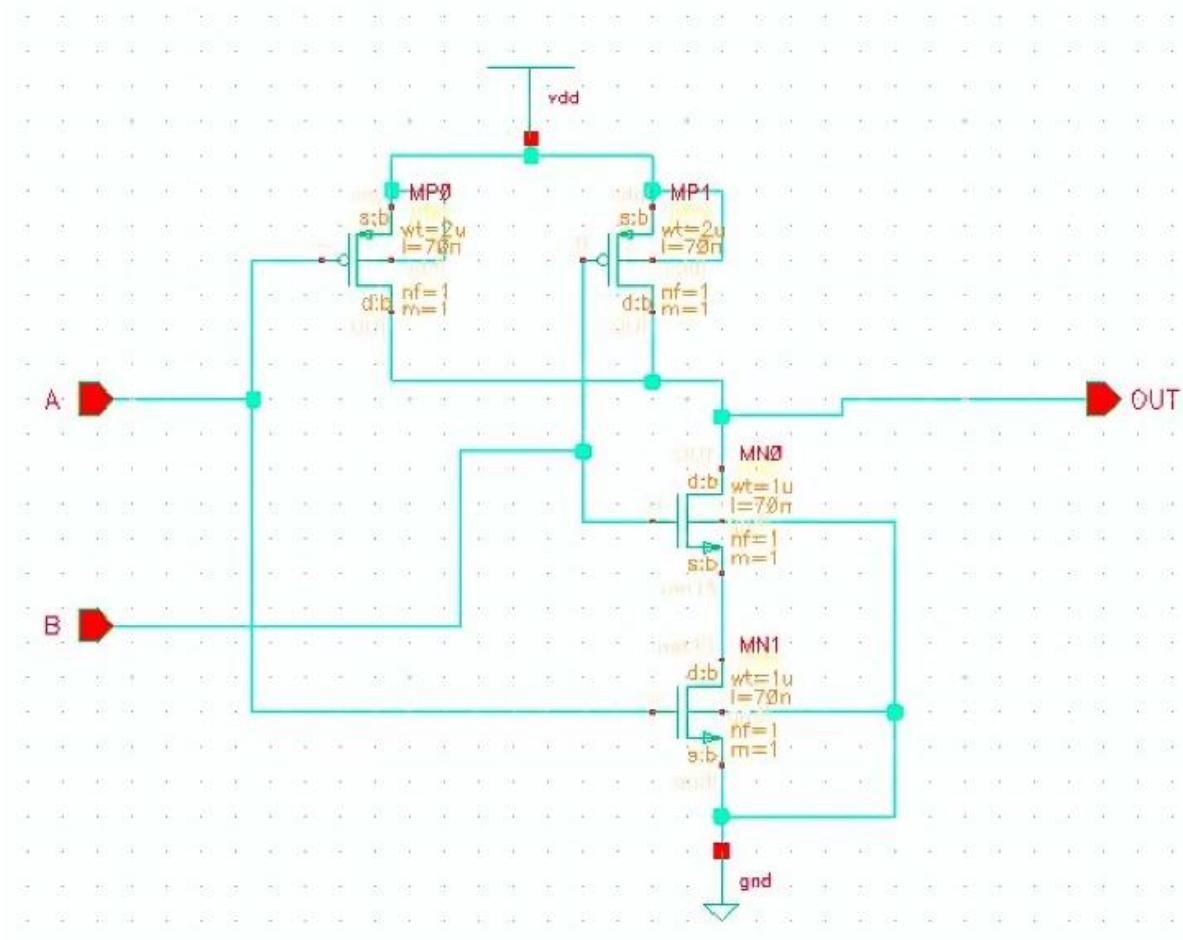
## NAND2 SCHEMATIC:

### P-MOS

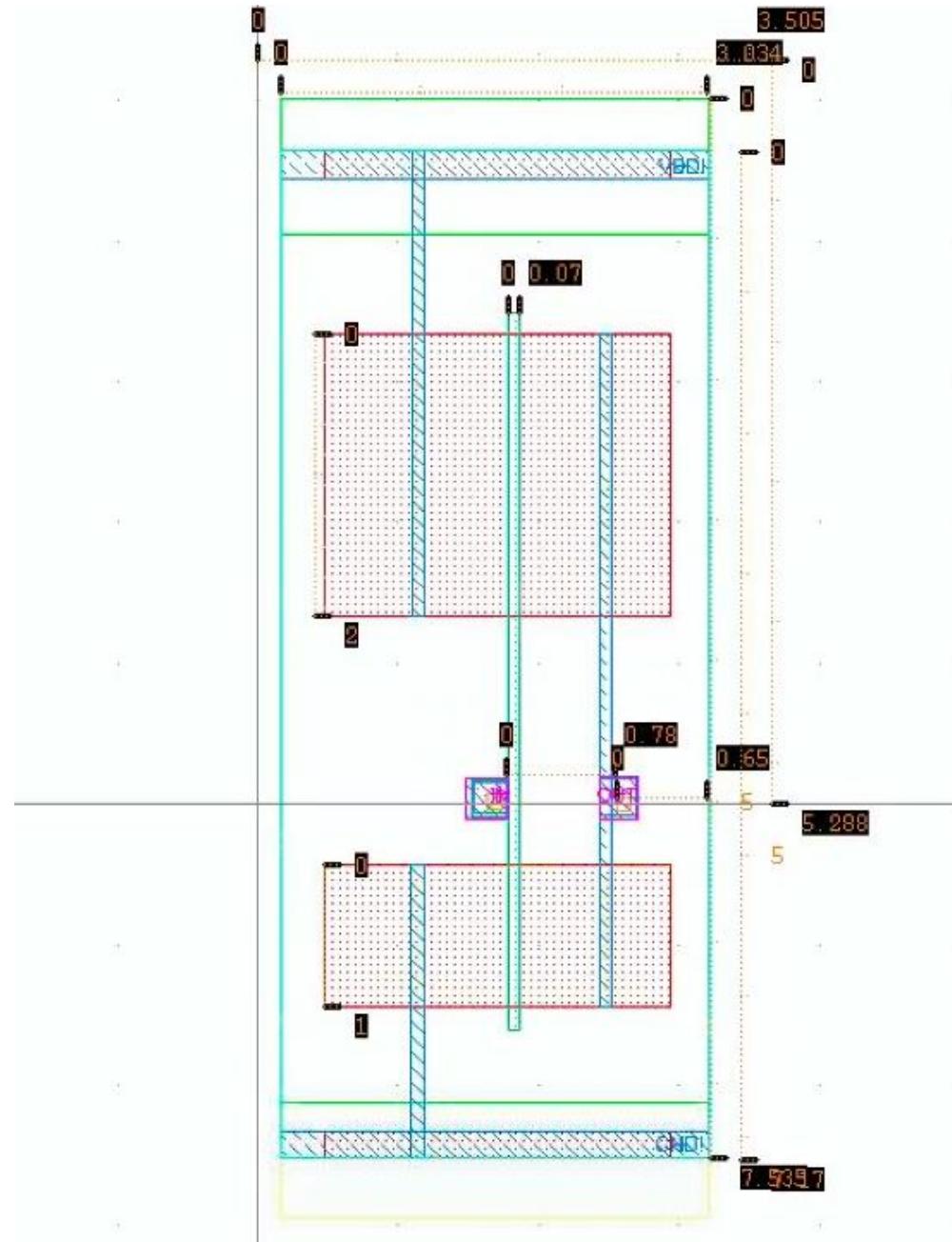
- Width of a single finger and all finger - 2um
- Length of the channel - 70um

### N-MOS

- Width of a single finger and all finger - 1um
- Length of the channel - 70um

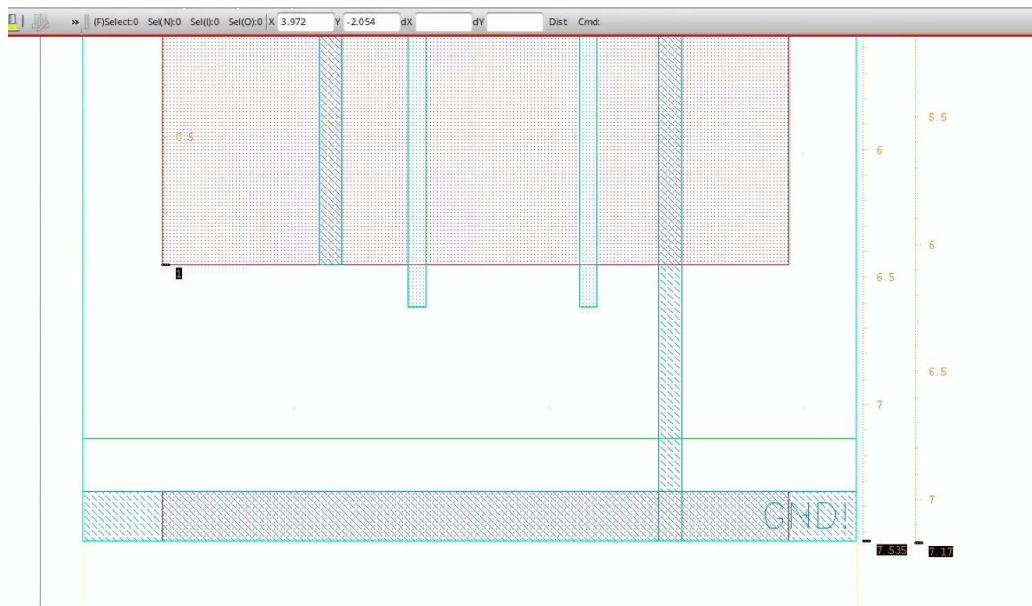


## NAND2 LAYOUT:

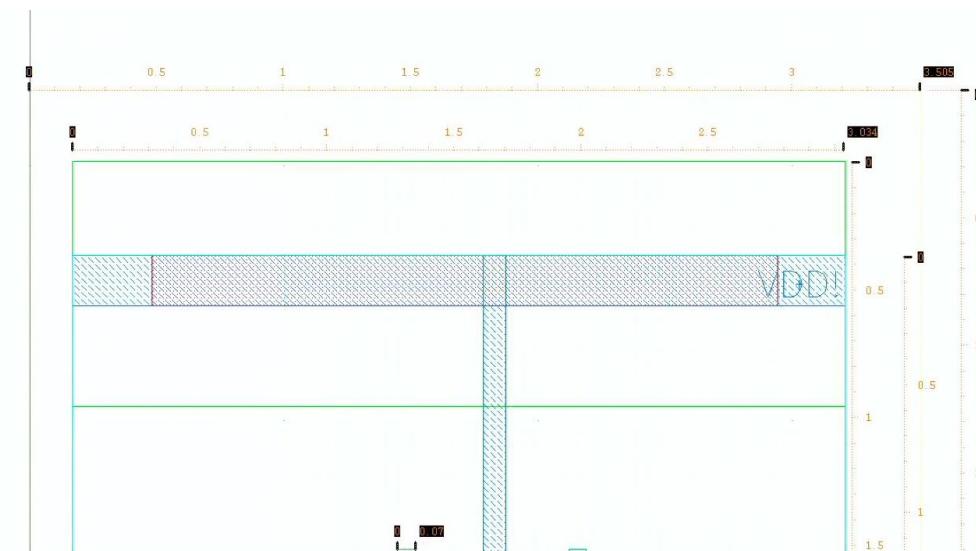


**Dimensions of cell**

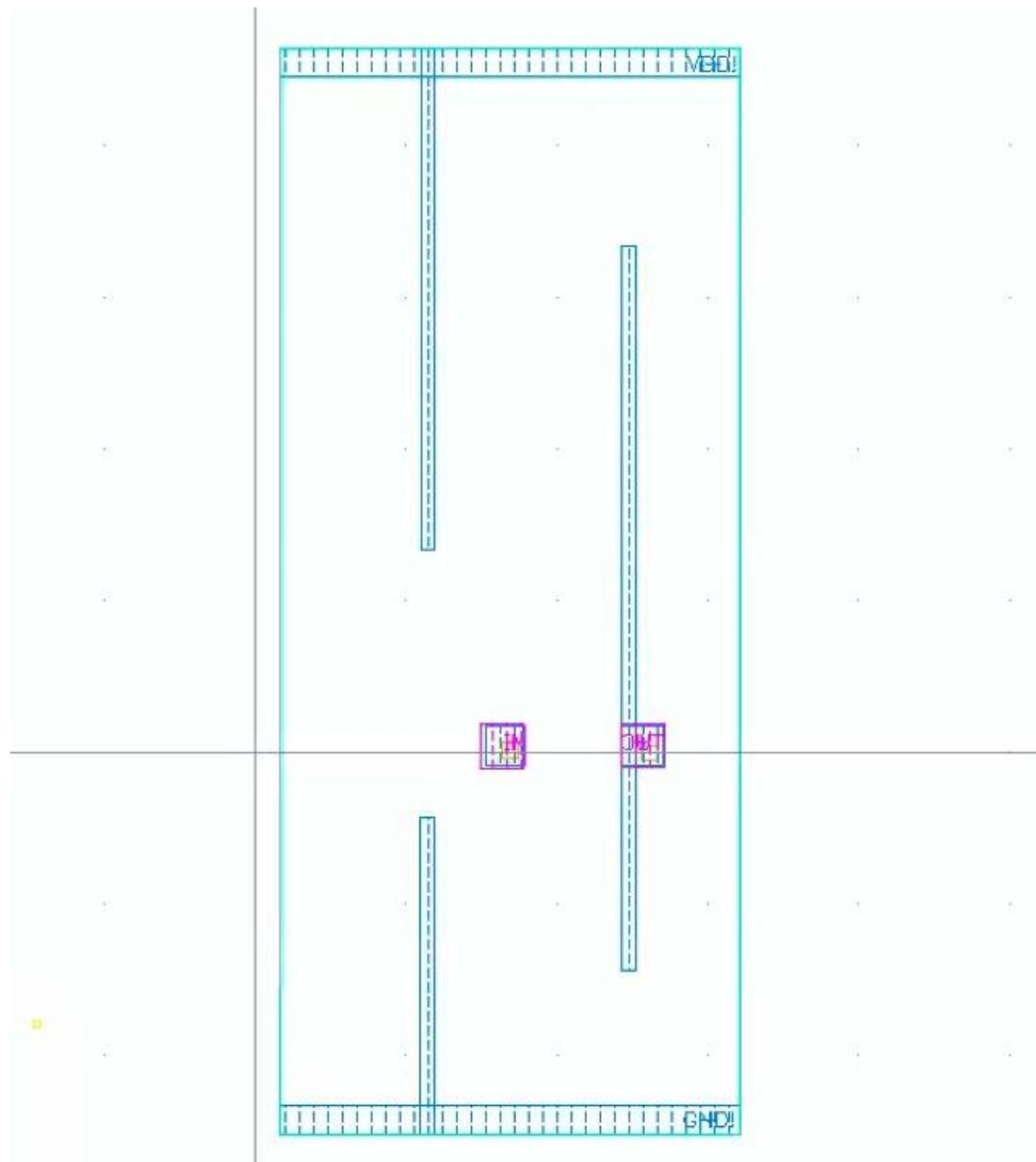
- Height of the cell: 7.535  $\mu\text{m}$



- Width of the cell: 3.034  $\mu\text{m}$



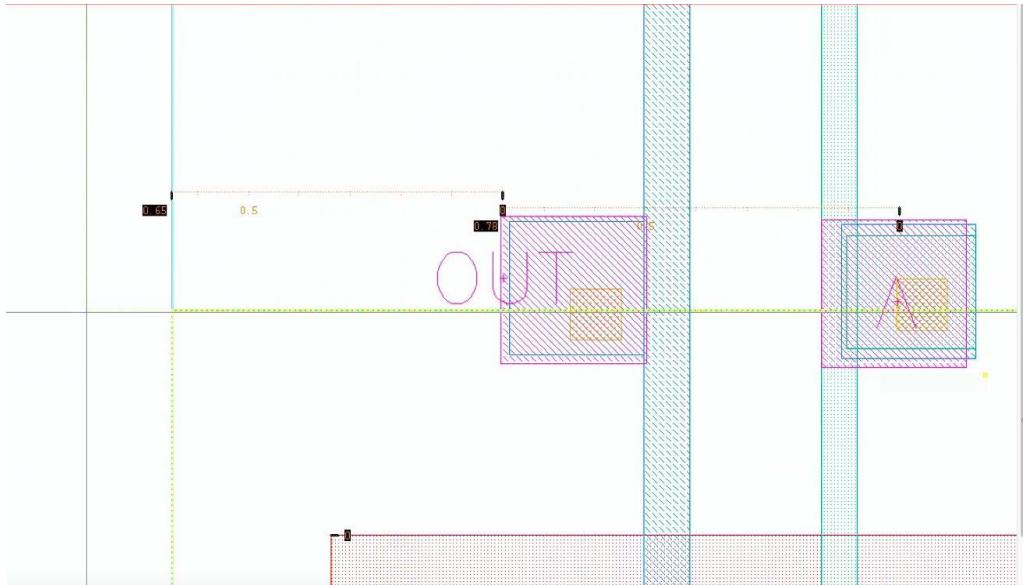
## NAND2 ABSTRACT:



**NAND2 PIN PITCH AND OFFSET:**

The pin pitch and offset measurement requirements are satisfied:

- Pin Pitch=0.78
- Offset=0.65



## NAND2 NETLIST:

Calibre Interactive - PEX v2013.2\_18.13

File Transcript Setup

non-top-level nets = 0  
degenerate nets = 0  
merged nets = 0  
error nets = 0

-----  
CALIBRE xRC WARNING / ERROR Summary  
-----  
xRC Warnings = 0  
xRC Errors = 0

-----  
--- CALIBRE xRC::FORMATTER COMPLETED - Thu Oct 20 16:20:10 2022  
--- TOTAL CPU TIME = 1 REAL TIME = 2 LVHEAP = 39/81/467 MALLOC = 29

-----  
3 Warnings ]

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This Linux release is not supported for use with Calibre products.

PEX Netlist File - NAND2.pex.netlist

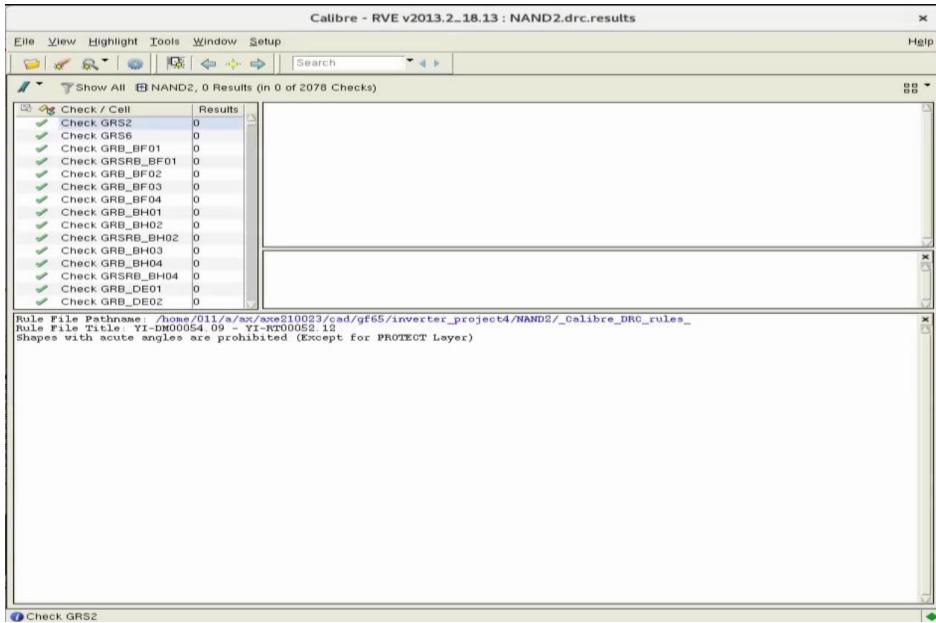
File Edit Options Windows

```
* File: NAND2.pex.netlist
* Created: Thu Oct 20 16:20:08 2022
* Program "Calibre xRC"
* Version "v2013.2_18.13"
*
.inclu...e "NAND2.pex.netlist.pex"
.subckt NAND2 OUT GND! VDD! A B
*
* B B
* A A
* VDD! VDD!
* GND! GND!
* OUT OUT
XDO noxref N GND! D0_noxref_pos N_VDD! D0_noxref_neg DIODENWX AREA=1 85396e-1
+ PERIM=1.7592e-05
XMMN1 N OUT MMN1_d N_A MMN1_g NET15_N_GND! D0_noxref_pos NFET L=7e-08 W=1e-06
+ AD=9.66e-13 AS=3.01e-13 PD=3.932e-06 PS=1.602e-06 NRd=0.305 NRS=0.301 M=1 NF=1
+ CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=9.66e-07 SB=1.426e-06 SD=0 PANV1=0
+ PANV2=0 PANV3=0 PANV4=7e-16 PANV5=3.5e-15 PANV6=7e-15 PANV7=1.4e-14
+ PANV8=1.4e-14 PANV9=2.8e-14 PANV10=2.8e-15
XMMN0 NET15_N_B MMN0_g N_GND! MMN0_s N_GND! D0_noxref_pos NFET L=7e-08 W=1e-06
+ AD=3.01e-13 AS=7.54e-13 PD=1.602e-06 PS=3.508e-06 NRd=0.301 NRS=0.288 M=1 NF=1
+ CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.638e-06 SB=7.54e-07 SD=0 PANV1=0
+ PANV2=0 PANV3=0 PANV4=7e-16 PANV5=3.5e-15 PANV6=7e-15 PANV7=1.4e-14
+ PANV8=1.4e-14 PANV9=2.8e-14 PANV10=2.8e-15
XMP0_N_OUT MP0_d N_A MP0_g N_VDD! MP0_s N_GND! D0_noxref_neg PFET L=7e-08
+ W=2e-05 AD=1.932e-12 AS=6.02e-13 PD=5.932e-06 PS=2.602e-06 NRd=0.1525
+ NRS=0.1555 M=1 NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=9.66e-07
+ SB=1.426e-06 SD=0 PANV1=0 PANV2=0 PANV3=0 PANV4=0 PANV5=0 PANV6=0 PANV7=0
```

## NAND2 DRC CHECK:

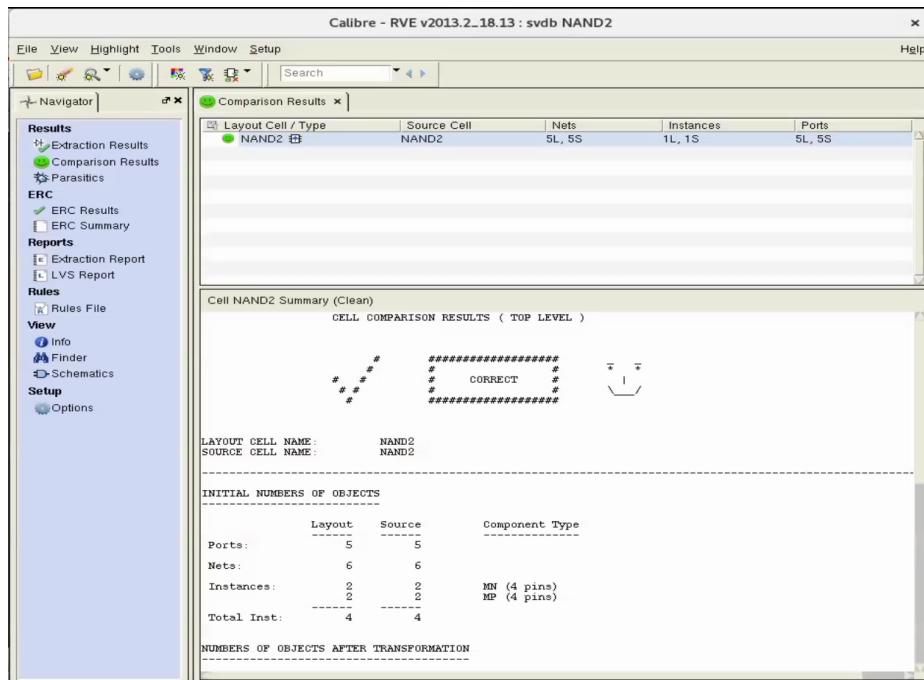
0 DRC errors - Successfully ran the DRC check for NAND2 Layout and there are 0 errors after

2078 Checks.



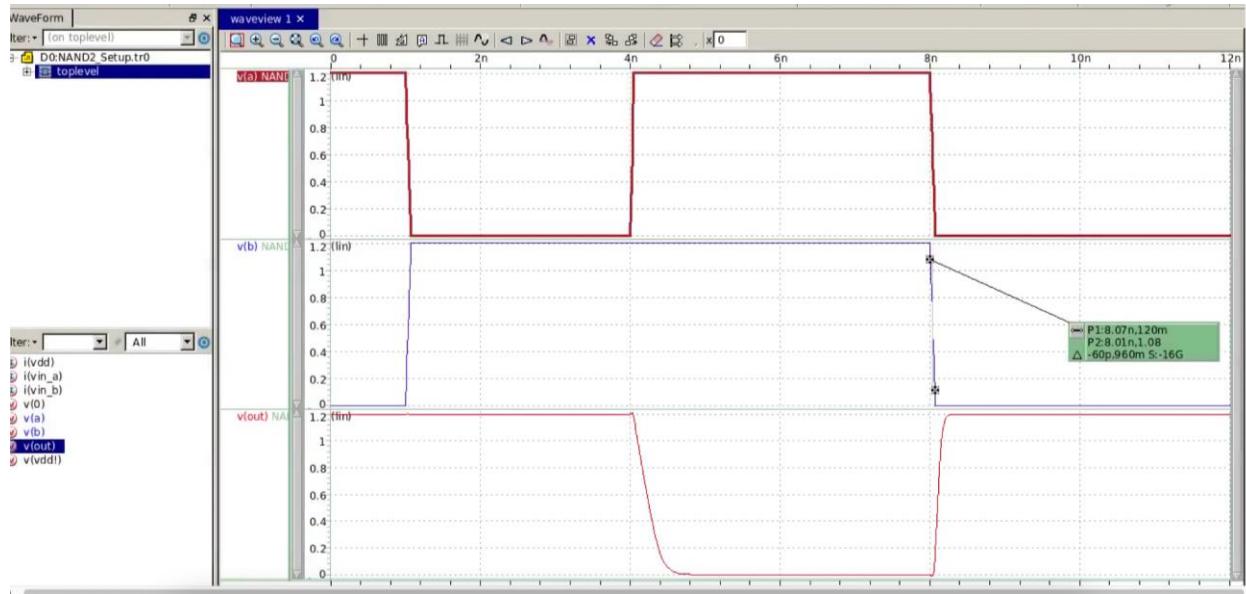
## NAND2 LVS CHECK:

0 LVS errors - Layout and Schematic of the NAND2 Gate is **CORRECT**



## NAND2 SIMULATION:

The waveform is generated using the NAND2 netlist and the input slew rate is 60 ps and a 70 fF load capacitance is given to the netlist when simulating.



### NAND2 TRUTH TABLE:

<b>Input A</b>	<b>Input B</b>	<b>Output</b>
0	0	1
0	1	1
1	0	1
1	1	0

**NOR2**

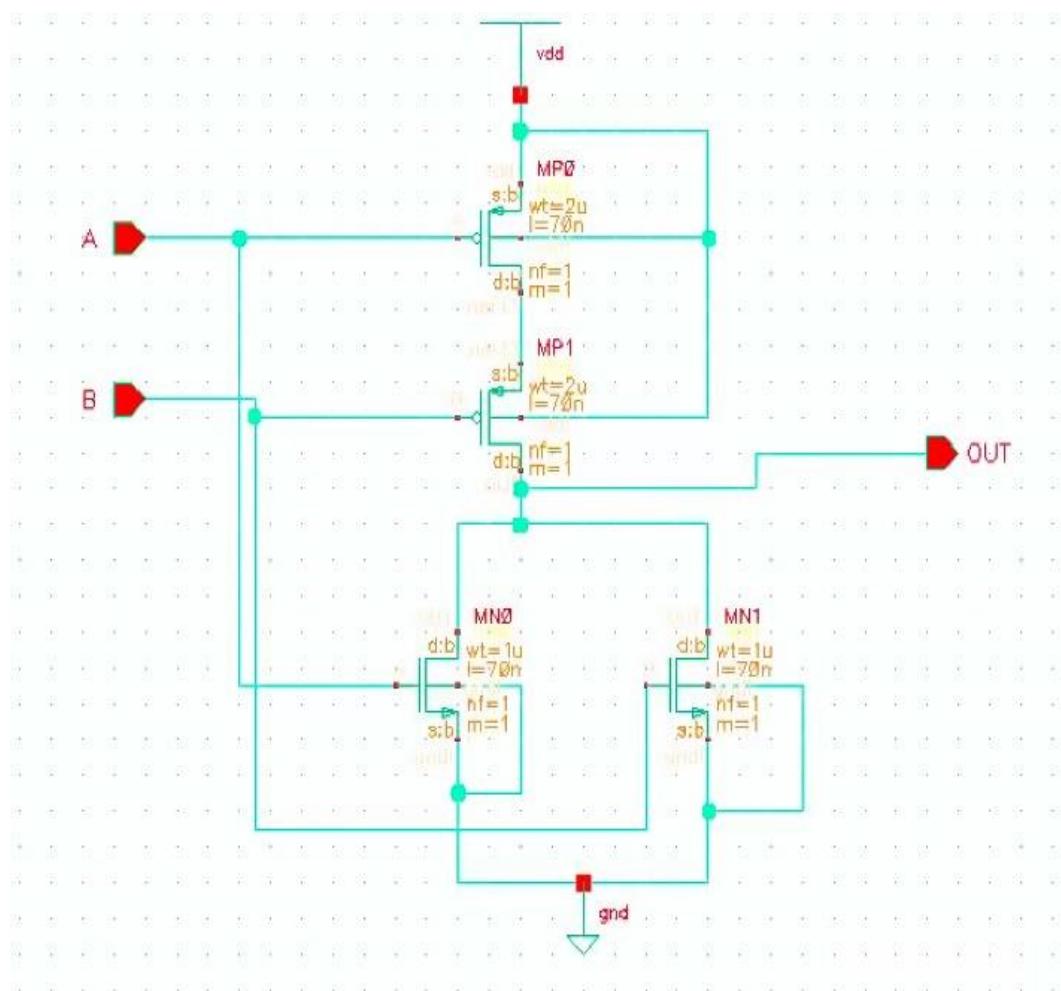
## NOR2 SCHEMATIC:

### P-MOS

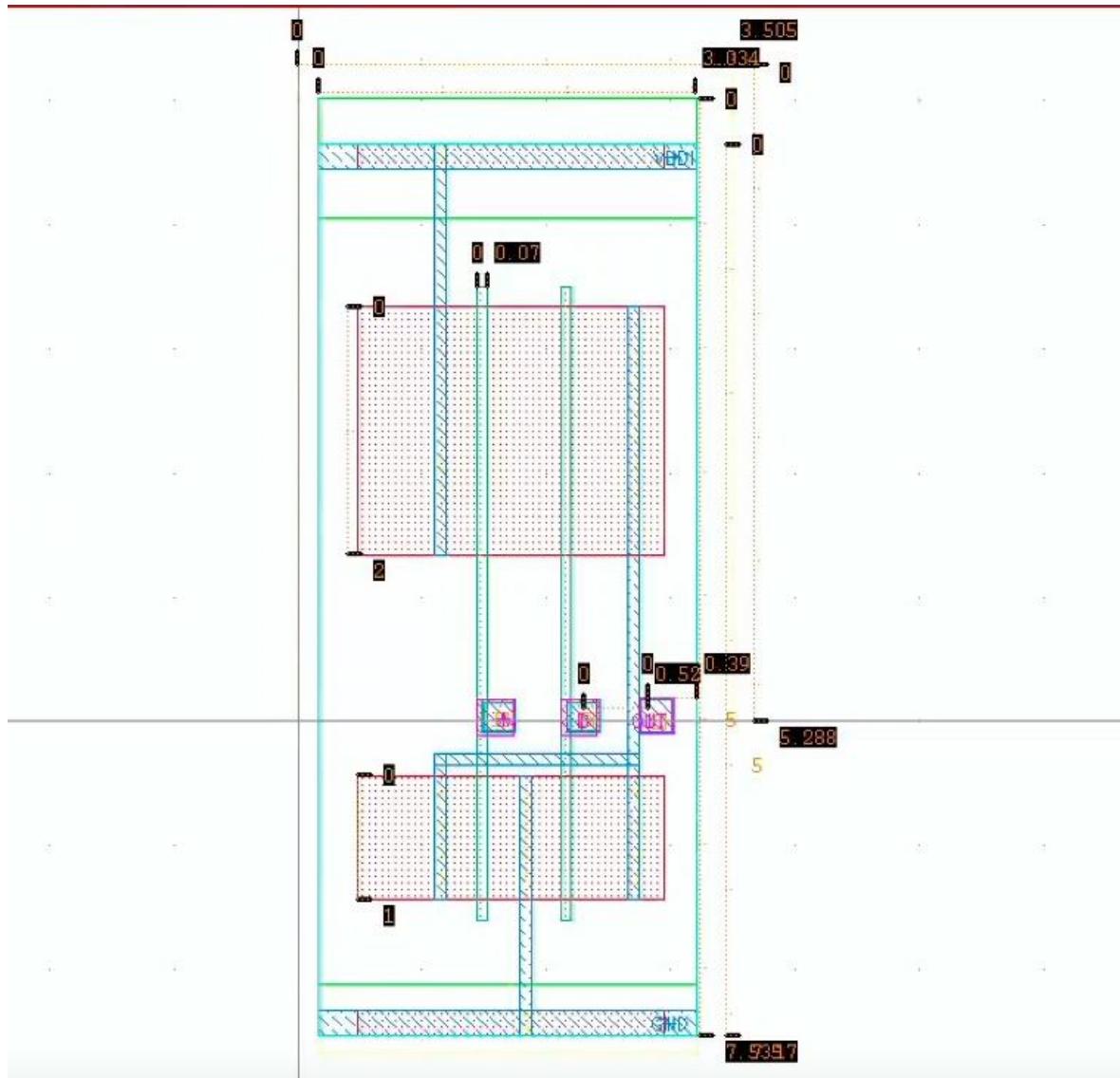
- Width of a single finger and all finger - 2um
- Length of the channel - 70um

### N-MOS

- Width of a single finger and all finger - 1um
- Length of the channel - 70um

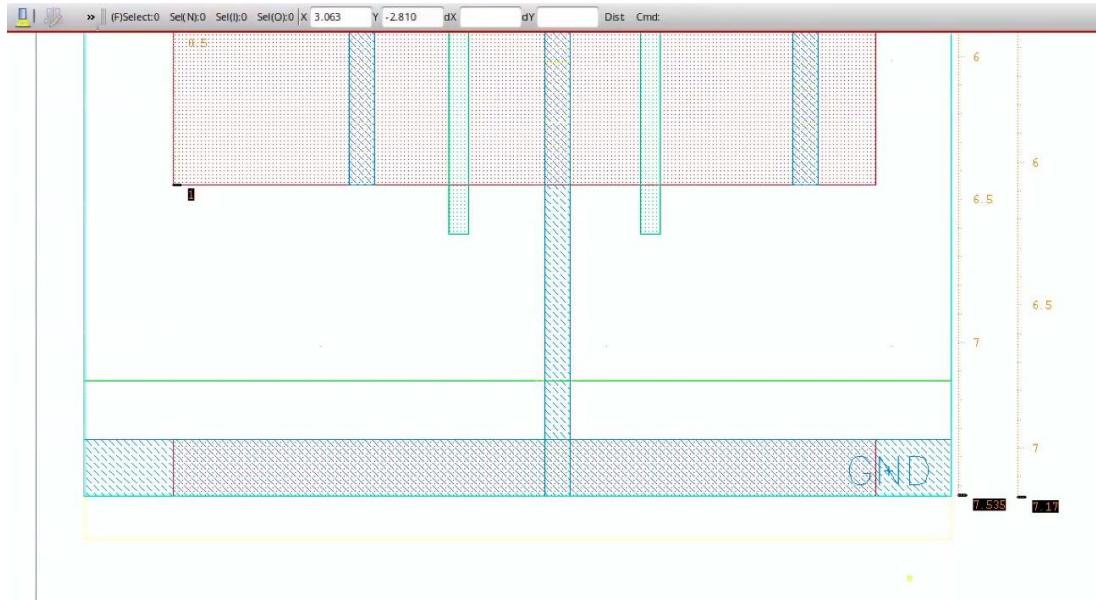


## NOR2 LAYOUT:

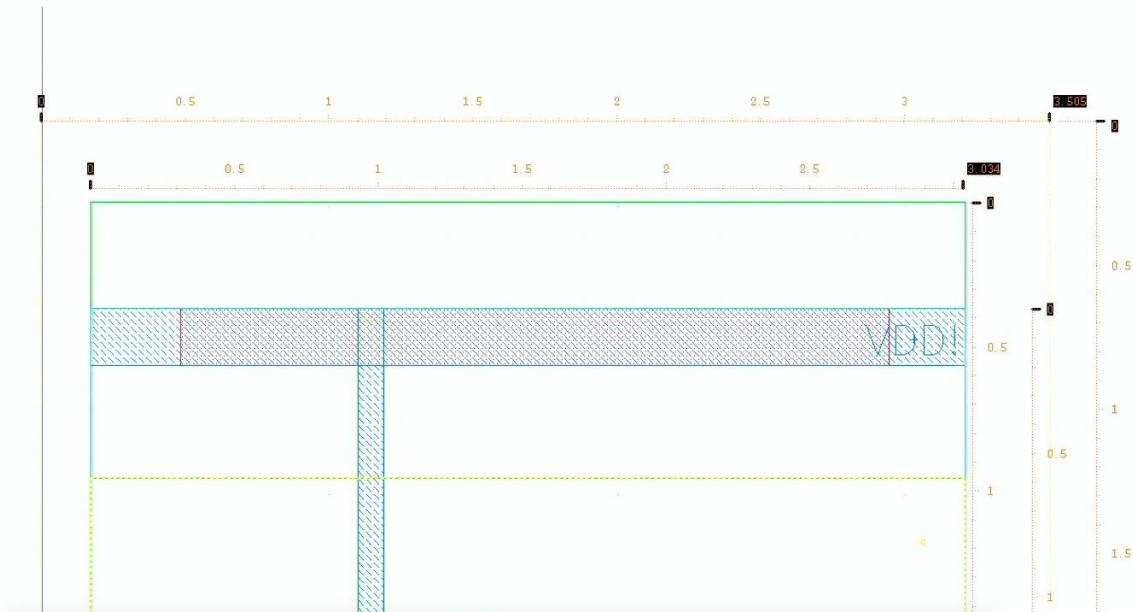


**Dimensions of cell**

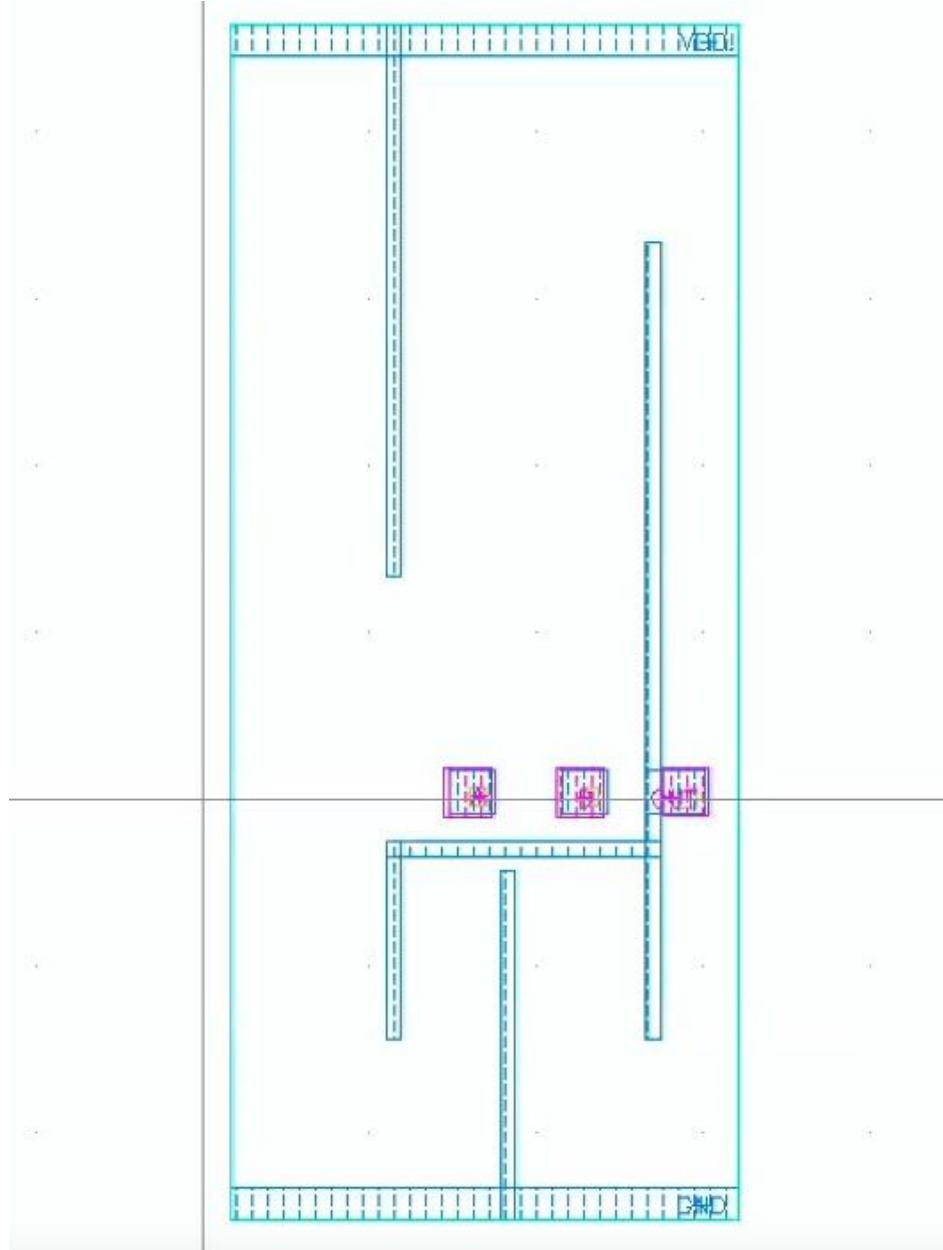
- Height of the cell: 7.535 um



- Width of the cell: 3.034um



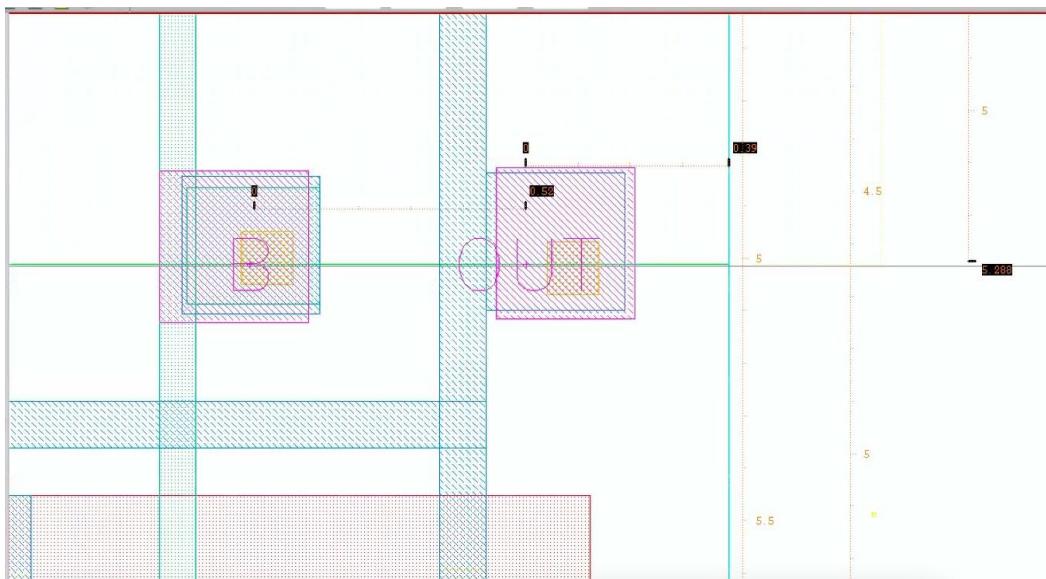
## NOR2 ABSTRACT:



**NOR2 PIN PITCH AND OFFSET:**

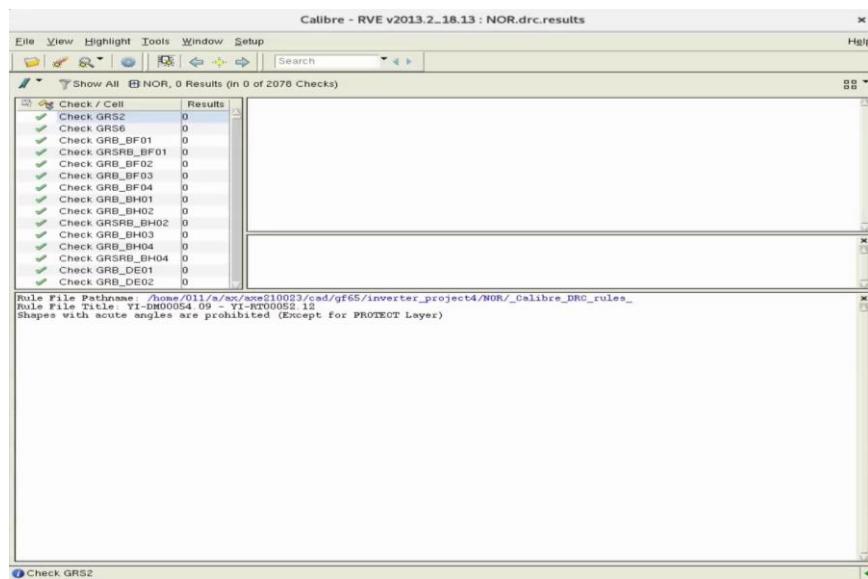
The pin pitch and offset measurement requirements are satisfied:

- Pin pitch= 0.52
- Offset= 0.39



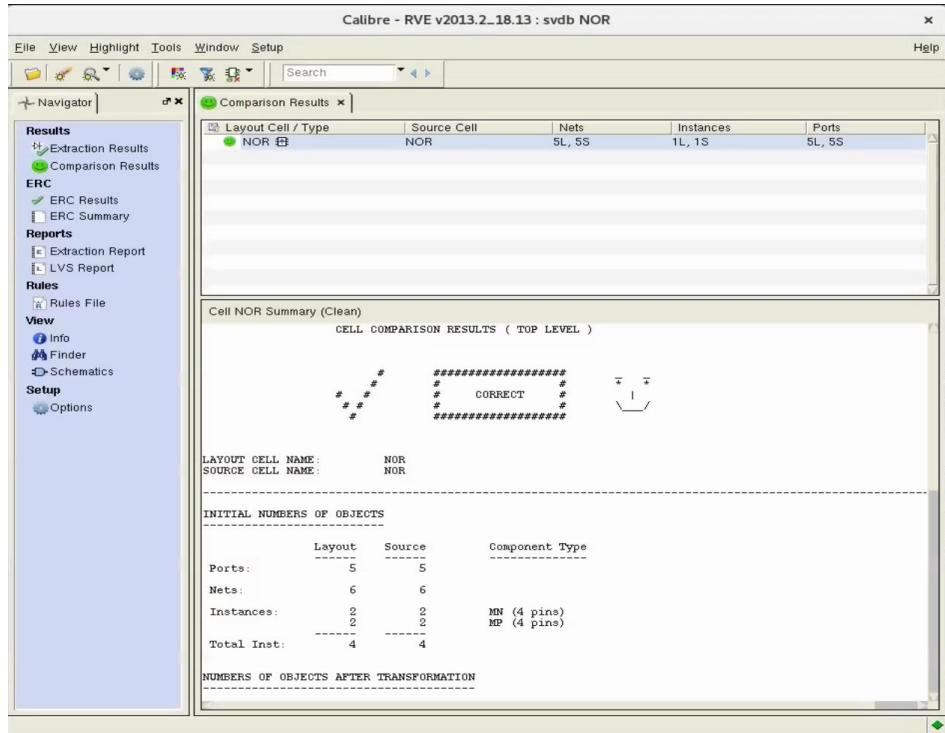
## NOR2 DRC CHECK:

0 DRC errors - Successfully ran the DRC check for NOR2 Layout and there are 0 errors after 2078 Checks.



## NOR2 LVS CHECK:

0 LVS errors - Layout and Schematic of the NOR2 Gate is **CORRECT**



## NOR2 NETLIST:

Calibre Interactive - PEX v2013.2\_18.13

```

File Transcript Setup Help
Rules Inputs Outputs Run Control Transcript Run PEX Start RVE
non-top-level nets = 0
degenerate nets = 1
merged nets = 0
error nets = 0

=====
CALIBRE xRC WARNING / ERROR Summary
=====
xRC Warnings = 0
xRC Errors = 0
=====

--- CALIBRE xRC:: FORMATTER COMPLETED - Thu Oct 20 16:27:37 2022
--- TOTAL CPU TIME = 1 REAL TIME = 2 LVHEAP = 39/81/467 MALLOC = 29

3 Warnings ]
This Linux release is not supported for use with Calibre products.
This Linux release is not supported for use with Calibre products.
This Linux release is not supported for use with Calibre products.

```

PEX Netlist File - NOR.pex.netlist

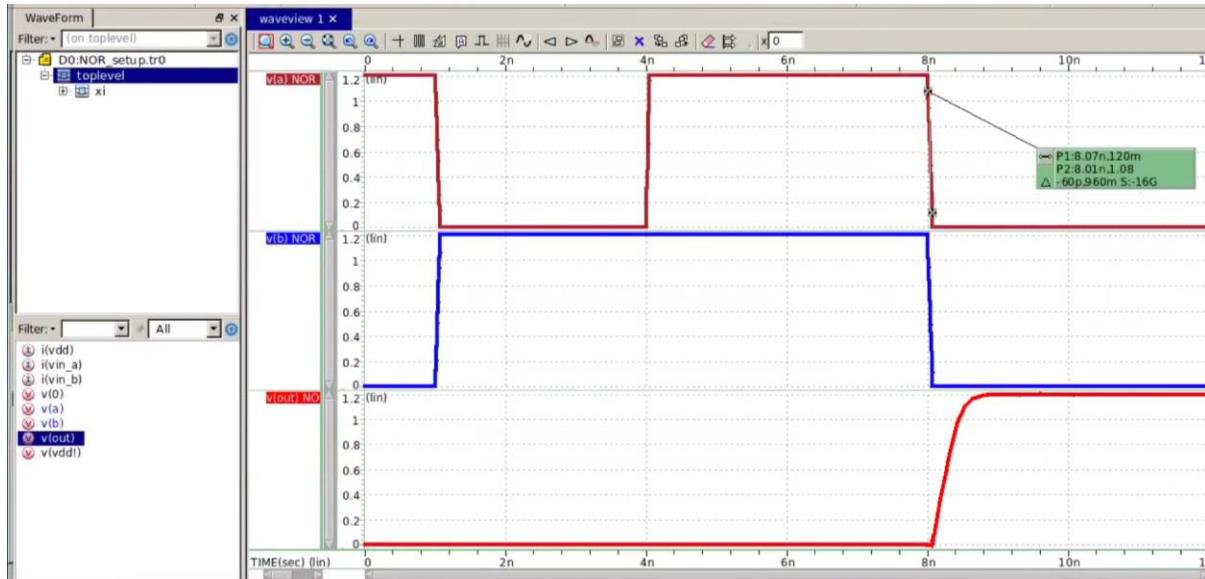
```

File Edit Options Windows
* File: NOR.pex.netlist
* Created: Thu Oct 20 16:27:35 2022
* Program "Calibre xRC"
* Version "v2013.2_18.13"
*
.includef NOR.pex.netlist.pex
.subckt NOR OUT GND! VDD! A B
*
* B B
* A A
* VDD! VDD!
* GND GND
* OUT OUT
D0_noxref N GND! D0_noxref_pos N_VDD! D0_noxref_neg DIODENWX AREA=1.85396e-1:
+ PERIM=1.7592e-05
MM0_N_OUT MM0_N A MM0_N q N GND! MM0_N s N GND! D0_noxref_pos NFET L=7e-08
+ W=1e-06 AD=9.66e-13 AS=3.0le-13 PD=3.932e-06 Ps=1.602e-06 NRd=0.305 NRS=0.31:
+ M=1 NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=9.66e-07 SB=1.426e-06 SD=0
+ PANW1=0 PANW2=0 PANW3=0 PANW4=7e-16 PANV5=3.5e-15 PANW6=7e-15 PANW7=1.4e-14
+ PANW8=1.4e-14 PANW9=2.8e-14 PANV10=2.8e-15
MM0_N_OUT MM0_N d N B MM0_N q N GND! MM0_N s N GND! D0_noxref_pos NFET L=7e-08
+ W=1e-06 AD=7.54e-13 AS=3.0le-13 PD=3.508e-06 Ps=1.602e-06 NRd=0.51 NRS=0.291
+ M=1 NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.638e-06 SB=7.54e-07 SD=0
+ PANW1=0 PANW2=0 PANW3=0 PANW4=7e-16 PANV5=3.5e-15 PANW6=7e-15 PANW7=1.4e-14
+ PANW8=1.4e-14 PANW9=2.8e-14 PANV10=2.8e-15
MM0_P_NET13 N A MM0_P q N VDD! MM0_P s N VDD! D0_noxref_neg PFET L=7e-08 W=2e-06
+ AD=6.02e-13 AS=1.932e-12 PD=2.602e-06 PS=5.932e-06 NRd=0.1505 NRS=0.1525 M=1
+ NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=9.66e-07 SB=1.426e-06 SD=0
+ PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0 PANW7=0 PANW8=0 PANW9=4.48e-06

```

## NOR2 SIMULATION:

The waveform is generated using the NOR2 netlist and the input slew rate is 60 ps and a 70 fF load capacitance is given to the netlist when simulating.



### NOR2 TRUTH TABLE:

<b>Input A</b>	<b>Input B</b>	<b>Output</b>
0	0	1
0	1	0
1	0	0
1	1	0

### XOR2

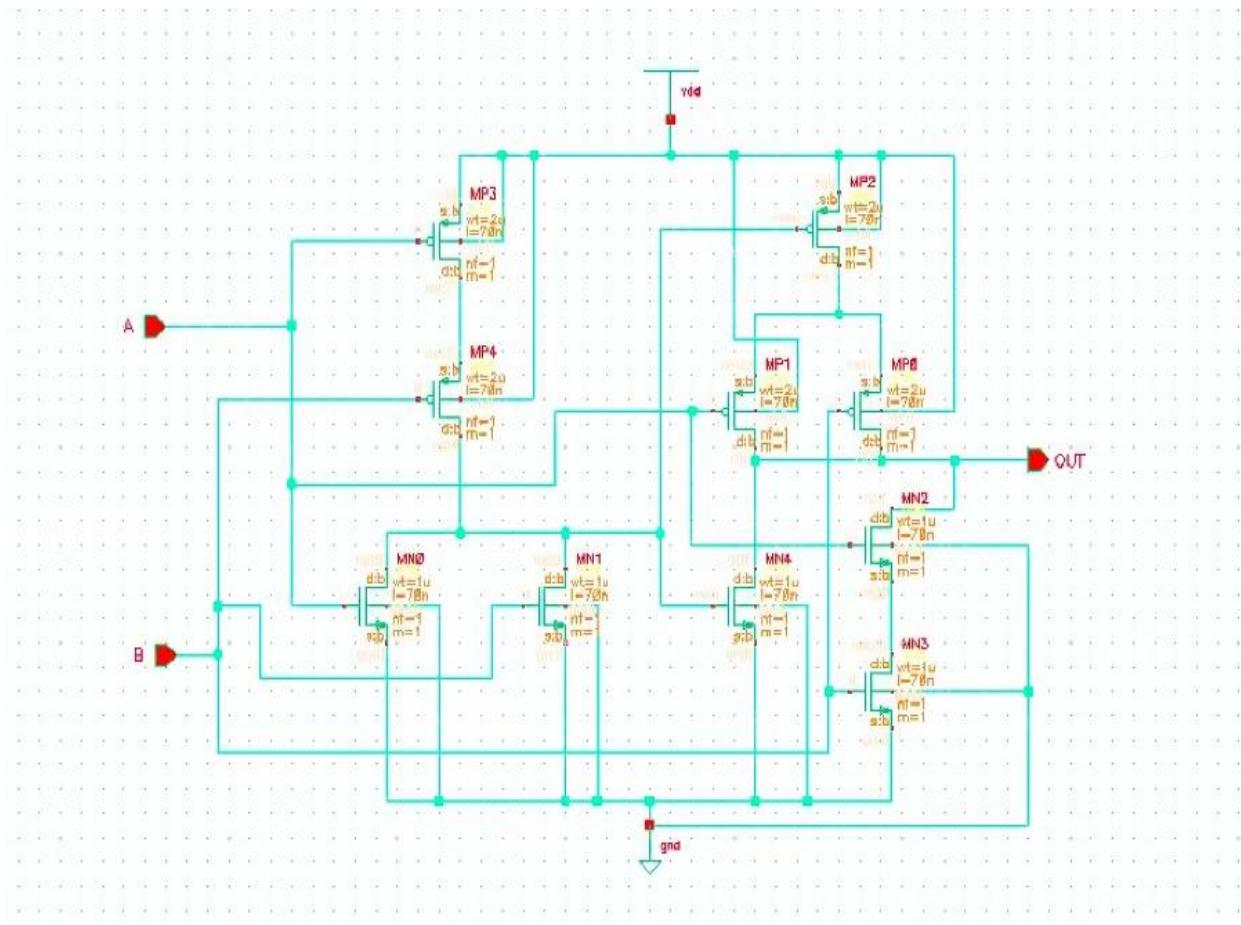
## XOR2 SCHEMATIC

### P-MOS

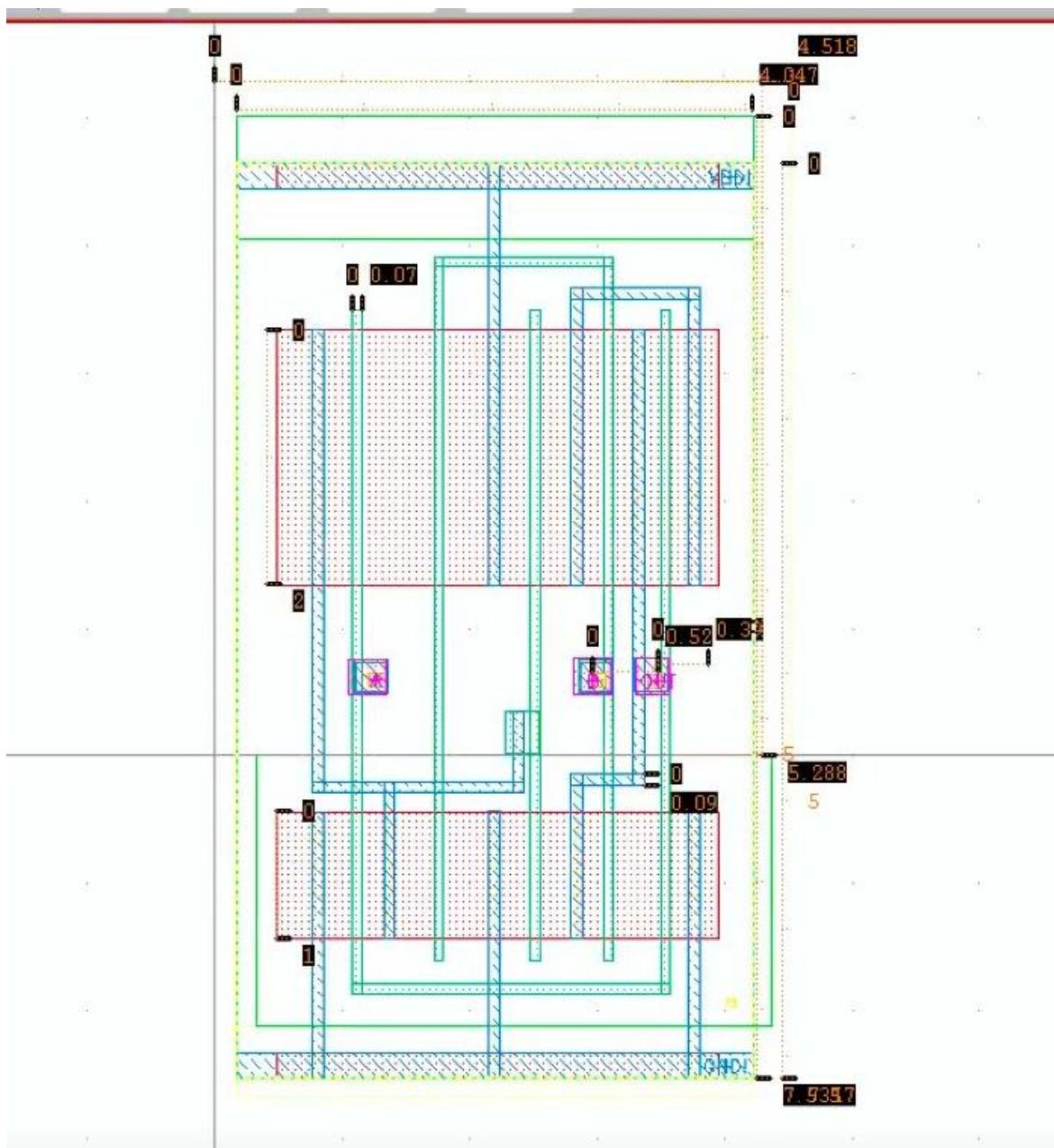
- Width of a single finger and all finger - 2um
- Length of the channel - 70um

### N-MOS

- Width of a single finger and all finger - 1um
- Length of the channel - 70um

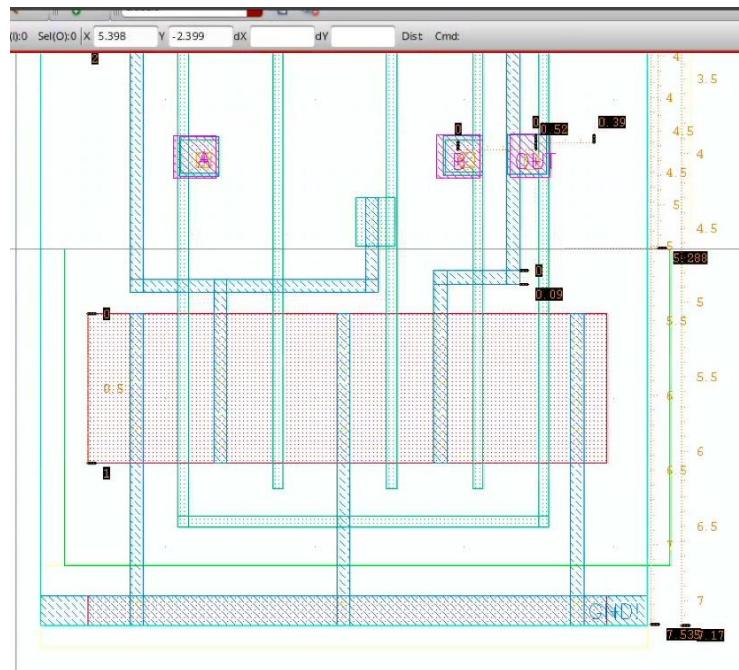


## XOR2 LAYOUT

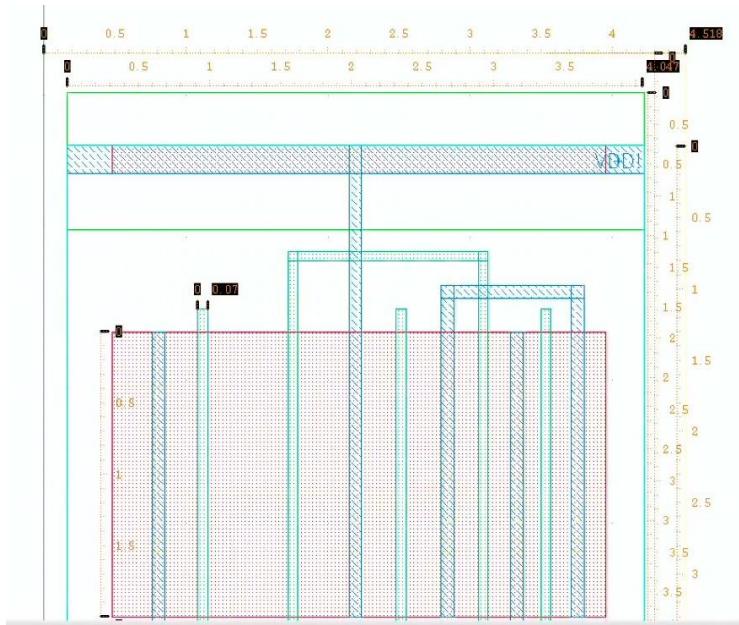


**Dimensions of cell**

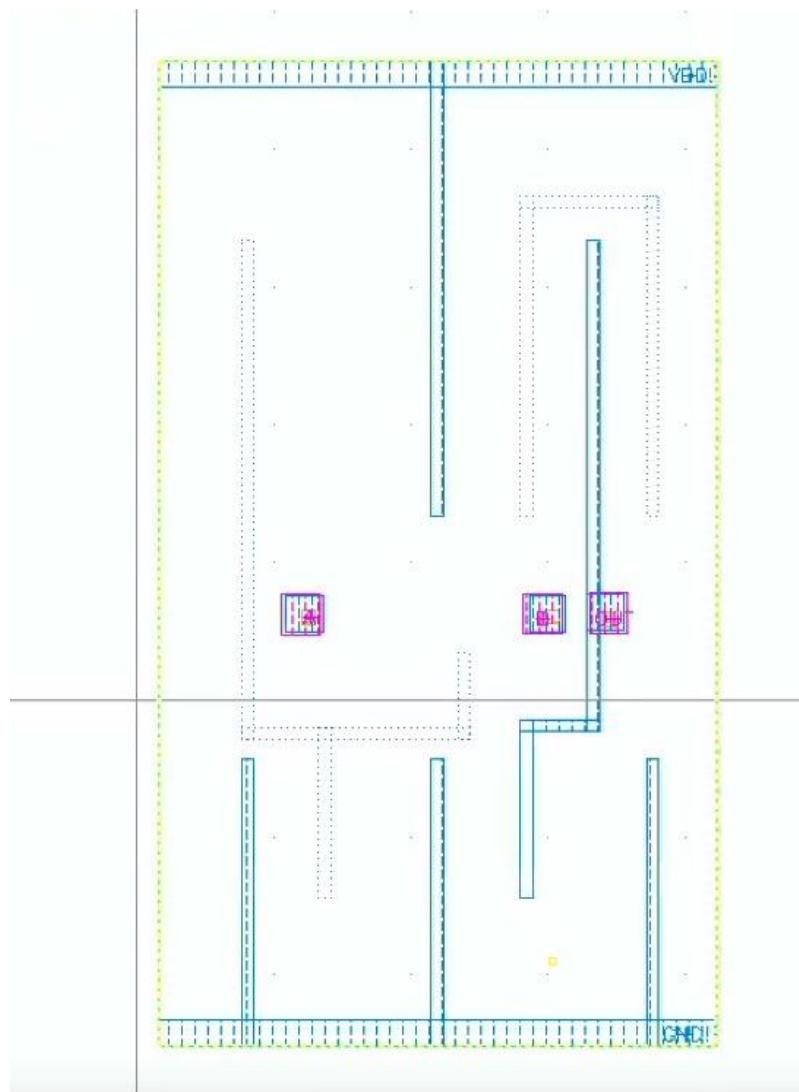
- Height of the cell: 7.535 um



- Width of the cell: 4.047 um



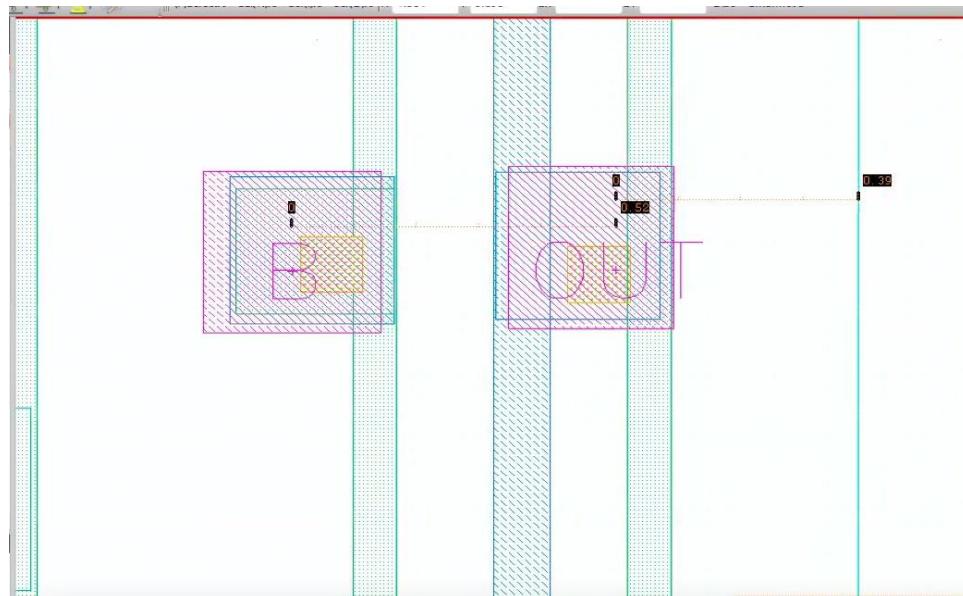
## XOR2 ABSTRACT



## XOR2 PIN PITCH AND OFFSET

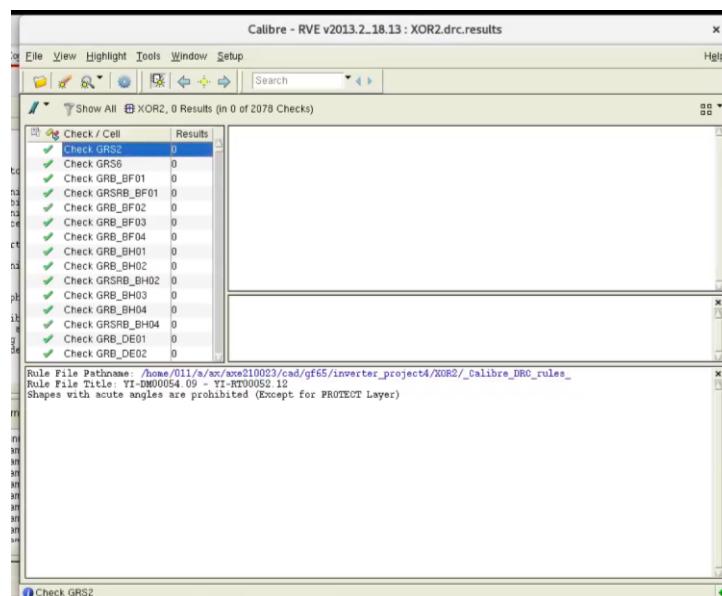
The pin pitch and offset measurement requirements are satisfied:

- Pin pitch= 0.52
- Offset= 0.39



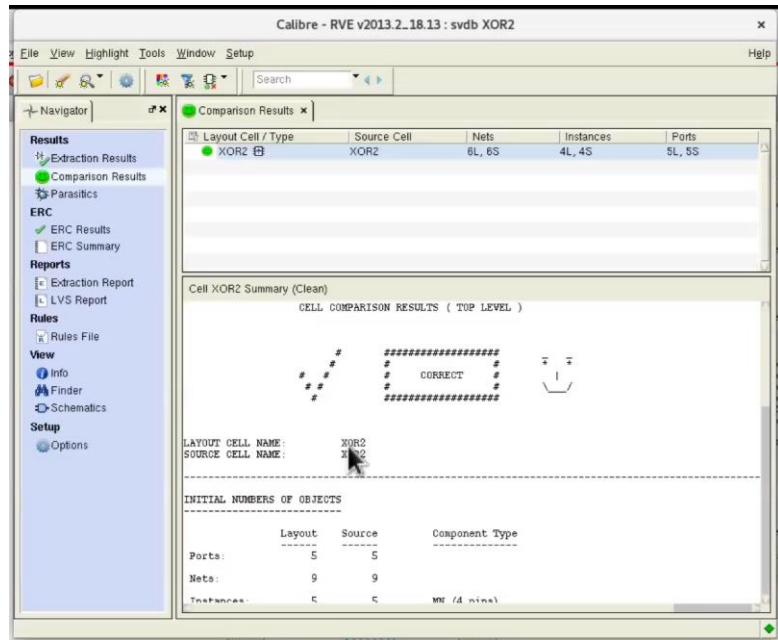
### XOR2 DRC CHECK :

0 DRC errors - Successfully ran the DRC check for XOR2 Layout and there are 0 errors after 2078 Checks.



### XOR2 LVS CHECK

0 LVS errors - Layout and Schematic of the XOR2 Gate is **CORRECT**



## XOR2 NETLIST

Calibre Interactive - PEX v2013.2\_18.13

```

File Transcript Setup
Rules Inputs Outputs Run Control Transcript Run PEX Start RVE

non-top-level nets = 0
degenerate nets = 1
merged nets = 0
error nets = 0
=====
CALIBRE xRC WARNING / ERROR Summary
=====
xRC Warnings = 0
xRC Errors = 0
=====

--- CALIBRE xRC::FORMATTER COMPLETED - Mon Oct 24 22:24:46 2022
--- TOTAL CPU TIME = 1 REAL TIME = 2 LVHEAP = 39/31/467 MALLOC = 29

```

3 Warnings ]

This Linux release is not supported for use with Calibre products.  
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This Linux release is not supported for use with Calibre products.

PEX Netlist File - XOR2.pex.netlist

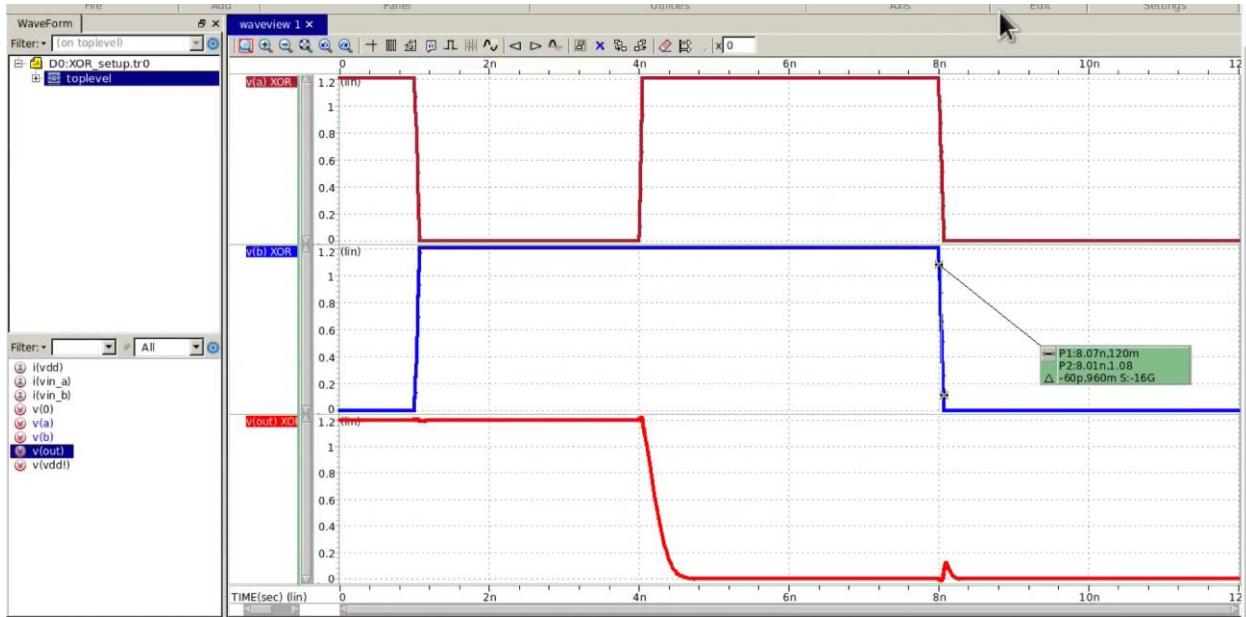
```

File Edit Options Windows
* File: XOR2.pex.netlist
* Created: Mon Oct 24 22:24:44 2022
* Program: "Calibre xRC"
* Version: "v2013.2_18.13"
*
include "XOR2.pex.netlist.pex"
subckt XOR2 GND! OUT VDD! A B
*
* B B
* A A
* VDD! VDD!
* OUT OUT
* GND GND!
XOR2 noxref N GND! D0_noxref_pos N_VDD! D0_noxref_neg DIODENWK AREA=2.39024e-11
* PERIM=1.9610e-05
MM001 N NET3 MM001 d N A MM001 g N GND! MM001_s N GND! D0_noxref_pos NFET L=7e-08
* W=1e-06 AD=2.925e-13 As=6.02e-12 PD=1.565e-06 PS=3.204e-06 NRD=0.215 NRS=0.27
* M=1 NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=6.02e-07 SB=2.803e-06 SD=0
* PANW1=0 PANW2=0 PANW3=0 PANW4=7e-16 PANW5=3.5e-15 PANW6=7e-15 PANW7=1.4e-14
* PANW8=1.4e-14 PANW9=2.8e-14 PANW10=2.8e-15
MM001 N NET3 MM001 d N B MM011 g N GND! MM011_s N GND! D0_noxref_pos NFET L=7e-08
* W=1e-06 AD=2.825e-13 As=3.46e-13 PD=1.555e-06 PS=1.692e-06 NRD=0.35 NRS=0.404
* M=1 NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.237e-06 SB=2.168e-06 SD=0
* PANW1=0 PANW2=0 PANW3=0 PANW4=7e-16 PANW5=3.5e-15 PANW6=7e-15 PANW7=1.4e-14
* PANW8=1.4e-14 PANW9=2.8e-14 PANW10=2.8e-15
MM004 N OUT MM04 d N NET28 MM04_g N GND! MM04_s N GND! D0_noxref_pos NFET L=7e-0
* W=1e-06 AD=2.535e-13 As=3.46e-13 PD=1.507e-06 PS=1.692e-06 NRD=0.292 NRS=0.28
* M=1 NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.999e-06 SB=1.406e-06 SD=0
* PANW1=0 PANW2=0 PANW3=0 PANW4=7e-16 PANW5=3.5e-15 PANW6=7e-15 PANW7=1.4e-14
* PANW8=1.4e-14 PANW9=2.8e-14 PANW10=2.8e-15
MM003 N OUT MM04 d N B MM03_g NET28 N GND! D0_noxref_pos NFET L=7e-08 W=1e-06
* AD=2.535e-13 As=1.855e-13 PD=1.507e-06 PS=1.371e-06 NRD=0.215 NRS=0.1855 M=1
* NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=2.576e-06 SE=8.29e-07 SD=0
* PANW1=0 PANW2=0 PANW3=0 PANW4=7e-16 PANW5=3.5e-15 PANW6=7e-15 PANW7=1.4e-14

```

## XOR2 SIMULATION

The waveform is generated using the XOR2 netlist and the input slew rate is 60 ps and a 70 fF load capacitance is given to the netlist when simulating.



### XOR2 TRUTH TABLE-

Input A	Input B	Output
0	0	0
0	1	1
1	0	1
1	1	0

### MUX 2:1

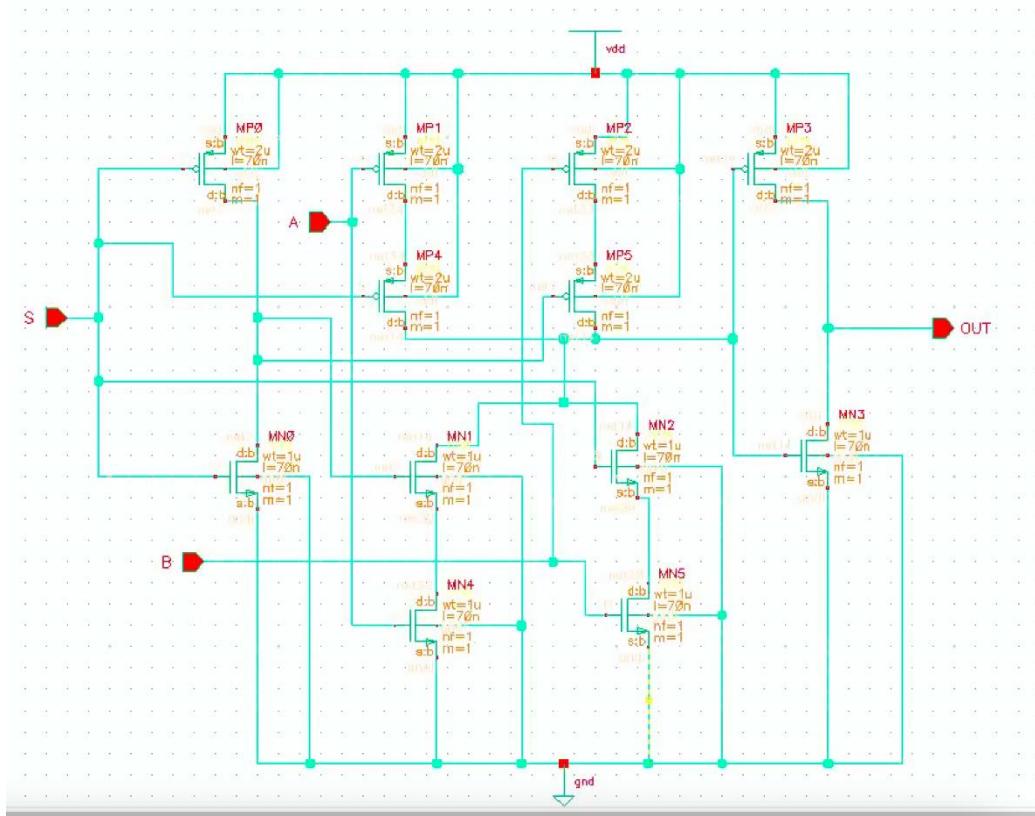
## MUX2:1 SCHEMATIC :

### P-MOS

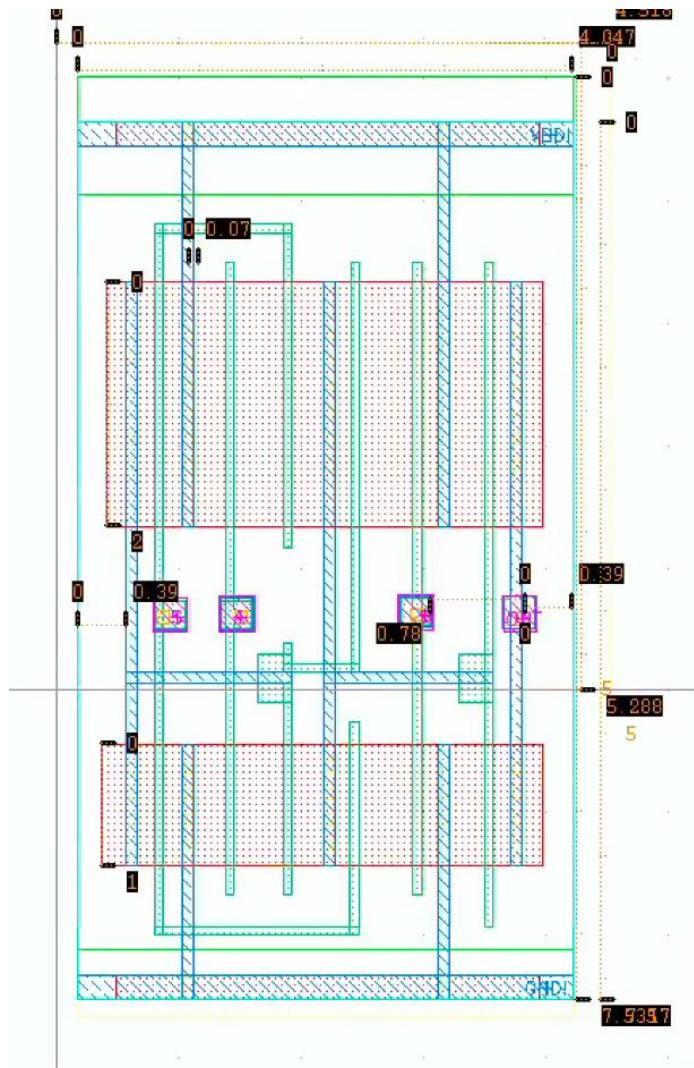
- Width of a single finger and all finger - 2um
- Length of the channel - 70um

### N-MOS

- Width of a single finger and all finger - 1um
- Length of the channel - 70um

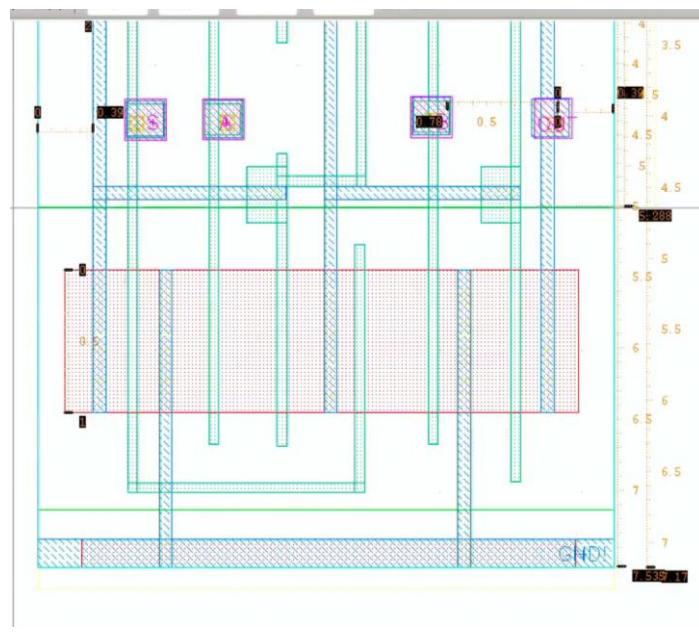


## MUX 2:1 LAYOUT:

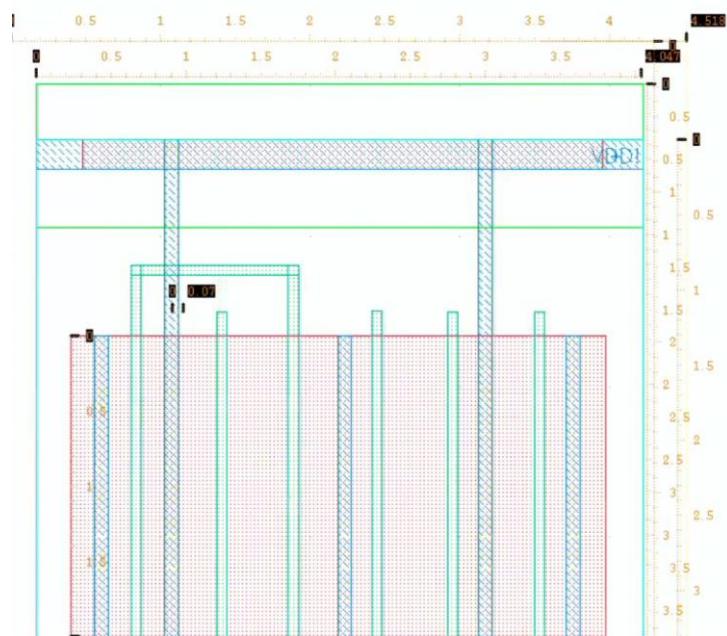


## Dimensions of cell

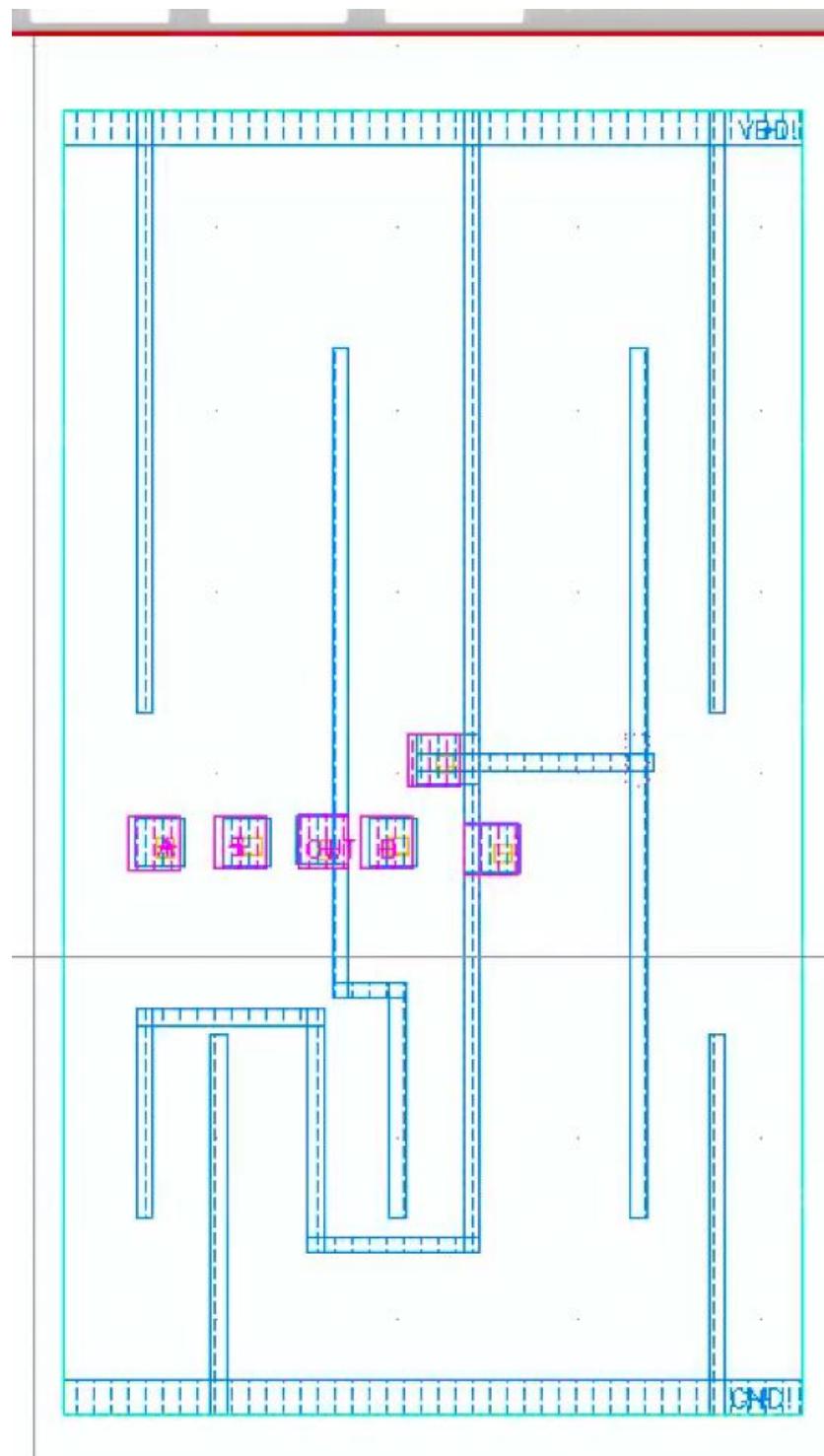
- Height of the cell= 7.535um



- Width of the cell = 4.047μm



## MUX2:1 ABSTRACT :

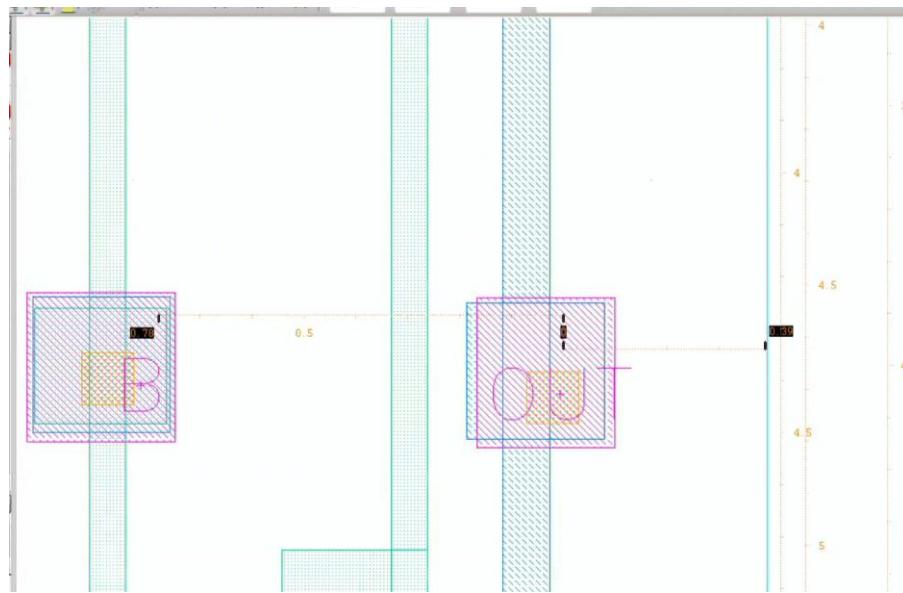


### **MUX2:1 PIN PITCH AND OFFSET:**

The pin pitch and offset measurement requirements are satisfied:

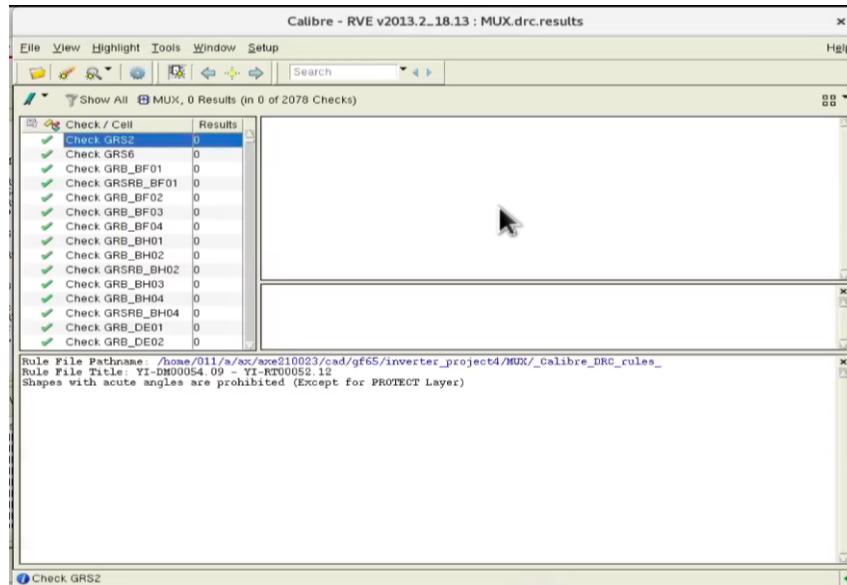
- Pin pitch= 0.78

- Offset= 0.39



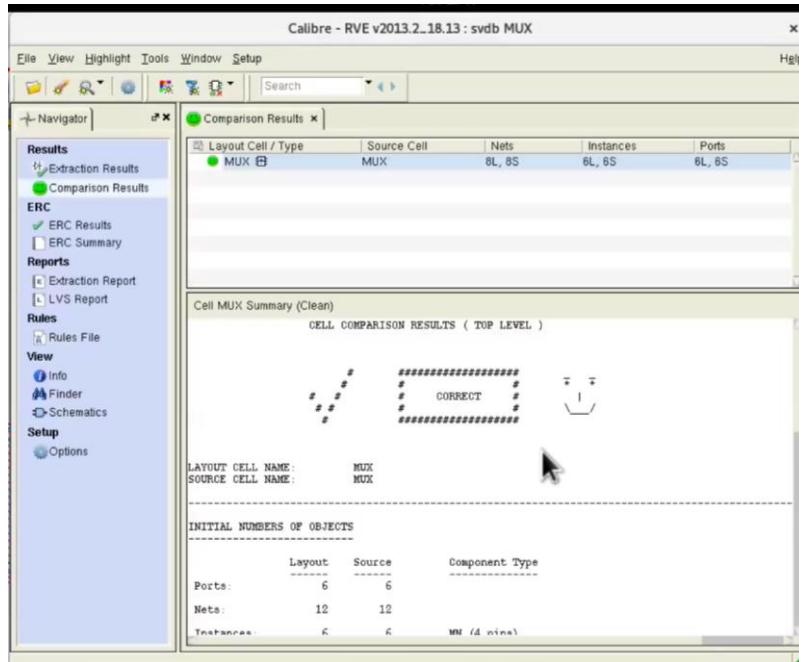
## MUX2:1 DRC CHECK:

0 DRC errors - Successfully ran the DRC check for MUX 2:1 Layout and the is 0 errors after 2078 Checks.



## MUX2:1 LVS CHECK:

0 LVS errors - Layout and Schematic of the MUX 2:1 Gate is **CORRECT**



## MUX2:1 NETLIST :

Calibre Interactive - PEX v2013.2\_18.13

```

File Transcript Setup
Rules Inputs Outputs Run Control Transcript Run PEX Start RVE
non-top-level nets = 0
degenerated nets = 2
merged nets = 0
error nets = 0
=====
CALIBRE xRC WARNING / ERROR Summary
xRC Warnings = 0
xRC Errors = 0
=====

--- CALIBRE xRC::FORMATTER COMPLETED - Tue Oct 25 13:10:16 2022
--- TOTAL CPU TIME = 1 REAL TIME = 2 LVHEAP = 39/81/467 MALLOC = 29
3 Warnings ]
This Linux release is not supported for use with Calibre products.
This Linux release is not supported for use with Calibre products.
This Linux release is not supported for use with Calibre products.

```

PEX Netlist File - MUX.pex.netlist

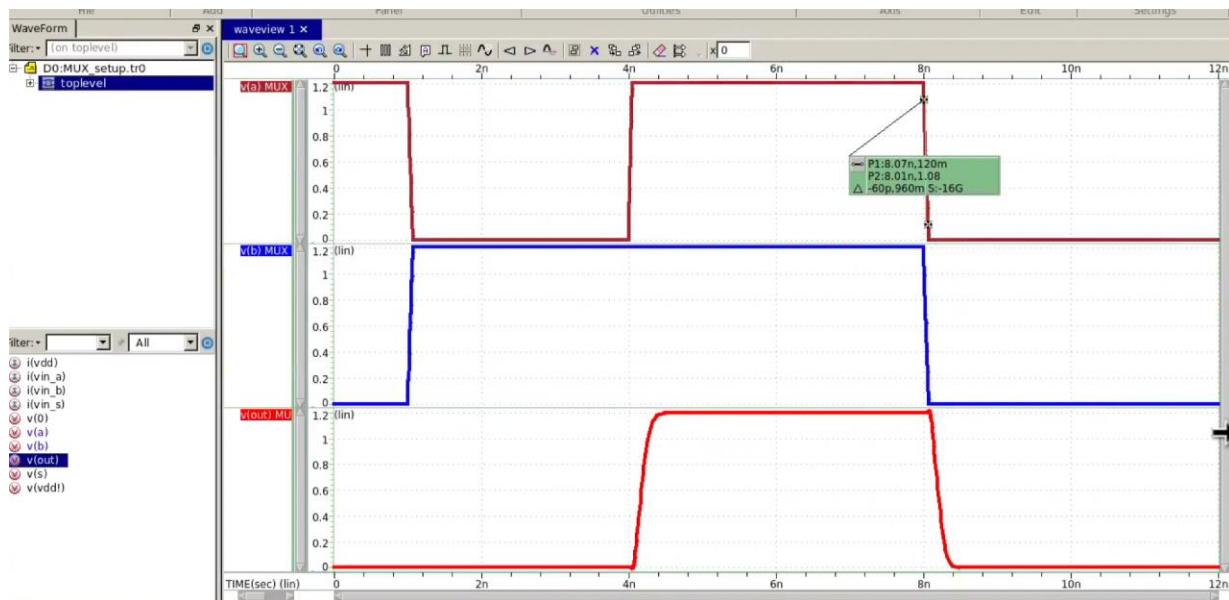
```

File Edit Options Windows
+ File: MUX.pex.netlist
+ Created: Tue Oct 25 13:10:14 2022
+ Program "Calibre xRC"
+ Version "v2013.2_18.13"
+
include "MUX.pex.netlist.pex"
subckt MUX GND! OUT VDD! S A B
+ B B
+ A A
+ S S
+ VDD! VDD!
+ OUT OUT
+ GND! GND!
XDO_noxref N GND! D0_noxref_pos N_VDD! D0_noxref_neg DIODENWX AREA=2.39024e-11
+ PERIM=1.9618e-05
MMNO N NET1 MMNO_d N_S_MMNO_s N_GND! MMNO_o N_GND! D0_noxref_pos NFET L=7e-08
+ W=1e-06 AD=4.41e-13 AS=2.52e-13 PD=1.802e-06 PS=1.904e-06 NRd=0.195 NRs=0.195
+ M=1 NF=1 CNR SWITCH=0 PCGRIT=0 PAR=1 PTWELL=0 SA=1.41e-07 SB=3.1e-06 SD=0
PANW1=0 PANW2=0 PANW3=0 PANW4=7e-15 PANW5=3.5e-15 PANW6=7e-15 PANW7=1.4e-14
+ PANW8=1.4e-14 PANW9=2.8e-14 PANW10=2.8e-15
XDM04 NET32 N_A_MM04_g N_GND! MM010_s N_GND! D0_noxref_pos NFET L=7e-08 W=1e-06
+ AD=2.03e-13 AS=2.52e-13 PD=1.406e-06 PS=1.504e-06 NRd=0.203 NRs=0.203 M=1 NF=1
+ CNR SWITCH=0 PCGRIT=0 PAR=1 PTWELL=0 SA=1.015e-06 SB=2.526e-06 SD=0 PANW1=0
PANW2=0 PANW3=0 PANW4=7e-15 PANW5=3.5e-15 PANW6=7e-15 PANW7=1.4e-14
+ PANW8=1.4e-14 PANW9=2.8e-14 PANW10=2.8e-15
XDM01_N NET14_MMN1_d N NET1 MMN1_g NET32_N_GND! D0_noxref_pos NFET L=7e-08
+ W=1e-06 AD=2.385e-13 AS=2.03e-13 PD=1.477e-06 PS=1.406e-06 NRd=0.308 NRs=0.203
+ M=1 NF=1 CNR SWITCH=0 PCGRIT=0 PAR=1 PTWELL=0 SA=1.491e-06 SB=2.05e-06 SD=0
+ PANW1=0 PANW2=0 PANW3=0 PANW4=7e-15 PANW5=3.5e-15 PANW6=7e-15 PANW7=1.4e-14
+ PANW8=1.4e-14 PANW9=2.8e-14 PANW10=2.8e-15
XDM02_N NET14_MMN2_d N_S_MM02_g NET30_N_GND! D0_noxref_pos NFET L=7e-08 W=1e-06
+ AD=2.385e-13 AS=2.03e-13 PD=1.477e-06 PS=1.448e-06 NRd=0.169 NRs=0.224 M=1
+ NF=1 CNR SWITCH=0 PCGRIT=0 PAR=1 PTWELL=0 SA=1.038e-06 SB=2.05e-06 SD=0 PANW1=0
PANW2=0 PANW3=0 PANW4=7e-15 PANW5=3.5e-15 PANW6=7e-15 PANW7=1.4e-14
+ PANW8=1.4e-14 PANW9=2.8e-14 PANW10=2.8e-15

```

## MUX2:1 SIMULATION :

The waveform is generated using the MUX 2:1 netlist and the input slew rate is 60 ps and a 70 fF load capacitance is given to the netlist when simulating.



### MUX2:1 TRUTH TABLE :

<b>Input A</b>	<b>Input B</b>	<b>Select</b>	<b>Output</b>
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1

**AOI21**

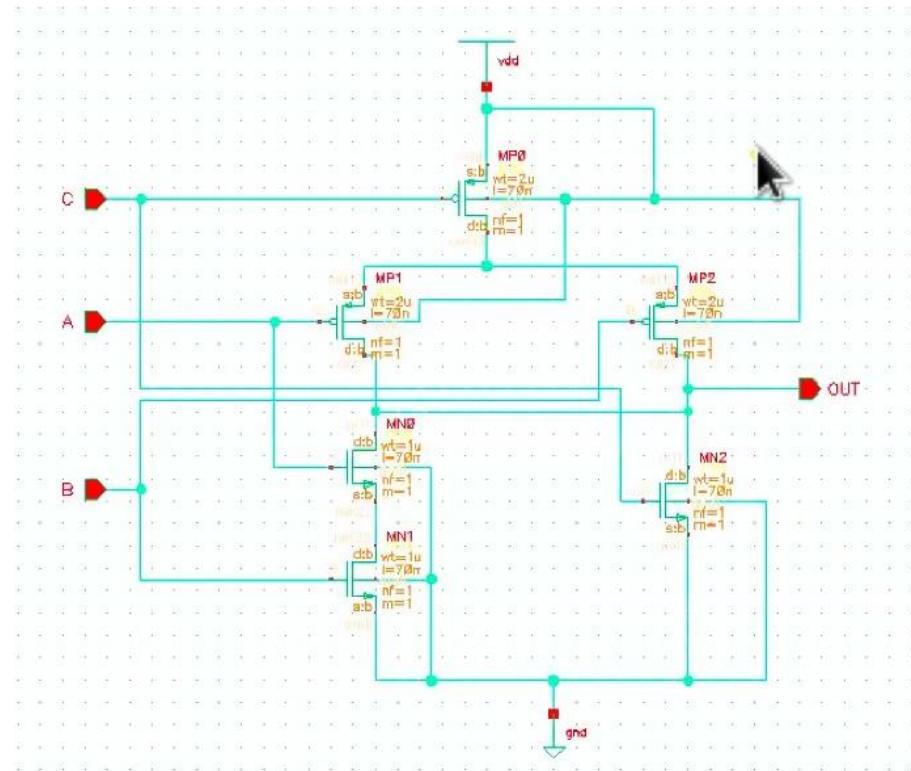
### AOI21 SCHEMATIC :

## P-MOS

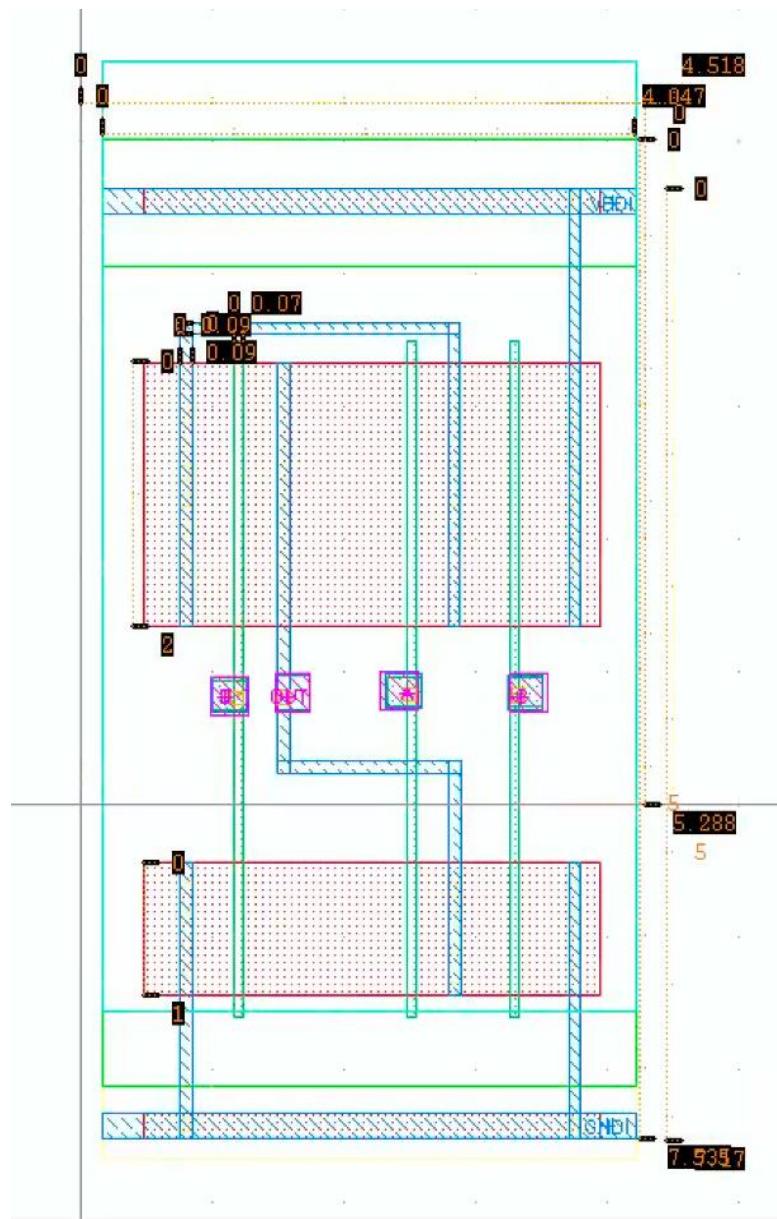
- Width of a single finger and all finger - 2um
- Length of the channel - 70um

## N-MOS

- Width of a single finger and all finger - 1um
- Length of the channel - 70um

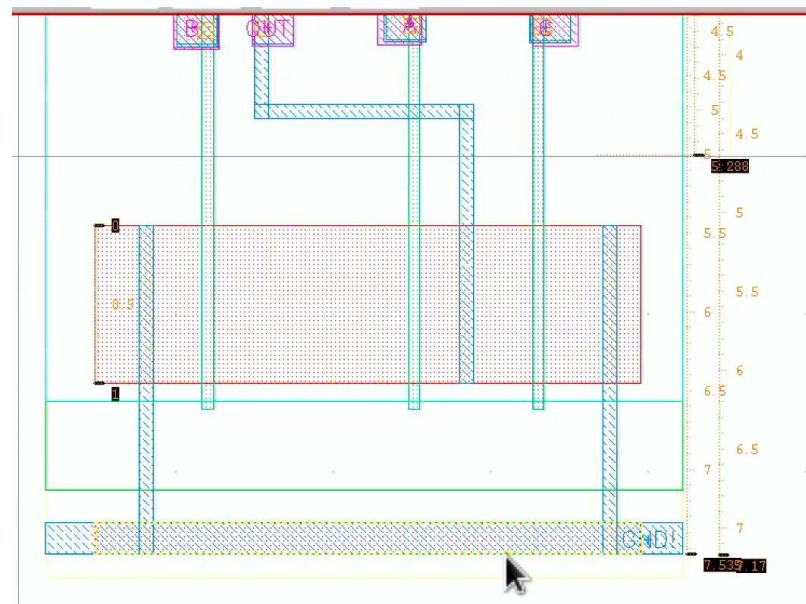


## AOI21 LAYOUT:

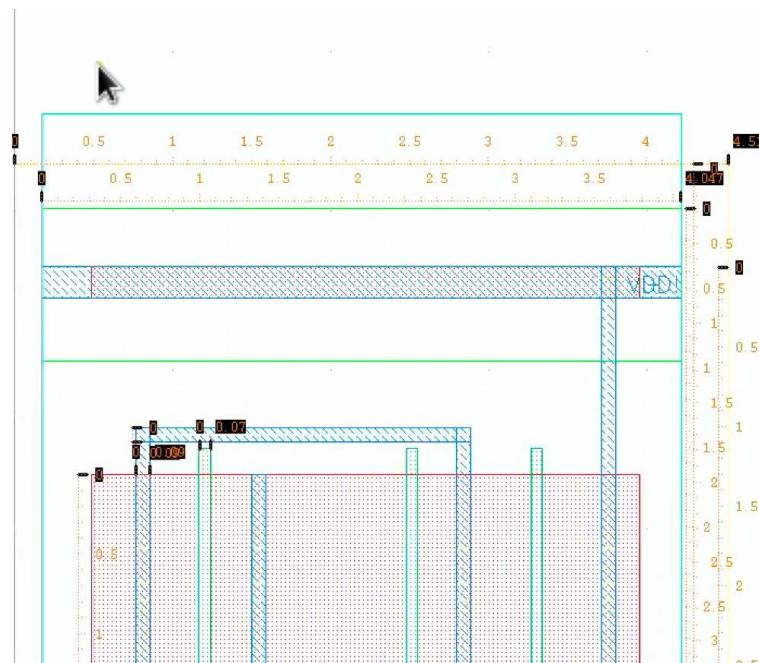


**Dimensions of cell**

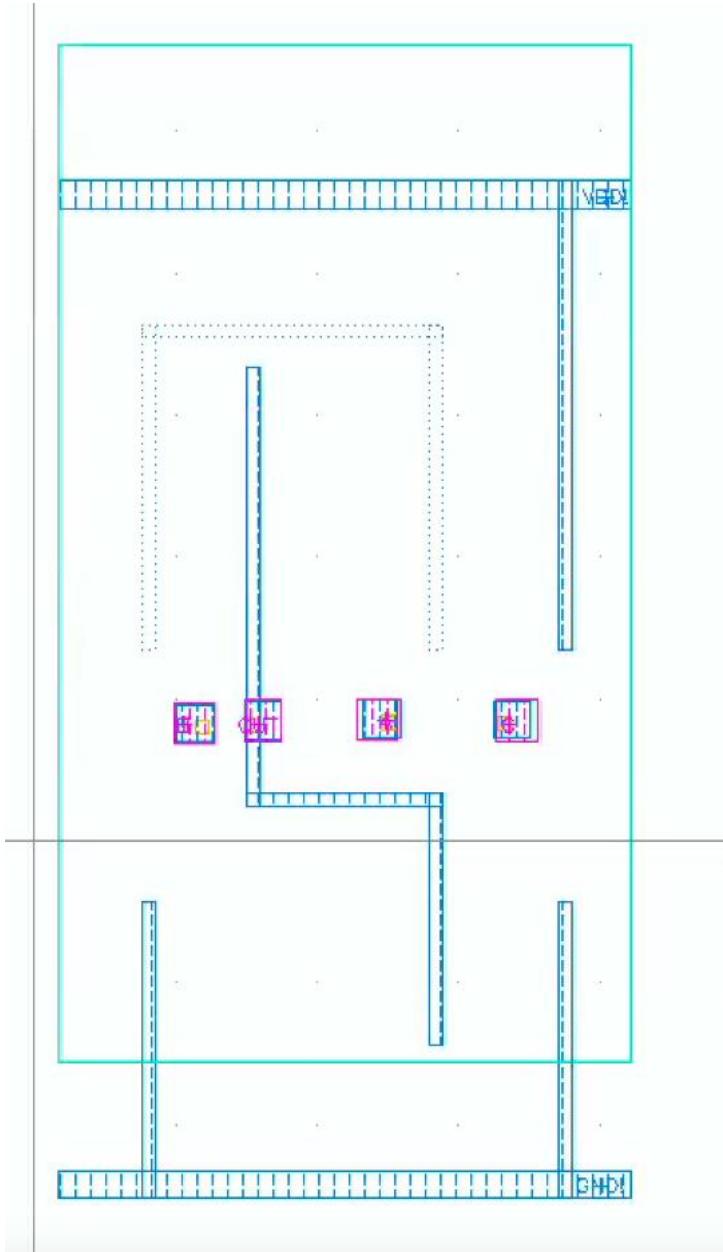
- Height of the cell= 7.535um



- Width of the cell= 4.047um



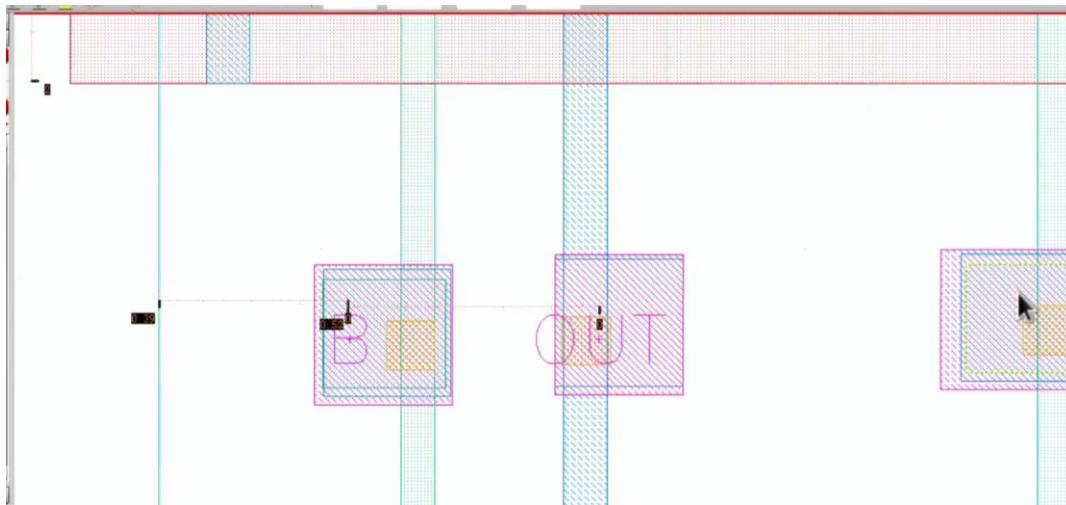
## AOI21 ABSTRACT:



**AOI21 PIN PITCH AND OFFSET:**

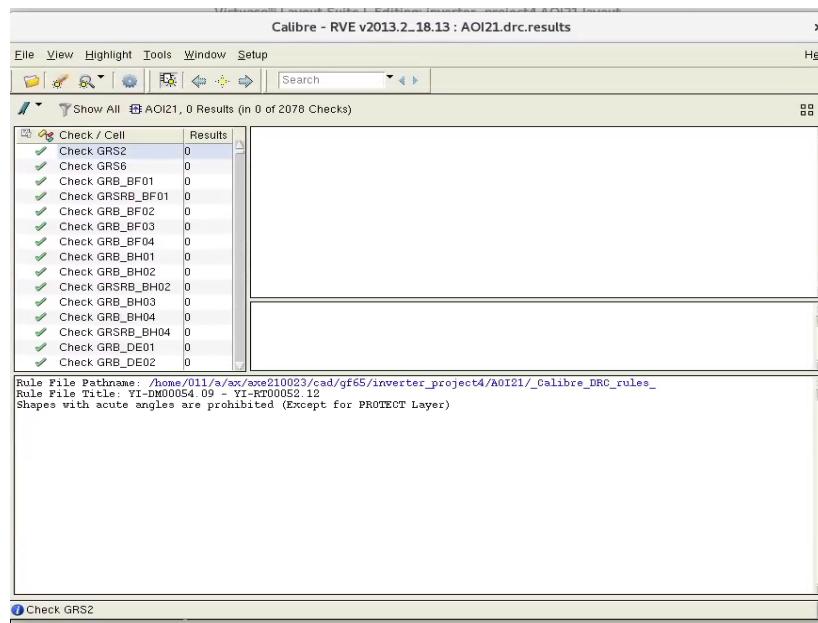
The pin pitch and offset measurement requirements are satisfied:

- Pin pitch= 0.52
- Offset= 0.39



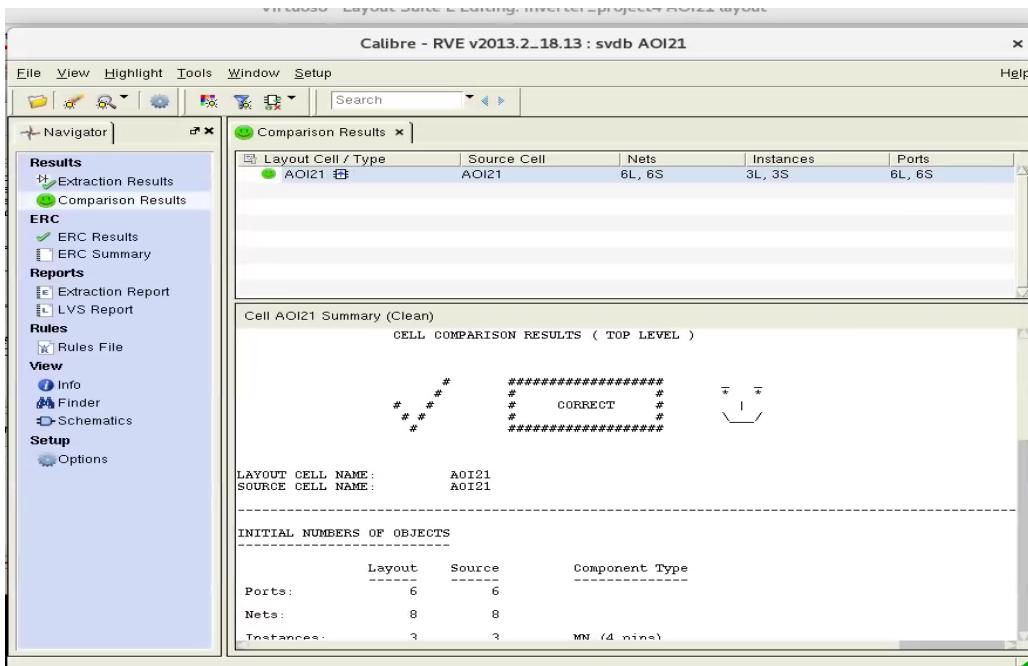
### AOI21 DRC CHECK:

0 DRC errors - Successfully ran the DRC check for AOI21 Layout and the is 0 errors after 2078 Checks.



### AOI21 LVS CHECK:

0 LVS errors - Layout and Schematic of the AOI21 Gate is **CORRECT**



## AOI21 NETLIST:

```

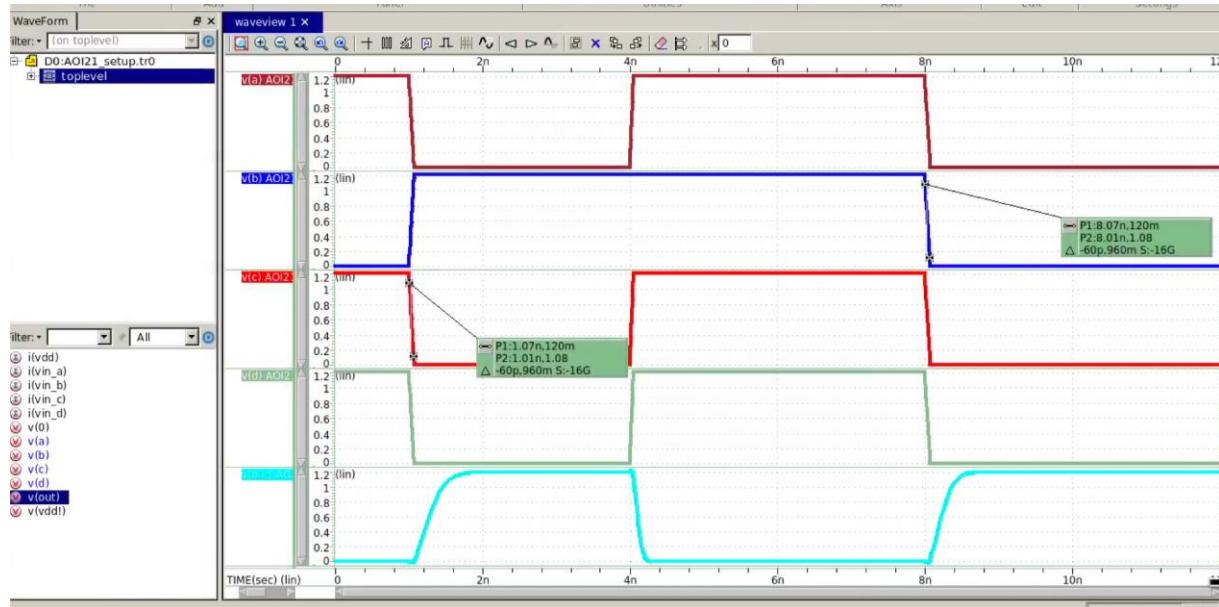
Calibre Interactive - PEX v2013.2_18.13
File Transcript Setup Help
Rules Inputs Outputs Run Control Transcript Run PEX Start RVE
non-top-level nets = 0
degenerate nets = 1
merged nets = 0
error nets = 0
----- CALIBRE XRC WARNING / ERROR Summary -----
XRC Warnings = 0
XRC Errors = 0
----- --- CALIBRE XRC::FORMATTER COMPLETED - Mon Oct 24 22:59:18 2022
--- TOTAL CPU TIME = 1 REAL TIME = 2 LVHEAP = 39/81/467 MALLOC = 29
----- This Linux release is not supported for use with Calibre products.
----- This Linux release is not supported for use with Calibre products.
----- This Linux release is not supported for use with Calibre products.

PEX Netlist File - AOI21.pex.netlist
File Edit Options Windows Help
Program "Calibre xRC"
Version "v2013.2_18.13"
include "AOI21.pex.netlist.pex"
subckt AOI21 GND! OUT VDD! B A C
*
* C C
* A A
* B B
* VDD! VDD!
* OUT OUT
* GND! GND!
D0 noxref N GND! D0_noxref_pos N_VDD! D0_noxref_neg DIODENWK AREA=2.39024e-11
PERIM=1.9518e-05
M0N0 N OUT MN01 N GND! MN01 s N GND! D0_noxref_pos NFET L=7e-08 W=1e-06
* AD=6.225e-13 AS=6 Bd=13 PD=2 245e-05 PS=3 369e-06 NRD=0.6225 NRS=0.358 M=1
* NP=1 CNR SWITCH=0 PCGRIT=0 PAR=1 PTWELL=0 Sa=6 84e-07 SB=2 721e-06 SD=0
* PANW1=0 PANW2=0 PANW3=0 PANW4=7e-16 PANW5=3 5e-15 PANW6=7e-15 PANW7=1 4e-14
* PANW8=1 4e-14 PANW9=2 8e-14 PANW10=2 8e-15
D0G0 N OUT MN00 d N A MN00 g NET22 N GND! D0_noxref_pos NFET L=7e-08 W=1e-06
AD=3.595e-13 AS=6 Bd=13 PD=2 715e-06 PS=3 245e-05 NRD=0.294 NRS=0.6225 M=1
NP=1 CNR SWITCH=0 PCGRIT=0 PAR=1 PTWELL=0 Sa=1 999e-06 SB=1 406e-06 SD=0
PANW1=0 PANW2=0 PANW3=0 PANW4=7e-16 PANW5=3 5e-15 PANW6=7e-15 PANW7=1 4e-14
* PANW8=1 4e-14 PANW9=2 8e-14 PANW10=2 8e-15
MN02 N OUT MN00 d N C MN02 g N GND! MN02 s N GND! D0_noxref_pos NFET L=7e-08
W=1e-06 Ad=3.595e-13 As=6 17e-13 PD=1.719e-06 PS=3.234e-06 NRD=0.425 NRS=0.419
* NC NF=1 CNR SWITCH=0 PCGRIT=0 PAR=1 PTWELL=0 Sa=2.788e-06 SB=6 17e-07 SD=0
* PANW1=0 PANW2=0 PANW3=0 PANW4=7e-16 PANW5=3 5e-15 PANW6=7e-15 PANW7=1 4e-14
* PANW8=1 4e-14 PANW9=2 8e-14 PANW10=2 8e-15
MN02 N OUT MN02 d N D MN02 g N NET13 MN02 s N VDD! D0_noxref_neg PFET L=7e-08
W=2e-06 Ad=1.245e-12 As=1.368e-12 PD=3 245e-06 PS=5.368e-06 NRD=0.1555
* NRS=0.179 M=1 NF=1 CNR SWITCH=0 PCGRIT=0 PAR=1 PTWELL=1 Sa=6 84e-07
* SB=2.721e-06 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0 PANW7=0
* MN03 N MN03 d N A MN03 g MN03 s N GND! D0_noxref_pos NFET L=7e-08
W=1e-06 Ad=3.595e-13 As=6 17e-13 PD=1.719e-06 PS=3.234e-06 NRD=0.425 NRS=0.419
* NC NF=1 CNR SWITCH=0 PCGRIT=0 PAR=1 PTWELL=0 Sa=2.788e-06 SB=6 17e-07 SD=0
* PANW1=0 PANW2=0 PANW3=0 PANW4=7e-16 PANW5=3 5e-15 PANW6=7e-15 PANW7=1 4e-14
* PANW8=1 4e-14 PANW9=2 8e-14 PANW10=2 8e-15
MN02 N OUT MN02 d N D MN02 g N NET13 MN02 s N VDD! D0_noxref_neg PFET L=7e-08
W=2e-06 Ad=1.245e-12 As=1.368e-12 PD=3 245e-06 PS=5.368e-06 NRD=0.1555
* NRS=0.179 M=1 NF=1 CNR SWITCH=0 PCGRIT=0 PAR=1 PTWELL=1 Sa=6 84e-07
* SB=2.721e-06 SD=0 PANW1=0 PANW2=0 PANW3=0 PANW4=0 PANW5=0 PANW6=0 PANW7=0

```

## AOI21 SIMULATION :

The waveform is generated using the AOI21 netlist and the input slew rate is 60 ps and a 70 fF load capacitance is given to the netlist when simulating.



### AOI21 TRUTH TABLE :

<b>Input A</b>	<b>Input B</b>	<b>Input C</b>	<b>Ouput</b>
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

**OAII22**

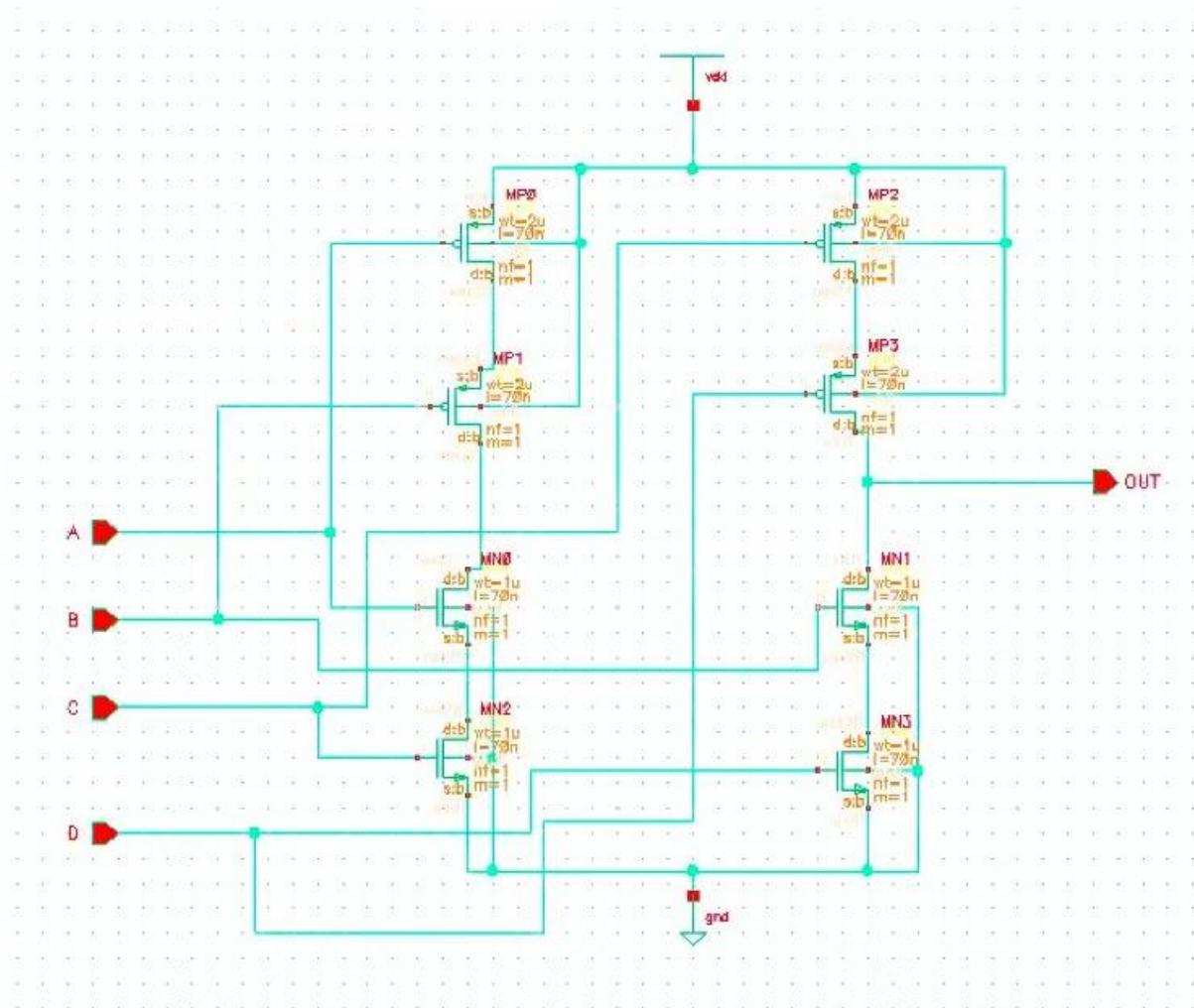
## OAI22 SCHEMATIC:

### P-MOS

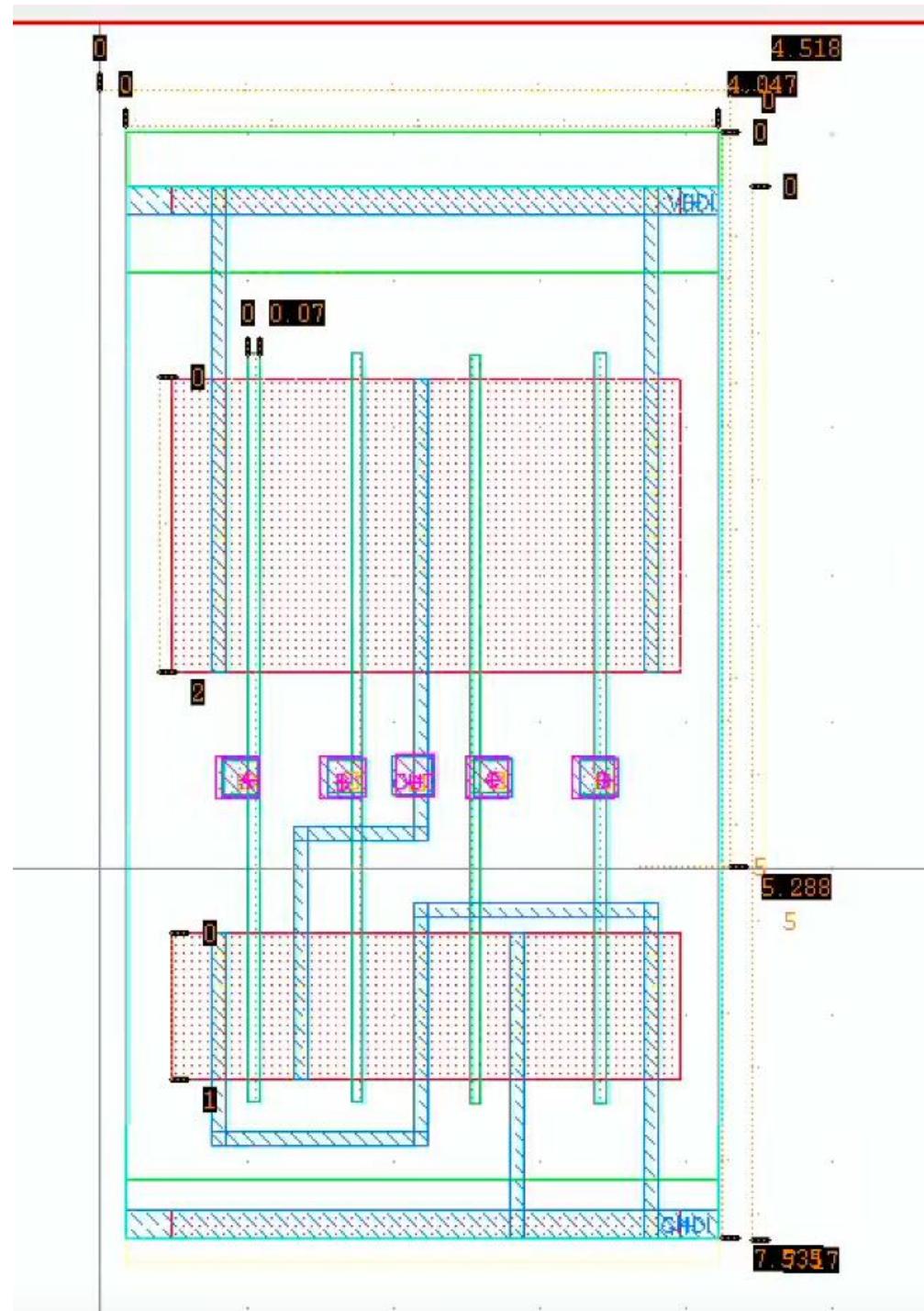
- Width of a single finger and all finger - 2um
- Length of the channel - 70um

### N-MOS

- Width of a single finger and all finger - 1um
- Length of the channel - 70um

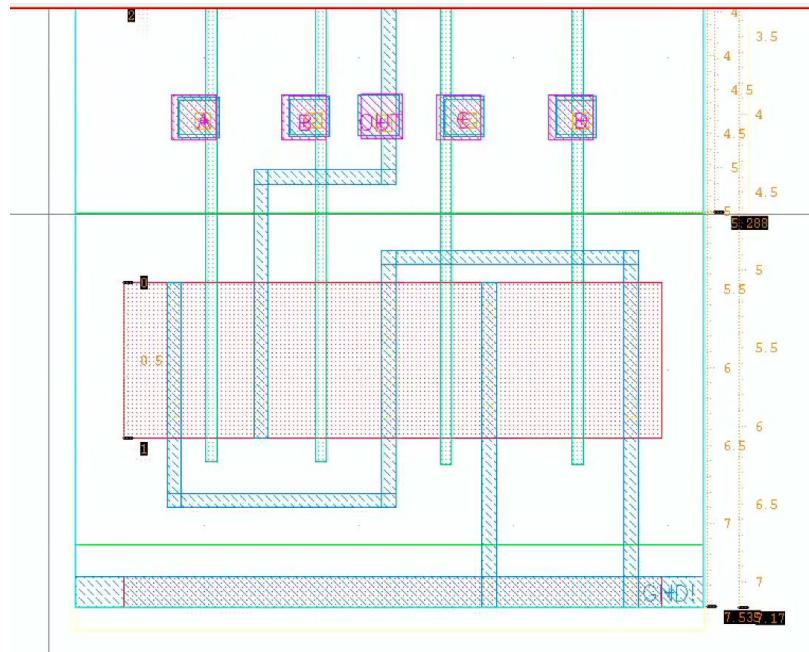


## OAI22 LAYOUT:

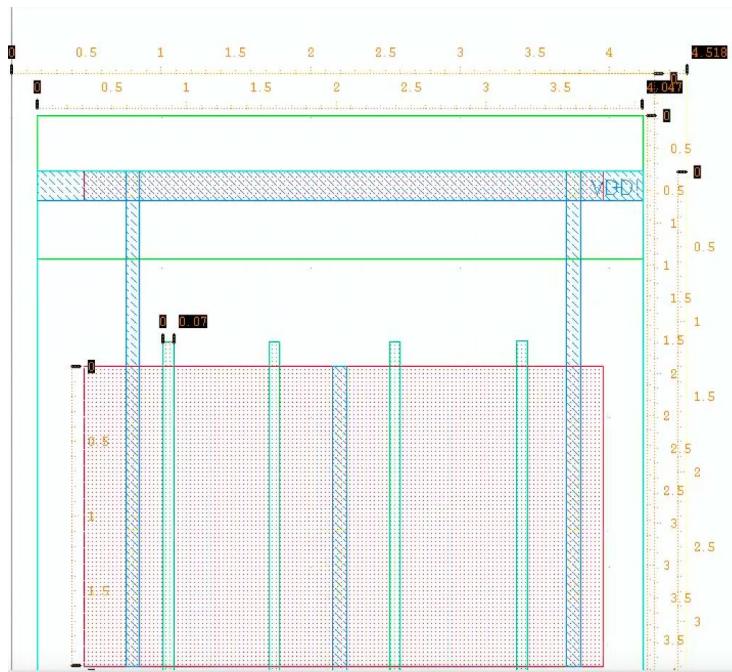


**Dimensions of cell**

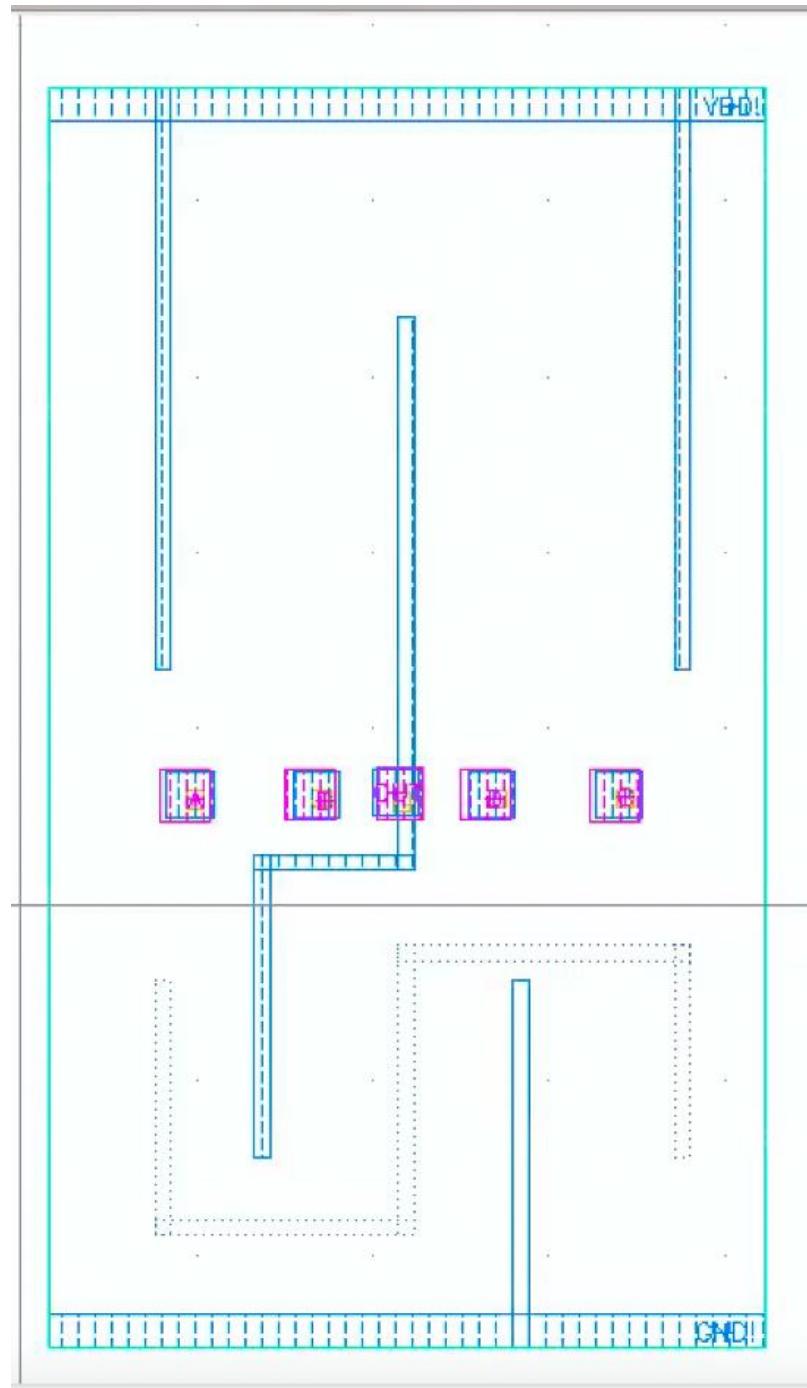
- Height of the cell= 7.535um



- Width of the cell= 4.047um



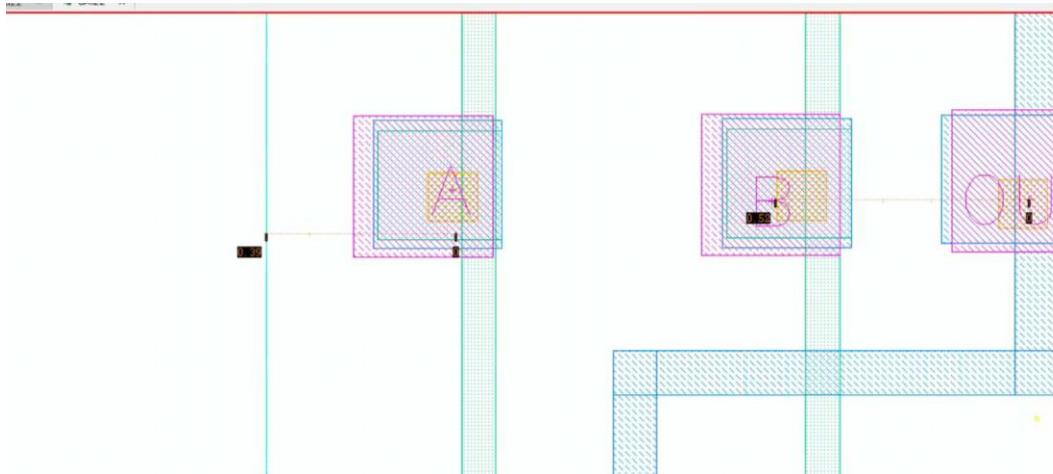
**OAI22 ABSTRACT :**



**OAI22 PIN PITCH AND OFFSET:**

The pin pitch and offset measurement requirements are satisfied:

- Pin pitch= 0.52
- Offset= 0.39



## OAI22 NETLIST :

Calibre Interactive - PEX v2013.2\_18.13

File Transcript Setup  
Rules Inputs Outputs Run Control Transcript Run PEX Start RVE

```

non-top-level nets = 0
degenerate nets = 2
merged nets = 0
error nets = 0
-----  
CALIBRE XRC WARNING / ERROR Summary  
-----  
XRC Warnings = 0  
XRC Errors = 0
-----  
--- CALIBRE FORMATTER COMPLETED - Tue Oct 25 00:08:11 2022
--- TOTAL CPU TIME = 1 REAL TIME = 2 LVHEAP = 39/81/467 MALLOC = 29

```

3 Warnings |

This Linux release is not supported for use with Calibre products.  
This Linux release is not supported for use with Calibre products.  
This Linux release is not supported for use with Calibre products.

PEX Netlist File - OAI22.pex.netlist

File Edit Options Windows

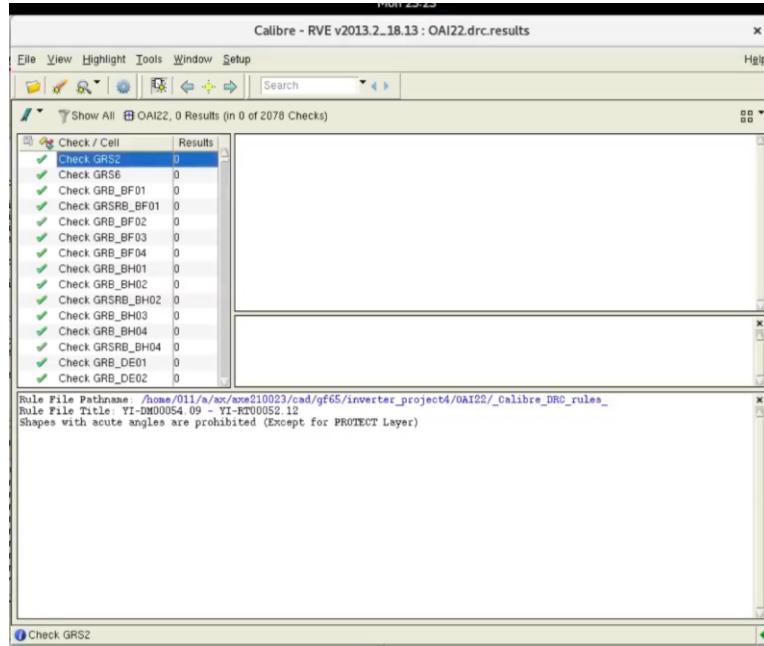
```

* File: OAI22.pex.netlist
* Created: Tue Oct 25 00:08:09 2022
* Program "Calibre XRC"
* Version "v2013.2_18.13"
*
include "OAI22.pex.netlist.pex"
subckt OAI22 _VDD GND! VDD! A B D C
*
* C C
* D D
* B B
* A A
* VDD! VDD!
* GND! GND
* OUT OUT
XDO_noxref N GND! D0_noxref_pos N VDD! D0_noxref_neg DIODENWX AREA=2.39024e-11
+ PERIM=1.9618e-05
XMMN0 N OUT MMN0_d N A MMN0_g N NET26 MMN0_s N GND! D0_noxref_pos NFET L=7e-08
+ W=1e-06 AD=3.18e-13 As=5.31e-13 PD=1.636e-06 PS=3.062e-06 NRH=0.286 NRS=0.205
+ M=1 NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=5.31e-07 SB=2.874e-06 SD=0
+ PANW1=0 PANW2=0 PANW3=0 PANW4=7e-15 PANW5=3.5e-15 PANW6=7e-15 PANW7=1.4e-14
+ PANW8=1.4e-14 PANW9=2.8e-14 PANW10=2.8e-15
XMMN1 N OUT MMN1_d N B MMN1_g N NET26 MMN1_s N GND! D0_noxref_pos NFET L=7e-08
+ W=1e-06 AD=3.18e-13 As=3.65e-13 PD=1.636e-06 PS=1.736e-06 NRH=0.32 NRS=0.404
+ M=1 NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=1.237e-07 SB=2.168e-06 SD=0
+ PANW1=0 PANW2=0 PANW3=0 PANW4=7e-15 PANW5=3.5e-15 PANW6=7e-15 PANW7=1.4e-14
+ PANW8=1.4e-14 PANW9=2.8e-14 PANW10=2.8e-15
XMMN2 N NET26 MMN1_d N C MMN2_g N GND! MMN2_s N GND! D0_noxref_pos NFET L=7e-08
+ W=1e-06 AD=3.18e-13 As=3.915e-13 PD=1.636e-06 PS=1.783e-06 NRH=0.332 NRS=0.248
+ M=1 NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=0 SA=2.043e-06 SD=1.362e-06 SD=0
+ PANW1=0 PANW2=0 PANW3=0 PANW4=7e-15 PANW5=3.5e-15 PANW6=7e-15 PANW7=1.4e-14
+ PANW8=1.4e-14 PANW9=2.8e-14 PANW10=2.8e-15
XMMN2 N NET26 MMN2_d N C MMN2_g N GND! MMN2_s N GND! D0_noxref_pos NFET L=7e-08
+ W=1e-06 AD=3.18e-13 As=3.915e-13 PD=1.636e-06 PS=1.783e-06 NRH=0.311 NRS=0.535

```

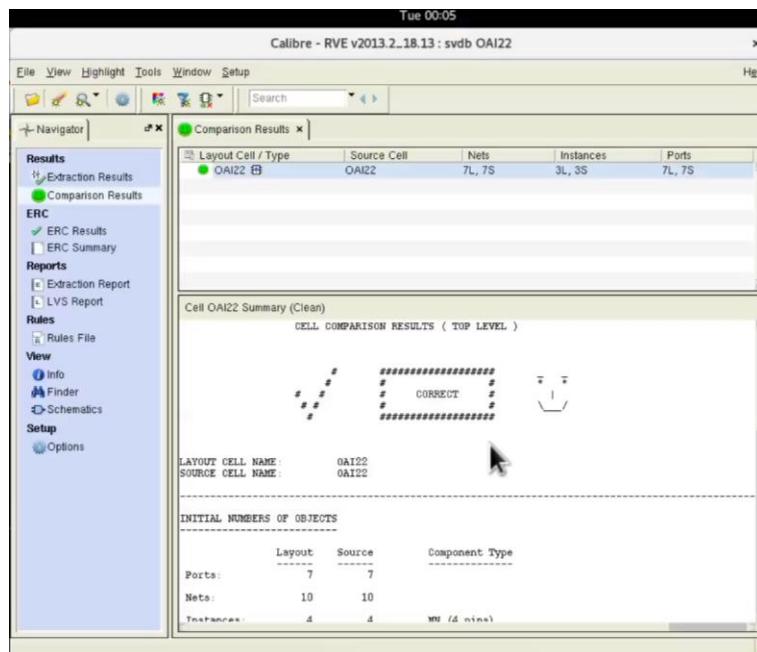
## OAI22 DRC CHECK:

0 DRC errors - Successfully ran the DRC check for OAI22 Layout and the is 0 errors after 2078 Checks.



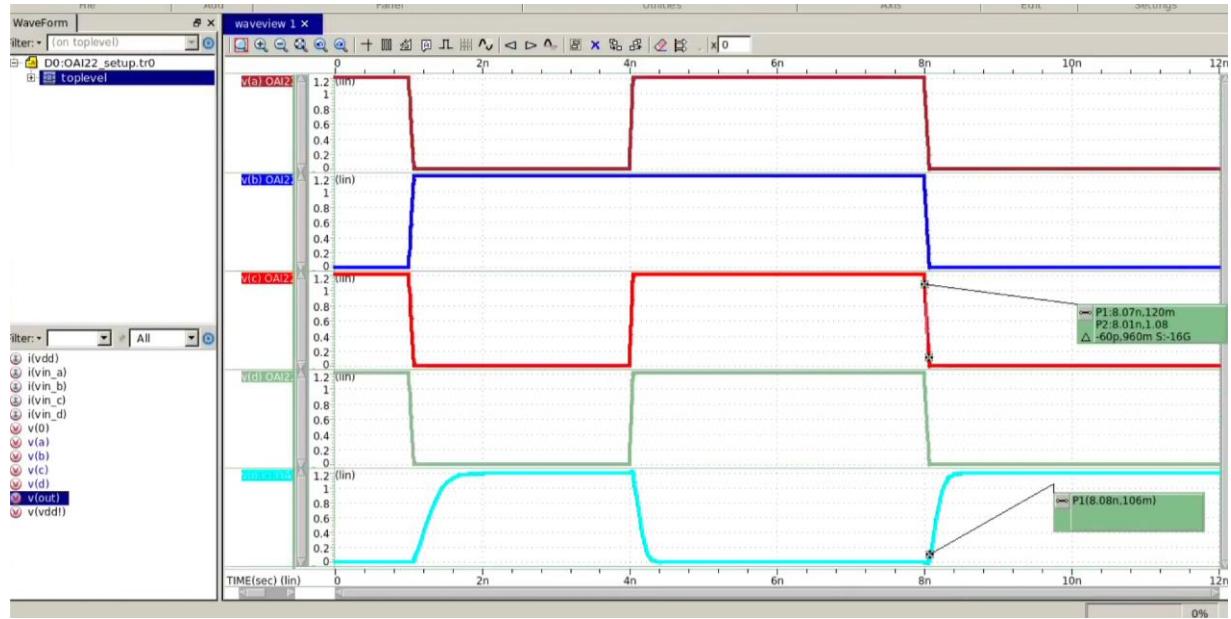
## OAI22 LVS CHECK:

0 LVS errors - Layout and Schematic of the OAI22 Gate is **CORRECT**



## OAI22 SIMULATION :

The waveform is generated using the OA122 netlist and the input slew rate is 60 ps and a 70 fF load capacitance is given to the netlist when simulating.



### OAI22 TRUTH TABLE :

<b>Input A</b>	<b>Input B</b>	<b>Input C</b>	<b>Input D</b>	<b>Output</b>
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1

1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

# AOI211

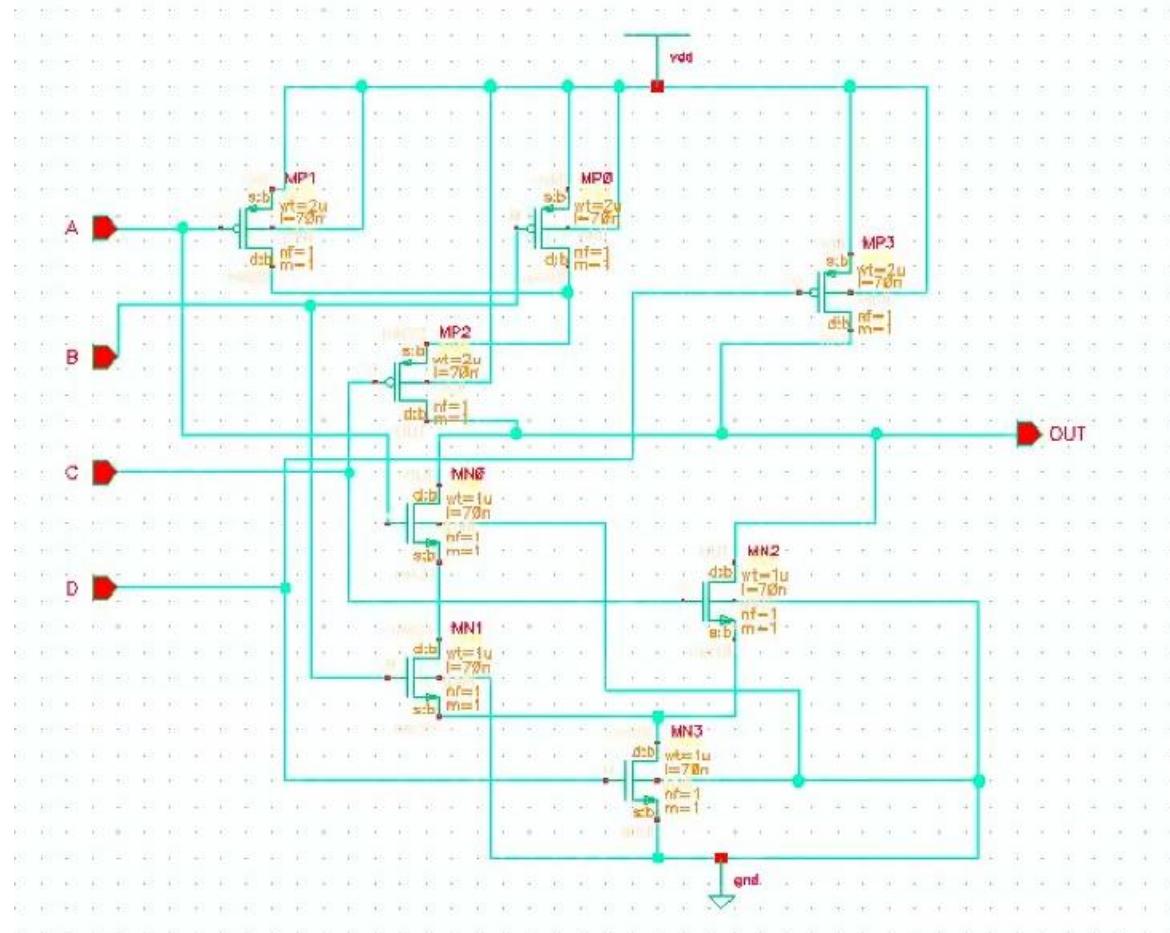
## AOAI211 SCHEMATIC:

### P-MOS

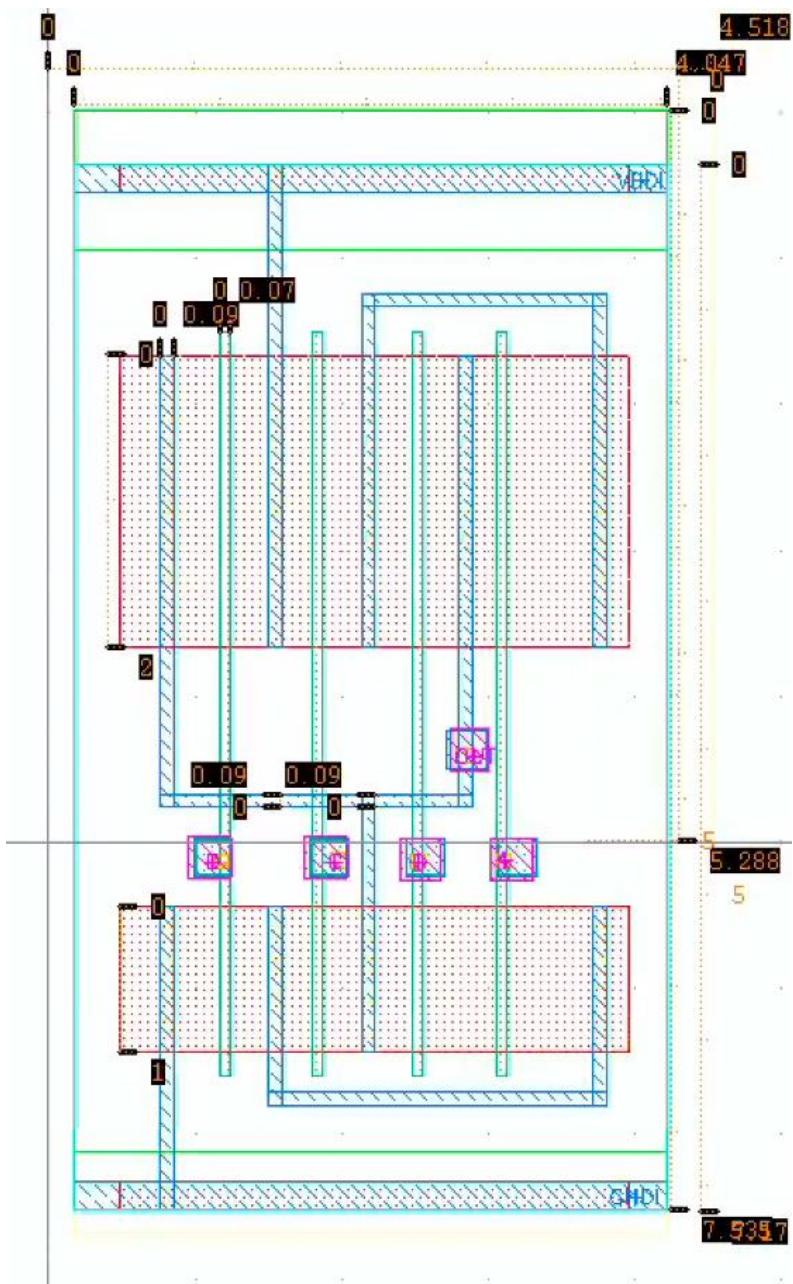
- Width of a single finger and all finger - 2um
- Length of the channel - 70um

### N-MOS

- Width of a single finger and all finger - 1um
- Length of the channel - 70um

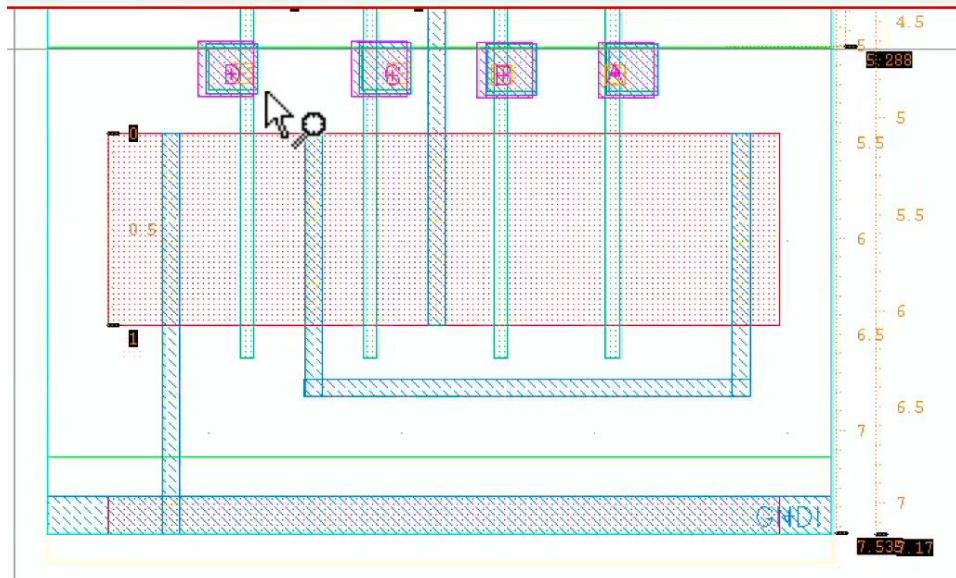


## AOAI211 LAYOUT:

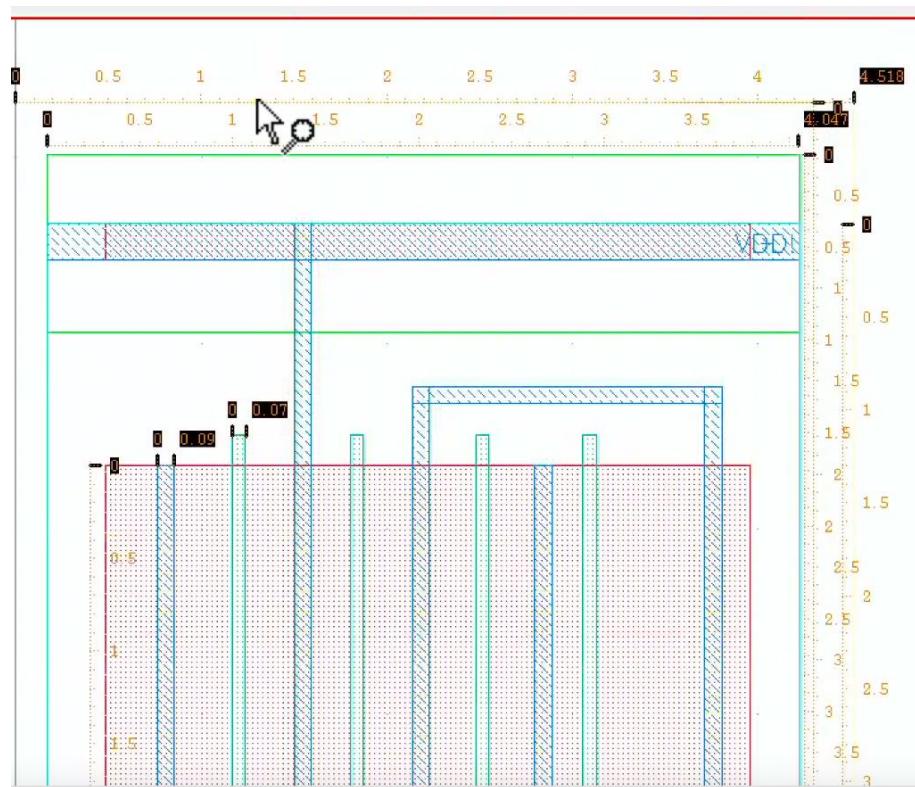


## Dimensions of cell

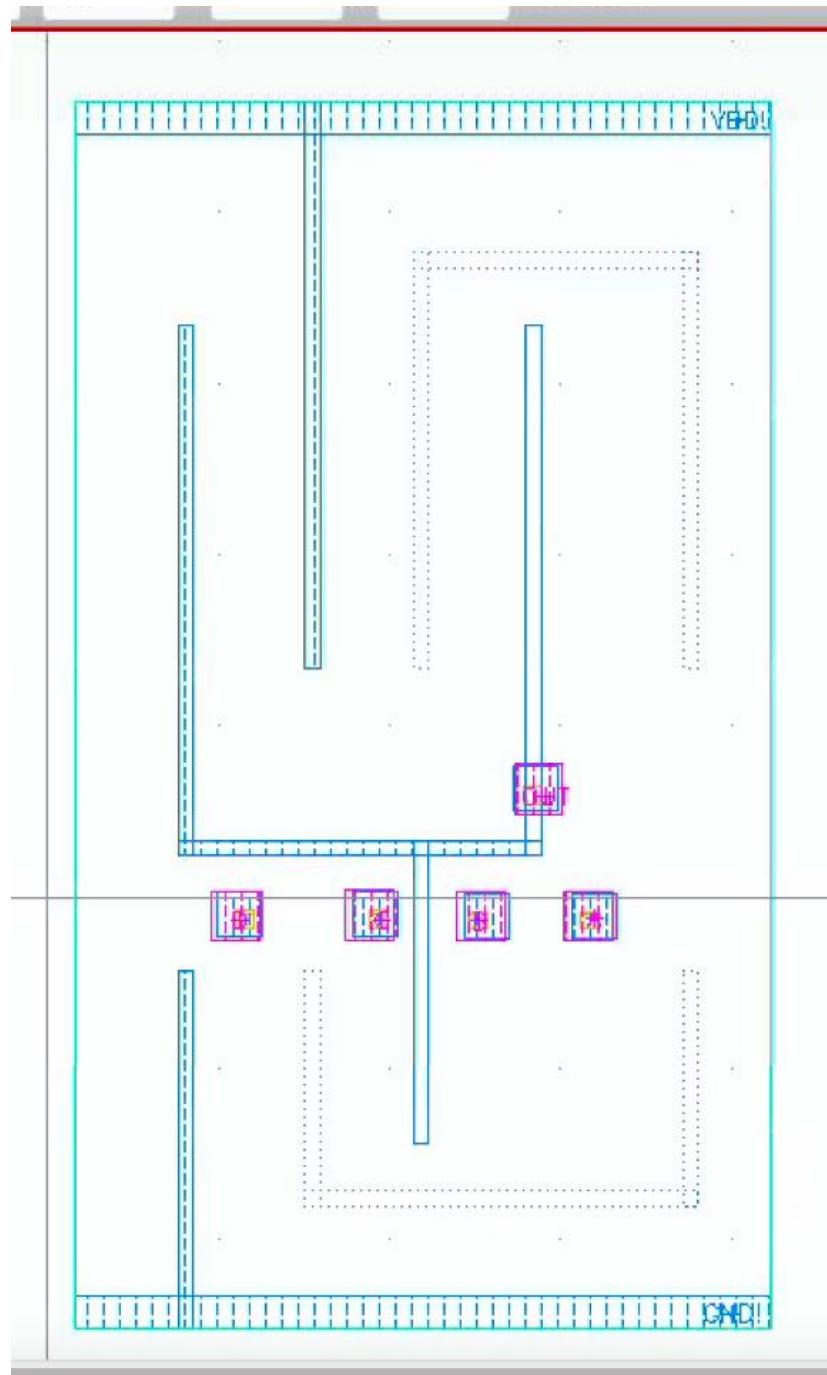
- Height of the cell= 7.535um



- Width of the cell= 4.047um



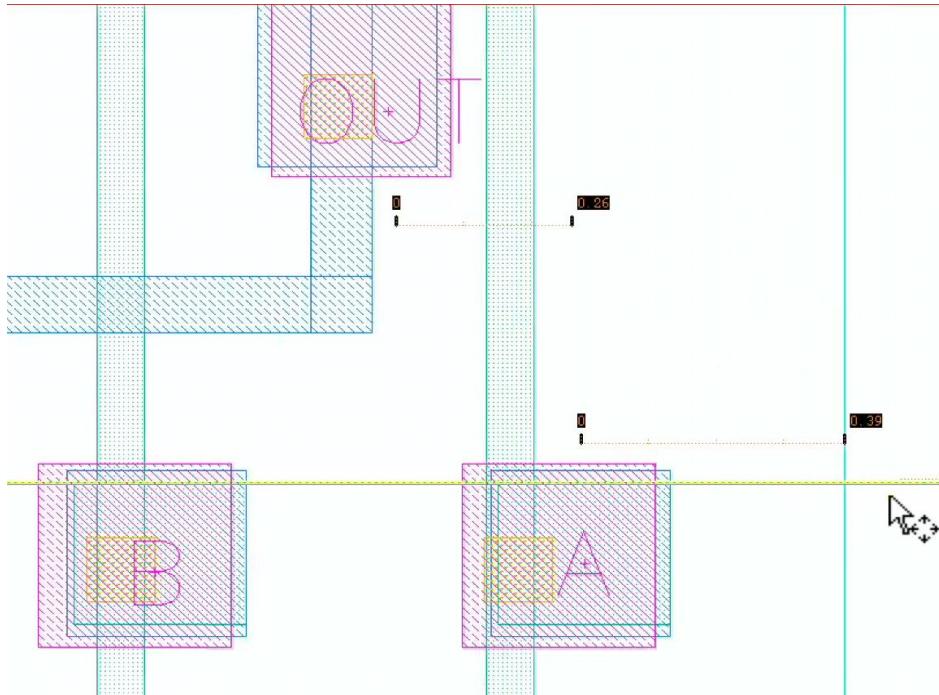
## **AOAI211 ABSTRACT :**



## A0AI211 PIN PITCH AND OFFSET:

The pin pitch and offset measurement requirements are satisfied:

- Pin pitch= 0.26
- Offset= 0.39



## A0AI211 NETLIST :

```
(F)Select:0 SelN0:0 SelD:0 SelO:0|X 2.515 Y 0.195 BX
File Transcript Setup Help
PEX v2013.2..18.13
File Edit Options Windows
PEX Netlist File - A0AI211.pex.netlist
File Transcript Setup Help
PEX Interactive - PEX v2013.2..18.13
non-top-level nets = 0
degenerate nets = 0
merged nets = 0
error nets = 0

CALIBRE xRC WARNING / ERROR SUMMARY
-----  

-----  

xRC Warnings = 0  

xRC Errors = 0
-----  

--- CALIBRE xRC: FORMATTER COMPLETED - Tue Oct 25 00:24:36 2022
--- TOTAL CPU TIME = 1 REAL TIME = 2 LVHEAP = 39/81/467 MALLOC = 29

-----  

-----  

3 Warnings |  

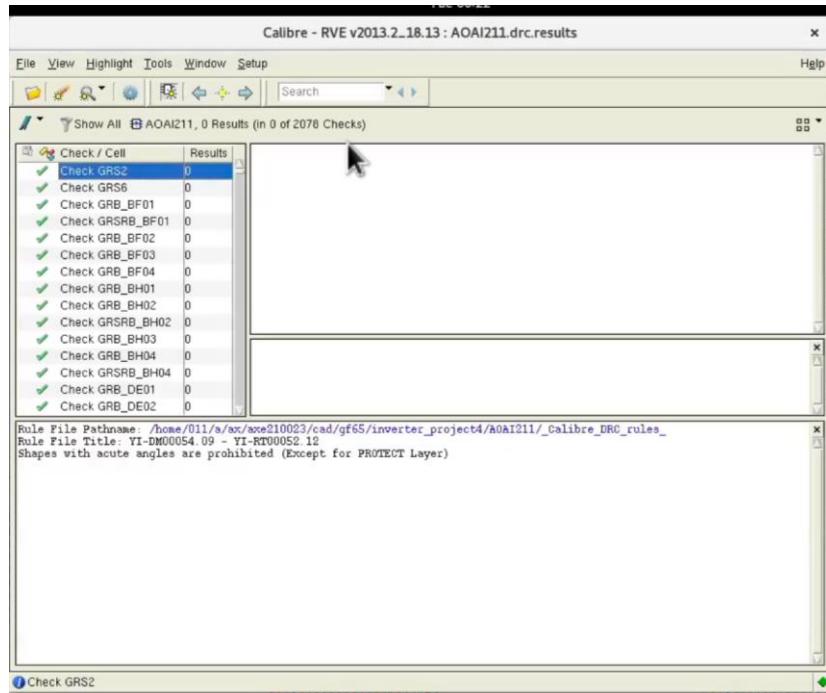
This Linux release is not supported for use with Calibre products  

This Linux release is not supported for use with Calibre products.  

This Linux release is not supported for use with Calibre products.
-----
```

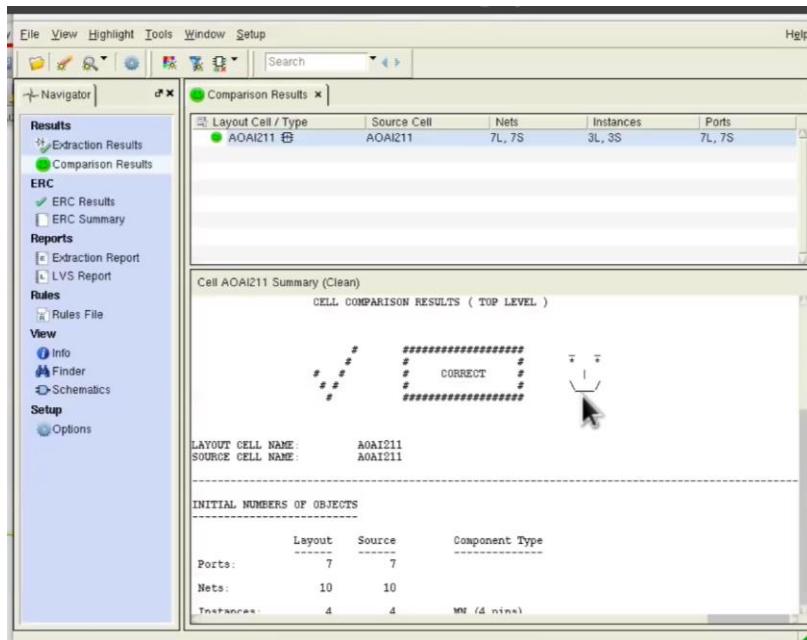
## AOAI211 DRC CHECK:

0 DRC errors - Successfully ran the DRC check for AOA211 Layout and the is 0 errors after 2078 Checks.



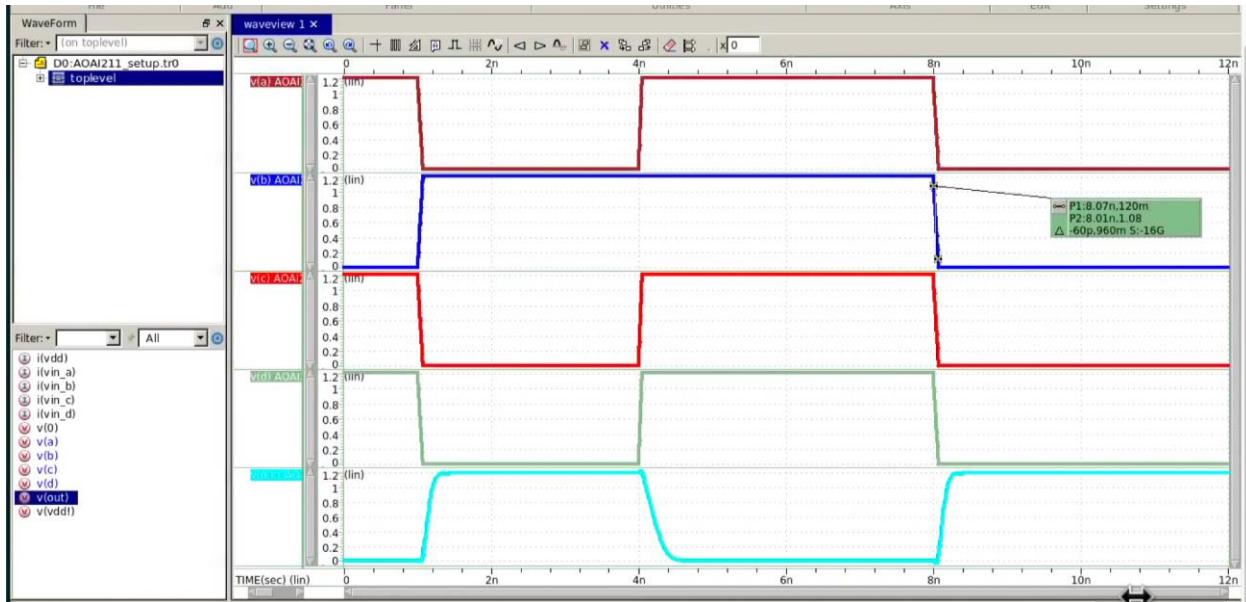
## AOAI211 LVS CHECK:

0 LVS errors - Layout and Schematic of the AOAI211 Gate is **CORRECT**



## AOAI211 SIMULATION :

The waveform is generated using the AOAI211 netlist and the input slew rate is 60 ps and a 70 fF load capacitance is given to the netlist when simulating.



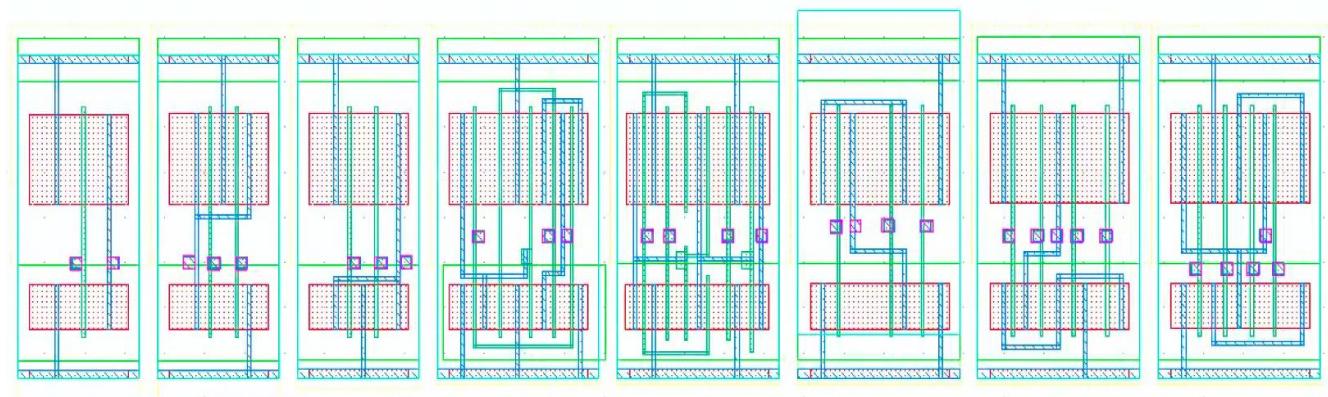
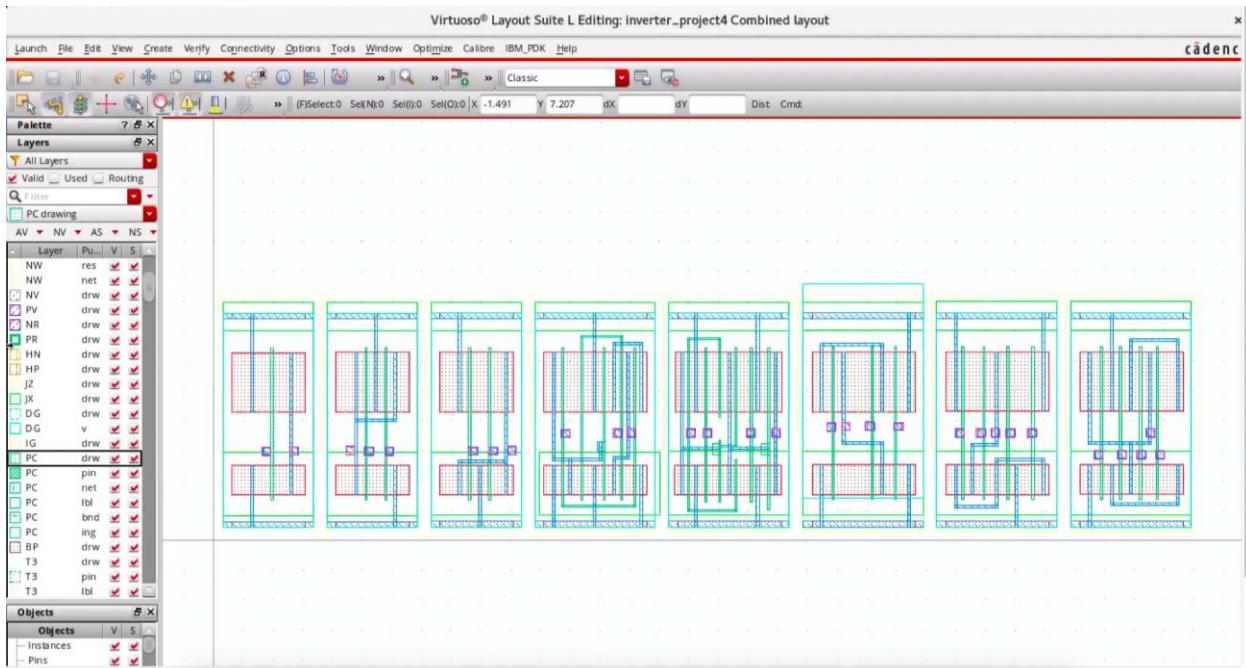
## AOAI211 TRUTH TABLE :

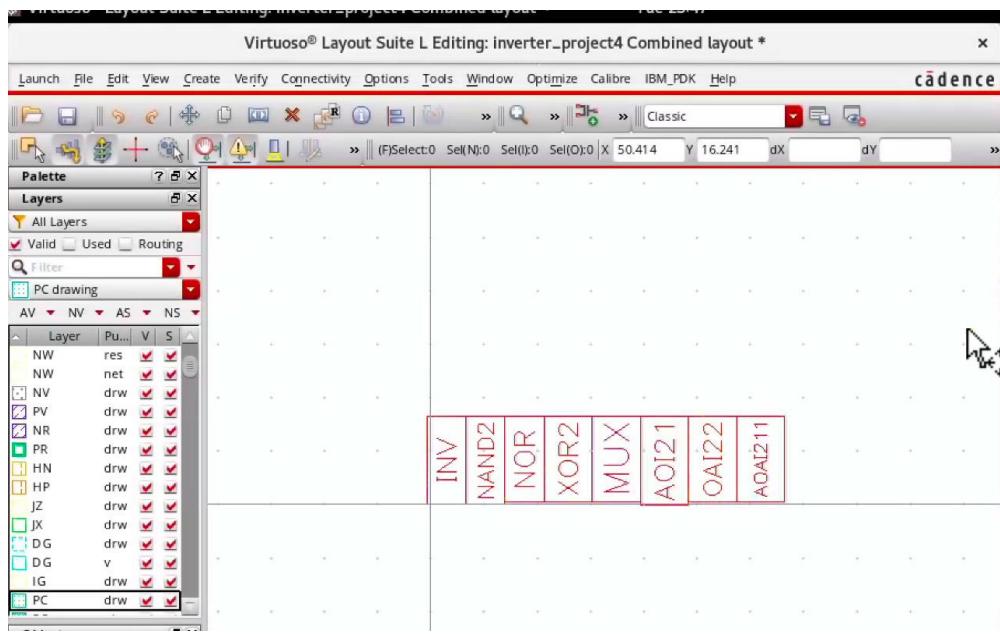
Input A	Input B	Input C	Input D	Output
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0

1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

## ALL MERGED/COMBINED CELLS :

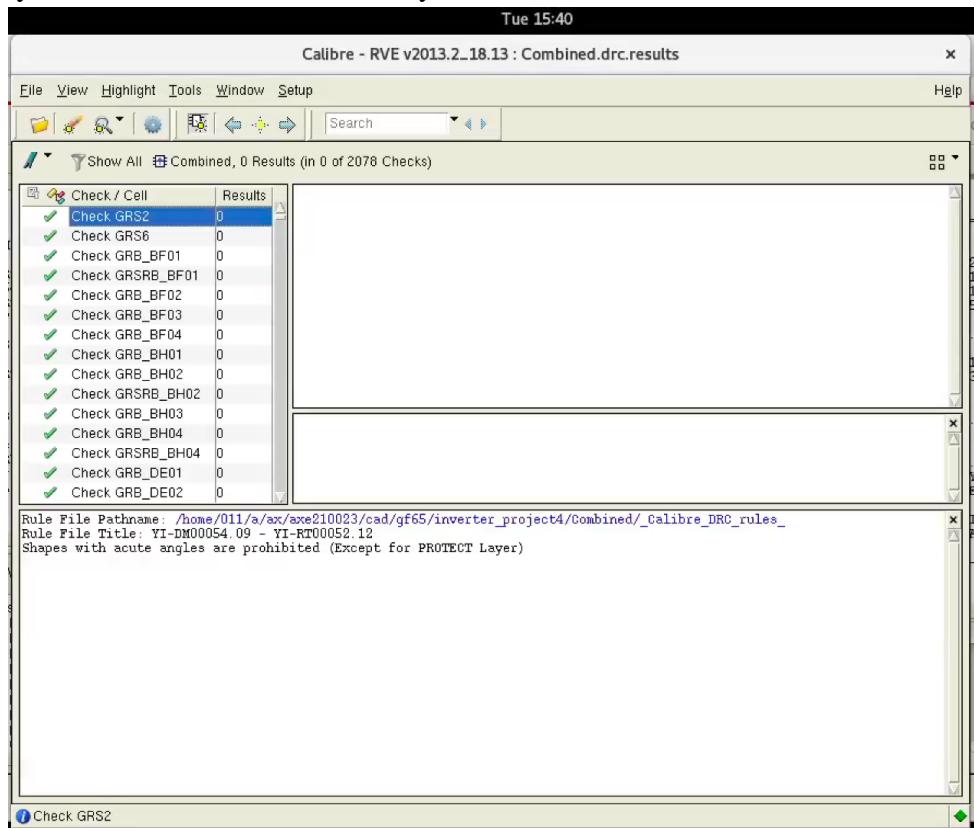
The Combined layout of All 8 Gates - INV, NAND2, NOR2, XOR2, MUX2:1, AOI21, OAI22 and AOAI211 are shown below. The layouts for each cell have been merged together flawlessly and then DRC check is also run to verify the accuracy and errors.





## COMBINED CELLS DRC CHECK :

Successfully ran the DRC check for the Layouts and there are 0 errors after 2078 Checks.



**CONCLUSION :** Hence all the Project goals have been completed successfully.