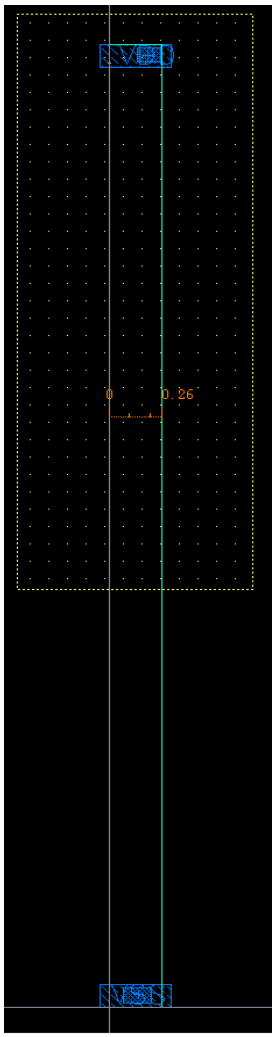
Project 6 Tutorial:

Create a filler cell:

I) Design of Filler cell: Filler should have layers:
- (i) **M1**, for VDD and GND with the **pin** and **label**
- **(ii) NW**
- **(iii) prBoundary** (boundary)



The width of filler should be equal to exactly **1 pitch (0.26 um)**. Make sure that the height of the filler is equal to the height of other cells in your library. Check only DRC.

II) Steps to generate .lef file:

i) Open virtuoso:

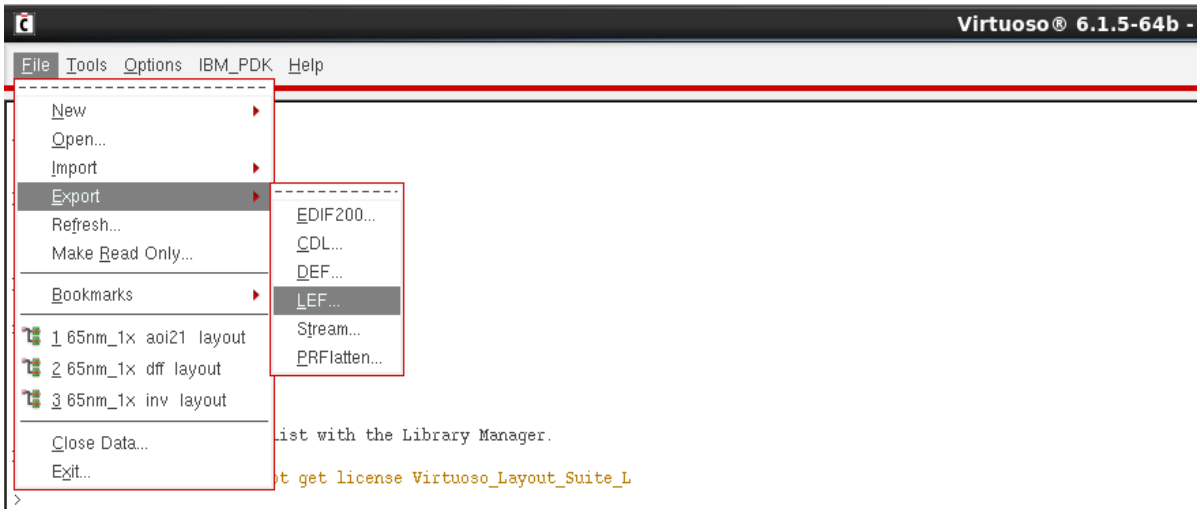
```
cd cad/gf65

. /proj/cad/startup/profile.ee7325

virtuoso &
```

ii) To export .lef (Before doing this, please generate abstract views of all your cells including DFF)

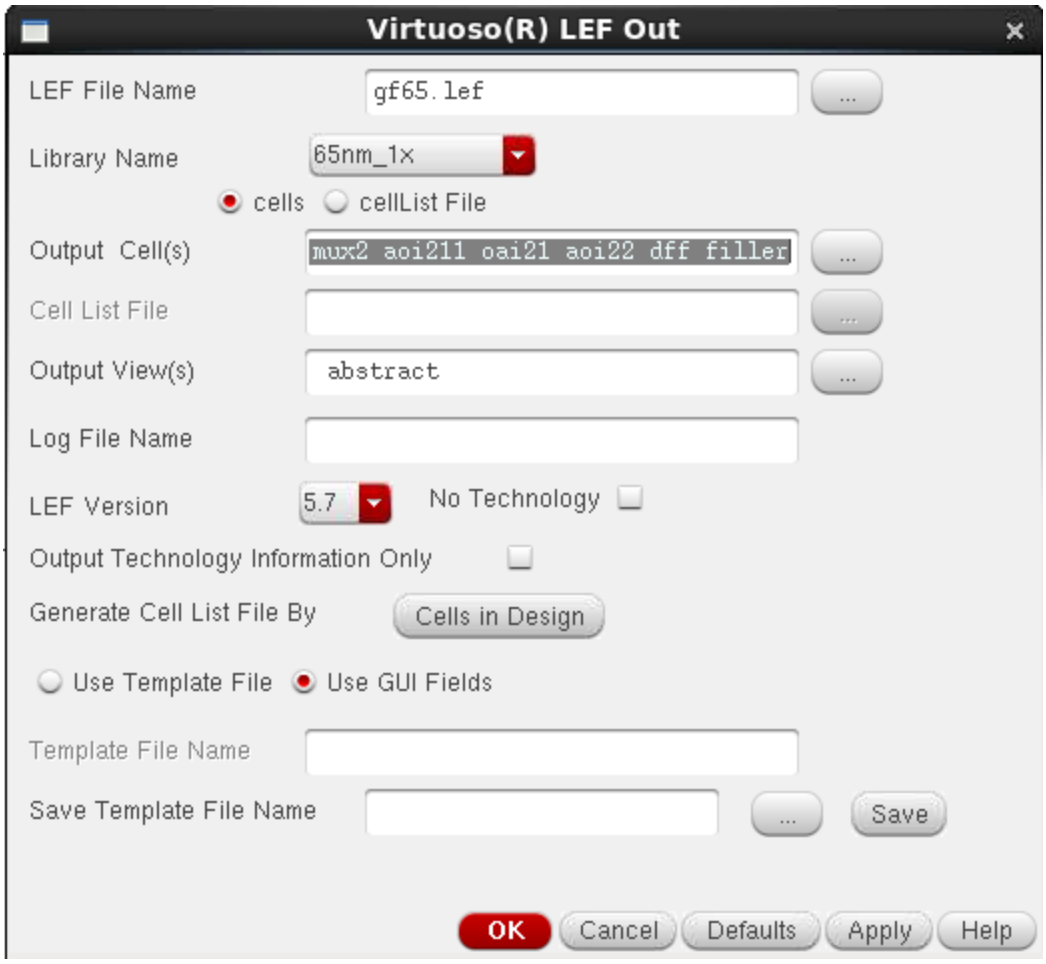
File -> Export -> LEF



Fill in the details

- LEF File Name: can give any name with .lef extension, I have given it as gf65.lef
- Library Name should be the name of your designed library
- Output Cell(s): Select all the cells in your library (including dff and filler).
- Output View(s): abstract

Click OK



Ignore the warnings, if you get errors then you are not doing it right.

You have now created a lef file, but you need to make some changes to your lef file so that Innovus understands your lef file.

- To see your generated lef file, open a new terminal and type the following:

```
cd cad/gf65
ls
gedit gf65.lef
```

- Delete lines 1 to (END VRX_M1) and replace it with contents of “gf65_tlef.lef” file.

  In gf65_tlef.lef, at line 304 and 326, change this encircled number to your cell height.

```
300  SITE  CoreSite
301      CLASS       CORE ;
302      SYMMETRY    Y ;
303      SYMMETRY    X ;
304      SIZE        0.260 BY 4.94 ;
305  END  CoreSite
306
307  SITE  TDCoverSite
308      CLASS       CORE ;
309      SIZE        0.0500 BY 0.0500 ;
310  END  TDCoverSite
311
312  SITE  SBlockSite
313      CLASS       CORE ;
314      SIZE        0.0500 BY 0.0500 ;
315  END  SBlockSite
316
317  SITE  PortCellSite
318      CLASS       PAD ;
319      SIZE        0.0500 BY 0.0500 ;
320  END  PortCellSite
321
322  SITE  Core
323      CLASS       CORE ;
324      SYMMETRY    Y ;
325      SYMMETRY    X ;
326      SIZE        0.260 BY 4.94 ;
327  END  Core
```

  Now your lef file is ready.

III) Create .lib and .db file

All .lib files needs to combined, the combined .lib file should have 1 set of all lut(s). Delete VDD and VSS pin information before creating a .db file.

Now, create a .db file using Synopsys lc shell. (Ignore the warnings)

```
lc_shell> read_lib gf65.lib
Reading '/home/eng/v/vks160030/cad/gf65/siliconsmart_gf65/gf65.lib' ...
Warning: Line 1, The default_operating_conditions is not defined. operating_conditions 'gf65' is set
        as the default_operating_conditions. (LBDB-663)
Warning: Line 1, No default 'normalized_driver_waveform" group defined in 'library'. (LBDB-788)
Warning: Overwriting an old technology library '/home/eng/v/vks160030/cad/gf65/siliconsmart_gf65/gf65.db' file with a new one. (UIL-2)
1
lc_shell> write_lib gf65 -format db -output gf65.db
Wrote the 'gf65' library to '/home/eng/v/vks160030/cad/gf65/siliconsmart_gf65/gf65.db' successfully
1
lc_shell>
```

IV) Create synthesized verilog (.v) using gf65.db (Similar to project2), and remember to add header.v to your synthesized verilog file.

Now you have the required files to import your designs into Innovus.

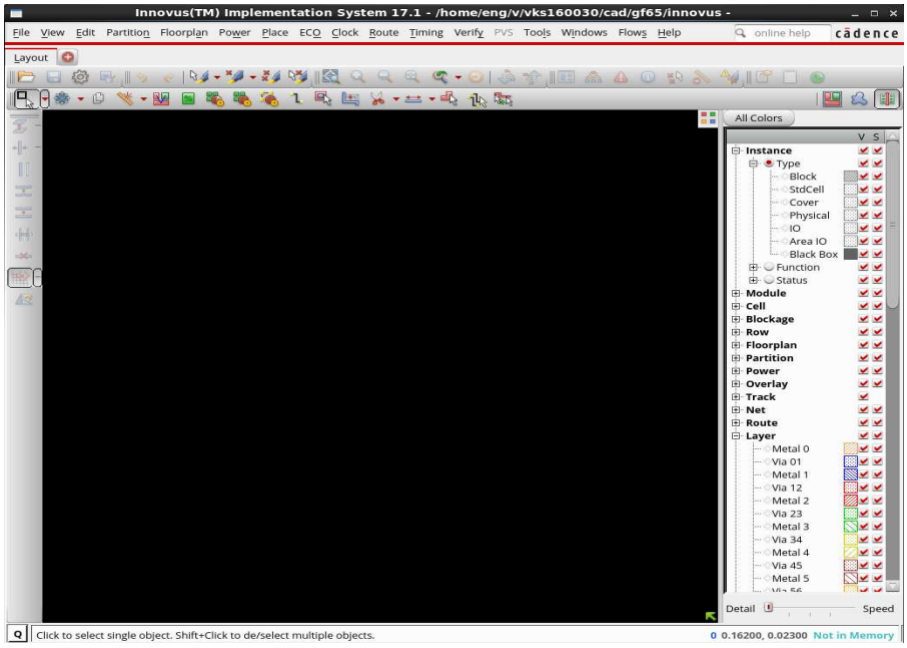
V) Steps to start Innovus:

1) Create a new directory for Innovus in your gf65:

```
cd cad/gf65
mkdir innovus
cd innovus
```

2) Invoke Innovus

```
. /proj/cad/startup/profile.ee7325
innovus
```



Cadence Innovus Tutorial

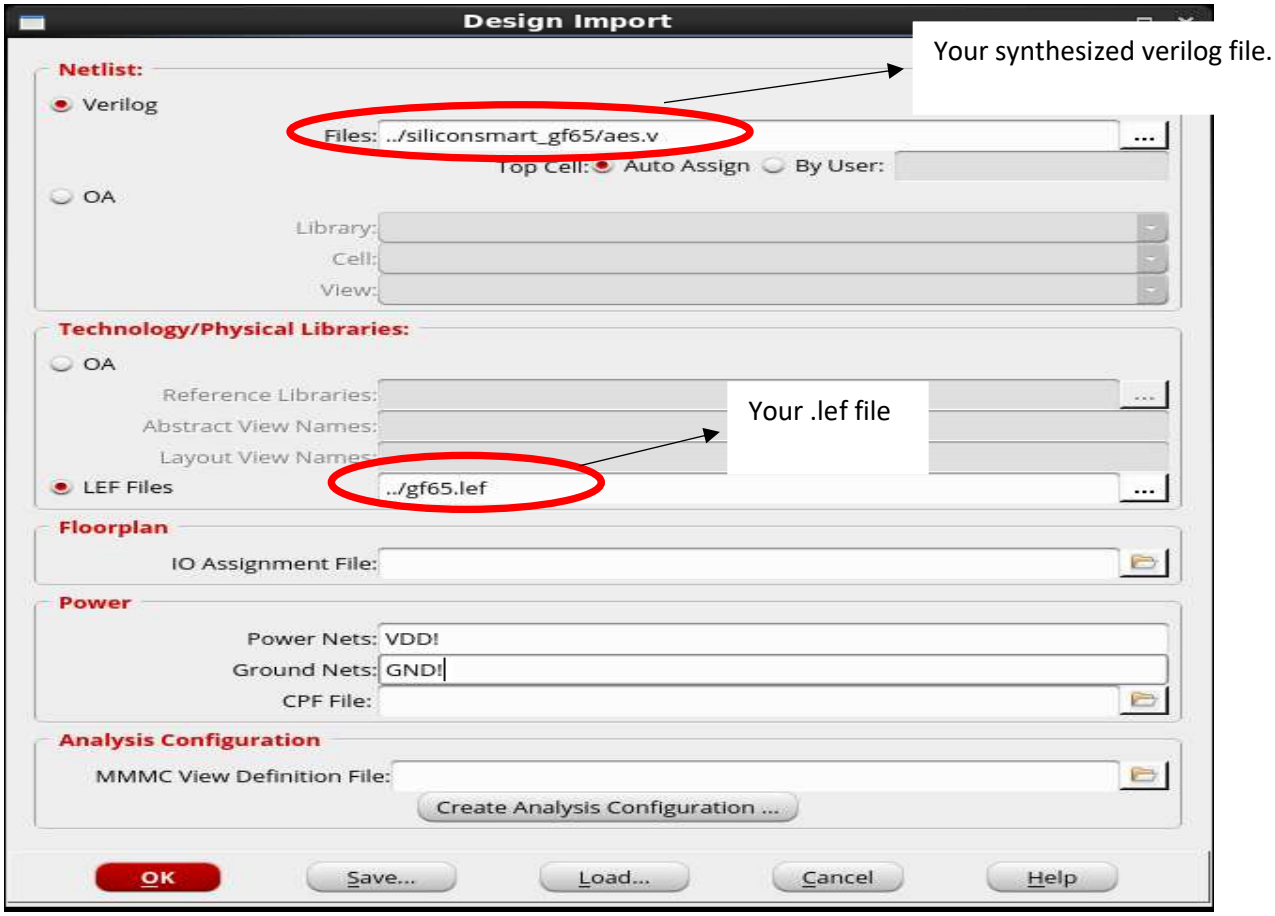
- Innovus is an automatic placement and routing tool, before starting Innovus, you should have .lef (library exchange file) and .v (synthesized netlist from Design Vision) file ready.

Step1: Import Design:

Note: Remove or comment-out “assign” statements in the header part of your synthesized verilog file (.v). If you don’t do this, your design won’t be imported into Innovus.

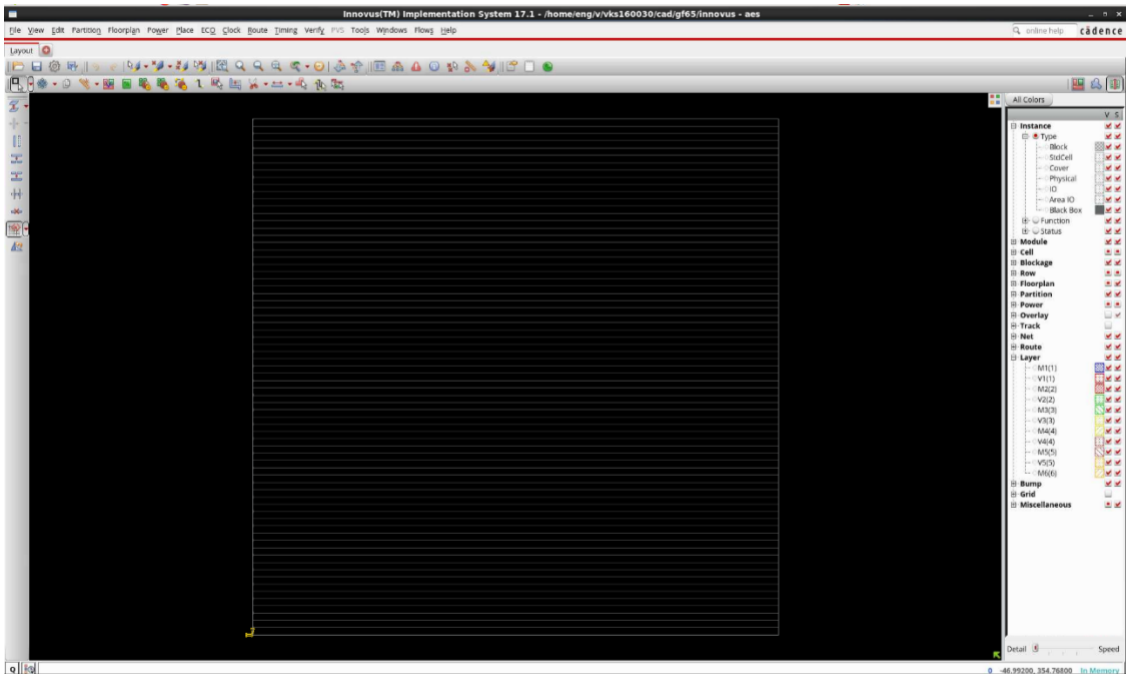
In Innovus GUI Click **File -> Import Design**

Fill in details as shown in the image.



Make sure the names you give in Power Nets and Ground Nets are same as that you have already given in schematic and layout.
Click OK

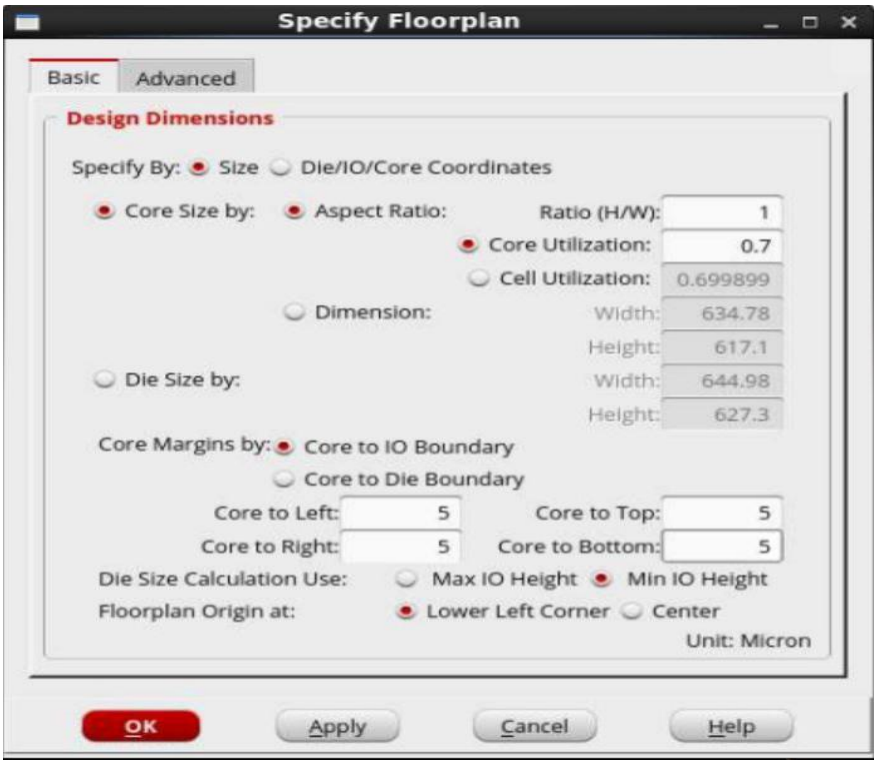
If you do not have any error then you should be able to see the imported outline as shown in the image below:



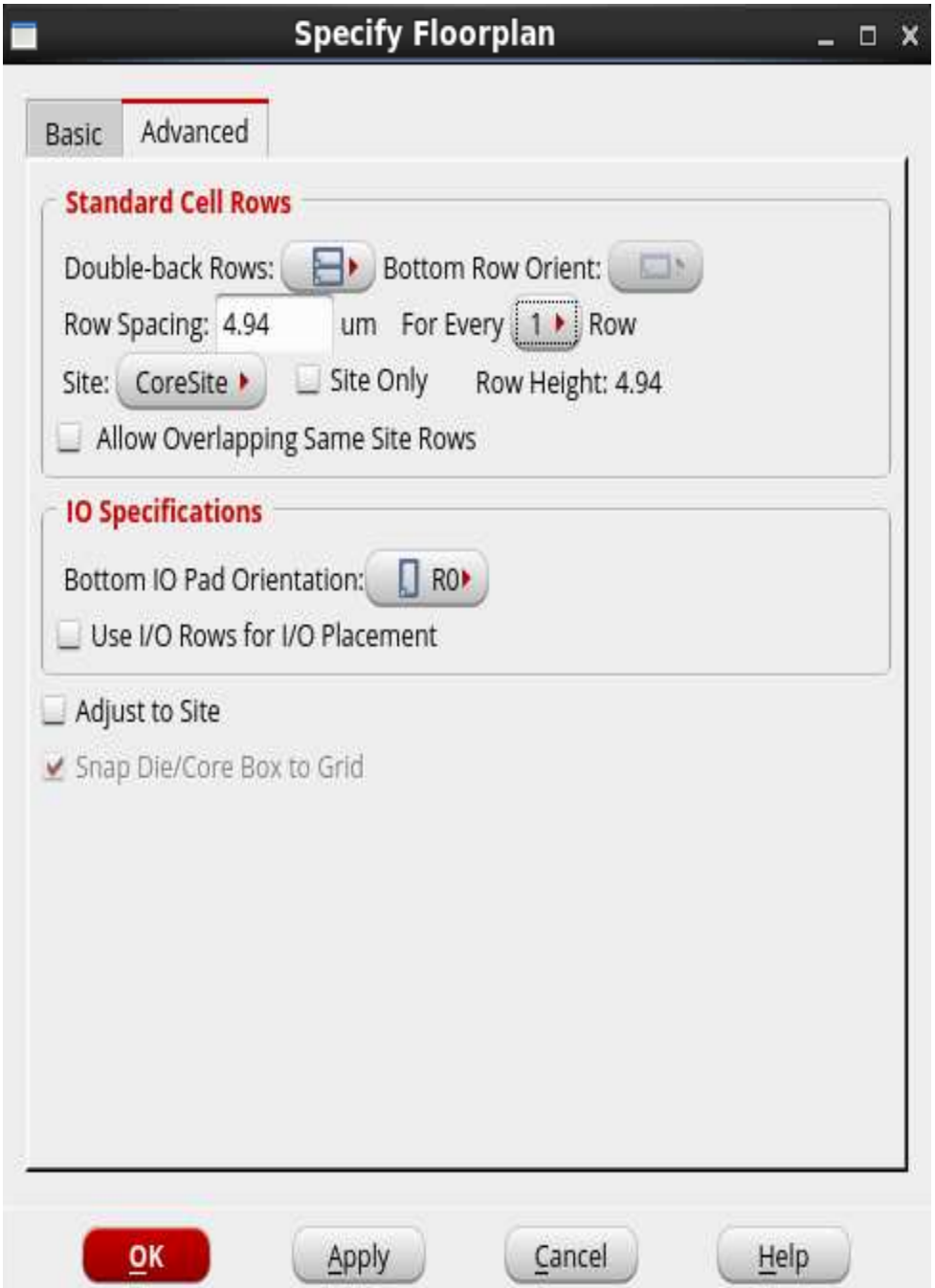
Step2: Floorplanning

Floorplan -> Specify Floorplan

In the **Basic** tab, fill in the details as shown in image:

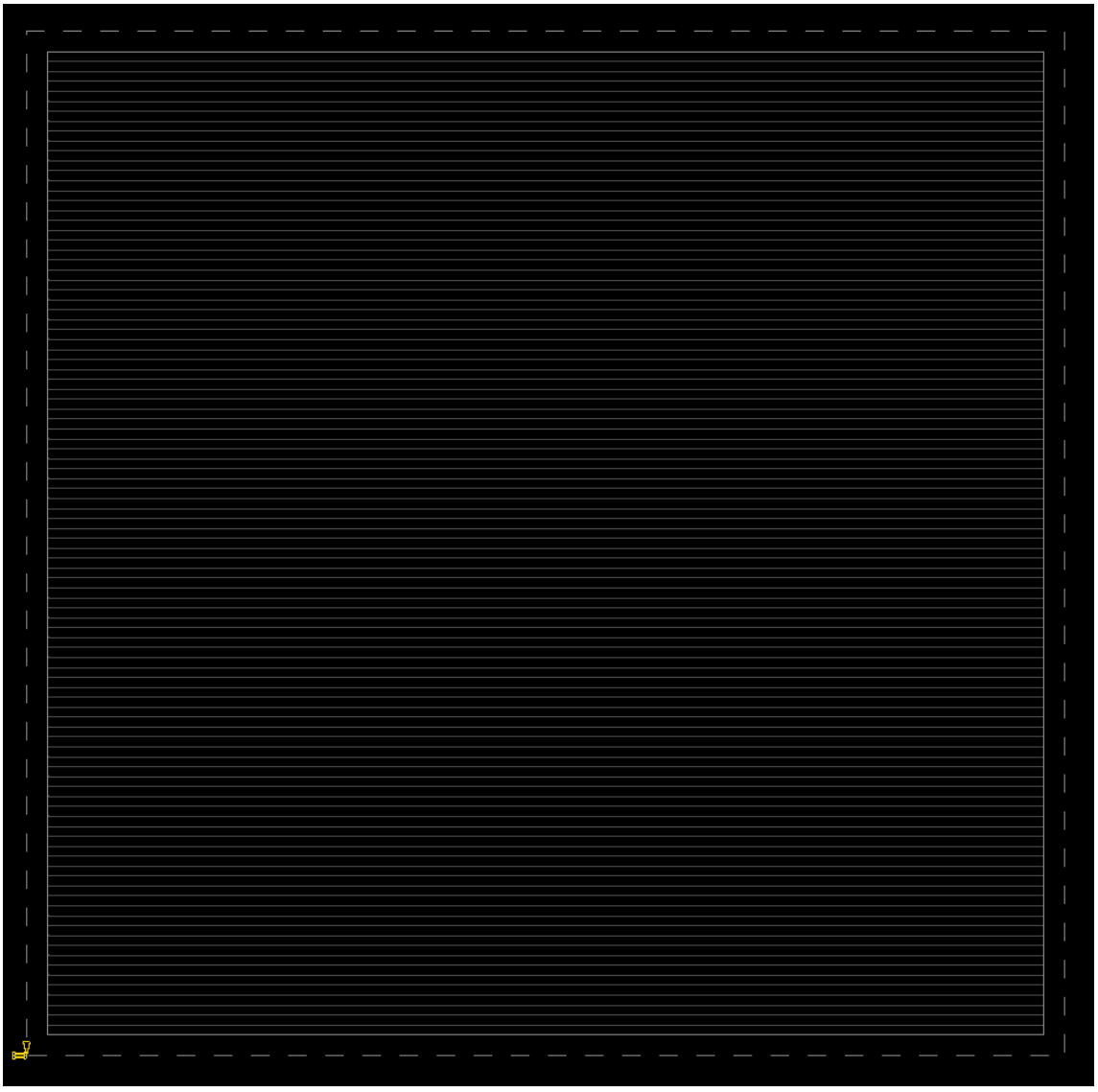


In the **Advanced** tab: Under the heading **Standard Cell Rows**, change **Double-back Rows** (as shown in picture).
Row Spacing: Your cell height; Change **For Every** to **1;**



Click OK

After floorplanning, your Innovus will looks like this. (You can use key **F** to zoom fit)



Step 3: Power/ Ground

i) Power -> Connect Global Nets

Under the heading **Power Ground Connection**, In **Connect** select **Tie High;**

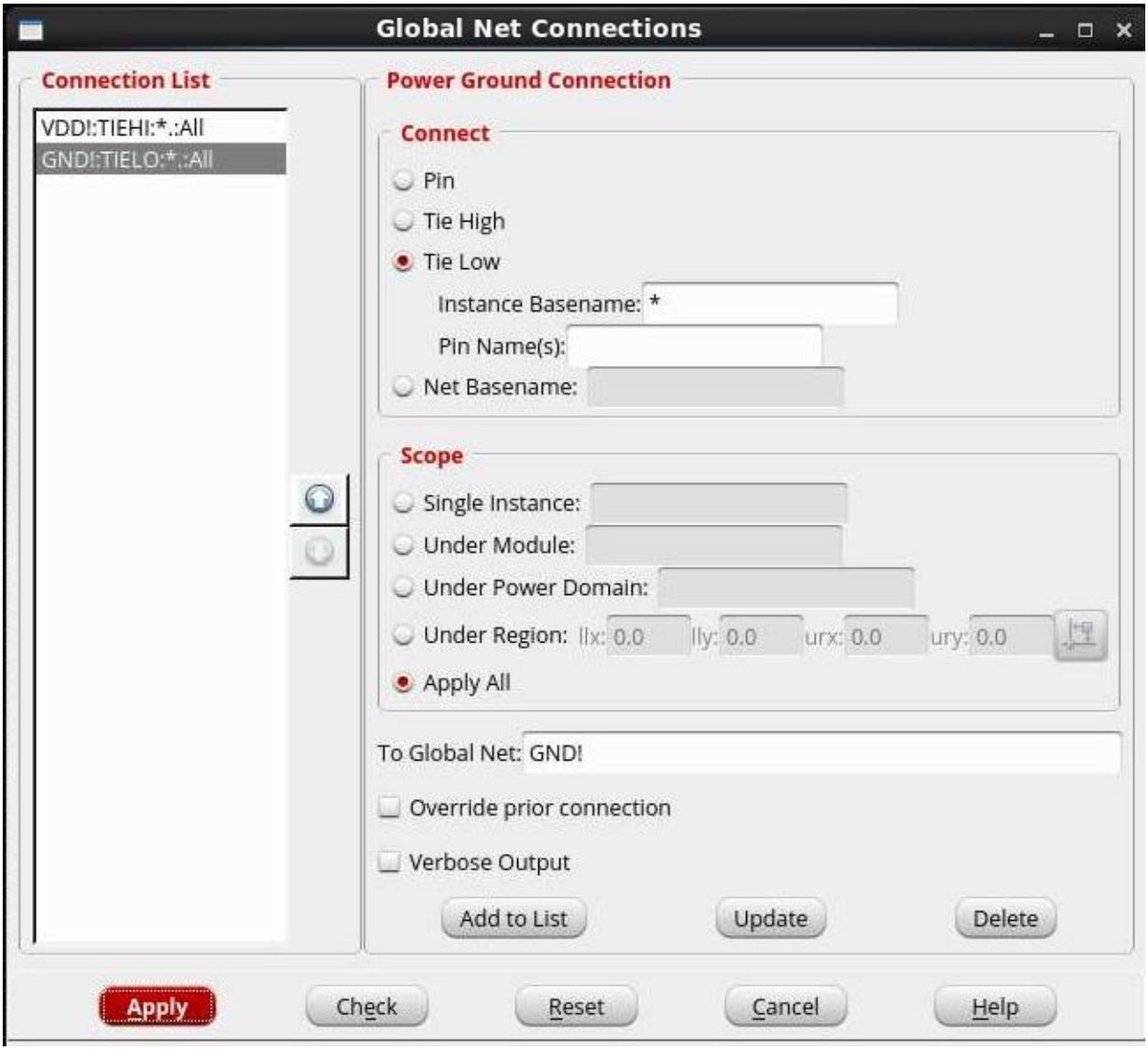
In **Scope** select **Apply All**;

At **To Global Net**, type **VDD!**

Click on **Add to List**

You will see **VDD!:TIEHI:*All** in **Connection List** (top left corner)

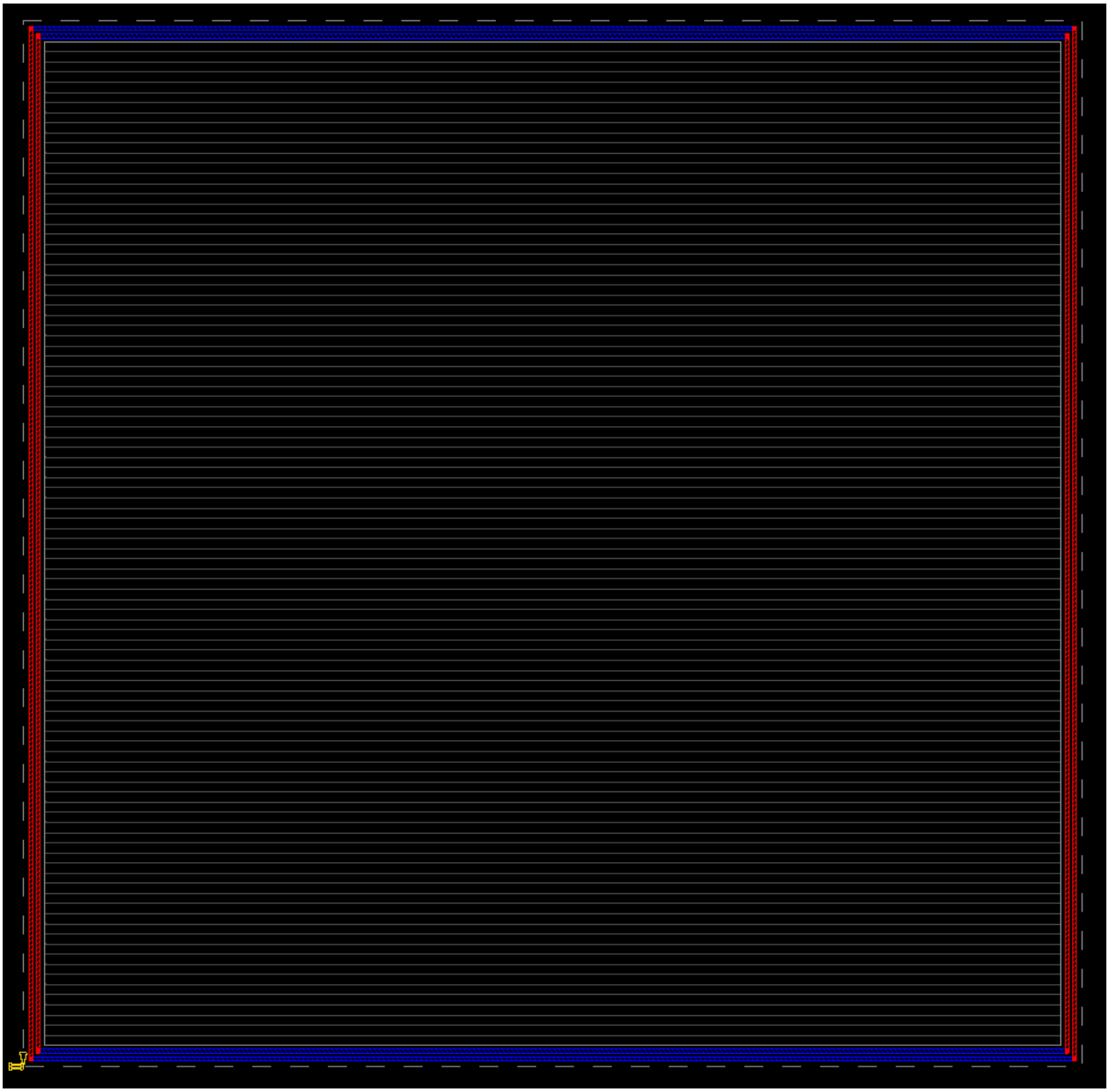
Similarly, under the heading **Power Ground Connection**, In **Connect** select **Tie Low;**
In **Scope** select **Apply All**;
At **To Global Net**, type **GND!**
Click on **Add to List**
You will see **GND!:TIELO:*All** in **Connection List** (top left corner)



Click **Apply,** go to Innovus command window and check if you have any errors, and close the **Global Net Connections** window. If you have errors in the Innovus command window, you have not imported the design properly.

ii) Add Rings:

Power -> Power Planning -> Add Rings



Make sure your power and ground net names **VDD! GND!** appear in the Net(s) window (you can select the net names with the browse button beside) select and add the **Possible Nets** to **Chosen Nets**. Click **OK**

Set the Width to **0.2**, the Spacing to **0.2,** and Offset to **0.78**.

Click **OK**

Step 4: Placement:

i) Standard Cell placement:

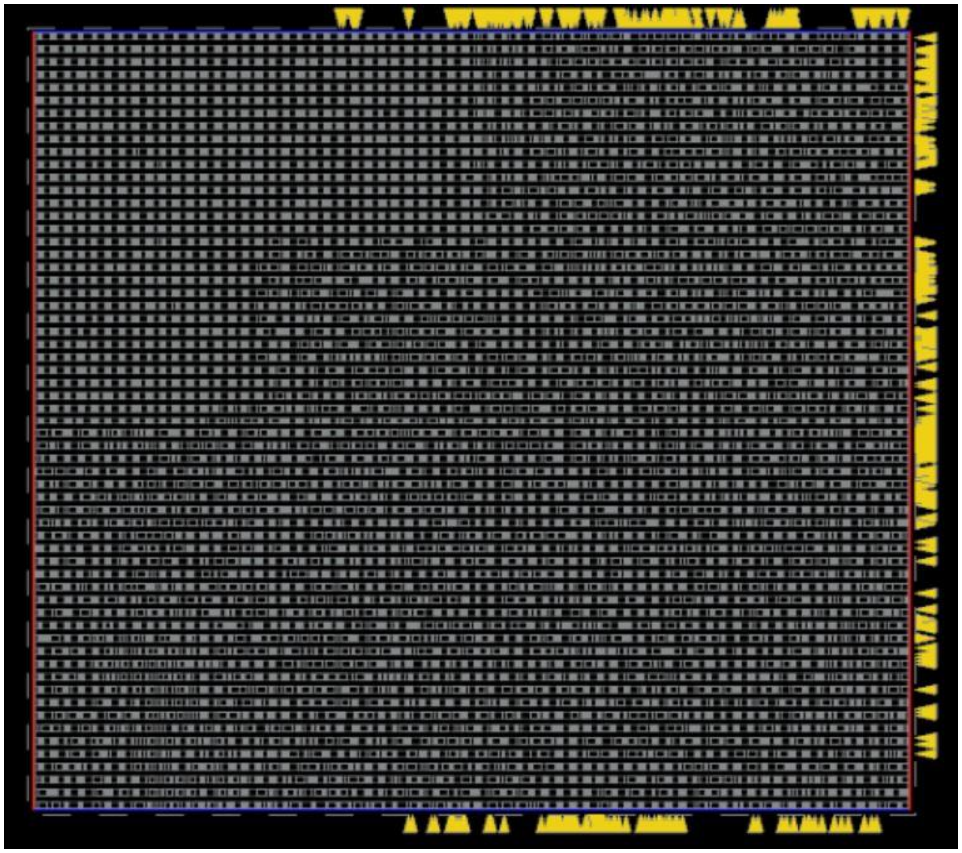
Place -> Place Standard Cell

Click on **Mode.**

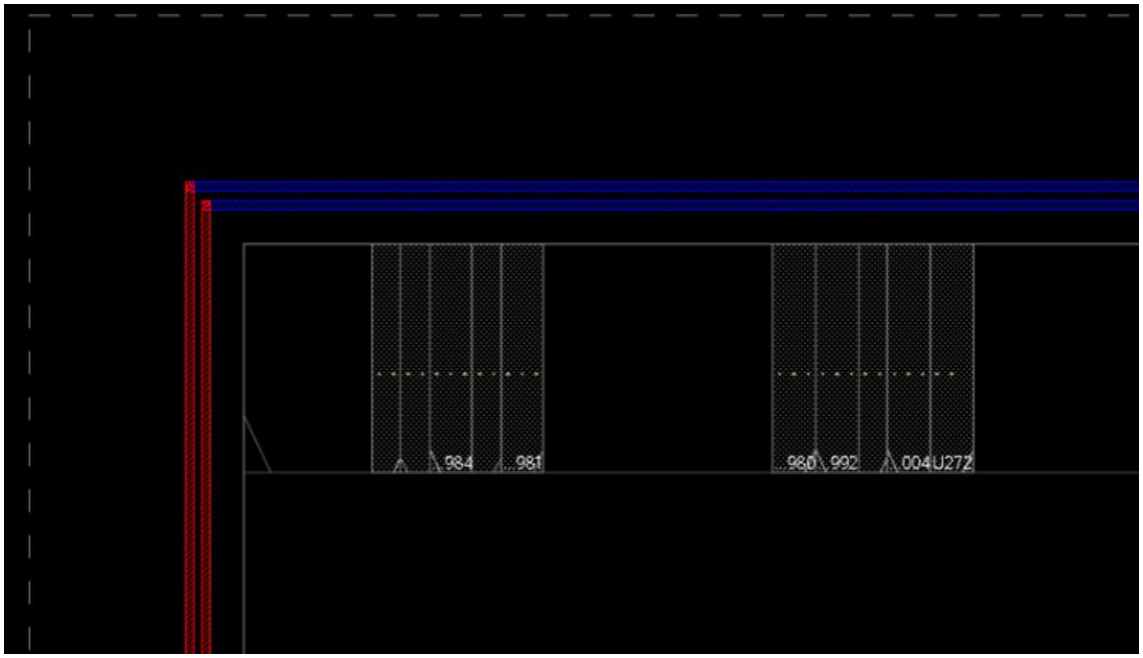
In **Congestion Effort ->** Select **Medium**

Check only **Place IO Pins**

Click **OK** (twice)



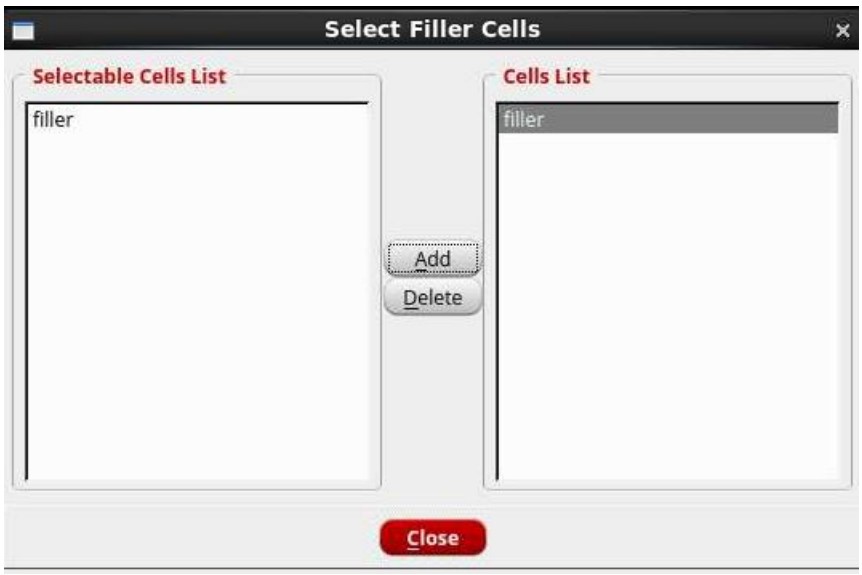
Zoom in (right click and drag the area you want to zoom in) to check if all the pins are in straight line.



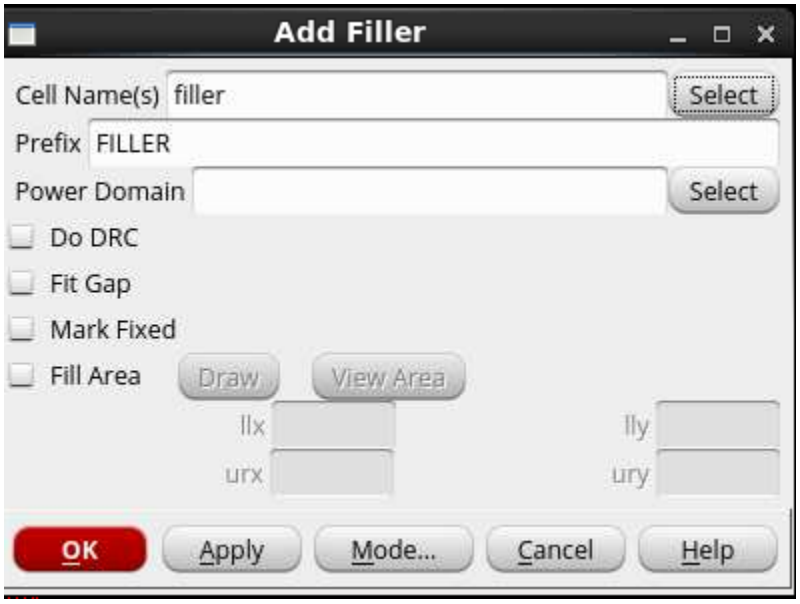
ii) Filler Placement:

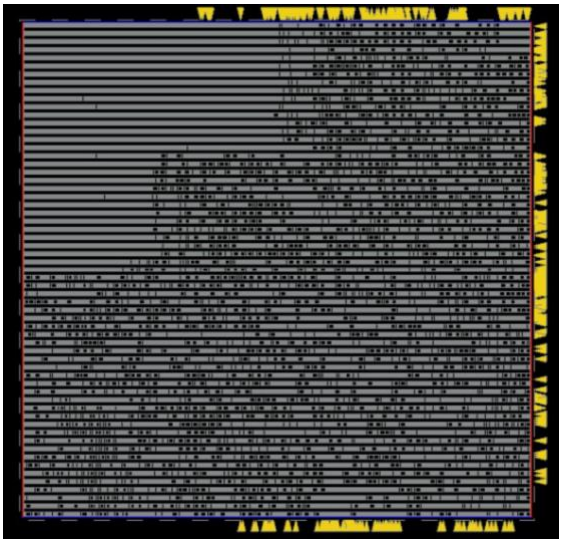
Place -> Physical Cell -> Add Filler

Click on **Select** (the one in front of Cell Name), Click on **filler** (under **Cell List**) and click **Add.** Click **Close.**

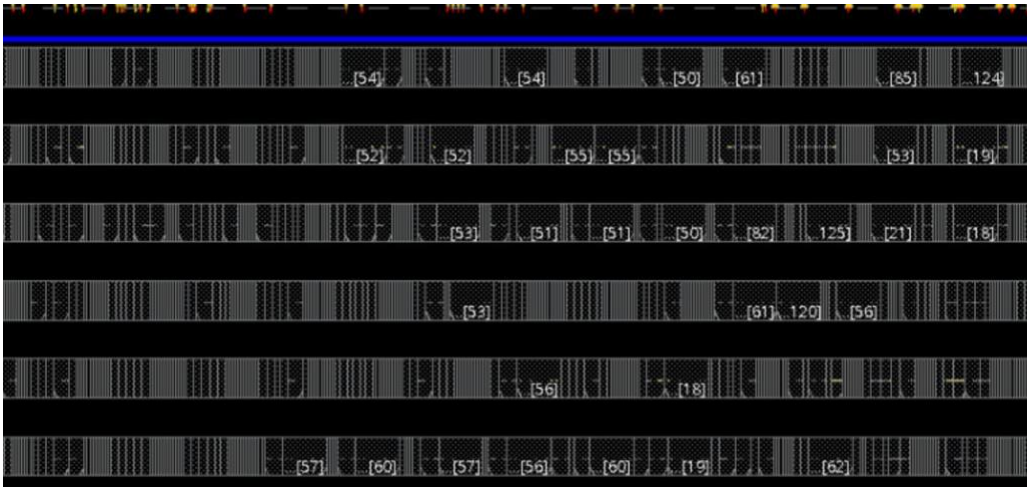


Click **OK**.





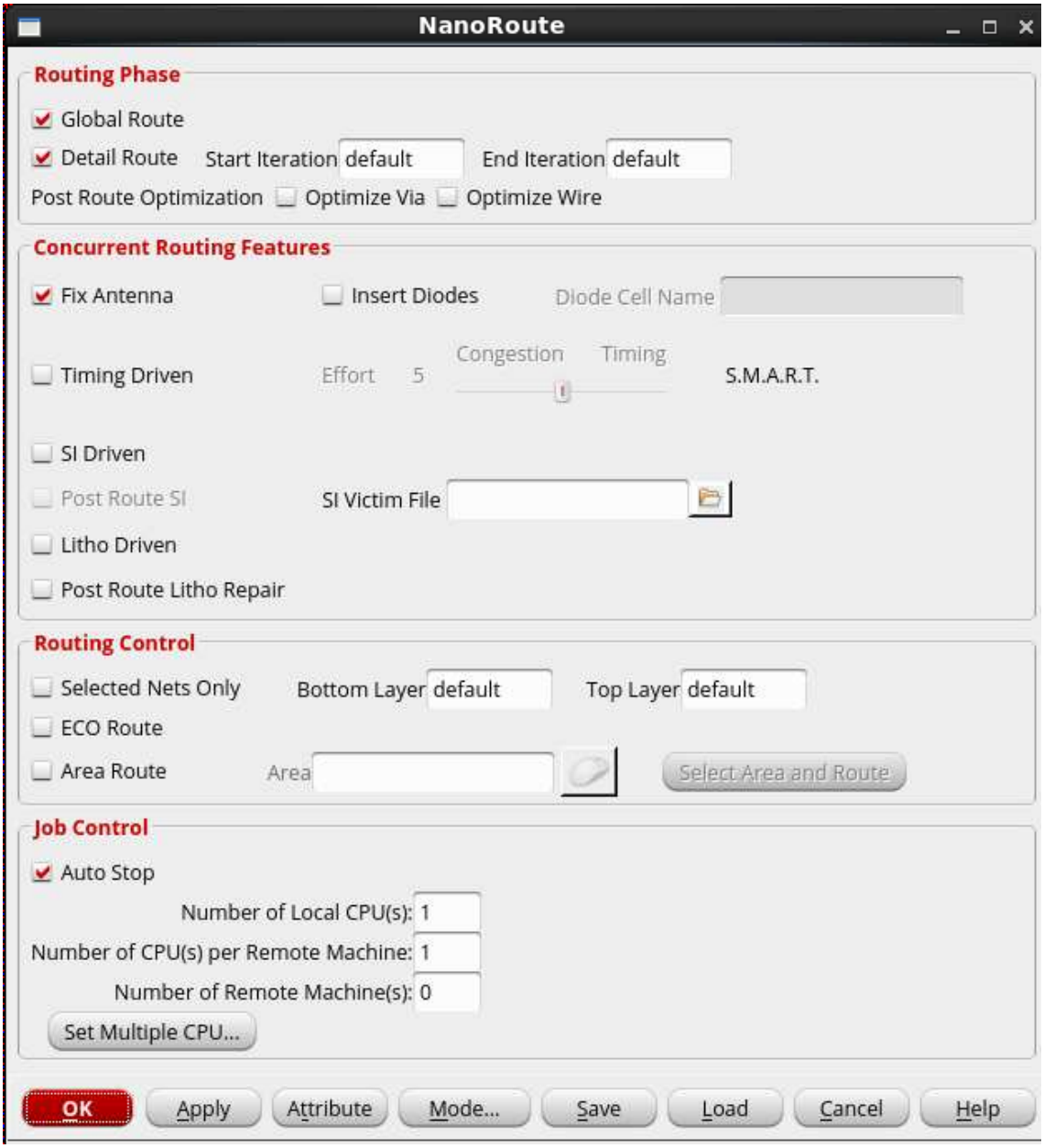
Zoom in to check if each and every blank space in the core area is filled with the filler



The placement step is completed, your design is ready for routing.

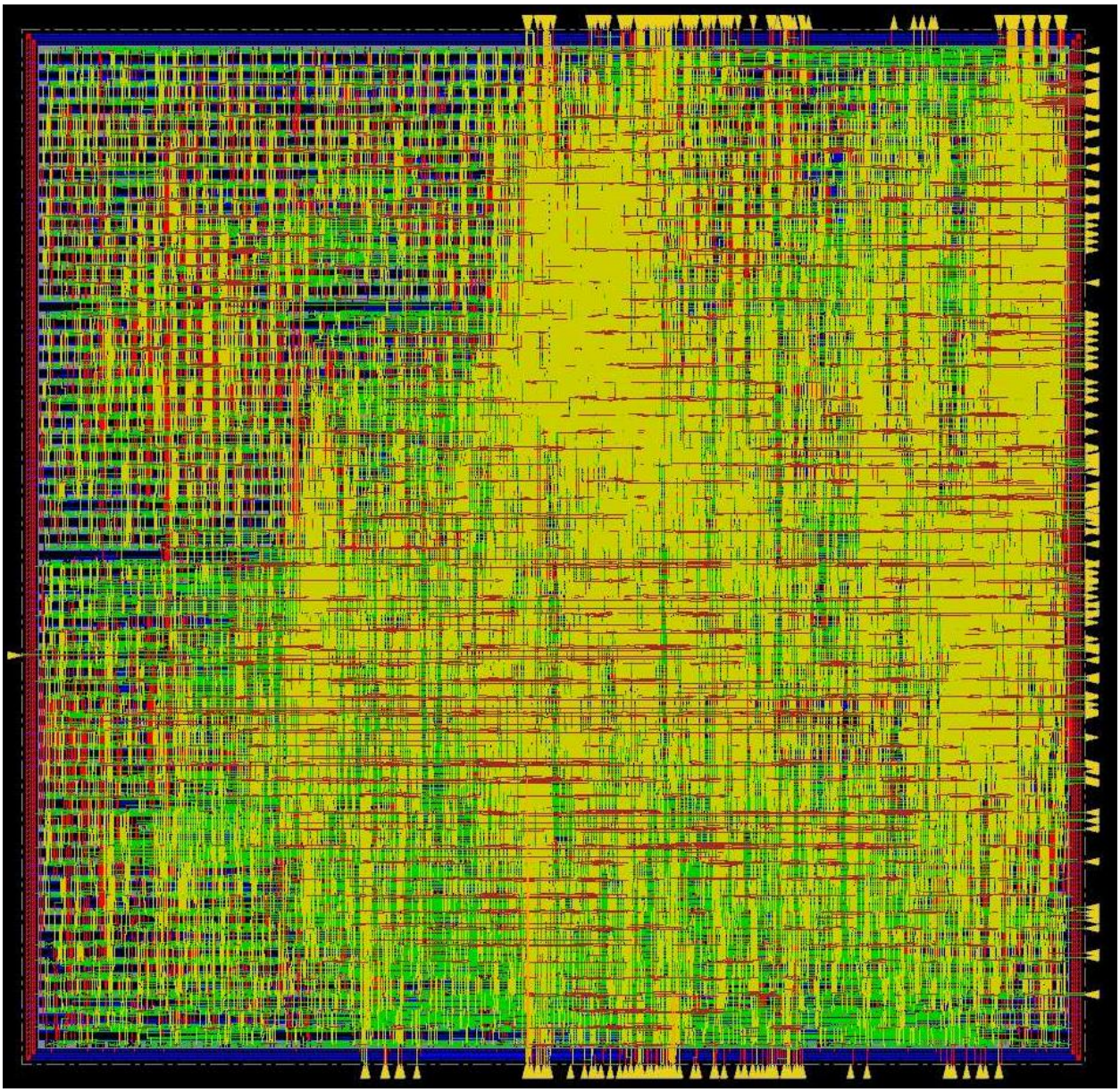
Step 5: Routing:

Route -> NanoRoute -> Route



Click **OK**

This step can take anywhere between **1 to 5 minutes** depending on the complexity of your design.

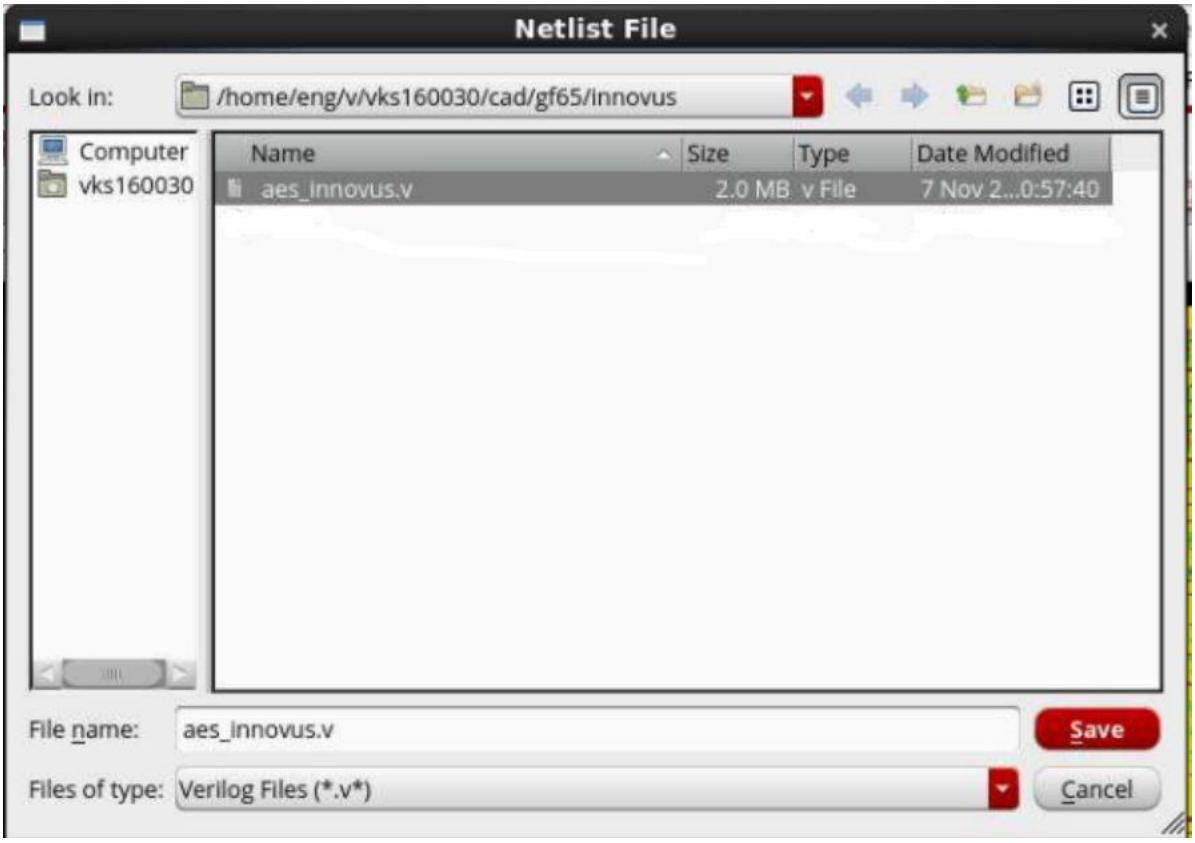


Routing is done now.

Next steps is to save the design.

- **Saving Schematic:**

  File -> Save -> Netlist



Click **Save**

- **Saving Layout**

  File -> Save -> DEF

Remember to check the boxes shown above in the picture, and change the

Output DEF Version to **5.6**

Click OK

Importing Schematic and Layout into Cadence Virtuoso

Open Virtuoso in a new terminal

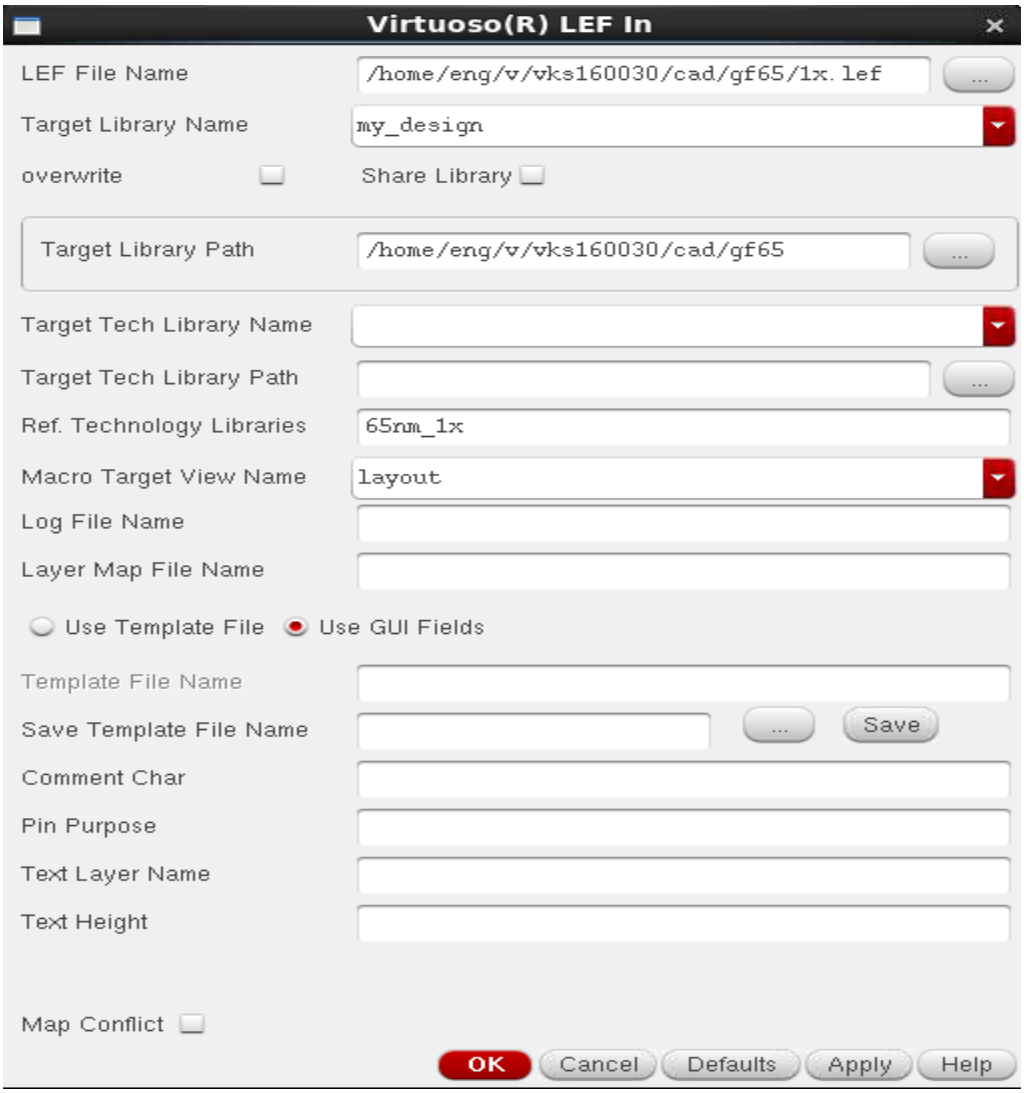
```
cd cad/gf65
. /proj/cad/startup/profile.ee7325
Virtuoso&
```

- Create a new library to import your new design (https://personal.utdallas.edu/~Xiangyu.Xu/gf65/#2-create-a-design-library)

  Remove/ delete the files (cdsinfo.tag and data.tm) from your new library.

- **Importing Layout:**
  - **File -> Import -> LEF**

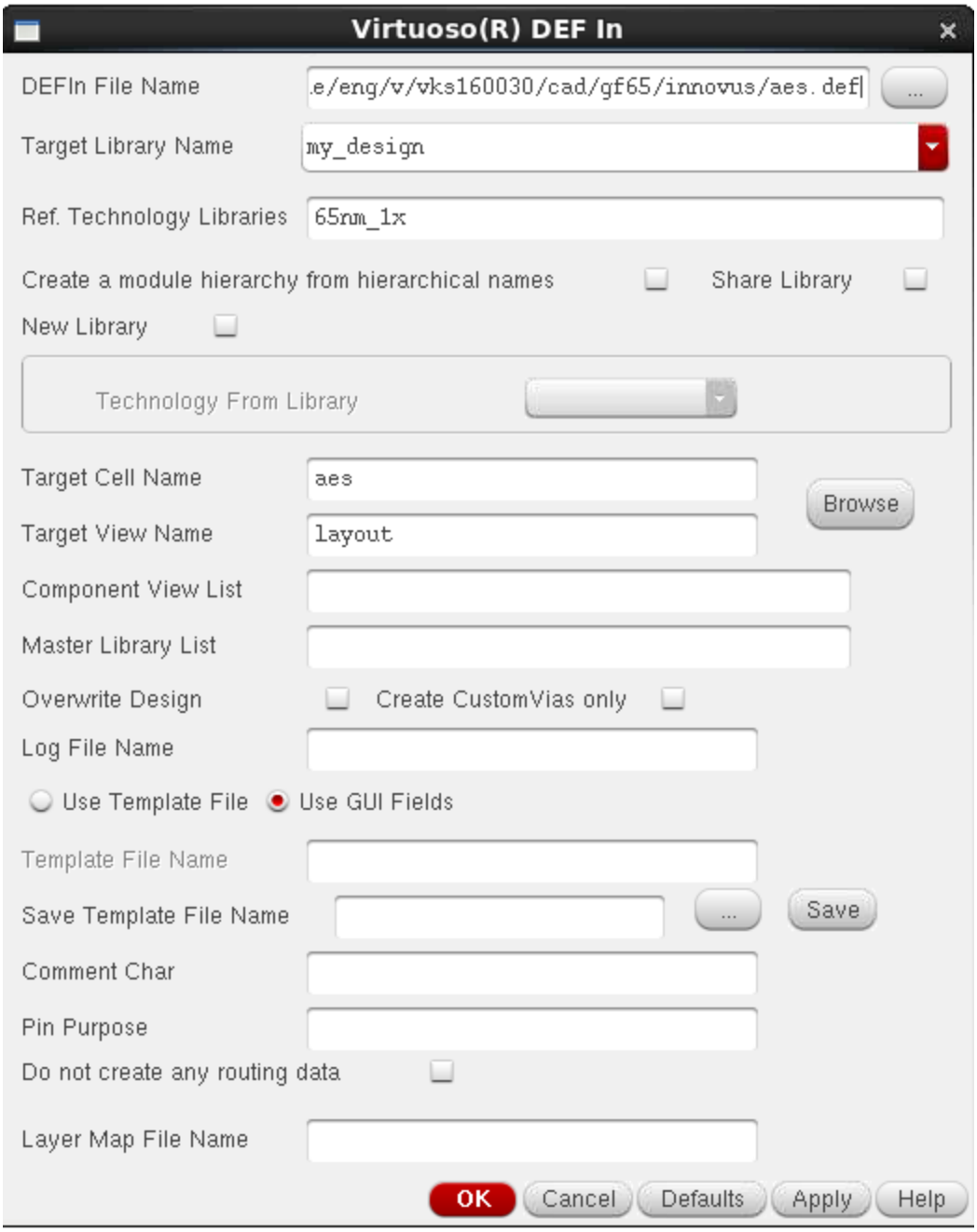
  LEF File Name: Path of your LEF file generated earlier.
  Target Library Name: new library name (created to import your design)
  Target Library Path: Path of your new library
  Reference Technology Libraries: Name of your Standard Cell Library (the library which comprises all your standard cells with all views: Schematic, Layout, Abstract, Symbol)
  Macro Target View Name: layout



Click OK (Ignore the 7 warnings, but if you get errors, you are doing something wrong)

- **File -> Import -> DEF**

DEFIn File Name: Path of your DEF file generated from Innovus.
Target Library Name: new library name (created to import your design)
Reference Technology Libraries: Name of your Standard Cell Library (the library which comprises all your standard cells with all views: Schematic, Layout, Abstract, Symbol)
Target Cell Name: name of the top module of your design
Target View Name: layout
Click OK (you should not get any warnings or errors)



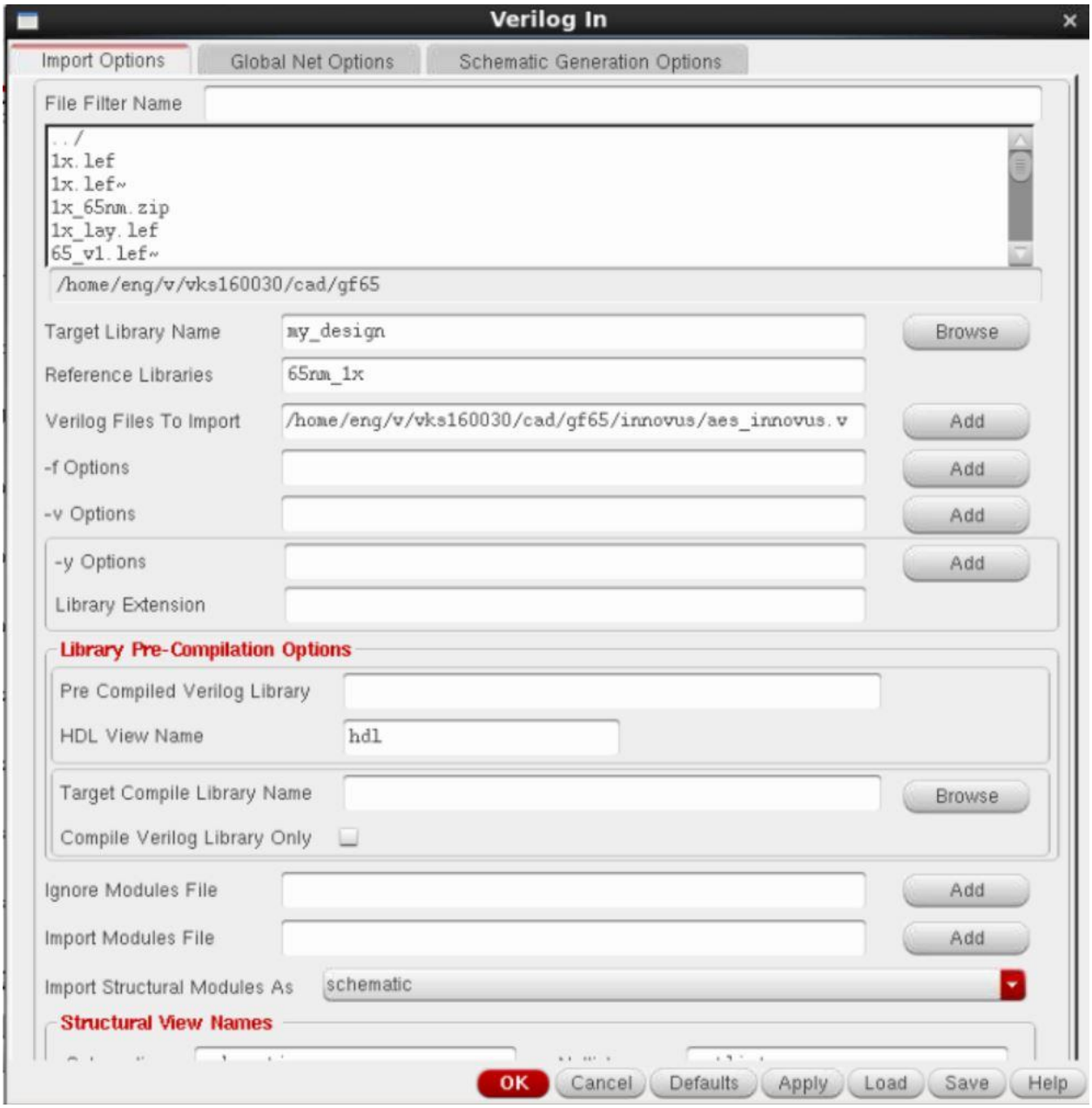
- ## Importing Schematic

  File -> Import -> Verilog

  Target Library Name: new library name (created to import your design)

  Reference Libraries: Name of your Standard Cell Library (the library which comprises all your standard cells with all views: Schematic, Layout, Abstract, Symbol)

Verilog Files to Import: Path of your .v (netlist) file generated from Innovus.



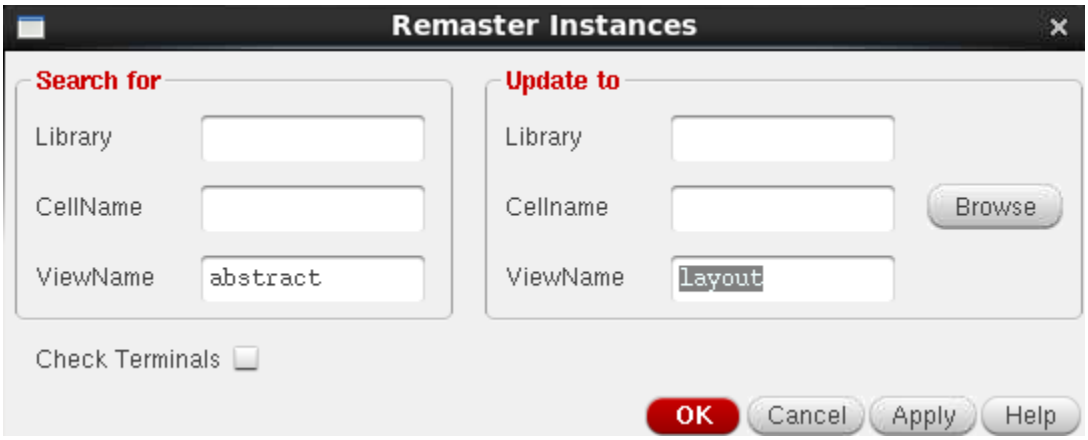
Click OK (Importing schematic can take up to 5 mins)

- Check your new library, it should have all your standard cell with symbol and layout views. Your complete design should have symbol, schematic and layout views.

Note: Copy all your schematic view from your standard cell library to new library, if you don't do this, LVS check won't start

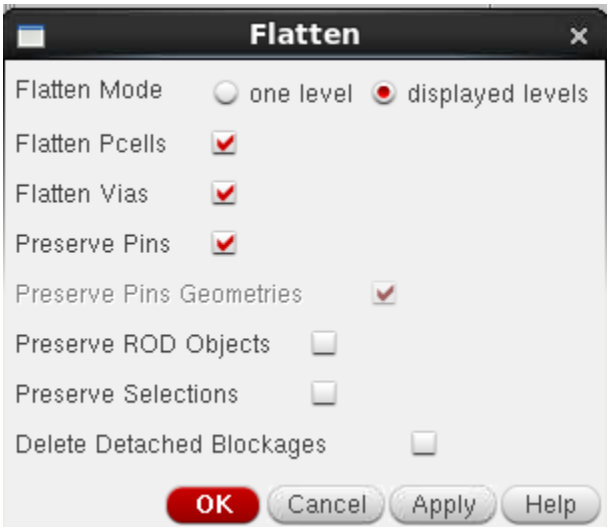
- After you open the layout of your design

  Tools -> Remaster Instances



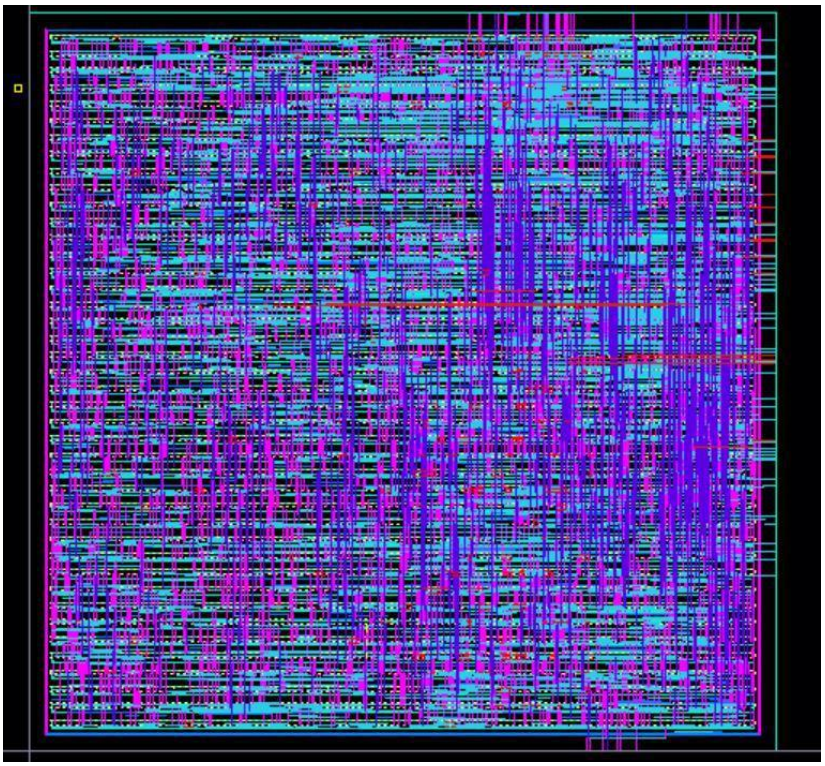
  Click OK

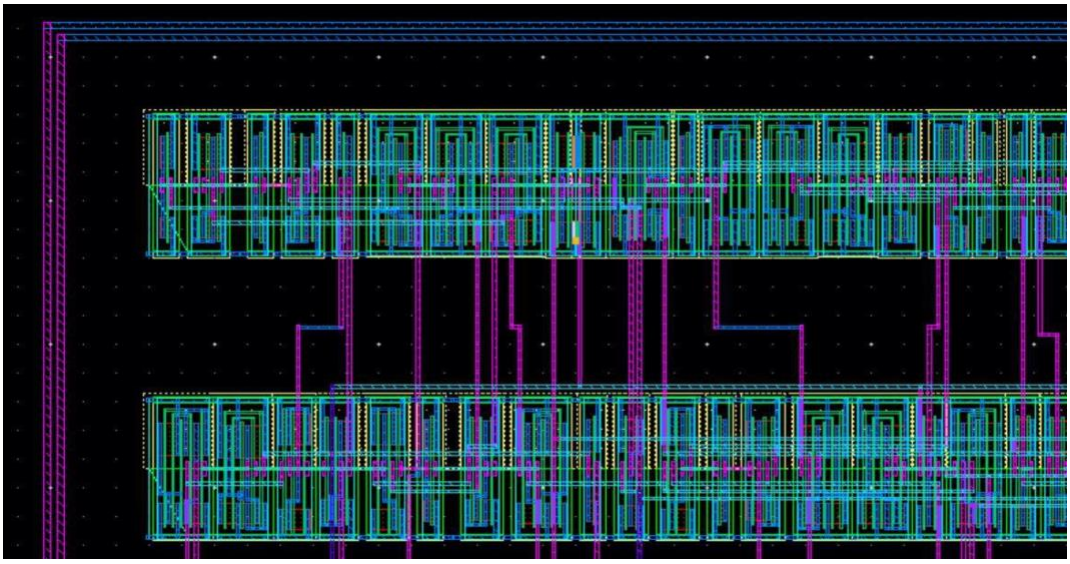
- **Edit -> Hierarchy -> Flatten**



  Click Ok

- You should now be able to see your complete design as shown in the pictures below:





- Perform DRC, LVS and PEX.

- After you get a DRC and LVS clean design, move to the PrimeTime tutorial given on the webpage**.**

Steps to do in order to pass LVS:

1) **Make sure all the lower-case nets names in your verilog file are replaced by any other net name. For example: Your ".v" file might have a net n100 and also N100. You can replace n100 by m100. This has to be done because Calibre is not case sensitive. It thinks n100 and N100 are same nets, but they aren't.**

2) **If you have pin labels and pins layers, delete them all (all input, output, VDD, GND). Innovus marks them all as nets while routing, and Calibre throws an error if you have extra pin or label.**

3) **Add labels to your final design I/O pins (make sure to select the correct metal layer while adding labels to your I/O)**

4) **Extend your VDD and GND metal layer to the VDD and GND rings respectively, do this to all your rows. Now, add labels "vdd!" and "gnd!" to your rings.**

After making these changes you should be able to get a clean LVS!!