EECT/ CE 6325 VLSI Design
Fall 2022

PROJECT #3: INVERTER DESIGN AND LAYOUT
Due: **Wed. Oct 5 at 11:30 am**

Project Introduction

For this project you will be using the GF65nm process and Cadence Design tools to design, layout and characterize an inverter. This project will get you familiar with Cadence and also with the simulation of the layouts that you create.

Project Description/Requirements

1) Review the inverter layout tutorial: GF65 Environment Setup and Inverter Tutorial
2) The input and output pin labels must be capitalized in both schematic view and layout view: IN, OUT
3) The power and ground pin labels in layout ~~should be VDD! and GND!~~
4) The length of the channel (L) for this project must be ***70nm*** (not 60nm).
5) Simulate the inverter: HSPICE Tutorial
6) You will be designing a symmetrical inverter with equal t_{LH} and t_{HL} (measured from 50% to 50%). (Delay **difference between** t_{LH} and t_{HL} must be within 5ps.)
7) The input slew rate is 60ps (the slew rate, for this problem, is defined as the time for the input to go from low (0.1* Vdd) to high (0.9* Vdd) and vice versa). Use a piecewise linear input waveform or, if you dare, a pulse waveform accordingly.
8) The load capacitance is 70 fF.
9) VDD is 1.2V & GND is 0V.
10) The poly gates for the two transistors must be vertically aligned.
11) ***DESIGN OBJECTIVE:*** Minimize the bounding box area (H*W) of your inverter layout while minimizing the energy-delay product (EDP).

Report Layout

1) A cover page containing:
   - Student names, NetID and project titles
   - Clearly state your energy (E), delay (D), EDP, and the area (widths & lengths are measured from highest Metal1 layer to the lowest Metal1 layer) on the front.
2) Soft copy of the report should include:
   - Spice test setup file (Don't include any spice netlist)
   - Report containing detailed explanation on how you achieved the minimum EDP
   - Waveforms showing tLH and tHL times measured with any waveform viewer. **NO BLACK BACKGROUND WAVE FORMS** or points will be deducted.
   - Inverter layout with rulers (**from cadence with only white background**)
   - Extracted Spice Netlist
3) Upload the zipped folder containing your Inverter layout, schematic on eLearning

Grading Breakdown

50% Functional correctness of the inverter; delay & other specifications met
25% Inverter EDP and area
25% Report clarity and completeness