EECT/CE 6325 VLSI Design

Fall 2022

PROJECT #1: Verilog/VHDL

Due: **Wed. September 7 (11:30 am)**

Project Introduction

In this project, students are required to design an arbitrary digital design of their choice using Verilog or VHDL. The only restriction is: the design must use flip-flops. Examples include FIR and IIR filters, state machines, etc. You can pick a design of your choice as long the above restrictions are met.

After project 2 your design needs to use 3000 cells or more. However, at this stage you will not know the cell count. So, it may be wise to choose a scalable design, one that is easy to extend, in case it is too small after the synthesis project.

No credit will be given for any design copied from the internet or from other sources.

Project Description/Requirements

1) We want you to code your digital design in Behavioral Verilog/VHDL.
2) One test bench and at least one module for your design.
3) Clear comments to your code including comments in your test bench that make it clear how you are testing your module(s).

Report Layout

1) A cover page containing names (max group of three), NetID and project title.
2) A paragraph on the general description of your design.
3) A block diagram of your design. Please label all inputs and outputs.
4) A block diagram of how the module(s) and test bench are connected.
5) A copy of your simulation waveform results with enough comments to make it clear that your design functions correctly.
6) A soft copy of your code is required, upload the document on eLearning. (**Projects** -> **Project 1** -> **Verilog / VHDL**).
7) A soft copy of the project report (**Projects** -> **Project 1** -> **Project 1 Report**). Everyone must submit the report even if you are working in a group

Project Flow and Tutorial Links

1) You will setup NX NoMachine client and be familiar with the environment.
   - Instructions are given in **VPN and NoMachine Setup** (**Projects** folder on eLearning)

2) You will simulate your Verilog code.
   - http://www.utdallas.edu/~xiangyu.xu/verilog