EECT/CE 6325 VLSI Design
Fall 2022

PROJECT #2: SYNOPSYS PROJECT
Due: **Wed. September 21, 11:30 am**

Project Introduction

For this project you will use Synopsys Design Vision to generate a mapped netlist based on the library of cells that we have provided. After running Design Vision, you will have a better idea of the complexity of your design as well as an exact cell count. This project will also give you a good idea of what cells you will be creating for your own library.

Project Description/Requirements

1) Create a working directory in your home directory, type the following command in the terminal: `source /proj/ndl/home/vks160030/GF65_6325/setup-GF65-cad`
2) Convert provided .lib file to .db file: (http://www.utdallas.edu/~xiangyu.xu/lc)
   Logic Synthesis with Synopsys Design Vision: (https://personal.utdallas.edu/~xxx110230/dv/)
3) From the tutorial, you will read your Verilog code and create a netlist based on the library that we have provided.
4) Print out the report showing the total number of cells used for your design. The report will be generated by Synopsys Design Vision.
5) Concatenate the mapped Verilog that you created with the ***header.v*** file that we have provided.
6) Test the code with any Verilog simulator and obtain graphical waves of the mapped Verilog.
7) Compare with your behavioral Verilog and verify that both function the same.

NOTE: **You are required to have at least 3000 cells for your design (however, if your Verilog design is very intricate/complex, you can seek approval for less than 3000 cells).**

Report Layout

1. A cover page containing name, student number, and project title.
2. Report should not be more than 20 pages (including the code).
3. New/scaled-up Verilog (or VHDL) code along with testbench.
4. Put behavioral code waveform and mapped code waveform together and prove that the two designs have the same function.
5. Report from Design Vision showing total amount of cells, DO NOT put full generated cell report, you can skip some rows, but AT LEAST ONE DFF unit must be shown.
6. **No waveforms with black background**; points deducted for not following format.
7. Submission of an electronic copy of project report is required

Grading Breakdown

- 50% Mapped (structural) Verilog has the correct functionality
- 25% Report clarity and content
- 25% Design complexity and size