

PROJECT 5

CE 6325.001 VLSI DESIGN

PROJECT: - D FLIP - FLOP

TEAM MEMBERS:

ALEXANDRA EDWINRAJ (NET ID: AXE210023)

HEENISHA REDDY BACHUGUDEM (NET ID: HXR210022)

KANUPRIYA SHARMA (NET ID: KXS220016)

D Flip-flop times:

Times	Passing 1	Passing 0
Tsu_dd	62.4	62.4
Tsu_opt	89.6	89.6
Thold	62.4	62.4
Tclk->Q	96.0	111.3
Td	187.4	200.9

D Flip-flop parameters:

DFF height	7.535
DFF width	10.294
Wn	1um
Wp	2um

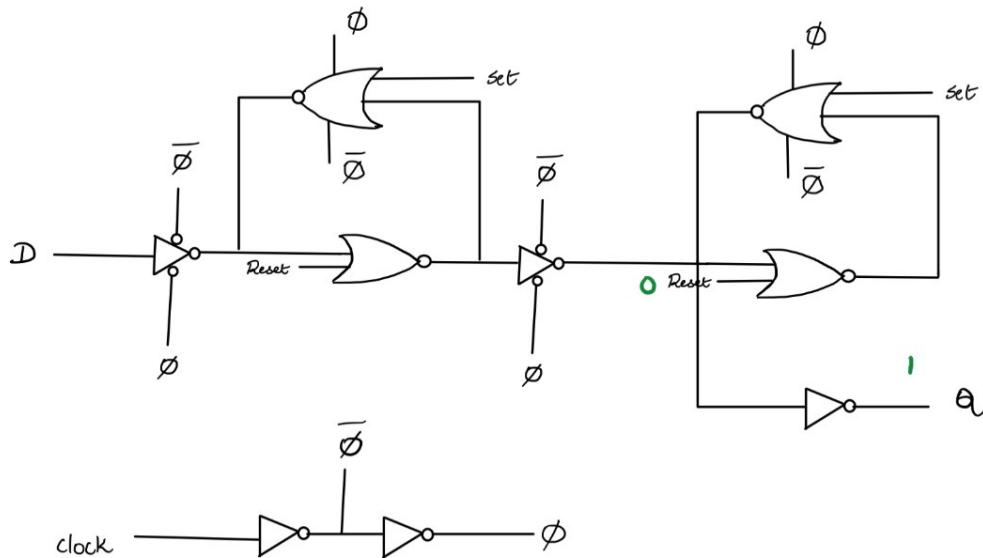
Objective:

- The objective of this project is to design a D flip-flop using Cadence by minimizing the cell width and diffusion breaks.
- To achieve this, the gate-schematic of DFF was converted to transistor level schematic and Euler trail was found.
- The designed DFF has D(data), CLK (active high), R(reset) and S(set) as inputs and Q as output

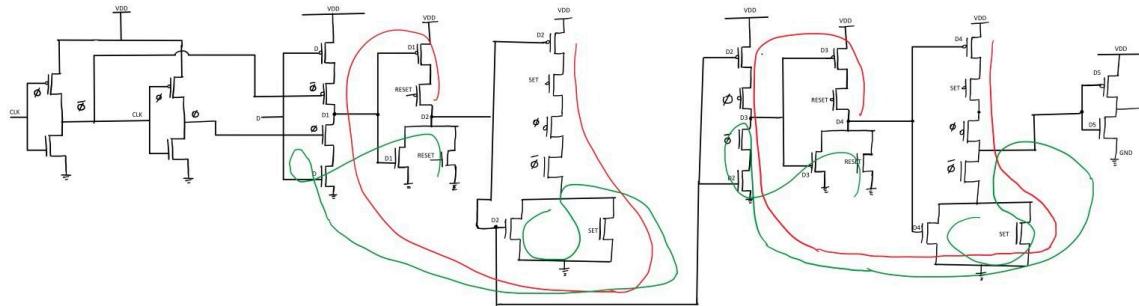
Brief descriptions of D Flip-Flop times:

1. **Tsu_dd** - is the shortest amount of time D must rise or fall before Q can demonstrate valid stable logic.
2. **Tsu_opt** - is the minimum value of Tsu that results in minimum td
3. **Thold** - After capturing the edge, Thold is the time during which D should remain stable and the same, ensuring that Q remains stable and the same
4. **Tclk->Q** - is the time for the Q to show valid logic after capturing edge on clock
5. **Td** - is the delay time for the Q to show stable logic after passing D. It means $td = Tsu-dd + Tclk->q$

D Flip-Flop Gate Level Design:



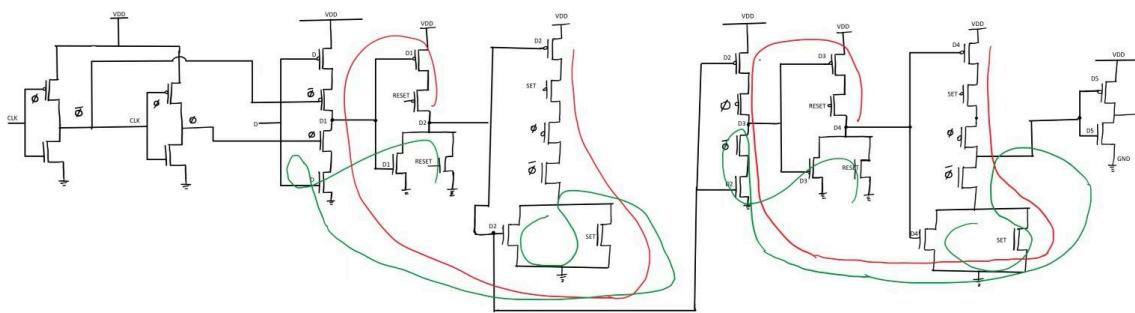
D Flip-Flop Transistor Level design:



Dual Euler Trail:

Euler Path:

Number of diffusion breaks = 3

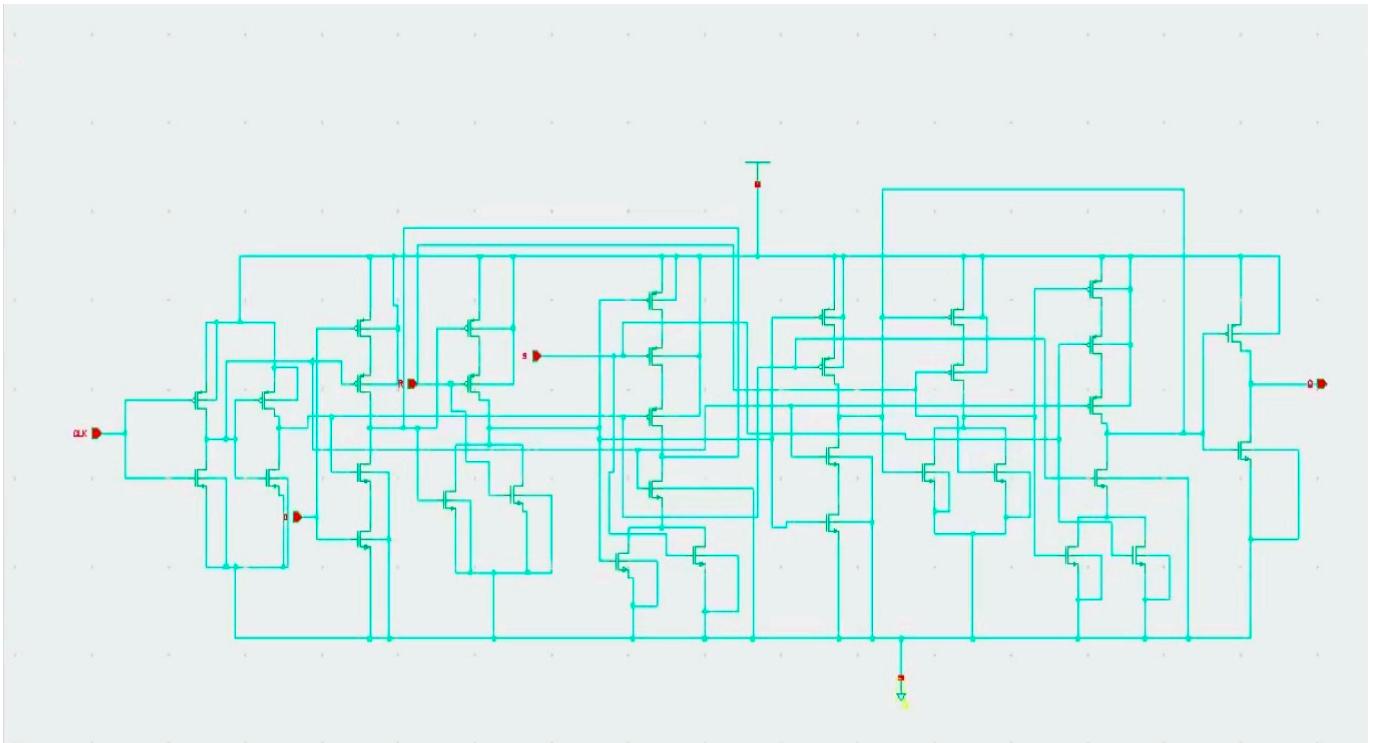
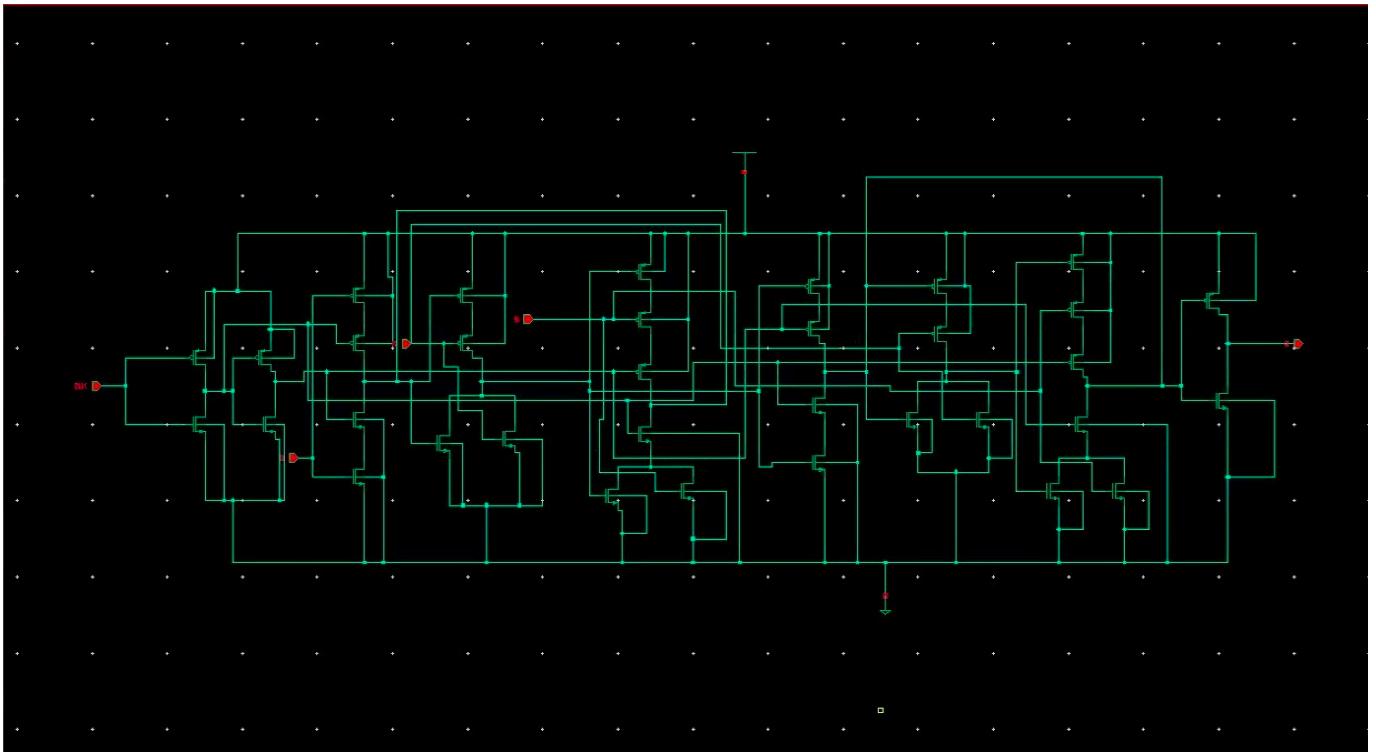


$$\text{Euler Trail : } \overbrace{\bar{\phi} \phi}^{\text{uk}} // D_2 S \left(\begin{matrix} \bar{\phi} \\ \phi \end{matrix} \right) D D_1 R // D_1 S \left(\begin{matrix} \phi \\ \bar{\phi} \end{matrix} \right) D_2 D_2 R // \text{out}$$

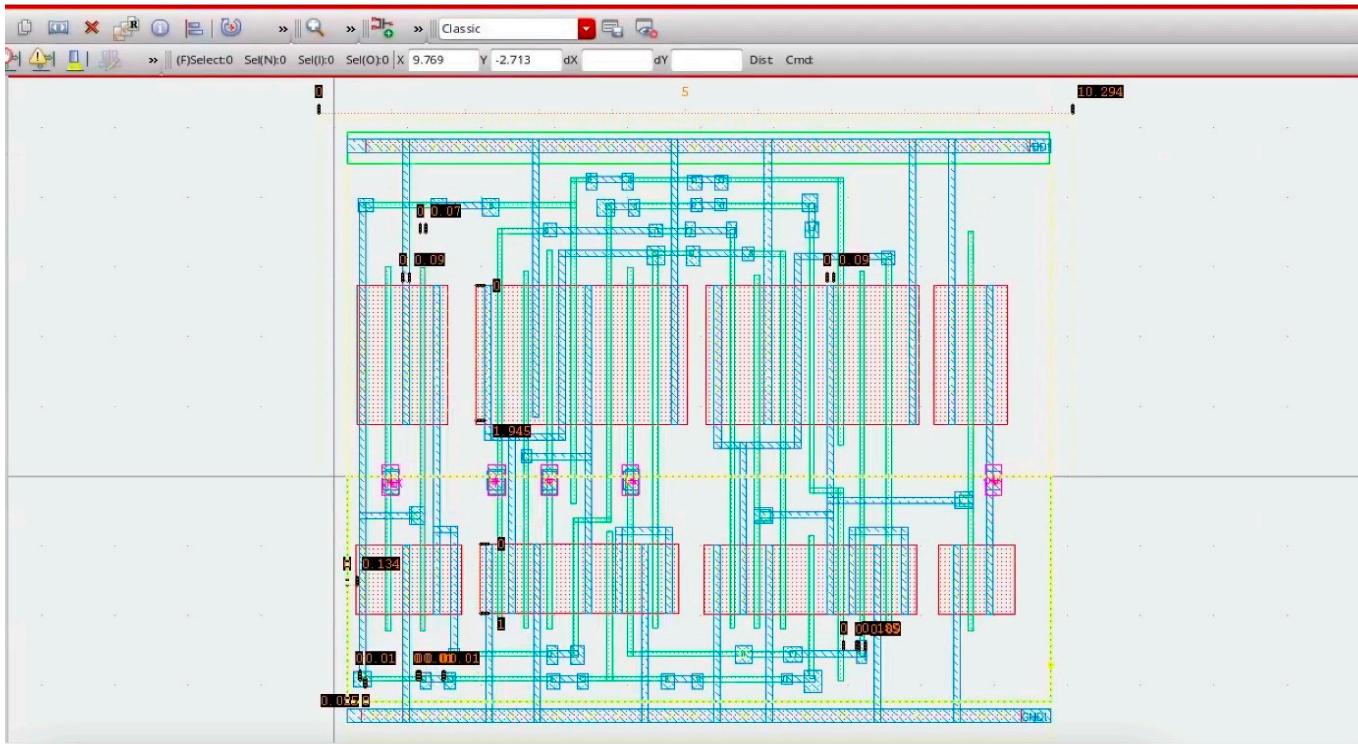
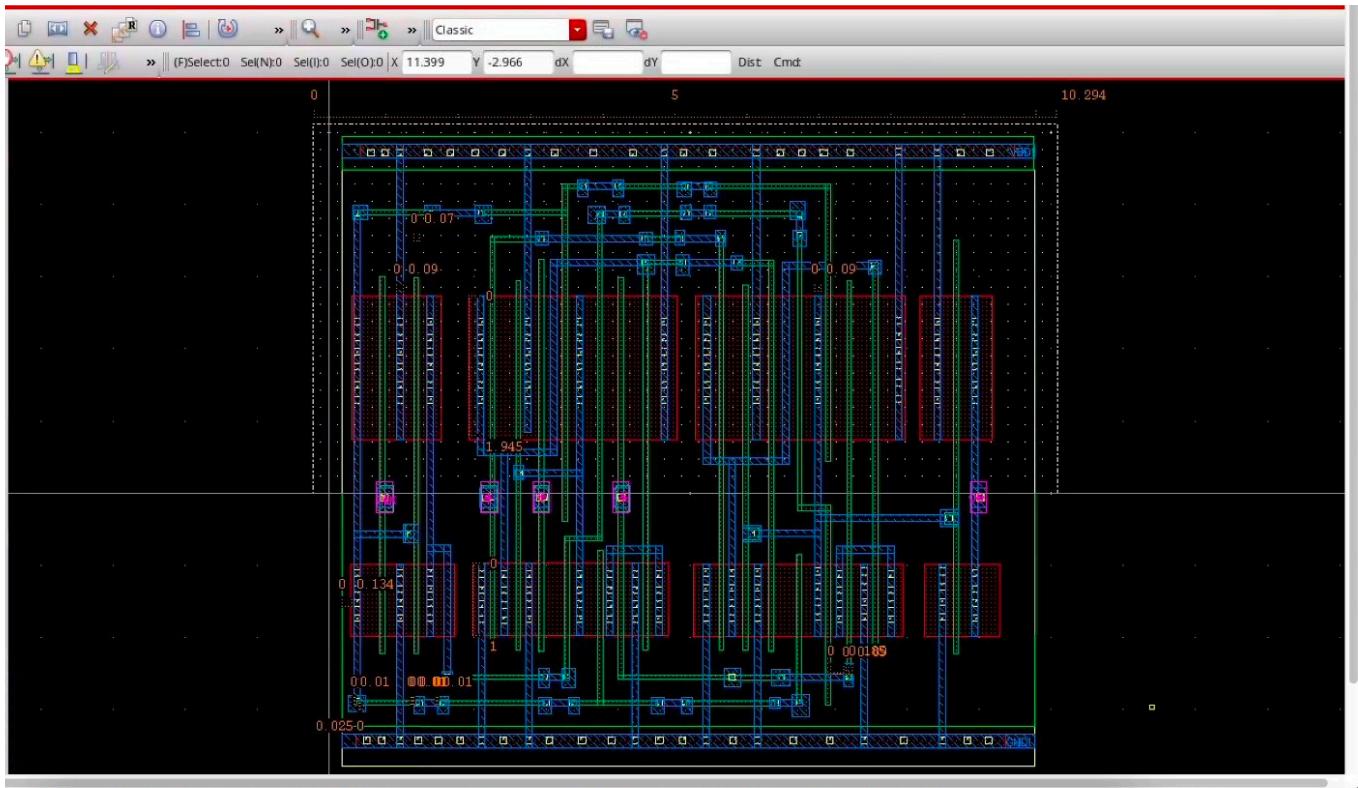
- The above circuit diagram is a D-flip flop discussed in class.
- Using the logic to draw the schematic and find the Euler path to find out the diffusion breaks required.
- Using the schematic, design the layout of the D flip flop

In Cadence

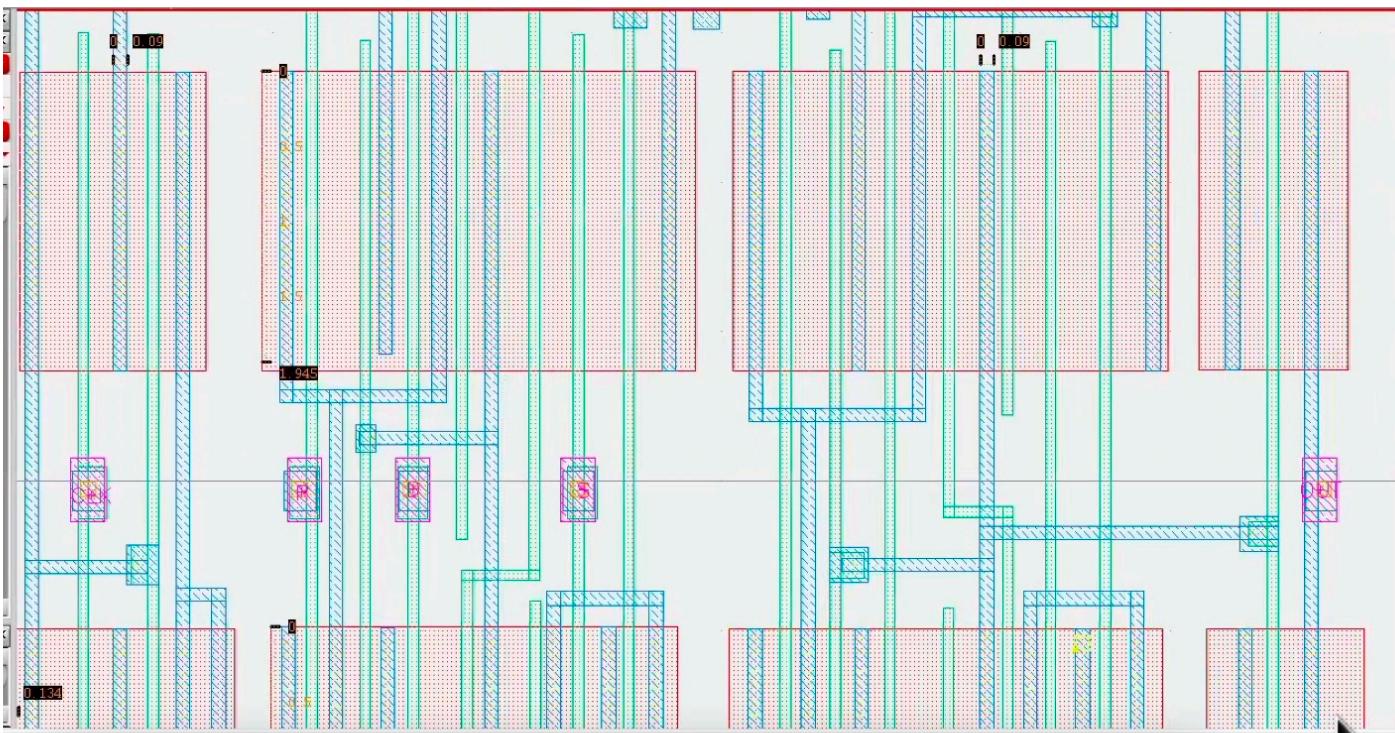
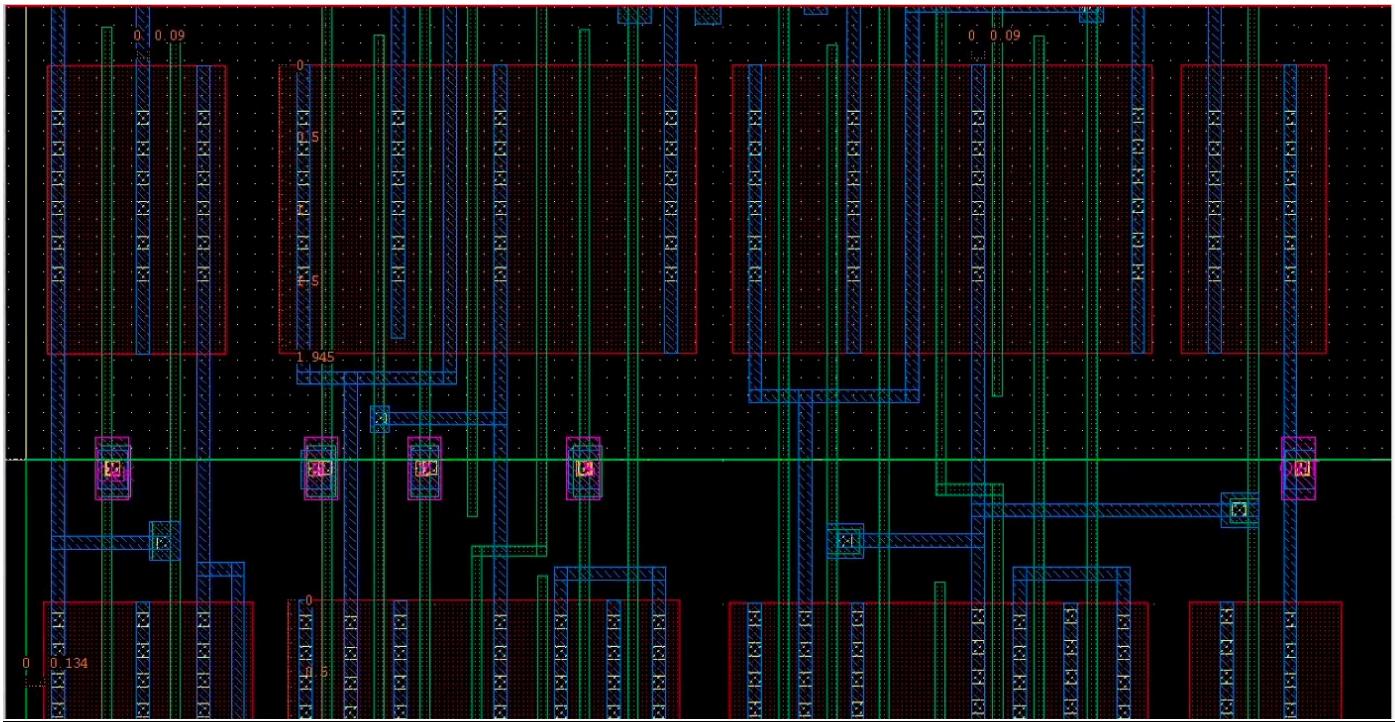
Schematic:



Layout:



Pin Placement:



Deriving DET:

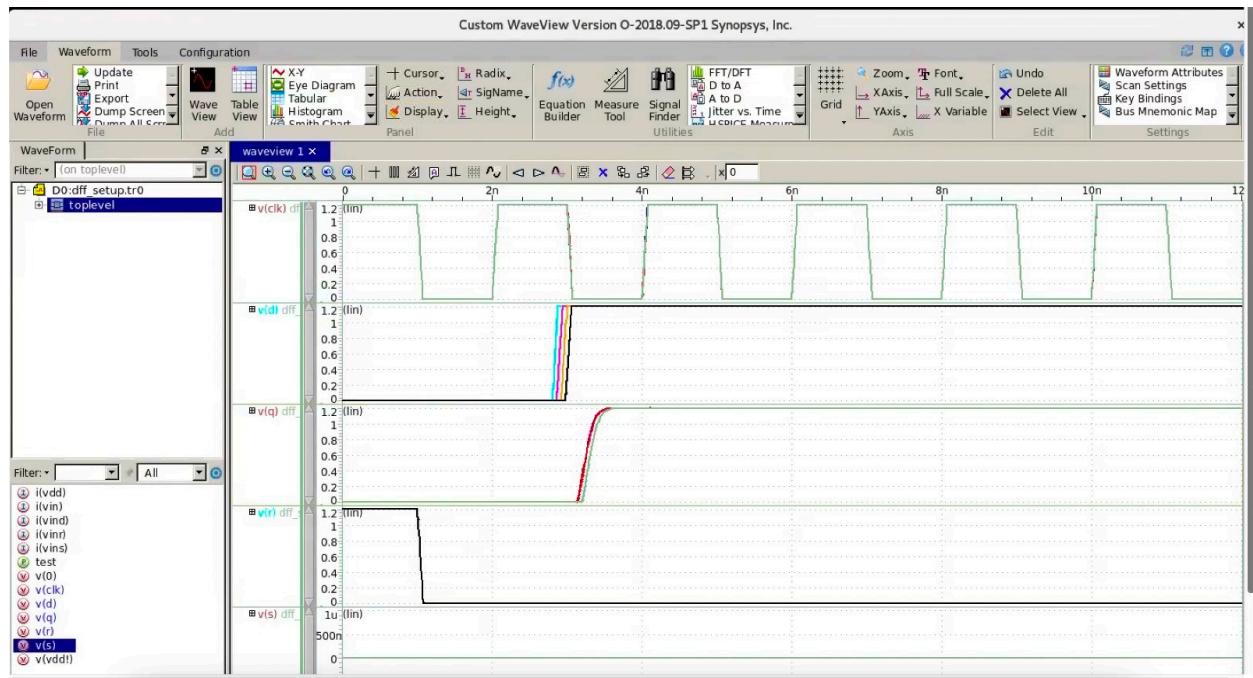
- Schematics can divide into 4 parts, 1st one clock, followed by latch 1 and latch 2 and output.
- Latch 1 and latch 2 has two separate dual-Euler trail (DET) and output also has separate DET as well as clock. With this logic we get 3 diffusion breaks. Clock we kept in between latch 1 and latch 2 to reduce the length of the metal

Calculating times for D-FF

- Times can be calculating by passing logics for D at different time intervals using ‘sweep’ in HSPICE.
- ‘.measure’ is used to calculate time at which Q is changed with respect to edge of the clock.

Waveform and simulation:

Passing 1:

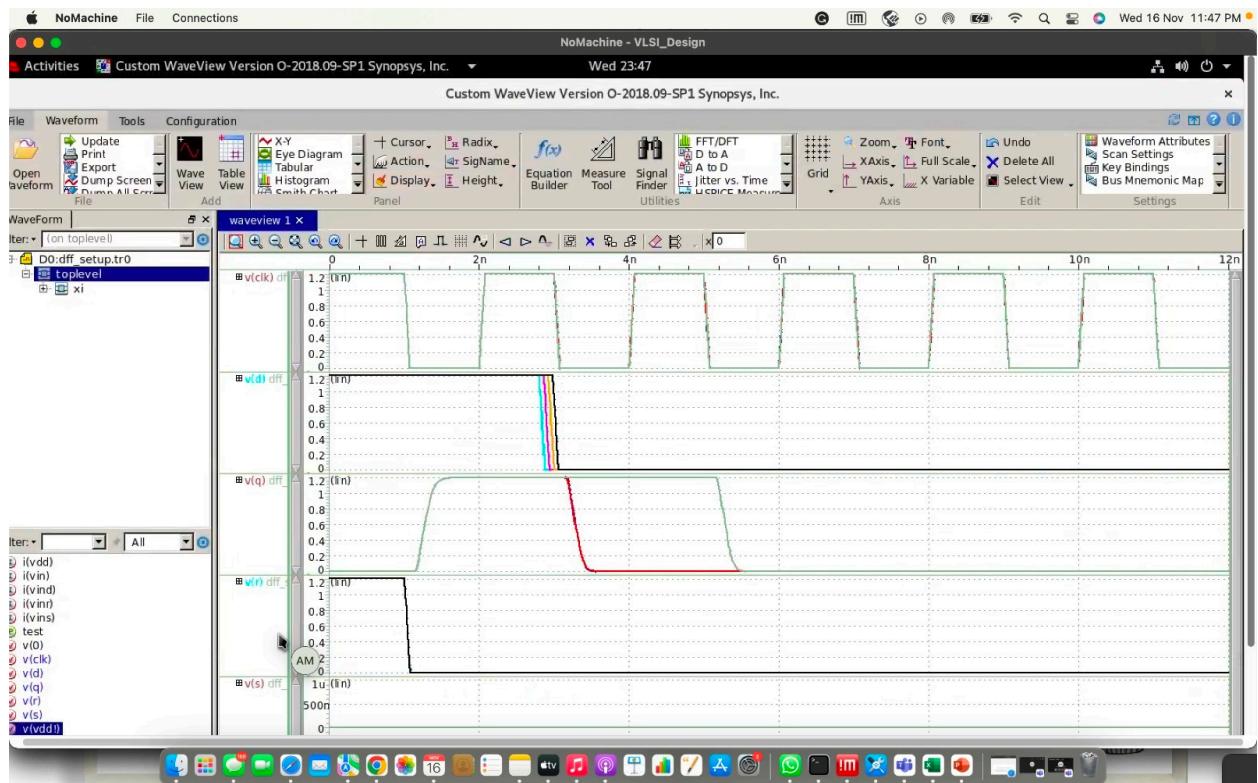


D_ff mt0 file:

test	tsu temper	tclk_q alter#	delay
2.800e-09	1.975e-10 25.0000	2.115e-10 1	4.090e-10
2.860e-09	1.375e-10 25.0000	2.118e-10 1	3.493e-10
2.920e-09	7.750e-11 25.0000	2.153e-10 1	2.928e-10
2.980e-09	1.750e-11 25.0000	2.711e-10 1	2.886e-10

- **Setup time - Tsu =** $1.975\text{e-}10$ which is equal to 89.6ps with respect to D
- **Tclk->q=** $2.115\text{e-}10$ which is equal to 96.0 ps
- **Delay time – Td =** 185.6ps ($4.090\text{e-}10$) ($\text{Tsu} + \text{Tclk->q} = 185.6 * 10^{-6}$)
- **Tsu-dd=** 62.4 ps
- **Tsu-opt=Tsu=** 89.6ps
- **T hold for passing 1 =** Tsu-dd of passing 0 = 62.4 ps

Passing 0:

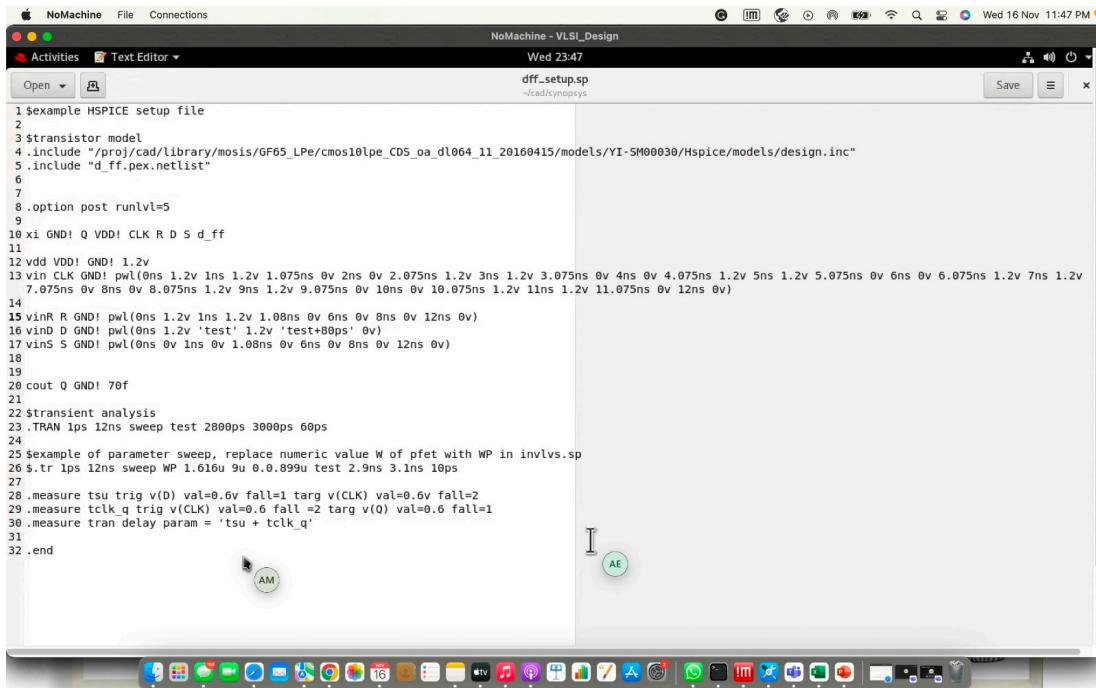


D ff mt0 file :

test	tsu	tclk_q	delay
2.800e-09	temper 1.975e-10 25.0000	alter# 2.452e-10 1	4.427e-10
2.860e-09	1.375e-10 25.0000	2.451e-10 1	3.826e-10
2.920e-09	7.750e-11 25.0000	2.450e-10 1	3.225e-10
2.980e-09	1.750e-11 25.0000	2.245e-09 1	2.263e-09

- **Setup time - Tsu = $1.975\text{e-}10$** which is equal to 89.6ps with respect to D
- **Tclk->q= $2.452\text{e-}10$** which is equal to 111.3 ps
- **Delay time – Td = 200.1ps ($4.427\text{e-}10$)** ($\text{Tsu} + \text{Tclk->q} = 200.1 \times 10^{-6}$)
- **Tsu-dd= 62.4 ps**
- **Tsu-opt=Tsu= 89.6ps**
- **T hold for passing 0 = Tsu-dd of passing 1 = 62.4 ps**

HSPICE Test setup file for passing 0:

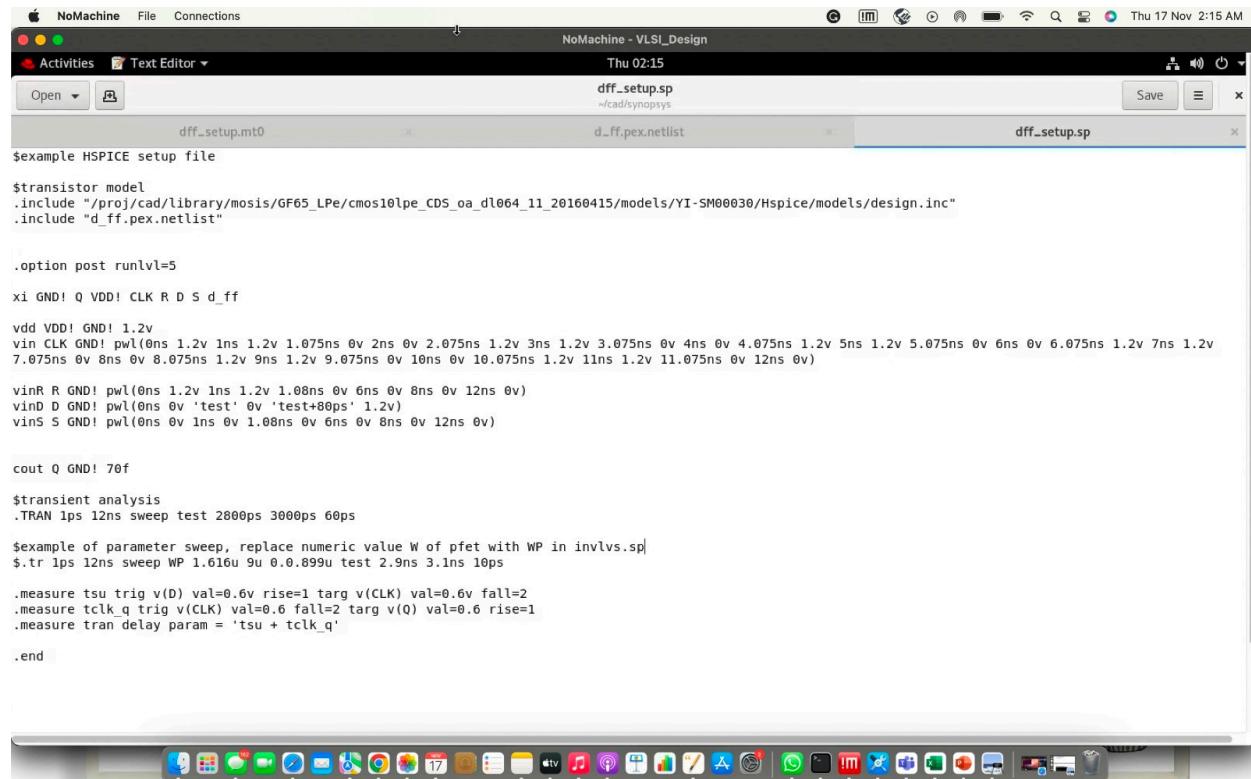


```

1 $example HSPICE setup file
2
3 $transistor model
4 .include "/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"
5 .include "d_ff.pex.netlist"
6
7
8 .option post runlvl=5
9
10 xi GND! Q VDD! CLK R D S d_ff
11
12 vdd VDD! GND! 1.2v
13 vin CLK GND! pw1(0ns 1.2v 1ns 1.2v 1.075ns 0v 2ns 0v 2.075ns 1.2v 3ns 1.2v 3.075ns 0v 4ns 0v 4.075ns 1.2v 5ns 1.2v 5.075ns 0v 6ns 0v 6.075ns 1.2v 7ns 1.2v
7.075ns 0v 8ns 0v 8.075ns 1.2v 9ns 1.2v 9.075ns 0v 10ns 0v 10.075ns 1.2v 11ns 1.2v 11.075ns 0v 12ns 0v)
14
15 vinR R GND! pw1(0ns 1.2v 1ns 1.2v 1.08ns 0v 6ns 0v 8ns 0v 12ns 0v)
16 vinD D GND! pw1(0ns 1.2v 'test' 1.2v 'test+80ps' 0v)
17 vinS S GND! pw1(0ns 0v 1ns 0v 1.08ns 0v 6ns 0v 8ns 0v 12ns 0v)
18
19
20 cout Q GND! 70f
21
22 $transient analysis
23 .TRAN 1ps 12ns sweep test 2800ps 3000ps 60ps
24
25 $example of parameter sweep, replace numeric value W of pfet with WP in invlvs.sp
26 $.tr 1ps 12ns sweep WP 1.616u 9u 0.0.899u test 2.9ns 3.1ns 10ps
27
28 .measure tsu trig v(D) val=0.6v fall=1 targ v(CLK) val=0.6v fall=2
29 .measure tclk_q trig v(CLK) val=0.6 fall=2 targ v(Q) val=0.6 rise=1
30 .measure tran delay param = 'tsu + tclk_q'
31
32 .end

```

HSPICE Test setup file for passing 1:



```

$example HSPICE setup file

$transistor model
.include "/proj/cad/library/mosis/GF65_LPe/cmos10lpe_CDS_oa_dl064_11_20160415/models/YI-SM00030/Hspice/models/design.inc"
.include "d_ff.pex.netlist"

.option post runlvl=5

xi GND! Q VDD! CLK R D S d_ff

vdd VDD! GND! 1.2v
vin CLK GND! pw1(0ns 1.2v 1ns 1.2v 1.075ns 0v 2ns 0v 2.075ns 1.2v 3ns 1.2v 3.075ns 0v 4ns 0v 4.075ns 1.2v 5ns 1.2v 5.075ns 0v 6ns 0v 6.075ns 1.2v 7ns 1.2v
7.075ns 0v 8ns 0v 8.075ns 1.2v 9ns 1.2v 9.075ns 0v 10ns 0v 10.075ns 1.2v 11ns 1.2v 11.075ns 0v 12ns 0v)

vinR R GND! pw1(0ns 1.2v 1ns 1.2v 1.08ns 0v 6ns 0v 8ns 0v 12ns 0v)
vinD D GND! pw1(0ns 0v 'test' 0v 'test+80ps' 1.2v)
vinS S GND! pw1(0ns 0v 1ns 0v 1.08ns 0v 6ns 0v 8ns 0v 12ns 0v)

cout Q GND! 70f

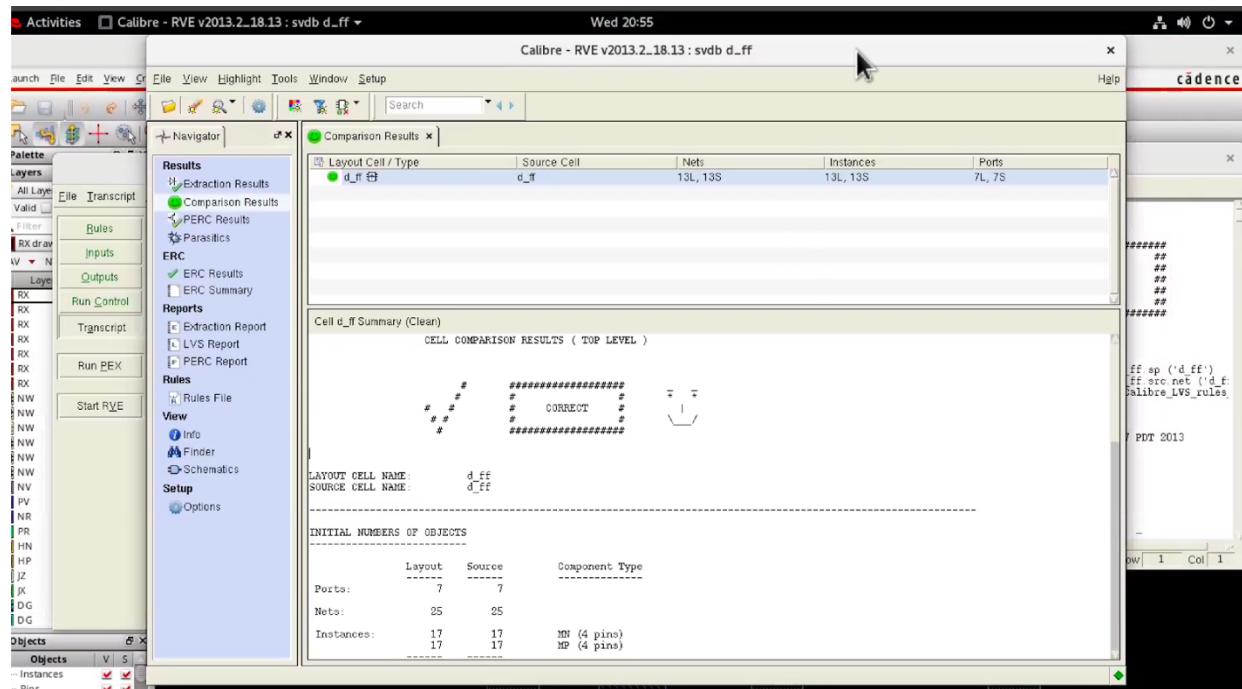
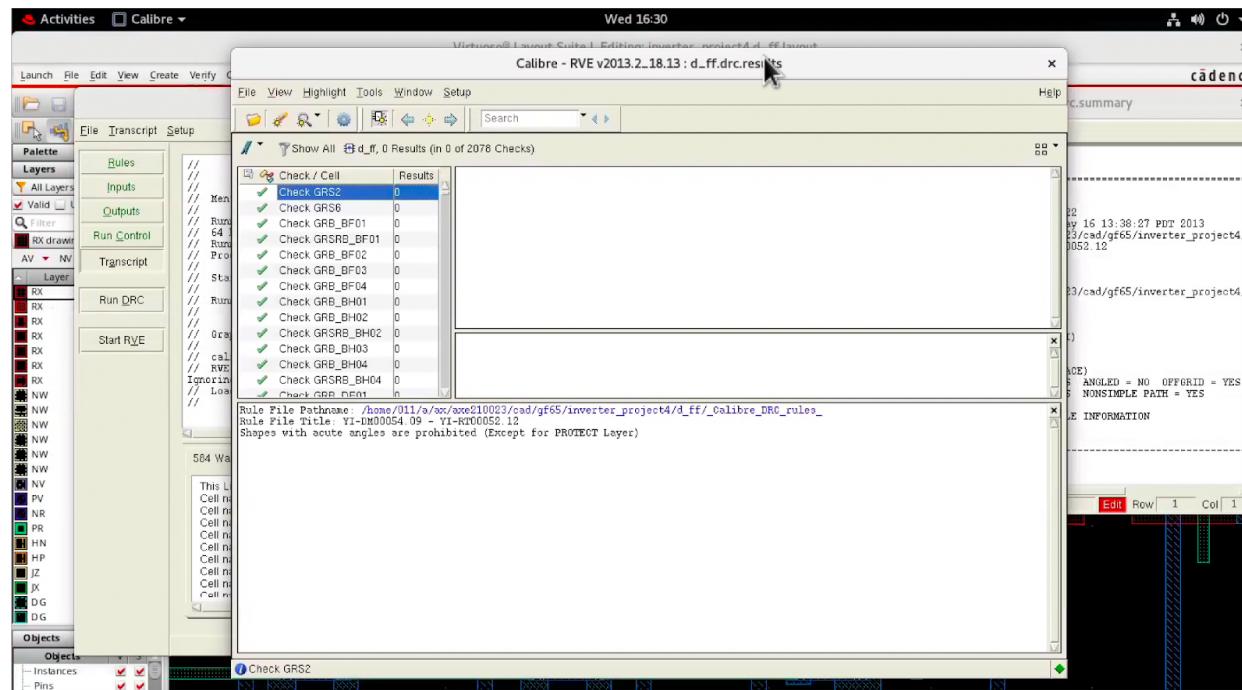
$transient analysis
.TRAN 1ps 12ns sweep test 2800ps 3000ps 60ps

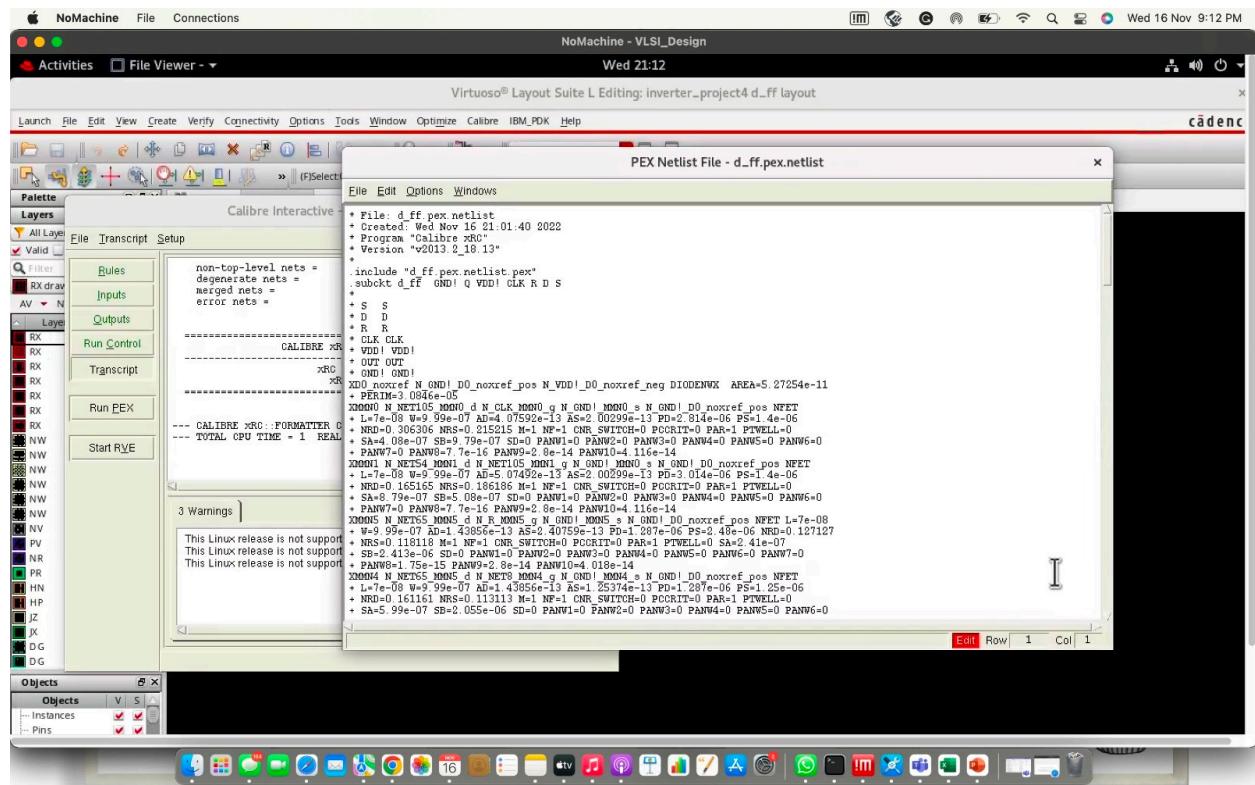
$example of parameter sweep, replace numeric value W of pfet with WP in invlvs.sp
$.tr 1ps 12ns sweep WP 1.616u 9u 0.0.899u test 2.9ns 3.1ns 10ps

.measure tsu trig v(D) val=0.6v rise=1 targ v(CLK) val=0.6v fall=2
.measure tclk_q trig v(CLK) val=0.6 fall=2 targ v(Q) val=0.6 rise=1
.measure tran delay param = 'tsu + tclk_q'

.end

```

DRC and LVS CHECK:

PEX - Netlist:**CONCLUSION:****1. Drop dead setup Time (T_{dd}):**

T_{dd} is the minimum time that is taken by the input to arrive before the active clock edge so that the input signal can be captured at the output. This is usually calculated by plotting a setup time vs. gate time delay graph.

2. Optimum Setup Time (T_{opt}):

Optimum Setup time is defined as the setup time for which time delay(t) is minimum.

3. $T_{opt} + T_{\text{hold}} = t$. Hold Time (T_h): The minimum amount of time that the data signal should be held steady after the clock even making sure the data is processed is called hold time.

$$T_{dd}(1) = Thold(0) \text{ and } T_{dd}(0) = Thold(1).$$

4. $T_{clk to Q}$ (T_{cq}): The clk to Q time is the time required for the output to have a stable/valid value after the falling edge of the clock. It is the time difference between the 50% amplitude of the clock and the output.**5. Delay Time(t):** Delay time is defined as $t = T_{opt} + T_{\text{hold}}$ **The Functionality of D-Flip Flop is designed and verified**