

PROJECT 3

CE 6325.001 VLSI DESIGN

**PROJECT 3:
REPORT FOR
INVERTOR DESIGN AND LAYOUT**

TEAM MEMBERS:

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RESULT:

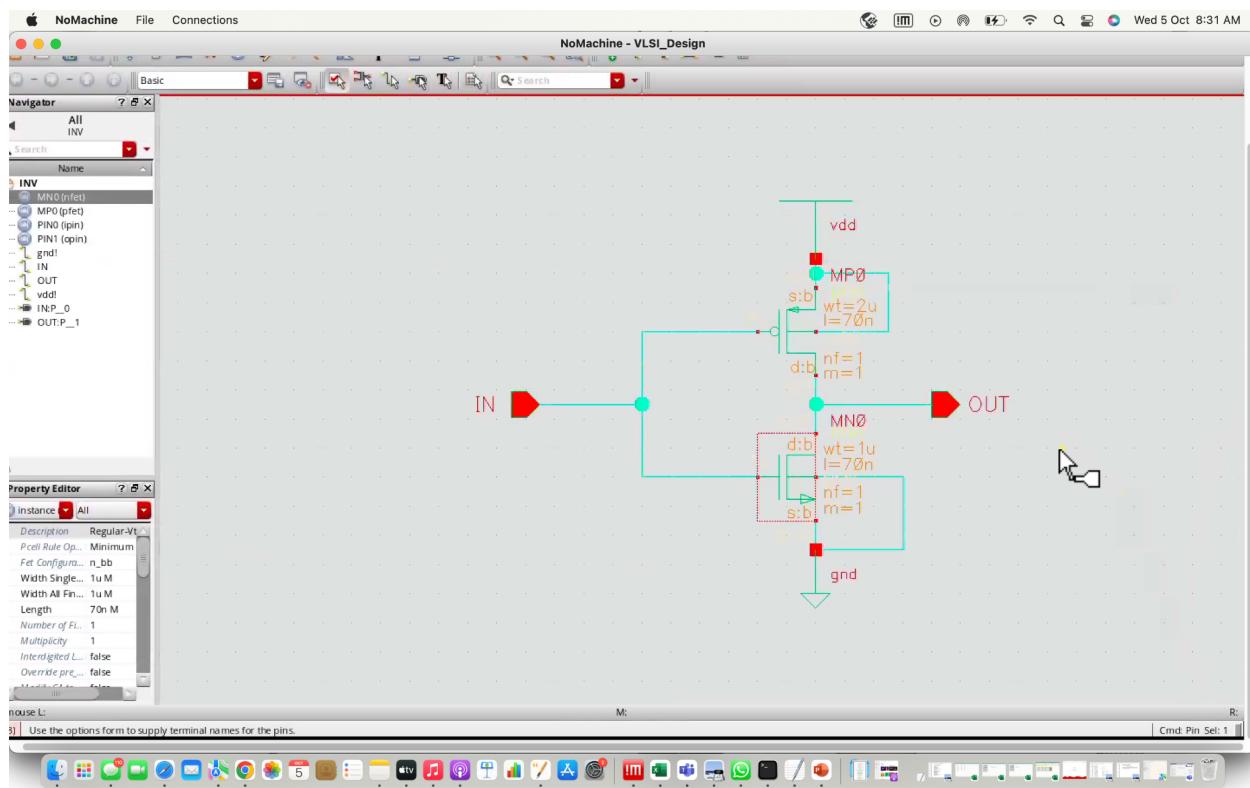
Energy	-1.061e-13
Delay	2.83e-10
EDP	2.981e-23
Area = (W * L)	$2\text{um} \times 1\text{um} = 2\text{um} = 2000.00\text{m}$
Tdiff (delay between t_{LH} and t_{HL})	4.35pm

OBJECTIVE:

In this project, we will use the 65nm process and Cadence design tools to design a layout and characterise an Inverter. The Design Objective is to minimise the Invertor layout's bounding box area ($H \times W$) while minimising the energy-delay product (EDP).

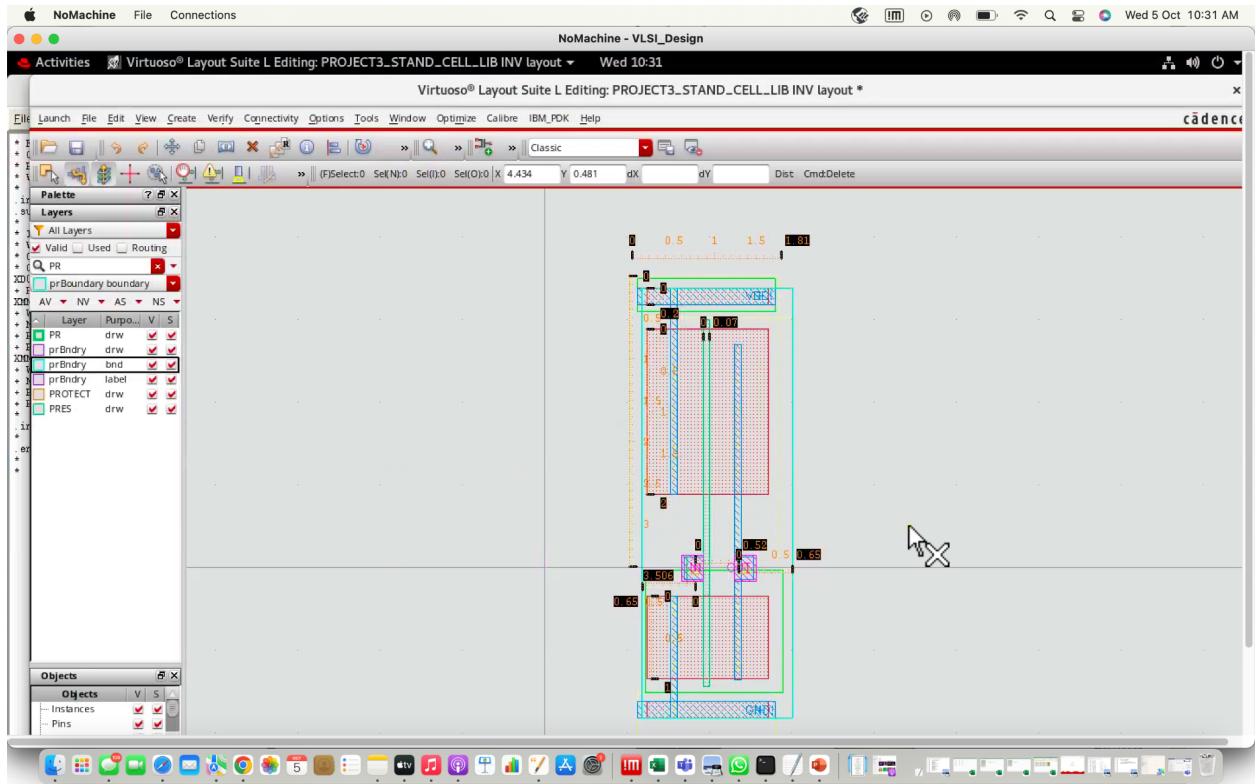
SCHEMATIC:

The Schematic version of the layout is given below:



LAYOUT:

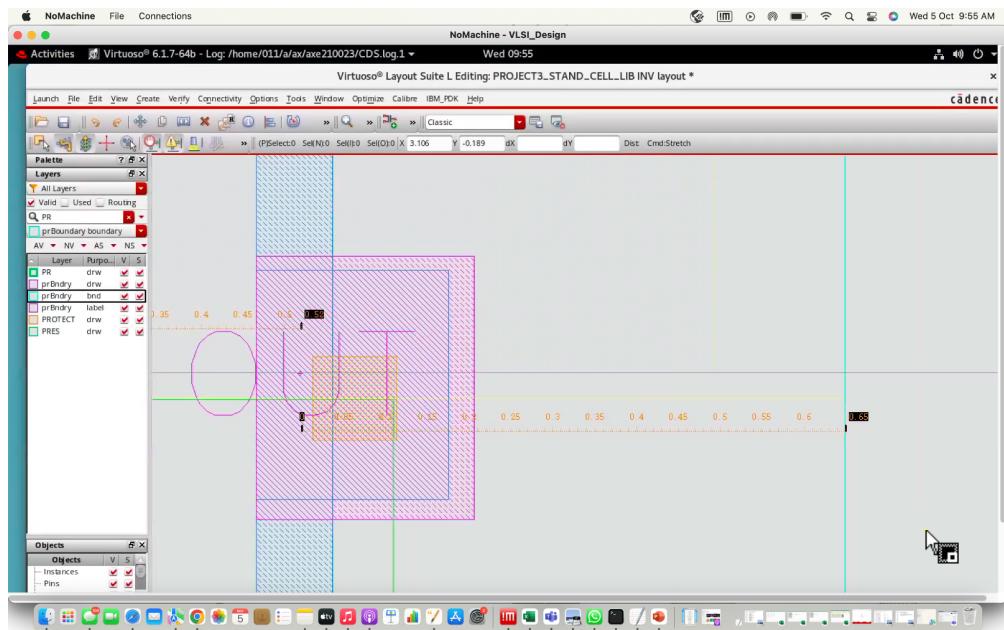
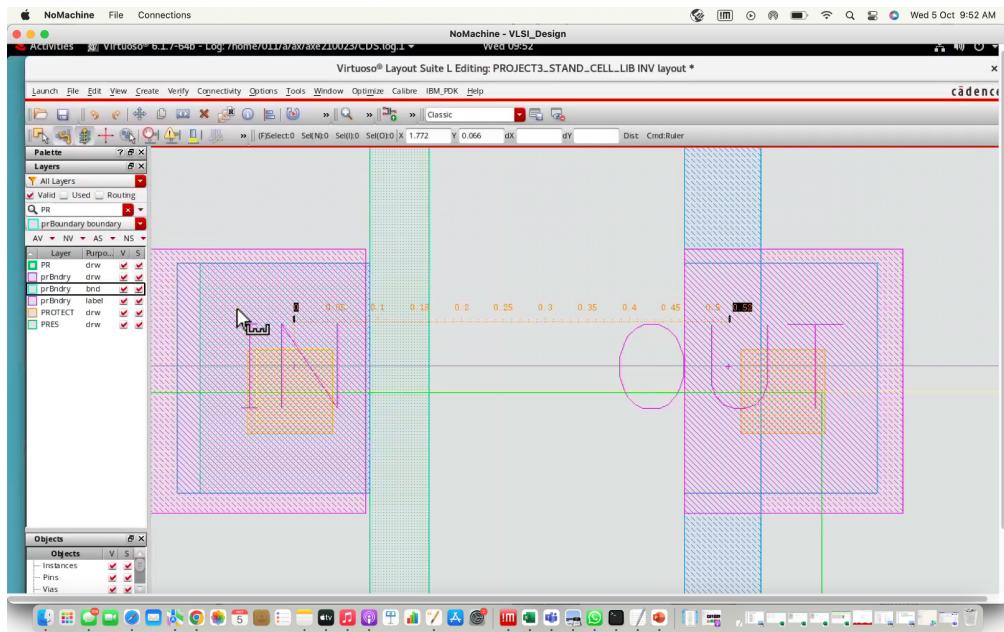
We have to build a layout of the invertor using Cadence Virtuso as below:

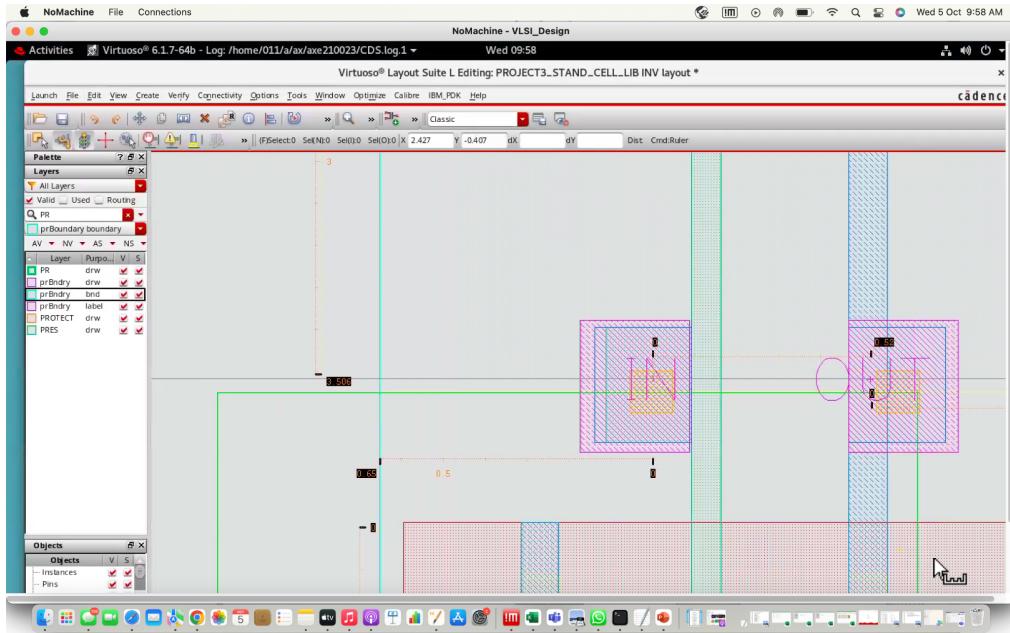


LAYOUT PARAMETER/PLACEMENT CHECK:

PIN PITCH: 0.52

OFFSET: 0.65





Layout Details: We have designed an inverter using cadence virtuoso with GF65nm process and the channel length of 70nm

VDD is 1.2V

GND is 0V.

Dimensions of Layout:

Height = 3.506 um

Width = 1.81 um

Width of PMOS = 2um

Width of NMOS = 1um

Length = 270nm

Area = 2um * 1um = 2um = 2,000.00nm

EDP = 2.981e-23

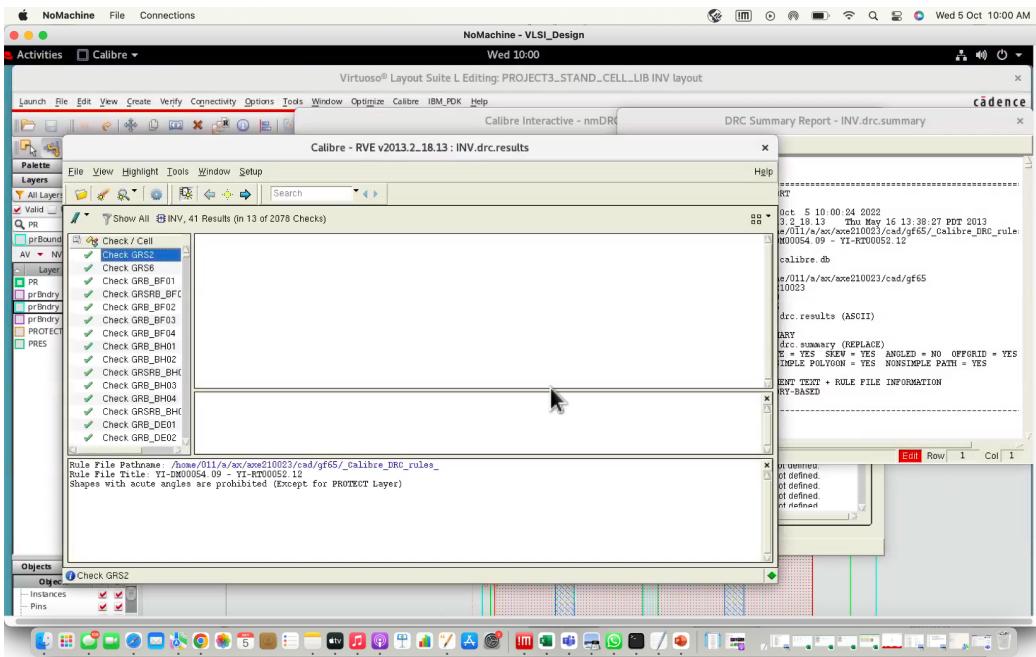
load capacitance = 70 fF.

Pin pitch = 0.52

Offset = 0.65

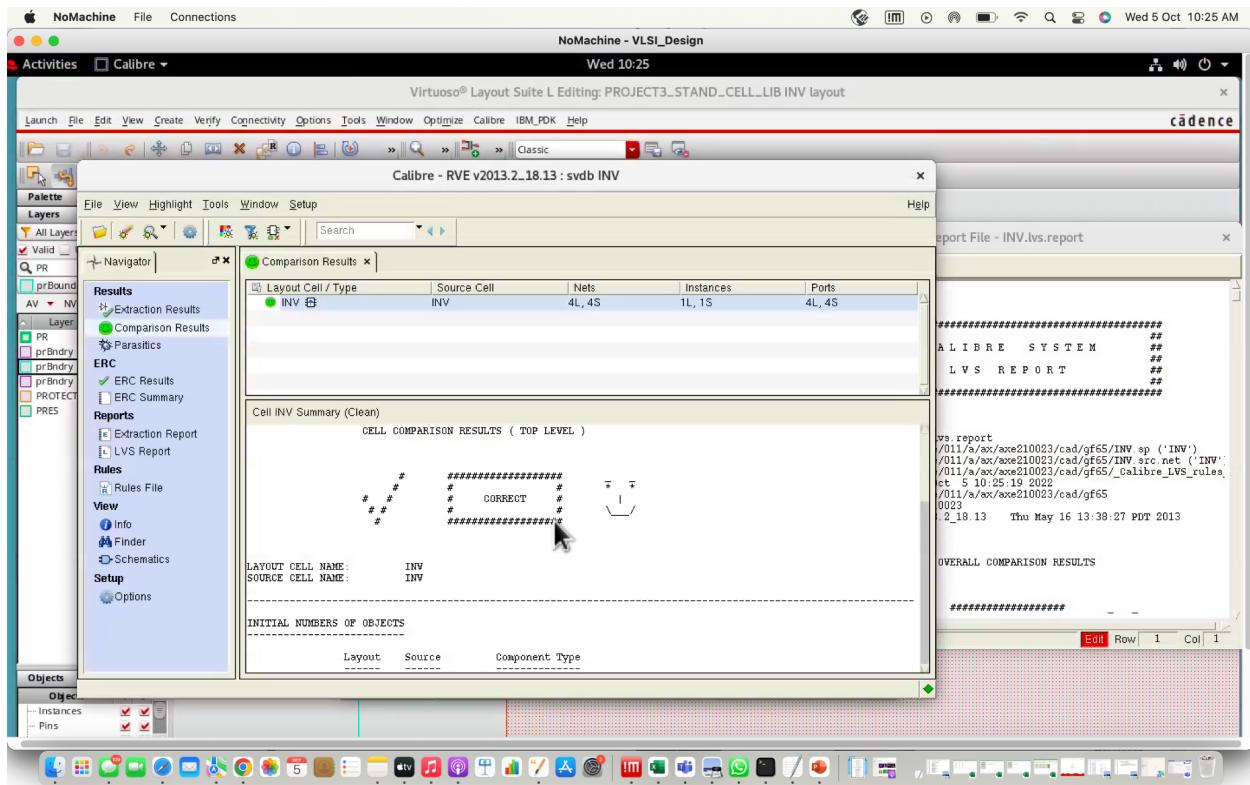
DRC:

We successfully ran the Design Rule Check

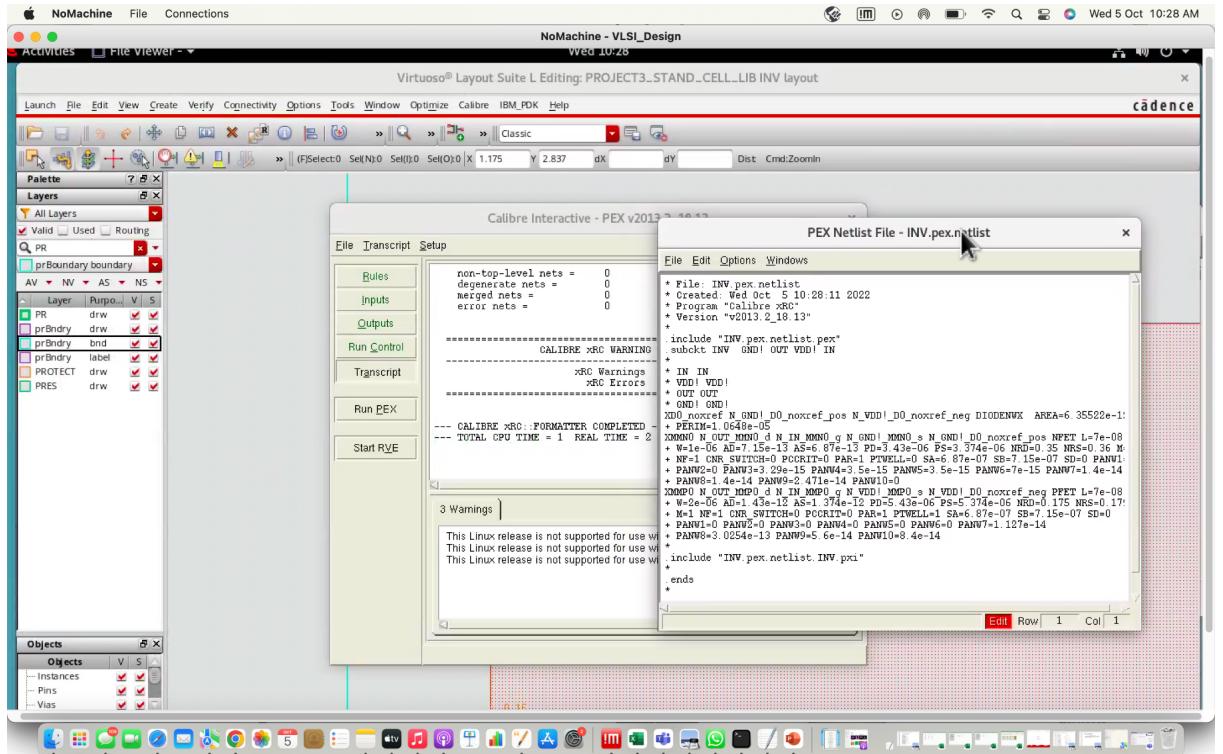


LVS :

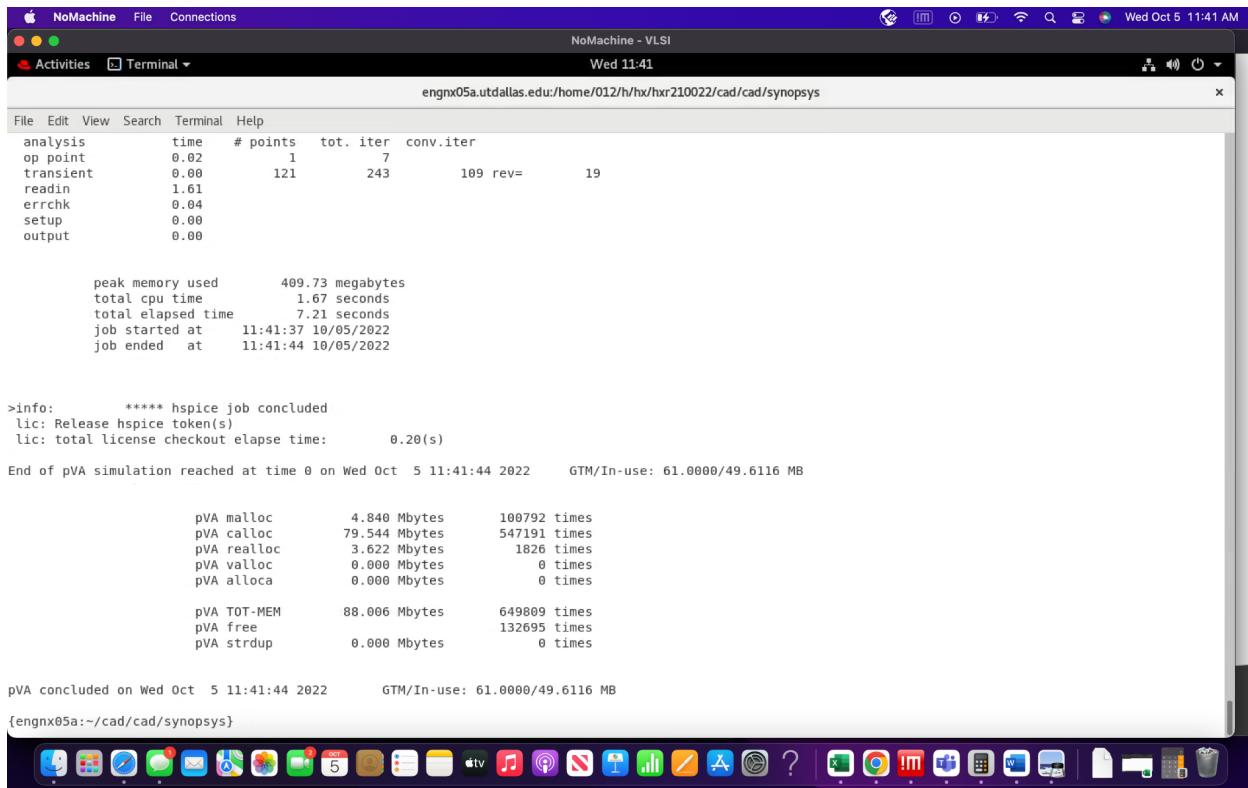
We ran the LVS check to check if the layout and schematic corresponding with each other and it ran successfully:



NETLIST:



SPICE Test Setup File:



```
NoMachine - VLSI
Activities Terminal ▾
engnx05a.utdallas.edu:/home/012/h/hx/hxr210022/cad/cad/synopsys
File Edit View Search Terminal Help
analysis      time # points tot. iter conv.riter
op point     0.02      1       7
transient    0.00     121     243     109 rev=      19
readin       1.61
errchk       0.04
setup        0.00
output       0.00

peak memory used      409.73 megabytes
total cpu time        1.67 seconds
total elapsed time    7.21 seconds
job started at        11:41:37 10/05/2022
job ended   at        11:41:44 10/05/2022

>info:      **** hspice job concluded
lic: Release hspice token(s)
lic: total license checkout elapse time:      0.20(s)

End of pVA simulation reached at time 0 on Wed Oct  5 11:41:44 2022      GTM/In-use: 61.0000/49.6116 MB

      pVA malloc      4.840 Mbytes      100792 times
      pVA calloc      79.544 Mbytes      547191 times
      pVA realloc     3.622 Mbytes      1826 times
      pVA valloc      0.000 Mbytes      0 times
      pVA alloca      0.000 Mbytes      0 times

      pVA TOT-MEM     88.006 Mbytes      649809 times
      pVA free        132695 times
      pVA strdup      0.000 Mbytes      0 times

pVA concluded on Wed Oct  5 11:41:44 2022      GTM/In-use: 61.0000/49.6116 MB
{engnx05a:~/cad/cad/synopsys}
```

Matrix :

```
$DATA1 SOURCE='HSPICE' VERSION='0-2018.09-2 linux64' PARAM_COUNT=0
.TITLE '$example hspice setup file'
trise          tfall          tavg          tdiff
delay          iavg           energy         edp1
t1              t2             t3            t4
i1              i2             energy1        energy2
energysum      edp2           temper         alter#
 1.269e-10    2.833e-10    2.051e-10    1.564e-10
 2.833e-10    -8.841e-06   -1.061e-13   3.006e-23
 6.001e-09    6.449e-09    6.250e-12    8.971e-10
-1.958e-04    -4.161e-08   -1.052e-13   -4.449e-17
-1.053e-13    2.983e-23    25.0000      1
```

SPICE Extracted Netlist File:



```
File: INV.pex.netlist
Created: Wed Oct 5 10:28:11 2022
Program: "Calibre XRC"
Version: "v2013.2_18.13"

include "INV.pex.netlist.pex"
subckt INV _VDD! OUT VDD! IN
    IN IN
    VDD! VDD!
    OUT OUT
    GND! GND!
    D0_noxref N _VDD! D0_noxref_pos N _VDD! D0_noxref_neg DIODENW2 AREA=6.35522e-12
    PERIM=1.76e-05
    M0N0 OUT MN0N d N IN MN0N g N GND! MN0N z N GND! D0_noxref_pos NPET L=7e-08
    W=1e-06 AD=7.15e-13 AS=6.87e-13 PD=3.43e-06 FS=3.374e-06 ND=0.35 NR=0.36 M=1
    NF=1 CNR SWITCH=0 PCCRIT=0 PAR=4.1e-12 L=0 SA=6.87e-07 SB=7.15e-07 SD=0 PANV1=0
    PANV2=0 PANV3=0 PANV4=0 PANV5=0 PANV6=0 PANV7=1.127e-14
    PANV8=1.4e-14 PANV9=2.471e-14 PANV10=0
    M0P0 OUT P0 d N P0N g N P0N z N P0N noxref_neg PFET L=7e-08
    W=2e-06 AD=1.473e-12 AS=1.374e-12 PD=4.39e-06 FS=5.374e-06 ND=0.1795 NR=0.1799
    M=1 NF=1 CNR SWITCH=0 PCCRIT=0 PAR=1 PTWELL=1 SA=6.87e-07 SB=7.15e-07 SD=0
    PANV1=0 PANV2=0 PANV3=0 PANV4=0 PANV5=0 PANV6=0 PANV7=1.127e-14
    PANV8=3.0254e-13 PANV9=5.6e-14 PANV10=0.4e-14

include "INV.pex.netlist INV.pxi"
ends
```

Output:

THL and TLH Waveforms:

Waveforms showing t_{LH} and t_{HL} times measured with Waveview. Delay difference between t_{LH} and t_{HL} is within 5ps, which is 4.35ps



