EECT/ CE 6325 VLSI Design
Fall 2022
Final Project: Layout & Verification
Due: Wednesday, Dec. 7, 2022, 11:30 AM

Project Introduction

For this project, you will take your Verilog code from project 2 (which can be modified in anyway) and lay it out using the cells that you generated in your cell library (projects 4 and 5).

Project Goals

1. Automatic placement and routing of your design using Cadence's Innovus
2. Run DRC (design rule checker) and LVS (layout versus schematic)
3. Run PrimeTime on the final layout using the extracted netlist to ascertain the worst-case delay

Project Rules & Requirements

1. Use an output capacitance of 70fF for all your outputs when testing, and input slew rates of 60 ps (0.1*Vdd to 0.9*Vdd and vice versa for Primetime)
2. At least 3000 cells (however, if your Verilog design is very intricate/complex, you can seek approval for less than 3000 cells).

What To Turn In (points are deducted for anything missing)

1. A cover page containing all the following information.
    - Name, NetID, "EECT / CE 6325", and project title
2. Formal Report detailing the complete design process from start to finish. This is where you will do your best to convince us that you have a quality design and have thought through your design carefully. All images, rulers, reports, etc., have to be readable to be graded. Your report must include, but is not limited to, the following:
    - Discuss tradeoffs
    - Clearly describe the function of your design
    - Worst-case delay of your design
    - Detail the testing process and describe how you tested it
    - Do not exceed 20 pages! (points will be deducted!)
3. A one-to-one comparison of output waveforms of your original Verilog/VHDL code, along with the waveforms from simulations of the actual layout (HSPICE) (Yes, that means with the same input and clock)
4. An image of the complete layout of the design with rulers clearly showing sizes.
5. DRC and LVS reports
    - Report if the design doesn't pass DRC or LVS and your interpretation of what is causing the error.
6. Primetime report to determine the best possible clock period and the total power consumed.

Project Flow and Tutorial Links:

1. You need to use Cadence virtuoso layout editor to create abstract views for your standard cells.
   - Refer abstract view generation tutorial on eLearning.
2. You then need to generate LEF files and prepare your design for Automatic Place and Route.
   - Project 6 Tutorial on eLearning.
3. Run Innovus to Place and Route your synthesized Verilog from project2
   - Project 6 Tutorial on eLearning.
4. Then import the routed design to cadence.
   - Project 6 Tutorial on eLearning.
5. You then need to clear DRC
   - https://personal.utdallas.edu/~Xiangyu.Xu/gf65/#41-design-rule-check-drc
   - Project6 tutorial on eLearning
6. You then need to clear LVS.
   - https://personal.utdallas.edu/~Xiangyu.Xu/gf65/#42-layout-vs-schematiccheck-lvs
   - Project6 tutorial on eLearning
7. Then Run Static Timing analysis using Primetime.
   - http://www.utdallas.edu/~xiangyu.xu/primetime/
8. You are now a VLSI expert!! :-)