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Chapter 06

Q1) Define clock signal and its use in digital electronic.

=> (i) A clock signal is a periodic waveform that oscillates between two voltage levels, used to synchronize the operation of digital components.

(ii) Purpose :- Its coordinates the timing of operations like data transfer, storage, and processing in a digital system.

(iii) Time Reference :- The clock signal ensure that operations occurs in the correct sequence and at the right time.

(iv) Uses :- Synchronization, Data sampling, Sequential Logic, Timing generation, Frequency Division.

Q2) Explain the working of Positive edge triggered SR Flip Flop with Preset and Clear inputs.

=> (1) When the CLK input transistions from low to high, the flip flop's output are updated based on the inputs.

(2) If both P and C inputs are low the flip-flop operates normally, and S and R inputs determine.

(3) If the P input is high and C input is low, the flip-flop is preset to set ($Q=1$, $\bar{Q}=0$) regardless to the S and R inputs.

(4) If P is low and C is high the flip-flop is cleared regardless of the S-R input.

(5) If both are high then the output is undefined.

Inputs			Outputs		Remark
CLK	S	R	Q_{n+1}	$\bar{Q}_{n+1}$	
0	x	x	Q_n	$\bar{Q}_n$	No change
1	x	x	q_n	$\bar{q}_n$	
↓	x	x	Q_n	$\bar{Q}_n$	No change
↑	0	0	Q_n	1	Reset
↑	0	1	0	1	Set
↑	1	0	1	0	
↑	1	1	Race	Race	Race

3) Differentiate between latch and flip-flop.

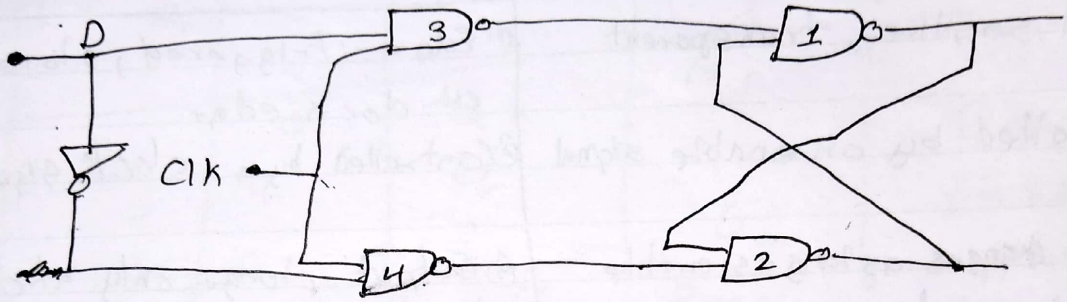
→

Latch	Flip Flop
① Level sensitive, transparent	① Edge-Triggered, stores data at clock edge.
② Controlled by an enable signal	② Controlled by a clock signal
③ Output changes as long as enable signal is active	③ Output changes only at clock edge.
④ More susceptible to glitches and timing issues	④ More stable less susceptible to glitches

4) Describe various methods of triggering a flip-flop.

→ ① Positive edge Trigger :- The flip flop changes its state on the rising edge of the clock signal i.e, when the clock signal transitions from low to high.
② Negative edge Trigger :- The flip flop changes its state on falling edge of the clock signal. i.e when the clock signal transition from low to high.
③ High level triggering :- The flip flop changes its state continuously as long as the clock signal is at high level
④ Low level triggering :- The flip flop changes its state continuously as long as the clock signal is at low level.

5) Draw the diagram of clock D flip flop and write Truth Table.



Inputs			outputs		Remarks
CLK	S	R	Q_{n+1}	$\bar{Q}_{n+1}$	
0	x	x	q_n	$\bar{q}_n$	No change
1	x	x	q_n	$\bar{q}_n$	
↓	x	x	q_n	$\bar{q}_n$	
↑	0	1	0	1	Reset
↑	1	0	1	0	Set

6) Explain the working of Positive Edge Triggered JK Flip-Flop.

=> (i) The clock signal is a train of rectangular wave.
(ii) It is passed through a differentiator [C-R1] and a rectifier (D-R2) to obtain only the positive spikes at point A.
(iii) Nand gates 1 and 2 forms the basic SR Latch.
(iv) Nand gates 3 & 4 have 3 inputs each.

(II) Working :-

(i) If CLK = 0 level or 1 level
No change (Flip Flop is disabled
Q and $\bar{Q}$ {do not change their state}

(ii) If CLK = ↓ :- R' = 1, S' = 1
No change

(iii) If CLK = ↑ :- J = 0, K = 0 (Output of R' = 1 & S' = 1
∴ No change

(iv) If CLK ↑ :- J = 0, K = 1

$R' = \overline{CLK \cdot J \cdot \bar{Q}} = \overline{1 \cdot 0 \cdot \bar{Q}} = 1$

~~S' = CLK.~~

$S' = \overline{CLK \cdot K \cdot Q} = \overline{1 \cdot 1 \cdot Q} = \bar{Q}$

(a) In previous state Q = 0 ; $\bar{Q}$ = 1

R' = 1, $S' = \overline{1 \cdot 1 \cdot 0} = 1$

∴ No change

(b) If previous state Q = 1 ; $\bar{Q}$ = 0;

$R' = \overline{1 \cdot 0 \cdot 0} = 1$

$S' = \overline{1 \cdot 1 \cdot 1} = 0$

∴ Reset condition

Q = 0 $\bar{Q}$ = 1

(5) If CLK = ↑ ; J = 1, K = 0

5) $R' = \overline{CLK \cdot J \cdot \bar{Q}}$ $\quad S' = \overline{CLK \cdot K \cdot Q}$

If previous state $Q = 0$, $\bar{Q} = 1$

$R' = \overline{1 \cdot 1 \cdot 1} = 0$

$S' = \overline{1 \cdot 0 \cdot 0} = 1$

$\therefore$ Set case

If Previous State $Q = 1$, $\bar{Q} = 1$

$R' = \overline{1 \cdot 1 \cdot 0} = 1$

$S' = \overline{1 \cdot 0 \cdot 1} = 1$

$\therefore$ No change

6) CLK = ↑, $J = 1, K = 1$

$R' = \overline{CLK \cdot J \cdot \bar{Q}}$

$S' = \overline{CLK \cdot K \cdot \bar{Q}}$

If Previous state $Q = 0$, $\bar{Q} = 1$

$R' = \overline{1 \cdot 1 \cdot 1} = 0$

$S' = \overline{1 \cdot 1 \cdot 0} = 1$

$\therefore$ Set case $(Q = 1, \bar{Q} = 0)$

If Previous state $Q = 1$, $\bar{Q} = 0$

$R' = \overline{1 \cdot 1 \cdot 0} = 1$

$S' = \overline{1 \cdot 1 \cdot 1} = 0$

$\therefore$ Reset case $(Q = 0, \bar{Q} = 1)$

6 $\frac{1}{2}$ Previous mode its in Toggle Mode.

7) Define race around condition. How can it be avoided.

=> (I) A race condition occurs in digital ~~electronics~~ circuits when the outputs of a flip-flop or other sequential logic elements becomes unstable due to conflicting timing or signal propagation delays. This can lead to unpredictable behaviour and incorrect results.

(II) It can be avoided by

(1) Use of edge triggers:-
(2) Synchronizing Inputs.
(3) Minimize Signal delays
(4) Use of Asynchronous Inputs.

~~8)~~