

		Date
913)	Compare Synchronous and as	ynchronous ripple counter
Estina	Synchronous	Asynchronous
Chok-	DAIL Aip-Hops receive the obck signal simultaneously	next flip-flop asynchronously
Symbro- nization	Bor all flips	@ No common clock stand
lomplezity	3) More complexed design due 28 The need for synchronized Clock signal	3) Relatively simpler design
Speed	Whater operation due to synchronized clark design	a Slower operation due to Asynchonous : Figgering
	SEasier to perform timing (6) Analysis	More challenging to perform
	Obsed in applications requiring soprecise timing and synchronous operation	application where speed is
	State all possible mode of	
3) OSiso! 37 O Serial In Serial Out (SISO]: Data is shifted in serially, one bit at a time, usually synchronous with a clock signal		

- @ Serial In Parallel Out (SIPO): Data is shifted in serially and then output in parallel.
- 3 Parallel In Iserial Out (PISO): Dat is shifted in sparallel and then sifted out serially.
- @ Parallel In/Parallel out CPIPOJ: Data is Ghifted in parallel and then sitted shifted out parallel. output in parallel
- 15) Describe the function of 3bit SISO/SIPO/PIPO/PISO register :-
- a DA 3 bit Serial In Serial Out (SISO) Shift register is a digital circuit that can store and shift a 3-bit binary nymber, one bit at a time.

Ily Working:

- I Serial In: (if The 3 bit binary number is input serially one bit at a time, into the shift register . Each Jinput bit is loaded in the first flip-flop (15B) on the rising edge of the clock signal.
- 2] Shift: if Once the 3-bits are loaded into the shift register, they can be shifted to right (or left) serially isshifting is done by applying clock stand pulse. iii) Each clock pulse causes the bit to move position to the By right (or left), with the LSB moving to the next
 - Flip-flop and MSB moving out of the register. 3] Serial - Out: The cutput of the shift register is taken from the last Flipflop. As The bits are shifted the MSB changes to the reflect the current value of 3-6145

number stored in the register

W Control signal: In addition to clock signal



