Chapter-6 FMP

Q1] List and define features of pentium processor:-

⇒ 1] Fifth-Generation Microprocessor:- It was introduced in 1993 as a part of 5th generation Microprocessor.
2] Clock Speed:- It operates at speed ranging from 60 MHz to 233 MHz
3] 32-bit Processor:- The processor features a 32 bit architecture with a 64-bit data bus.
4] Dual ALU:- It contains two separate ALU, each capable of performing 32-bit operations, supported by 8 memory banks
5] Superscalar Design:- The processor is 2 way superscalar utilizing 2 pipelines the U pipe and V pipe.
6] 32-bit Address bus:- The address bus is 32 bit, enabling access to upto 4GB of memory (2^{32}).
7] Integer pipelining:- It supports a 5-stage integer pipelining for faster data processing.
8] Floating point Unit:- The on chip floating point unit features an 8-stage pipeline for single operations.
9] Branch Prediction:- It includes branch prediction logic with a 256-entry Branch Target Buffer (BTB).
10] On-Chip Cache Memory:- The processor has an-chip memory with :-
a] 8 kb instruction cache
b] 8 kb data cache.

Q2] Define the role of Prefetch buffer of pentium processor with the help of an example

⇒ 1] The processor contains 32-byte prefetch buffer
2] These buffers operates independently but not simultaneously.
3] One prefetch buffer sequentially fetches instructions until a branch instruction is encountered.

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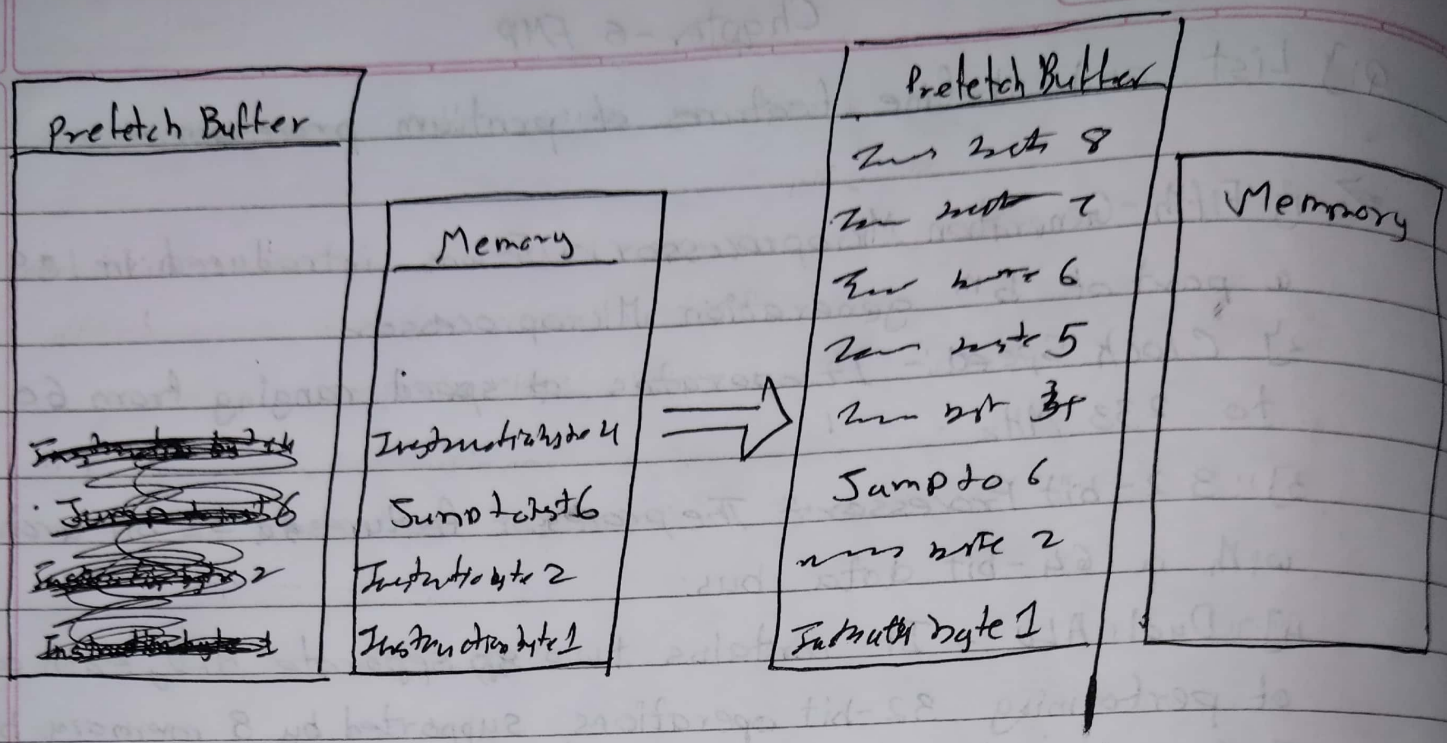


Q3) Define the role of the execution unit of pentium processor

=> 1] The Execution unit consists of two integer pipelines. the U-pipe and the V-pipe, each with its own ALU

2] Thes pipelines operate through five stages:-

i) Prefetch

ii) Decode-1

iii) Decod-2

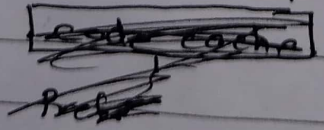
iv) Execute

v) Writeback

3] The U-pipe handles the execution of all integer and floating point instructions.

4] The V-pipe executes simple integer and some floating point instructions

~~Q4) Draw and explain pentium super scalar architecture~~



9} Draw and explain Pentium super-scalar architecture

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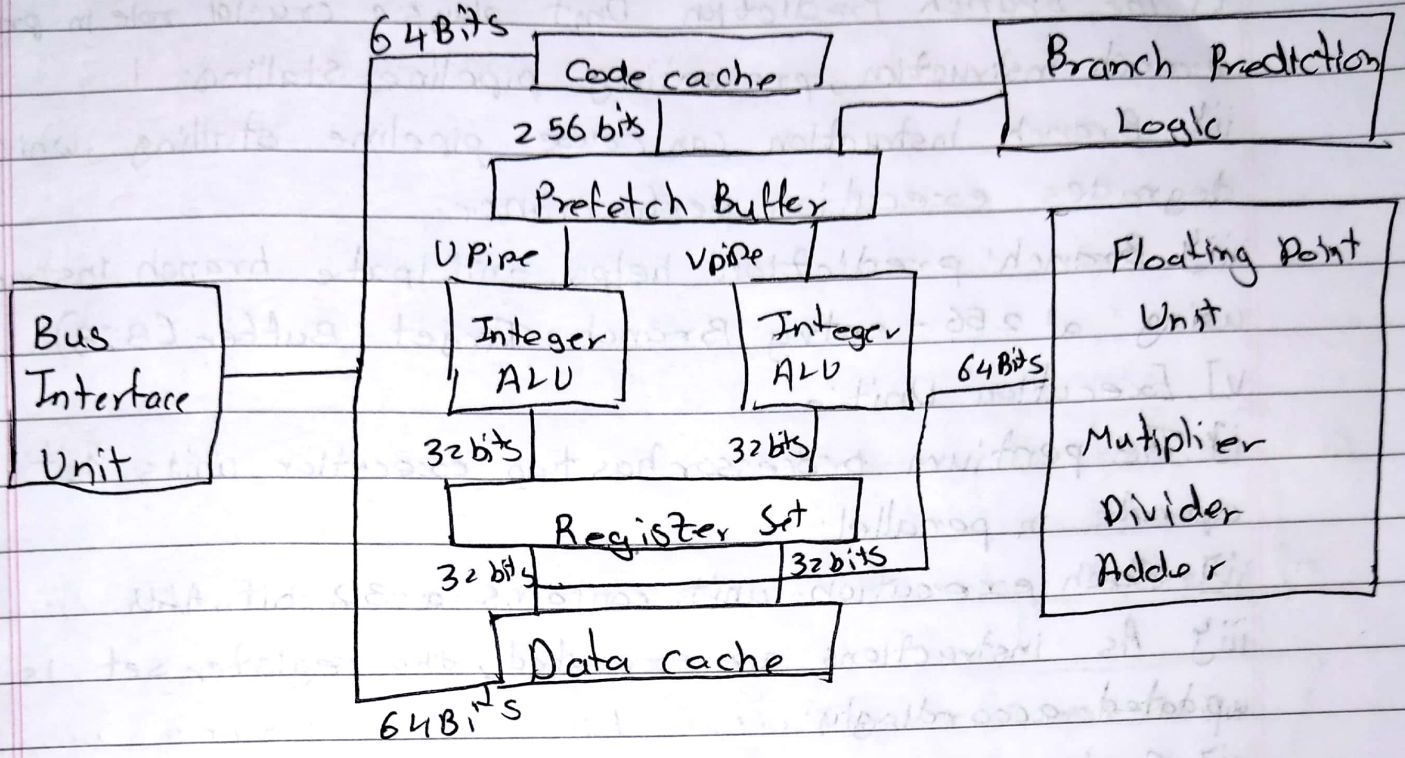

I} BIU:-

i} The BIU manages all system buses of the microprocessor unit

ii} It is responsible for the addressing of both memory ~~& I/O~~ and I/O devices.

iii} It features a 64-bit data bus and 32 bit address bus

II} Superscalar Structure:-

i} Superscalar architecture refers to the presense of more than one execution unit.

ii} The Pentium Processor contains two ~~or~~ integer units.

a} U-Pipe

b] V-pipe.

iii} Each integer unit is equipped with a 32 bit ALU

iv} With these two execution units, the Pentium performance is effectively doubled.

III} Prefetch Unit:-

i} The prefetch unit implements a five stages pipelining process.

ii} It contains a pair of 32-byte prefect buffer, which operates independently but not simultaneously.

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IV] Branch Prediction Unit

i] The Branch Prediction Unit plays a crucial role in predicting branch instruction, preventing pipeline stalling.

ii] Branch instruction can cause pipeline stalling, which degrades execution performance.

iii] Branch prediction helps anticipate branch instructions, using a 256-entry Branch Target Buffer (BTB).

V] Execution Unit:-

i] The pentium processor has two execution units that operate in parallel.

ii] Each execution unit contains a 32-bit ALU

iii] As instructions are executed, the register set is updated accordingly.

vi] Cache Memory :-

i] The pentium processor features integrated cache memory, enhancing execution speed.

ii] It has a 16kB split cache, with seperate memory for data and code, integrated on the chip.

vii] Floating Point Unit (FPU]:-

i] The FPU is responsible for executing floating-point instructions, significantly enhancing the microprocessor's capabilities for graphics and multimedia applications.

ii] It supports an 8-stage pipeline, improving the efficiency of floating point operations.

iii] The FPU features dedicated hardware circuits for operations such as multiplication, division and addition, boosting overall performance

iv] It supports single-double and extended precision floating point operations, utilizing eight 80 bits registers.

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Q5) Pipelining of Pentium processor with diagram

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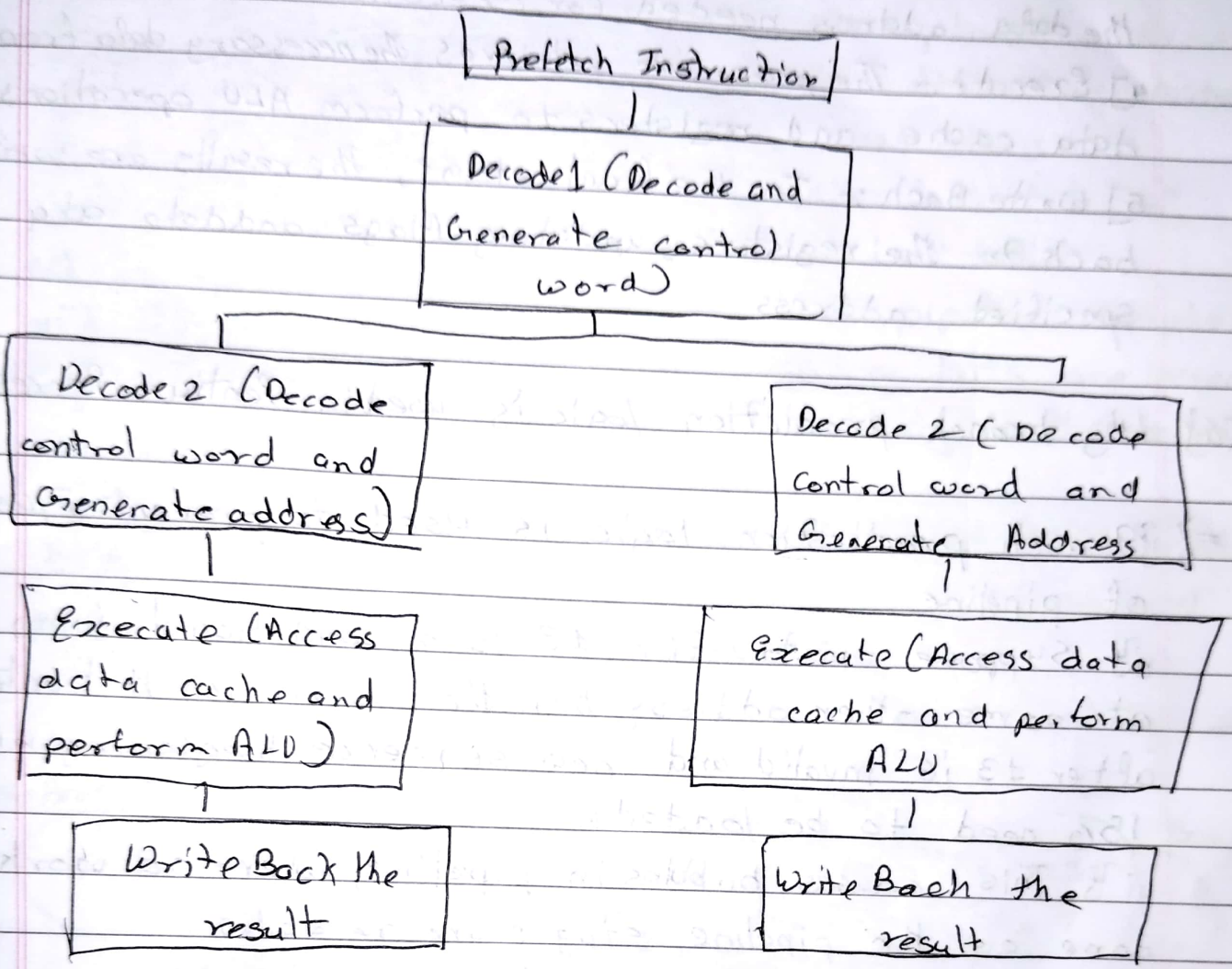

i) The Pentium processor features two integer units, referred as the U and V pipelines, each equipped with its own ALU and other components.

ii) This design allows the Pentium to execute two integer instructions in a single clock cycle using both pipelines, resulting in significantly enhanced performance.

iii) Each Pentium pipeline operates on five stage pipelining process:-

1] Prefetch:- This stage fetches instruction from code cache.

2] Decode 1 :- In this stage, two instructions are decoded in parallel. It also checks for dependencies between them. If there are no dependencies, the instructions are dispatched to the U and V pipelines, and a control word is generated.

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3] Decode 2:- This stage decodes the control word and computes the data address needed for execution.
4] Execute:- The processor retrieves the necessary data from the data cache and registers to perform ALU operations.
5] Write Back:- In the final stage, the results are written back to the registers, updating flags and data at a specified address.

Q6} Why branch prediction logic is used in Pentium Processor

=> i} Branch prediction logic is used to prevent Flushing of pipeline
ii} Suppose instruction 13 is a conditional jump to 150 at some other address, then the instruction that entered after 13 is invalid and new sequence beginning with 150 need to be loaded in.
iii} This causes bubbles in pipeline, where no work is done as the pipeline stages are reloaded.
iv} This is called flushing of pipeline problem.

Q7} Explain the solution to overcome flushing pipeline problem

=> i} The Pentium microprocessor employs a Dynamic Branch Prediction scheme. This method predicts the outcome of branch instruction currently in the pipeline as follows:
ii} True Prediction:- If the prediction is correct, the pipeline continues without being flushed, resulting in no loss of clock cycles
iii} False Prediction:- If the prediction is incorrect, the pipeline is flushed, and execution starts over with the current instruction.

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iv) The branch prediction logic is implemented using a 4-way set associative memory with 256 entries, known as Branch Target Buffer (BTB). The 4-way set is defined by history bits, which determines the prediction as follows.

i) History Bits = 00 or 01 : Prediction is "not taken".

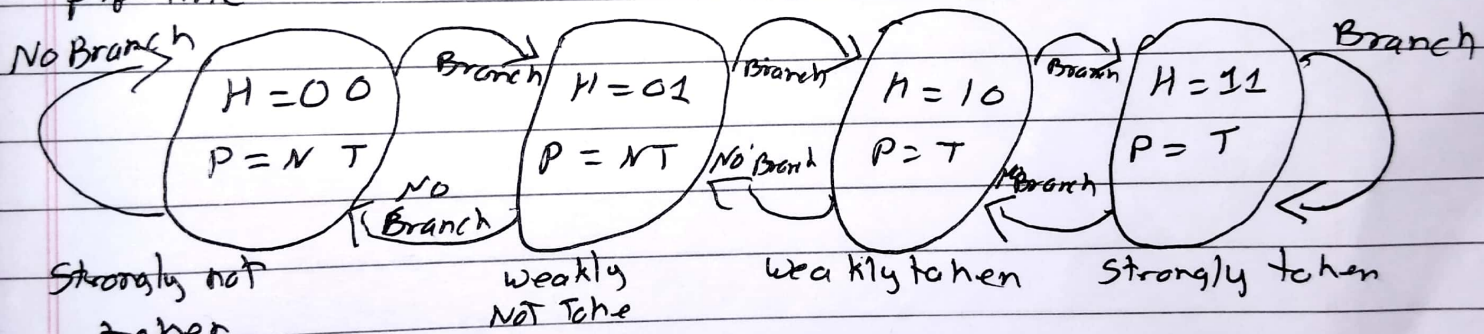
ii) History Bits = 10 or 11 : Prediction is "taken".

iv) In event of a false prediction, the pipeline is flushed

vi) If branch is executed, the history bits are incremented by one, indicating an increased priority for that branch prediction.

vii) Conversely, if the branch is not executed the history bits are decremented by one, reflecting a decreased priority for that branch prediction.

viii) The above logic is used to prevent flushing of pipeline.



History Bits	Branch Prediction
00	Not taken
01	Not Taken
10	Taken
11	Taken

Q8) Explain Branch predction logic for pentium processor.

=> Same as above just cancel out the 8th point.

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