Experiment no. 01

Date:- 13/07/24

Roll No:- A046

Aim:- To draw the architecture of 8086 and explain each block.

Theory:-

The architecture of 8086 is divided into two parts EU and BIU

I] The Execution Unit [EU]:- The main function of EU is decoding and execution of the instructions. In order to carry out this tasks it has the following units.

i) Arithmetic Logic Unit (ALU) :- The ALU is a bit bit unit .i.e. it can perform 16-bit operation simultaneously.
It is capable of performing a variety of arithmetic and logical operation such as add, subtract, AND, OR, NOT, increment, decrement, shift, etc.

ii) Flag Register :- It is a 16 bit register with each bit corresponding to a flip-flop. It is used to give the status of operation performed by the processor. It indicates some condition produced by the execution of an instruction.

iii) General purpose register:- EU has four general purpose 16-bit register. Each one of them can be used for temporory storage of 8-bit, 16-bit, 32 bit data. These register can be used for general purpose computing when their other specialized functions do not interfere.

iv) Control Unit :- It is a part of EU which is used for directing the internal operations

v) Decoder :- The process of translation ~~for~~ from instructions into action is known as decoding. It's used to translate the instructions fetched from the memory into a series of actions.

vi) Pointer and Index Registers :- Thes registers can be used as general purpose 16-bit registers. But mainly they are used to hold the 16-bit offset of data word in one of the segment.

II) BUI :- The bus interface unit performs all the activities related to Bus. Specifically BIU has the following 5 functions

i) Intruction Queue :- The execution unit is ~~performed~~ supposed to decode or execute an intruction. Decoding does not require theuse of buses. When EU is busy decoding and executing intructions, the BIU fetches upto six instructions bytes for the next instruction. These bytes are called prefetched bytes and they are stored in a first in an first out register which is called a queue.

ii) Segment Registers :- The purpose of using these segment registers and segmentation can be explained as. They ar 16 bits register. There are a total of 4 segment registers. namely The code segment register, The stack segment register, The extra segment register, The data segment register.

iii) Instruct Pointer Register (IP) :- It holds the next offset address of the next Instruction to be executed within the code segment It points to the memory location in code segment where the next instruction is to be fetched. The combination of CS and IP registers gives the complete address of the ~~ins~~ instruction. The effective address for fetching an instruction can be calculated as CS x 16 + IP.

iv) Physical address generation:- The CS register contains the upper 16-bits of the starting address of the code. The BIU will automatically insert zeroes for the lowest 4 bits of the segment base address to get 20 bit physical address starting from CS.

The I.P ~~address~~ register contains the offset or distance from this address. Add the starting address of code segment to the offset to get the physical address of the location containing the next code byte.

Conclusion:- Hence we successfully explained the architecture of 8086.