

1-Bit Phase Shifting Switch Module for Reconfigurable Intelligent Surface

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Abstract

This study focuses on the design of a 1-bit phase shifter for Reconfigurable Intelligent Surface (RIS). The goal is to design a switch centered at 8 GHz, achieved through careful matching network design and transistor size selection. To ensure optimal performance in high-frequency applications, the switch will utilize GaAs HEMT (High Electron Mobility Transistor), which provides high electron mobility and superior performance in the RF spectrum. In addition to schematic-level design, this work presents a layout implementation optimized for high-frequency operation; in parallel, a wideband matching strategy is also proposed to enhance performance over the target bandwidth. This work contributes to the development of efficient and high-performance switch design for RIS systems in next-generation communication networks.

1. Introduction

Reconfigurable Intelligent Surface (RIS) is an innovative technology in wireless communication systems that enables reconfigurable control of electromagnetic wave propagation. As shown in Fig. 1, RIS consists of an array of unit cells that reflect incident signals with adjustable phase shifts. By intelligently shaping the propagation environment, RIS can significantly improve signal strength, coverage, and overall network performance. This makes RIS a promising solution for overcoming propagation challenges in obstructed or non-line-of-sight environments. Furthermore, its low-cost, energy-efficient architecture improves its practicality for implementation in future communication systems.

As shown in Fig. 2, RIS is composed of multiple unit cells, each responsible for controlling the phase of the reflected signals. Among these components, the phase shifter plays a critical role, as it directly determines the beamforming and signal manipulation capabilities of the surface. This

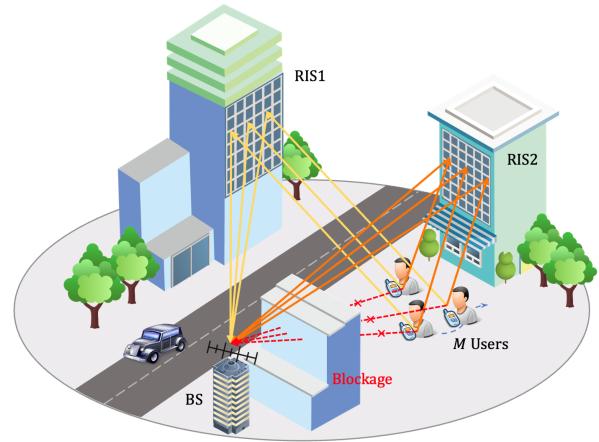


Figure 1. RIS-assisted wireless communication in a blocked environment.

study focuses on the design of a 1-bit phase shifter based on a Single-Pole Single-Throw (SPST) switch, which operates between two discrete phase states—typically 0° and 180°—by utilizing the on/off control of the switch. To realize this, a GaAs HEMT (High Electron Mobility Transistor) switch is employed to ensure fast operation and near-zero power consumption, which are essential in high-frequency RIS applications.

The core of this research lies in designing and optimizing a 1-bit phase shifter that exhibits accurate switching behavior at the target frequency of 8 GHz. In addition, the design aims to minimize insertion loss and ensure precise phase difference, both of which are critically influenced by the careful design of the matching network and the selection of optimal transistor size. To analyze and refine the circuit performance, the study employs Advanced Design System (ADS) simulations.

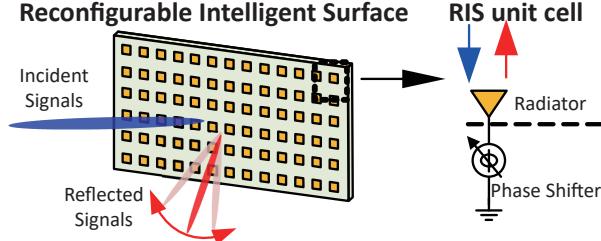


Figure 2. Configuration of RIS with unit cell.

2. Related work

Previous studies have explored various implementations of 1-bit phase shifters for Reconfigurable Intelligent Surfaces (RIS). For example, [1] proposed a dual-polarized RIS with low loss and wide bandwidth for X-band applications, focusing on passive component integration and system-level validation. Additionally, [2] designed a QFN-packaged 8-channel 1-bit phase shifting switch module using FETs, demonstrating its feasibility for Ku-band operations. These studies provided valuable insight into the architectures and packaging techniques of RIS unit cells, laying the foundation for future developments in high-frequency RIS systems.

In contrast to former studies, this study adopts Gallium Arsenide (GaAs) HEMT-based switches instead of the commonly used CMOS or diode technologies. This choice is motivated by the superior high-frequency characteristics of GaAs, which allow for fast switching and near-zero power consumption. Furthermore, while previous studies have focused on fixed single-frequency operation, this work goes a step further by proposing a broadband matching strategy aimed at extending the performance over a desired frequency range. These distinctions highlight the novelty and contribution of the proposed approach to the field of RIS design.

3. Method

3.1. Why GaAs HEMT is Suitable for RIS 1-Bit Phase Shifter

In reconfigurable intelligent surface (RIS) architectures, 1-bit phase shifters are essential components that must deliver low signal loss, minimal power consumption, high linearity, and fast switching for real-time beam control. GaAs high electron mobility transistors (HEMTs) offer a strong candidate that meets these demands and frequently outperform traditional PIN diodes and CMOS switches in key performance metrics.

First, GaAs HEMTs achieve low insertion loss thanks to their high electron mobility, which results in a low on-state resistance (R_{on}) and minimizes signal attenuation in the ON

state. In the OFF state, their inherently low off-state capacitance (C_{off}) helps reduce signal leakage and phase distortion. These characteristics are particularly advantageous in high-frequency RIS arrays, where maintaining uniform phase shifts across many unit cells is essential. By contrast, CMOS switches typically exhibit higher R_{on} and noticeable C_{off} , leading to greater loss and degraded phase control.

Second, GaAs HEMTs demonstrate excellent power efficiency over PIN diodes. PIN diodes require continuous forward bias current, causing static power consumption, whereas GaAs HEMTs are voltage-controlled and draw negligible steady-state current, making them suitable for low-power RIS designs.

Third, GaAs HEMTs support fast switching speeds thanks to their short gate lengths and high transition frequencies (f_T), which enable rapid phase changes even at millimeter-wave bands. This capability is essential for dynamic beam steering. While CMOS is more integrable, it generally underperforms in high-frequency switching and linearity under large-signal conditions.

In addition, GaAs HEMTs often incorporate back vias, which allow direct grounding beneath the device. This eliminates the need for large ground pads, simplifies the layout, and reduces parasitic inductance—particularly important in compact and densely packed RIS implementations.

In summary, GaAs HEMTs combine low insertion loss, low power consumption, fast switching, and high linearity with practical layout benefits. These advantages make them superior switching elements for 1-bit phase shifters in high-frequency RIS applications.

3.2. Trade-Off Relationship in Non-Ideal Switch

In practical FET-based switch design, the switch exhibits distinct behaviors depending on its state. In the ON state, it behaves as a resistor characterized by on-state resistance R_{on} , as shown in Fig. 3(a). The on-state resistance R_{on} causes reflection loss, reducing the magnitude of the reflected signal.

In contrast, when the switch is in the OFF state, it behaves as a capacitor with off-state capacitance C_{off} , as shown in Fig. 3(b). Similarly, C_{off} alters impedance across frequencies, disrupting the required 180° phase difference and causing phase distortion.

For a 1-bit phase shifter to function properly, it must ensure the same reflection magnitude in both states and maintain an exact 180° phase difference between them. However, due to the presence of R_{on} and C_{off} , these non-ideal parasitics critically affect the performance of phase shifters, especially by disturbing the phase balance and increasing the reflection loss.

In the ideal scenario, a FET-based switch operates with zero on-state resistance ($R_{on} = 0$) and zero off-state capacitance ($C_{off} = 0$). Under these conditions, the impedance

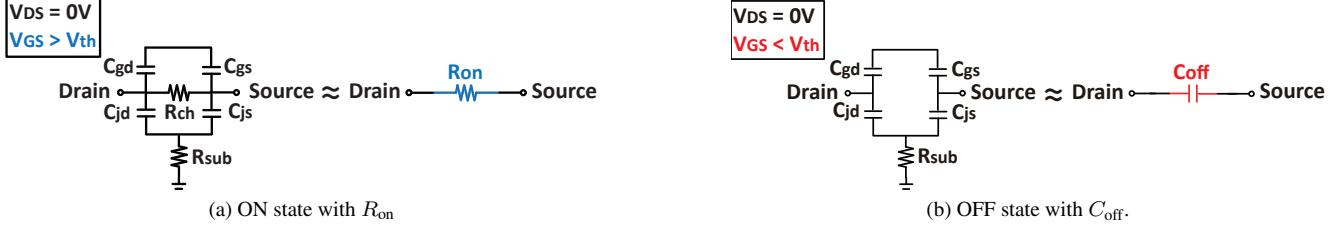


Figure 3. Equivalent circuit model of a FET switch : (a) ON state and (b) OFF state.

and reflection coefficient in the ON state are given by

$$Z_{\text{on}} = R_{\text{on}}, \quad (1)$$

$$\Gamma_{\text{on}} = \frac{Z_{\text{on}} - Z_0}{Z_{\text{on}} + Z_0} = \frac{R_{\text{on}} - Z_0}{R_{\text{on}} + Z_0}, \quad (2)$$

which simplifies to $\Gamma_{\text{on}} = -1$ when $R_{\text{on}} = 0$.

In the OFF state, the impedance and reflection coefficient are

$$Z_{\text{off}} = \frac{1}{j\omega C_{\text{off}}}, \quad (3)$$

$$\Gamma_{\text{off}} = \frac{Z_{\text{off}} - Z_0}{Z_{\text{off}} + Z_0} = \frac{\frac{1}{j\omega C_{\text{off}}} - Z_0}{\frac{1}{j\omega C_{\text{off}}} + Z_0}, \quad (4)$$

which becomes $\Gamma_{\text{off}} = +1$ when $C_{\text{off}} = 0$. This results in the ON and OFF states having the same reflection magnitude and an exact 180° phase difference. Fig. 4 illustrates the ideal behavior, where the impedance points lie at opposite ends of the Smith chart.

However, in practical designs, R_{on} and C_{off} are non-zero. A non-zero C_{off} shifts Γ_{off} from $+1$, disturbing the 180° phase difference. Similarly, a non-zero R_{on} reduces $|\Gamma_{\text{on}}|$, causing unwanted reflection and insertion loss. As shown in Fig. 4, these non-idealities cause the impedance points to shift asymmetrically and inward, disrupting both ideal phase separation and magnitude symmetry.

Importantly, R_{on} decreases as the transistor size increases, while C_{off} increases with transistor size. This inverse relationship introduces a fundamental trade-off: minimizing signal loss and preserving ideal phase performance cannot be achieved simultaneously through transistor sizing alone. Therefore, careful co-design of transistor dimensions and the matching network is essential to ensure that the switch achieves both amplitude symmetry and the target 180° phase difference.

3.3. Initial Schematic and Simulation Results

Fig. 5 illustrates the schematic of initial switch module without a matching network. The schematic was implemented in ADS using the PDK provided by Winsemi, the GaAs HEMT manufacturer used in this research.

At the center of the circuit is the GaAs HEMT, which is grounded via a back via structure. The threshold voltage of

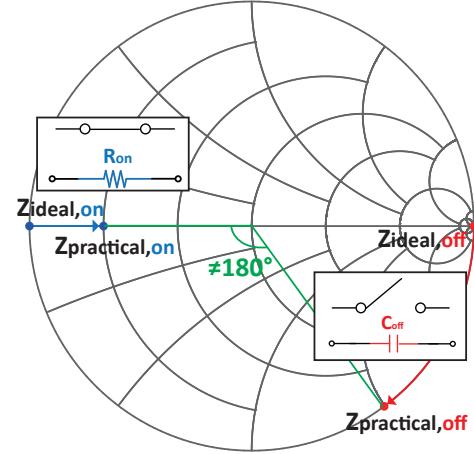


Figure 4. Ideal and practical impedance points on the Smith chart.

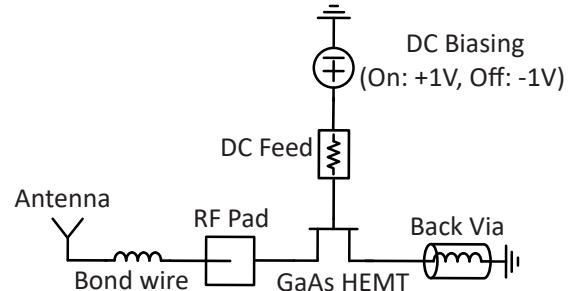


Figure 5. Schematic of the initial switch module.

the selected transistor is -0.95 V, and we define the gate bias conditions as $+1$ V (ON state) and -1 V (OFF state), respectively. A DC feed is inserted at the gate terminal to block RF signals while allowing only the DC control voltage to pass. The RF signal paths are connected through pads to the HEMT, and the bond wires—implemented as inductors—are modeled with an inductance of 1 nH in this research. This stage corresponds to the chip-level design. When combined with an antenna, it forms a complete unit cell for the RIS.

Fig. 6 shows the simulation results of this initial model. At the target frequency of 8 GHz, the ON and OFF states exhibit both magnitude and phase mismatches. The phase

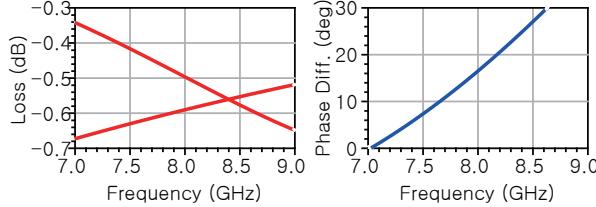


Figure 6. Simulation results of the initial switch module.

difference deviates significantly from 180° , and the reflection magnitudes are unequal. These imperfections originate from the absence of a properly designed matching network.

3.4. Matching Network Design

To realize a perfect switch operating at the target frequency of 8 GHz—exhibiting identical reflection magnitudes and a 180° phase difference between ON and OFF states—a matching network must be designed and integrated into the circuit.

3.4.1. " $R \ll X$ " Region Strategy

A fundamental requirement for perfect switching is that the reflection coefficients of the ON and OFF states satisfy the condition:

$$\Gamma_{\text{on}} = -\Gamma_{\text{off}}. \quad (5)$$

This leads to the following relationship:

$$\frac{Z_{\text{on}} - Z_a}{Z_{\text{on}} + Z_a} = -\frac{Z_{\text{off}} - Z_a}{Z_{\text{off}} + Z_a}, \quad (6)$$

which can be algebraically solved to yield the optimal matching impedance Z_a , which represents the impedance seen when looking toward the antenna from the output of the matching network:

$$Z_a = \sqrt{|Z_{\text{on}}| \cdot |Z_{\text{off}}|}. \quad (7)$$

If the transistor is properly sized such that both Z_{on} and Z_{off} lie in the “ $R \ll X$ ” region on the Smith chart—i.e., where the reactive component dominates, as shown in Fig. 7—the expression can be further approximated as:

$$Z_a \approx \sqrt{|X_{\text{on}}| \cdot |X_{\text{off}}|}, \quad (8)$$

where X_{on} and X_{off} are the imaginary components of the respective impedances. This approximation simplifies the calculation of Z_a , enabling a more practical design approach based on dominant reactance values.

Once Z_a is determined, A quarter-wave transformer can then be designed to match this impedance to a 50Ω antenna as shown in Fig. 8. The characteristic impedance of the transformer is selected as:

$$Z = \sqrt{50 \cdot Z_a}. \quad (9)$$

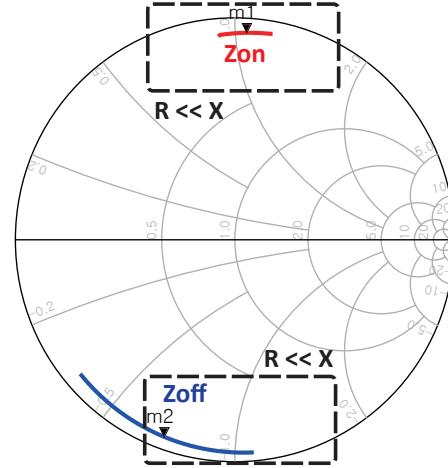


Figure 7. $R \ll X$ region on the Smith chart.

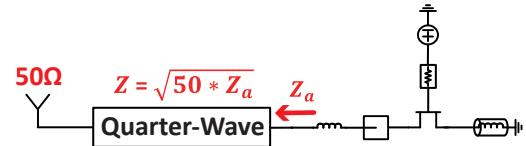


Figure 8. Quarter-wave transformer for matching between 50Ω and Z_a .

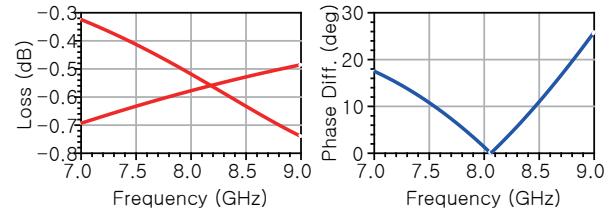


Figure 9. Simulation results after applying the $R \ll X$ region strategy.

As shown in Fig. 9, the proposed matching network significantly improves performance compared to the unmatched initial design. However, the switch does not yet achieve ideal performance at 8 GHz. Two primary reasons contribute to this deviation: (1) the “ $R \ll X$ ” approach relies on an approximation that introduces inherent errors, and (2) traditional reflection coefficient analysis can not fully account for the behavior of circuits under complex impedance conditions.

3.4.2. Power Waves

As explained in [3], traditional reflection coefficient analysis, which is based on voltage and current relationships, assumes a real-valued characteristic impedance and provides accurate results only when the system operates with purely real impedances. However, in scenarios such as this research, where complex impedance conditions are involved,

power wave-based analysis becomes necessary.

To address this, the power wave reflection coefficient Γ_p is introduced. It is defined as:

$$\Gamma_p = \frac{Z_L - Z_R^*}{Z_L + Z_R}. \quad (10)$$

This formulation enables proper analysis under general impedance conditions.

To find the desired value Z_a , we define the ON and OFF state impedances as:

$$Z_{\text{on}} = R_1 + jX_1, \quad Z_{\text{off}} = R_2 + jX_2, \quad (11)$$

and the wanted value as:

$$Z_a = R_3 + jX_3. \quad (12)$$

Using the power wave reflection coefficient and applying the condition:

$$\Gamma_{p,\text{on}} = -\Gamma_{p,\text{off}}, \quad (13)$$

This leads to the following equation:

$$\frac{Z_{\text{on}} - Z_a^*}{Z_{\text{on}} + Z_a} = -\frac{Z_{\text{off}} - Z_a^*}{Z_{\text{off}} + Z_a}. \quad (14)$$

Solving this yields the following expressions for R_3 and X_3 :

$$R_3 = \sqrt{R_1 R_2 - X_1 X_2 + \frac{(R_1 X_2 + R_2 X_1)(R_1 X_1 + R_2 X_2)}{(R_1 + R_2)^2}}, \quad (15)$$

$$X_3 = -\frac{R_1 X_2 + R_2 X_1}{R_1 + R_2}. \quad (16)$$

This result provides the value of Z_a corresponding to the given transistor size.

3.4.3. Matching Network Design Based on Z_a

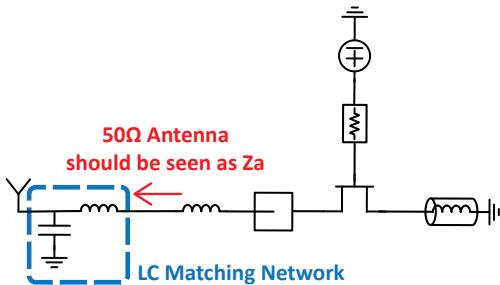


Figure 10. LC matching network to make the 50Ω antenna appear as Z_a .

Based on the previously derived expressions, the value of Z_a was calculated for a transistor size of $200\mu\text{m}$. Using this Z_a , the required LC values were derived to transform

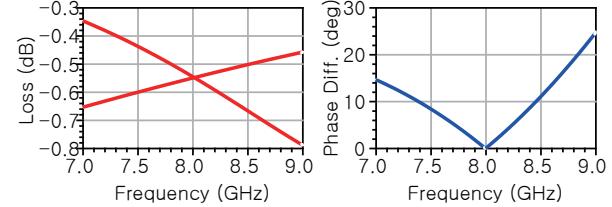


Figure 11. Simulation results with LC matching: Perfect switch at 8 GHz.

a 50Ω antenna impedance into Z_a , and the corresponding matching network was implemented as shown in Fig. 10.

The simulation results, presented in Fig. 11, confirm that the designed network achieves equal reflection magnitude and an exact 180° phase difference at 8 GHz, thus realizing a perfect switch.

At this stage, it became evident that a perfect switch could be achieved for any given transistor size by appropriately designing the matching network. With this methodology in hand, the focus was shifted toward finding the optimal transistor size—one that minimizes loss while maintaining a 180° phase difference over a wide bandwidth.

3.5. Transistor Sizing Methodology

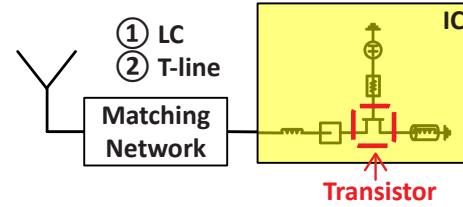


Figure 12. Transistor sizing under two different matching network techniques.

To evaluate the optimal transistor size that ensures low loss and a consistent 180° phase difference across a wide frequency range, two types of matching network implementations are considered: LC matching network and transmission line (T-line) matching network. The analysis is conducted separately for each matching technique to determine the most suitable transistor size as illustrated in Fig. 12.

3.5.1. LC Matching Network

The transistor size (TR size) is defined as the product of unit gate width (UGW) and number of fingers (NOF):

$$\text{TR size} = \text{UGW} \times \text{NOF}. \quad (17)$$

Once the TR size is determined, the corresponding Z_a is uniquely defined. Then, the 50Ω antenna must be transformed to the Z_a on the Smith chart using a matching network. The required values of L and C can then be obtained by mathematically solving the impedance transformation.

3.5.2. T-Line Matching Network

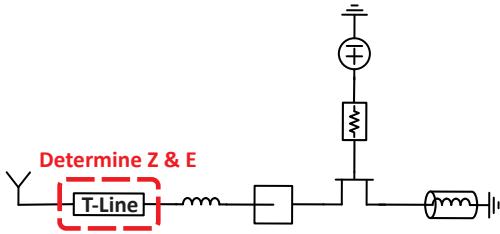


Figure 13. T-line matching network and determination of Z and E .

For T-line-based matching, the key parameters to determine are the characteristic impedance Z and electric length E of the transmission line, as illustrated in Fig. 13.

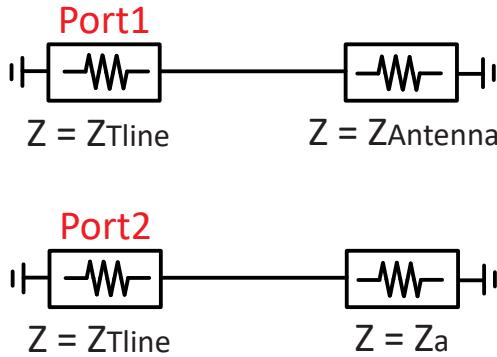


Figure 14. T-line tuning setup.

To determine the appropriate characteristic impedance Z_{Tline} , a tuning procedure was performed as shown in Fig. 14. In this setup, both Port 1 and Port 2 are assigned a transmission line impedance Z_{Tline} , while their respective opposite terminals are terminated with the antenna impedance $Z_{Antenna}$ and Z_a .

By tuning Z_{Tline} to equalize $S(1,1)$ and $S(2,2)$ (as shown in Fig. 15), the optimal characteristic impedance was obtained. Then, the angle between the two impedance points on the Smith chart was halved to determine the electric length.

4. Experiments

4.1. Transistor Size Selection

4.1.1. Performance with LC Matching

As previously mentioned in equation (17), the TR size is defined as the product of UGW and NOF. In this research, NOF was fixed to 4, and UGW was varied to evaluate five TR size candidates ranging from $200\mu\text{m}$ to $600\mu\text{m}$.

The corresponding values of Z_a (R_3 , X_3) and the LC components for each matching network are summarized in

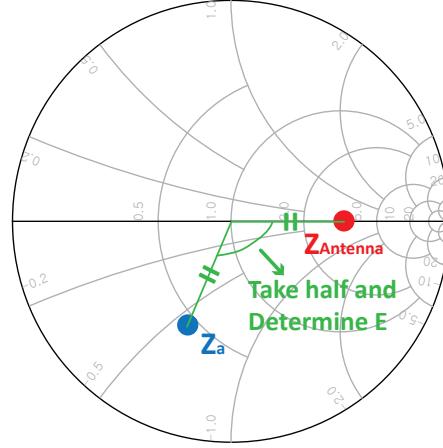


Figure 15. Equalizing reflection coefficients and extracting electric length.

UGW	NOF	TR size	R_3	X_3	C_shunt	L_series	C_series	C_shunt
50	4	200	0.853	0.043	0.165	0.396	-	-
75	4	300	0.618	-0.280	0.313	0.205	-	-
100	4	400	0.473	-0.471	0.420	0.028	-	-
125	4	500	0.383	-0.592	-	-	0.731	0.307
150	4	600	0.323	-0.672	-	-	0.468	0.285

Table 1. Za and LC values for each transistor sizes.

Table 1. Based on these values, LC matching networks were constructed for each case, and their switching performance was evaluated in terms of ON/OFF state loss and phase difference, as shown in Fig. 16.

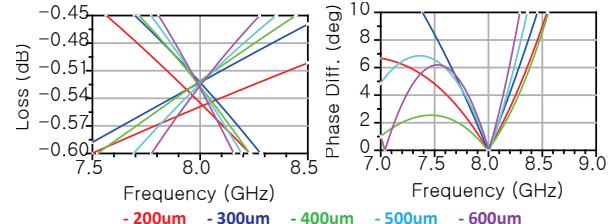


Figure 16. LC matching performance across TR size candidates.

The results indicate that the TR size of $400\mu\text{m}$ yields the lowest insertion loss and, more importantly, the widest bandwidth over which the 180° phase difference is maintained. Hence, for LC-based matching, $400\mu\text{m}$ is selected as the optimal TR size.

4.1.2. Performance with T-Line Matching

The resulting values of Z_a and corresponding Z and E for each TR size are listed in Table 2. But for TR sizes of $500\mu\text{m}$ and $600\mu\text{m}$, Z_a lies too far, making single T-line matching infeasible (as shown in Fig. 17).

Thus, for the feasible TR sizes (200, 300, and $400\mu\text{m}$), T-line matching networks were implemented using values from Table 2. Performance comparison in Fig. 18 shows

UGW	NOF	TR size	R3	X3	Za Tline	E_Tline
50	4	200	0.853	0.043	0.165	0.396
75	4	300	0.618	-0.280	0.313	0.205
100	4	400	0.473	-0.471	0.420	0.028
125	4	500	0.383	-0.592	-	-
150	4	600	0.323	-0.672	-	-

Table 2. Za and T-line values for each transistor sizes.

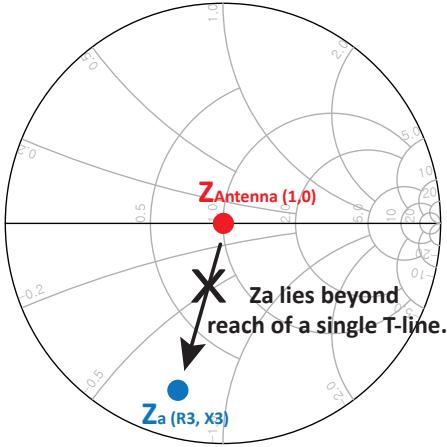


Figure 17. Matching infeasibility for large TR sizes with T-line matching.

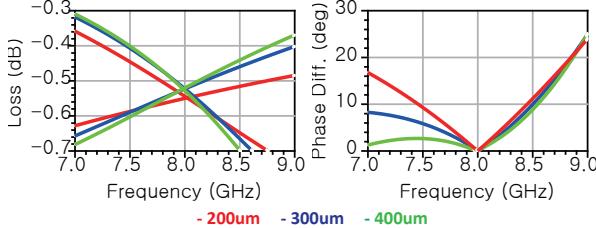


Figure 18. T-line matching performance across TR size candidates.

that the $400 \mu\text{m}$ TR size again provides the best results in terms of low loss and wide 180° phase bandwidth. Therefore, $400 \mu\text{m}$ is also the optimal TR size for T-line matching network.

4.1.3. LC vs. T-Line at $400 \mu\text{m}$

Both LC and T-line matching methods identify $400 \mu\text{m}$ as the optimal transistor size. Therefore, a direct comparison between the two approaches was conducted using the same TR size.

As shown in Fig. 19, the performance of both matching techniques is nearly identical. This observation is attributed to the equivalence between a T-line and a series-L/shunt-C configuration, as illustrated in Fig. 20.

However, from a practical design perspective, implementing precise L and C values (in Table 1) in hardware is challenging. On the other hand, the T-line with the $400 \mu\text{m}$

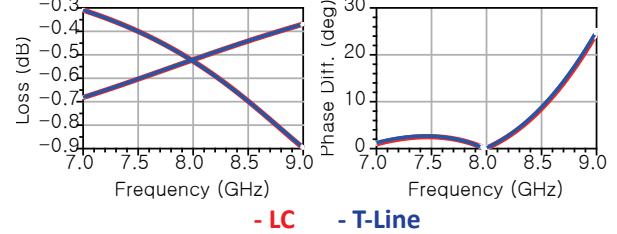


Figure 19. Performance comparison between LC and T-line matching at $400 \mu\text{m}$.

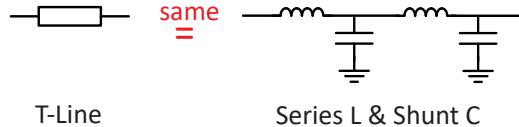


Figure 20. Equivalence between T-line and LC matching networks.

requires a short electric length (0.028), making the design more compact and robust.

Consequently, the $400 \mu\text{m}$ TR size with T-line matching is concluded to be the optimal configuration in terms of both electrical performance and design simplicity.

4.2. Layout

Fig. 21 shows the schematic and corresponding layout of the finalized switch module. A notable point is that the transistor is designed with four gate fingers, which can be observed in the layout. The GaAs HEMT is connected in parallel with multiple back vias to ground to reduce inductive effects. The DC feed line delivers the gate bias while isolating RF signals from the DC path. It is designed to behave as an open circuit to RF signals and as a short circuit to DC. While an inductor could easily implement this function, its required size was impractically large relative to the circuit, so a resistor was used instead.

After completing the layout of the individual switch module, eight switches were integrated into a 16-lead QFN package as shown in Fig. 22. Two switches are connected to a single antenna unit to enable dual polarization operation—one for each polarization. To minimize inductive effects, the bond wires connected to the RF pads were kept as short as possible, since bond wires inherently behave as inductive elements. Therefore, the switch was positioned as close as possible and perpendicular to the RF pads to ensure the shortest wire length for vertical bonding.

Fig. 23 presents the overall appearance of the final IC packaged in a 16-lead QFN for use in the RIS system.

4.3. Next Step: Broadband Matching

The switch implemented in this research was designed for single-frequency operation at 8 GHz. As a next step, the

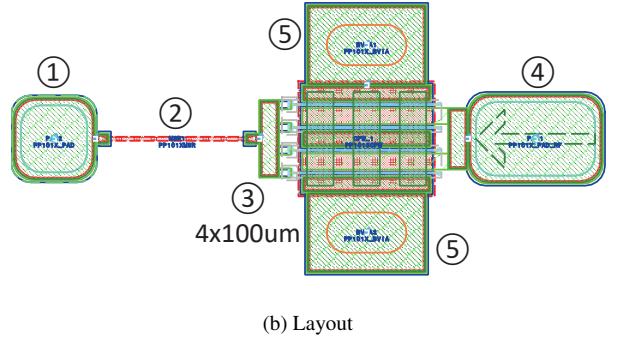
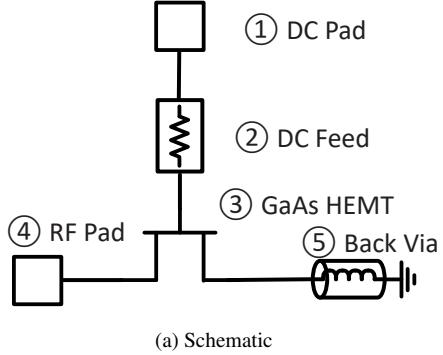


Figure 21. Schematic and layout of the finalized switch module.

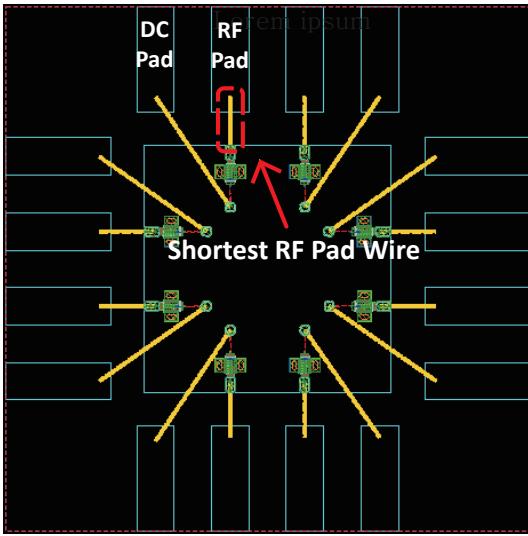


Figure 22. Integration of switch modules into a 16-lead QFN package.

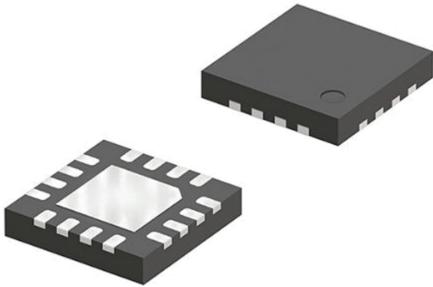


Figure 23. Final IC packaged in a 16-lead QFN for dual-polarized RIS.

goal is to extend its functionality over a wider frequency range by developing a broadband matching.

One possible approach is to design a matching network such that the trajectory of the antenna impedance trans-

formed by the matching network exactly follows the **natural trajectory of Z_a** as frequency varies. If these two trajectories are identical on the Smith chart, broadband matching can theoretically be achieved over the corresponding frequency range.

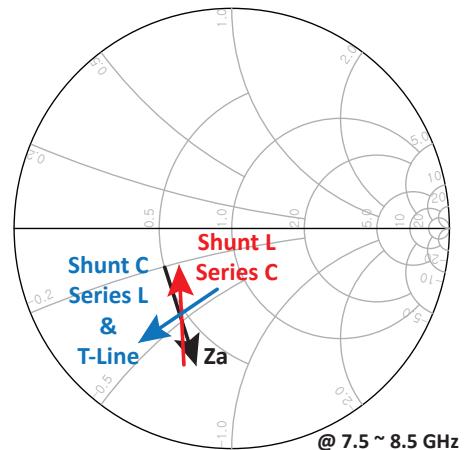


Figure 24. Mismatch between Z_a and matching network trajectories.

Fig. 24 illustrates the trajectory of Z_a and the impedance transformation paths of different matching networks in the 7.5 – 8.5 GHz frequency range. It is evident that the two trajectories do not align. This discrepancy arises from a fundamental limitation: as frequency increases, the electric length of the matching network also increases, inherently rotating the transformed impedance clockwise on the Smith chart.

Secondly, the performance of the final configuration—400 μm TR size with T-line matching—was evaluated across a wider frequency range, as shown in Fig. 25. The results indicate that the insertion loss remains below 1 dB over a broad range, and the phase difference remains acceptable from approximately 6.5 to 8.5 GHz. While perfect matching at all frequencies may not be achievable,

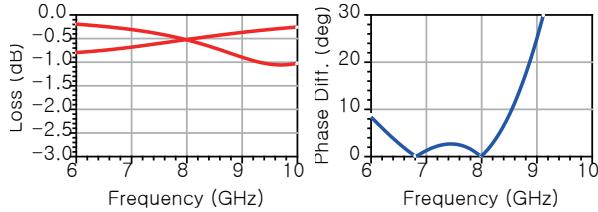


Figure 25. Performance of the finalized configuration over a wider frequency range.

the results suggest that by designing the matching network based on a target frequency within the desired range, it is possible to implement a switch with roughly broadband characteristics over that range.

5. Conclusion

This study presented the design and analysis of a 1-bit GaAs HEMT-based phase shifting switch module optimized for operation at 8 GHz. Through systematic evaluation of various transistor sizes and matching strategies, it was confirmed that a TR size of $400\ \mu\text{m}$ combined with T-line matching yields the best performance in terms of insertion loss and phase balance.

The proposed methodology is not limited to this specific case. If the bond wire inductance or other physical parameters were to change, the same design framework could be applied to determine a new optimal TR size and matching network configuration accordingly.

In addition, if broadband matching can be achieved, the switch module could operate over a wider frequency range, further enhancing its applicability to RIS (Reconfigurable Intelligent Surface) systems.

6. Reference

References

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