MEMORY UPGRADE MODULE SPECIFICATIONS
Revision 1.1

12MB, 16MB, 24MB, 28MB

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Trademarks:

Date : 4 February, 1997

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CONTACT INFORMATION

For documents relating to the Memory Upgrade Module specification, you can contact Creative at
avp_memory@ctlsg.creaf.com

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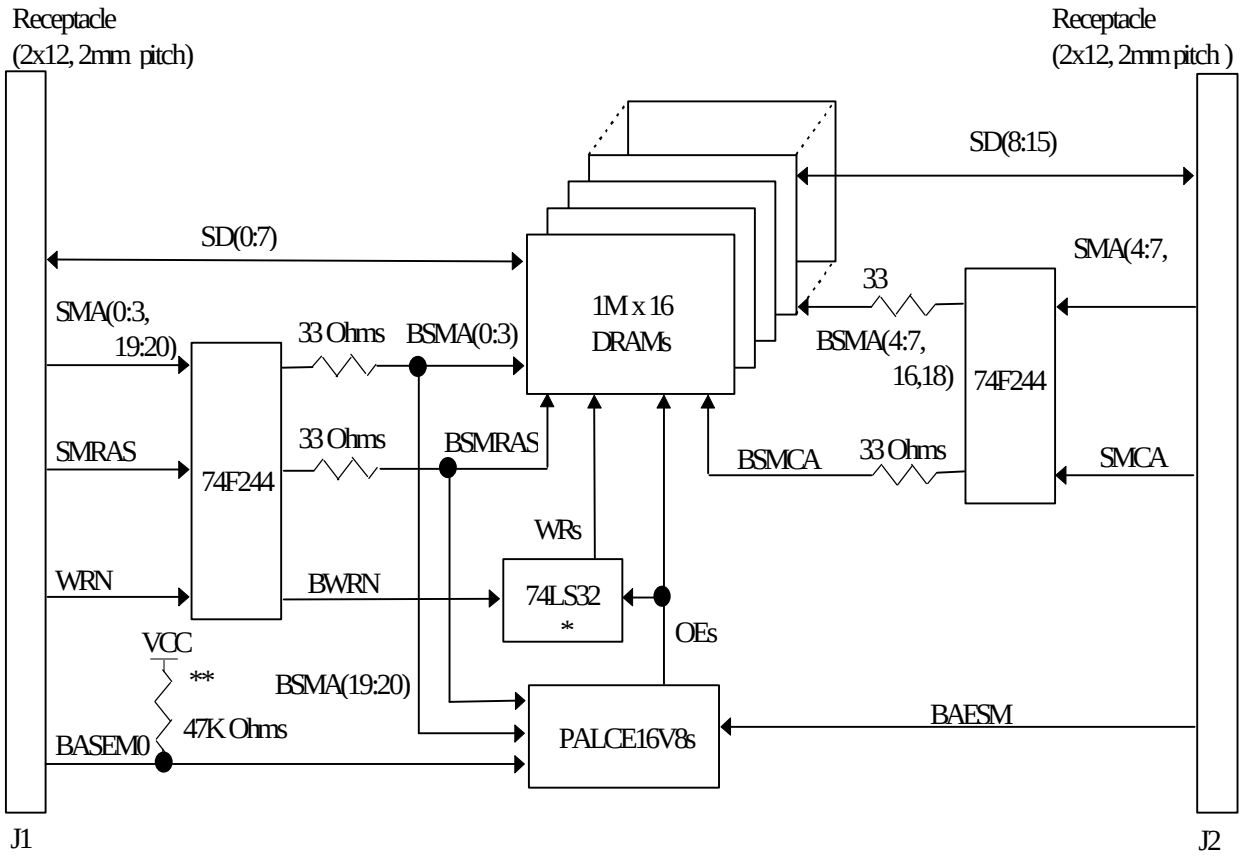
2.0 Introduction

The memory upgrade module is designed to plug onto AWE64 range of products. Its function is to provide more local memory space for the sound card to download wavetable samples (SoundFonts). It comes in the following configurations:
a) 12MB version

b) 16MB version
c) 24MB version
d) 28MB version

3.0 Functional Block Diagram



* 74LS32 logic can be integrated into PLD

** If the PLD used do not support internal pull-up for BASEM0, a pull-up resistor of 47Kohms is required.

4.0 Circuit Description

(Refer to the Block Diagram)

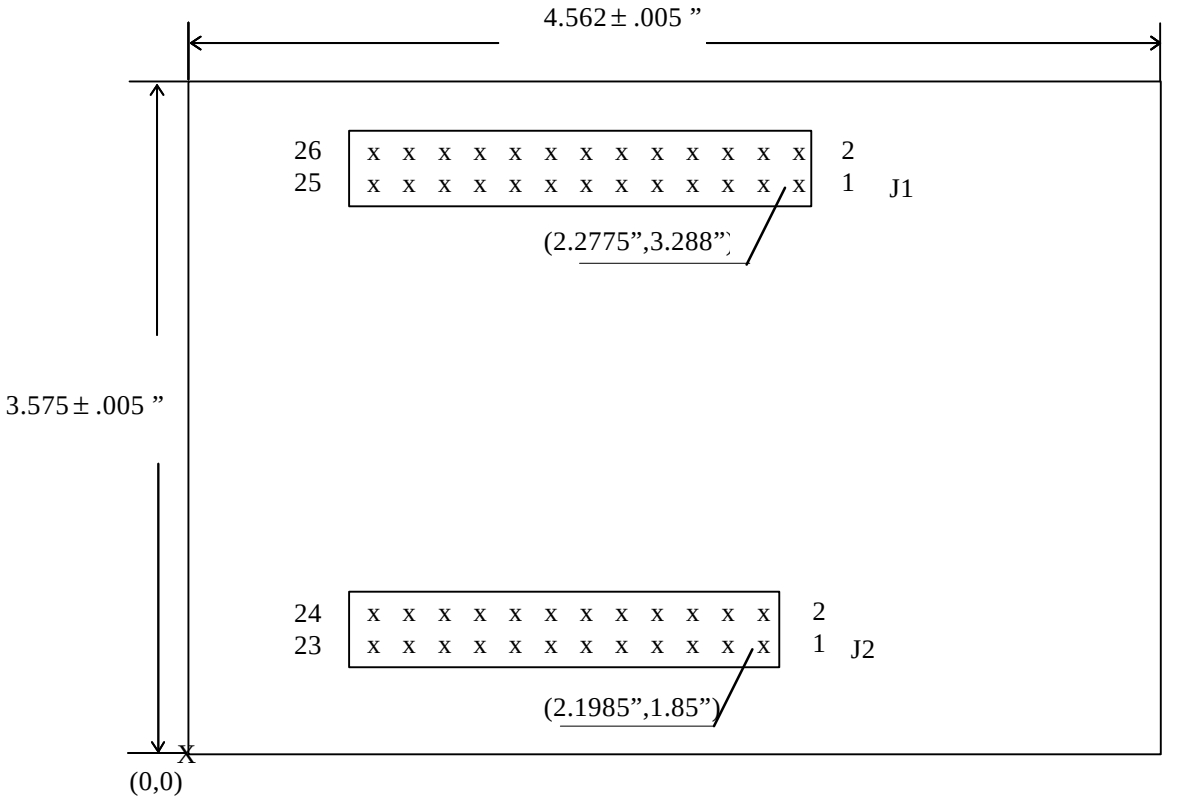
The design is based on EMU8000 and 1M x 16 DRAM (at least 60ns access time). The data and control signals (BSMRAS, BSMCAS) connection is straight forward, that is, direct from the receptacles to the respective signal lines of the DRAMs. The address lines are slightly complicated and are connected in the following order : BSMA(0:7), BSMA(16), BSMA(18) from the receptacle to A0-A9 of the DRAM. This does the basic decoding within the 1M x 16 DRAM.

In order to differentiate from each of the DRAMs, PALs(PALCE16V8) are used to decode the high addresses BSMA(19:20) further. The decoded signals control the respective WR and OE for each of the DRAM to enable reading and writing. In this particular design , a maximum of 14M Words are supported.

At the same time, the PAL also decodes “BASEM0” and “BAESM1” to determine the size of the downloadable DRAM on the sound card. In other words, if both “BASEM0” and “BASEM1” are found to be ‘HIGH’, the small DRAM on the sound card is ignored, and address of the memory module starts from location 0; whereas for the other 3 combinations, the size of the sound card DRAM is determined, and the memory module offsets from the address accordingly. Please look under ‘Connector Pin Assignment’ for detailed information.*Note : If the PLD used do not support internal pull-up for BASEM0, a pull-up resistor of 47KW is required.*

To minimise capacitive loading seen by EMU8000, a 74F244 buffer with 33ohm damping resistor at the output is needed on the address and control signals.

5.0 Profile of the board layout



Solder side of receptacles

Notes:

1. The above shows the board size and locations of some critical components recommended.
2. The dimension in bracket shows the centre location of pin 1 of each of the receptacle with reference to (0,0).
3. The height of the receptacle, J1 and J2 should be 6.73 mm minimum.
4. The relative location of the receptacle, J1 and J2, must comply to the above.
5. Components (DRAMs, capacitors, PLDs, and resistors) shall be mounted on solder side of the receptacles.

6.0 Connector Pin Assignment

2 x 12 Receptacle(J1)

Pin No.	Signal	Descriptions
	Address lines	To be buffered through a 74F244 with 33ohm damping resistor a output before connecting to DRAM or PAL.
8	SMA(0)	connect to address 0 of DRAM.
5	SMA(1)	connect to address 1 of DRAM.
6	SMA(2)	connect to address 2 of DRAM.
3	SMA(3)	connect to address 3 of DRAM.
7	SMA(19)	connect to PAL for further address decoding.
4	SMA(20)	connect to PAL for further address decoding.
	Data lines	No buffering is needed.
21	SD(0)	connect to data 0 of DRAM.
22	SD(1)	connect to data 1 of DRAM.
19	SD(2)	connect to data 2 of DRAM.
20	SD(3)	connect to data 3 of DRAM.
17	SD(4)	connect to data 4 of DRAM.
18	SD(5)	connect to data 5 of DRAM.
15	SD(6)	connect to data 6 of DRAM.
16	SD(7)	connect to data 7 of DRAM.
	Control lines	
11	WRN	Write signal. To be buffered through a 74F244 with 33ohm damping resistor a the output before connecting to 74LS32 to generate respective DRAM write signal.
12	SMRAS	Row Access Signal. To be buffered through a 74F244 with 33ohm damping resistor a the output before connecting to DRAM and PAL.
1	BASEM0	BASEM0 and BASEM1 will determine the amount of DRAM available on the sound card.
	Others	
2, 23,24	VCC	+5V Supply
9,10, 13,14	GND	Ground

6.0 Connector Pin Assignment (cont'd)

2 x 13 Receptacle (J2)

Pin no.	Signal	Descriptions
	Address lines	To be buffered through a 74F244 with 33ohm damping resistor a the output before connecting to DRAM or PAL.
3	SMA(4)	connect to address 4 of DRAM.
6	SMA(5)	connect to address 5 of DRAM.
5	SMA(6)	connect to address 6 of DRAM.
8	SMA(7)	connect to address 7 of DRAM.
7	SMA(16)	connect to address 8 of DRAM.
4	SMA(18)	connect to address 9 of DRAM.
	Data lines	No buffering is needed.
18	SD(8)	connect to data 8 of DRAM.
17	SD(9)	connect to data 9 of DRAM.
20	SD(10)	connect to data 10 of DRAM.
19	SD(11)	connect to data 11 of DRAM.
22	SD(12)	connect to data 12 of DRAM.
21	SD(13)	connect to data 13 of DRAM.
24	SD(14)	connect to data 14 of DRAM.
23	SD(15)	connect to data 15 of DRAM.
	Control lines	
13	SMCAS	Column Access Signal. To be buffered through a 74F244 with 33ohm damping resistor a the output before connecting to DRAM.
14	BASEM1	BASEM1 and BASEM0 will determine the amount of DRAM available on the sound card. This will in turn offset the address o the DRAM on the memory module. BASEM1 BASEM0 0 0 8MB 0 1 4MB 1 0 2MB 1 1 0MB
	Others	
1,2, 25,26	VCC	+5V Supply
9-12, 15,16	GND	Ground

7.0 PAL equations

```
; PALASM Design Description
; Copyright (c) CREATIVE TECHNOLOGY PTE LTD 1996
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;---------------------------------- Declaration Segment ------------
TITLE         MEMORY  UPGRADE MODULE
PATTERN       MEM1.PDS
REVISION      A
AUTHOR        CREATIVE TECHNOLOGY LTD.
COMPANY       CREATIVE TECHNOLOGY LTD.
DATE          9/01/97
CHIP          MEM1 PALCE16V8
;---------------------------------- PIN Declarations ---------------
;INPUT
PIN  1        CLK
PIN  11       /OE

PIN  2        BSMRAS
PIN  3        BSMA19
PIN  4        BSMA20
PIN  5        BASEM1
PIN  7        BASEM0

;OUTPUT
PIN  12       A23     REG
PIN  13       A21     REG
PIN  14       OE_8MN
PIN  15       OE_6MN
PIN  16       OE_4MN
PIN  17       OE_2MN
PIN  19       RASB

;POWER
PIN  10       GND
PIN  20       VCC

;---------------------------------- Boolean Equation Segment ------
EQUATIONS

/RASB = BSMRAS

A23 = BSMA19
A23.CLKF = CLK

A21 = BSMA20
A21.CLKF = CLK

OE_2MN = (A23 + BSMA19 + /A21 + BSMA20 + /BASEM1 + /BASEM0)
      * (A23 + BSMA19 + /A21 + /BSMA20 + /BASEM1 + BASEM0)
      * (A23 + /BSMA19 + A21 + BSMA20 + BASEM1 + /BASEM0)
      * (A23 + /BSMA19 + /A21 + BSMA20 + BASEM1 + BASEM0)

OE_4MN = (A23 + BSMA19 + /A21 + /BSMA20 + /BASEM1 + /BASEM0)
      * (A23 + /BSMA19 + A21 + BSMA20 + /BASEM1 + BASEM0)
      * (A23 + /BSMA19 + A21 + /BSMA20 + BASEM1 + /BASEM0)
      * (A23 + /BSMA19 + /A21 + /BSMA20 + BASEM1 + BASEM0)
```

7.0 PAL equations (cont'd)

OE_6MN = (A23 + /BSMA19 + A21 + BSMA20 + /BASEM1 + /BASEM0)
* (A23 + /BSMA19 + A21 + /BSMA20 + /BASEM1 + BASEM0)
* (A23 + /BSMA19 + /A21 + BSMA20 + BASEM1 + /BASEM0)
* (/A23 + BSMA19 + A21 + BSMA20 + BASEM1 + BASEM0)

OE_8MN = (A23 + /BSMA19 + A21 + /BSMA20 + /BASEM1 + /BASEM0)
* (A23 + /BSMA19 + /A21 + BSMA20 + /BASEM1 + BASEM0)
* (A23 + /BSMA19 + /A21 + /BSMA20 + BASEM1 + /BASEM0)
* (/A23 + BSMA19 + A21 + /BSMA20 + BASEM1 + BASEM0)

7.0 PAL equations (cont'd)

```
; PALASM Design Description
; Copyright (c) CREATIVE TECHNOLOGY PTE LTD 1996
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;---------------------------------- Declaration Segment ------------
TITLE         MEMORY  UPGRADE MODULE
PATTERN     MEM2.PDS
REVISION    A
AUTHOR      CREATIVE TECHNOLOGY LTD.
COMPANY    CREATIVE TECHNOLOGY LTD.
DATE          20/1/97
CHIP           MEM2 PALCE16V8
;---------------------------------- PIN Declarations ---------------
;INPUT
PIN  1        A23
PIN  2        A21
PIN  3        BSMA19
PIN  4        BSMA20
PIN  5        BASEM1
PIN  6        BWRN
PIN  7        BASEM0
PIN  8        NC
PIN  9        NC
PIN  11       /OE

;OUTPUT
PIN  12       WR_14MN
PIN  13       OE_14MN
PIN  14       WR_16MN
PIN  15       OE_16MN
PIN  16       WR_10MN
PIN  17       OE_10MN
PIN  18       OE_12MN
PIN  19       WR_12MN

;POWER
PIN  10       GND
PIN  20       VCC
;----------------------------------- Boolean Equation Segment ------
EQUATIONS

OE_10MN = (A23 + /BSMA19 + /A21 + BSMA20 + /BASEM1 + /BASEM0)
      * (A23 + /BSMA19 + /A21 + /BSMA20 + /BASEM1 + BASEM0)
      * (/A23 + BSMA19 + A21 + BSMA20 + BASEM1 + /BASEM0)
      * (/A23 + BSMA19 + /A21 + BSMA20 + BASEM1 + BASEM0)

WR_10MN = BWRN + OE_10MN

OE_12MN = (A23 + /BSMA19 + /A21 + /BSMA20 + /BASEM1 + /BASEM0)
      * (/A23 + BSMA19 + A21 + BSMA20 + /BASEM1 + BASEM0)
      * (/A23 + BSMA19 + A21 + /BSMA20 + BASEM1 + /BASEM0)
      * (/A23 + BSMA19 + /A21 + /BSMA20 + BASEM1 + BASEM0)

WR_12MN = BWRN + OE_12MN
```

7.0 PAL equations (cont'd)

OE_14MN = (/A23 + BSMA19 + A21 + BSMA20 + /BASEM1 + /BASEM0)
* (/A23 + BSMA19 + A21 + /BSMA20 + /BASEM1 + BASEM0)
* (/A23 + BSMA19 + /A21 + BSMA20 + BASEM1 + /BASEM0)
* (/A23 + /BSMA19 + A21 + BSMA20 + BASEM1 + BASEM0)

WR_14MN = BWRN + OE_14MN

OE_16MN = (/A23 + BSMA19 + A21 + /BSMA20 + /BASEM1 + /BASEM0)
* (/A23 + BSMA19 + /A21 + BSMA20 + /BASEM1 + BASEM0)
* (/A23 + BSMA19 + /A21 + /BSMA20 + BASEM1 + /BASEM0)
* (/A23 + /BSMA19 + A21 + /BSMA20 + BASEM1 + BASEM0)

WR_16MN = BWRN + OE_16MN

7.0 PAL equations (cont'd)

```
; PALASM Design Description
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;---------------------------------- Declaration Segment ------------
TITLE         MEMORY  UPGRADE MODULE
PATTERN       MEM3.PDS
REVISION      A
AUTHOR        CREATIVE TECHNOLOGY LTD.
COMPANY       CREATIVE TECHNOLOGY LTD.
DATE          20/1/97
CHIP          MEM3 PALCE16V8
;---------------------------------- PIN Declarations ---------------
;INPUT
PIN  1        A23
PIN  2        A21
PIN  3        BSMA19
PIN  4        BSMA20
PIN  5        BASEM1
PIN  6        BWRN
PIN  7        BASEM0
PIN  8        NC
PIN  9        NC
PIN  11       /OE

;OUTPUT
PIN  12       WR_18MN
PIN  13       OE_18MN
PIN  14       WR_22MN
PIN  15       OE_22MN
PIN  16       WR_20MN
PIN  17       OE_20MN
PIN  18       OE_24MN
PIN  19       WR_24MN

;POWER
PIN  10       GND
PIN  20       VCC
;---------------------------------- Boolean Equation Segment ------
EQUATIONS

OE_18MN = (/A23 + BSMA19 + /A21 + BSMA20 + /BASEM1 + /BASEM0)
      * (/A23 + BSMA19 + /A21 + /BSMA20 + /BASEM1 + BASEM0)
      * (/A23 + /BSMA19 + A21 + BSMA20 + BASEM1 + /BASEM0)
      * (/A23 + /BSMA19 + /A21 + BSMA20 + BASEM1 + BASEM0)

WR_18MN = BWRN + OE_18MN

OE_20MN = (/A23 + BSMA19 + /A21 + /BSMA20 + /BASEM1 + /BASEM0)
      * (/A23 + /BSMA19 + A21 + BSMA20 + /BASEM1 + BASEM0)
      * (/A23 + /BSMA19 + A21 + /BSMA20 + BASEM1 + /BASEM0)
      * (/A23 + /BSMA19 + /A21 + /BSMA20 + BASEM1 + BASEM0)

WR_20MN = BWRN + OE_20MN
```

7.0 PAL equations (cont'd)

OE_22MN = (/A23 + /BSMA19 + A21 + BSMA20 + /BASEM1 + /BASEM0)
* (/A23 + /BSMA19 + A21 + /BSMA20 + /BASEM1 + BASEM0)
* (/A23 + /BSMA19 + /A21 + BSMA20 + BASEM1 + /BASEM0)

WR_22MN = BWRN + OE_22MN

OE_24MN = (/A23 + /SMA19 + A21 + /BSMA20 + /BASEM1 + /BASEM0)
* (/A23 + /SMA19 + /A21 + BSMA20 + /BASEM1 + BASEM0)
* (/A23 + /SMA19 + /A21 + /BSMA20 + BASEM1 + /BASEM0)

WR_24MN = BWRN + OE_24MN

7.0 PAL equations (cont'd)

```
; PALASM Design Description
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;---------------------------------- Declaration Segment ------------
TITLE         MEMORY  UPGRADE MODULE
PATTERN     MEM4.PDS
REVISION    A
AUTHOR      CREATIVE TECHNOLOGY LTD.
COMPANY    CREATIVE TECHNOLOGY LTD.
DATE          20/1/97
CHIP           MEM4 PALCE16V8
;---------------------------------- PIN Declarations ---------------
;INPUT
PIN  1        A23
PIN  2        A21
PIN  3        BSMA19
PIN  4        BSMA20
PIN  5        BASEM1
PIN  6        BWRN
PIN  7        BASEM0
PIN  8        NC
PIN  9        NC
PIN  11       /OE

;OUTPUT
PIN  12       WR_26MN
PIN  13       OE_26MN
PIN  14       WR_28MN
PIN  15       OE_28MN

;POWER
PIN  10       GND
PIN  20       VCC

;---------------------------------- Boolean Equation Segment ------
EQUATIONS

OE_26MN = (/A23 + /BSMA19 + /A21 + BSMA20 + /BASEM1 + /BASEM0)
      * (/A23 + /BSMA19 + /A21 + /BSMA20 + /BASEM1 + BASEM0)

WR_26MN = BWRN + OE_26MN

OE_28MN = (/A23 + /BSMA19 + /A21 + /BSMA20 + /BASEM1 + /BASEM0)

WR_28MN = BWRN + OE_28MN
```

8.0 Bill of Materials

For the 12MB version:

	Descriptions	Quantity	Approved Vendor
1.	1M x 16 DRAM (at least 60ns access time)	6	
2.	74F244	2	
3.	74LS32	1	
4.	PALCE 16V8-15	2	
5.	Post Header Receptacle 2mm Pitch, 2 x 12 ways	1	Astron Technology Corp.*
6.	Post Header Receptacle 2mm Pitch, 2 x 13 ways	1	Astron Technology Corp.
7.	Resistor array, 33 ohm x4 (isolated)	4	
8.	Decoupling capacitor, 0.1uF	15	

For the 16MB version:

	Descriptions	Quantity	Approved Vendor
1.	1M x 16 DRAM (at least 60ns access time)	8	
2.	74F244	2	
3.	74LS32	1	
4.	PALCE 16V8-15	2	
5.	Post Header Receptacle 2mm Pitch, 2 x 12 ways	1	Astron Technology Corp.
6.	Post Header Receptacle 2mm Pitch, 2 x 13 ways	1	Astron Technology Corp.
7.	Resistor array, 33 ohm x4 (isolated)	4	
8.	Decoupling capacitor, 0.1uF	19	

For the 24MB version:

	Descriptions	Quantity	Approved Vendor
1.	1M x 16 DRAM (at least 60ns access time)	12	
2.	74F244	2	
3.	74LS32	1	
4.	PALCE 16V8-15	3	
5.	Post Header Receptacle 2mm Pitch, 2 x 12 ways	1	Astron Technology Corp.
6.	Post Header Receptacle 2mm Pitch, 2 x 13 ways	1	Astron Technology Corp.
7.	Resistor array, 33 ohm x4 (isolated)	4	
8.	Decoupling capacitor, 0.1uF	28	

For the 28MB version:

	Descriptions	Quantity	Approved Vendor
1.	1M x 16 DRAM (at least 60ns access time)	14	
2.	74F244	2	
3.	74LS32	1	
4.	PALCE 16V8-15	4	
5.	Post Header Receptacle 2mm Pitch, 2 x 12 ways	1	Astron Technology Corp.
6.	Post Header Receptacle 2mm Pitch, 2 x 13 ways	1	Astron Technology Corp.
7.	Resistor array, 33 ohm x4 (isolated)	4	
8.	Decoupling capacitor, 0.1uF	33	

* Astron part number for J1 use by Creative is “AT-PHR21-24-2-0-15G”
Astron part number for J2 use by Creative is “AT-PHR21-26-2-0-15G”

8.0 Bill of Materials (cont'd)

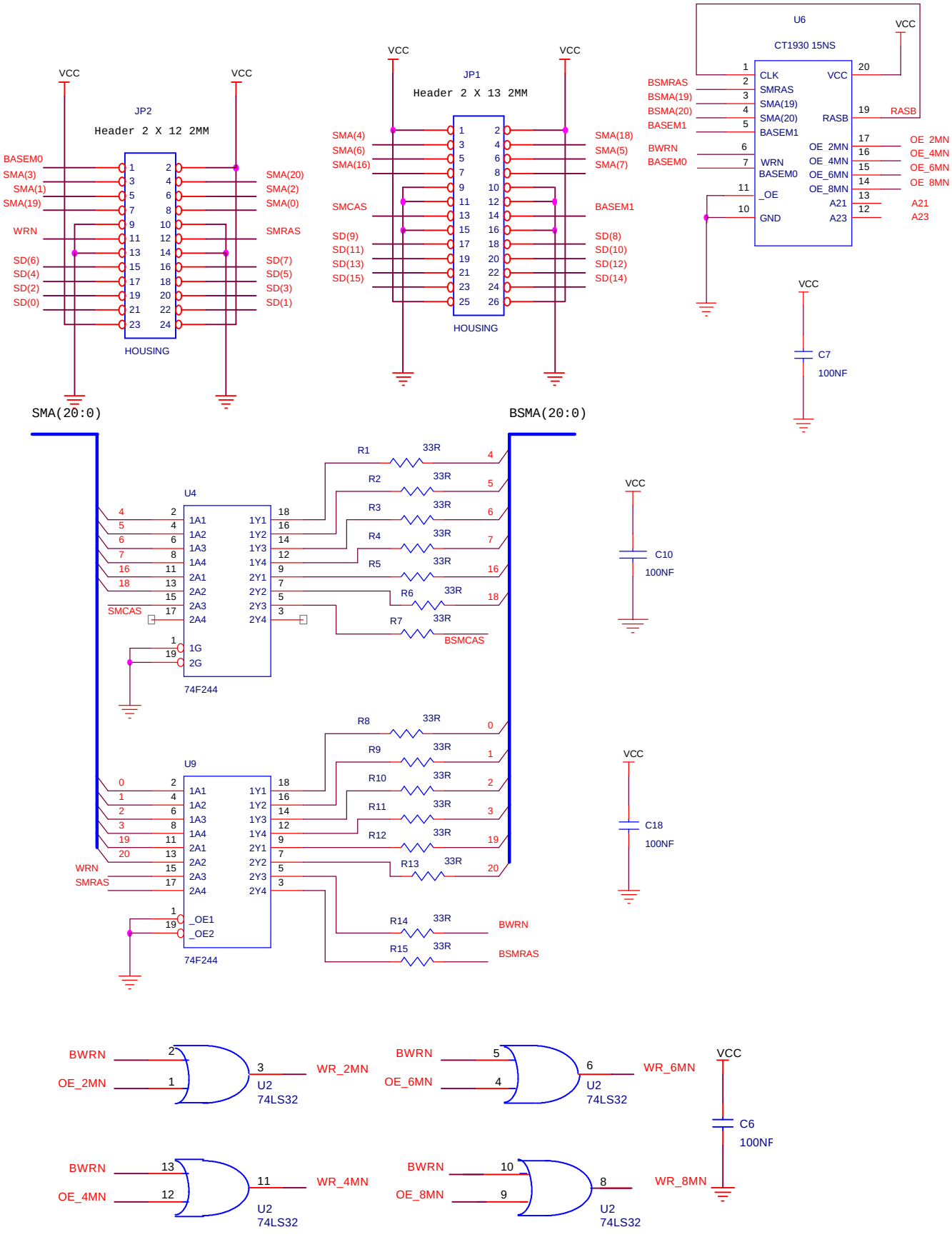
For more information on the receptacles, please refer to:

Astron-A.t. Corporation
774 Charcot Avenue
San Jose CA 95131
Tel : 408-232-1100
Fax : 408-232-1108

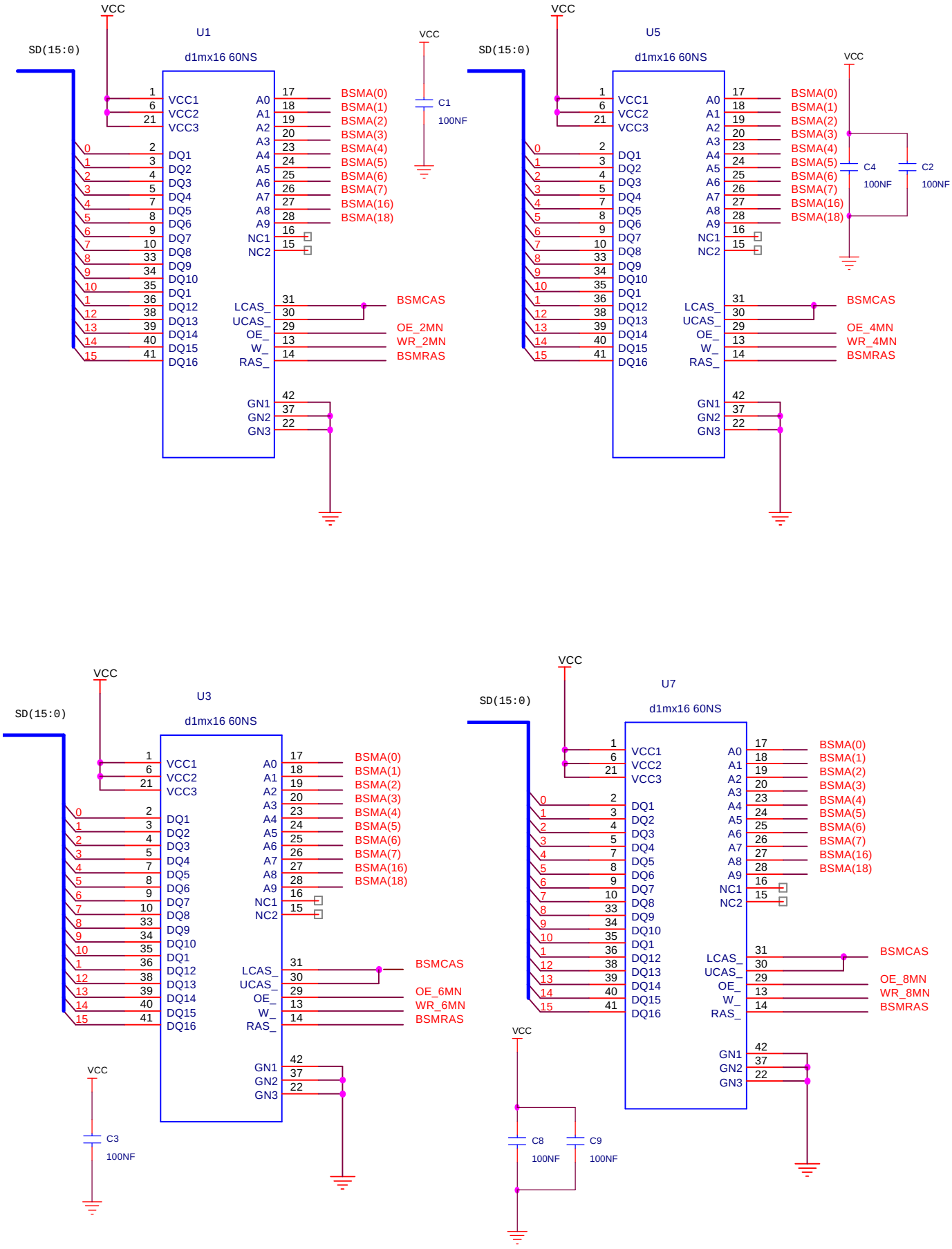
Astron Technology Corporation
6F, No.23, Wu-Kung 6 Road
Wu-Ku Ind Park
Taipei Hsien
Taiwan, R.O.C.
Tel : 886-2-299-0885
Fax : 886-2-298-8757

Remarks : It is found that some manufacturers' receptacles may have contact issues.

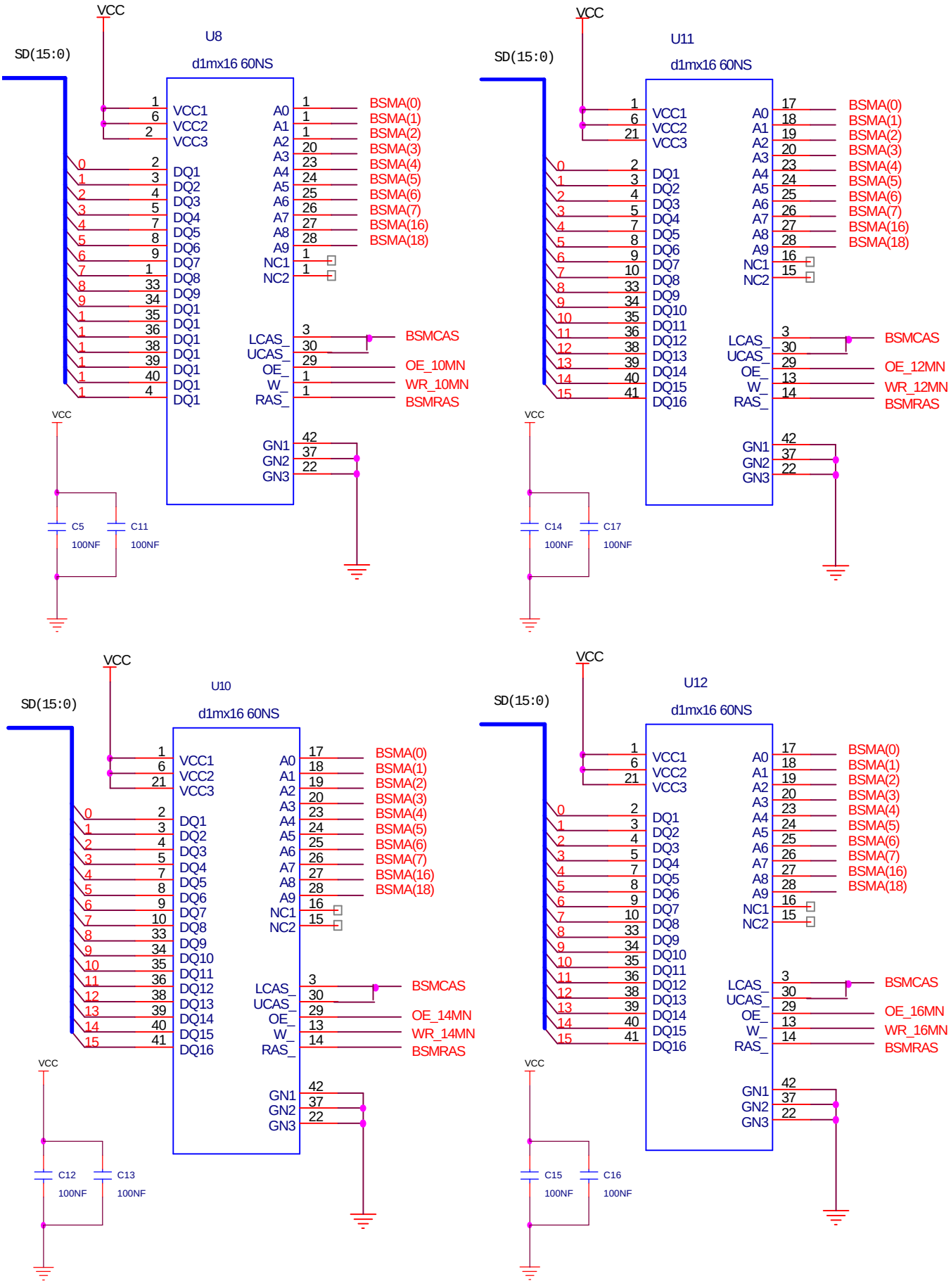
SCHEMATICS for the Memory Upgrade Module.



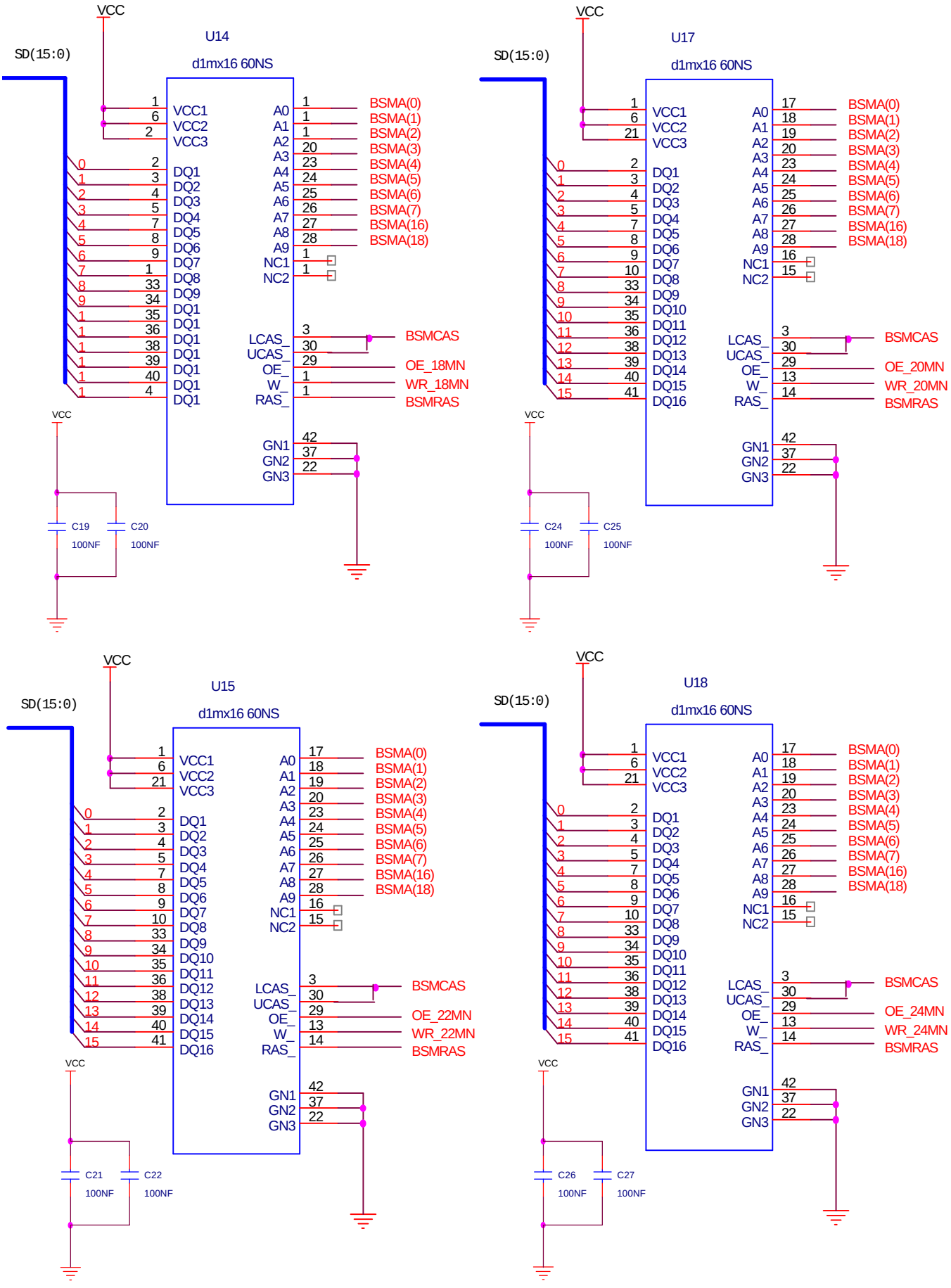
Date : 4 February, 1997



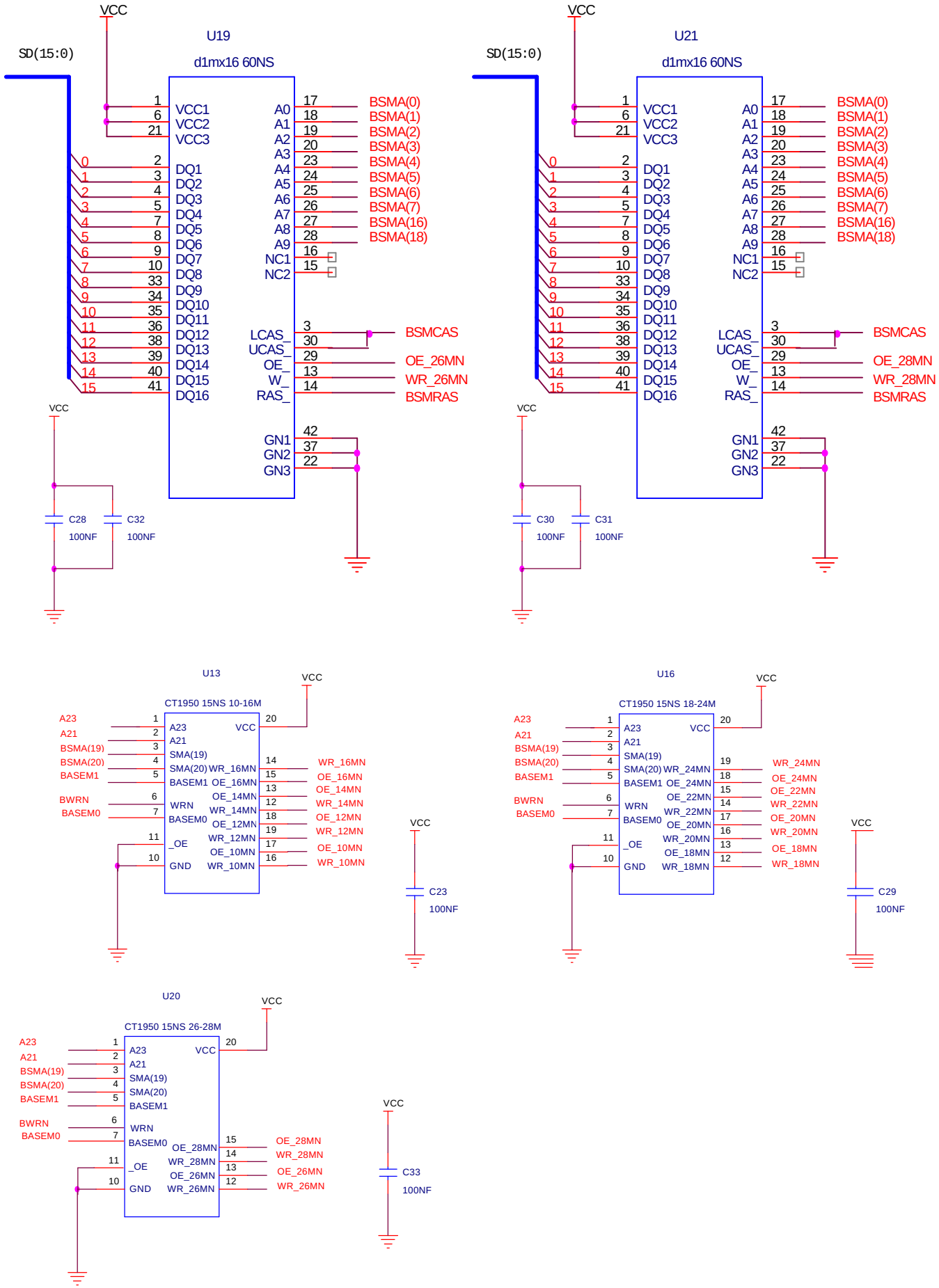
Date : 4 February, 1997



Date : 4 February, 1997



Date : 4 February, 1997



Date : 4 February, 1997

Appendix A : Installation of Memory Upgrade Module

The Creative Memory Module upgrades your Sound Blaster™ AWE64 or AWE64 Gold audio card with additional RAM for downloading SoundFonts®, enhancement of 3D Positional Audio and DirectSound mixing and acceleration. This memory add-on can be easily plugged into your audio card without the need for jumper setting. Your audio card immediately detects the presence of additional RAM.

To install your memory upgrade module:

1. Switch off your system and all peripheral devices, and unplug the power cord from the wall outlet.
2. Touch a metal plate on your system to ground yourself and discharge any static electricity.
3. Remove your system's cover and unplug any devices connected to the audio card; then remove the audio card from your system.
4. Mount your memory upgrade module onto the audio card, as shown in Figure 1.

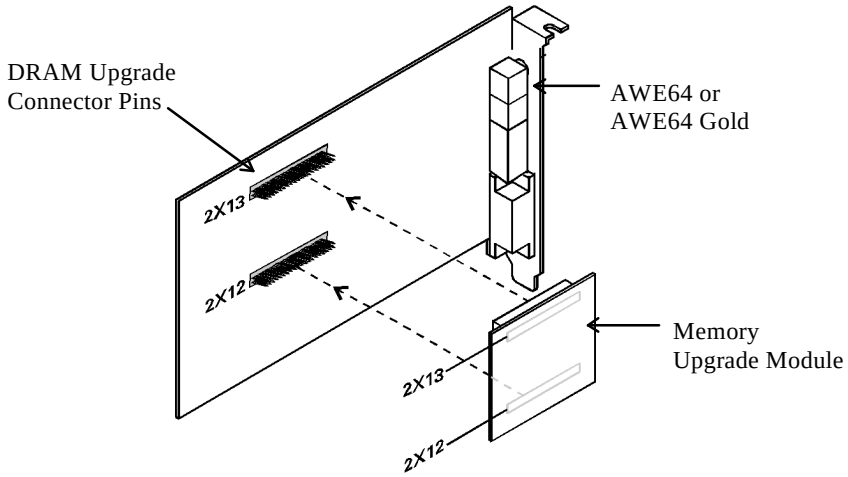


Figure 1 : Mounting the memory upgrade module

5. Reinstall the audio card into your system.
6. Reconnect speakers and devices to the audio card.
7. Replace the cover of your system, plug the power cord back into the wall outlet and switch on the system.

Your audio card immediately detects the presence of additional RAM. To test, start the AWE Control Panel of the Creative Audio software and download SoundFont® banks. The memory status bar will indicate the changes in the available memory onboard. Thereafter, play your SoundFont® banks to make sure your memory upgrade module is working properly.