CMOS OPEN ENDED

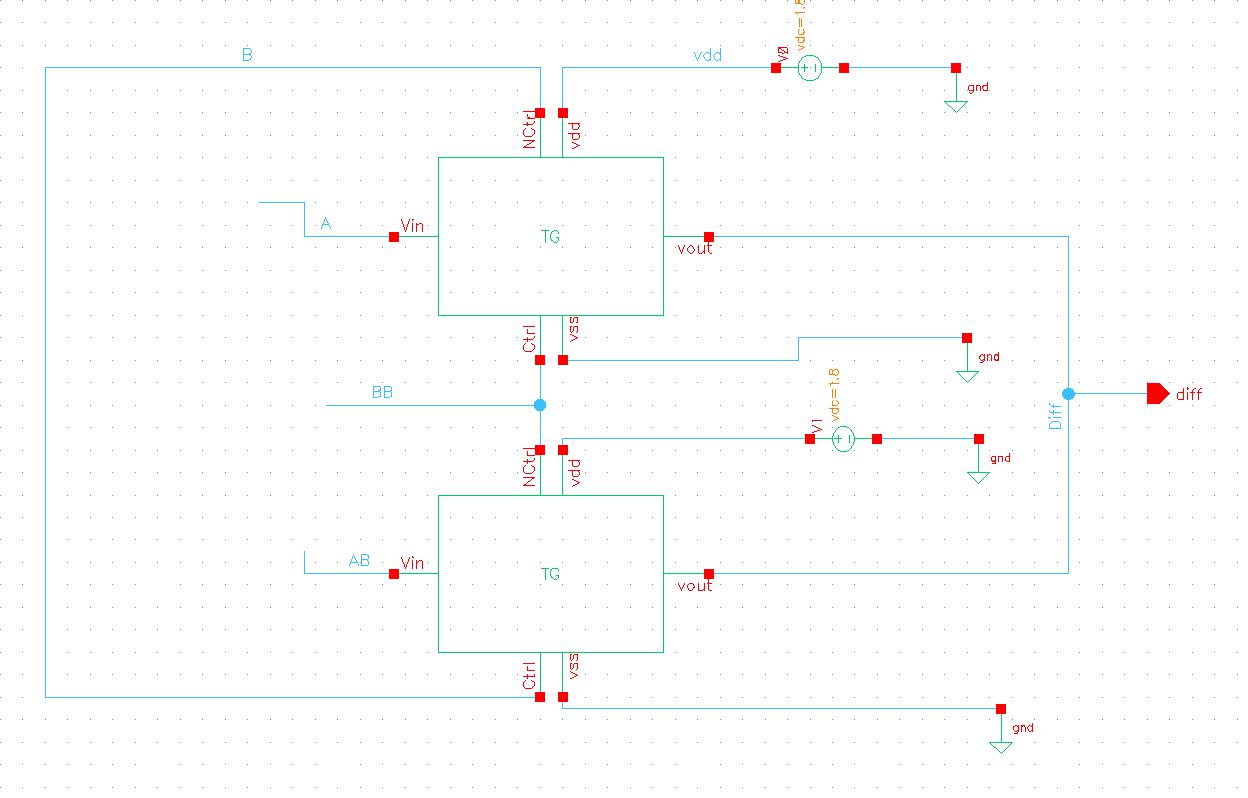
HALF ADDER

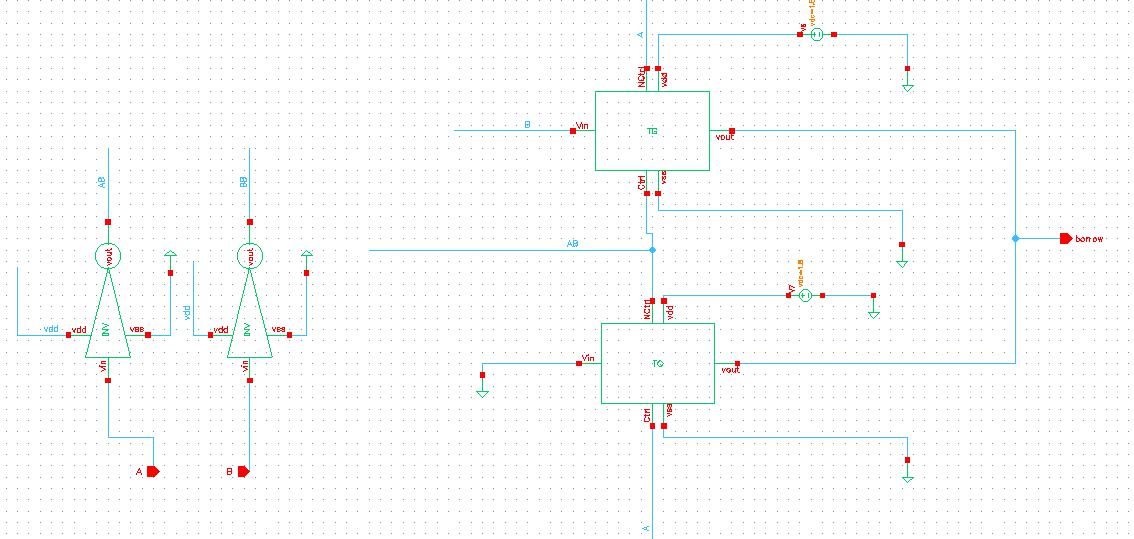
TEAM – 16

|  |  |
| --- | --- |
| **NAME** | **USN** |
| VINAYA SHETTI | 01FE21BEC232 |
| ROHIT S BIRADAR PATIL | 01FE21BEC234 |
| SHREESHA HEGDE | 01FE21BEC226 |

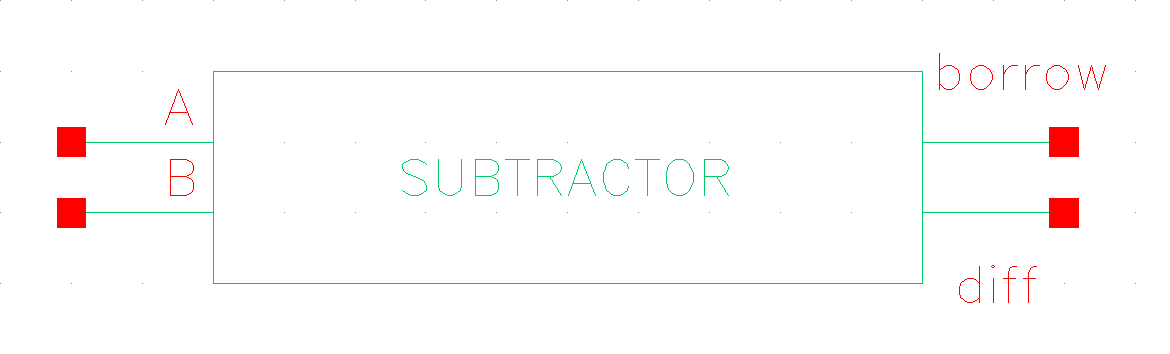
1. HALF SUBTRACTOR TRANSMISSION GATE LOGIC

* ***Fig. 1. Half subtractor TG Circuit***

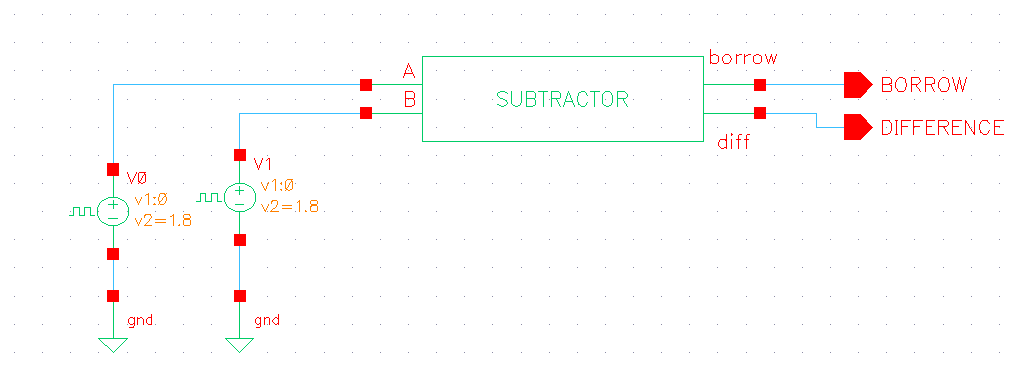
**

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* ***Fig. 2. Half Subtractor Symbol***

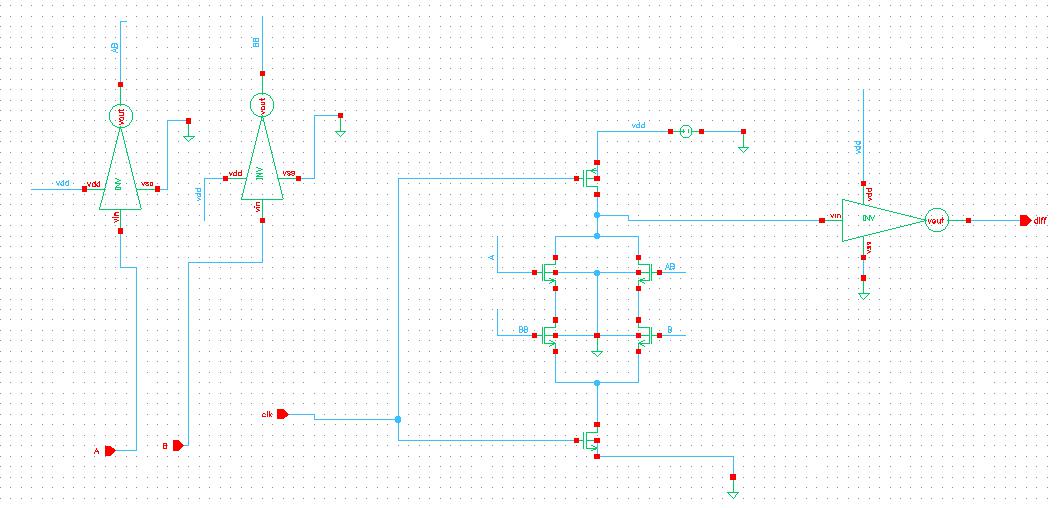
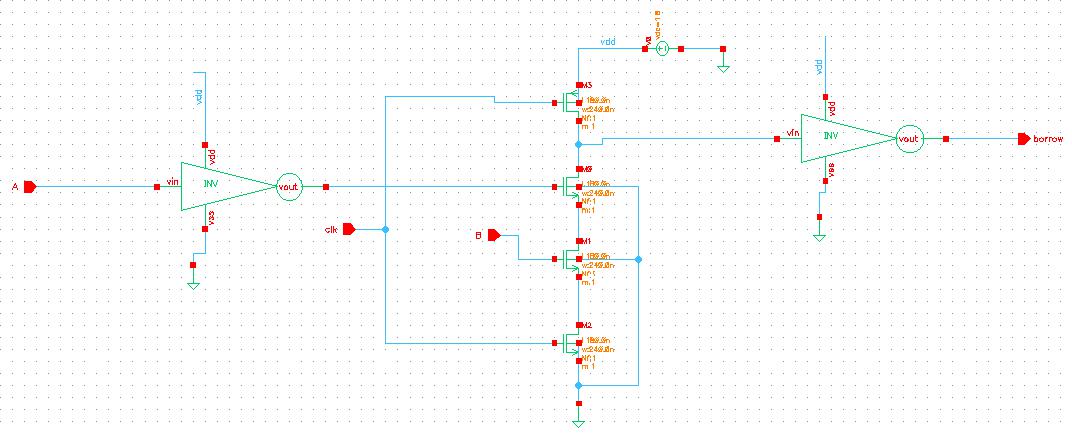


* ***Fig. 3. Half Subtractor Test Circuit***

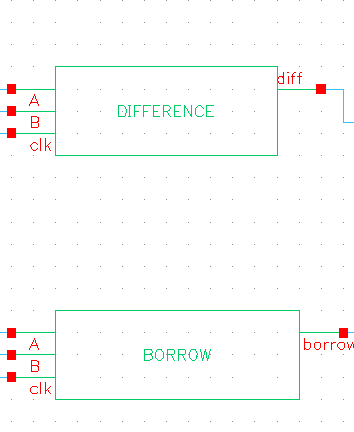
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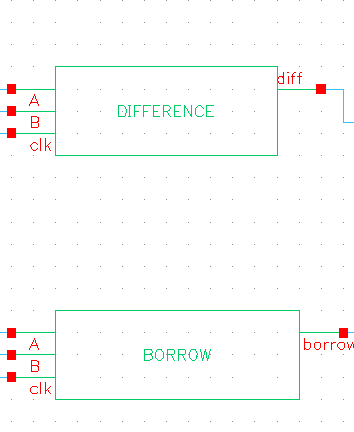
1. HALF SUBTRACTOR DOMINO GATE LOGIC

* ***Fig. 4. Half Subtractor Domino Circuit***

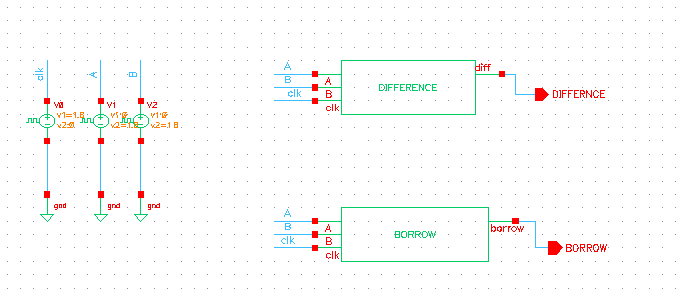


* ***Fig. 5. Half subtractor Symbol***

**

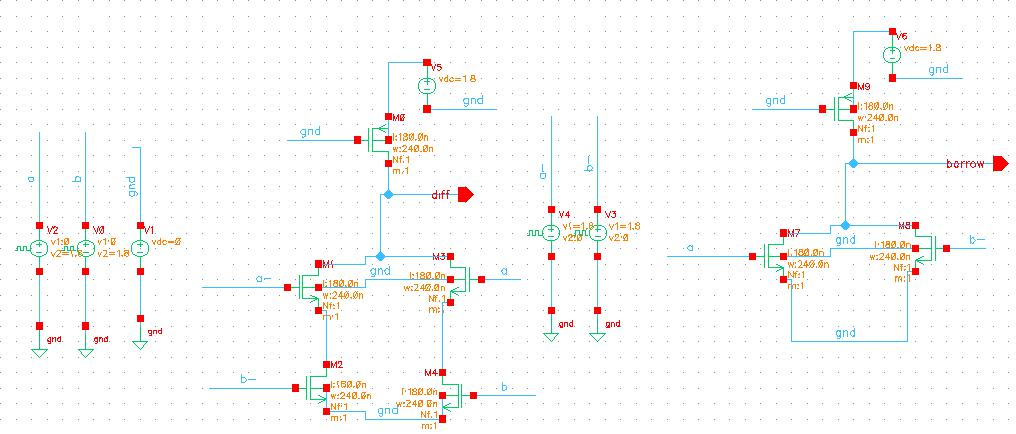


* ***Fig. 6. Half Adder Test Circuit***

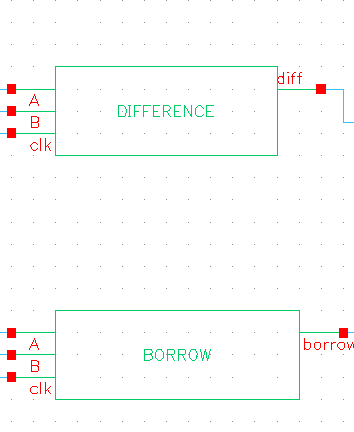
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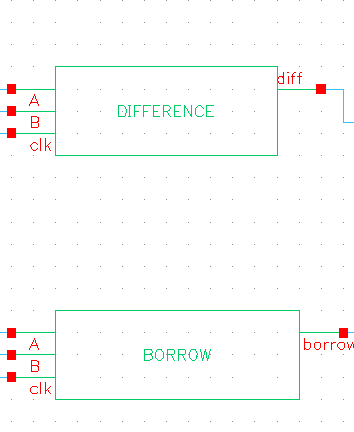
1. HALF SUBTRACTOR PSUEDO NMOS GATE LOGIC

* ***Fig. 7. Half Subtractor Pseudo nmos Circuit***

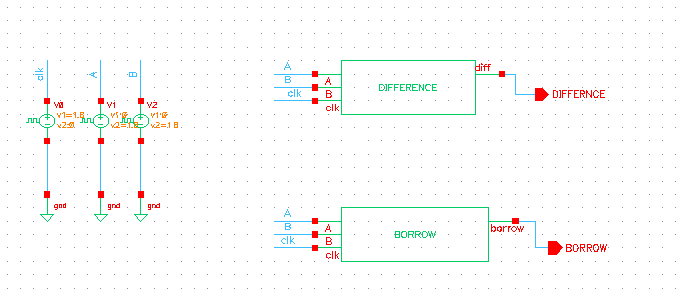
**

* ***Fig. 8. Half subtractor Symbol***

**

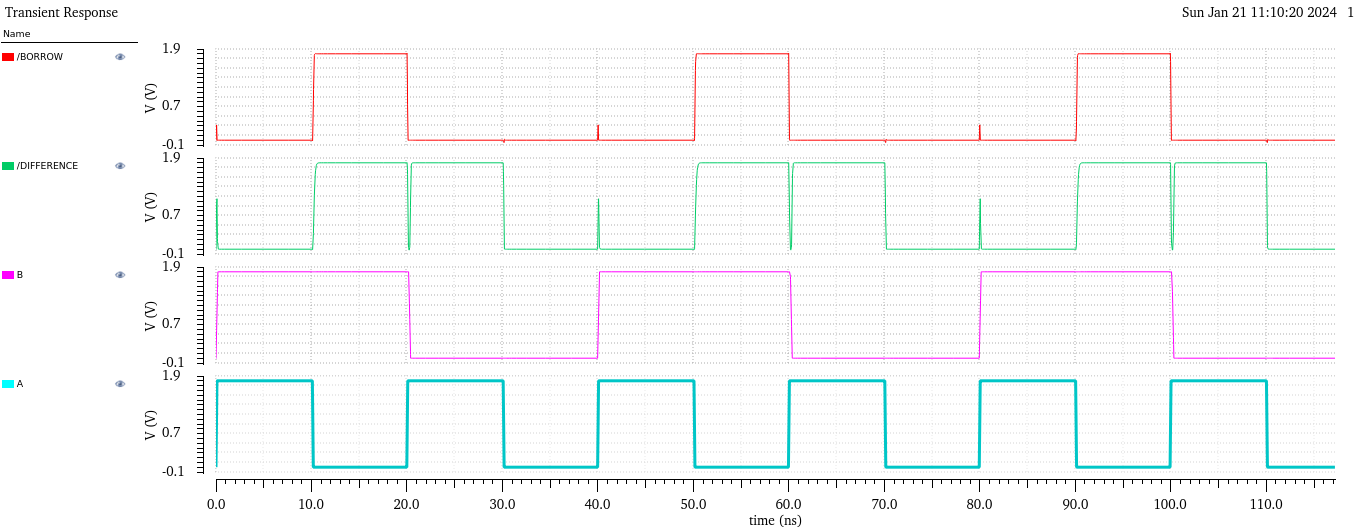


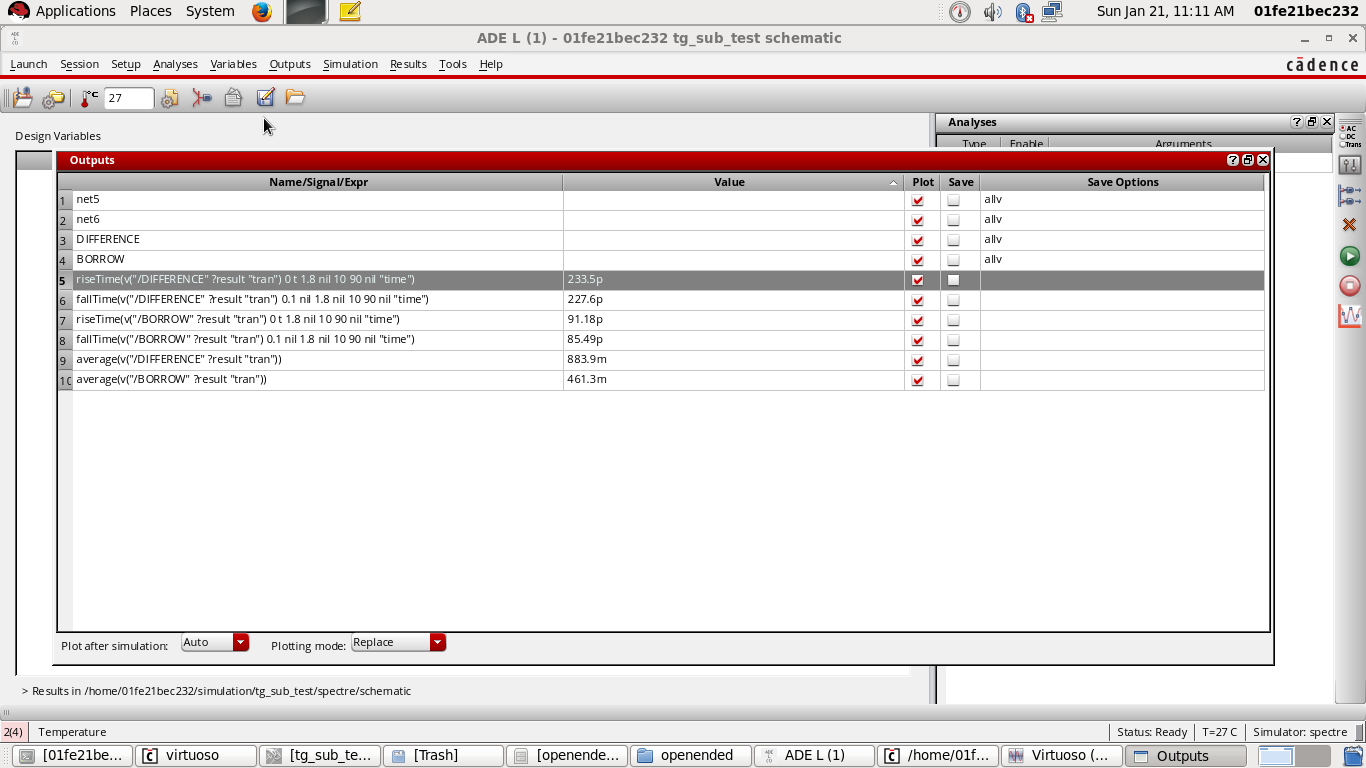
* *Fig. 6. Half Subtractor Test Circuit*

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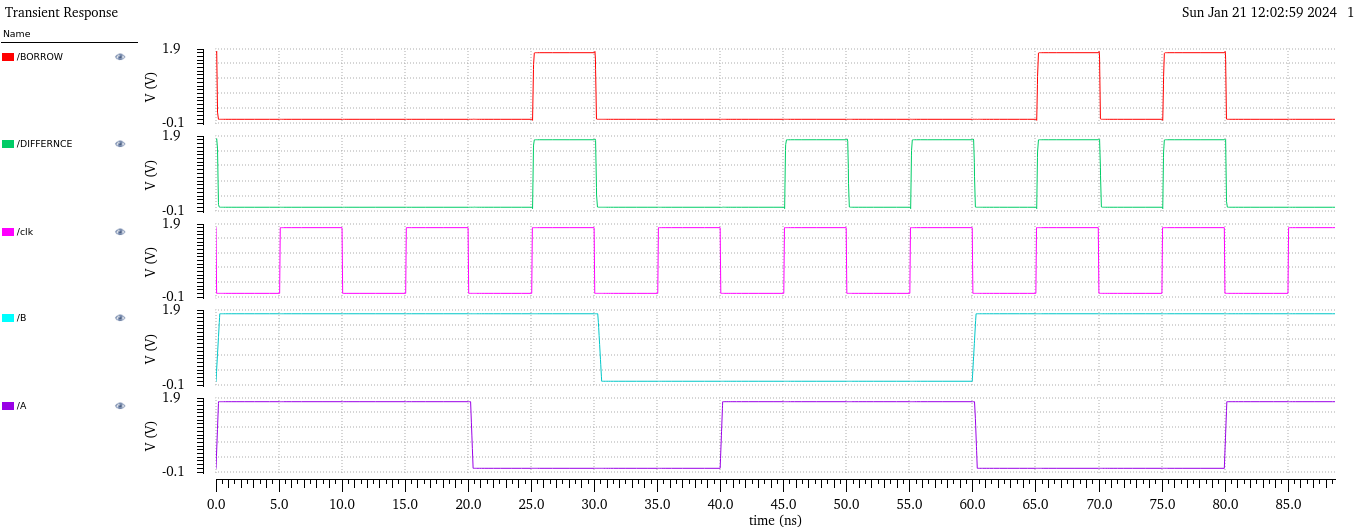
**RESULTS:**

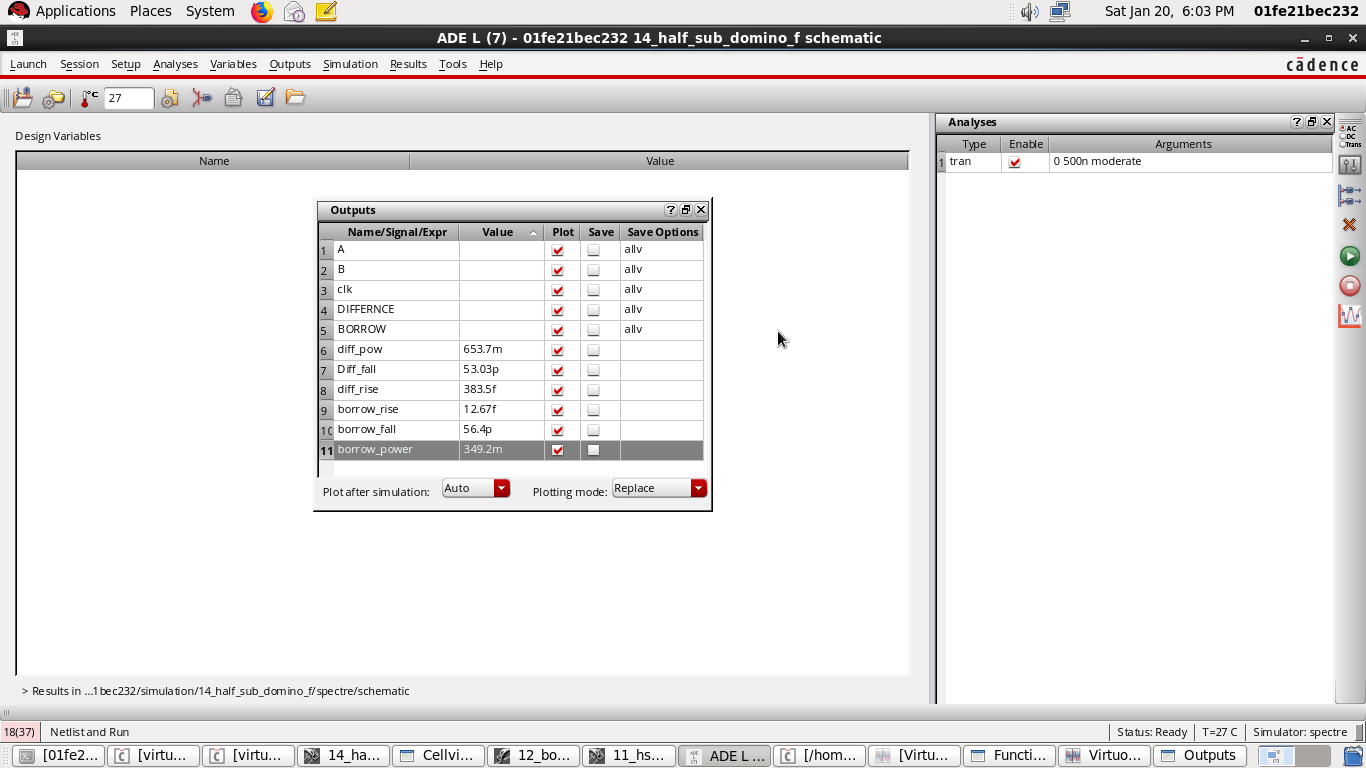
TRANMISSION GATE LOGIC :





DOMINO GATE LOGIC :





COMPARISON:

|  |  |  |
| --- | --- | --- |
| Parameters | Transmission Gate LOGIC | DOMINO LOGIC |
| Rise Time (sum) | 233.5 p | 383.5 f |
| Fall Time (sum) | 227.6 p | 53.03p |
| Power () | 883.9m | 653.7m |
| Rise Time (carry) | 91.18 p | 12.67f |
| Fall Time (carry) | 85.49 p | 56.4p |
| Power | 461.3 m | 349.2m |
| Area |  |  |