`timescale 1ns / 1ps

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// Company: Ratner Surf Designs

// Engineer: James Ratner

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// Create Date: 11/04/2018 07:39:17 PM

// Design Name:

// Module Name: mux\_4t1\_nb

// Project Name:

// Target Devices:

// Tool Versions:

// Description: 8:1 MUX with parametized data widths

//

// USEAGE: (for 4-bit data instantion)

//

// mux\_8t1\_nb #(.n(4)) my\_8t1\_mux (

// .SEL (my\_sel),

// .D0 (my\_d0),

// .D1 (my\_d1),

// .D2 (my\_d2),

// .D3 (my\_d3),

// .D4 (my\_d4),

// .D5 (my\_d5),

// .D6 (my\_d6),

// .D7 (my\_d7),

// .D\_OUT (my\_d\_out) );

//

// Dependencies:

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// Revision History:

// Revision 1.00 - File Created: 11-04-2018

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// Additional Comments:

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module mux\_8t1\_nb(SEL, D0, D1, D2, D3, D4, D5, D6, D7, D\_OUT);

input [2:0] SEL;

input [n-1:0] D0, D1, D2, D3, D4, D5, D6, D7;

output reg [n-1:0] D\_OUT;

parameter n = 8;

always @(SEL, D0, D1, D2, D3, D4, D5, D6, D7)

begin

case (SEL)

0: D\_OUT = D0;

1: D\_OUT = D1;

2: D\_OUT = D2;

3: D\_OUT = D3;

4: D\_OUT = D4;

5: D\_OUT = D5;

6: D\_OUT = D6;

7: D\_OUT = D7;

default: D\_OUT = 0;

endcase

end

endmodule