`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company: Ratner Surf Designs

// Engineer: James Ratner

//

// Create Date: 09/08/2018 07:17:37 PM

// Design Name:

// Module Name: reg\_nb

// Project Name:

// Target Devices:

// Tool Versions:

// Description: Model for generic register (defaults to 8 bits)

// with asynchronous clear

//

// //- Usage example for instantiating 16-bit register

// reg\_nb #(16) MY\_REG (

// .data\_in (my\_data\_in),

// .ld (my\_ld),

// .clk (my\_clk),

// .clr (my\_clr),

// .data\_out (my\_data\_out)

// );

//

// Dependencies:

//

// Revision:

// Revision 1.00 - File Created: 09-09-2018

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module reg\_nb(data\_in, clk, clr, ld, data\_out);

input [n-1:0] data\_in;

input clk, clr, ld;

output reg [n-1:0] data\_out;

parameter n = 8;

always @(posedge clr, posedge clk)

begin

if (clr == 1) // asynch clr

data\_out <= 0;

else if (ld == 1)

data\_out <= data\_in;

end

endmodule