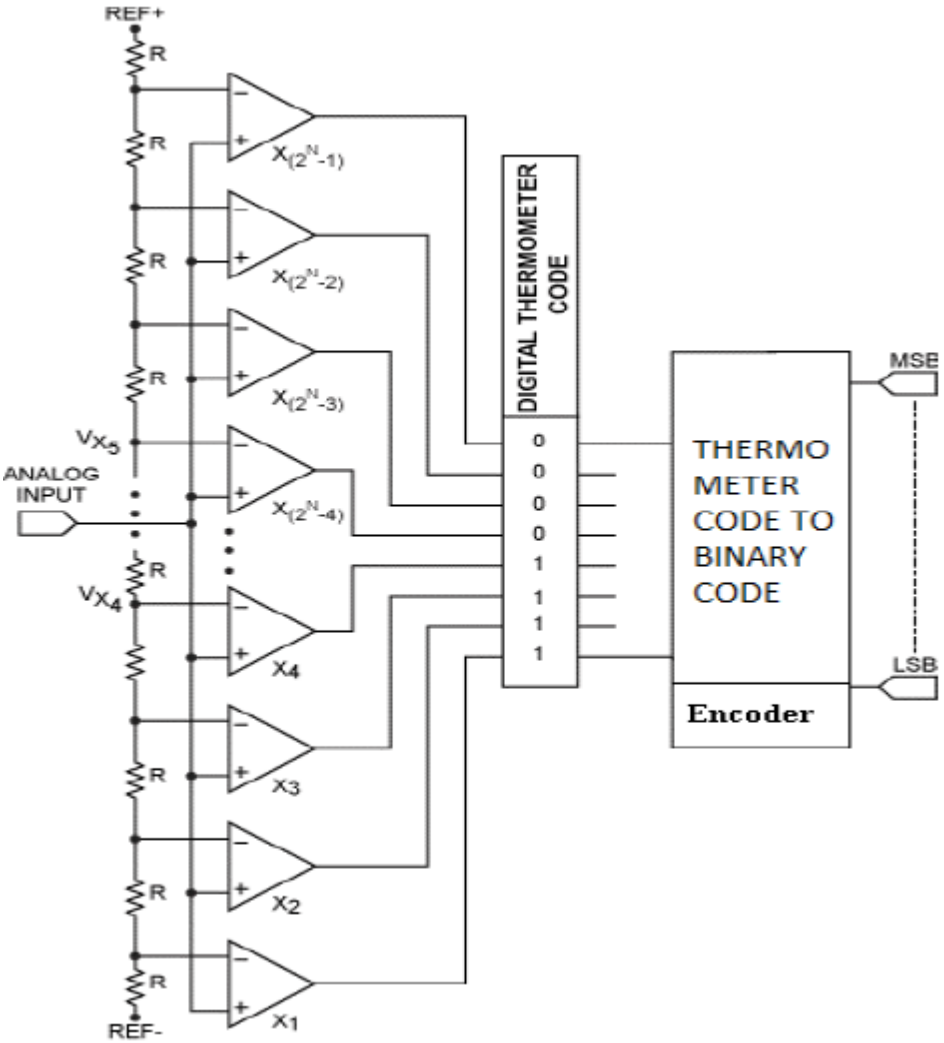
EE288 Homework #2 (5 points) Feb 12, 2018

Due: Feb 26, 2018 6:00PM
Homework will not be received after due.
Homework submission file should be in a pdf format and file name convention should be EE288HW2_yourname. If you submit a file other than the pdf format and your filename does not confirm to the file name convention, there will be a deduction on your score.

In this homework, you will build a 4-bit Flash ADC using ideal components based on the following architecture where the comparator block should be implemented as a clocked comparator.



Assume the following design constraint.
VDD=1.8V
Vrefp or REF+ = 1.4V
Vrefm or REF- = 0.4V
Input signal range 0.4V ~ 1.4V
Sampling clock pulse, fs = 100 MHz
Input signal frequency at fin = (cycles/N) * fs where cycles=7 and N=64 for 64-point FFT in MATLAB.

Select the resistor values of the resistor ladder to get 1 mA current through the ladder to generate various threshold levels for 15 comparators. You should have a sample and hold circuit inside the comparator such that the comparator tracks the signal when the clock is high and hold the sampled value at the falling edge of the clock. Therefore, the ideal comparator should generate valid output while the clock is low. Additionally, the comparator output should be zero when the comparator clock is high.

To test the functionality of the ADC, build an ideal 4-bit DAC similar to what you did in Homework#1. Then apply a full-scale sinusoid to run a transient simulation for 640ns in Cadence Spectre. Plot the transient waveforms for input, sampled input, and output signals along with clock and other relevant signals in white background.

Then open Calculator to sample the data points of the DAC output. Each data point needs to be 10ns apart and you should get 64 data points for FFT analysis in MATLAB. For this, use "sample" function in Calculator to get 64 samples at 9ns, 19ns, 29ns, …. 639ns.

Once you have the data in MATLAB, write a code to run FFT on the loaded samples. Report your results similar to Homework#1. But this time, the FFT plot should show the spectrum up to fs/2.

Next, write Verilog-A codes for the clocked comparator and the thermometer to binary encoder. Then, create test benches to check if the Verilog code is working. Report the test bench schematic for the clocked comparator and the thermometer to binary encoder, and include the simulation results and the Verilog codes in your homework submission.

If you are new to Verilog-A, please check the file named "EE288_VerilogA.pdf" in the homework folder in Canvas and search internet to learn the coding syntax.

Summary of what you need to submit electronically:

1. Schematics of your design – use white background
2. Transient simulation results showing all relevant signal waveforms
3. MATLAB code and the FFT plot for the ADC
4. Verilog-A codes for the clocked comparator and the thermometer to binary encoder
5. Test bench schematics and the simulation results showing the functionality of the Verilog codes