



# Conception numérique (DiD)

# Field Programmable Gate Array

# FPGA

Filière Systèmes industriels

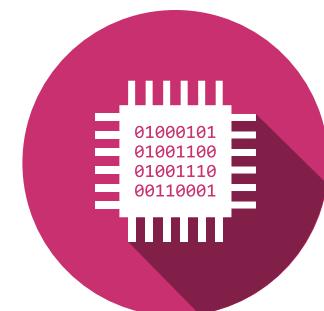
Filière Energie et techniques environnementales

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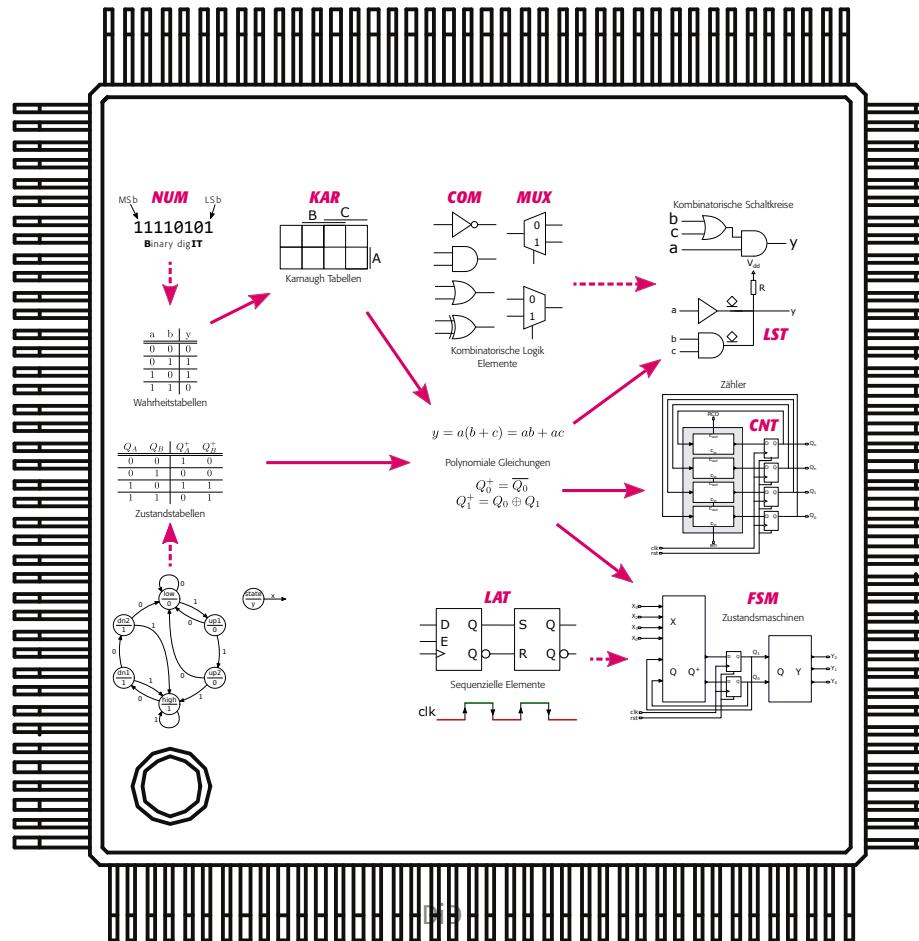
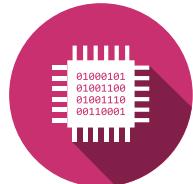
Silvan Zahno [silvan.zahno@hevs.ch](mailto:silvan.zahno@hevs.ch)

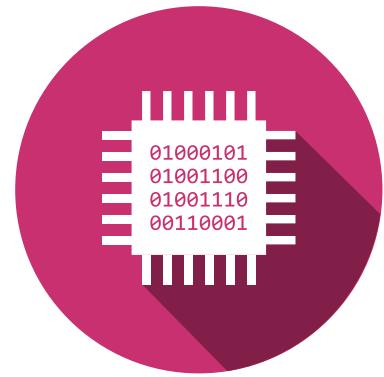
Christophe Bianchi [christophe.bianchi@hevs.ch](mailto:christophe.bianchi@hevs.ch)

François Corthay [francois.corthay@hevs.ch](mailto:francois.corthay@hevs.ch)



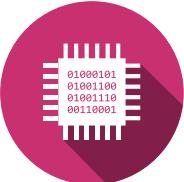
# Current content of the topic in the course



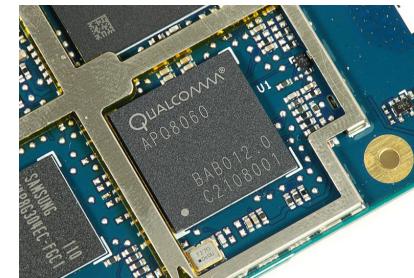
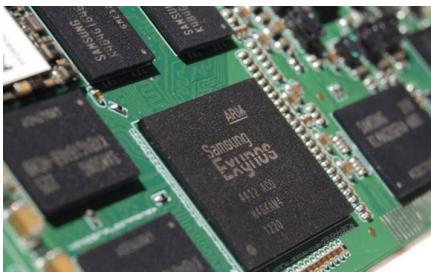


## ASIC vs. FPGA

# ASIC vs. FPGA Differences



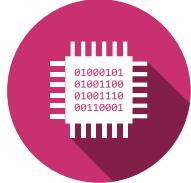
- ASIC – Application Specific Integrated Circuit



- FPGA – Field Programmable Gate Array



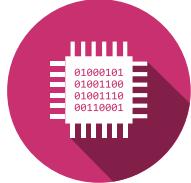
# ASIC vs. FPGA Differences



- ASIC – **A**pplication **S**pecific **I**ntegrated **C**ircuit
  - From the behavior description to the physical layout
  - Designs must be sent to a semiconductor factory for costly and time-consuming production
- FPGA – **F**ield **P**rogrammable **G**ate **A**rray
  - A physical layout ends with a bitstream that is used to configure a device.
  - Purchased on the market and reconfigured by the designers themselves.



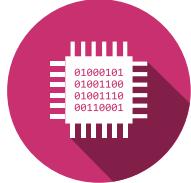
# ASIC vs. FPGA Differences



- ASIC – Application Specific Integrated Circuit
  - High efficiency
  - Low power consumption
  - Low cost with high volume
- FPGA – Field Programmable Gate Array
  - Commercial standard product
  - Low development costs
  - Short time to market
  - Reconfigurability



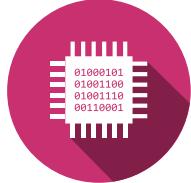
# ASIC vs. FPGA Differences



- ASIC – **A**pplication **S**pecific **I**ntegrated **C**ircuit
  - von der Verhaltensbeschreibung bis zum physikalischen Layout
  - Entwürfe müssen zur kostspieligen und zeitaufwendigen Herstellung in eine Halbleiterfabrik geschickt werden
- FPGA – **F**ield **P**rogrammable **G**ate **A**rray
  - ein physikalisches Layout endet mit einem Bitstrom, der zur Konfiguration eines Geräts verwendet wird.
  - auf dem Markt gekauft und von den Designern selbst rekonfiguriert.



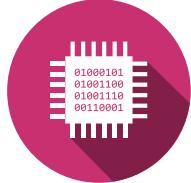
# ASIC vs. FPGA Differences



- ASIC – Application Specific Integrated Circuit
  - Hohe Effizienz
  - Kleine Leistungsaufnahme
  - Niedrige Kosten bei hohem Volumen
- FPGA – Field Programmable Gate Array
  - kommerzielles Standardprodukt
  - niedrige Entwicklungskosten
  - kurze Produkteinführungszeit
  - Rekonfigurierbarkeit



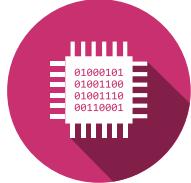
# ASIC vs. FPGA Differences



- ASIC – **A**pplication **S**pecific **I**ntegrated **C**ircuit
  - de la description du comportement à l'aménagement physique
  - les conceptions doivent être envoyées pour une fabrication coûteuse et longue dans une fonderie de semi-conducteurs
- FPGA – **F**ield **P**rogrammable **G**ate **A**rray
  - aucun plan d'implantation physique ne se termine par un flux de bits utilisé pour configurer un périphérique
  - achetés sur le marché et reconfigurés par les concepteurs eux-mêmes



# ASIC vs. FPGA Differences

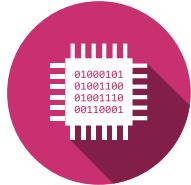


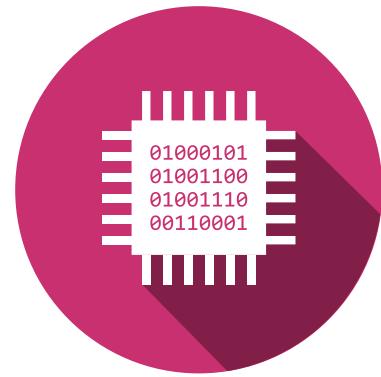
- ASIC – **A**pplication **S**pecific **I**ntegrated **C**ircuit
  - haute performance
  - faible puissance
  - faible coût dans des volumes élevés
- FPGA – **F**ield **P**rogrammable **G**ate **A**rray
  - produit commercial standard
  - faible coût de développement
  - délai de mise sur le marché court
  - reconfigurabilité



# ASIC vs. FPGA Differences

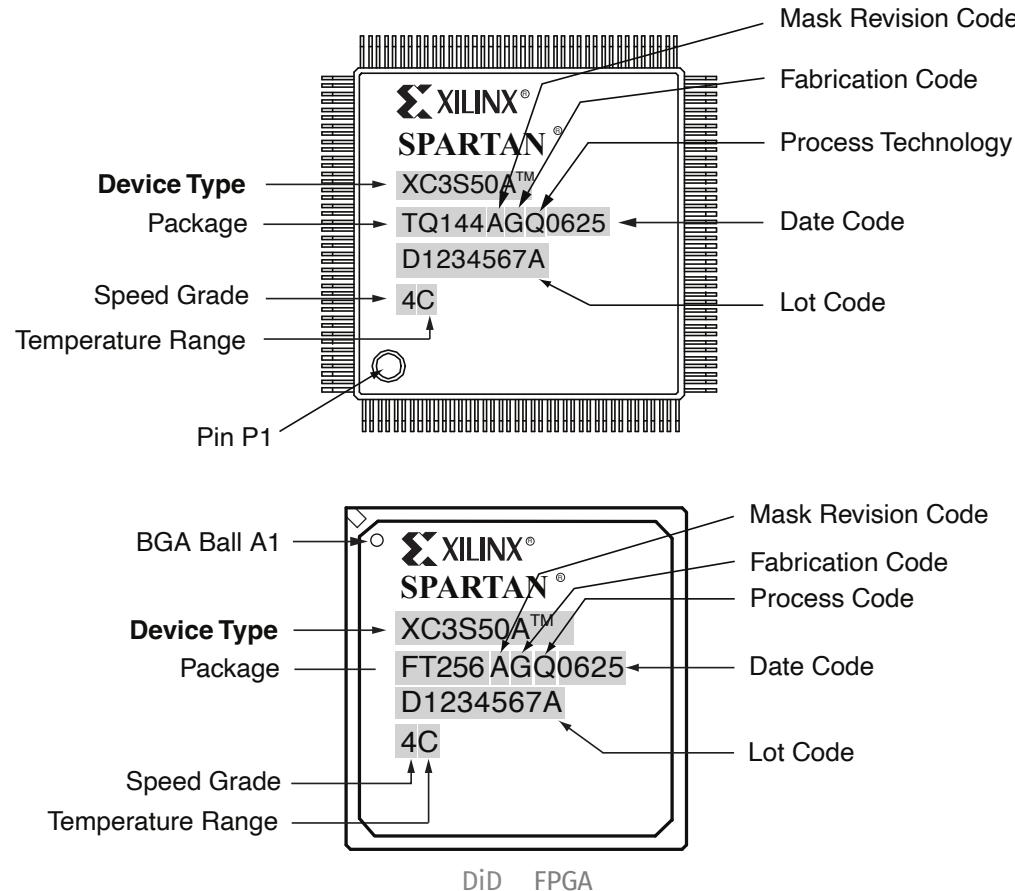
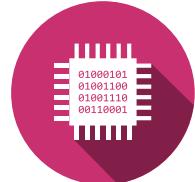
- ASIC – Application Specific Integrated Circuit
- FPGA – Field Programmable Gate Array



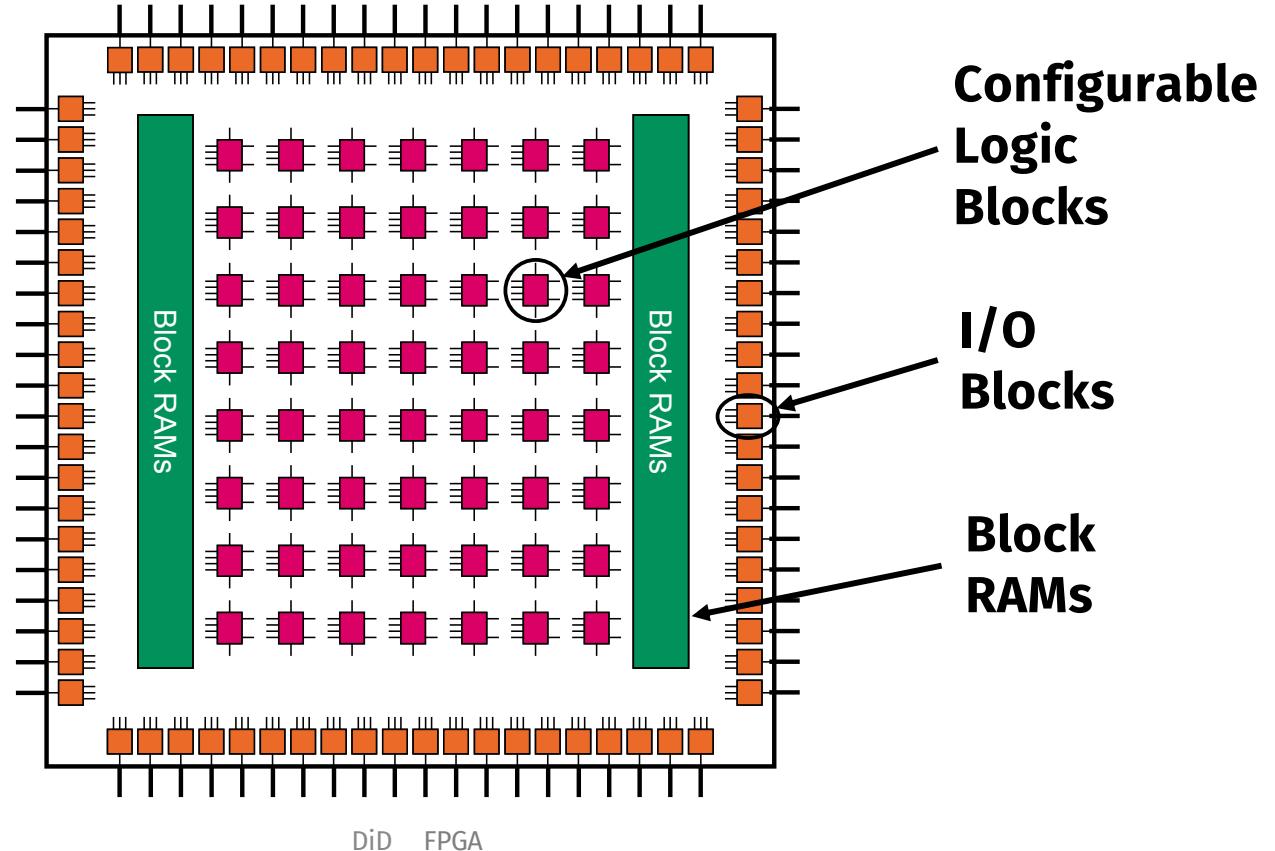
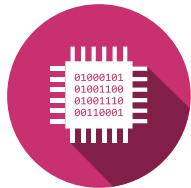


FPGA

# FPGA Packaging



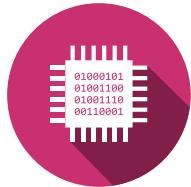
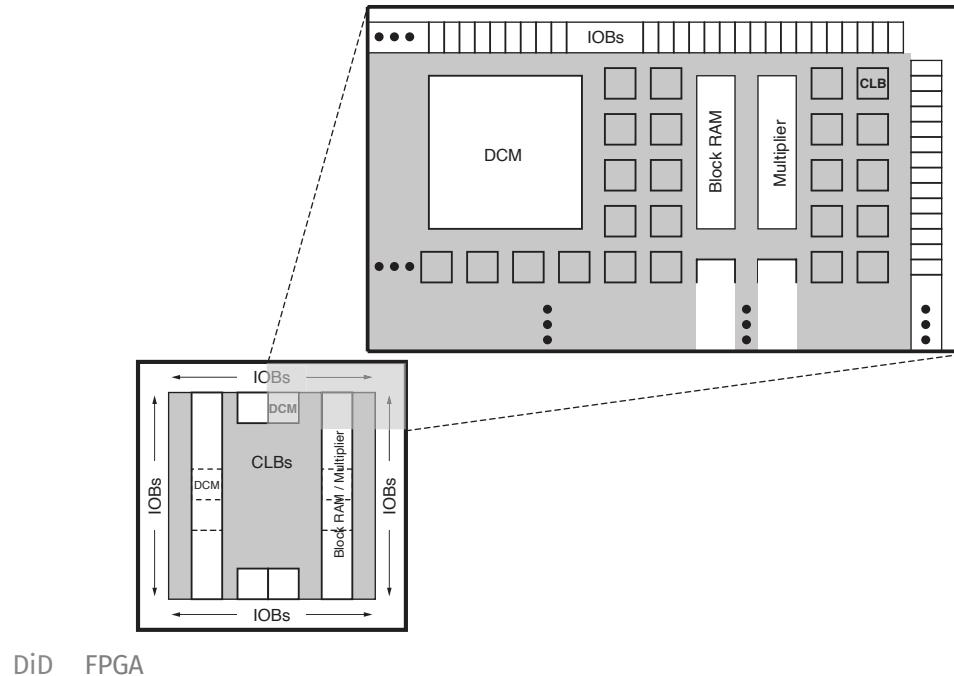
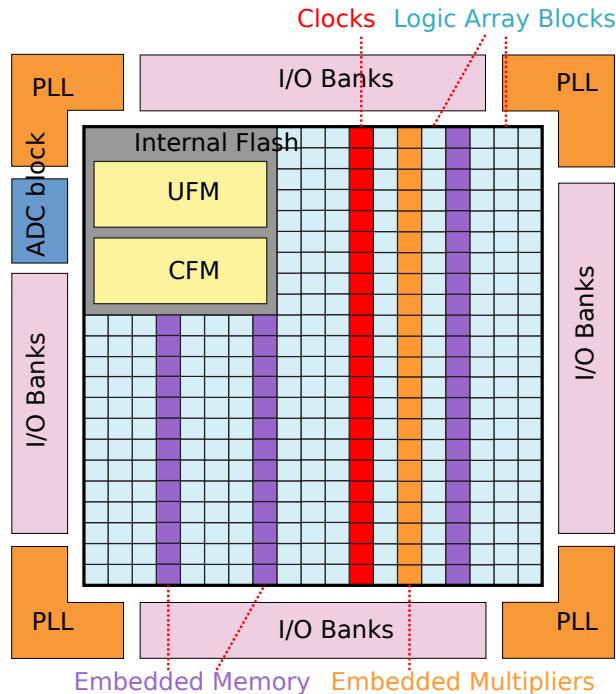
# FPGA Architecture



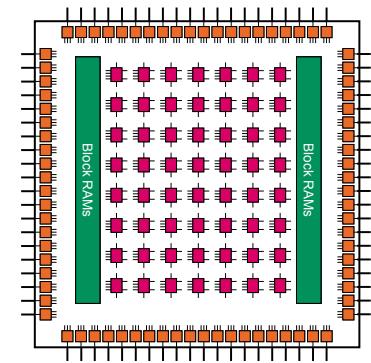
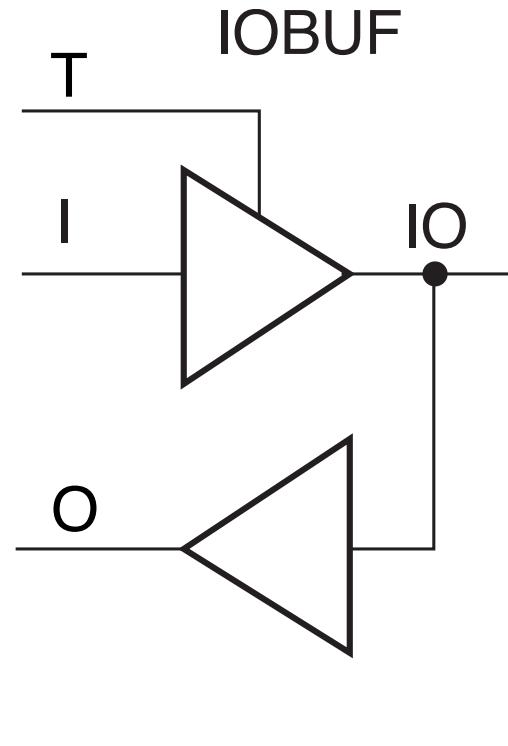
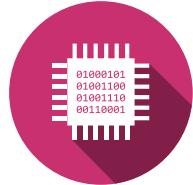
# FPGA Architecture



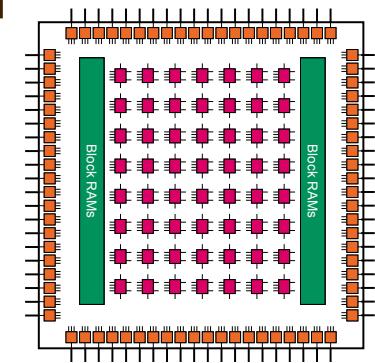
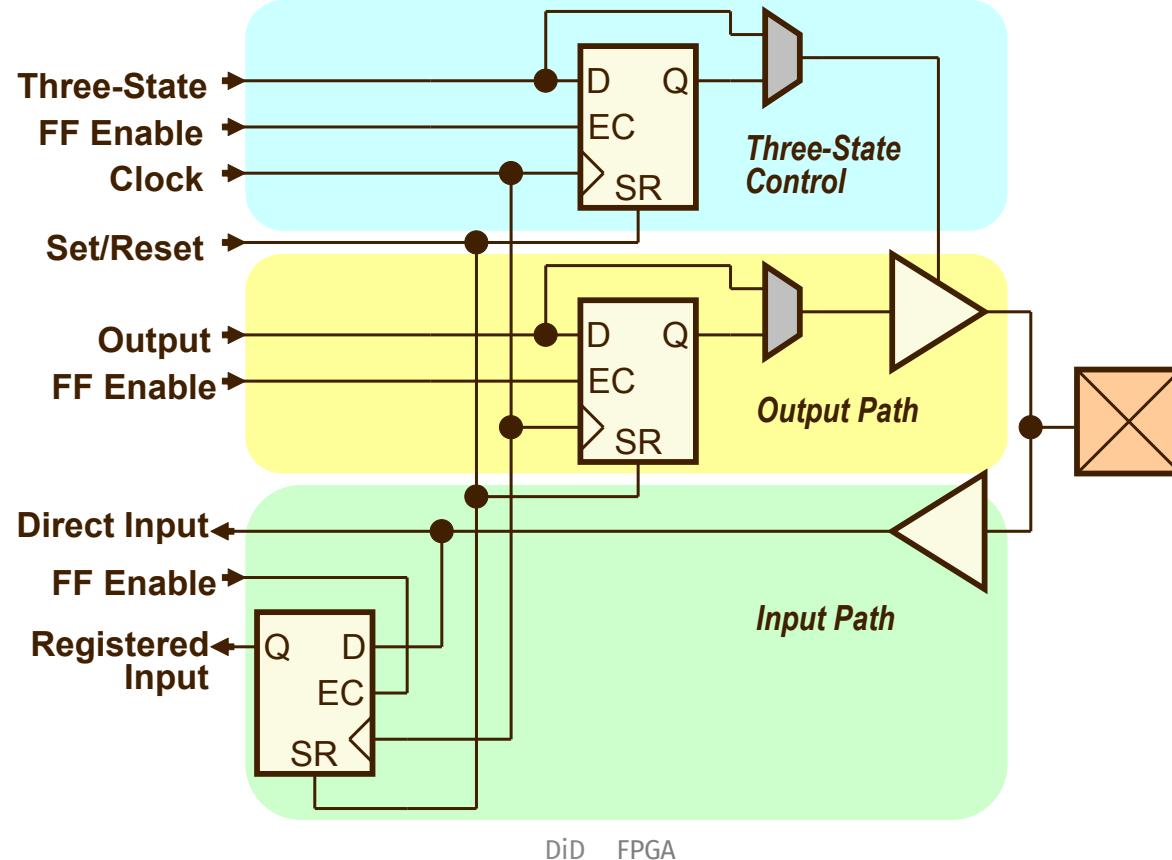
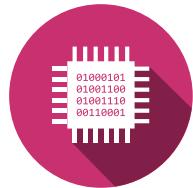
FPGA Design  
Solutions Network



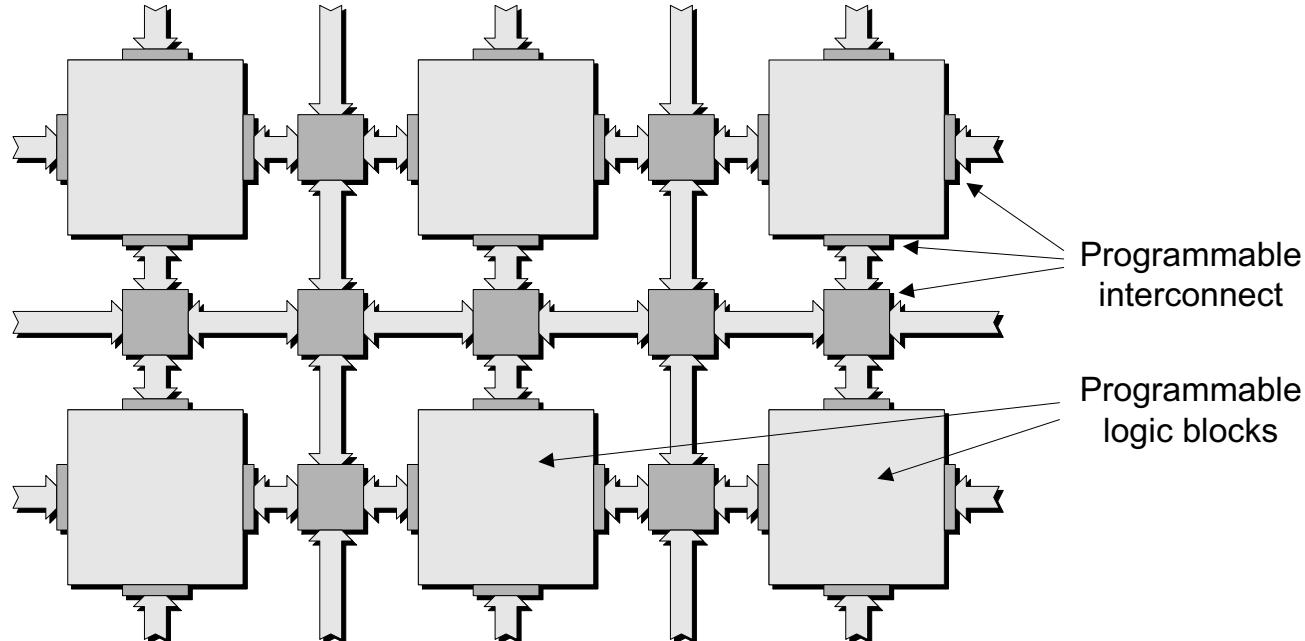
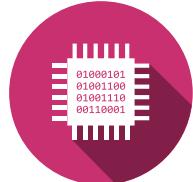
# FPGA I/O Elements



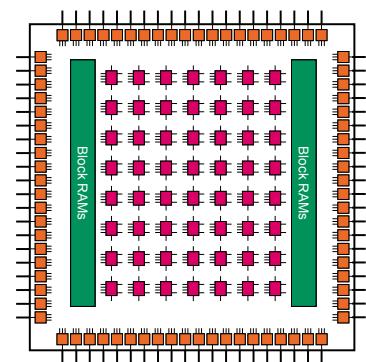
# FPGA I/O Elements



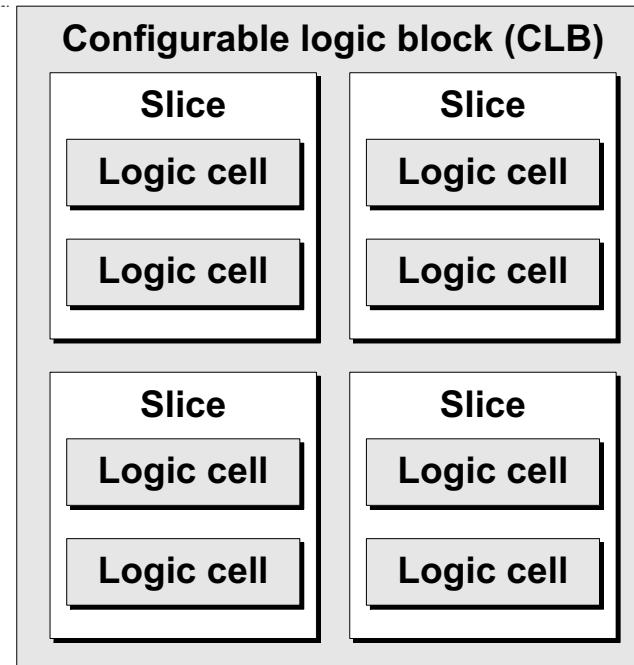
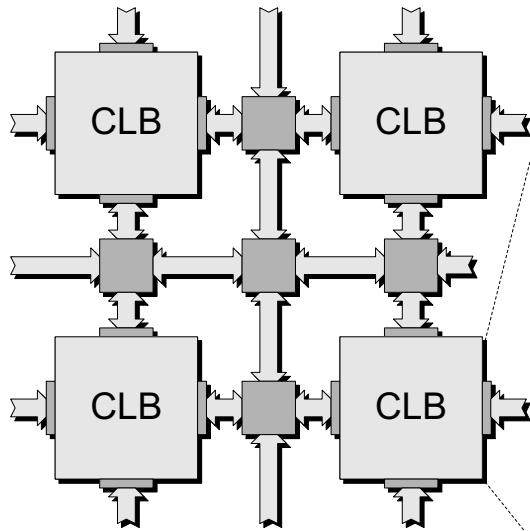
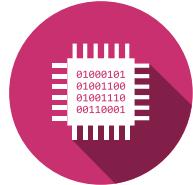
# FPGA Slice Elements



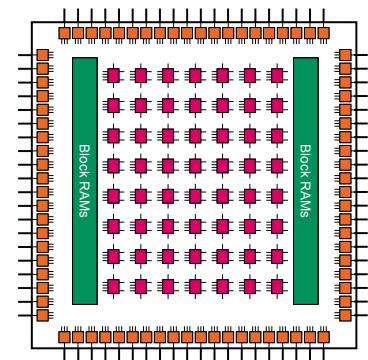
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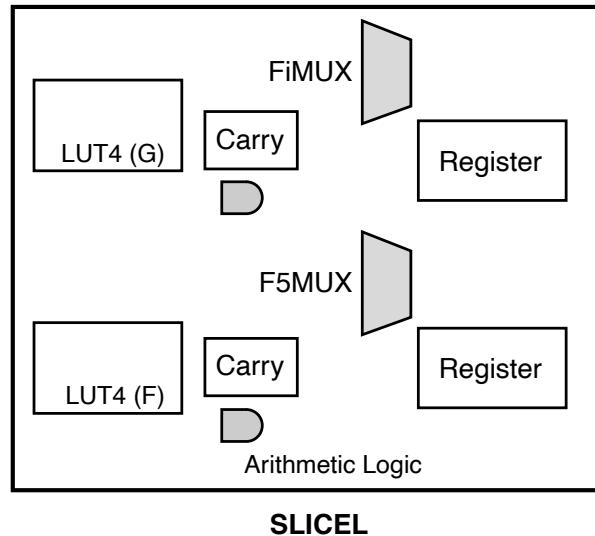
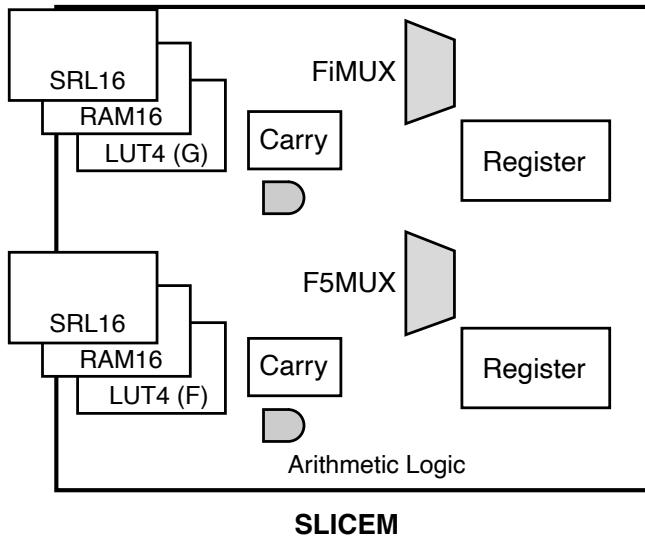
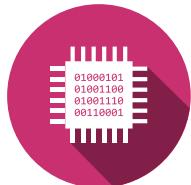
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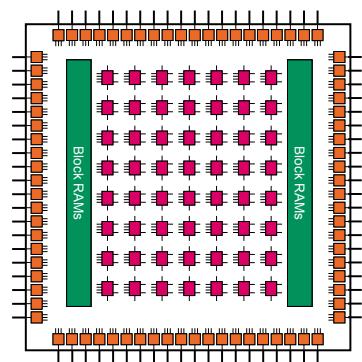
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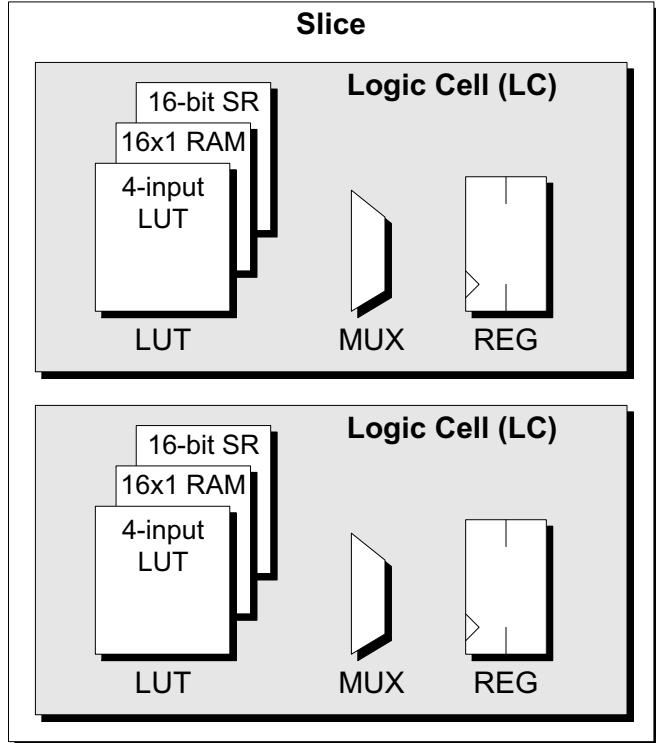
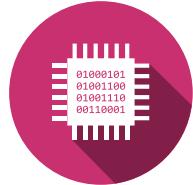


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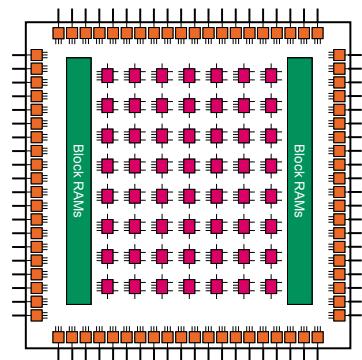


# FPGA

## Slice Elements

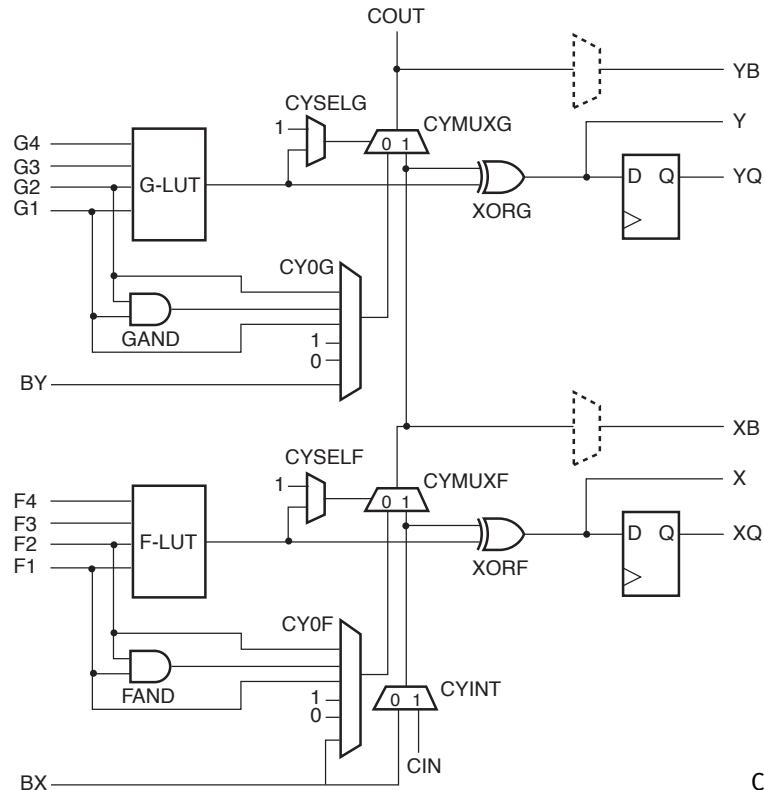
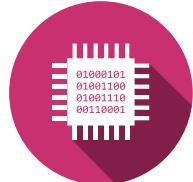


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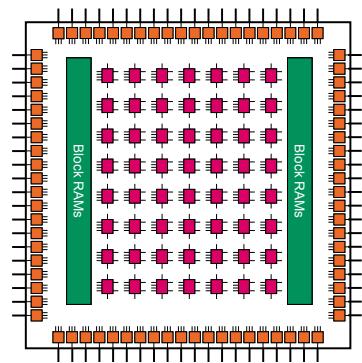


# FPGA

## Slice Elements

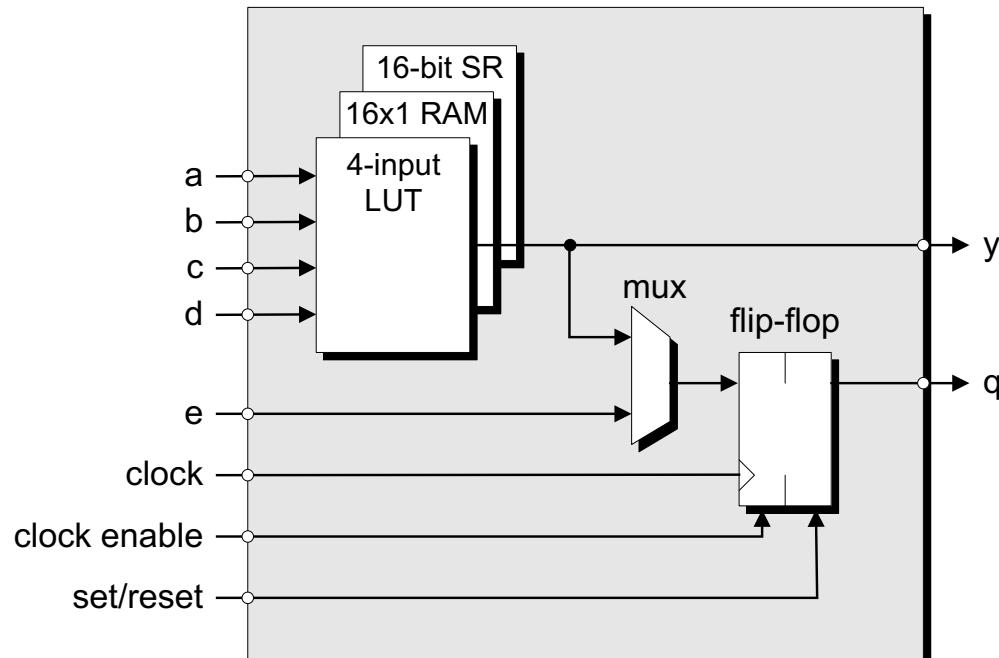
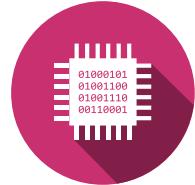


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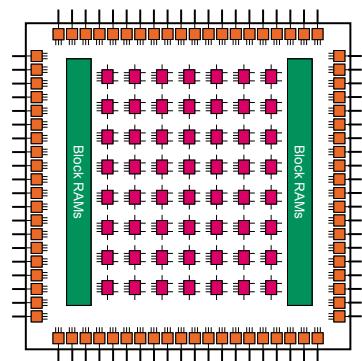


# FPGA

## Logic Elements

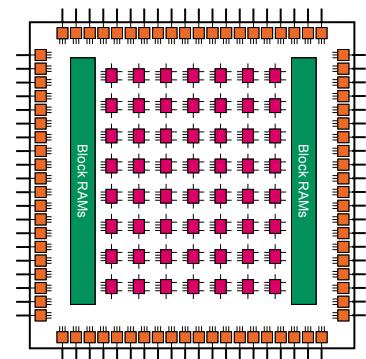
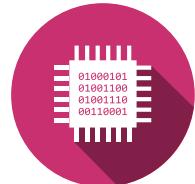
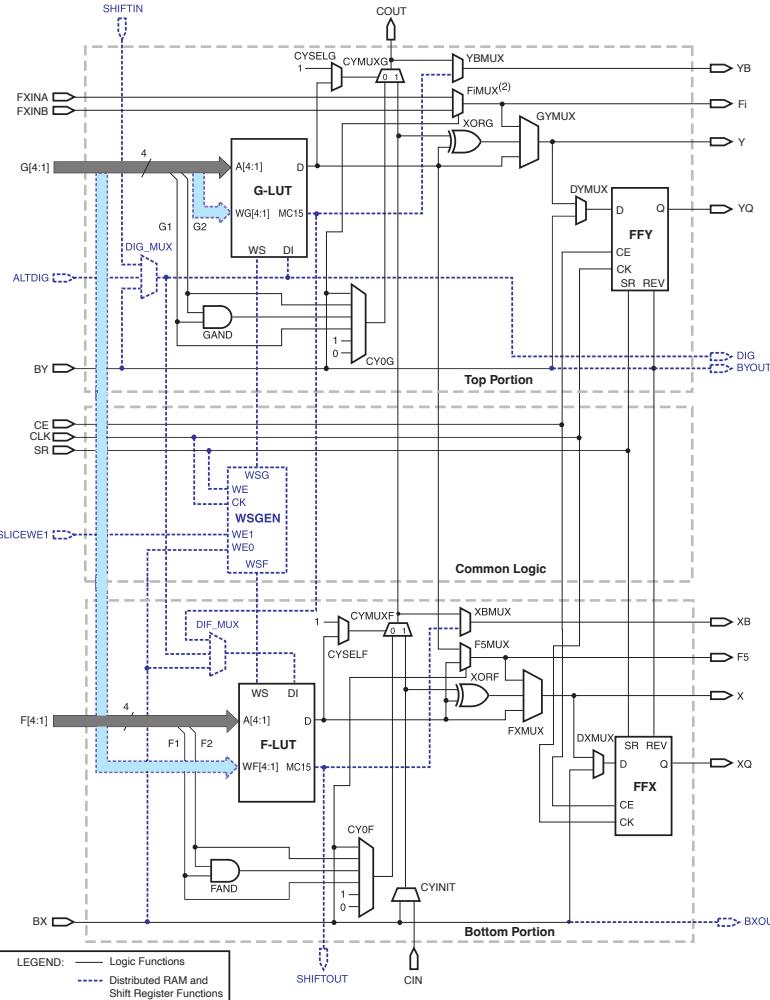


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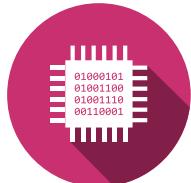
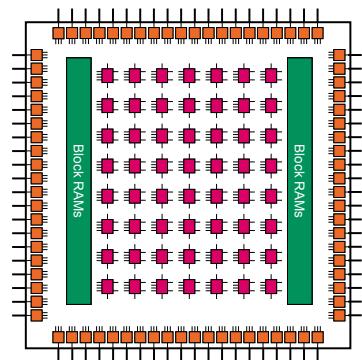
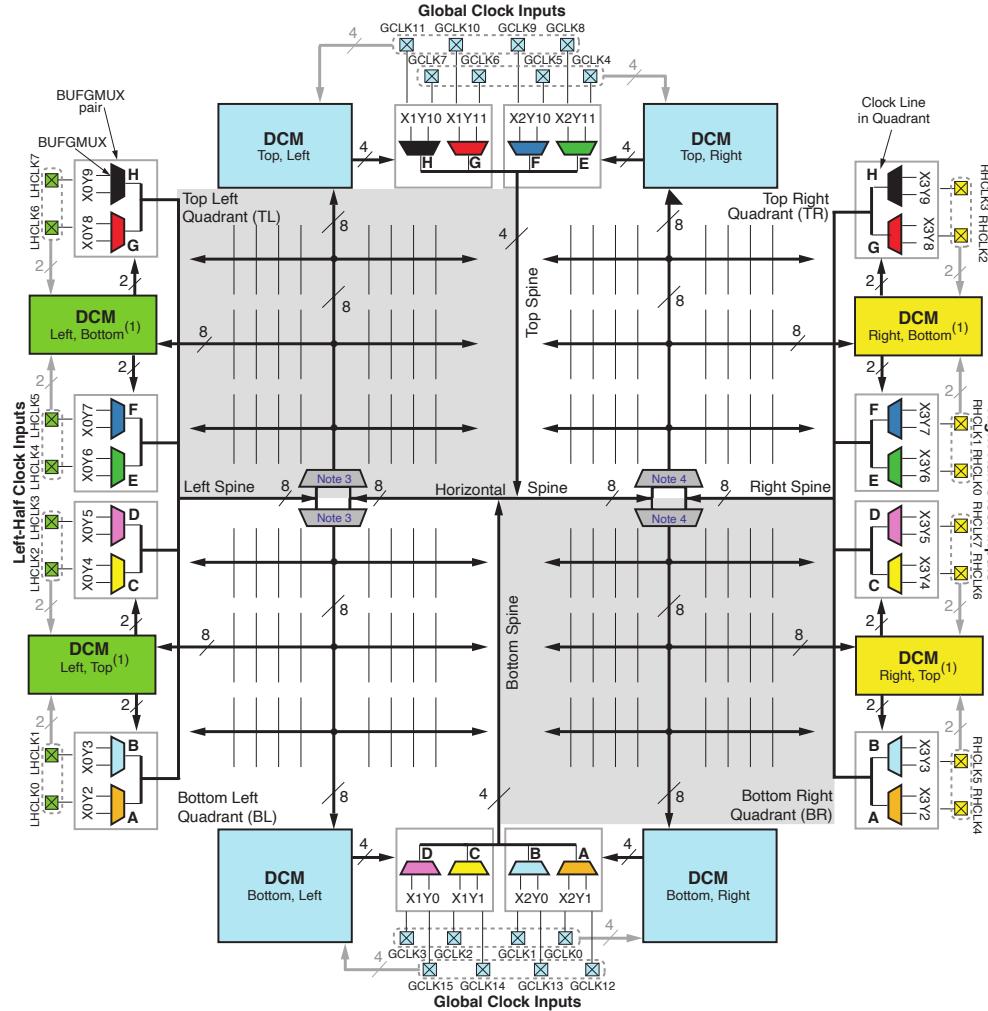


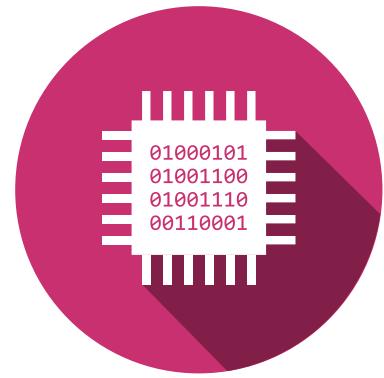
# FPGA

## Logic Elements



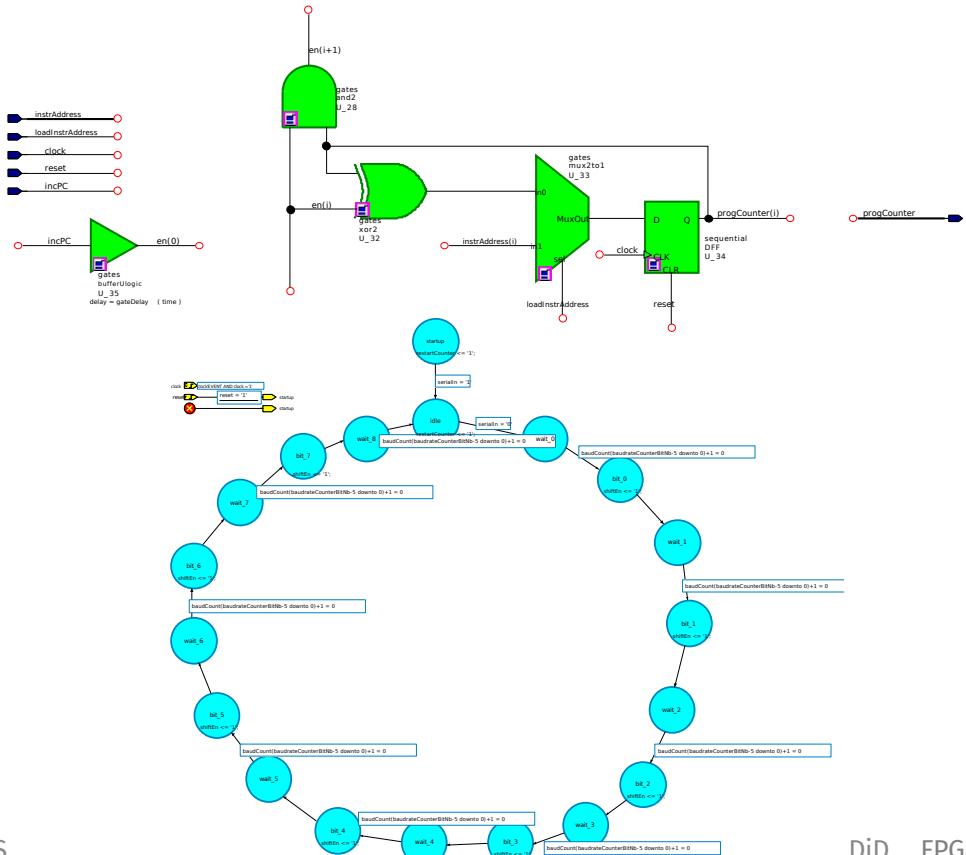
# FPGA Networks





# Design Flow

# Design Flow Implementation



```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.NUMERIC_STD.all;
```

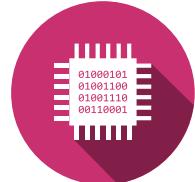
```
ENTITY audioAmp_FPGA IS
  GENERIC(
    gainBitNb    positive := 8
```

```

PORT(
    ADC_bClk           IN    std_logic;
    ADC_data            IN    std_logic;
    ADC_lrck            IN    std_logic;
    ADC_ovf_l           IN    std_logic;
    ADC_ovf_r           IN    std_logic;
    DAC_zero             IN    std_logic;
    clock                IN    std_ulogic;
    functionSelect       IN    std_logic;
    gain_n               IN    unsigned (gainBitNb-1 DOWNTO 0);
    reset_n              IN    std_ulogic;
    ADC_DAC_rst_n       OUT   std_logic;
    ADC_bypass           OUT   std_logic;
    ADC_osr              OUT   std_ulogic_vector (2 DOWNTO 0);
    ADC_sClk             OUT   std_logic;
    DAC_bclk             OUT   std_logic;
    DAC_data              OUT   std_logic;
    DAC_lrck             OUT   std_logic;
    DAC_mute              OUT   std_logic;
    DAC_sclk             OUT   std_logic;
    LED1                 OUT   std_logic;
    audioPwmL            OUT   std_ulogic;
    audioPwmL_n          OUT   std_ulogic;
    audioPwmR            OUT   std_ulogic;
    audioPwmR_n          OUT   std_ulogic;
    stepUpPwm             OUT   std_ulogic;
    )

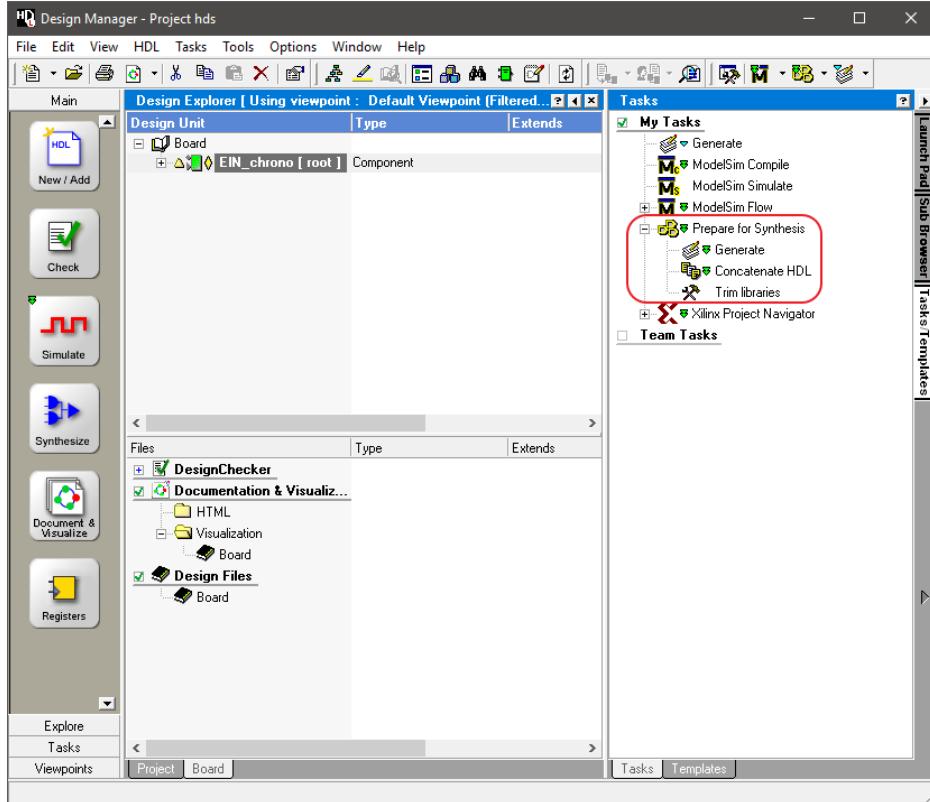
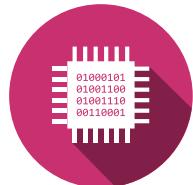
```

END audioAmp FPGA ;



# Design Flow

## Generation VHDL

A screenshot of the "Log Window" from the software. The window title is "Log Window". The log output is as follows:

```
gates/logic1
◆ Generating entity C:\work\git\Education\eln\projects\solution\eln_chrono\Libs\Gates\vhdl\Logic1_entity.vhd

sequential/DFF
◆ Generating entity C:\work\git\Education\eln\projects\solution\eln_chrono\Libs\Sequential\vhdl\dff_entity.vhd
◆ Generating architecture C:\work\git\Education\eln\projects\solution\eln_chrono\Prefs..\Board\vhdl\eln_chrono_struct.vhd

Generation completed successfully.

Current working directory is C:/work/git/Education/eln/projects/solution/eln_chrono/Scripts

Executing data preparation for plug-in Generic Concatenation

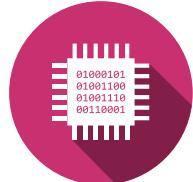
◆ Writing composite output file
'C:/work/git/Education/eln/projects/solution/eln_chrono/Prefs../Board/concat/concatenated.vhd'.

Running executable : $HDS_HOME\resources\perl\bin\perl.exe
Moving to initial directory "C:/work/git/Education/eln/projects/solution/eln_chrono/Board/concat"

Trimming library declarations from concatenated.vhd to eln_chrono.vhd
temporary file spec: eln_chrono.vhd.tmp
```

# Design Flow

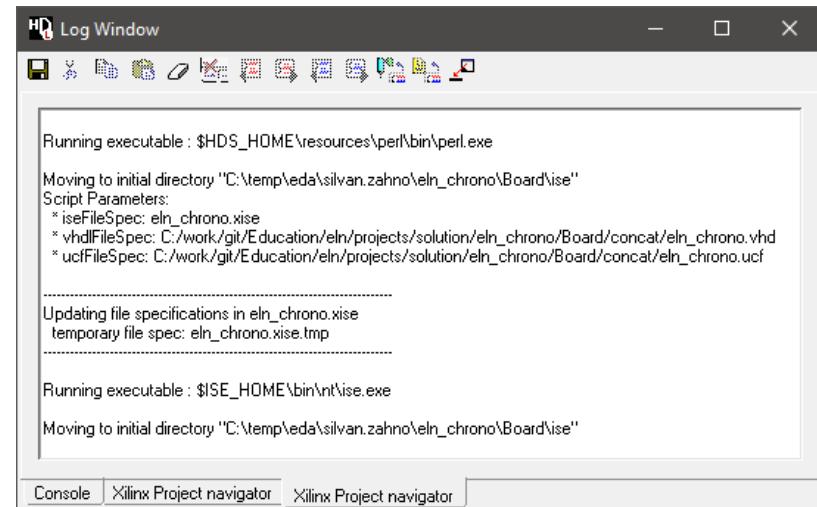
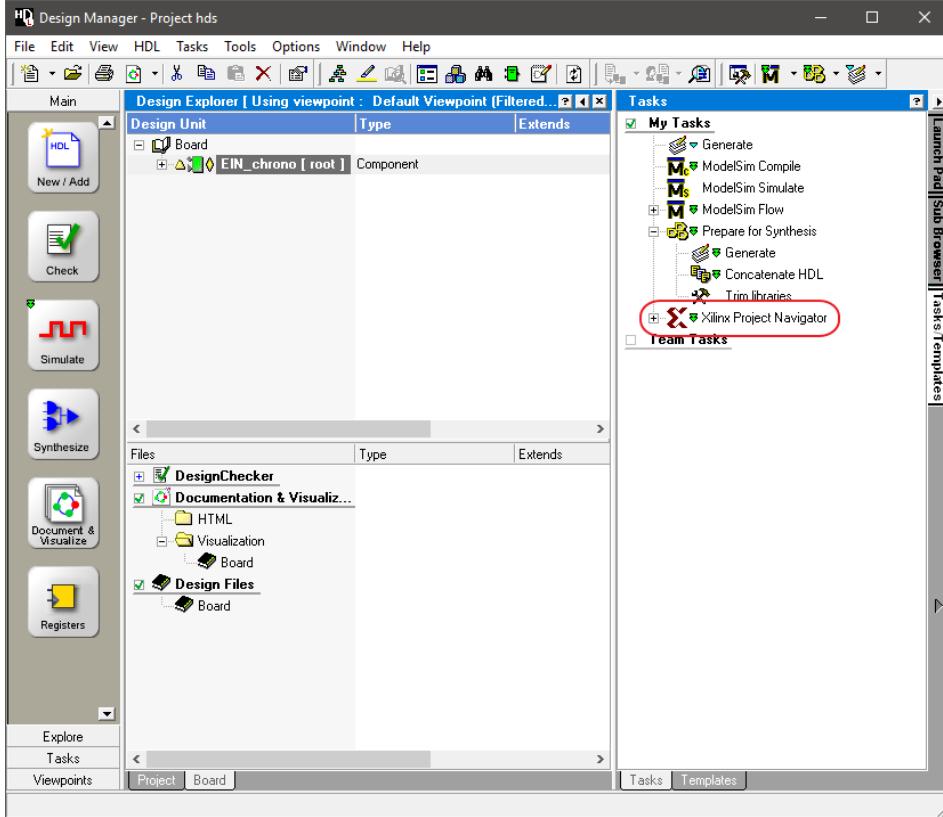
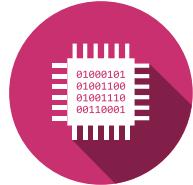
## Generation UCF



```
-----  
# Clock and reset  
#  
NET      "clock"          LOC = "A10";  
NET      "reset_n"         LOC = "A15"    | PULLUP;  
NET      "testMode"        LOC = "T10";  
  
-----  
# Buttons  
#  
NET      "restart_n"      LOC = "E8" ;  
NET      "start_n"         LOC = "G9" ;  
NET      "stop_n"          LOC = "F9" ;  
  
-----  
# LEDs_n  
#  
NET      "LED1"            LOC = "B16";  
NET      "LED2"            LOC = "A16";  
NET      "LEDs_n<1>"      LOC = "E7" ;  
NET      "LEDs_n<2>"      LOC = "B14";  
NET      "LEDs_n<3>"      LOC = "B13";  
NET      "LEDs_n<4>"      LOC = "B11";  
NET      "LEDs_n<5>"      LOC = "A8" ;  
NET      "LEDs_n<6>"      LOC = "C7" ;  
NET      "LEDs_n<7>"      LOC = "A14";  
NET      "LEDs_n<8>"      LOC = "A11";  
  
-----  
# Motor  
#  
NET      "motorOn1"        LOC = "B4" ;  
NET      "motorOn2"        LOC = "B3" ;  
NET      "coil1_n"          LOC = "G6" ;  
NET      "coil2_n"          LOC = "C5" ;  
NET      "coil3_n"          LOC = "C4" ;  
NET      "coil4_n"          LOC = "C3" ;  
  
NET      "sensor_n"        LOC = "A4" ;  
  
-----  
# Globals  
#  
NET  "*" IOSTANDARD = LVCMOS33;
```

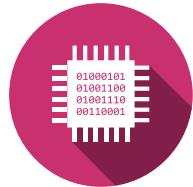
# Design Flow

## Starting Xilinx ISE



# Design Flow

## Xilinx ISE



ISE Project Navigator (P.20131013) - C:\temp\eda\silvan.zahno\eln\_chrono\Board\ise\eln\_chrono.xise - [Design Summary (Programming File Generated)]

File Edit View Project Source Process Tools Window Layout Help

Design Overview

- View: Implementation Simulation
- Hierarchy
  - eln\_chrono
    - xc3s500e-5fg320
      - eln\_chrono - struct (eln\_chrono.vhd)
- No Processes Running
- Processes: Eln\_chrono - struct
- Design Summary/Reports
  - Design Utilities
  - User Constraints
  - Synthesizer - XST
    - View RTL Schematic
    - View Technology Schematic
    - Check Syntax
    - Generate Post-Synthesis Simulation Model
  - Implement Design
    - Translate
      - Generate Post-Translate Simulation Model
    - Map
      - Generate Post-Map Static Timing
      - Manually Place & Route (FPGA Editor)
      - Generate Post-Map Simulation Model
    - Place & Route
      - Generate Post-Place & Route Static Timing
        - Analyze Timing / Floorplan Design (PlanAhead)
        - View/Edit Routed Design (FPGA Editor)
        - Analyze Power Distribution (XPower Analyzer)
        - Generate Text Power Report
        - Generate Post-Place & Route Simulation Model
        - Generate IBIS Model
        - Back-annotate Pin Locations
      - Configure Target Device
      - Analyze Design Using ChipScope

**eln\_chrono Project Status (11/01/2019 - 11:01:06)**

<b>Project File:</b> eln_chrono.xise	<b>Parser Errors:</b> No Errors
<b>Module Name:</b> Eln_chrono	<b>Implementation State:</b> Programming File Generated
<b>Target Device:</b> xc3s500e-5fg320	<b>Errors:</b> No Errors
<b>Product Version:</b> ISE 14.7	<b>Warnings:</b> 126 Warnings (126 new)
<b>Design Goal:</b> Balanced	<b>Routing Results:</b> All Signals Completely Routed
<b>Design Strategy:</b> Xilinx Default (unlocked)	<b>Timing Constraints:</b> All Constraints Met
<b>Environment:</b> System Settings	<b>Final Timing Score:</b> 0 (Timing Report)

**Device Utilization Summary**

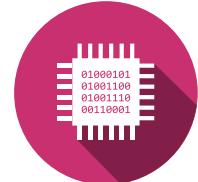
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	178	9,312	1%	
Number of 4 input LUTs	688	9,312	7%	
Number of occupied Slices	421	4,656	9%	
Number of Slices containing only related logic	421	421	100%	
Number of Slices containing unrelated logic	0	421	0%	
Total Number of 4 input LUTs	784	9,312	8%	
Number used as logic	501			
Number used as a route-thru	96			
Number used as 16x1 RAMs	185			
Number used for 32x1 RAMs	2			
Number of bonded IOBs	29	232	12%	
Number of BUFMUXes	1	24	4%	
Average Fanout of Non-Clock Nets	4.10			

**Performance Summary**

<b>Final Timing Score:</b> 0 (Setup: 0, Hold: 0)	<b>Pinout Data:</b> Pinout Report
<b>Routing Results:</b> All Signals Completely Routed	<b>Clock Data:</b> Clock Report
<b>Timing Constraints:</b> All Constraints Met	

# Design Flow

## Xilinx ISE Report



EIN_chrono Project Status (11/01/2019 - 11:01:06)			
<b>Project File:</b>	eln_chrono.xise	<b>Parser Errors:</b>	No Errors
<b>Module Name:</b>	EIN_chrono	<b>Implementation State:</b>	Programming File Generated
<b>Target Device:</b>	xc3s500e-5fg320	<b>*Errors:</b>	No Errors
<b>Product Version:</b>	ISE 14.7	<b>*Warnings:</b>	126 Warnings (126 new)
<b>Design Goal:</b>	Balanced	<b>*Routing Results:</b>	All Signals Completely Routed
<b>Design Strategy:</b>	<a href="#">Xilinx Default (unlocked)</a>	<b>*Timing Constraints:</b>	All Constraints Met
<b>Environment:</b>	<a href="#">System Settings</a>	<b>*Final Timing Score:</b>	0 ( <a href="#">Timing Report</a> )

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	178	9,312	1%	
Number of 4 input LUTs	688	9,312	7%	
Number of occupied Slices	421	4,656	9%	
Number of Slices containing only related logic	421	421	100%	
Number of Slices containing unrelated logic	0	421	0%	
Total Number of 4 input LUTs	784	9,312	8%	
Number used as logic	501			
Number used as a route-thru	96			
Number used as 16x1 RAMs	185			
Number used for 32x1 RAMs	2			
Number of bonded IOBs	29	232	12%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	4.10			

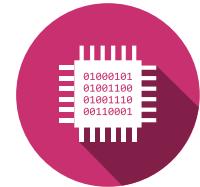
Performance Summary			
<b>Final Timing Score:</b>	0 (Setup: 0, Hold: 0)	<b>Pinout Data:</b>	<a href="#">Pinout Report</a>
<b>Routing Results:</b>	<a href="#">All Signals Completely Routed</a>	<b>Clock Data:</b>	<a href="#">Clock Report</a>
<b>Timing Constraints:</b>	<a href="#">All Constraints Met</a>		

Detailed Reports					
Report Name	Status	Generated	Errors	Warnings	Infos
<a href="#">Synthesis Report</a>	Current	Fri Nov 1 11:00:10 2019	0	<a href="#">62 Warnings (62 new)</a>	<a href="#">204 Infos (204 new)</a>
<a href="#">Translation Report</a>	Current	Fri Nov 1 11:00:14 2019	0	0	0
<a href="#">Map Report</a>	Current	Fri Nov 1 11:00:25 2019	0	<a href="#">60 Warnings (60 new)</a>	<a href="#">4 Infos (4 new)</a>
<a href="#">Place and Route Report</a>	Current	Fri Nov 1 11:00:54 2019	0	<a href="#">3 Warnings (3 new)</a>	<a href="#">2 Infos (2 new)</a>
Power Report					
<a href="#">Post-PAR Static Timing Report</a>	Current	Fri Nov 1 11:00:57 2019	0	0	<a href="#">6 Infos (6 new)</a>
<a href="#">Bitgen Report</a>	Current	Fri Nov 1 11:01:04 2019	0	<a href="#">1 Warning (1 new)</a>	0

Secondary Reports		
Report Name	Status	Generated
<a href="#">WebTalk Report</a>	Current	Fri Nov 1 11:01:04 2019
<a href="#">WebTalk Log File</a>	Current	Fri Nov 1 11:01:06 2019

# Design Flow

## Report Synthesis



```
=====
*          Design Summary          *
=====
Top Level Output File Name : ElN_chrono.ngc
Primitive and Black Box Usage:
-----
# BELS           : 889
# BUF            : 1
# GND            : 1
# INV            : 17
# LUT1           : 95
# LUT2           : 47
# LUT2_D          : 1
# LUT2_L          : 3
# LUT3           : 199
# LUT3_D          : 6
# LUT3_L          : 3
# LUT4           : 193
# LUT4_D          : 16
# LUT4_L          : 15
# MUXCY          : 52
# MUXF5          : 141
# MUXF6          : 51
# MUXF7          : 7
# VCC            : 1
# XORCY          : 40
# FlipFlops/Latches
#   FDC           : 48
#   FDCE          : 71
#   FDE           : 44
#   FDP            : 4
#   FDPD           : 11
#   RAMS           : 187
#   RAM16X1D       : 187
# Clock Buffers
#   BUFGP          : 1
#   IO Buffers      : 27
#   IBUF            : 6
#   OBUF            : 21

Device utilization summary:
-----
Selected Device : 3s500efg320-5

Number of Slices:          624 out of 4656 13%
Number of Slice Flip Flops: 178 out of 9312 1%
Number of 4 input LUTs:
  Number used as logic:    595
  Number used as RAMs:     374
Number of IOs:              29
Number of bonded IOBs:      28 out of 232 12%
Number of GCLKs:            1 out of 24 4%
```

=====
\* Timing Report \*
=====

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.  
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT  
GENERATED AFTER PLACE-and-ROUTE.

*Clock Information:*

-----

<i>Clock Signal</i>	/ Clock buffer(FF name) / Load /
clock	/ BUFGP / 365 /

-----

*Asynchronous Control Signals Information:*

-----

<i>Control Signal</i>	/ Buffer(FF name)
/ Load /	
-----	
resetSync(I7/out11_INV_0:0)	/
NONE(I0/I_lcdCtl/I_ser/resetCounter_0)/ 133 /	
reset(I1/out11_INV_0:0)	/ NONE(I6/Q)
/ 1 /	

-----

*Timing Summary:*

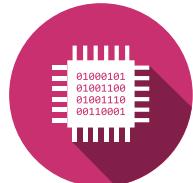
-----

Speed Grade: -5

Minimum period: 10.079ns (Maximum Frequency: 99.215MHz)  
Minimum input arrival time before clock: 5.798ns  
Maximum output required time after clock: 10.466ns  
Maximum combinational path delay: 8.860ns

# Design Flow

## Report Place & Route



### Design Information

```
Command Line : map -intstyle ise -p xc3s500e-fg320-5 -cm area -ir off -pr off
-c 100 -o ElN_chrono_map.ncd ElN_chrono.ngd ElN_chronopcf
Target Device : xc3s500e
Target Package : fg320
Target Speed : -5
Mapper Version : spartan3e -- $Revision: 1.55 $
Mapped Date : Fri Nov 01 11:00:17 2019
```

### Design Summary

Number of errors:	0
Number of warnings:	60
<b>Logic Utilization:</b>	
Number of Slice Flip Flops:	178 out of 9,312 1%
Number of 4 input LUTs:	688 out of 9,312 7%
<b>Logic Distribution:</b>	
Number of occupied Slices:	421 out of 4,656 9%
Number of Slices containing only related logic:	421 out of 421 100%
Number of Slices containing unrelated logic:	0 out of 421 0%
*See NOTES below for an explanation of the effects of unrelated logic.	
Total Number of 4 input LUTs:	784 out of 9,312 8%
Number used as logic:	501
Number used as a route-thru:	96
Number used as 16x1 RAMs:	185
Number used for 32x1 RAMs:	2
(Two LUTs used per 32x1 RAM)	

The Slice Logic Distribution report is not meaningful if the design is over-mapped for a non-slice resource or if Placement fails.

Number of bonded IOBs:	29 out of 232 12%
Number of BUFGMUXs:	1 out of 24 4%

Average Fanout of Non-Clock Nets: 4.10

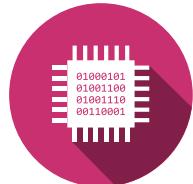
Peak Memory Usage: 300 MB  
 Total REAL time to MAP completion: 8 secs  
 Total CPU time to MAP completion: 2 secs

### Design Summary Report:

Number of External IOBs	29 out of 232 12%
Number of External Input IOBs	8
Number of External Input IBUFs	8
Number of LOCed External Input IBUFs	8 out of 8 100%
Number of External Output IOBs	21
Number of External Output IOBs	21
Number of LOCed External Output IOBs	21 out of 21 100%
Number of External Bidir IOBs	0
Number of BUFGMUXs	1 out of 24 4%
Number of Slices	421 out of 4656 9%
Number of SLICEMs	111 out of 2328 4%
<b>Overall effort level (-ol): High</b>	
<b>Placer effort level (-pl): High</b>	
<b>Placer cost table entry (-t): 1</b>	
<b>Router effort level (-rl): High</b>	

# Design Flow

## Programming



ISE iMPACT (P.20131013) - [Boundary Scan]

File Edit View Operations Output Debug Window Help

iMPACT Flows

- Boundary Scan
- SystemACE
- Create PROM File (PROM File Format...)
- WebTalk Data

Right click

- Add Xilinx Device... Ctrl+D
- Add Non-Xilinx Device... Ctrl+K
- Initialize Chain Ctrl+I**
- Cable Auto Connect
- Cable Setup...
- Output File Type

Boundary Scan

No Cable Connection | No File Open |

ISE iMPACT (P.20131013) - [Boundary Scan]

File Edit View Operations Output Debug Window Help

iMPACT Flows

- Boundary Scan
- SystemACE
- Create PROM File (PROM File Format...)
- WebTalk Data

Right click device to select operations

The diagram shows a boundary scan chain connecting two Xilinx devices: an xc04s bypass chip and an xc3s500e bypass chip. The connection is made through their TDI (Test Data In) and TDO (Test Data Out) pins. The xc04s chip is labeled 'bypass' and the xc3s500e chip is also labeled 'bypass'. A blue bracket above the chain indicates the selection of both devices for operations.

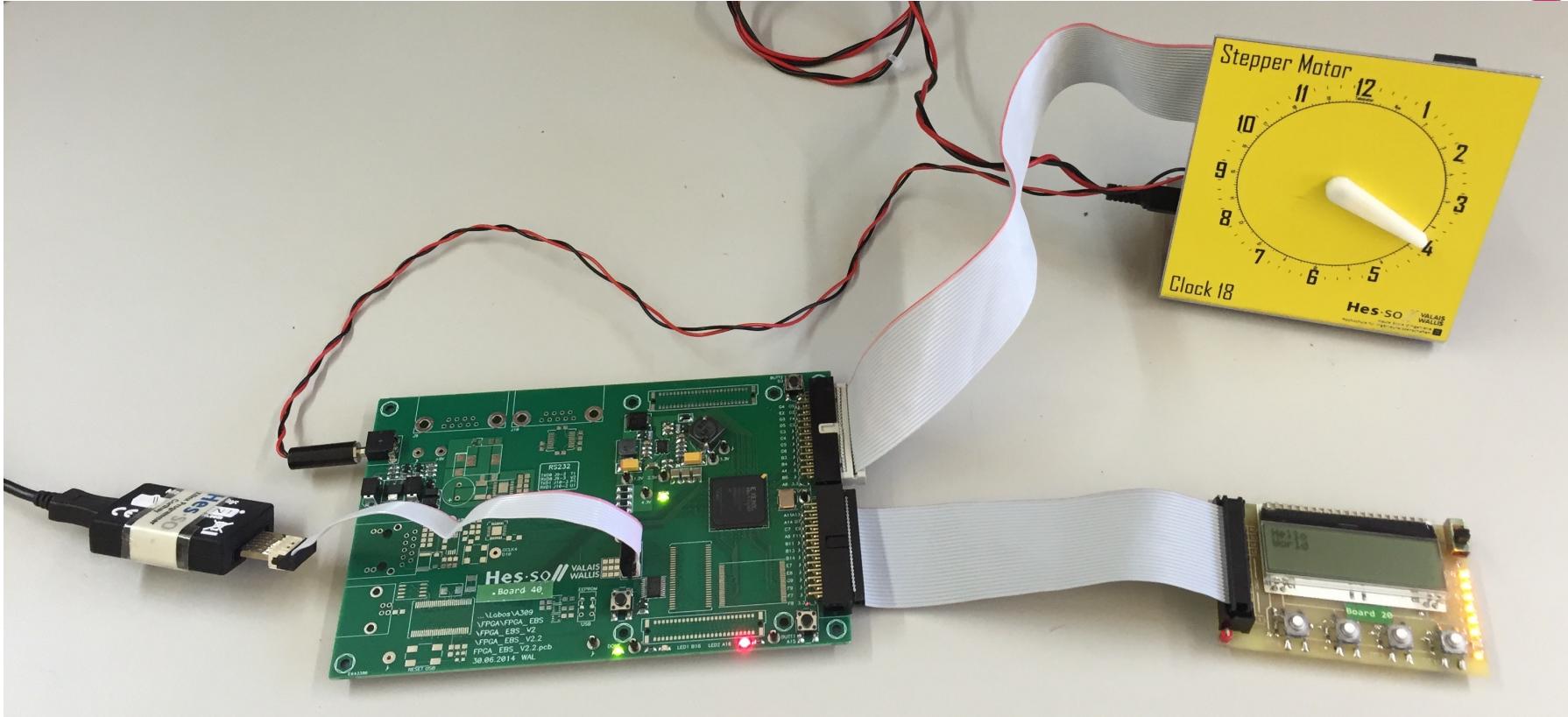
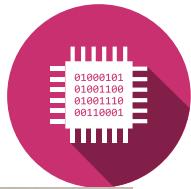
TDI ————— (xc04s bypass) ————— (xc3s500e bypass) ————— TDO

Boundary Scan

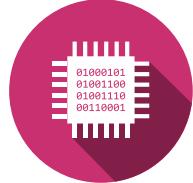
Configuration | Platform Cable USB | 6 MHz | ush-hs |

# Design Flow

## Programming

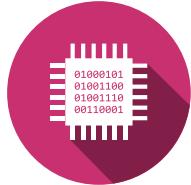


# FPGA



- We now know everything about:
  - ASIC's
  - FPGA's
  - Implementation

# References



- [War17] (English) FPGA Designer Warrior  
[http://blog.aku.edu.tr/ismailkoyuncu/files/2017/04/01\\_ebook.pdf](http://blog.aku.edu.tr/ismailkoyuncu/files/2017/04/01_ebook.pdf)
- [Int19] (English) Intel FPGA Website  
<https://www.intel.com/content/www/us/en/products/programmable.html>
- [Xil19] (English) Xilinx FPGA Website  
<https://www.xilinx.com/>
- [Act19] (English) Actel FPGA Website  
<https://www.microsemi.com/product-directory/1636-fpga-soc>

WHY ARE THERE MIRRORS ABOVE BEDS

WHY DO I SAY UH

WHY IS SEA SALT BETTER

WHY ARE THERE TREES IN THE MIDDLE OF FIELDS

WHY IS THERE NOT A POKEMON MMO

WHY IS THERE LAUGHING IN TV SHOWS

WHY ARE THERE DOORS ON THE FREEWAY

WHY ARE THERE SO MANY SVHOST-EXE RUNNING

WHY AREN'T ANY COUNTRIES IN ANTARCTICA

WHY ARE THERE SCARY SOUNDS IN MINECRAFT

WHY IS THERE KICKING IN MY STOMACH

WHY ARE THERE TWO SLASHES AFTER HTTP

WHY ARE THERE CELEBRITIES

WHY DO SNAKES EXIST

WHY DO OYSTERS HAVE PEARLS

WHY ARE DUCKS CALLED DUCKS

WHY DO THEY CALL IT THE CLAP

WHY ARE KYLE AND CARTMAN FRIENDS

WHY IS THERE AN ARROW ON AANG'S HEAD

WHY ARE TEXT MESSAGES BLUE

WHY ARE THERE MUSTACHES ON CLOTHES

WHY WUBA LUBBA DUB DUB MEANING

WHY IS THERE A WHALE AND A POT FALLING

WHY ARE THERE SO MANY BIRDS IN SWISS

WHY IS THERE SO LITTLE RAIN IN WALLIS

WHY IS WALLIS WEATHER FORECAST ALWAYS WRONG

WHY ARE THERE BRIDES/MAIDS

WHY DO DYING PEOPLE REACH UP

HOW FAST IS LIGHTSPEED

WHY ARE OLD KLINGONS DIFFERENT

WHY ARE THERE SQUIRRELS

WHY ARE THERE TINY SPIDERS IN MY HOUSE

WHY DO SPIDERS COME INSIDE

WHY ARE THERE HUGE SPIDERS IN MY HOUSE

WHY ARE THERE LOTS OF SPIDERS IN MY HOUSE

WHY ARE THERE SPIDERS IN MY ROOM

WHY ARE THERE SO MANY SPIDERS IN MY ROOM

WHY DO SPIDER BITES ITCH

WHY IS DYING SO SCARY

WHY IS THERE NO GPS IN LAPTOPS

WHY DO KNEES CLICK

WHY IS THERE CAFFEINE IN MY SHAMPOO

WHY HAVE DINOSAURS NO FUR

WHY ARE SWISS AFRAID OF DRAGONS

WHY IS HTTPS CROSSED OUT IN RED

WHY IS THERE A LINE THROUGH HTTPS

WHY IS THERE A RED LINE THROUGH HTTPS ON TWITTER

WHY IS HTTPS IMPORTANT

WHY ARE THERE WEEKS

WHY DO I FEEL DIZZY

# QUESTIONS

CAN BE ASKED BY ANYONE ANYTIME

WHY AREN'T MY ARMS GROWING



WHY ARE THERE SO MANY CROWS IN ROCHESTER

WHY IS TO BE OR NOT TO BE FUNNY

WHY DO CHILDREN GET CANCER

WHY IS POSEIDON ANGRY WITH ODYSSEUS

WHY IS THERE ICE IN SPACE

WHY ARE THERE ANTS IN MY LAPTOP

WHY IS THERE AN OWL IN MY BACKYARD

WHY IS THERE AN OWL OUTSIDE MY WINDOW

WHY IS THERE AN OWL ON THE DOLLAR BILL

WHY DO OWLS ATTACK PEOPLE

WHY ARE FPGA's EVERYWHERE

WHY ARE THERE HELICOPTERS CIRCLING MY HOUSE

WHY ARE THERE GODS

WHY ARE THERE TWO SPOCKS

WHY ARE THERE DUCKS IN MY POOL

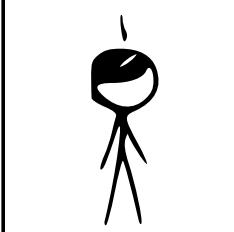
WHY IS JESUS WHITE

WHY IS THERE LIQUID IN MY EAR

WHY DO Q TIPS FEEL GOOD

WHY DO PEOPLE DIE

WHY ARE THERE GHOSTS



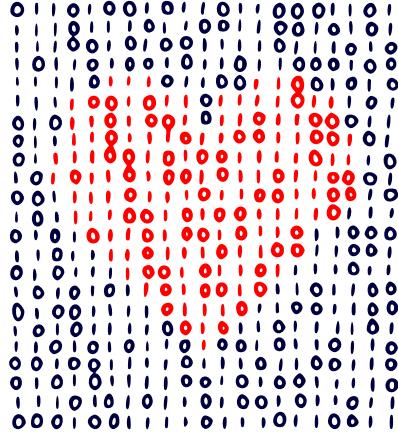
WHAT IS https://xkcd.com/1256/

WHY DO THEY SAY T-MINUS

WHY ARE THERE OBELISKS

WHY ARE WRESTLERS ALWAYS WET

WHY AREN'T THERE GUNS IN



Hes·so // VALAIS  
WALLIS



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Hochschule für Ingenieurwissenschaften

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