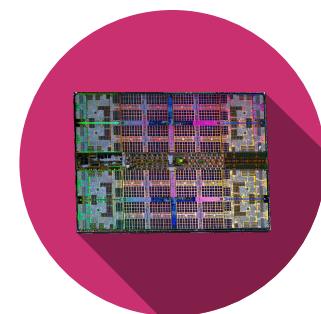


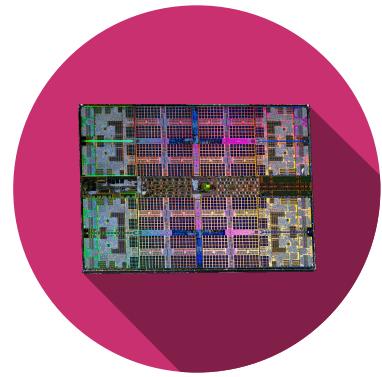


Computer Architecture Fundamentals Fun

Information and Communication Systems program

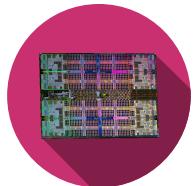
Silvan Zahno silvan.zahno@hevs.ch





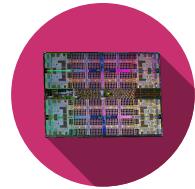
Binarysystem

Binary System

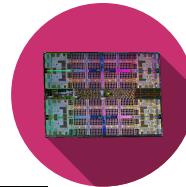
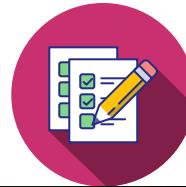


The diagram shows a horizontal line representing a number. Above the line, the word "Number" is written with a small triangle pointing to the line. Below the line, there is a bracket grouping several boxes. An arrow labeled "Digit" points from the word "Digit" to the first box in the group. The boxes are labeled a_{n-1} , a_{n-2} , ..., a_0 . There are also three empty boxes between the first group and the last two labels.

Bender's scare

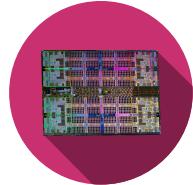


Bender's scare



Binary System

Naming conventions

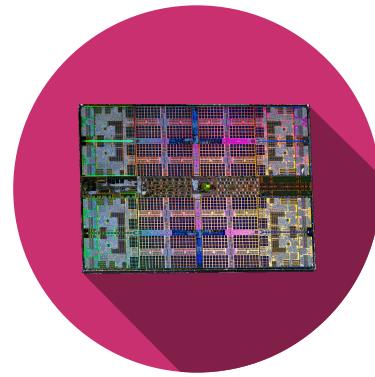


- 8 BIT make up one byte (octet)
 - Purely historical

- Using IEC standard:
 - 1 KiB = 1'024 bytes (Note: big K)
 - 1 MiB = 1'024 KiB = 1'048'576 bytes
 - 1 GiB = 1'024 MiB = 1'048'576 KiB = 1'073'741'824 bytes
- Using SI standard:
 - 1 kB = 1'000 bytes (Note: small k)
 - 1 MB = 1'000 kB = 1,000,000 bytes
 - 1 GB = 1'000 MB = 1'000'000 KB = 1'000'000'000 bytes

11110101

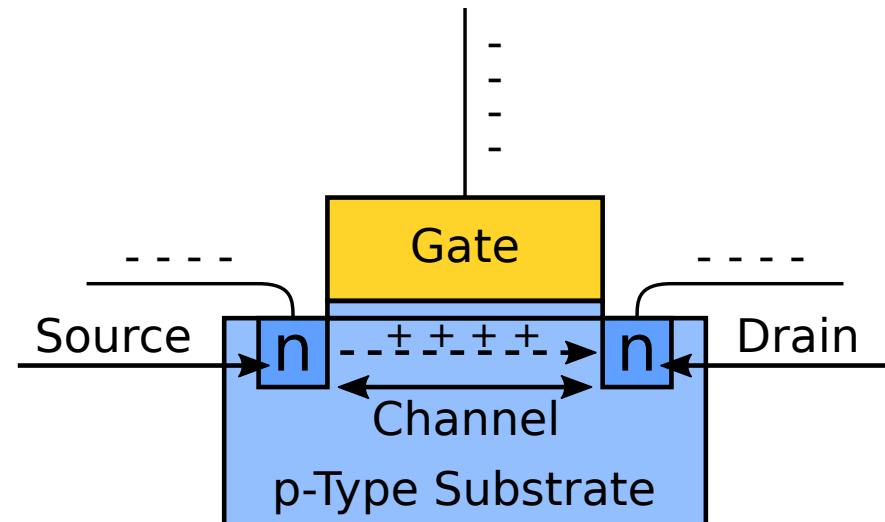
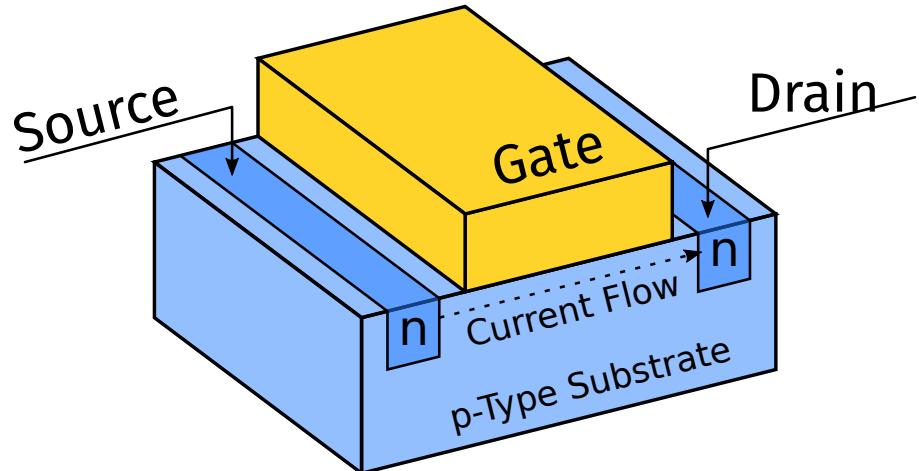
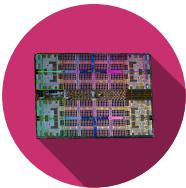
8 Bit = 1 Byte



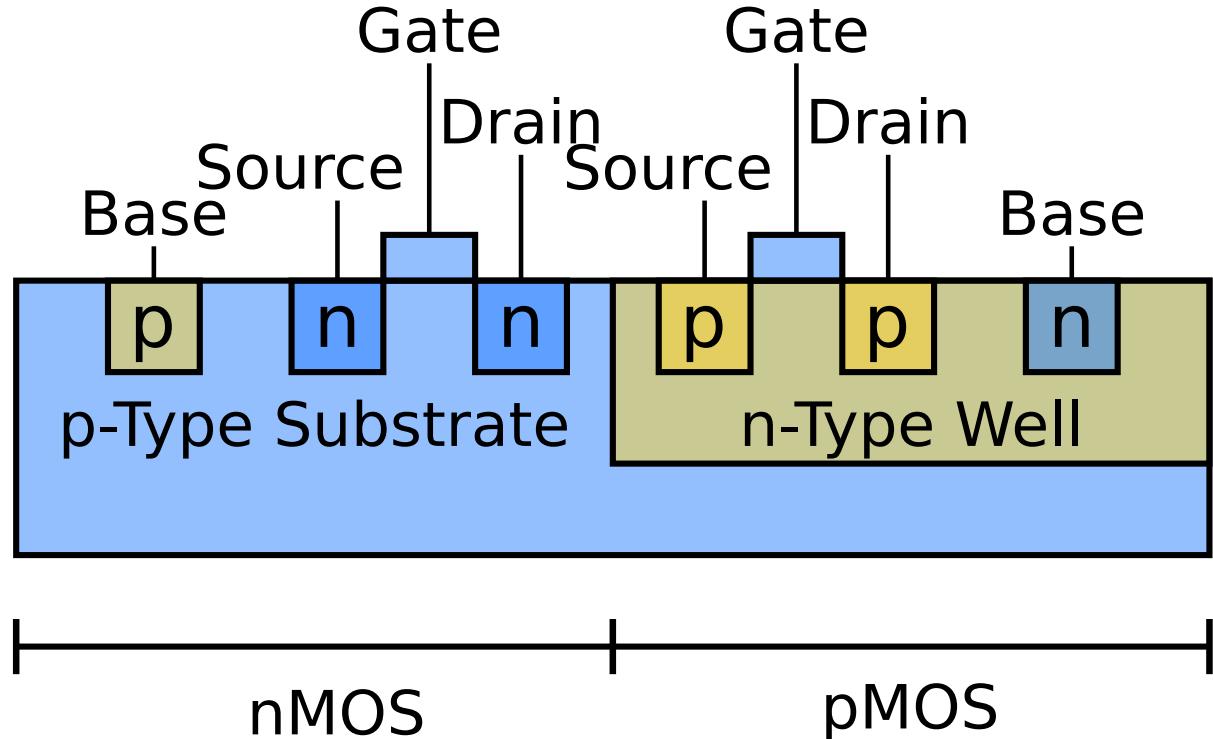
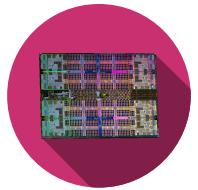
Transistor Level

Transistor Level

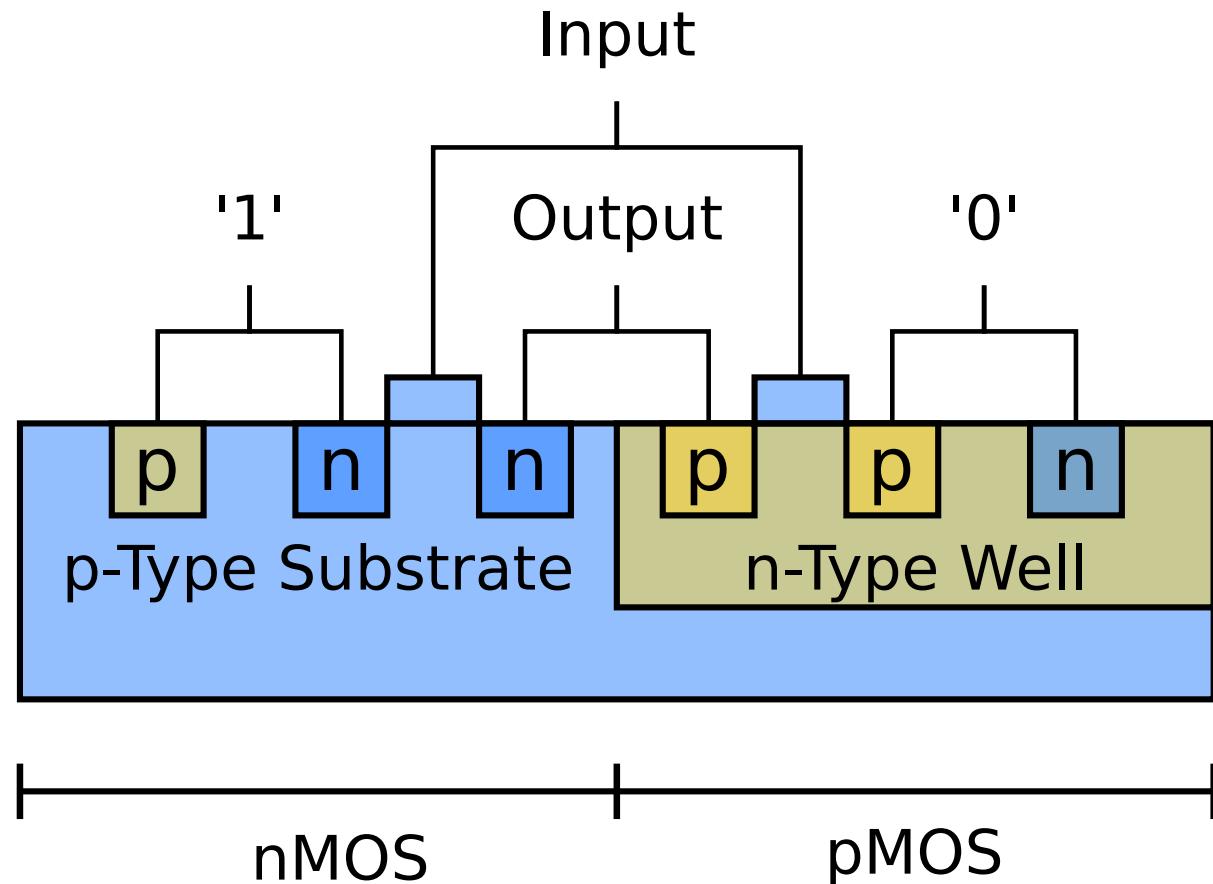
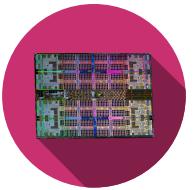
N-Channel



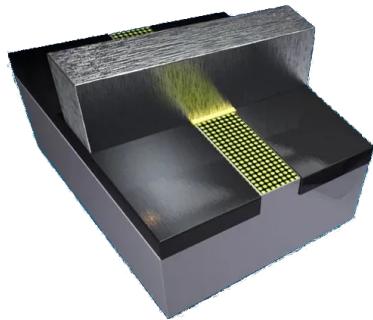
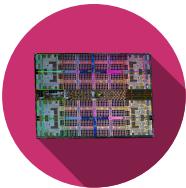
Transistor Level CMOS



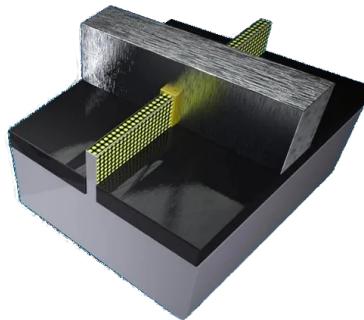
Transistor Level CMOS



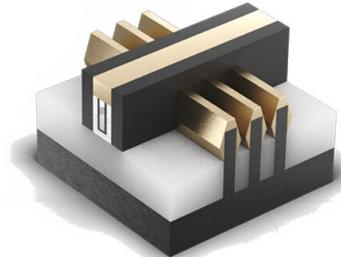
Transistor Level Evolution



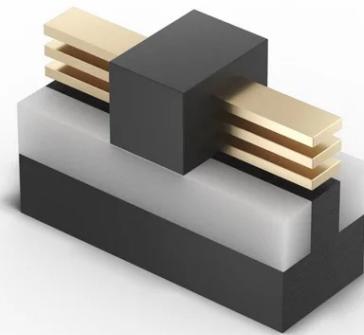
PlanarFET
32nm



TriGateFET
22nm

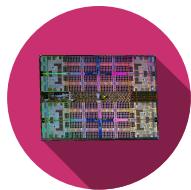


FinFET
22nm-10nm

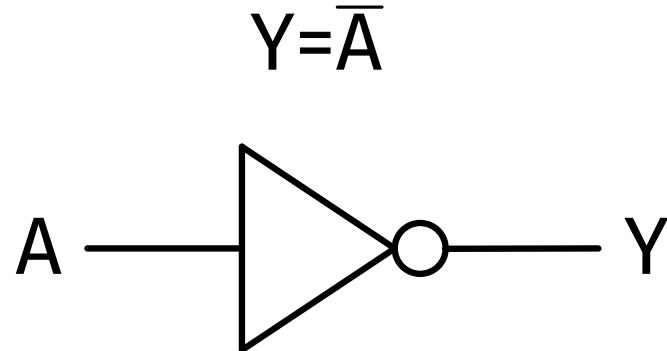
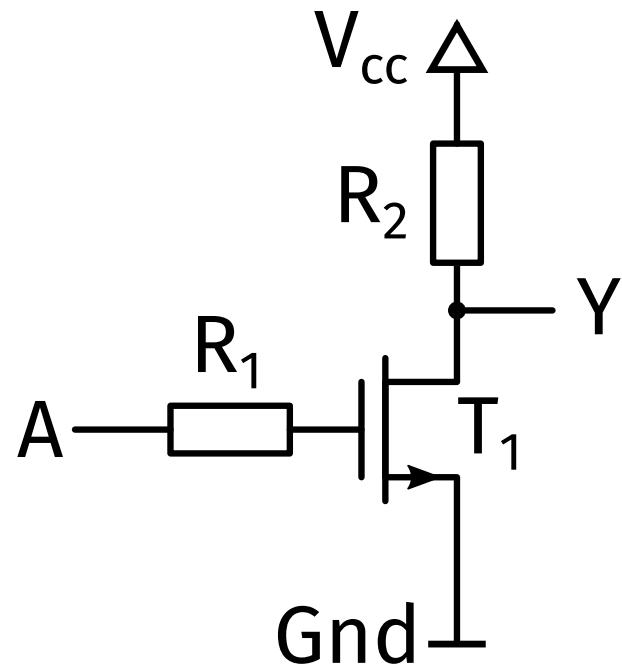


RibbonFET
4nm

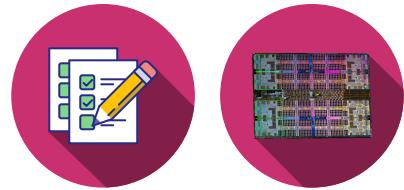
Transistor Level NOT



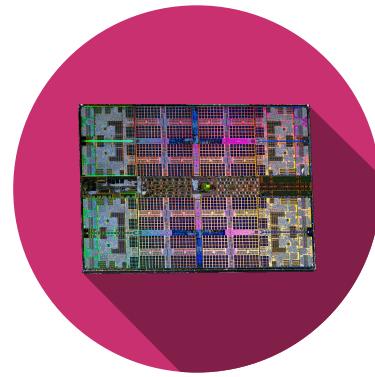
NOT



Transistor Level Exercise



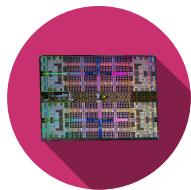
- Draw a AND and a OR on a transistor level



Performance Growth

Performance Growth

Moore's Law



Every 18 Month twice as many transistors for the same amount of money
- Gordon Moore -

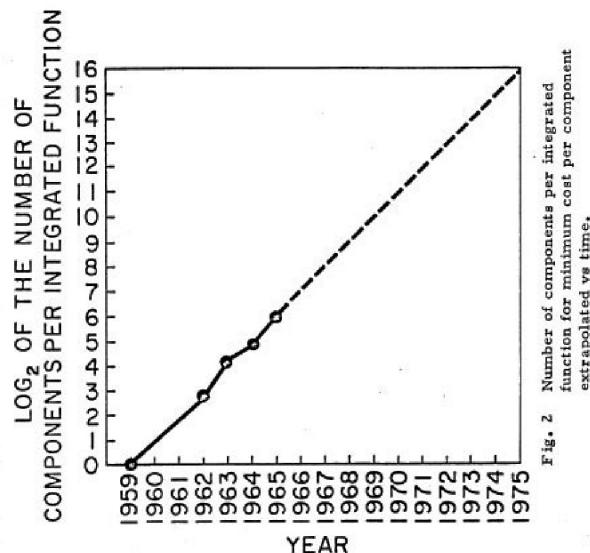
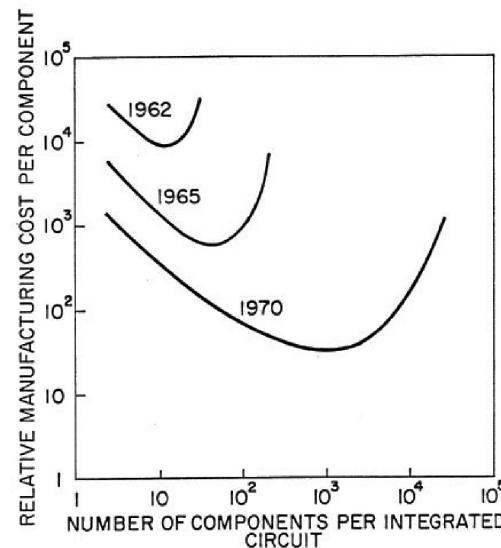
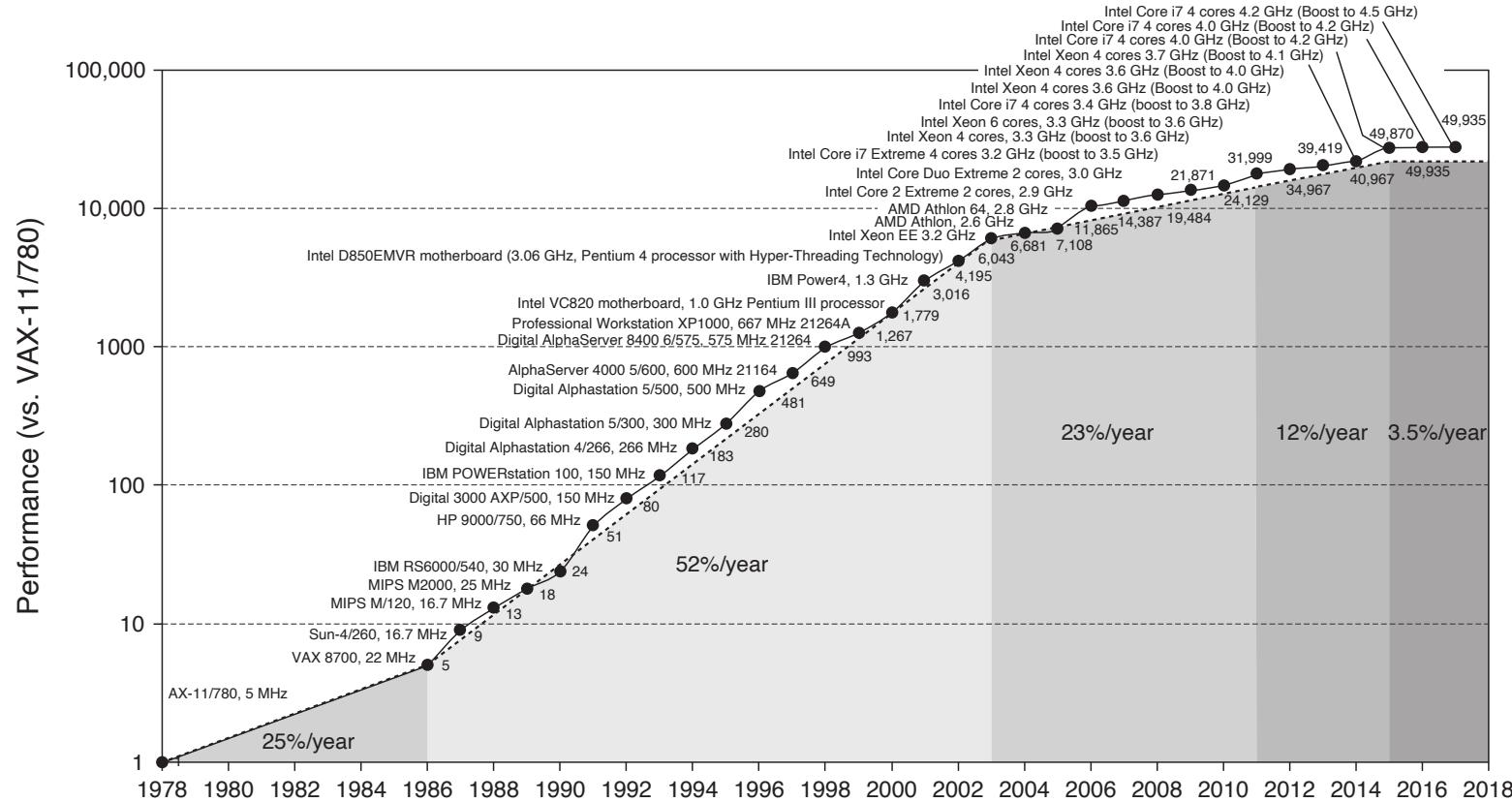
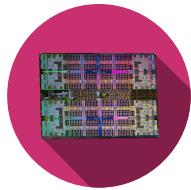


Fig. 2 Number of components per integrated function for minimum cost per component extrapolated vs time.



Performance Growth

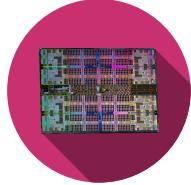
Moore's Law



[3]

Performance Growth

Moore's Law

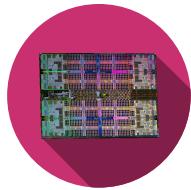


Revelations of Moore's Law

- Size of transistors halves every 18 months
- Number of transistors per chip doubles every 18 months
- Frequency doubles every 18 months
- (Performance doubles every 18 months)

Performance Growth

Dennard Scaling



Robert Dennard observed the scaling trends in 1974 and analyzed what they implied for the future if devices became $1/k$ smaller.

SCALING RESULTS FOR CIRCUIT PERFORMANCE

Device or Circuit Parameter	Scaling Factor
Device dimension t_{ox}, L, W	$1/k$
Doping concentration N_e	k
Voltage V	$1/k$
Current I	$1/k$
Capacitance $\epsilon A/t$	$1/k$
Delay time/circuit VC/I	$1/k$
Power dissipation/circuit VI	$1/k^2$
Power density VI/A	1

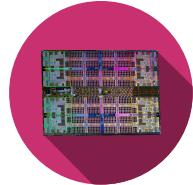
SCALING RESULTS FOR INTERCONNECTION LINES

Parameter	Scaling Factor
Line resistance, $R_L = \rho L/Wt$	k
Normalized voltage drop IR_L/V	k
Line response time $R_L C$	1
Line current density I/A	k

[1]

Performance Growth

Dennard Scaling



<i>Device or Circuit Parameters</i>	<i>Scaling Factor</i>
Device dimension t_{ox}, L, W	$1/k$
Doping concentration N_a	k
Voltage V	$1/k$
Current I	$1/k$
Capacitance A/t	$1/k$
Delay time/circuit VC/I	$1/k$
Power dissipation/circuit VI	$1/k^2$
Power density VI/A	1

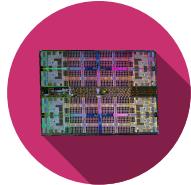
If we do scale these

We get these

=> Transistors run faster and use less power

Performance Growth

Moore's Law & Dennard Scaling



Outcome

- Chip can fit 2x as many transistors
- Transistors can run 2x as fast
- Each transistor uses $\frac{1}{4}$ the power

Limitation

- Physical doping limits
 - How many atoms can we fit in
- Human greed
 - Frequency was not scaled as intended
- Voltage limits
 - Below 0.6V silicon transistors behave differently

Performance Growth

Moore's Law & Dennard Scaling

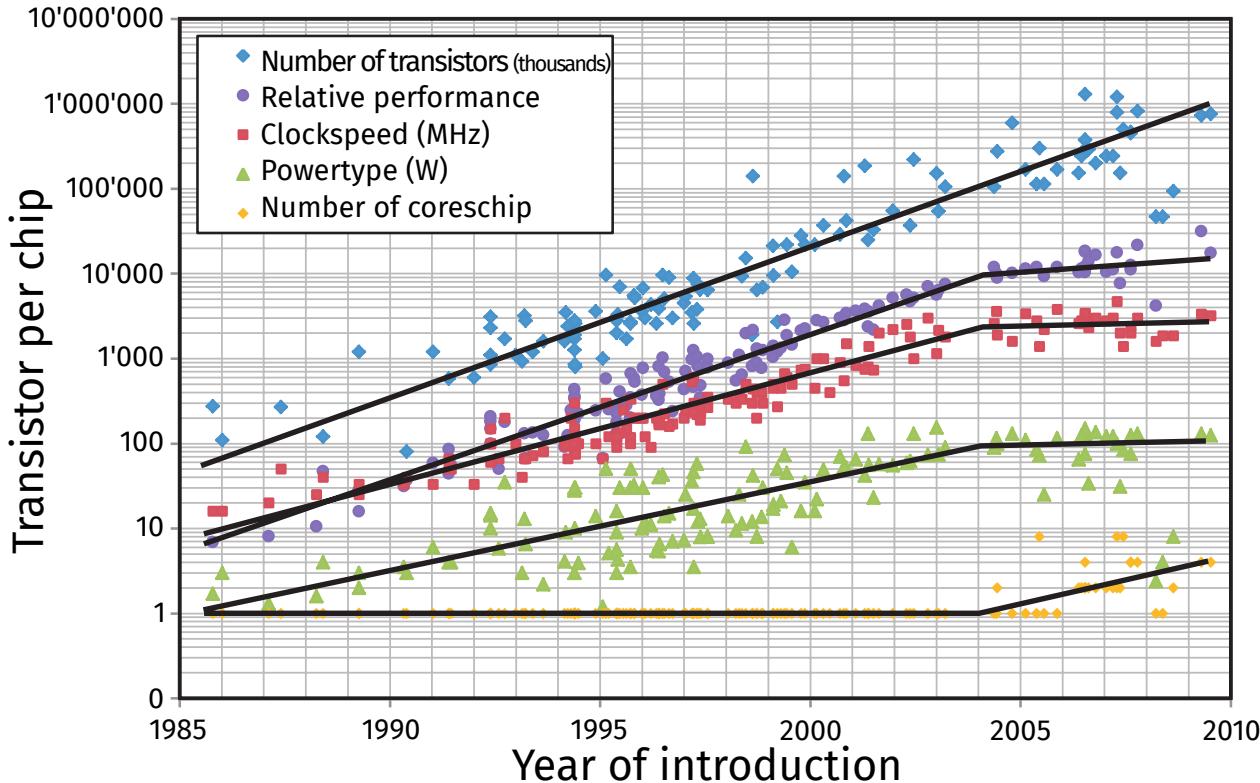
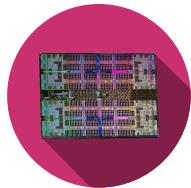
- Transistors keep getting smaller
- Voltage is not keeping pace
- Result: Power does not scale if we increase frequency
- Transition to multicore
 - Much slower performance rise
 - Much harder to realize gains (4cores != 4x faster)
- Today: Focus in powerconsumption



[4]

Performance Growth

Moore's Law & Dennard Scaling



Voltage/Frequency

- Can't reduce Voltage enough

The Power Wall

- Too expensive to cool anything hotter

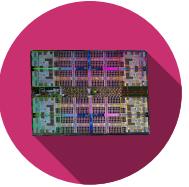
Result Multicore

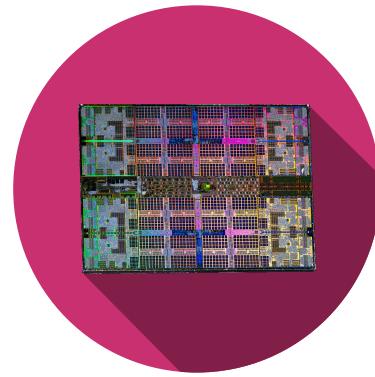
[4]

Performance Growth

Moore's Law & Dennard Scaling

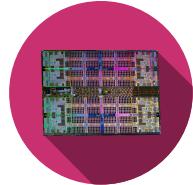
What is the main reason why the speed increase slowed down in recent years?





Power Consumption

Power Consumption of a Logic Gate



- $P_{total} = P_{dynamic} + P_{static}$
 - $P_{dynamic} = \alpha C V_{DD}^2 f$
 - $P_{static} = V_{DD} I_{DD}$

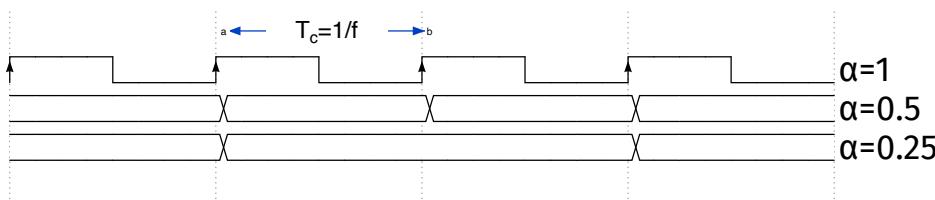
α = Activity factor

C = Capacitance of logic gate
and the wires

V_{DD} = Voltage

f = Clockfrequency

I_{DD} = leakage current or
quiescent supply current

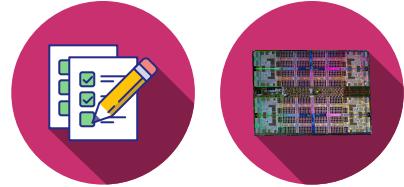


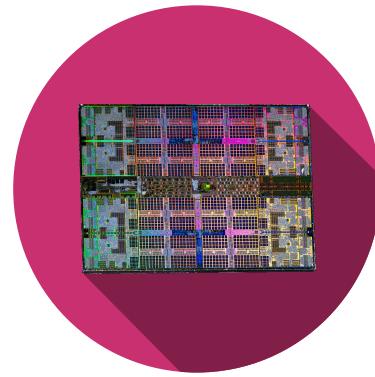
Power Consumption

Example

A particular cell phone has an **8W-hr battery** and operates at **0.707V**. Suppose that, when it is in use, the cell phone operates at **2GHz**. The total capacitance of the circuitry is **10 nF**, and the **activity factor** is **0.05**. When voice or data are active (**10% of its time in use**), it also broadcasts **3W** of power out of its antenna. When the phone is not in use, the dynamic power drops to almost zero because the signal processing is turned off. But the phone also draws **100mA** of quiescent current whether it is in use or not.

Determine the battery life of the phone (a) if it is not being used and (b) if it is being used continuously.





Fabrication

Fabrication

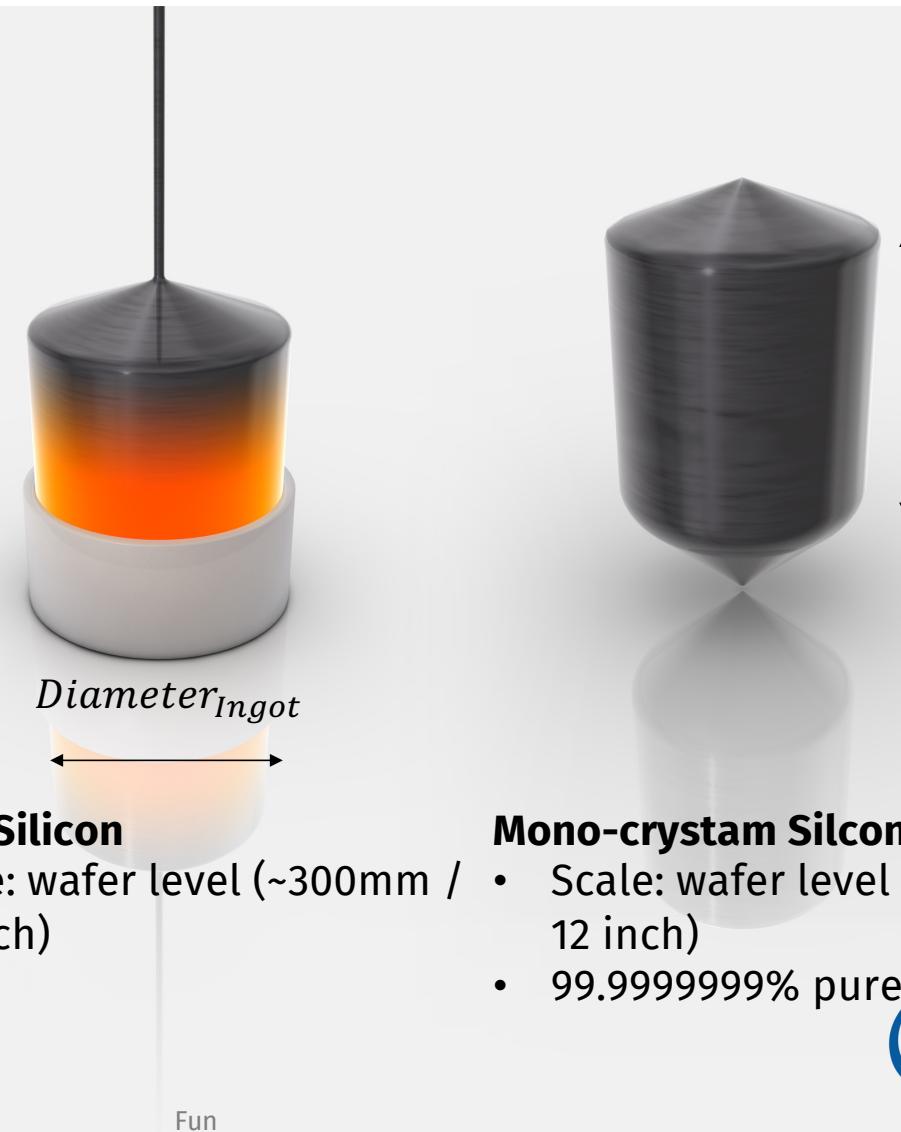
Sand to Ingot



Sand

- 25 % is Silicon
- Second most frequent chemical element in the earth's crust SiO_2

01 Sand Melted Into Ingot



Melted Silicon

- Scale: wafer level (~300mm / 12 inch)

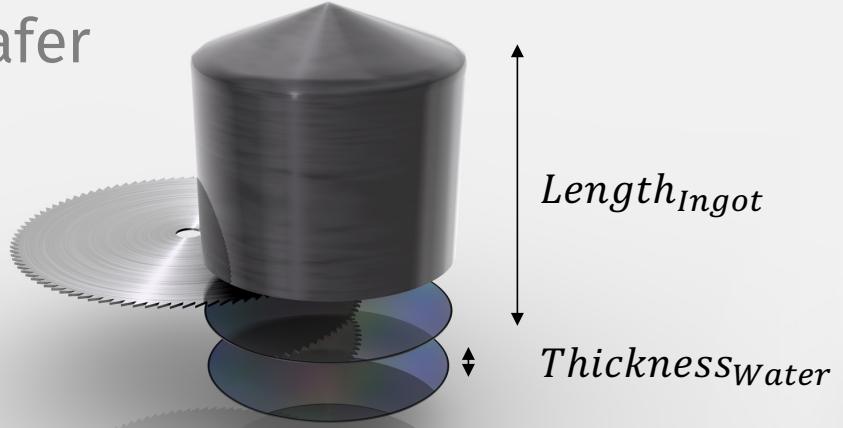
Mono-crystalline Silicon Ingot

- Scale: wafer level (~300mm / 12 inch)
- 99.999999% pure Silicon



Fabrication

Ingot to Wafer

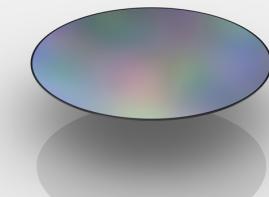


$$\#Wafer = \frac{Length_{Ingot}}{Thickness_{Wafer}}$$

Ingot Slicing

- Ingot is cut into individual discs called wafers

$Diameter_{Wafer}$



$$Area_{Wafer} = \pi * \left(\frac{Diameter_{Wafer}}{2} \right)^2$$

Wafer

- Polished for a flawless mirror finish

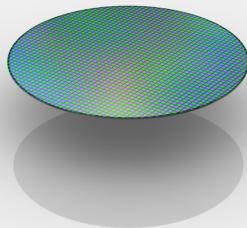
02 Ingot Sliced Into Wafer

Fun



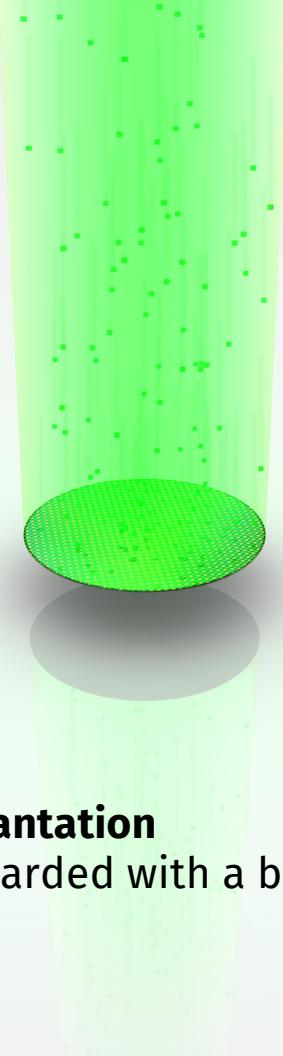
Fabrication

Ion Implantation



Applying Photo Resist

- Protects zones where no ions should be implanted



03 Ion Implantation

Ion Implantation

- Bombarded with a beam of ions

Removing Photo Resist

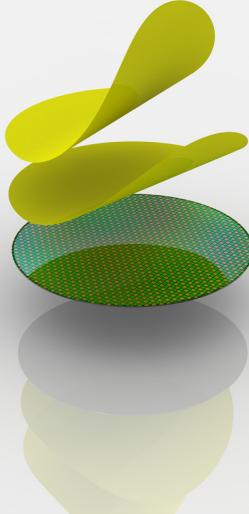
- Removing the protecting material

Fun



Fabrication

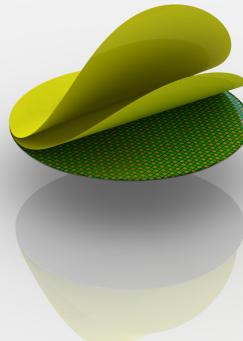
High-k Material Application



Applying High-k Dielectric

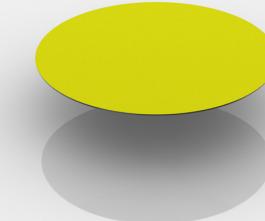
- Isolation between transistor's gate and its channel
- Improves energy-efficiency

04 High-k Material Application



Applying High-k Dielectric

- Multiple layers are applied



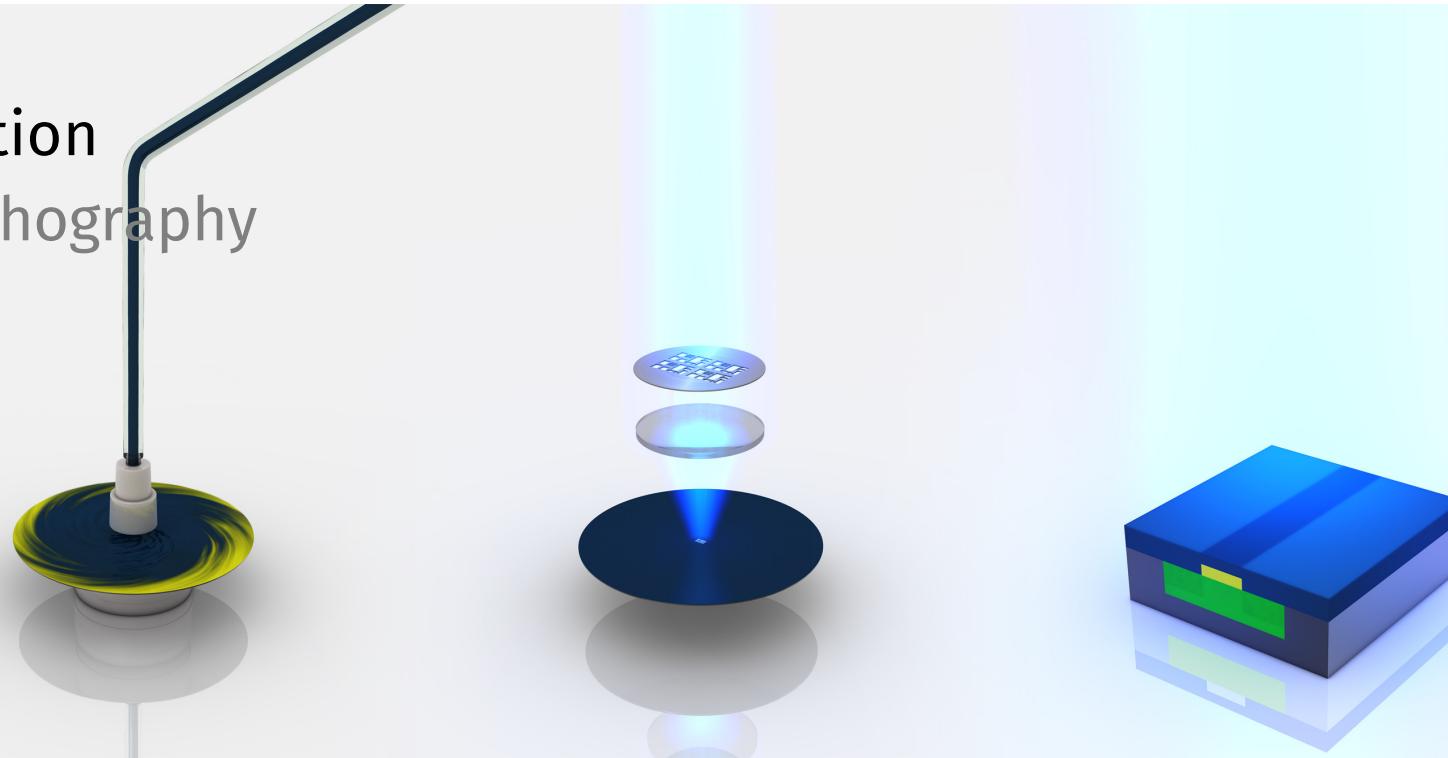
High-K Dielectric

- Less current leaks



Fabrication

Photolithography



Applying Photo Resist

- Very thin layer through spinning

05 Photolithographic „Printing“ Process

Exposure

- UV Light removes part of the applied film

Exposure

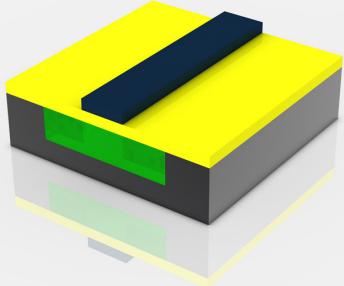
- We will focus on a small part from now on

Fun



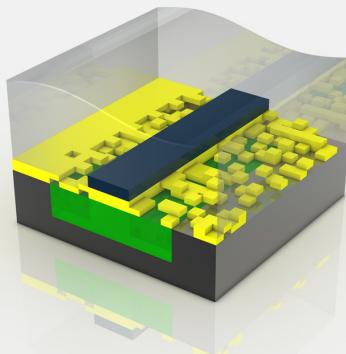
Fabrication

Etching



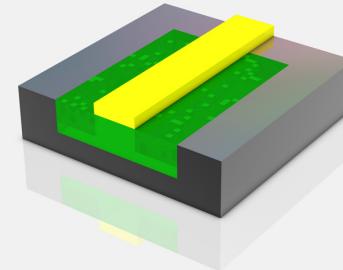
Washing off of Photo Resist

- Remove the Photo Resist layer completely



Etching

- With chemicals etching away the unprotected areas



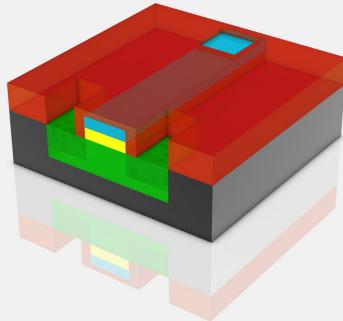
Removing Photo Resist

- After removing the remaining photo resist the intend shape is visible



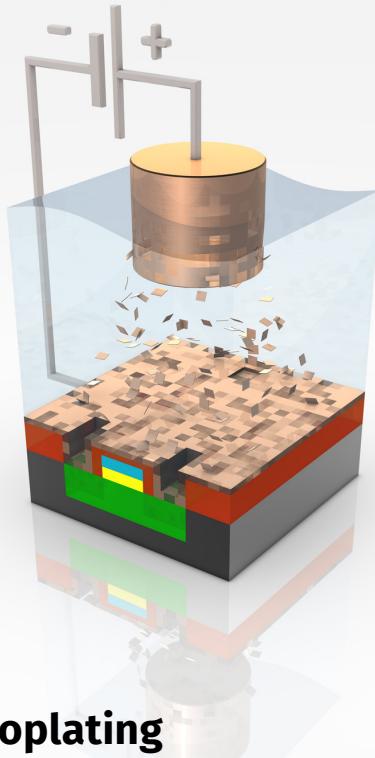
Fabrication

Metal Deposition



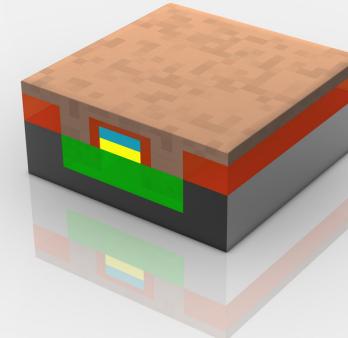
Ready Transistor

- Holes have been etched to be filled with copper and other materials



Electroplating

- Through an electrochemical process transfer copper ions onto the wafer

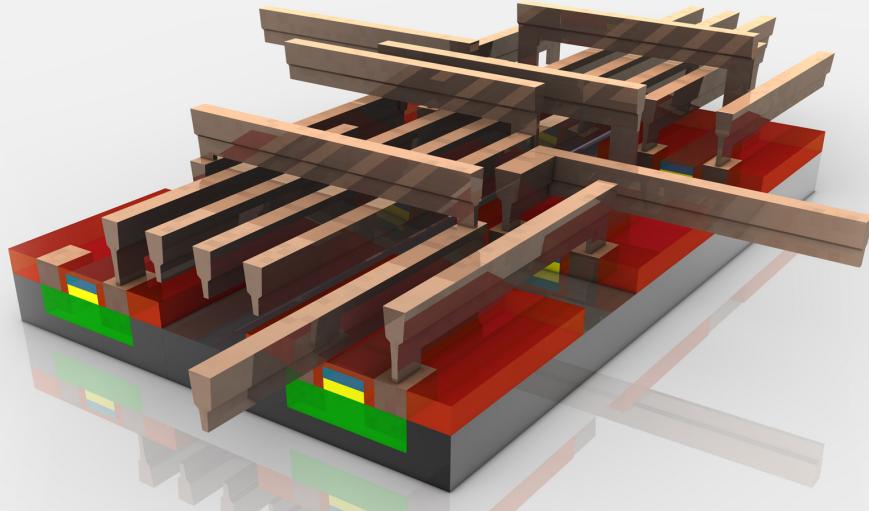
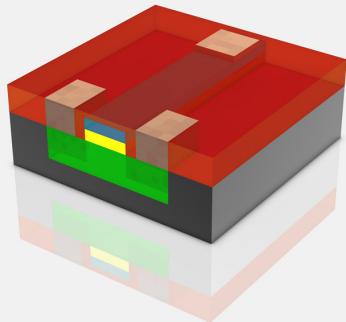


After Electroplating

- Thin layer of copper is placed

Fabrication

Metall Interconnections



Polishing

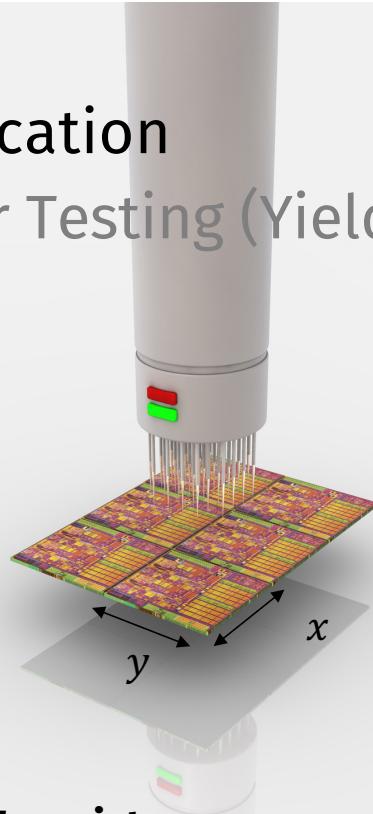
- Excess material is polished off

Metal Layers

- Multiple metal layers create the interconnections
- It is a multi-layered highway system

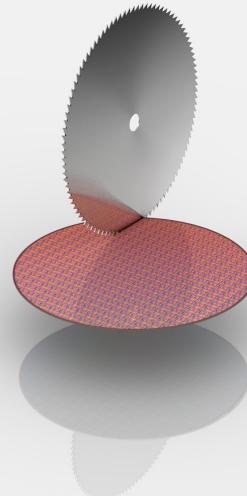
Fabrication

Wafer Testing (Yield)



Ready Transistor

- Holes have been etched to be filled with copper and other materials



Electroplating

- Through an electrochemical process transfer copper ions onto the wafer



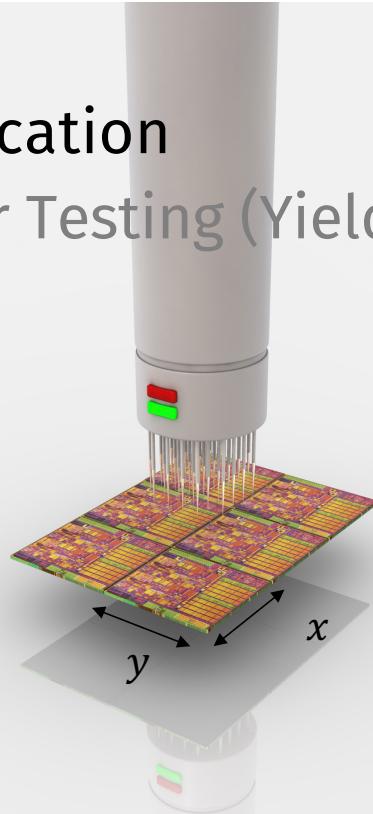
After Electroplating

- Thin layer of copper is placed

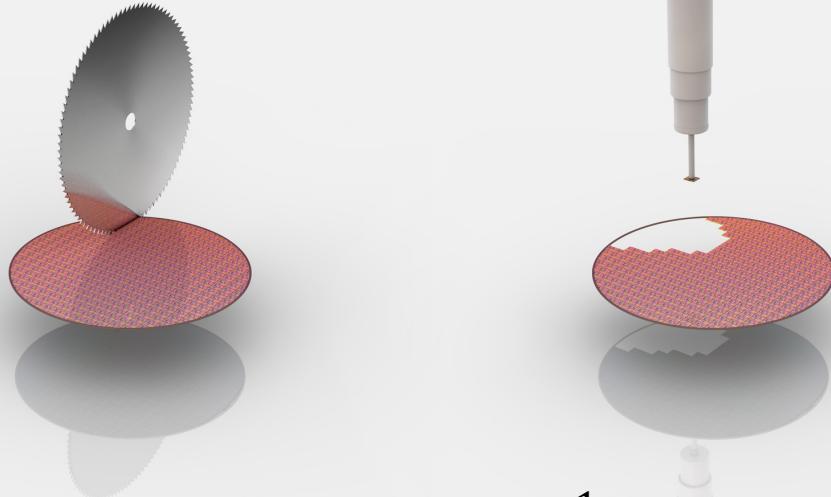


Fabrication

Wafer Testing (Yield)



$$Area_{Die} = x * y$$

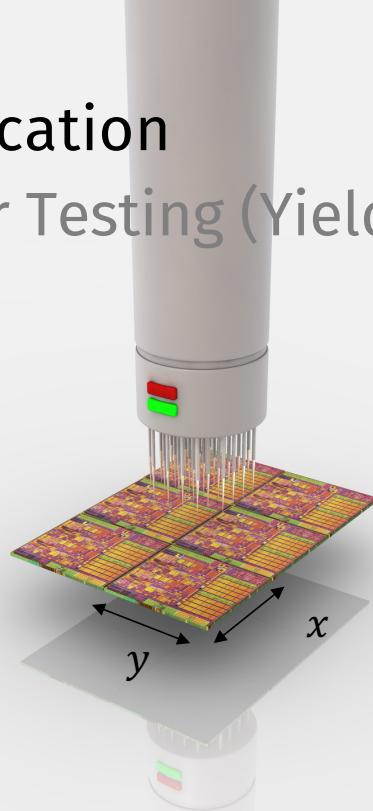


$$Yield = \frac{1}{(1 + \frac{Area_{Die} * Defect_per_Area}{2})^2}$$

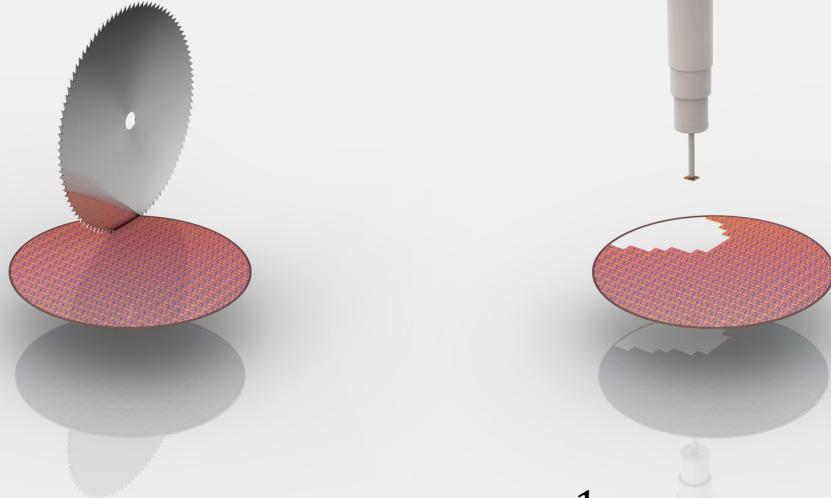
$$\#Dies = \frac{Area_{wafer}}{Area_{Die}}$$

Fabrication

Wafer Testing (Yield)



$$Area_{Die} = x * y$$



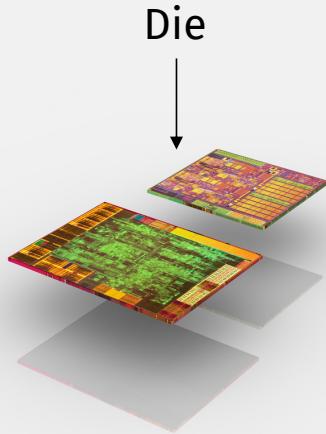
$$Yield = \frac{1}{(1 + \frac{Area_{Die} * Defect_per_Area}{2})^2}$$

$$\#Dies = \frac{Area_{wafer}}{Area_{Die}} - \frac{\pi * Diameter_{wafer}}{\sqrt{2 * Area_{Die}}}$$



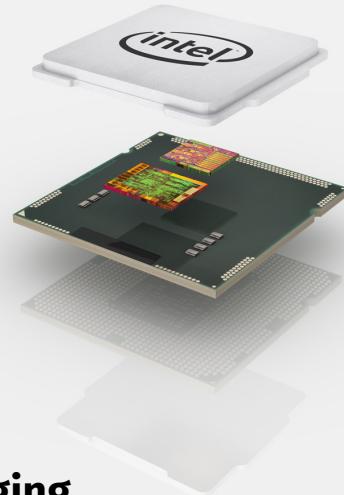
Fabrication

Packaging



Individual Die

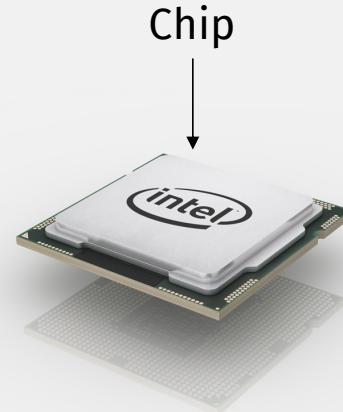
10 Packaging



Packaging

- Substrate and heatspreader is connected
- Microwires connect the transistors to the packagepins

Fun



Processor

- Finished product



Fabrication

Testing and Sorting



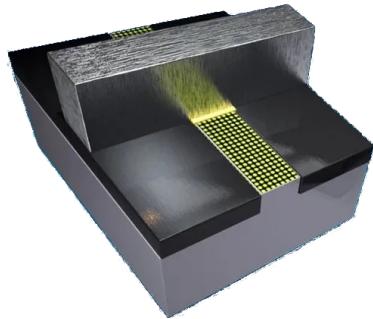
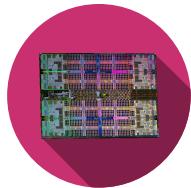
11 Testing And Sorting

Fun

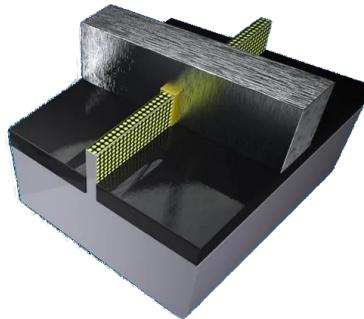


Fabrication

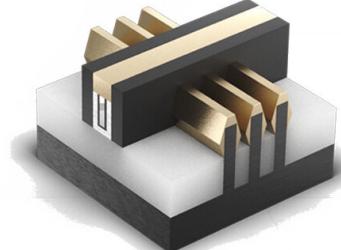
Transistor Evolution



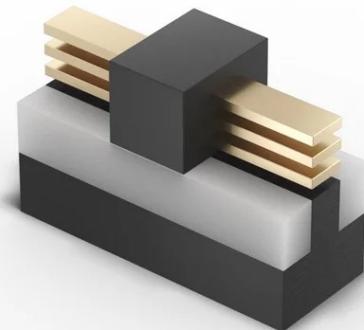
PlanarFET
32nm



TriGateFET
22nm



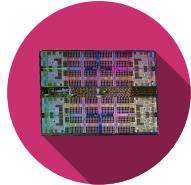
FinFET
22nm-10nm



RibbonFET
4nm

Fabrication

Factory Tours

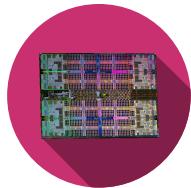


Know how the cause gets made

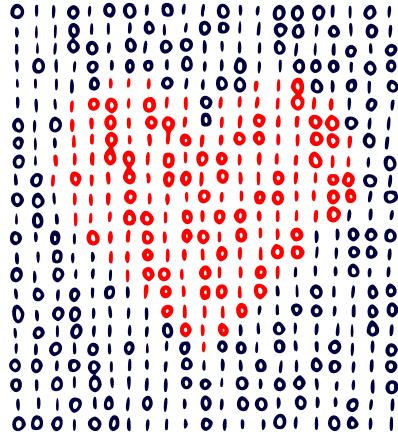
- Intel - <https://www.youtube.com/watch?v=2ehSCWoaoqQ>
- Micron - <https://www.youtube.com/watch?v=-EhDLXx3okU>
- Cherry MX - <https://www.youtube.com/watch?v=Pu1gP4PfqCQ>
- Omron - <https://www.youtube.com/watch?v=9fNijKh6q-E>
- One Plus 6 QC - <https://www.youtube.com/watch?v=ES-s9KQrUTY>

Source : Linus Tech Tips <https://www.youtube.com/@LinusTechTip>

References



- [1] "Bender 0101100101 - YouTube." https://www.youtube.com/watch?v=_4TPlwwHM8Q (accessed Jul. 18, 2022).
- [2] D. Wentzlaff, "Computer Architecture ELE 475 / COS 475." Princeton University, 2019.
- [3] J. L. Hennessy and D. A. Patterson, *Computer Architecture: A Quantitative Approach*, 6th Edition. Elsevier, 2019.
- [4] G. E. Moore, "Cramming more components onto integrated circuits, Reprinted from Electronics, volume 38, number 8, April 19, 1965, pp.114 ff.," *IEEE Solid-State Circuits Society Newsletter*, vol. 11, no. 3, pp. 33–35, Sep. 2006, doi: [10.1109/N-SSC.2006.4785860](https://doi.org/10.1109/N-SSC.2006.4785860).
- [5] R. H. Dennard, F. H. Gaenslen, H.-N. Yu, V. L. Rideout, E. Bassous, and A. R. Leblanc, "Design Of Ion-implanted MOSFET's with Very Small Physical Dimensions," *Proceedings of the IEEE*, vol. 87, no. 4, pp. 668–678, Apr. 1999, doi: [10.1109/JPROC.1999.752522](https://doi.org/10.1109/JPROC.1999.752522).
- [6] Intel, "From Sand to Silicon," 2011.
- [7] STMicroelectronics, "Introduction to semiconductor technology," p. 15, 2000.
- [8] M. Horowitz, E. Alon, D. Patil, S. Naffziger, R. Kumar, and K. Bernstein, "Scaling, power, and the future of CMOS," in *IEEE International Electron Devices Meeting, 2005. IEDM Technical Digest*, Dec. 2005, p. 7 pp. – 15. doi: [10.1109/IEDM.2005.1609253](https://doi.org/10.1109/IEDM.2005.1609253).



Hes·so // VALAIS
WALLIS



Haute Ecole d'Ingénierie
Hochschule für Ingenieurwissenschaften

Silvan Zahno silvan.zahno@hevs.ch

