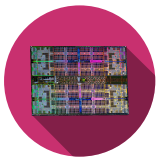


Fundamentals

Student Solutions
Exercises Computer Architecture

1 | Chip & Die Fabrication

1.1 Fabrication

a) 71.8%
b) 235.5 dies
c) 169.1 good_dies
d) 1.18 CHF

fun/fabrication-01

1.2 Fabrication

a) $120 \frac{\text{wafers}}{\text{ingot}}$
b) 250CHF
c) 0.796CHF
d) 209.3 dies
e) 158.23 dies
f) 2.05CHF

fun/fabrication-02

1.3 Fabrication

a) 200CHF
b) $\approx 600 \frac{\text{dies}}{\text{wafer}}$
c) $1.06 \frac{\text{CHF}}{\text{die}}$

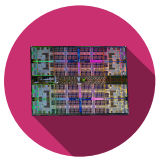
fun/fabrication-03

2 | Moore's Law & Denard scaling

2.1 Dennard Scaling

a) $1.414 = \sqrt{2}$
b) 406pm equals to 16601 times smaller

fun/dennardscaling-01



2.2 Dynamic power consumption of a CMOS circuit is:

Two statements are true, one is false.

fun/dennardscaling-02

3 Power Consumption

3.1 Cell phone battery life

a) $112.6h$
b) $9.19h$

fun/powerconsumption-01