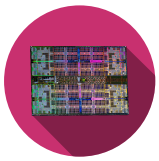


Architecture

Student Solutions
Exercises Computer Architecture

1 Architecture

1.1 Stack-Architecture

a) -
b) 7 explicit fetch and none implicit
c) 7 explicit fetch, 4 implicit fetch, 4 implicit store

arc/stack-01

1.2 Stack-Architecture

a) -
b) 7 explicit fetch
c) 7 explicit fetch (with compiler optimizations)
   7 explicit fetch, 1 implicit store, 1 implicit fetch (without compiler optimizations)
d) 7 explicit fetch, 3 implicit store, 3 implicit fetch (without compiler optimizations)

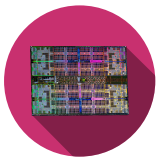
arc/stack-02

2 Single-Cycle RISC-V

2.1 Single-Cycle Processor Operation

```
PCScr = '0'
RegWrite = '1'
ImmScr[1:0] = "xx"
ALUSrc = '0'
ALUControl[2:0] = "010"
MemWrite = '0'
ResultScr = '0'
```

arc/scr-01



2.2 Extend Single Cycle with instruction `jal`

```
PCScr = '0'
RegWrite = '1'
ImmScr[1:0] = "xx"
ALUSrc = '0'
ALUControl[2:0] = "010"
MemWrite = '0'
ResultScr = '0'
```

arc/scr-02

2.3 Single Cycle Processor Performance

$$T_{\text{program\_single\_cycle}} = 75\text{sec} \tag{1}$$

arc/scr-03

3 Multi-Cycle RISC-V

3.1 Multi Cycle Processor Performance

$$\begin{aligned} \text{CPI}_{\text{load}} &= 5 \text{ cycles} \\ \text{CPI}_{\text{store}} &= 4 \text{ cycles} \\ \text{CPI}_{\text{branch}} &= 3 \text{ cycles} \\ \text{CPI}_{\text{jump}} &= 4 \text{ cycles} \\ \text{CPI}_{\text{alu}} &= 4 \text{ cycles} \\ \text{CPI}_{\text{average}} &= 4.14 \text{ cycles} \end{aligned} \tag{2}$$

arc/mcr-01

3.2 Multi-Cycle Processor Performance

$$T_{\text{program\_single\_cycle}} = 155.25\text{sec} \tag{3}$$

arc/mcr-02