



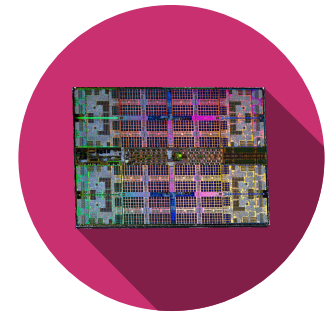
Computer Architecture

Micro-Architecture

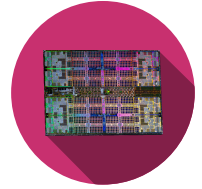
Arc

Information and Communication Systems program

Silvan Zahno silvan.zahno@hevs.ch

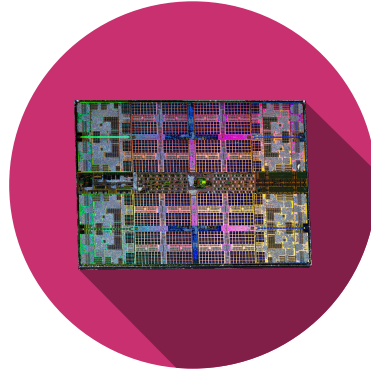


Recapitulation: CPU Performance Equation



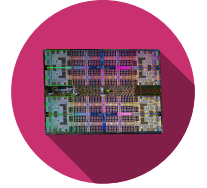
$$T = IC * CPI * CT = \frac{IC * CPI}{f}$$

- $T = \textit{Execution time}$
- $IC = N_{instr} = \# \text{ instructions executed (Instruction Count)}$
- $CPI = \textbf{C}ycles \textbf{P}er \textbf{I}nstruction$
- $CT = t_{cycle} = \textbf{C}ycle \textbf{T}ime = \text{duration of clock cycle}$
- $f = \text{clock frequency} = \frac{1}{t_{cycle}}$



Architectures vs. Microarchitectures

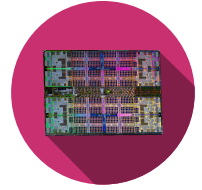
Architecture vs. Microarchitecture



- “Architecture”/Instruction Set Architecture:
 - Programmer visible state (Memory & Register) • Operations (Instructions and how they work)
 - Execution Semantics (interrupts)
 - Input/Output
 - Data Types/Sizes
- Microarchitecture/Organization:
 - Tradeoffs on how to implement ISA for some metric (Speed, Energy, Cost)
 - Examples: Pipeline depth, number of pipelines, cache size, silicon area, peak power, execution ordering, bus widths, ALU widths

Architecture vs. Microarchitecture

Same Architecture / Different Microarchitecture



AMD Phenom X4

- x86 Instruction Set
- Quad Core
- 125W
- Decode 3 Instructions/Cycle/Core
- 64KB L1 I Cache, 64KB L1 D Cache
- 512KB L2 Cache
- Out-of-order
- 2.6GHz

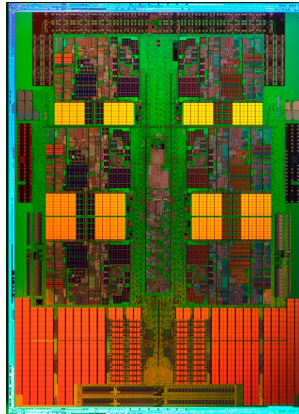


Image Credit: AMD CAR Arc

Intel Atom

- x86 Instruction Set
- Single Core
- 2W
- Decode 2 Instructions/Cycle/Core
- 32KB L1 I Cache, 24KB L1 D Cache
- 512KB L2 Cache
- In-order
- 1.6GHz

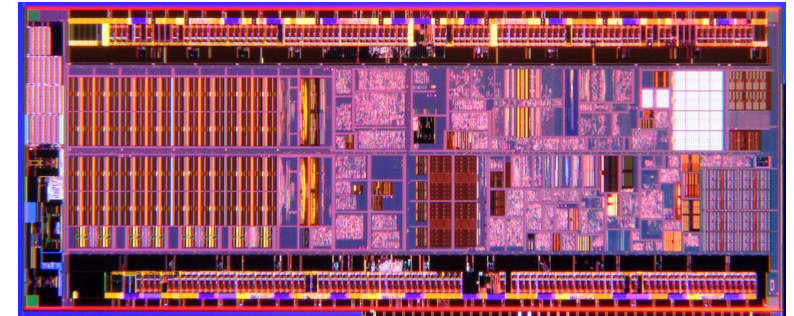
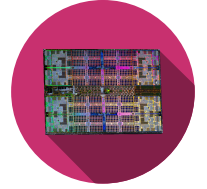


Image Credit: Intel 271

Architecture vs. Microarchitecture

Different Architecture / Different Microarchitecture



AMD Phenom X4

- X86 Instruction Set
- Quad Core
- 125W
- Decode 3 Instructions/Cycle/Core
- 64KB L1 I Cache, 64KB L1 D Cache
- 512KB L2 Cache
- Out-of-order
- 2.6GHz



Image Credit: AMD CAR Arc

IBM POWER7

- Power Instruction Set
- Eight Core
- 200W
- Decode 6 Instructions/Cycle/Core
- 32KB L1 I Cache, 32KB L1 D Cache
- 256KB L2 Cache
- Out-of-order
- 4.25GHz

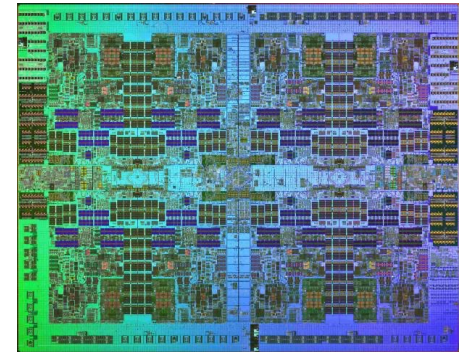
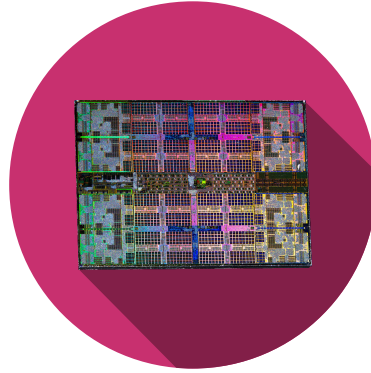


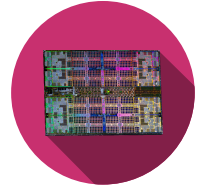
Image Credit: IBM 272



Machine Models

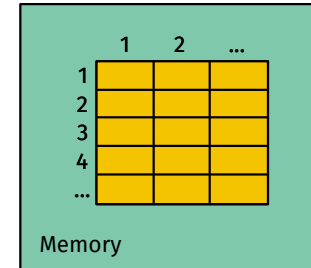
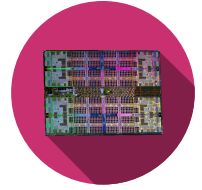
Machine Models

Elements



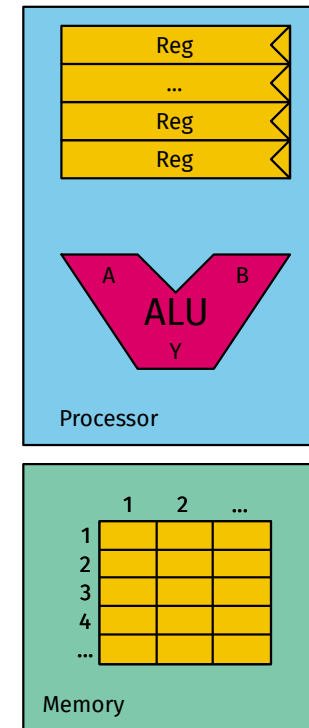
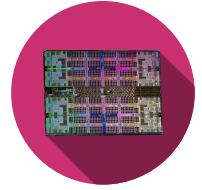
Machine Models

Elements



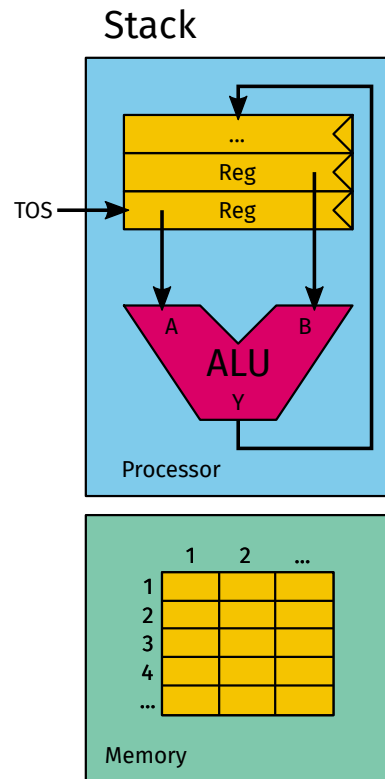
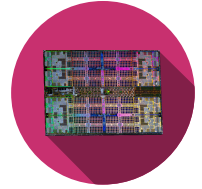
Machine Models

Elements



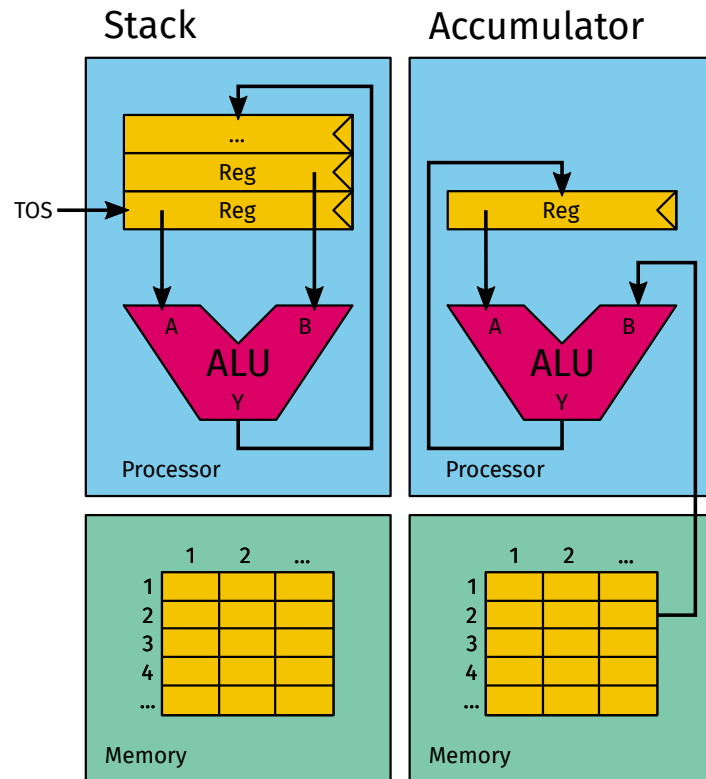
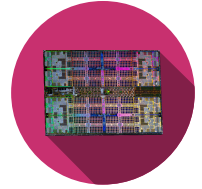
Machine Models

Elements



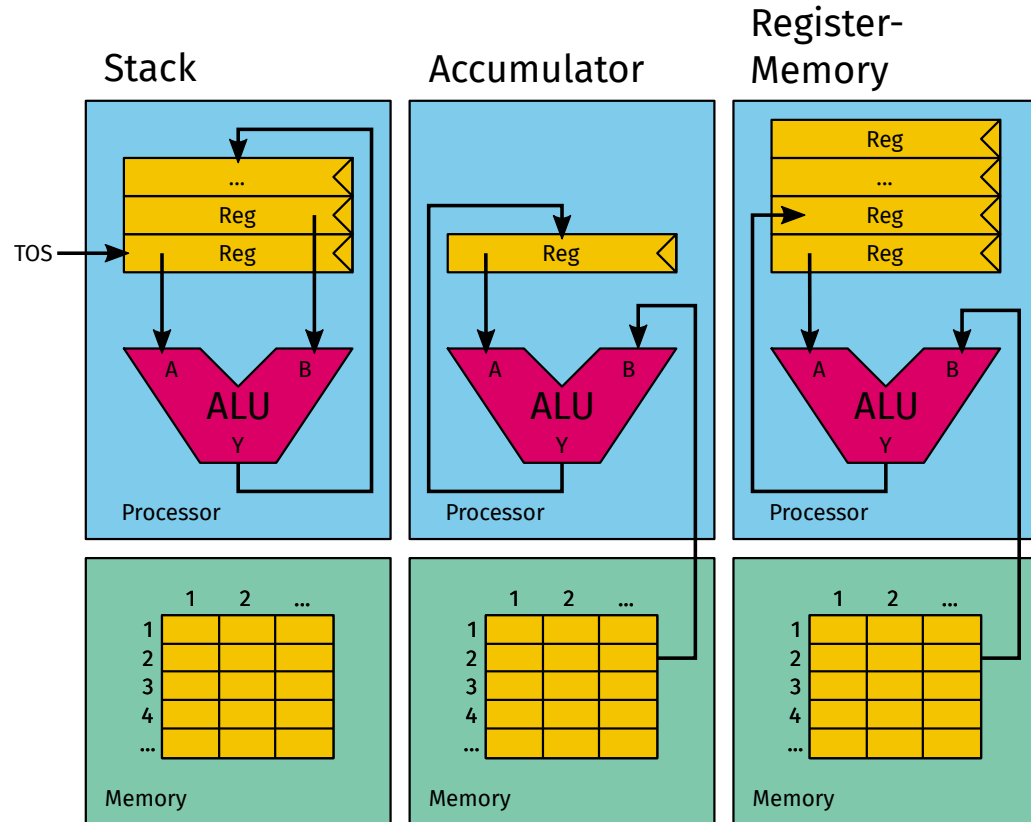
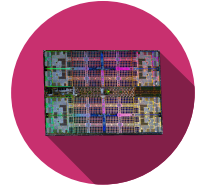
Machine Models

Elements



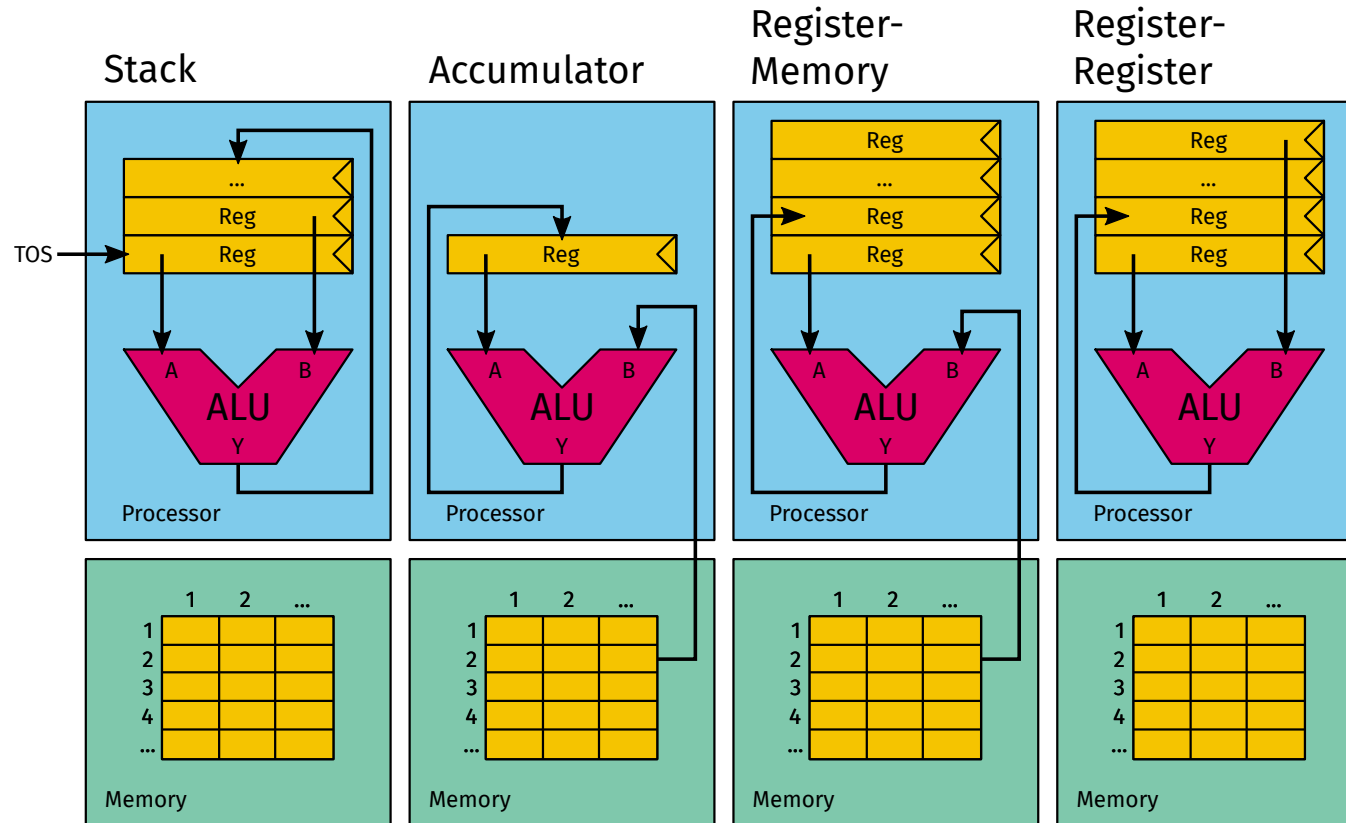
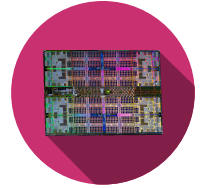
Machine Models

Elements



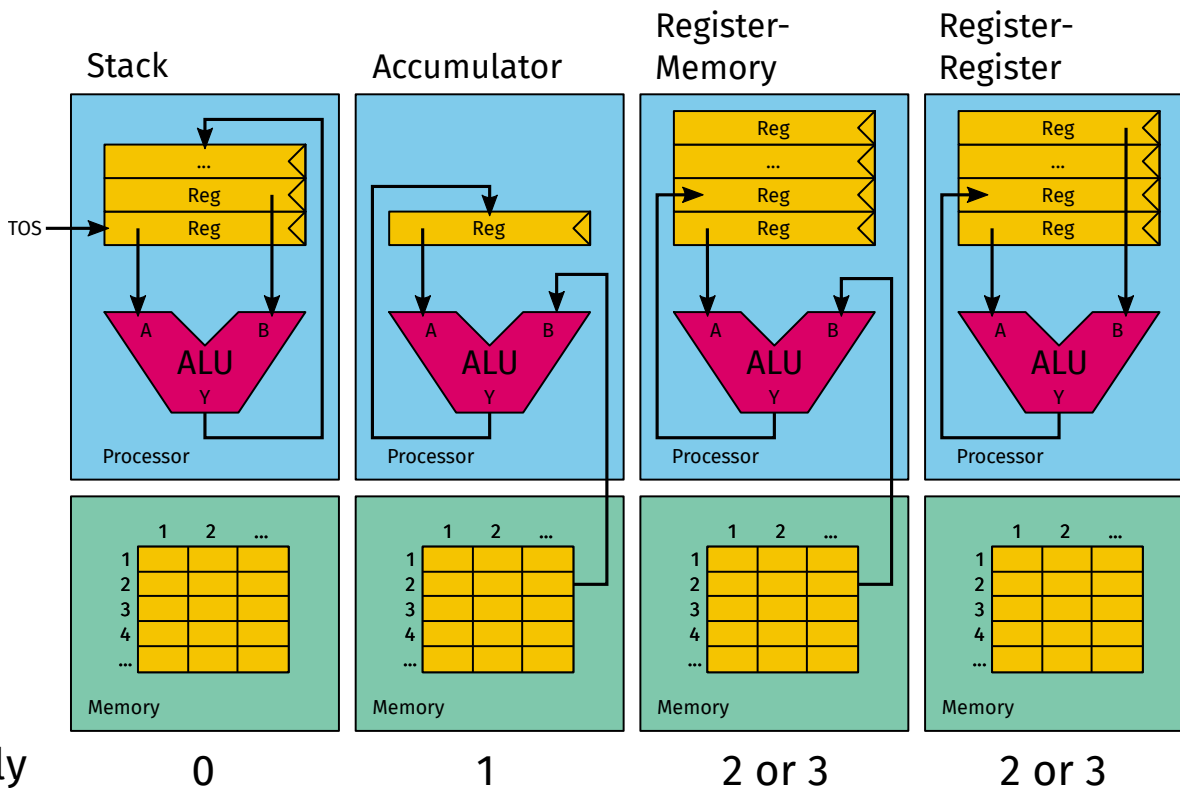
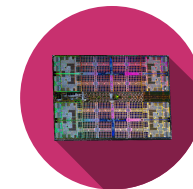
Machine Models

Elements



Machine Models

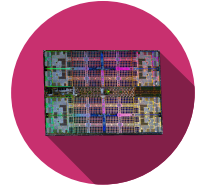
Elements



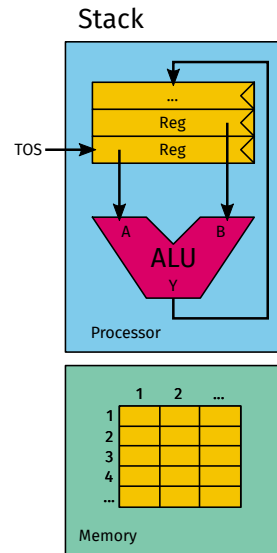
Number Explicitly
Named Operands:

Machine Models

Example Stack machine model

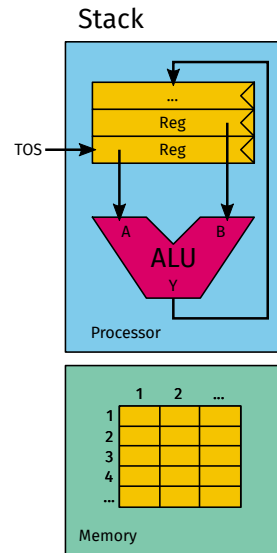
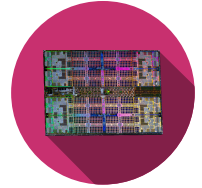


$$(a+b*c)/(a+d*c-e)$$



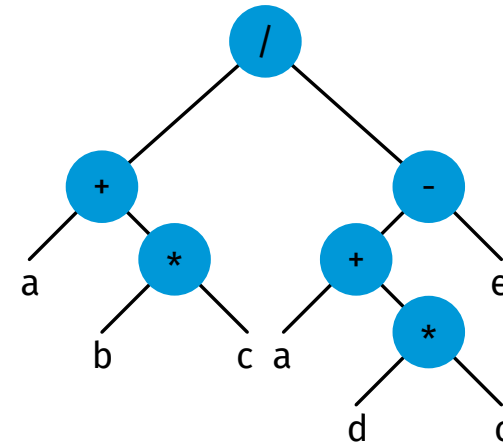
Machine Models

Example Stack machine model



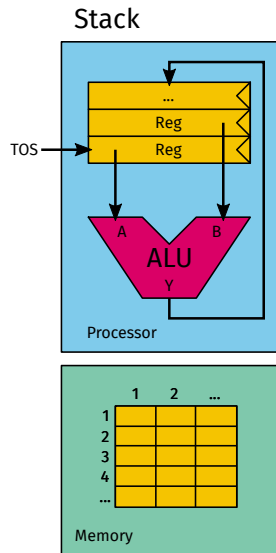
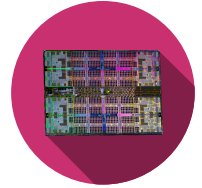
$(a+b*c)/(a+d*c-e)$

Parsetree



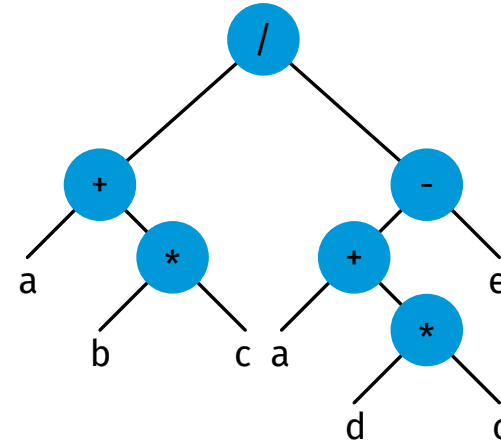
Machine Models

Example Stack machine model



$(a+b*c)/(a+d*c-e)$

Parsetree



Reverse stack

abc*+adc*+e- /

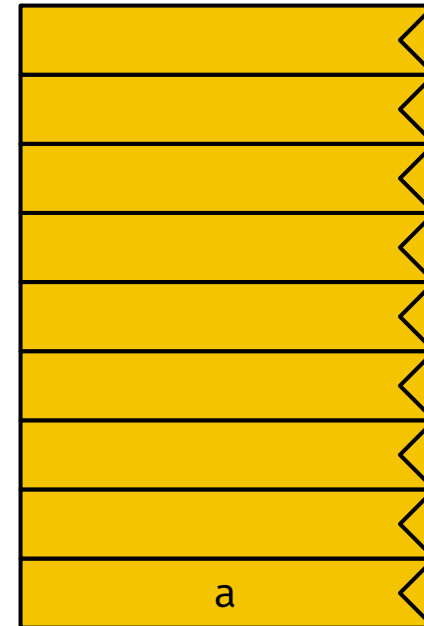
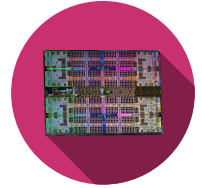
Machine Models

Example Stack machine model

Reverse stack

abc**adc**e- /

Program	stack	memory refs
push a	r0	a
push b	r0 r1	b
push c	r0 r1 r2	c
*	r0 r1	
+	r0	
push a	r0 r1	a
push d	r0 r1 r2	d
push c	r0 r1 r2 r3	c
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	e
-	r0 r1	
/	r0	



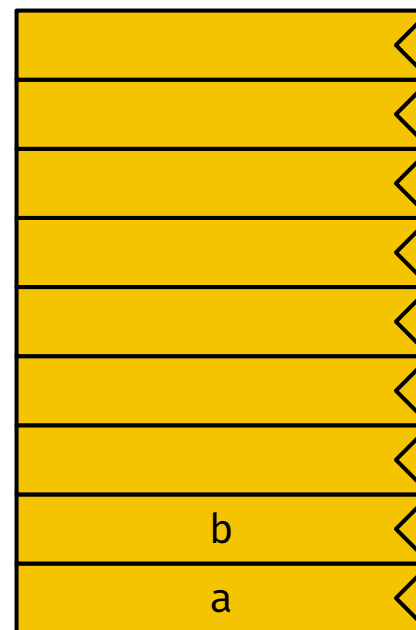
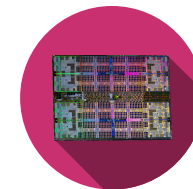
Machine Models

Example Stack machine model

Reverse stack

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+	r0	
push a	r0 r1	a
push d	r0 r1 r2	d
push c	r0 r1 r2 r3	c
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	e
-	r0 r1	
/	r0	



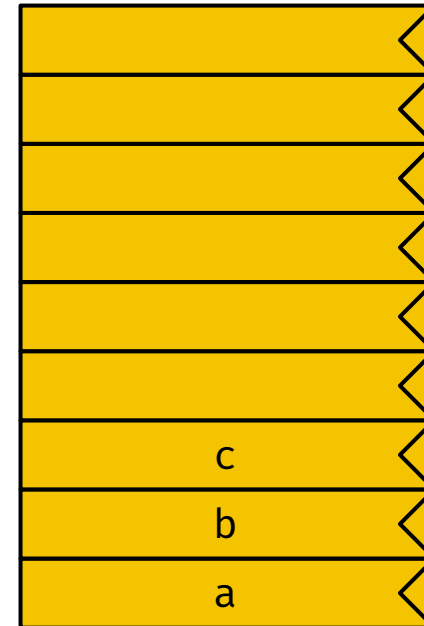
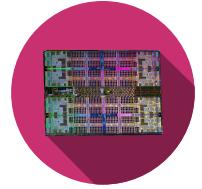
Machine Models

Example Stack machine model

Reverse stack

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+	r0 r1	
push e	r0 r1 r2	e
-	r0 r1	
/	r0	



Machine Models

Example Stack machine model

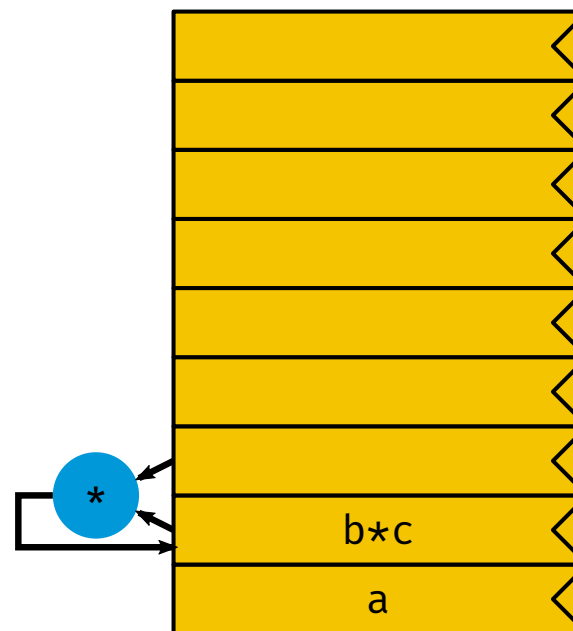
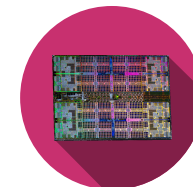
Reverse stack

abc**+adc**+e-/

Program	stack	memory refs
push a	r0	a
push b	r0 r1	b
push c	r0 r1 r2	c
*	r0 r1	
+	r0	
push a	r0 r1	a
push d	r0 r1 r2	d
push c	r0 r1 r2 r3	c
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	e
-	r0 r1	
/	r0	

ZaS

CAR Arc



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Machine Models

Example Stack machine model

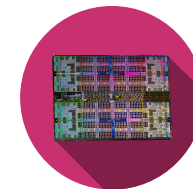
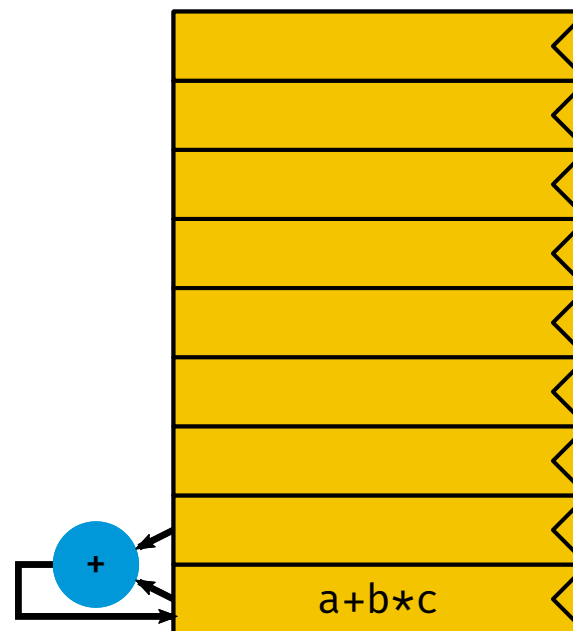
Reverse stack

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push c	r0 r1 r2	c
*	r0 r1	
+	r0	
push a	r0 r1	a
push d	r0 r1 r2	d
push c	r0 r1 r2 r3	c
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	e
-	r0 r1	
/	r0	

ZaS

CAR Arc



Machine Models

Example Stack machine model

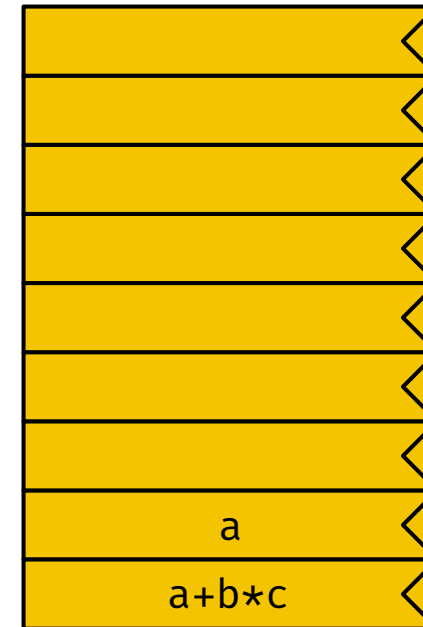
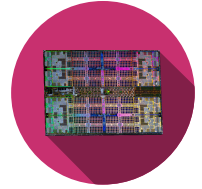
Reverse stack

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push c	r0 r1 r2	c
*	r0 r1	
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push a	r0 r1	a
push d	r0 r1 r2	d
push c	r0 r1 r2 r3	c
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	e
-	r0 r1	
/	r0	

ZaS

CAR Arc



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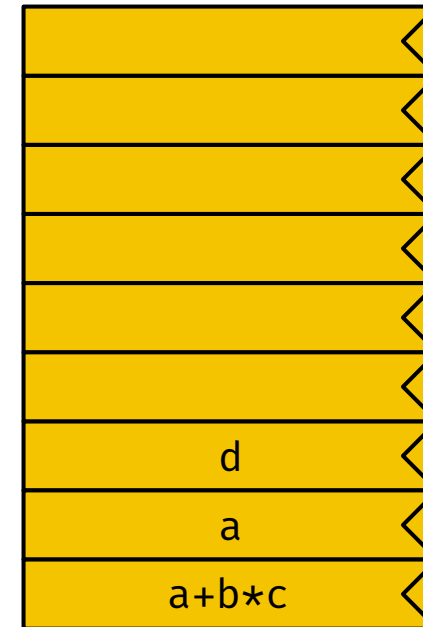
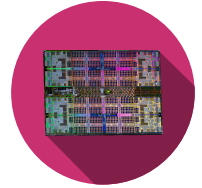
Machine Models

Example Stack machine model

Reverse stack

abc**adc**e- /

Program	stack	memory refs
push a	r0	a
push b	r0 r1	b
push c	r0 r1 r2	c
*	r0 r1	
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push a	r0 r1	a
push d	r0 r1 r2	d
push c	r0 r1 r2 r3	c
*	r0 r1 r2	
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push e	r0 r1 r2	e
-	r0 r1	
/	r0	



Machine Models

Example Stack machine model

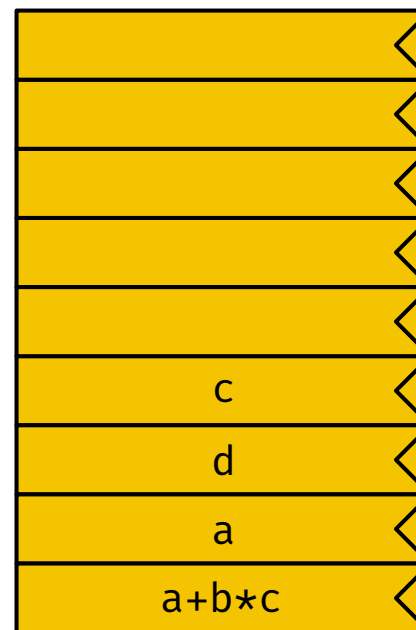
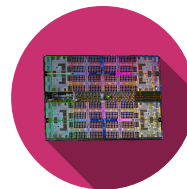
Reverse stack

abc**adc**e- /

Program	stack	memory refs
push a	r0	a
push b	r0 r1	b
push c	r0 r1 r2	c
*	r0 r1	
+	r0	
push a	r0 r1	a
push d	r0 r1 r2	d
push c	r0 r1 r2 r3	c
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	e
-	r0 r1	
/	r0	

ZaS

CAR Arc



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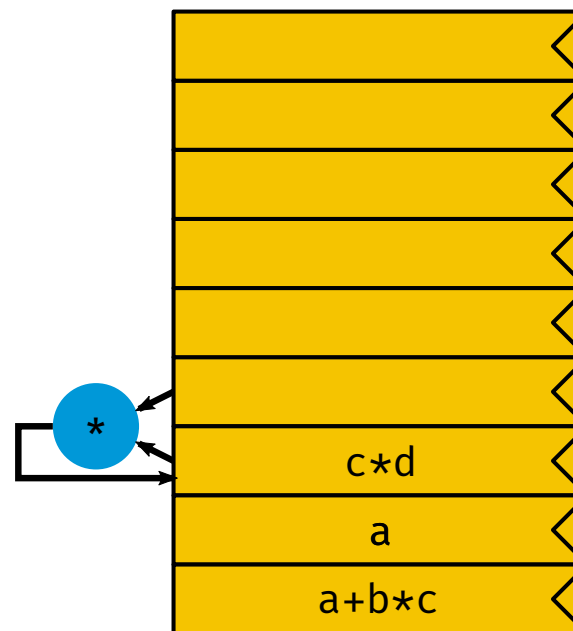
Machine Models

Example Stack machine model

Reverse stack

abc**+adc**+e- /

Program	stack	memory refs
push a	r0	a
push b	r0 r1	b
push c	r0 r1 r2	c
*	r0 r1	
+	r0	
push a	r0 r1	a
push d	r0 r1 r2	d
push c	r0 r1 r2 r3	c
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	e
-	r0 r1	
/	r0	



Machine Models

Example Stack machine model

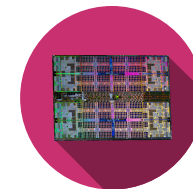
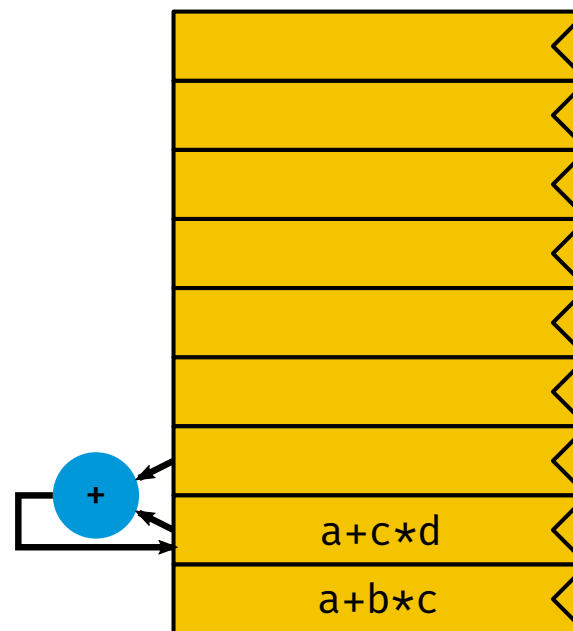
Reverse stack

abc**adc**e- /

Program	stack	memory refs
push a	r0	a
push b	r0 r1	b
push c	r0 r1 r2	c
*	r0 r1	
+	r0	
push a	r0 r1	a
push d	r0 r1 r2	d
push c	r0 r1 r2 r3	c
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	e
-	r0 r1	
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ZaS

CAR Arc



Machine Models

Example Stack machine model

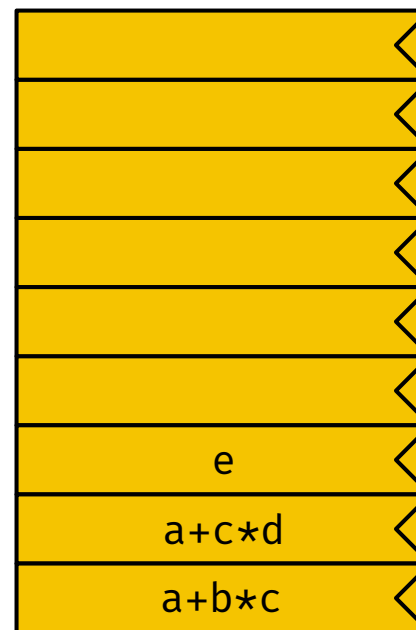
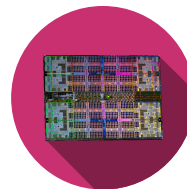
Reverse stack

abc**adc**e- /

Program	stack	memory refs
push a	r0	a
push b	r0 r1	b
push c	r0 r1 r2	c
*	r0 r1	
+	r0	
push a	r0 r1	a
push d	r0 r1 r2	d
push c	r0 r1 r2 r3	c
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	e
-	r0 r1	
/	r0	

ZaS

CAR Arc



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Machine Models

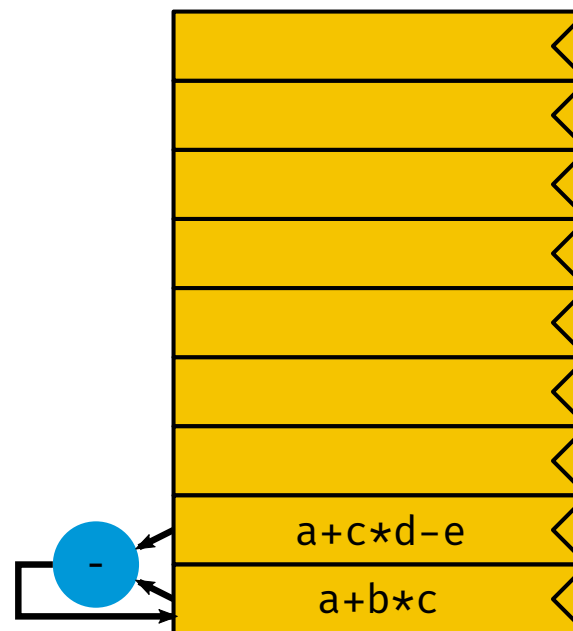
Example Stack machine model

Reverse stack

abc**adc**e- /

Program	stack	memory refs
push a	r0	a
push b	r0 r1	b
push c	r0 r1 r2	c
*	r0 r1	
+	r0	
push a	r0 r1	a
push d	r0 r1 r2	d
push c	r0 r1 r2 r3	c
*	r0 r1 r2	
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push e	r0 r1 r2	e
-	r0 r1	
/	r0	

ZaS



CAR Arc

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Machine Models

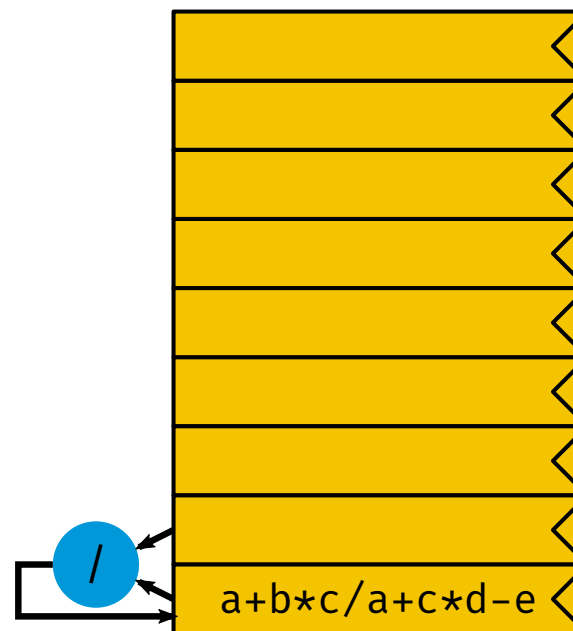
Example Stack machine model

Reverse stack

abc**adc**e-/

Program	stack	memory refs
push a	r0	a
push b	r0 r1	b
push c	r0 r1 r2	c
*	r0 r1	
+	r0	
push a	r0 r1	a
push d	r0 r1 r2	d
push c	r0 r1 r2 r3	c
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	e
-	r0 r1	
/	r0	

ZaS



CAr Arc

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Machine Models

Example Stack machine model

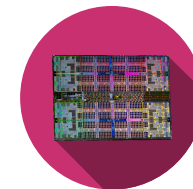
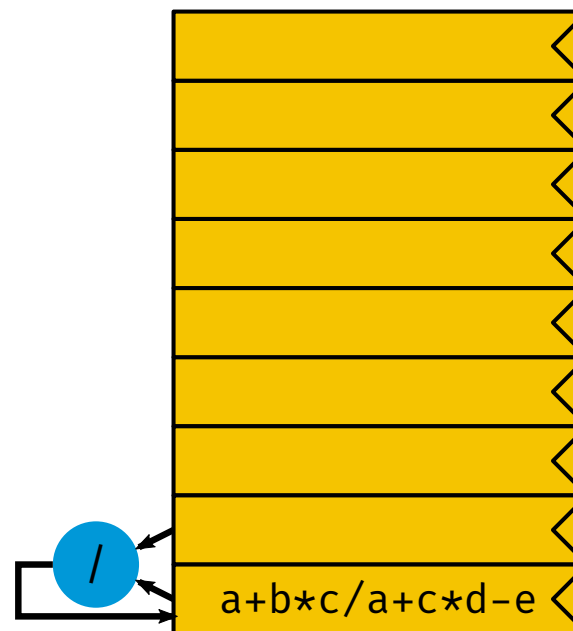
Reverse stack

abc**adc**e- /

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push b	r0 r1	b
push c	r0 r1 r2	c
*	r0 r1	
+	r0	
push a	r0 r1	a
push d	r0 r1 r2	d
push c	r0 r1 r2 r3	c
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	e
-	r0 r1	
/	r0	

ZaS

CAR Arc



Machine Models

Example Stack machine model

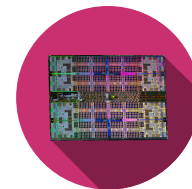
Reverse stack

abc**adc**e-/

Program	stack	memory refs
push a	r0	a
push b	r0 r1	b
push c	r0 r1 r2	c
*	r0 r1	
+	r0	
push a	r0 r1	a
push d	r0 r1 r2	d
push c	r0 r1 r2 r3	c
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	e
-	r0 r1	
/	r0	

Not efficient use of registers

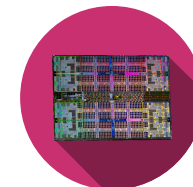
a & c are fetched twice



Machine Models

Exercise Stack machine model

Evaluate the stack in case of a stacksize of 2. How many memory references are there?



Reverse stack

abc**adc**e-/-

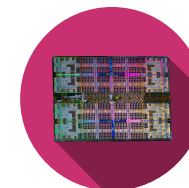
Program	stack (size = 2)	memory refs
push a	r0	
push b	r0 r1	
push c	r0 r1 r2	
*	r0 r1	
+	r0	
push a	r0 r1	
push d	r0 r1 r2	
push c	r0 r1 r2 r3	
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	
-	r0 r1	
/	r0	

Machine Models

Exercise Stack machine model

Evaluate the stack in case of a stacksize of 2. How many memory references are there?

- 7 explicit fetch
- 4 implicit fetch
- 4 implicit store



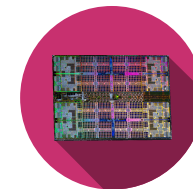
Reverse stack

abc**adc**e-/-

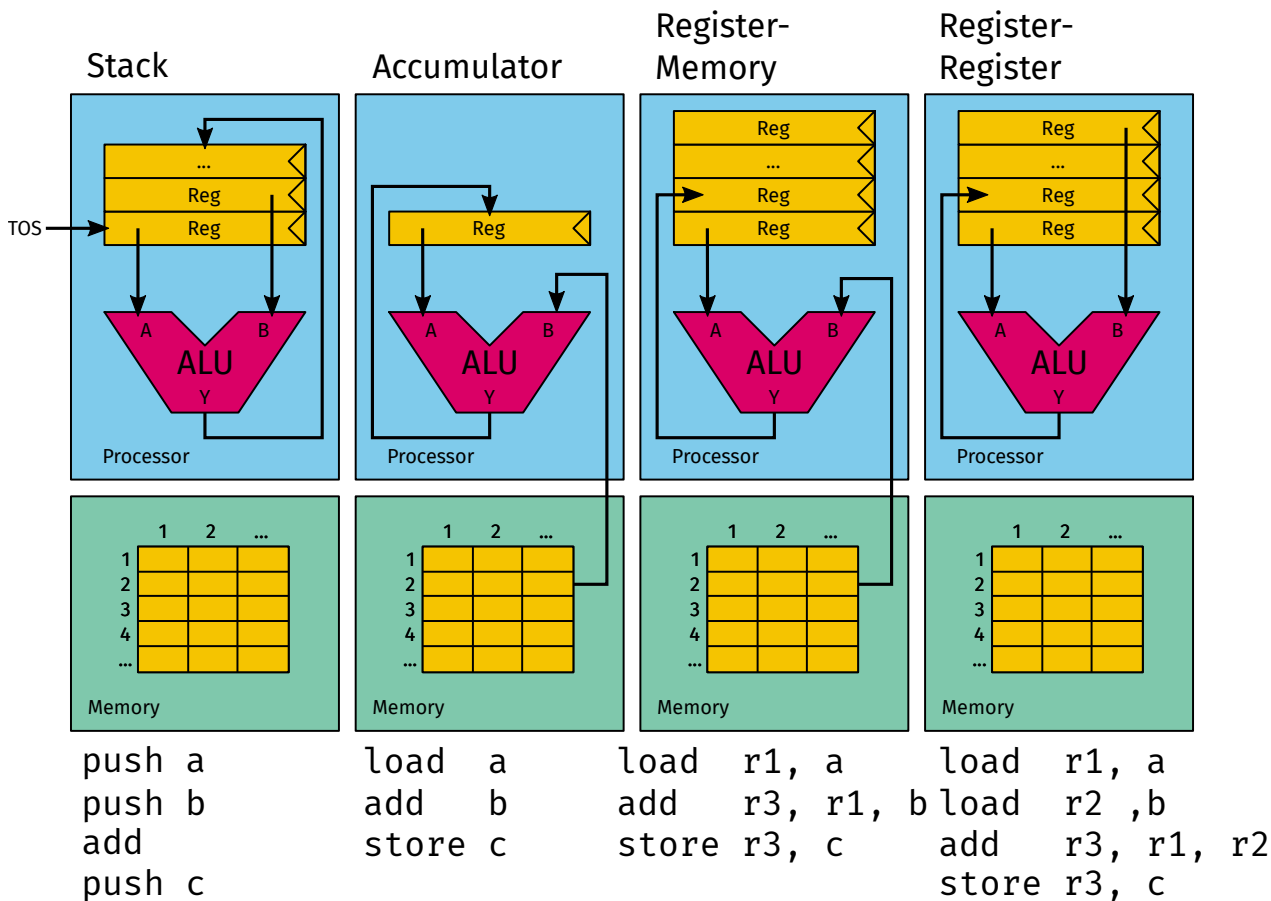
Program	stack (size = 2)	memory refs
push a	r0	a
push b	r0 r1	b
push c	r0 r1 r2	c, ss(a)
*	r0 r1	sf(a)
+	r0	
push a	r0 r1	a
push d	r0 r1 r2	d, ss(a+b*c)
push c	r0 r1 r2 r3	c, ss(a)
*	r0 r1 r2	sf(a)
+	r0 r1	sf(a+b*c)
push e	r0 r1 r2	e, ss(a+b*c)
-	r0 r1	sf(a+b*c)
/	r0	

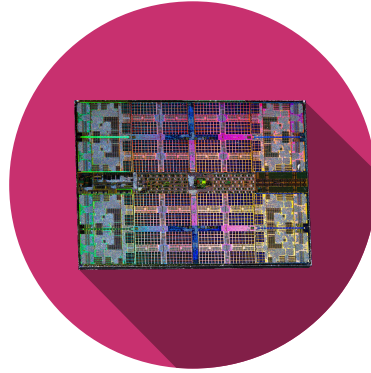
Machine Models

Summary



$c = a + b$





Data Architectures

Data Architectures

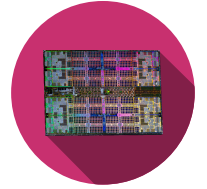
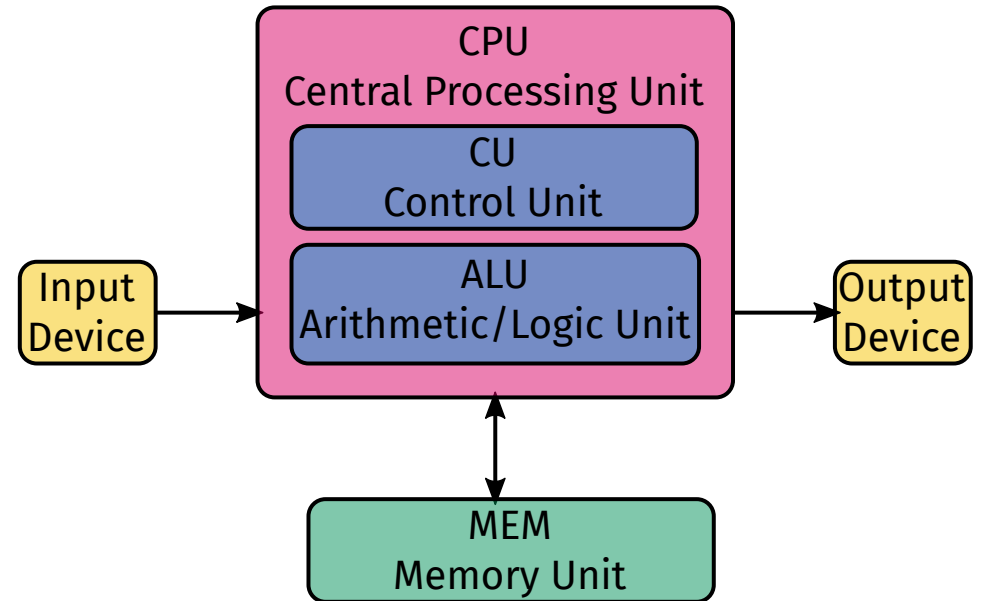
Von Neumann

- Same memory holds data and instructions
- A single set of address/data busses between CPU and memory

Advantages – Cheaper, less logic, less power consumption

Disadvantages – databus speed slower than harvard, bottleneck problems

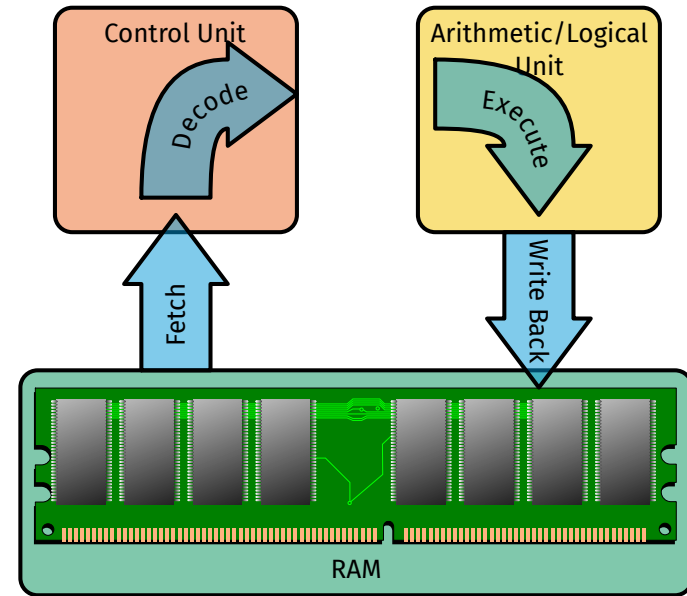
Examples – All Intel x86, ARM7



Data Architectures

Von Neumann 4-step instruction cycle

1. **Fetch** – the instruction from memory into the IR
 1. Load the MAR with the PC
 2. Place instruction into the MDR
 3. Load IR with the MDR
2. **Decode** – Examined the IR and decides what to perform
3. **Execute** – Executes the operation
4. **Write Back** – Write the result back into memory



IR – Instruction Register
MAR – Memory address register
MDR – Memory data register

Data Architectures

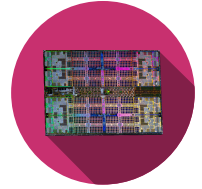
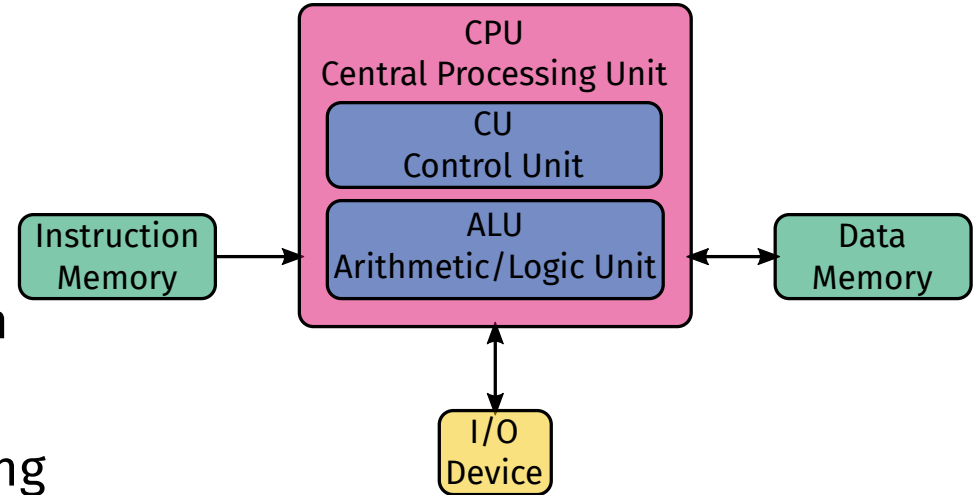
Harvard

- Separate memories for data and instructions
- Two sets of address/data busses between CPU and memory

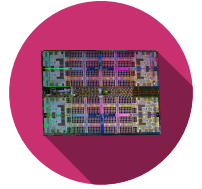
Advantages – greater memory bandwidth, different bit depth between instruction and data

Disadvantages – can't use self-modifying code

Examples – DSP, ARM9



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- [2]
D. Wentzlaff, “Computer Architecture ELE 475 / COS 475.” Princeton University, 2019.
- [3]
J. L. Hennessy and D. A. Patterson, *Computer Architecture: A Quantitative Approach*, 6th Edition. Elsevier, 2019.
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“Difference Between Von Neumann and Harvard Architecture,” *Circuit Globe*, Jun. 10, 2021. <https://circuitglobe.com/difference-between-von-neumann-and-harvard-architecture.html> (accessed Nov. 03, 2022).
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- [7]
“What’s the difference between Von-Neumann and Harvard architectures?” <https://www.microcontrollertips.com/difference-between-von-neumann-and-harvard-architectures/> (accessed Nov. 03, 2022).

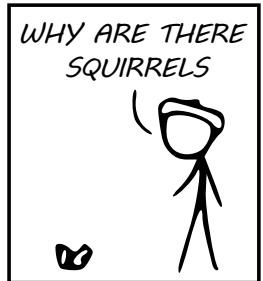
WHY ARE THERE MIRRORS ABOVE BEDS

WHY DO I SAY UH
WHY IS SEA SALT BETTER

WHY ARE THERE TREES IN THE MIDDLE OF FIELDS
WHY IS THERE NOT A POKEMON MMO
WHY IS THERE LAUGHING IN TV SHOWS
WHY ARE THERE DOORS ON THE FREEWAY
WHY ARE THERE SO MANY SVCHOST:EXE RUNNING
WHY AREN'T ANY COUNTRIES IN ANTARCTICA
WHY ARE THERE SCARY SOUNDS IN MINECRAFT
WHY IS THERE KICKING IN MY STOMACH
WHY ARE THERE TWO SLASHES AFTER HTTP
WHY ARE THERE CELEBRITIES
WHY DO SNAKES EXIST
WHY DO OYSTERS HAVE PEARLS
WHY ARE DUCKS CALLED DUCKS
WHY DO THEY CALL IT THE CLAP
WHY ARE KYLE AND CARTMAN FRIENDS
WHY IS THERE AN ARROW ON AANG'S HEAD
WHY ARE TEXT MESSAGES BLUE
WHY ARE THERE MUSTACHES ON CLOTHES
WHY WUBA LUBBA DUB DUB MEANING
WHY IS THERE A WHALE AND A POT FALLING
WHY ARE THERE SO MANY BIRDS IN SWISS
WHY IS THERE SO LITTLE RAIN IN WALLIS
WHY IS WALLIS WEATHER FORECAST ALWAYS WRONG

WHY ARE THERE MALE AND FEMALE BIKES

WHY ARE THERE BRIDESMAIDS
WHY DO DYING PEOPLE REACH UP
HOW FAST IS LIGHTSPEED
WHY ARE OLD KLINGONS DIFFERENT



WHY ARE THERE TINY SPIDERS IN MY HOUSE
WHY DO SPIDERS COME INSIDE
WHY ARE THERE HUGE SPIDERS IN MY HOUSE
WHY ARE THERE LOTS OF SPIDERS IN MY HOUSE
WHY ARE THERE SPIDERS IN MY ROOM
WHY ARE THERE SO MANY SPIDERS IN MY ROOM
WHY DO SPYDER BITES ITCH
WHY IS DYING SO SCARY

WHY IS THERE NO GPS IN LAPTOPS
WHY DO KNEES CLICK
WHY AREN'T THERE 5 GRADES

WHY IS THERE CAFFEINE IN MY SHAMPOO
WHY HAVE DINOSAURS NO FUR

WHY DO IGUANAS DIE
WHY AREN'T THERE DINOSAUR GHOSTS

WHY AREN'T ECONOMISTS RICH
WHY DO AMERICANS CALL IT SOCCER
WHY ARE MY EARS RINGING
WHY IS 42 THE ANSWER TO EVERYTHING
WHY CAN'T NOBODY ELSE LIFT THORS HAMMER
WHY IS MARVIN ALWAYS SO SAD

WHY ARE THERE ANTS IN MY LAPTOP

WHY IS EARTH TILTED
WHY IS SPACE BLACK
WHY IS OUTER SPACE SO COLD
WHY ARE THERE PYRAMIDS ON THE MOON
WHY IS NASA SHUTTING DOWN

WHY ARE THERE FEMALE N
WHY ARE THERE GHOSTS
WHY ARE THERE GODS
WHY ARE THERE TWO SPOCKS
WHAT IS <https://xkcd.com/1256/>
WHY DO THEY SAY T-MINUS
WHY ARE THERE OBELISKS
WHY ARE WRESTLERS ALWAYS WET
WHY ARE OCEANS BECOMMING MORE ACIDIC

WHY ARE SWISS AFRAID OF DRAGONS

WHY IS THERE A SWARM OF ANTS
WHY IS THERE PILGRIM
WHY ARE THERE SO MANY CROWS IN ROCHESTER
WHY IS TO BE OR NOT TO BE FUNNY
WHY DO CHILDREN GET CANCER
WHY IS POSEIDON ANGRY WITH ODYSSEUS
WHY IS THERE ICE IN SPACE

WHY IS THERE LAVA
WHY ARE THERE DOGS AFRAID OF FIRE
WHY IS THERE NO KING IN EN

WHY ARE THERE GHOSTS



WHY ARE THERE DOGS AFRAID OF FIRE
WHY IS THERE NO KING IN EN

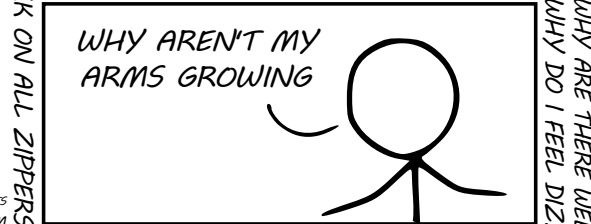
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WHY DO THEY SAY T-MINUS
WHY ARE THERE OBELISKS
WHY ARE WRESTLERS ALWAYS WET
WHY ARE OCEANS BECOMMING MORE ACIDIC

WHY ARE THERE ANTS IN MY LAPTOP

WHY IS THERE AN OWL IN MY BACKYARD
WHY IS THERE AN OWL OUTSIDE MY WINDOW
WHY IS THERE AN OWL ON THE DOLLAR BILL
WHY DO OWLS ATTACK PEOPLE
WHY ARE FPGA'S EVERYWHERE
WHY ARE THERE HELICOPTERS CIRCLING MY HOUSE
WHY ARE THERE GODS
WHY ARE THERE TWO SPOCKS

WHY ARE MY BOOBS ITCHY
WHY ARE CIGARETTES LEGAL
WHY ARE THERE DUCKS IN MY POOL
WHY IS JESUS WHITE
WHY IS THERE LIQUID IN MY EAR
WHY DO Q TIPS FEEL GOOD
WHY DO PEOPLE DIE

WHY IS THERE A LINE THROUGH HTTPS
WHY IS THERE A RED LINE THROUGH HTTPS ON TWITTER
WHY IS HTTPS IMPORTANT



WHY ARE THERE WEEKS
WHY DO I FEEL DIZZY
WHY ARE THERE DOGS AFRAID OF FIRE
WHY IS THERE NO KING IN EN

WHY ARE THERE ANTS IN MY LAPTOP

WHY ARE THERE GODS
WHY ARE THERE TWO SPOCKS
WHAT IS <https://xkcd.com/1256/>
WHY DO THEY SAY T-MINUS
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WHY ARE MY BOOBS ITCHY
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WHY DO PEOPLE DIE

QUESTIONS

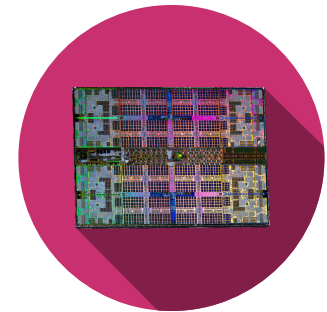
CAN BE ASKED BY ANYONE ANYTIME



Hes·so  **VALAIS
WALLIS**



Haute Ecole d'Ingénierie
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