<div style="border:1px solid; padding:1em">

Architektur

Studentenlösungen
Übungen Computerarchitektur

</div>

1 | Architektur

1.1 Stack-Architektur

a) -

b) 7 explicit fetch and none implicit

c) 7 explicit fetch, 4 implicit fetch, 4 implicit store

arc/stack-01

1.2 Stack-Architektur

a) -

b) 7 explicit fetch

c) 7 explicit fetch (with compiler optimizations)

   7 explicit fetch, 1 implicit store, 1 implicit fetch (without compiler optimizations)

d) 7 explicit fetch, 3 implicit store, 3 implicit fetch (without compiler optimizations)

arc/stack-02

2 | Single-Cycle RISC-V

2.1 Single-Cycle-Prozessorbetrieb

```
PCScr = '0'
RegWrite = '1'
ImmScr[1:0] = "xx"
ALUSrc = '0'
ALUControl[2:0] = "010"
MemWrite = '0'
ResultScr = '0'
```

arc/scr-01

2.2 Einzelzyklus mit Anweisung `jal` verlängern

```
PCScr = '0'
RegWrite = '1'
ImmScr[1:0] = "xx"
ALUSrc = '0'
ALUControl[2:0] = "010"
MemWrite = '0'
ResultScr = '0'
```

2.3 Einzelzyklus-Prozessorleistung

$$T_{\text{program\_single\_cycle}} = 75\text{sec} \tag{1}$$

3 | Multi-Cycle RISC-V

3.1 Mehrzyklus-Prozessorleistung

$$\text{CPI}_{\text{load}} = 5 \text{ cycles}$$
$$\text{CPI}_{\text{store}} = 4 \text{ cycles}$$
$$\text{CPI}_{\text{branch}} = 3 \text{ cycles}$$
$$\text{CPI}_{\text{jump}} = 4 \text{ cycles} \tag{2}$$
$$\text{CPI}_{\text{alu}} = 4 \text{ cycles}$$
$$\text{CPI}_{\text{average}} = 4.14 \text{ cycles}$$

3.2 Multi-Zyklus-Prozessorleistung

$$T_{\text{program\_single\_cycle}} = 155.25\text{sec} \tag{3}$$