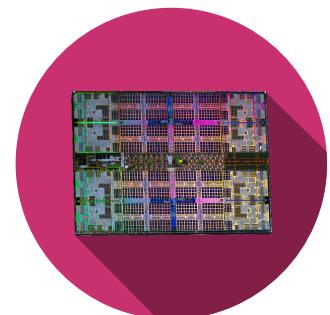


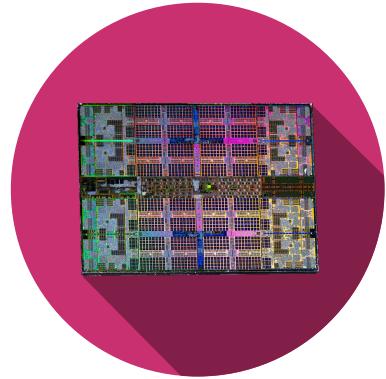


# Computer Architecture Fundamentals Fun

Information and Communication Systems program

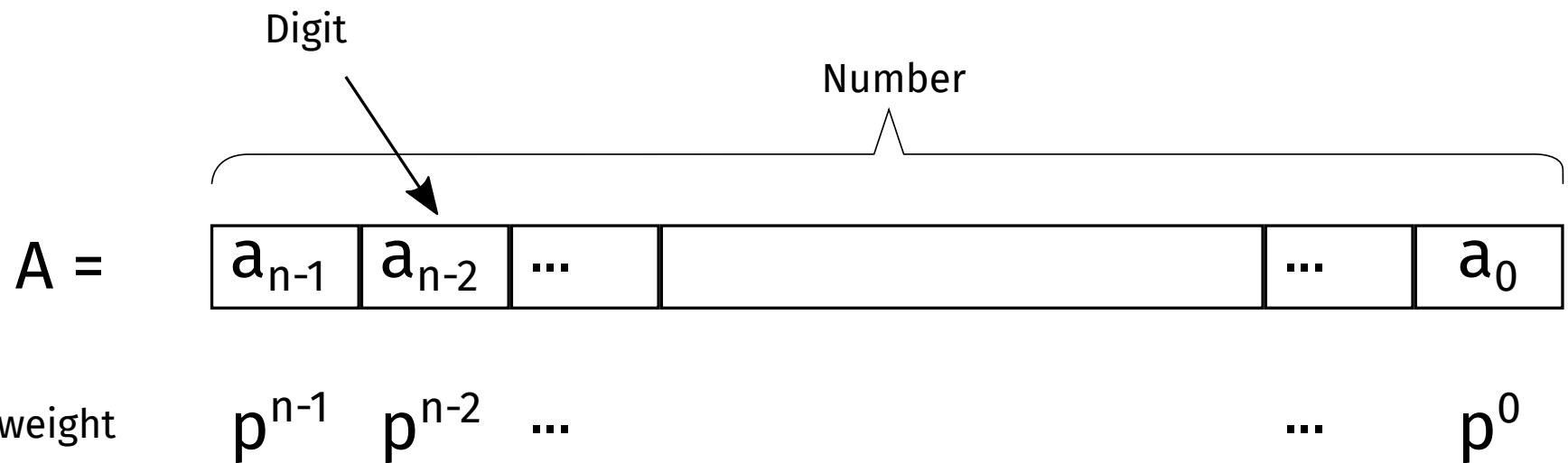
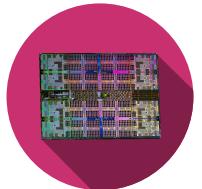
Silvan Zahno [silvan.zahno@hevs.ch](mailto:silvan.zahno@hevs.ch)



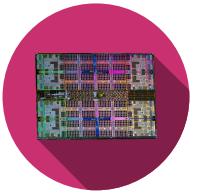


# Binarysystem

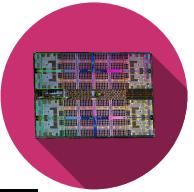
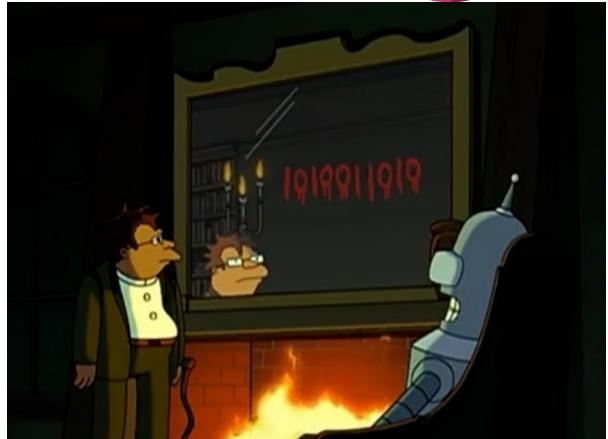
# Binary System



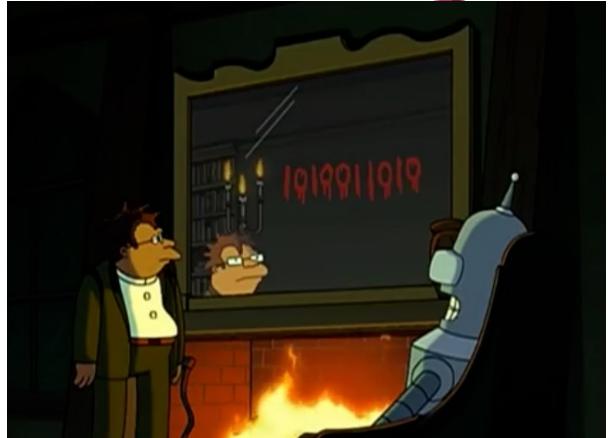
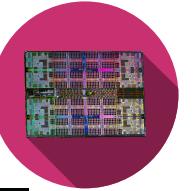
# Bender's scare



# Bender's scare



# Bender's scare



$$0101100101 = 256 + 64 + 32 + 4 + 1 = 357$$

$$1010011010 = 512 + 128 + 16 + 8 + 2 = 666$$

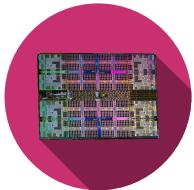
# Binary System

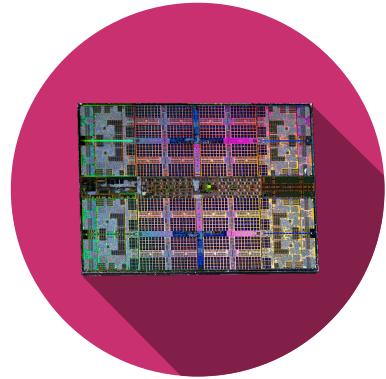
## Naming conventions

- 8 BIT make up one byte (octet)
  - Purely historical
- Using IEC standard:
  - 1 KiB = 1'024 bytes (Note: big K)
  - 1 MiB = 1'024 KiB = 1'048'576 bytes
  - 1 GiB = 1'024 MiB = 1'048'576 KiB = 1'073'741'824 bytes
- Using SI standard:
  - 1 kB = 1'000 bytes (Note: small k)
  - 1 MB = 1'000 kB = 1,000,000 bytes
  - 1 GB = 1'000 MB = 1'000'000 KB = 1'000'000'000 bytes

11110101

8 Bit = 1 Byte

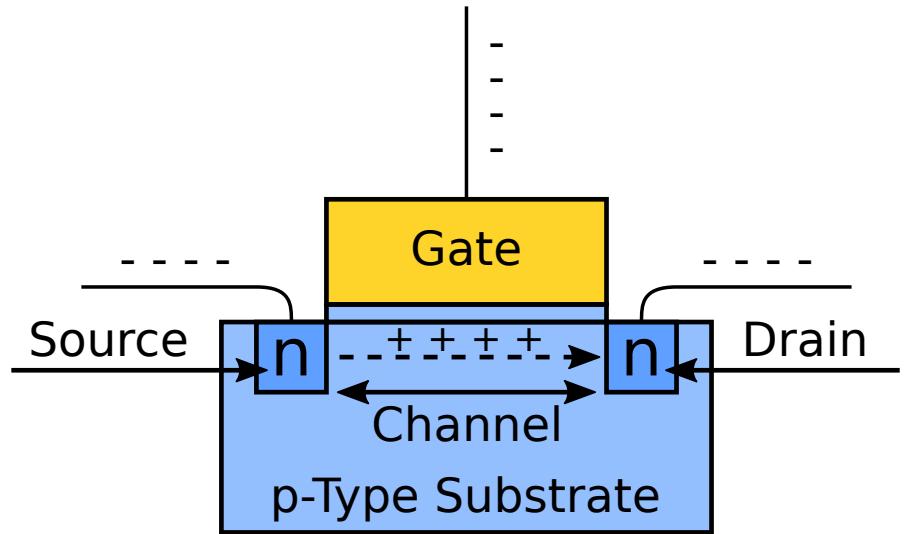
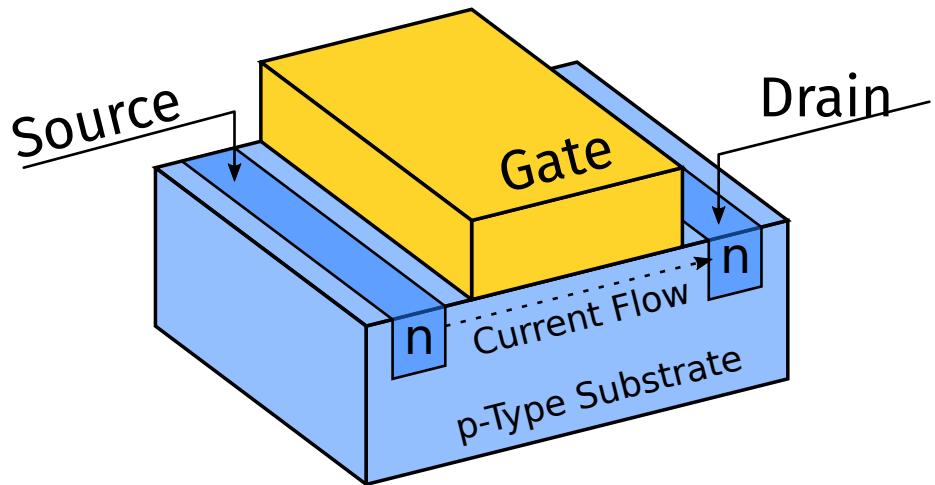
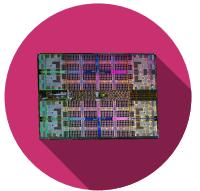




Transistor Level

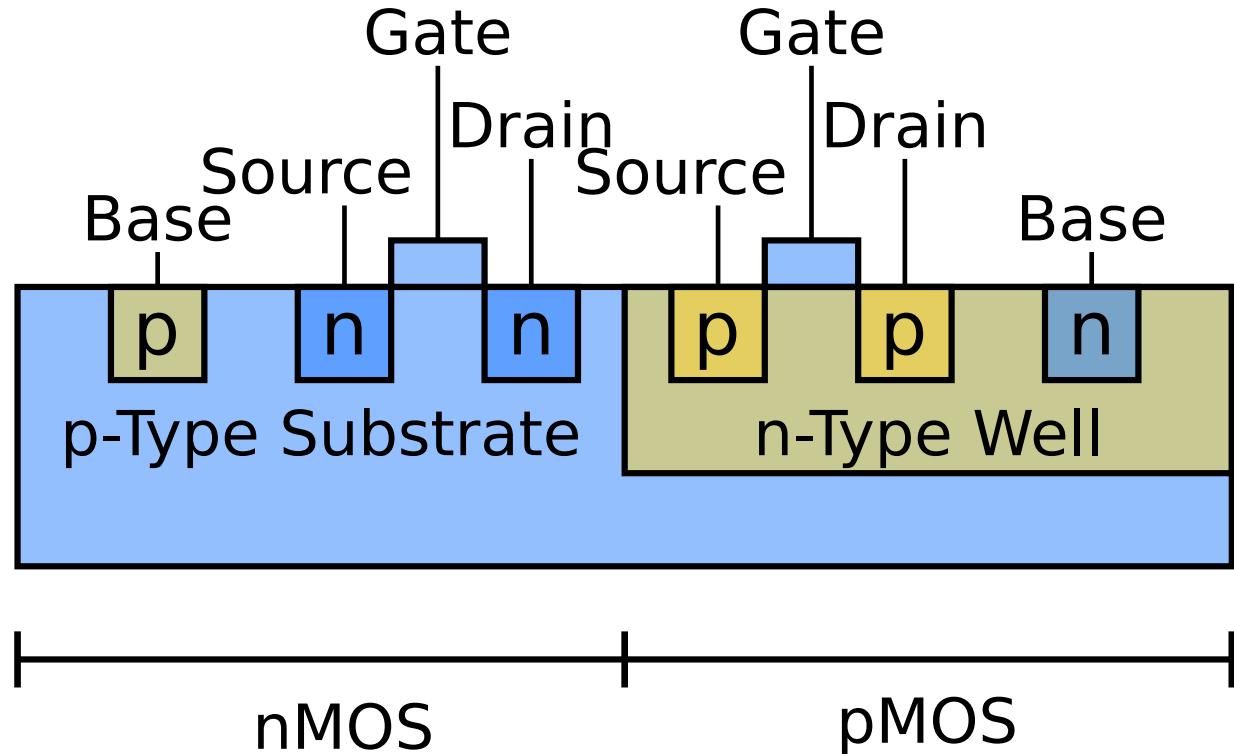
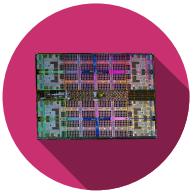
# Transistor Level

## N-Channel



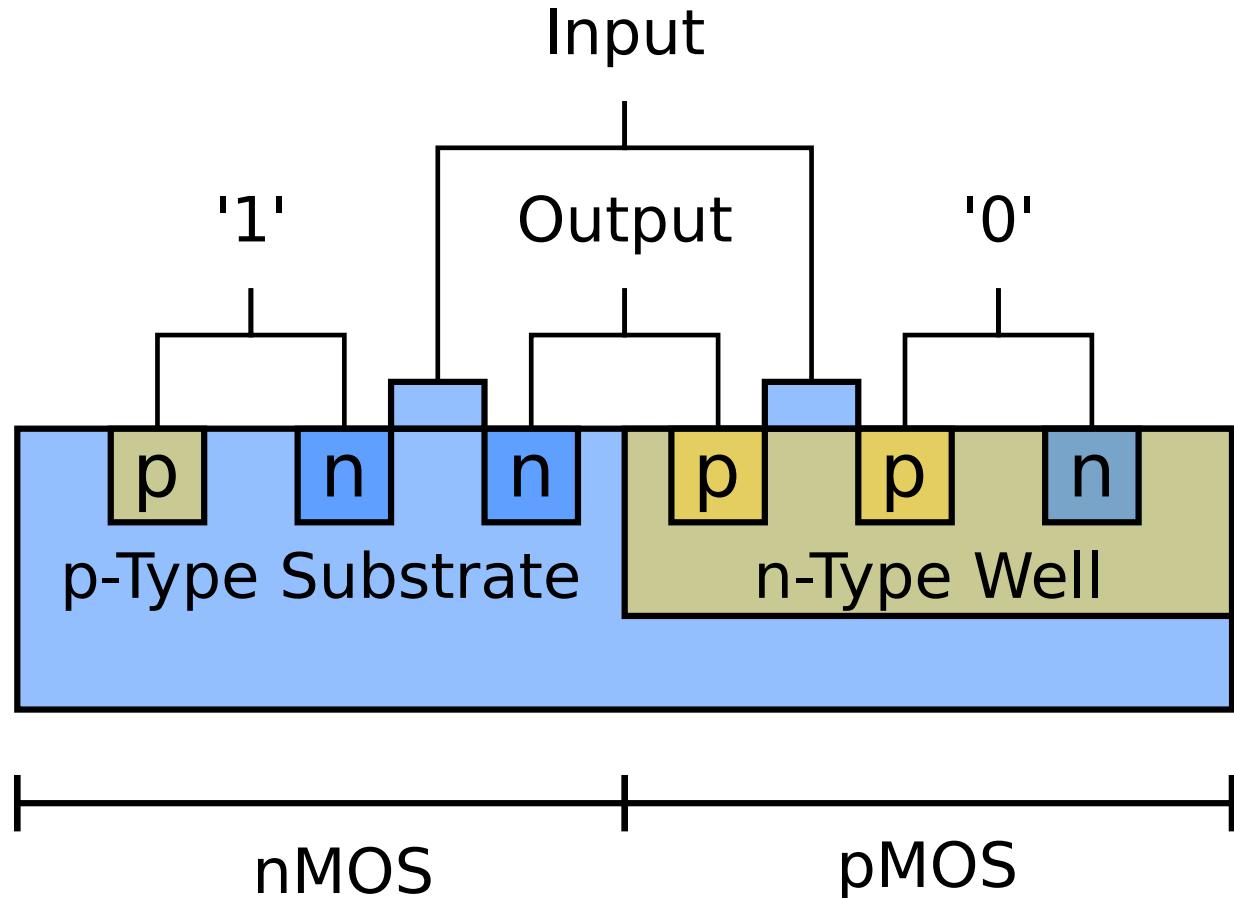
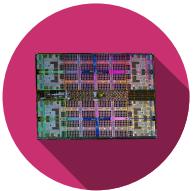
# Transistor Level

## CMOS



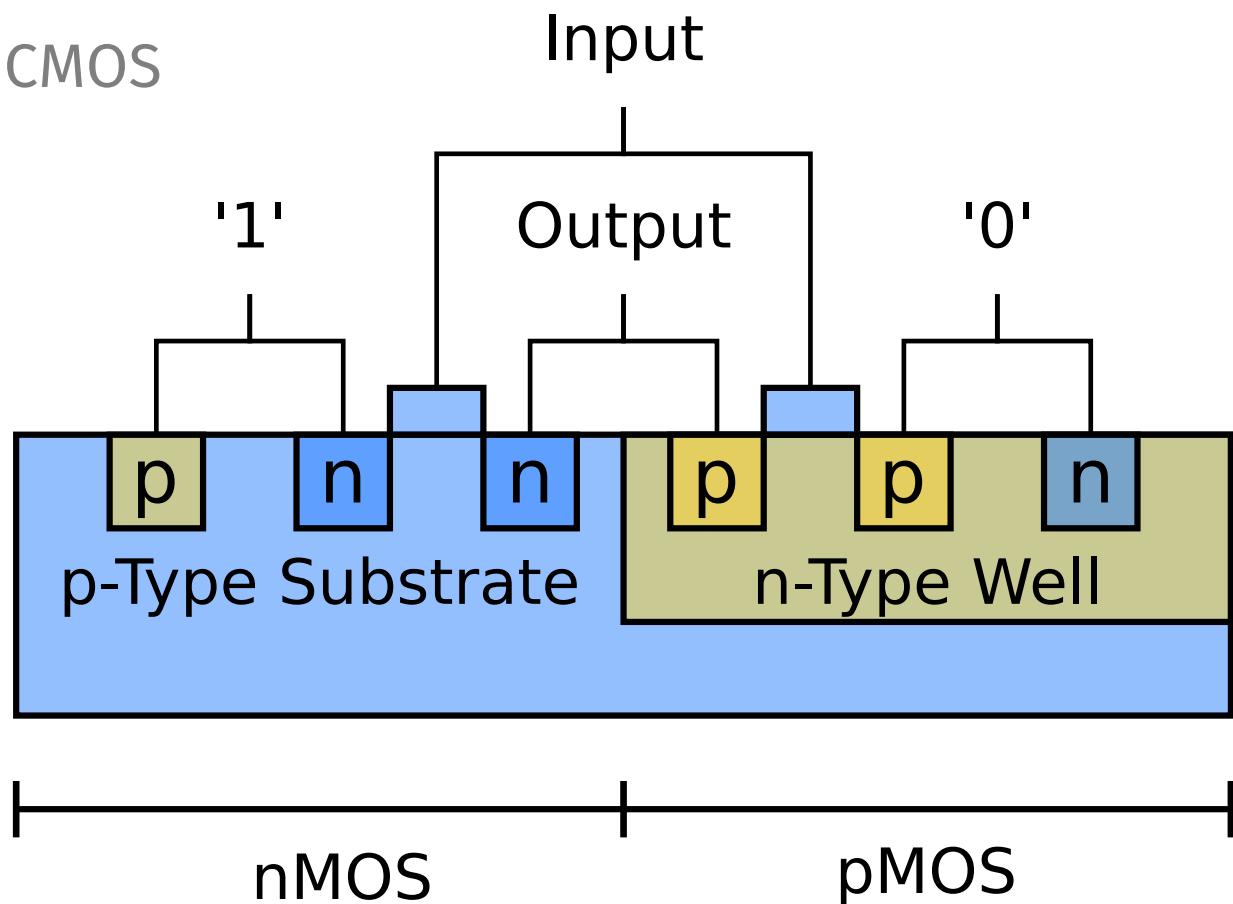
# Transistor Level

## CMOS

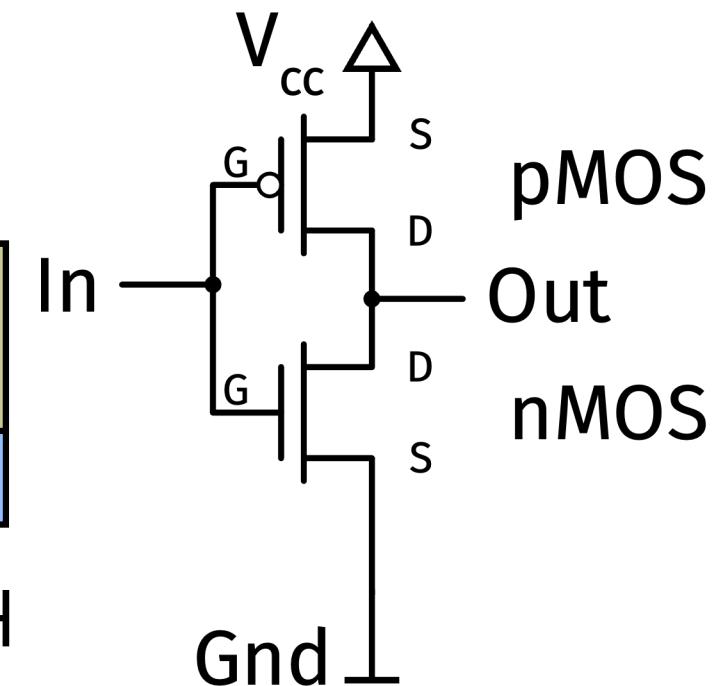
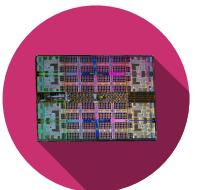


# Transistor Level

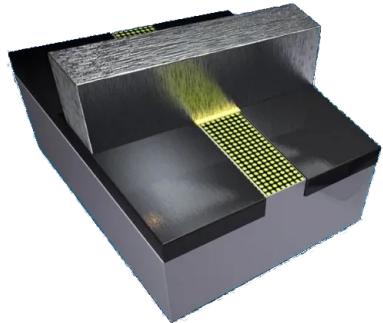
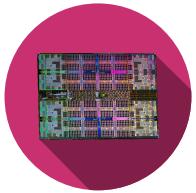
CMOS



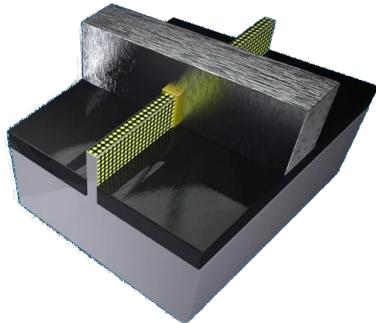
CMOS



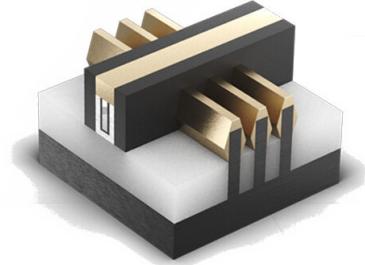
# Transistor Level Evolution



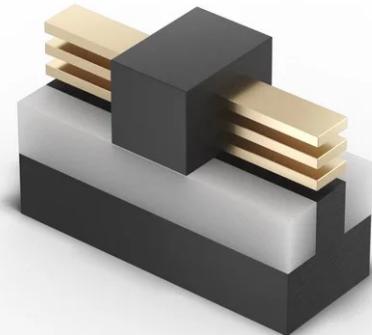
PlanarFET  
32nm



TriGateFET  
22nm



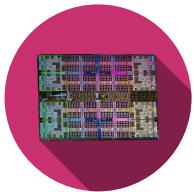
FinFET  
22nm-10nm



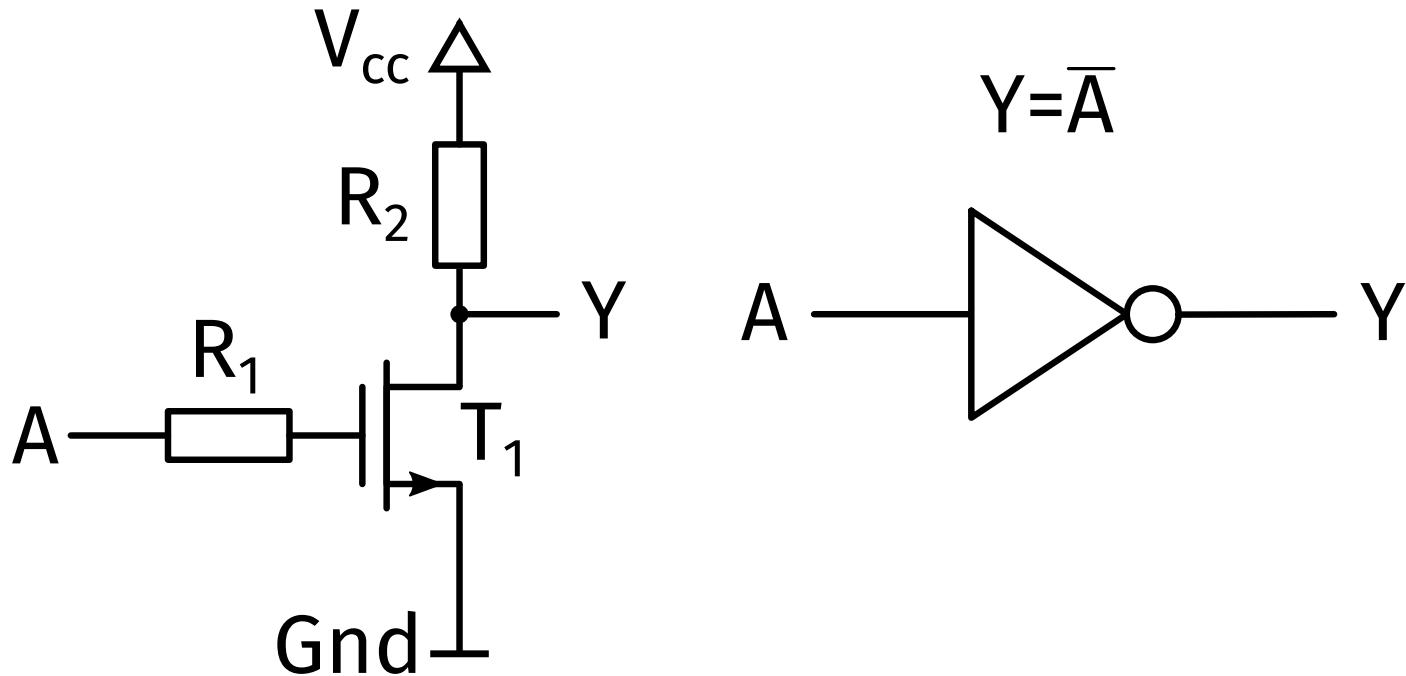
RibbonFET  
4nm

# Transistor Level

NOT



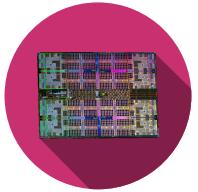
NOT

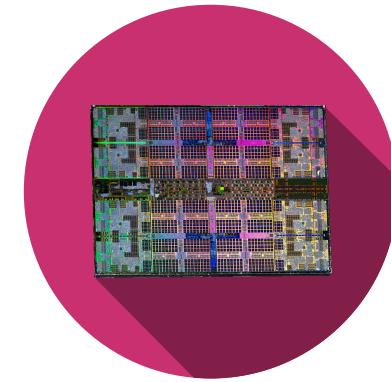


# Transistor Level

## Exercise

- Draw a AND and a OR on a transistor level

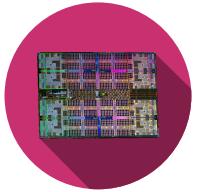




# Performance Growth

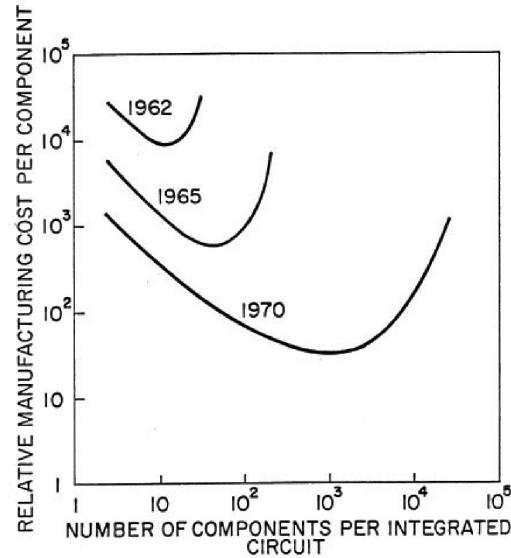
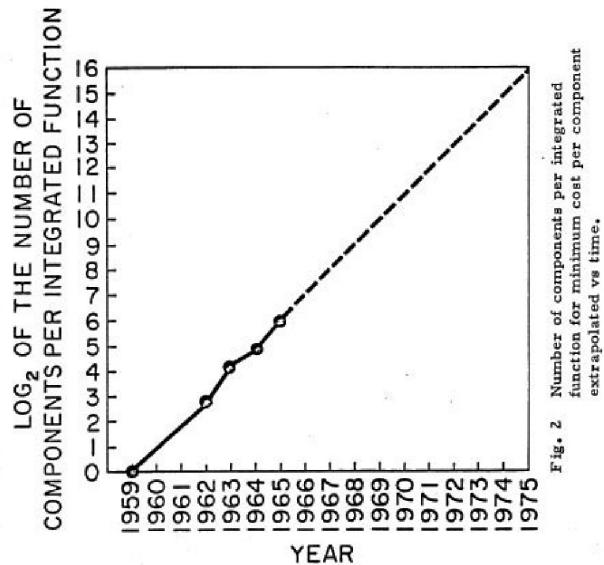
# Performance Growth

## Moore's Law



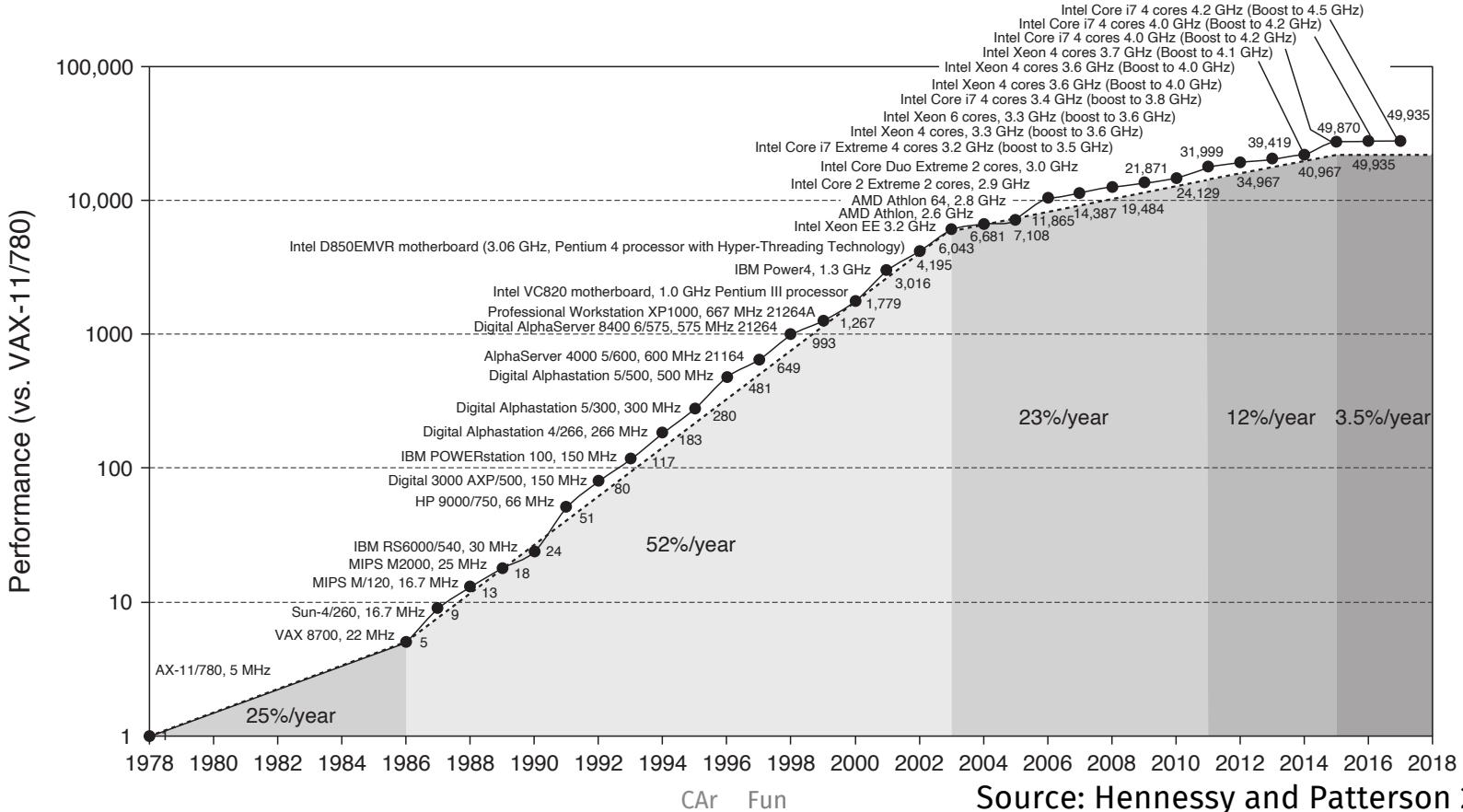
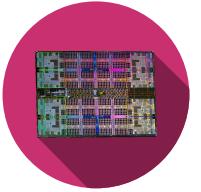
Every 18 Month twice as many transistors for the same amount of money

- Gordon Moore -



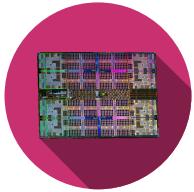
# Performance Growth

## Moore's Law



# Performance Growth

## Moore's Law

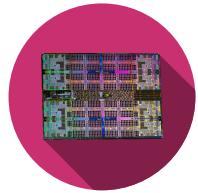


### Relevations of Moore's Law

- Size of transistors halves every 18 months
- Number of transistors per chip doubles every 18 months
- Frequency doubles every 18 months
- (Performance doubles every 18 months)

# Performance Growth

## Dennard Scaling



Robert Dennard observed the scaling trends in 1974 and analyzed what they implied for the future if devices became  $\frac{1}{k}$  smaller.

SCALING RESULTS FOR CIRCUIT PERFORMANCE

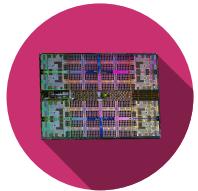
Device or Circuit Parameter	Scaling Factor
Device dimension $t_{ox}, L, W$	$1/k$
Doping concentration $N_e$	$k$
Voltage $V$	$1/k$
Current $I$	$1/k$
Capacitance $\epsilon A/t$	$1/k$
Delay time/circuit $VC/I$	$1/k$
Power dissipation/circuit $VI$	$1/k^2$
Power density $VI/A$	1

SCALING RESULTS FOR INTERCONNECTION LINES

Parameter	Scaling Factor
Line resistance, $R_L = \rho L/Wt$	$k$
Normalized voltage drop $IR_L/V$	$k$
Line response time $R_L C$	1
Line current density $I/A$	$k$

# Performance Growth

## Dennard Scaling



<i>Device or Circuit Parameters</i>	<i>Scaling Factor</i>
Device dimension $t_{ox}, L, W$	$1/k$
Doping concentration $N_a$	$k$
Voltage $V$	$1/k$
Current $I$	$1/k$
Capacitance $A/t$	$1/k$
Delay time/circuit $VC/I$	$1/k$
Power dissipation/circuit $VI$	$1/k^2$
Power density $VI/A$	1

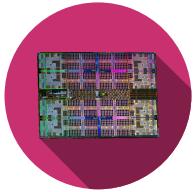
If we do scale these

We get these

=> Transistors run faster and use less power

# Performance Growth

## Moore's Law & Dennard Scaling



### Outcome

- Chip can fit 2x as many transistors
- Transistors can run 2x as fast
- Each transistor uses  $\frac{1}{4}$  the power

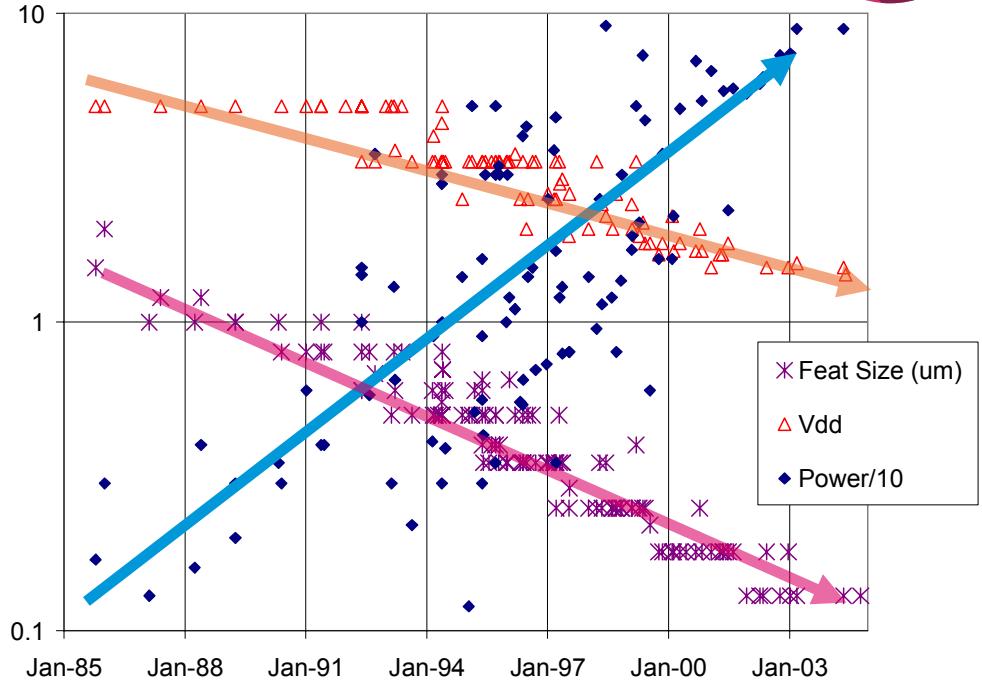
### Limitation

- Physical doping limits
  - How many atoms can we fit in
- Human greed
  - Frequency was not scaled as intended
- Voltage limits
  - Below 0.6V silicon transistors behave differently

# Performance Growth

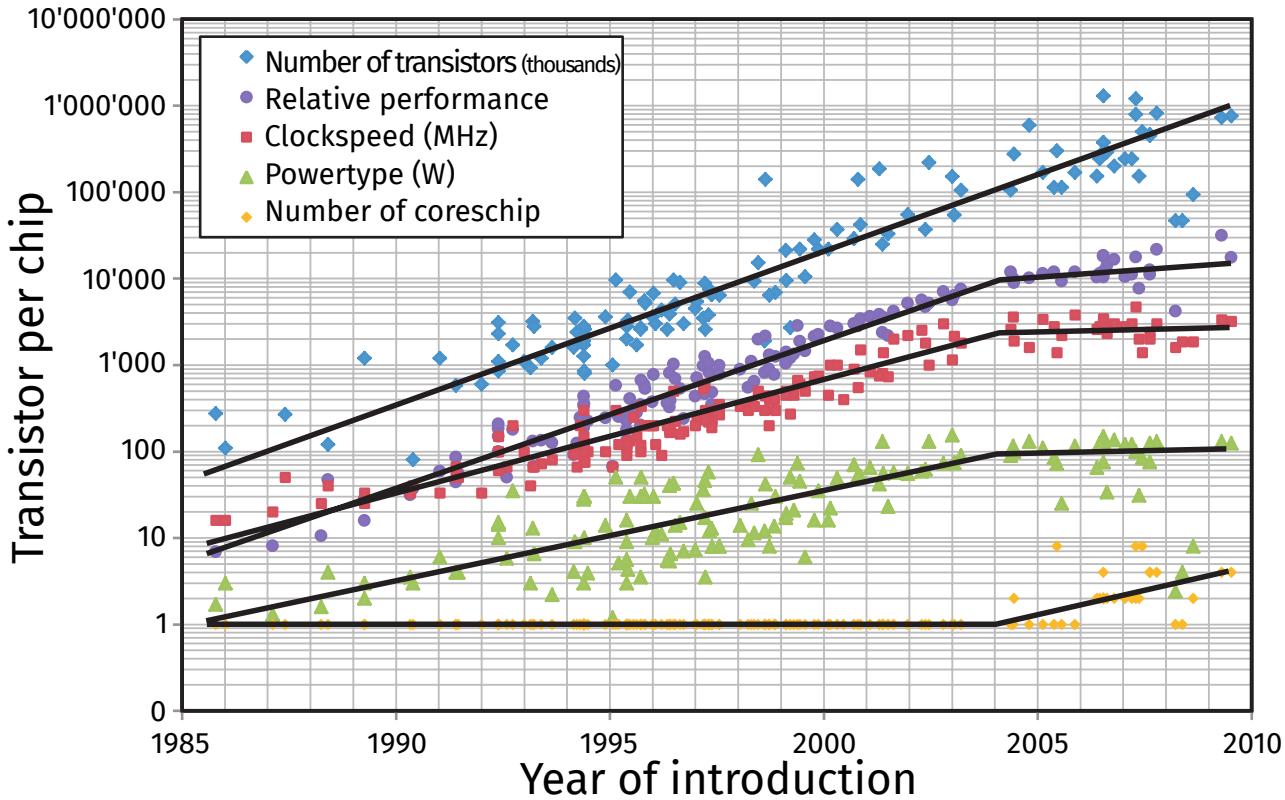
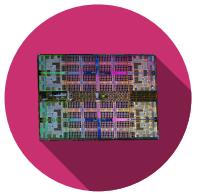
## Moore's Law & Dennard Scaling

- Transistors keep getting smaller
- Voltage is not keeping pace
- Result: Power does not scale if we increase frequency
- Transition to multicore
  - Much slower performance rise
  - Much harder to realize gains (4cores != 4x faster)
- Today: Focus in powerconsumption



# Performance Growth

## Moore's Law & Dennard Scaling



### Voltage/Frequency

- Can't reduce Voltage enough

### The Power Wall

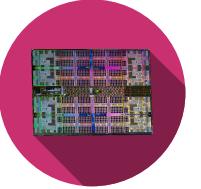
- Too expensive to cool anything hotter

### Result Multicore

# Performance Growth

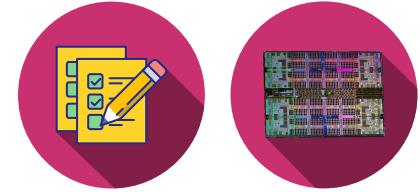
## Moore's Law & Dennard Scaling

*What is the main reason why the speed increase slowed down in recent years?*



# Performance Growth

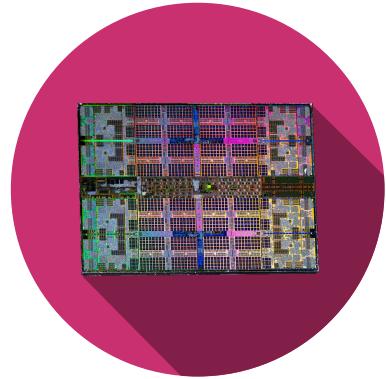
## Moore's Law & Dennard Scaling



*What is the main reason why the speed increase slowed down in recent years?*

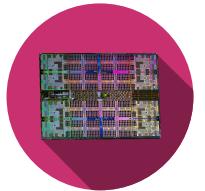
The circuits are still getting faster and we can make them (still) smaller. Also the chip size increases with the help of chiplets and other technologies.

The problem is that the minimum Voltage is determined by silicon physics and cannot be changed.

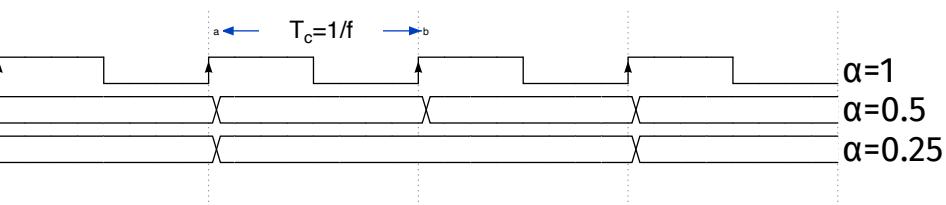


# Power Consumption

# Power Consumption of a Logic Gate



- $P_{total} = P_{dynamic} + P_{Static}$ 
  - $P_{dynamic} = \alpha C V_{DD}^2 f$
  - $P_{static} = V_{DD} I_{DD}$



$\alpha$  = Activity factor

C = Capacitance of logic gate  
and the wires

$V_{DD}$  = Voltage

$f$  = Clockfrequency

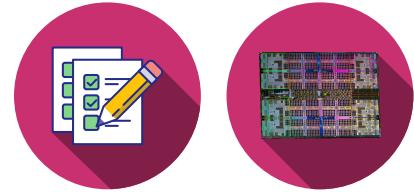
$I_{DD}$  = leakage current or  
quiescent supply current

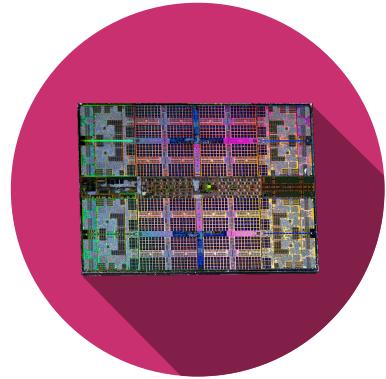
# Power Consumption

## Example

A particular cell phone has an **8W-hr battery** and operates at **0.707V**. Suppose that, when it is in use, the cell phone operates at **2GHz**. The total capacitance of the circuitry is **10 nF**, and the **activity factor is 0.05**. When voice or data are active (**10% of its time in use**), it also broadcasts **3W** of power out of its antenna. When the phone is not in use, the dynamic power drops to almost zero because the signal processing is turned off. But the phone also draws **100mA** of quiescent current whether it is in use or not.

Determine the battery life of the phone (a) if it is not being used and (b) if it is being used continuously.





# Fabrication

# Fabrication

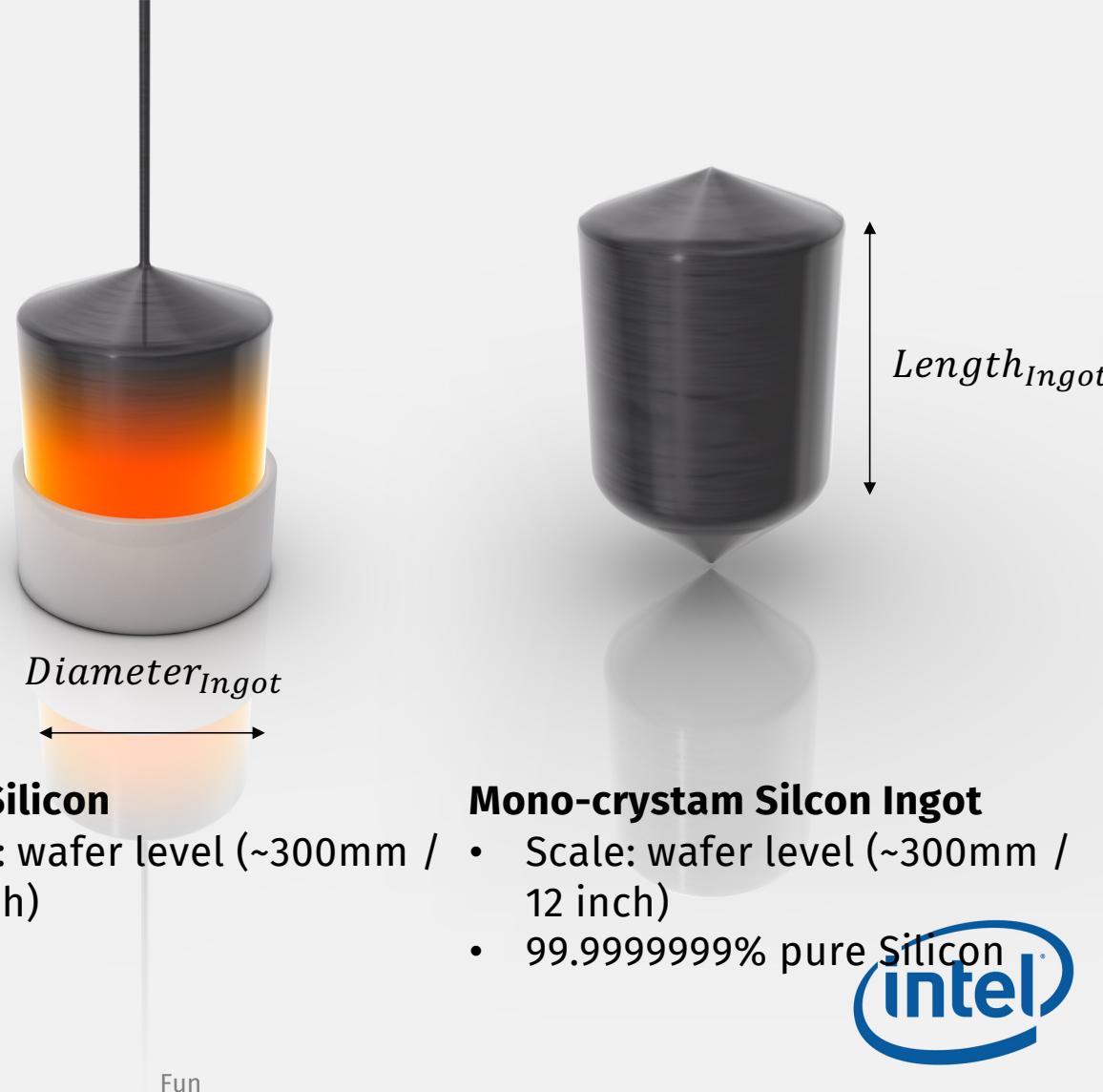
## Sand to Ingot



### Sand

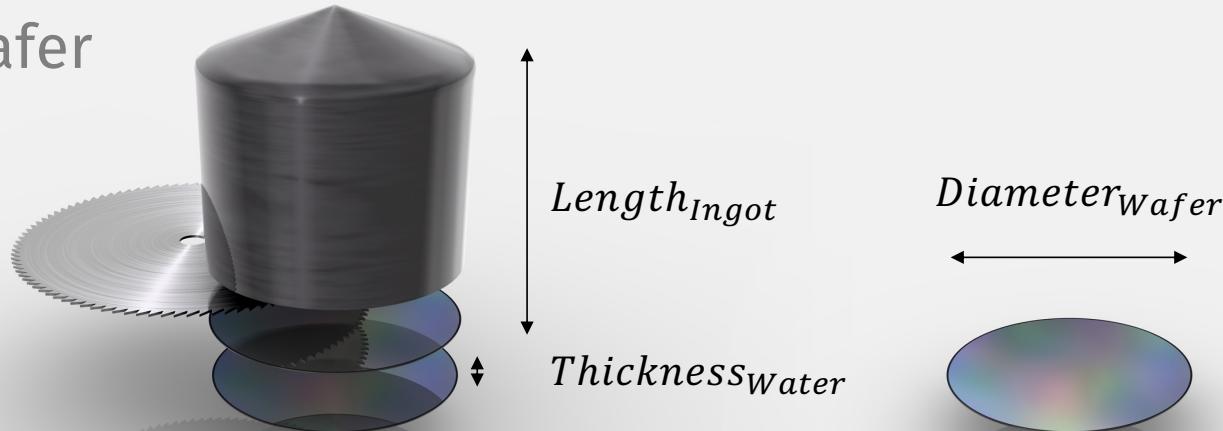
- 25 % is Silicon
- Second most frequent chemical element in the earth's crust  $\text{SiO}_2$

### 01 Sand Melted Into Ingot



# Fabrication

## Ingot to Wafer



$$\#Wafer = \frac{Length_{Ingot}}{Thickness_{Wafer}}$$

### Ingot Slicing

- Ingot is cut into individual discs called wafers

$$Area_{Wafer} = \pi * \left( \frac{Diameter_{Wafer}}{2} \right)^2$$

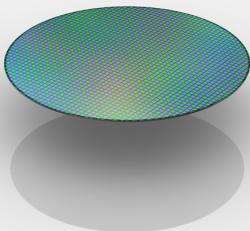
### Wafer

- Polished for a flawless mirror finish

02 Ingot Sliced Into Wafer

# Fabrication

## Ion Implantation

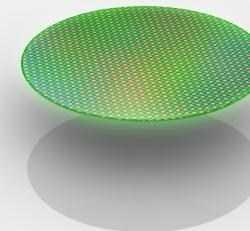
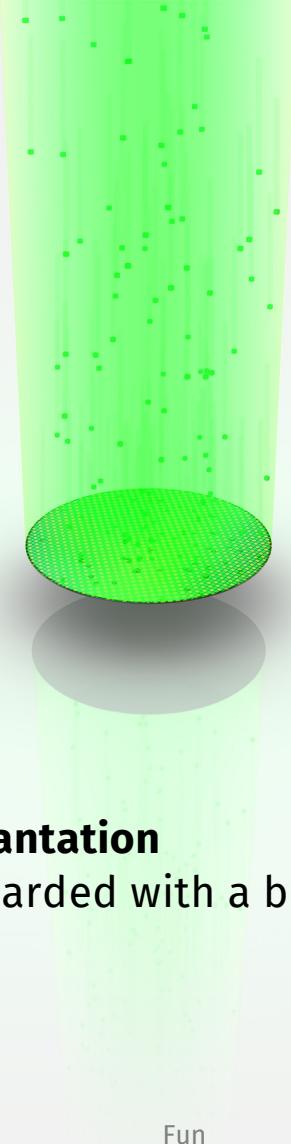


### Applying Photo Resist

- Protects zones where no ions should be implanted

### Ion Implantation

- Bombarded with a beam of ions

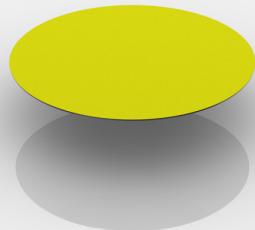
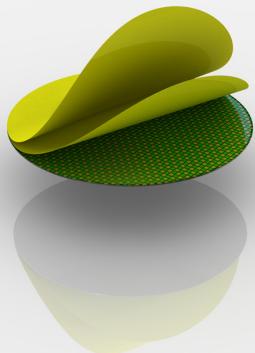
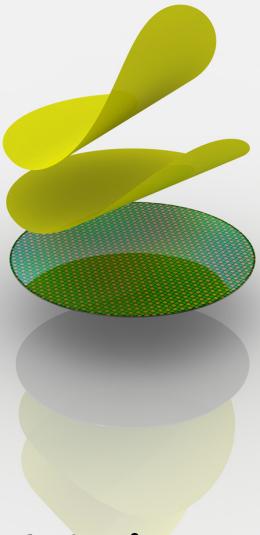


### Removing Photo Resist

- Removing the protecting material

# Fabrication

## High-k Material Application



### Applying High-k Dielectric

- Isolation between transistor's gate and it's channel
- Improves energy-efficiency

### Applying High-k Dielectric

- Multiple layers are applied

### High-K Dielectric

- Less current leaks

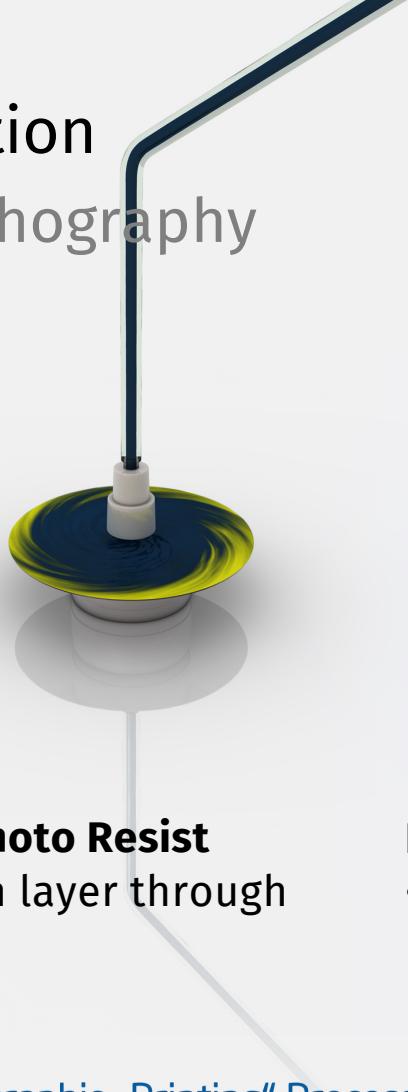
## 04 High-k Material Application

Fun



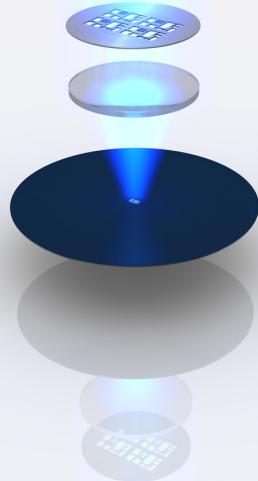
# Fabrication

## Photolithography



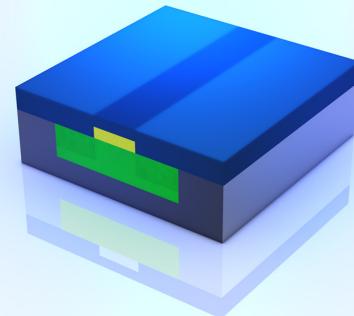
### Applying Photo Resist

- Very thin layer through spinning



### Exposure

- UV Light removes part of the applied film

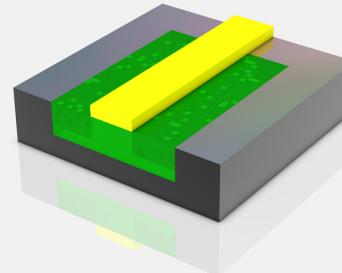
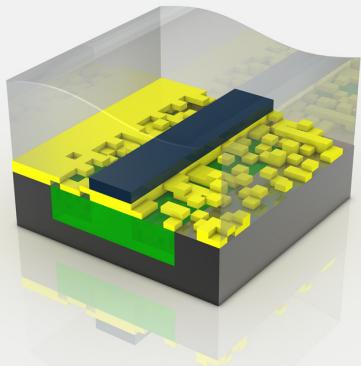
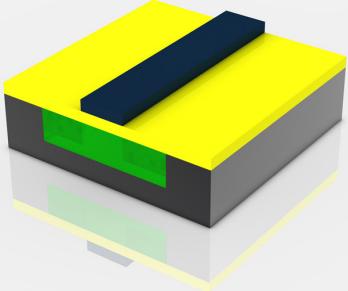


### Exposure

- We will focus on a small part from now on

# Fabrication

## Etching



### Washing off of Photo Resist

- Remove the Photo Resist layer completely

### Etching

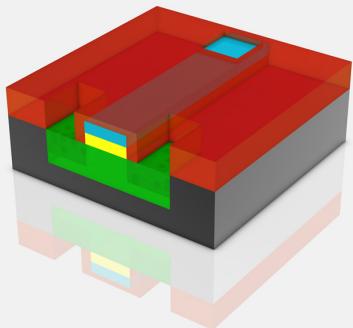
- With chemicals etching away the unprotected areas

### Removing Photo Resist

- After removing the remaining photo resist the intend shape is visible

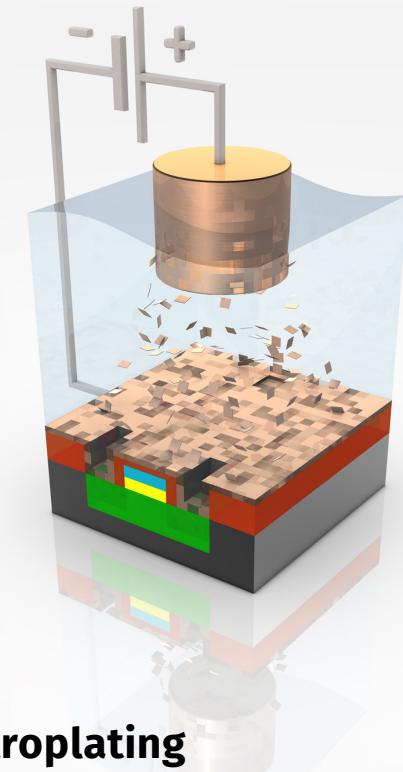
# Fabrication

## Metal Deposition



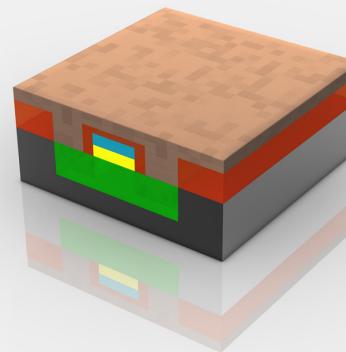
### Ready Transistor

- Holes have been etched to be filled with copper and other materials



### Electroplating

- Through an electrochemical process transfer copper ions onto the wafer

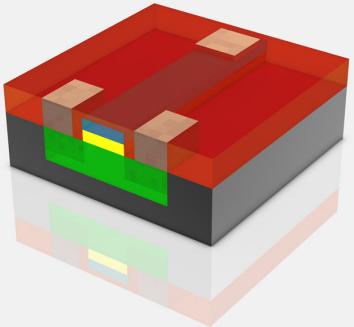


### After Electroplating

- Thin layer of copper is placed

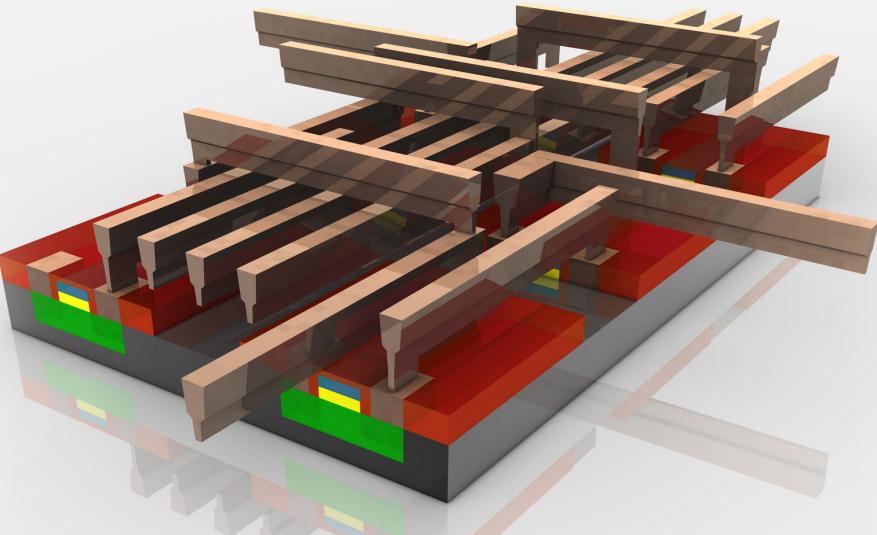
# Fabrication

## Metall Interconnections



### Polishing

- Excess material is polished off

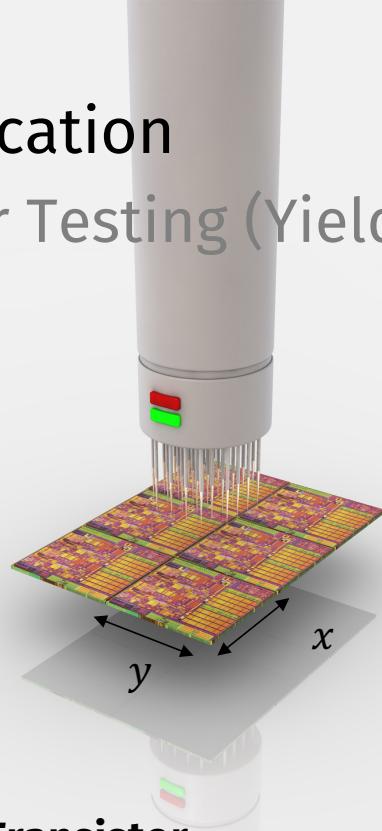


### Metal Layers

- Multiple metal layers create the interconnections
- It is a multi-layered highway system

# Fabrication

## Wafer Testing (Yield)

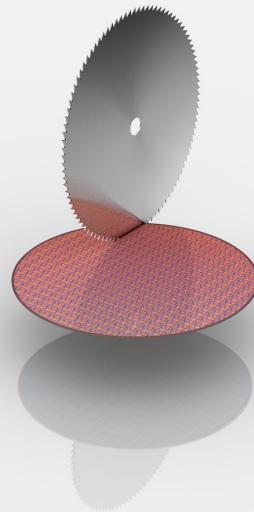


### Ready Transistor

- Holes have been etched to be filled with copper and other materials

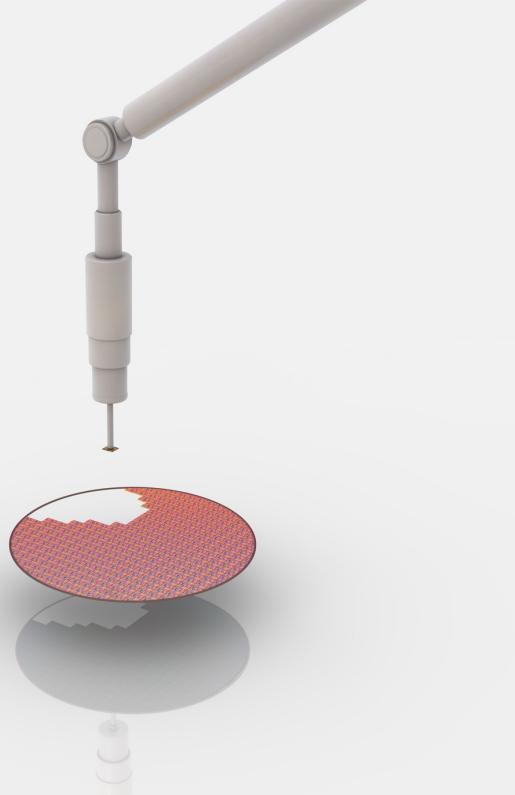
### Electroplating

- Through an electrochemical process transfer copper ions onto the wafer



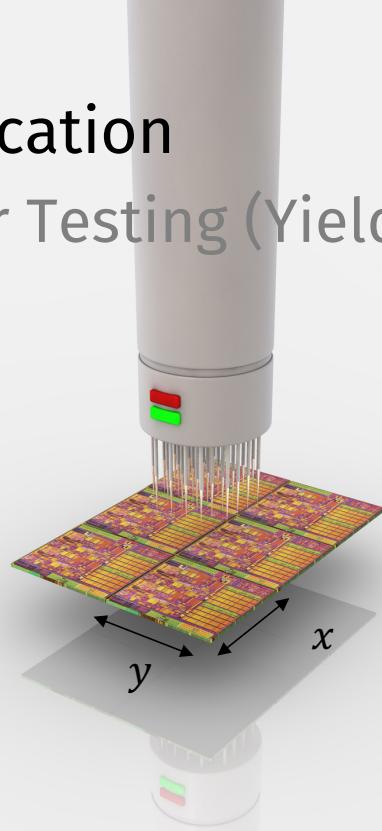
### After Electroplating

- Thin layer of copper is placed



# Fabrication

## Wafer Testing (Yield)



$$Area_{Die} = x * y$$

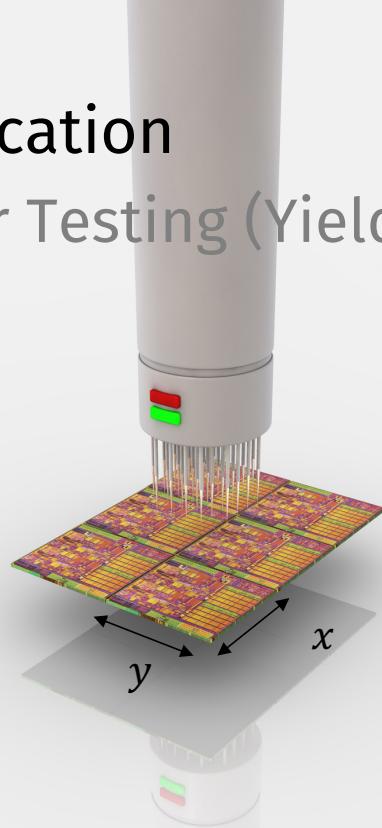


$$Yield = \frac{1}{(1 + \frac{Area_{Die} * Defect\_per\_Area}{2})^2}$$

$$\#Dies = \frac{Area_{wafer}}{Area_{Die}}$$

# Fabrication

## Wafer Testing (Yield)



$$Area_{Die} = x * y$$



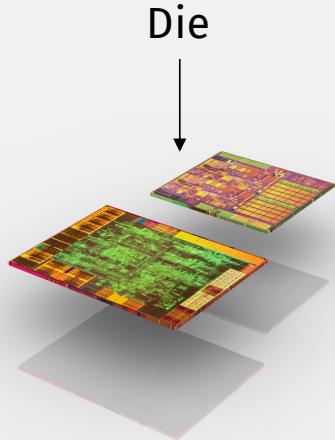
$$Yield = \frac{1}{(1 + \frac{Area_{Die} * Defect\_per\_Area}{2})^2}$$

$$\#Dies = \frac{Area_{wafer}}{Area_{Die}} - \frac{\pi * Diameter_{Wafer}}{\sqrt{2 * Area_{Die}}}$$



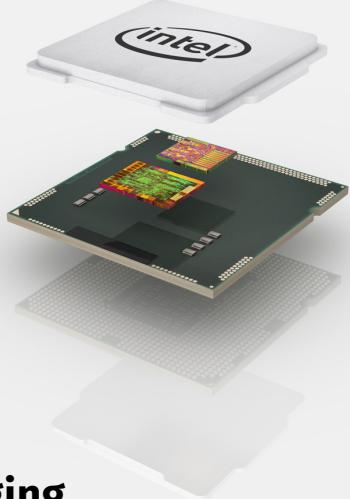
# Fabrication

## Packaging



**Individual Die**

10 Packaging



### Packaging

- Substrate and heatspreader is connected
- Microwires connect the transistors to the package pins



### Processor

- Finished product



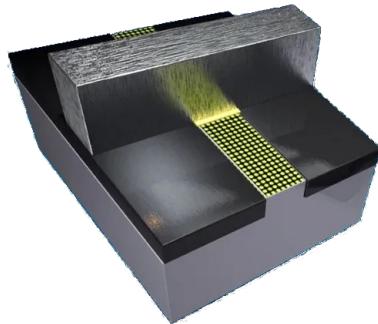
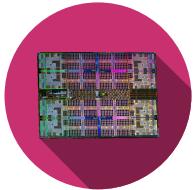
# Fabrication

## Testing and Sorting

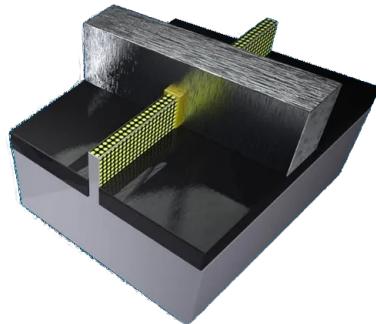


# Fabrication

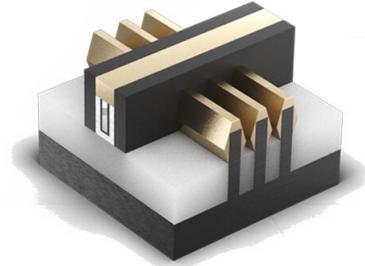
## Transistor Evolution



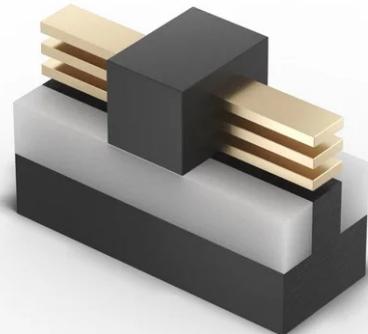
PlanarFET  
32nm



TriGateFET  
22nm



FinFET  
22nm-10nm

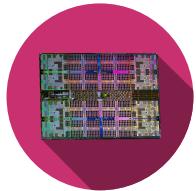


RibbonFET  
4nm

# Fabrication

## Factory Tours

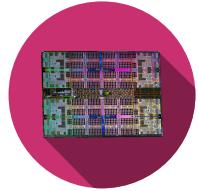
Know how the sauce gets made



- Intel - <https://www.youtube.com/watch?v=2ehSCWoa0qQ>
- Micron - <https://www.youtube.com/watch?v=-EhDlXx3okU>
- Cherry MX - <https://www.youtube.com/watch?v=Pu1gP4PfqCQ>
- Omron - <https://www.youtube.com/watch?v=9fNijKh6q-E>
- One Plus 6 QC - <https://www.youtube.com/watch?v=ES-s9KQrUTY>

Source : Linus Tech Tips <https://www.youtube.com/@LinusTechTip>

# References



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G. E. Moore, "Cramming more components onto integrated circuits, Reprinted from Electronics, volume 38, number 8, April 19, 1965, pp.114 ff.," *IEEE Solid-State Circuits Society Newsletter*, vol. 11, no. 3, pp. 33–35, Sep. 2006, doi: [10.1109/N-SSC.2006.4785860](https://doi.org/10.1109/N-SSC.2006.4785860).

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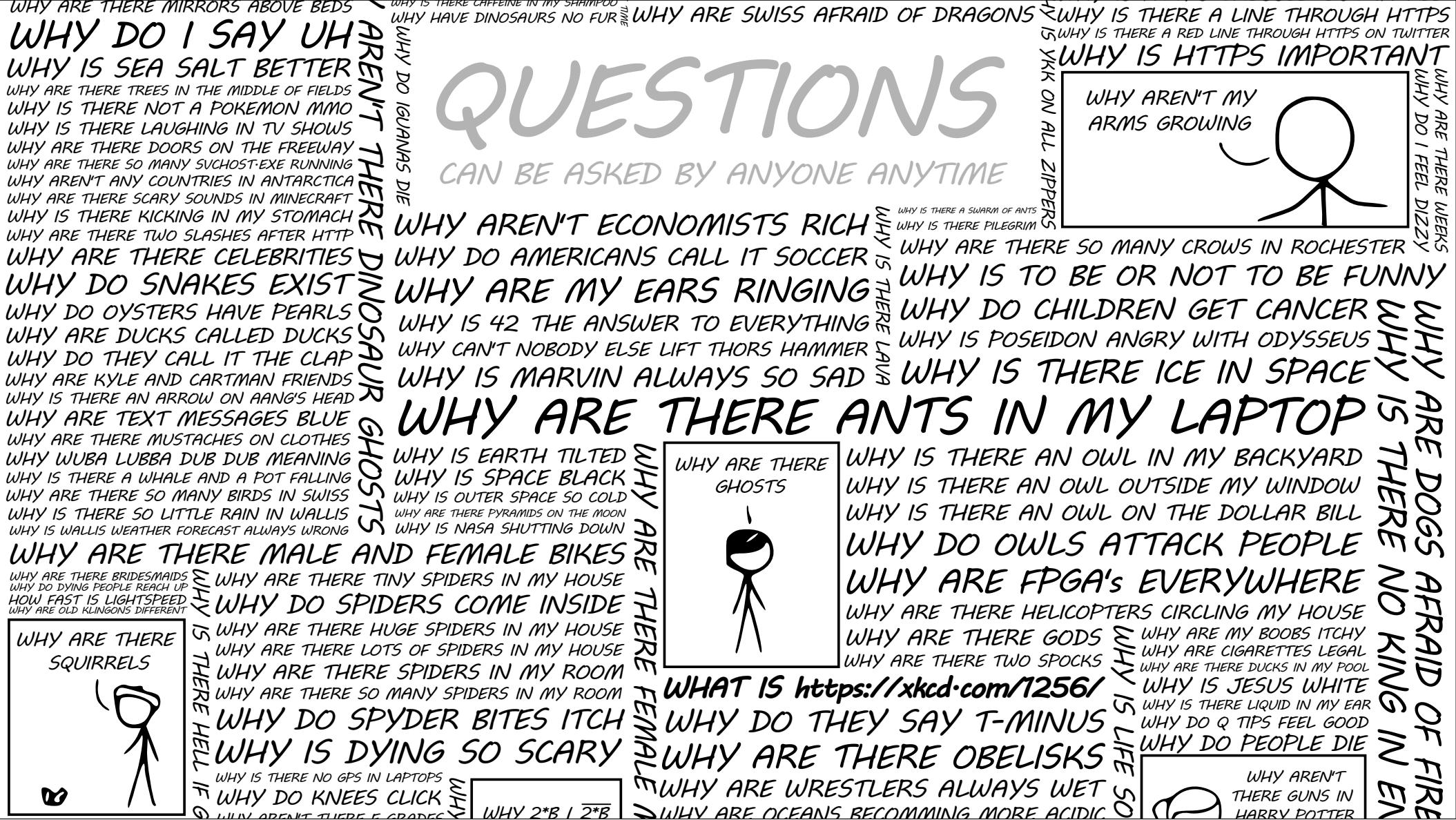
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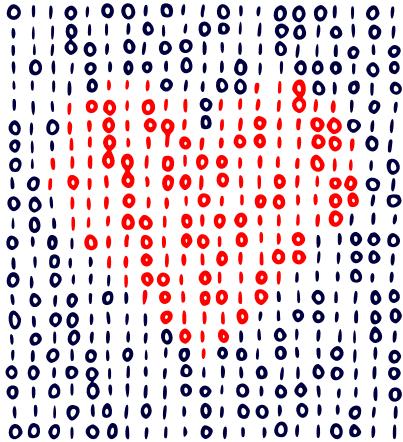
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STMicroelectronics, "Introduction to semiconductor technology," p. 15, 2000.

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