

# **Fundamentals**

## **Exercises Computer Architecture**

## 1 | Chip & Die Fabrication

#### 1.1 Fabrication

We wish to produce a chip that has a die size of  $15 \text{mm} \times 20 \text{mm}$ . The dies will be fabricated on 30 cm diameter silicon wafers. We purchase ingots for 20'000 CHF, each of which can be sliced into 100 wafers. We use a process which results in an average of  $0.12 \text{ defects per cm}^2$ 

- a) What is the fabrication yield?
- b) How many dies can fit on a wafer?
- c) How many good dies do we get per wafer?
- d) What is the cost per good die?

fun/fabrication-01

#### 1.2 Fabrication

We wish to produce a chip with a die size of  $150 \text{mm}^2$ . The dies will be fabricated on 20 cm diameter silicon wafers with a thickness of 5mm. We purchase ingots for 30'000 CHF, each has a length of 60cm. We use a process which results in an average of 0.2 defects per cm<sup>2</sup>, the package yield is 80% and the package cost are 0.06 CHF per die.

- a) How many wafers per ingot?
- b) What is the cost per wafer?
- c) What is the cost per cm<sup>2</sup> of the wafer?
- d) How many dies can fit on a wafer?
- e) How many good dies on a wafer?
- f) What does the final chip cost?

fun/fabrication-02

#### 1.3 Fabrication

A process uses a 20 cm diameter wafer and a  $52.3 \text{mm}^2$  die. The ingot costs 6000 CHF and can be sliced into 30 wafers. The process results in 0.03 defects per  $\text{mm}^2$ .

- a) How much does a wafer cost?
- b) What is the Yield?
- c) How many dies fit on a wafer?
- d) What is the cost per die?



fun/fabrication-03

## 2 | Moore's Law & Denard scaling

### 2.1 Dennard Scaling

If the number of transistors per unit area (i.e., on the same chip size) doubles every 24 months:

- a) By what factor does the length of the side of a transistor, assuming it is square, decrease every year?
- b) Starting with a length of 18.4nm (2014), what would be the size of a transistor in 2025? How does this compare to the value of  $6.75\mu m$ ?

fun/dennardscaling-01

### 2.2 Dynamic power consumption of a CMOS circuit is:

$\bigcirc$	directly proportional to the frequency
$\bigcirc$	inversely proportional to the frequency
0	directly proportional to the square of the supply voltage

fun/dennardscaling-02

## 3 | Power Consumption

### 3.1 Cell phone battery life

A particular cell phone has an 8W-hr battery and operates at 0.707V. Suppose that, when it is in use, the cell phone operates at 2GHz. The total capacitance of the circuitry is 10 nF, and the activity factor is 0.05. When voice or data are active (10% of its time in use), it also broadcasts 3W of power out of its antenna. When the phone is not in use, the dynamic power drops to almost zero because the signal processing is turned off. But the phone also draws 100mA of quiescent current whether it is in use or not.

Determine the battery life of the phone:

- a) if it is not being used
- b) if it is being used continuously

fun/powerconsumption-01