102 – Material Architecture

Module descriptioon

Degree programme	Computer science and communication	**Level**	Bachelor
Teaching axis	ICT fundamentals	**Major**	Common trunk
Academic year	2022-2023		

1. Description and organization

Module	Material Architecture	**Module code**	102
Type	Obligatoire	**ECTS credits**	9
Language(s)	French	**Academic year**	First year
Responsible	Silvan Zahno		

Code	Teaching units	S1	S2	SS1	S3	S4	SS2	S5	S6
102.1	Digital Systems	6							
102.2	Computer architecture		4						

Table 1: Teaching units, in weekly periods (45 min)

Volume de travail	Enseignement	Travail personnel	Total
	150 h	75 h	225 h

2. Prerequisites

- ☐ The module(s) should have been validated
- ☐ The module(s) should have been followed
- ☒ No prerequisite
- ☐ Other :

3. Skills targeted by the module

At the end of this module the student is capable[1] of:

- to interpret the specifications of a simple hardware system and to carry out the logical functions which result from it according to the basic principles of design and the methodologies proposed **(A)**
- to represent and understand the internal structure of a simple processor **(C)**
- perform processor performance calculations and compare them **(C)**
- select the hardware blocks of adequate calculations to perform a specific function **(A)**
- to understand the hardware development cycle **(C)**

[1] *The learning objectives of this module are classified according to the three increasing degrees of knowledge* ***(C)*** *Knowledge and understanding* ***(A)*** *Application,* ***(J)*** *Judgment (analysis, synthesis, evaluation).*

4. Evaluation and validation methods

The evaluation of the module is based on the evaluation of the different Teaching Units (UE), as follows:

Final mark of the module:

$$M = \frac{5 \cdot m_{\text{SysNum}} + 4 \cdot m_{\text{ArchOrd}}}{9}$$

Avec :

- m_{SysNum} – mark of *Digital Systems*
- m_{ArchOrd} – mark of *Computer architecture*

All grades and averages are specified to tenths of a point.

Pass condition:

- Final grade for module $M >= 4.0$ (rounded to half a point)
- Average of each of the UEs: $m >= 3.0$ (rounded to tenths of a point)

5. Remediation modalities

☐ Possible remediation
☒ No remediation
☐ Other

6. Repetition modalities

The student who repeats a module does not redo the teaching units of the module whose average m_i is equal to or greater than 5.0, rounded to ½ point. On request, the student can redo a unit of teaching to which he/she is not required.

7. Contents

UE descriptions are defined in the following pages.

Teaching unit *102.1 – Digital Systems*

Short description / objectives

In this course, you will learn the basics and individual building blocks of digital circuits. Classroom lessons are complemented by exercises, labs, and projects. You will develop your ability to design and build simple digital circuits in a autonomously using EDA (*Electronic design automation*) and simulation tools. In addition, you will begin to learn one of the engineering development methodologies by breaking a big problem into many small ones.

Teaching methods

- ☒ Courses and exercises
- ☒ Laboratories / TP
- ☐ Inverted class

Evaluation methods

An intermediate exam as well as the notation of the semester project in addition to the semester exam. The weight of each note is specified at the beginning of the semester.

Content (keywords)

1. Combinatorial logic - Numerical representations and operations, combinatorial logic functions, multiplexers and demultiplexers
2. Sequential logic – Memory elements and flip-flops, synchronous counters, state machines
3. Design methodology and realization - Design methodology, logic states, programmable logic circuits

Course materials

Script, slides, exercises, labs and mini-projects

Used tools

- Development environment *Mentor HDL-Designer*, *Mentor Modelsim*, *AMD Xilinx ISE/Vivado*

Bibliography

Organizational particularity

No specific hours assigned to the lab, labs are defined week by week.

Teaching unit *102.2 – Computer architecture*

Short description / objectives

Starting from the bases acquired in the course *102.1 – Numerical systems*, this course approaches the basic knowledge of the operation and the organization of a processor, in particular in its aspects of logical operation, structural as well as the point of view of performance. These new skills will be put to the test in working groups in the laboratory and within the framework of a semester-long project.

Teaching methods

- ☒ Courses and exercises
- ☒ Laboratories / TP
- ☐ Inverted class

Evaluation methods

At least 2 marks during the semester, the weight of which is specified at the beginning of the semester. This module does not have a semester exam.

Content (keywords)

- Performance calculations
- Benchmark
- Implementation possibilities
- Microarchitectures
- *Instruction Set Architecture*
- `RISC-V`.

Course materials

Script, slides, exercises, labs and mini-projects

Used tools

- `SiFive Freedom SDK`
- VHDL hardware description language
- Development environment `Mentor HDL-Designer`, `Mentor Modelsim`, `AMD Xilinx ISE`/`Vivado`

Bibliography

- John Hennessy, David A. Patterson, *Computer Architecture, Sixth Edition - A Quantitative Approach*, ISBN 978-0-12-811905-1, 2019.
- John Hennessy, David A. Patterson, *Computer Organization and Design, RISC-V Edition, Second Edition*, ISBN 978-0-12-820331-6, 2021.
- Sarah L. Harris, David M. Harris, *Digital Design and Computer Architecture, RISC-V Edition*, ISBN 978-0-12-820064-3, 2022.

Organizational particularity

8. Validation

Validated on 11.8.2022 par Pierre-André Mudry, head of the ISC degree programme.