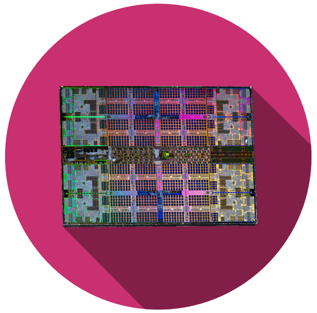
Computer Architecture

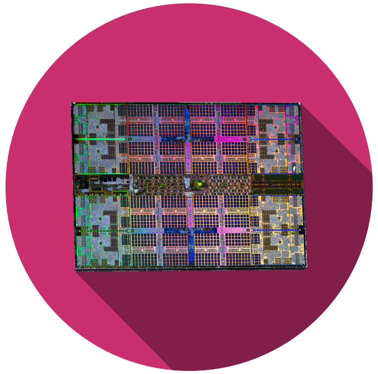
Single-Cycle RISC-V

SCR

Information and Communication Systems program



Silvan Zahno silvan.zahno@hevs.ch



RISC-V MicroArchitecture

RISC-V Processor

Instructions

Consider subset of RISC-V instructions:

- R-type instructions
  - `add, sub, or, slt`
- Memory instructions
  - `lw, sw`
- Branch instructions
  - `beq`

RISC-V Processor

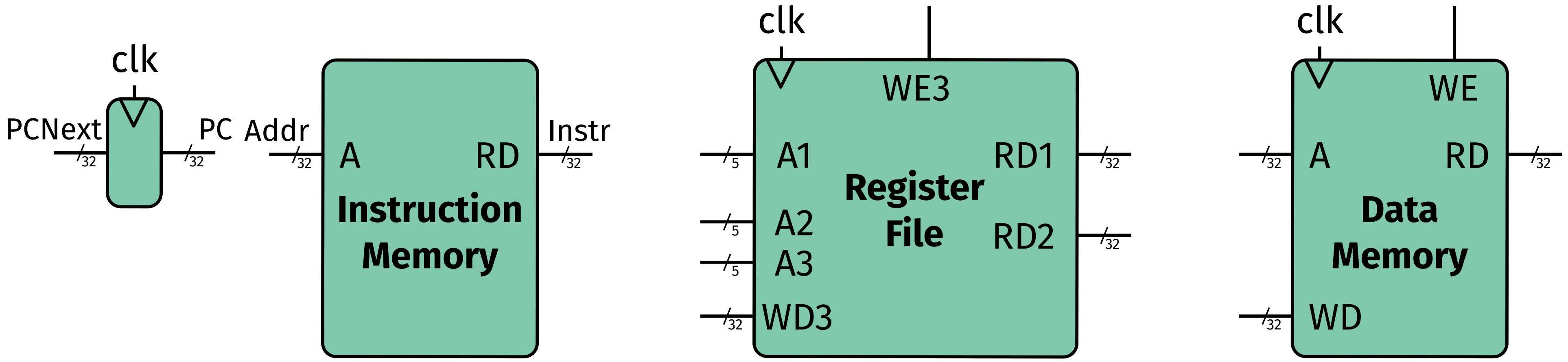
Architectural State Elements

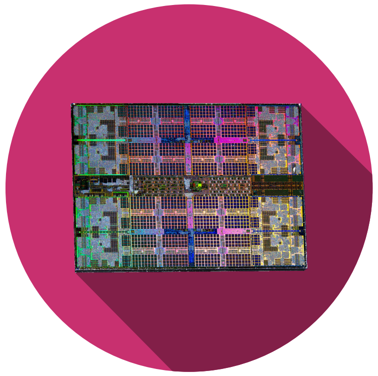
Determines everything about a processor at any given moment.

- Architectural state:
  - 32 Registers
  - PC
  - Memory

RISC-V Processor

Architectural State Elements





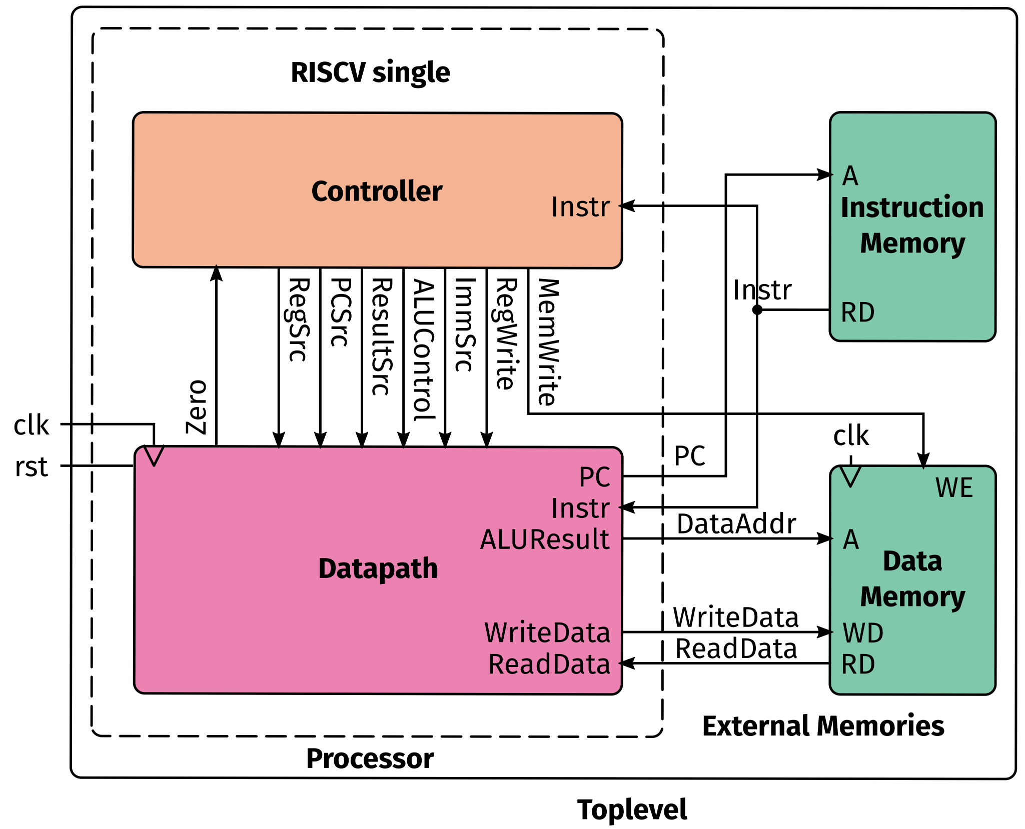
Single-Cycle RISC-V Processor

Single-Cycle RISC-V Processor
Example Program

Address	Instruction	Type	Fields						Machine Language
0x1000	L7: lw x6, -4(x9)	I	imm[11:0] 111111111100		rs1 01001	f3 010	rd 00110	op 0000011	FFC4A303
0x1004	sw x6, 8(x9)	S	imm[11:5] 0000000	rs2 00110	rs1 01001	f3 010	imm[4:0] 01000	op 0100011	0064A423
0x1008	or x4, x5, x6	R	funct7 0000000	rs2 00110	rs1 00101	f3 110	rd 00100	op 0110011	0062E233
0x100C	beq x4, x4, L7	B	imm[12,10:5] 1111111	rs2 00100	rs1 00100	f3 000	imm[4:1,11] 10101	op 1100011	FE420AE3

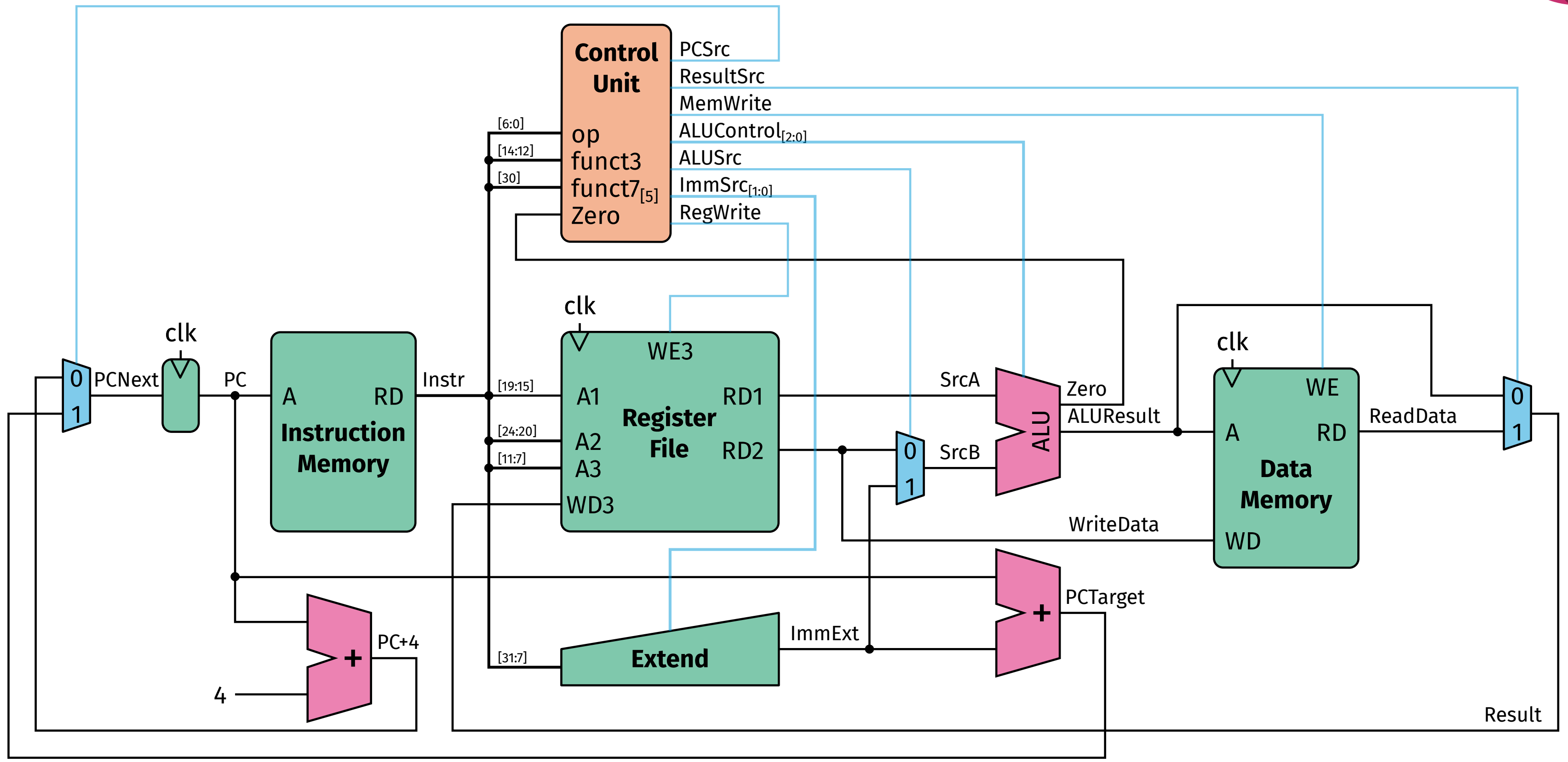
RISC-V

Toplevel



RISC-V

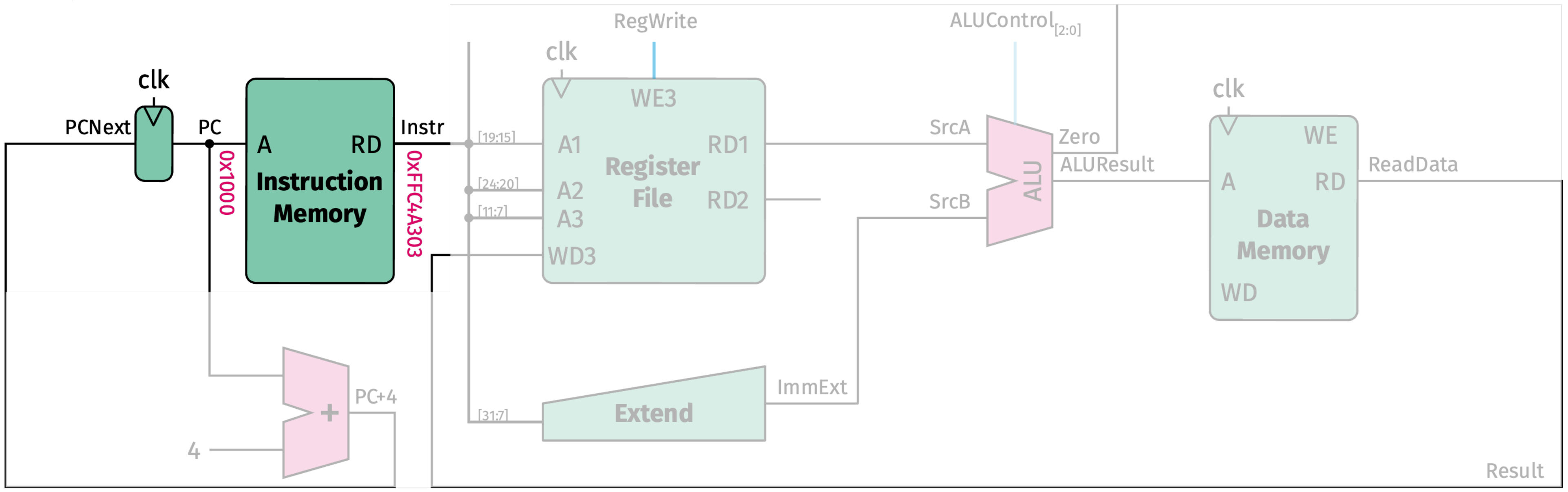
Singlecycle



RISC-V Single-Cycle

Instruction `lw` (I-Type) fetch

Step 1: Fetch instruction

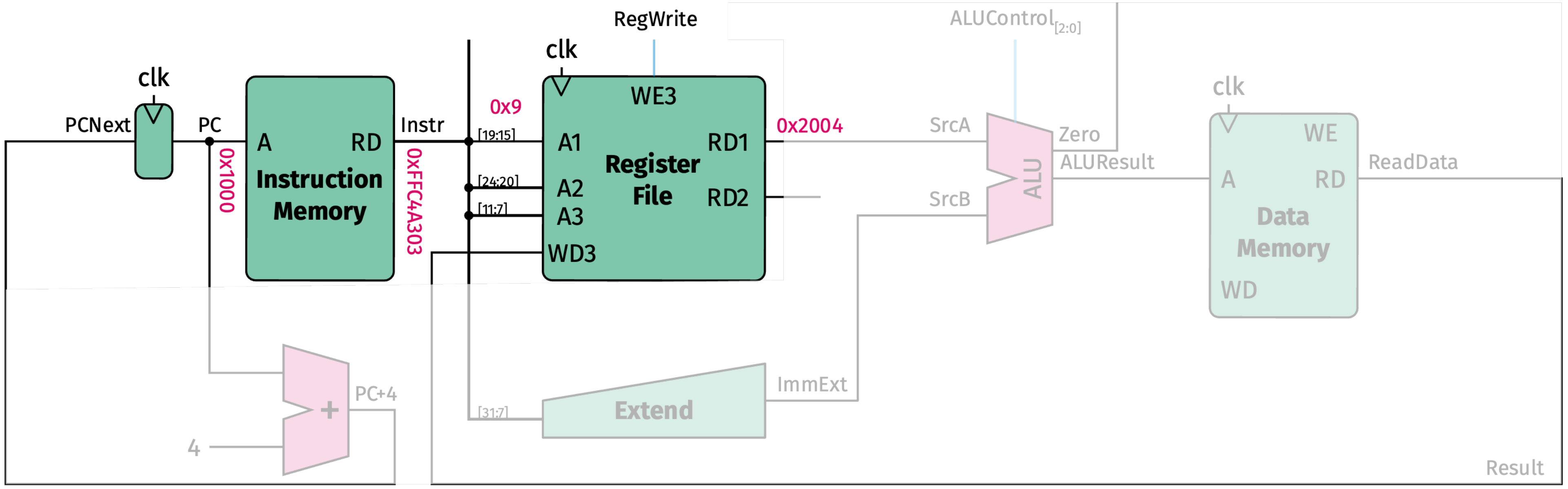


Address	Instruction	Type	Fields				Machine Lang
			imm[11:0]	rs1	f3	rd	op
0x1000	L7: lw x6, -4(x9)	I	111111111100	01001	010	00110	0000011 FFC4A303

RISC-V Single-Cycle

Instruction lw (I-Type) Reg Read

Step 2: Read source operand (rs1) from RF

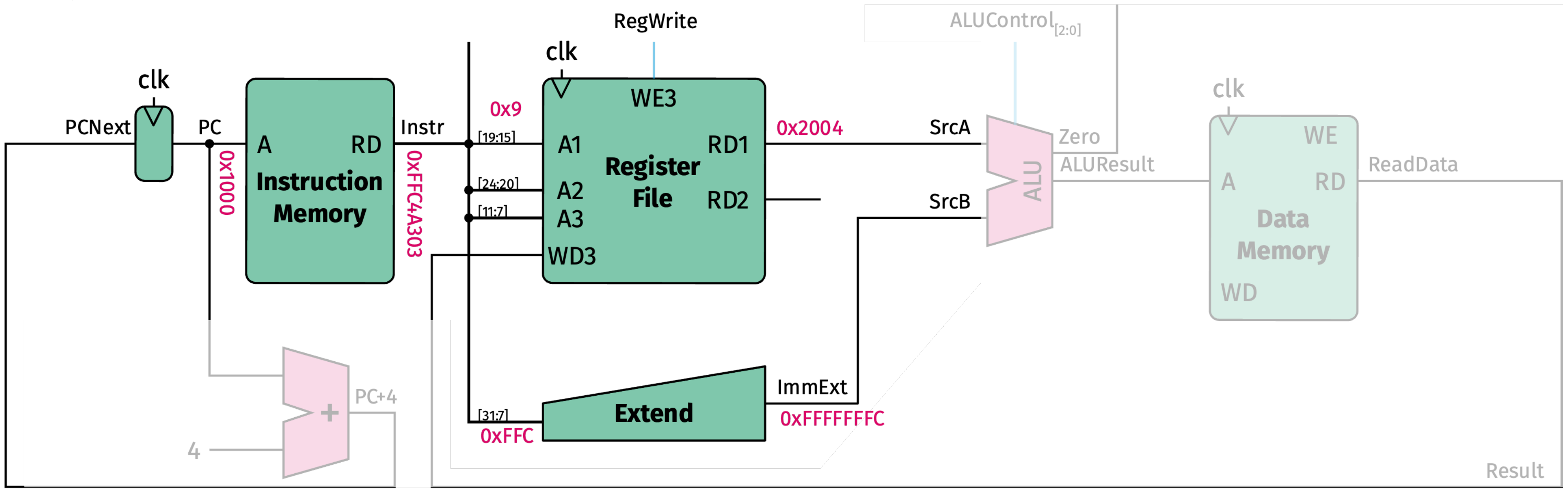


```
Address      Instruction        Type Fields                                        Machine Lang
                                     imm[11:0]           rs1   f3  rd          op
0x1000   L7: lw   x6, -4(x9)    I    111111111100        01001 010 00110       0000011 FFC4A303
```

RISC-V Single-Cycle

Instruction `lw` (I-Type) immediate

Step 3: Extend the immediate

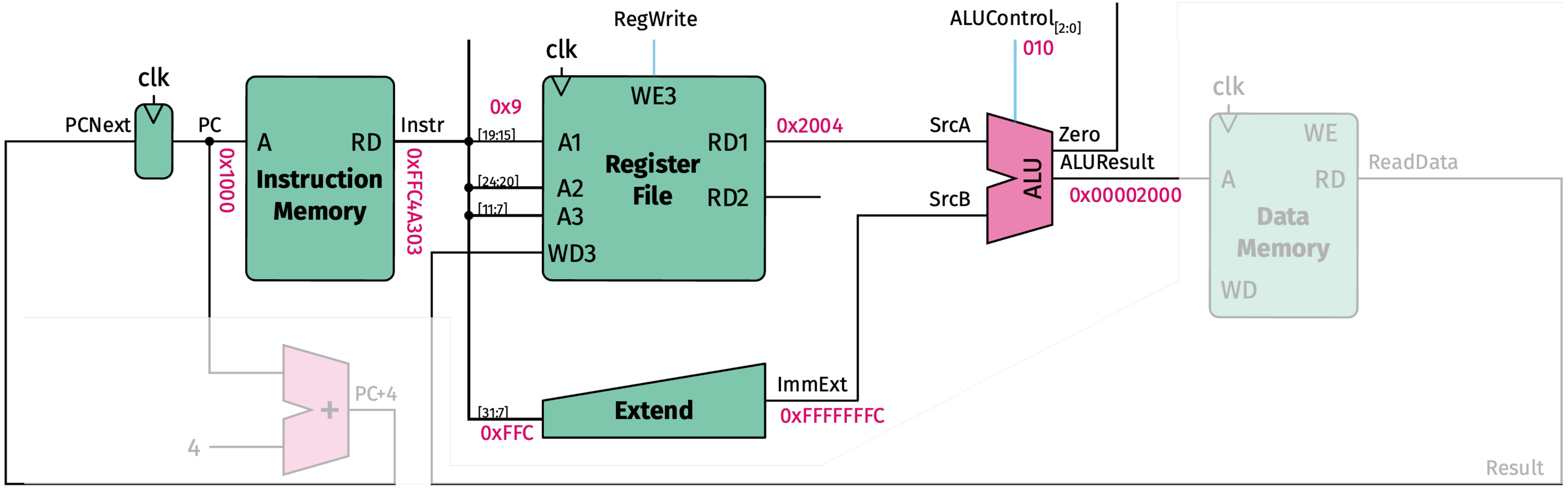


Address	Instruction	Type	Fields					Machine Lang
			imm[11:0]	rs1	f3	rd	op	
0x1000	L7: lw x6, -4(x9)	I	111111111100	01001	010	00110	0000011	FFC4A303

RISC-V Single-Cycle

Instruction lw (I-Type) Address

Step 4: Compute the memory address

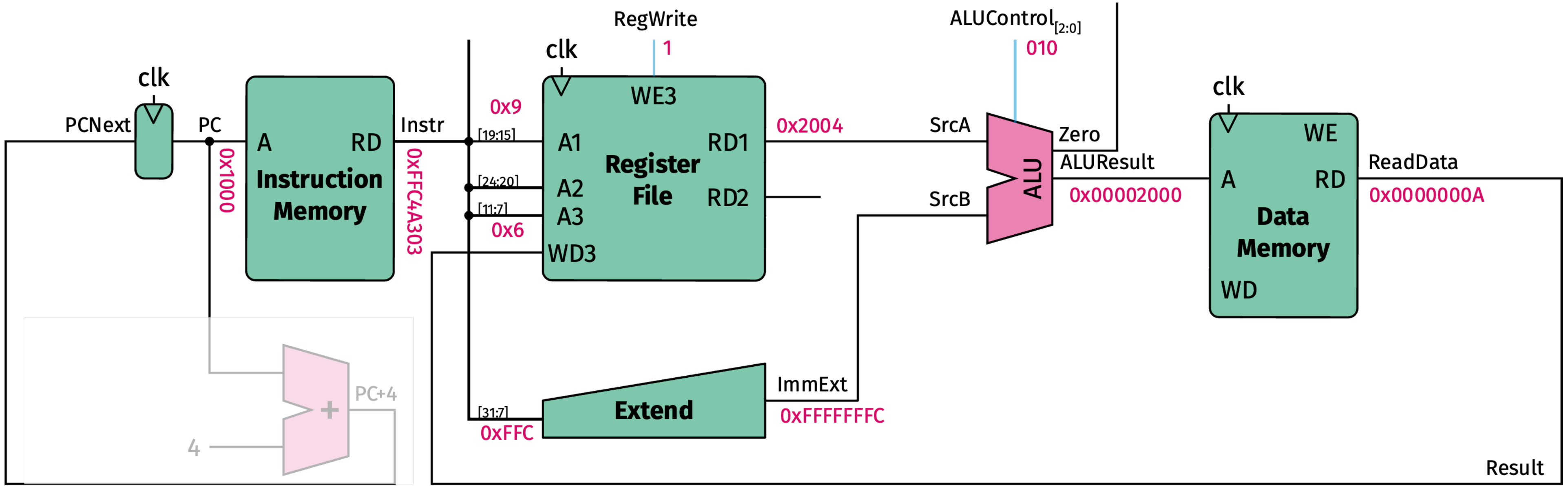


Address	Instruction	Type	Fields				Machine Lang
			imm[11:0]	rs1	f3	rd	op
0x1000	L7: lw x6, -4(x9)	I	111111111100	01001	010	00110	0000011 FFC4A303

RISC-V Single-Cycle

Instruction `lw` (I-Type) Mem Read

Step 5: Read data from memory and write it back to register file

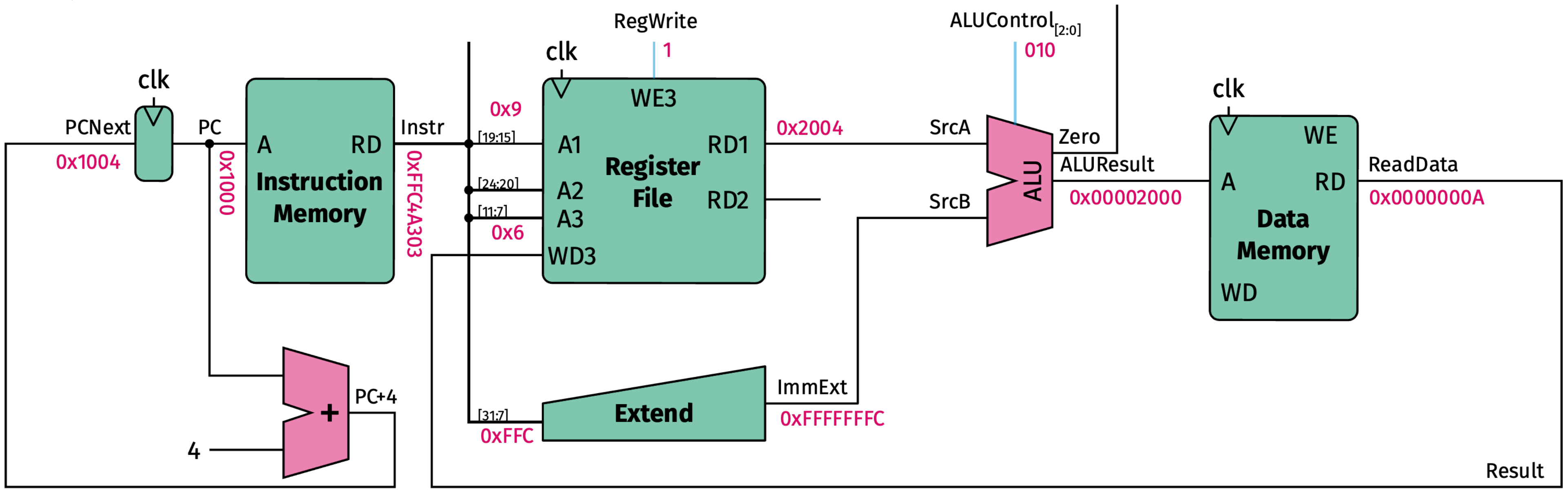


```
Address     Instruction        Type Fields                                              Machine Lang
                                    imm[11:0]            rs1    f3   rd           op
0x1000   L7: lw   x6, -4(x9)  I     111111111100         01001  010  00110        0000011 FFC4A303
```

RISC-V Single-Cycle

Instruction `lw` (I-Type) PC increment

Step 6: Determine address of next

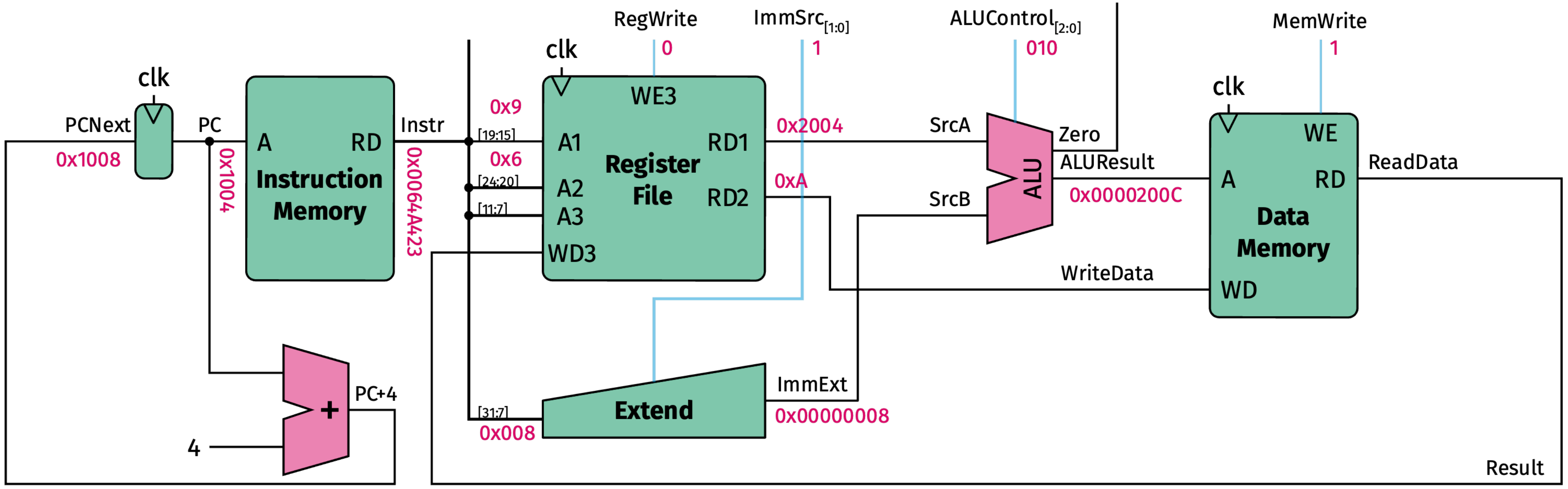


```
Address     Instruction      Type Fields                               Machine Lang
                                  imm[11:0]          rs1   f3  rd         op
0x1000   L7: lw   x6, -4(x9) I    111111111100       01001 010 00110      0000011 FFC4A303
```

RISC-V Single-Cycle

Instruction sw (S-Type)

Add control signals: `ImmSrc`, `MemWrite`

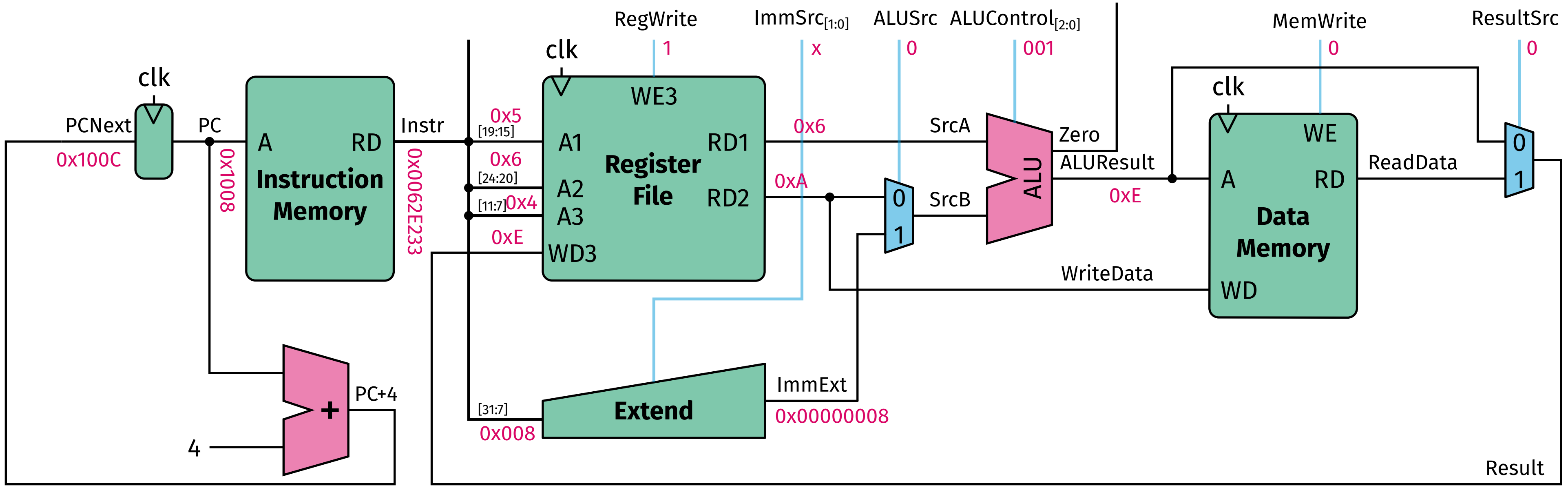


Address	Instruction	Type	Fields						Machine Lang
			imm[11:5]	rs2	rs1	f3	imm[4:0]	op	
0x1004	sw x6, 8(x9)	S	0000000	00110	01001	010	01000	0100011	0064A423

RISC-V Single-Cycle

Instruction or (R-Type)

Add control signals: `ALUSrc`, `ResultScr`

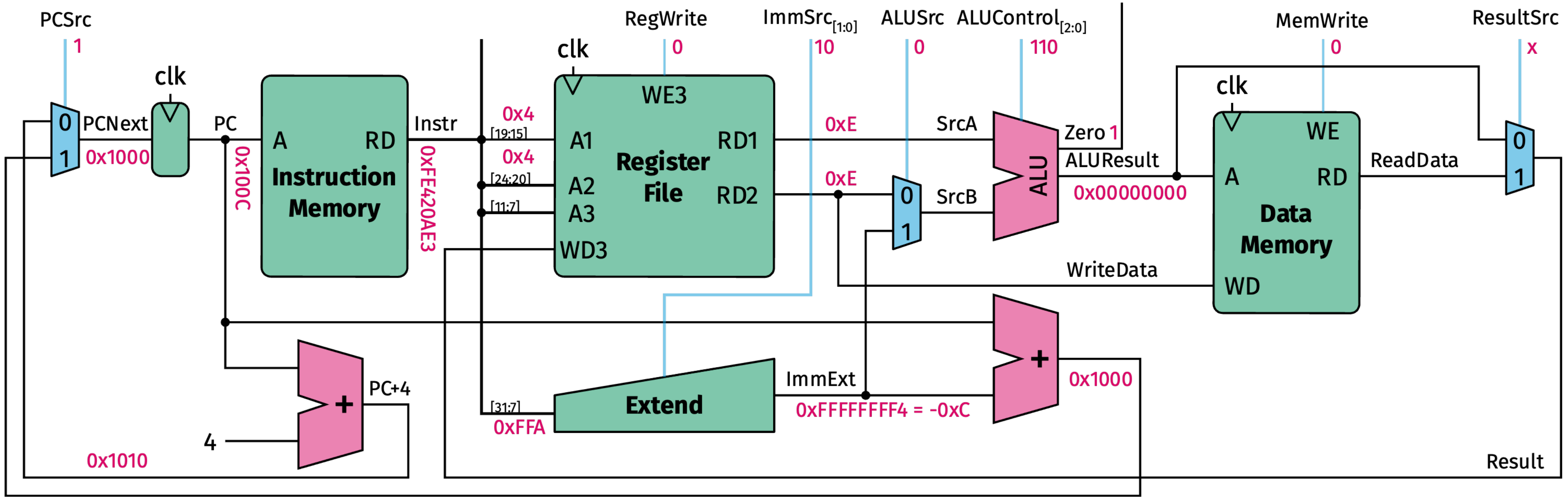


Address	Instruction	Type	Fields					Machine Lang	
			funct7	rs2	rs1	f3	rd	op	
0x1008	or x4, x5, x6	R	0000000	00110	00101	110	00100	0110011	0062E233

RISC-V Single-Cycle

Instruction beq (B-Type)

Add control signals: PCSrc

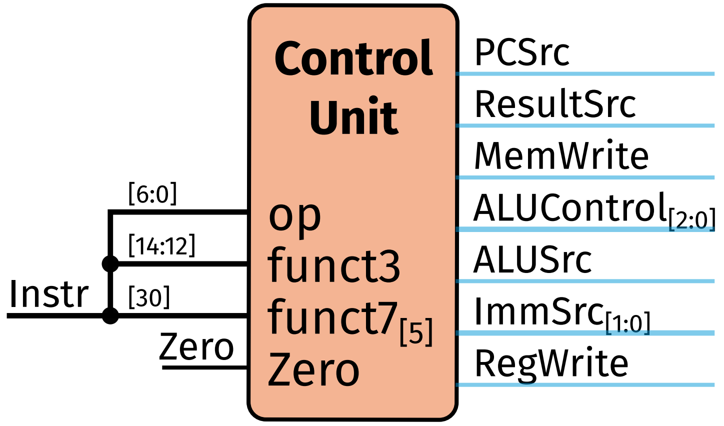


Address	Instruction	Type	Fields						Machine Lang
			imm[12,10:5]	rs1	rs2	f3	imm[4:1,11]	op	
0x100C	beq x4, x4, L7	B	1111111	00100	00100	000	10101	1100011	FE420AE3

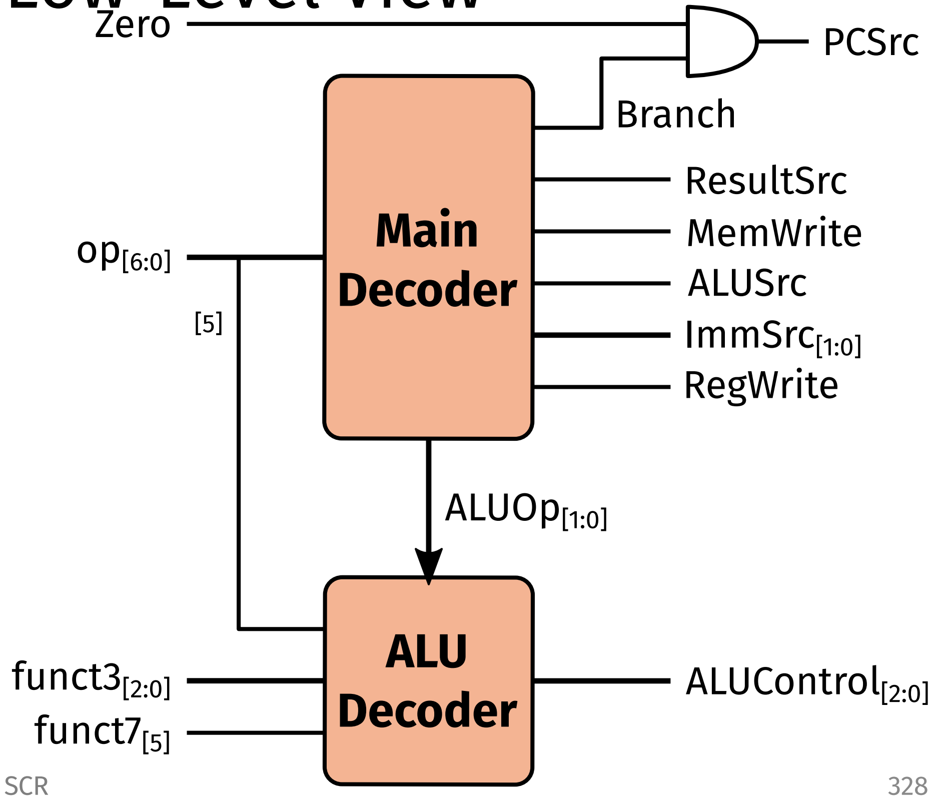
RISC-V Single-Cycle

Single-Cycle – Control Unit

High-Level View



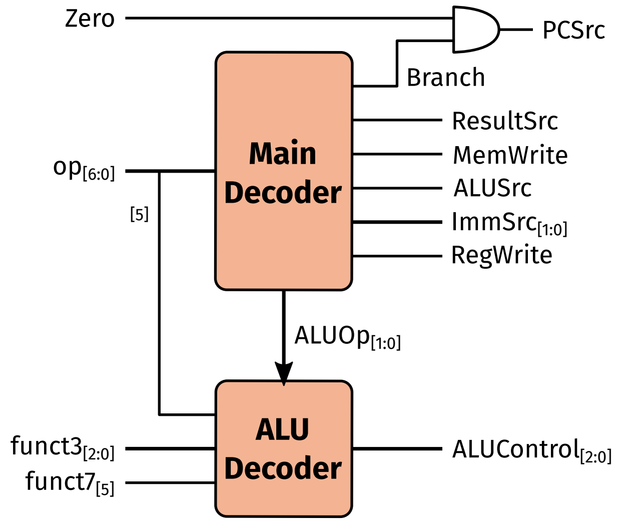
Low-Level View



RISC-V Single-Cycle

Single-Cycle – Main Decoder

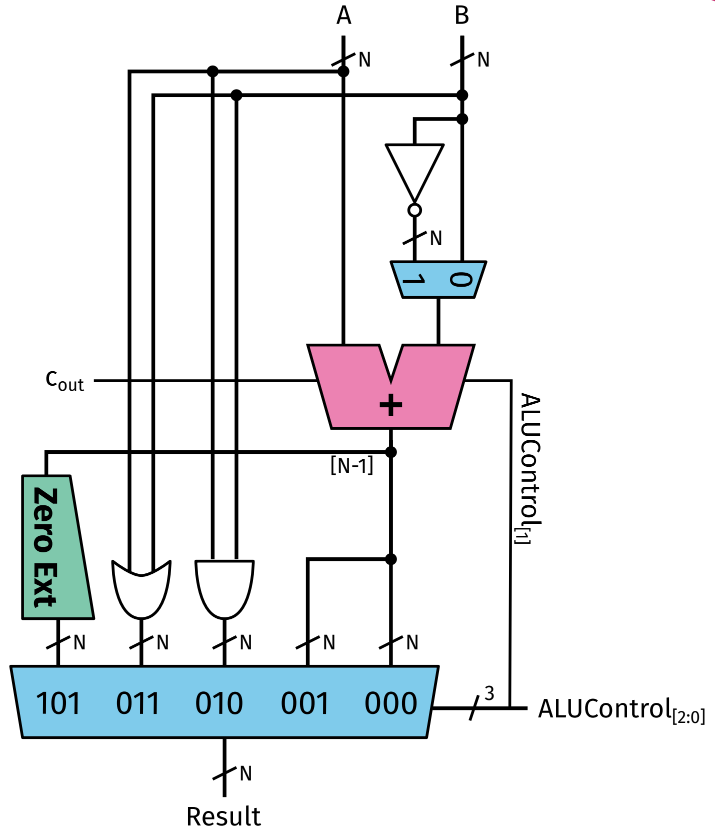
Op	Instr.	RegWrite	ImmSrc	ALUSrc	MemWrite	ResultSrc	Branch	ALUOp
3	lw	1	00	1	0	1	0	00
35	sw	0	01	1	1	–	0	00
51	or	1	--	0	0	0	0	10
99	beq	0	10	0	0	--	1	01



RISC-V Single-Cycle

ALU Implementation

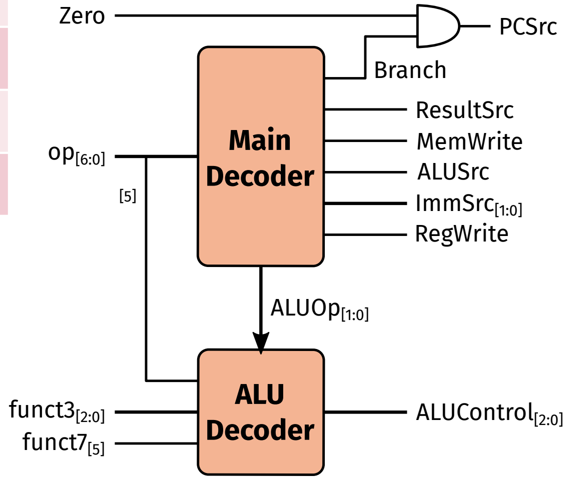
ALUControl[2:0]	Function
000	addition
001	substract
010	and
011	or
101	slt



RISC-V Single-Cycle

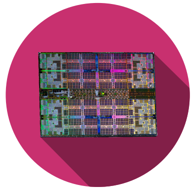
ALU Implementation

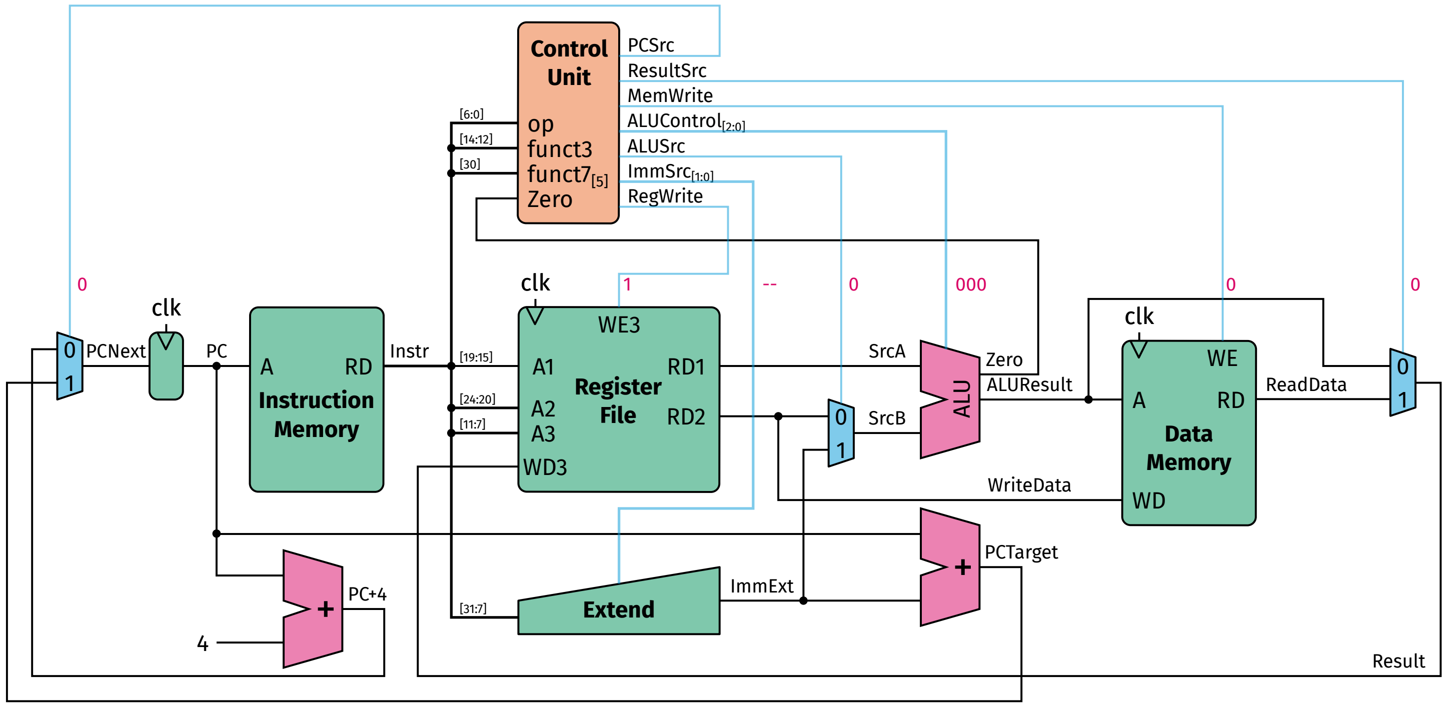
ALUOp	funct3	Op[5], funct7[5]	Instruction	ALUControl[2:0]
00	---	--	lw, sw	000 (add)
01	---	--	beq	001 (subtract)
10	000	00,01,10	add	000 (add)
	000	11	sub	001 (subtract)
	010	--	slt	101 (set less than)
	110	--	or	010 (or)
	111	--	and	011 (and)



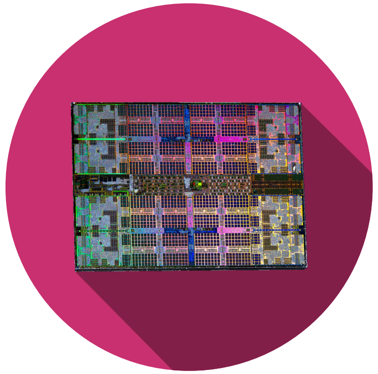
RISC-V Single-Cycle

Single-Cycle Example `and x5, x6 ,x7`





op	Instruction	RegWrite	ImmSrc	ALUSrc	MemWrite	ResultSrc	Branch	ALUOp
51	R-Type	1	--	0	0	0	0	10



Single-Cycle Performance

RISC-V Processor Performance

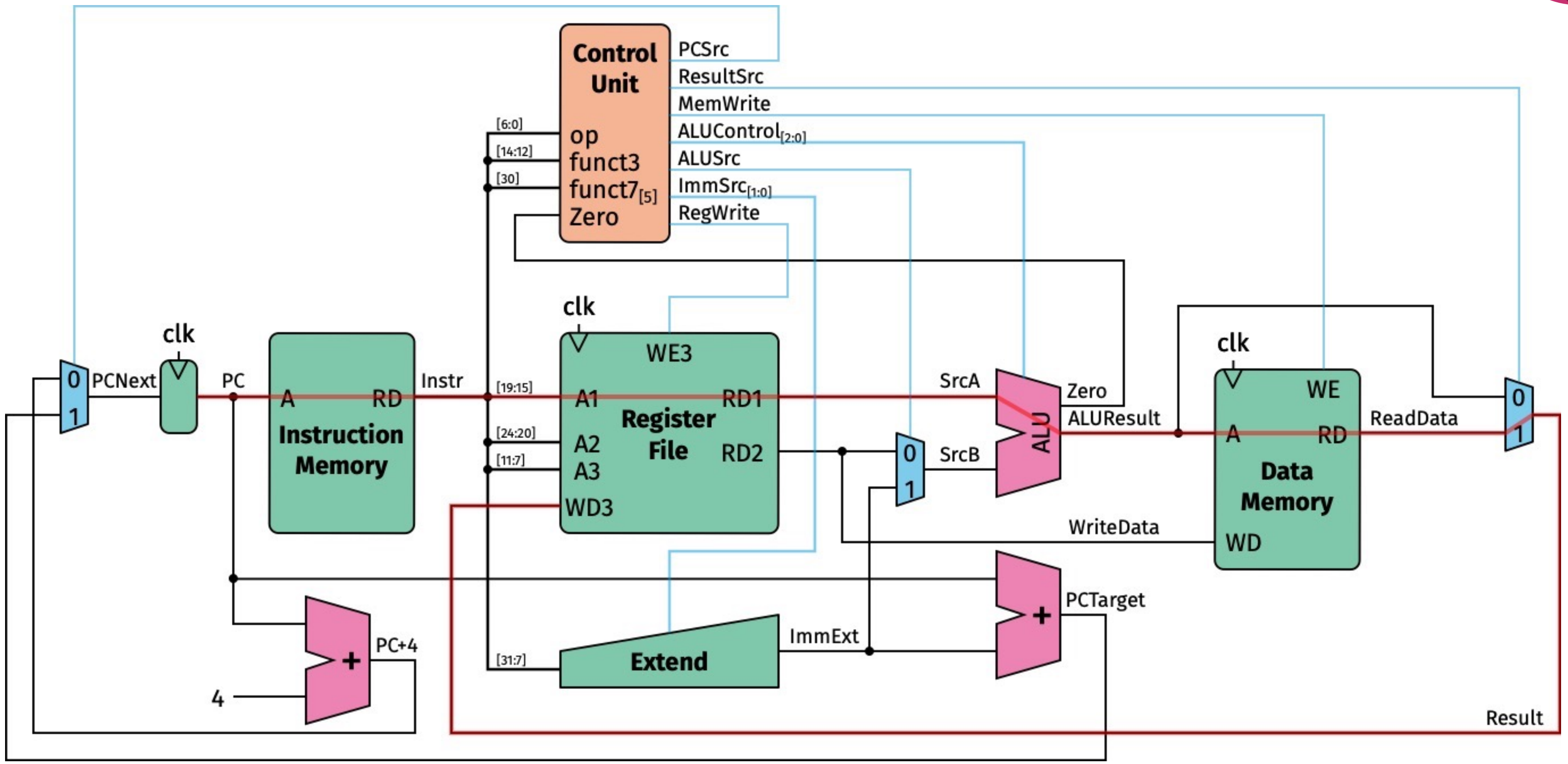
Program Execution Time

$$T = IC * CPI * CT = \frac{IC * CPI}{f}$$

- $T = Execution\ time$
- $IC = N_{instr}$ = # instructions executed (**I**nstruction **C**ount)
- CPI = **C**ycles **P**er **I**nstruction
- $CT = t_{cycle}$ = **C**ycle **T**ime = duration of clock cycle
- f = clock frequency = $\frac{1}{t_{cycle}}$

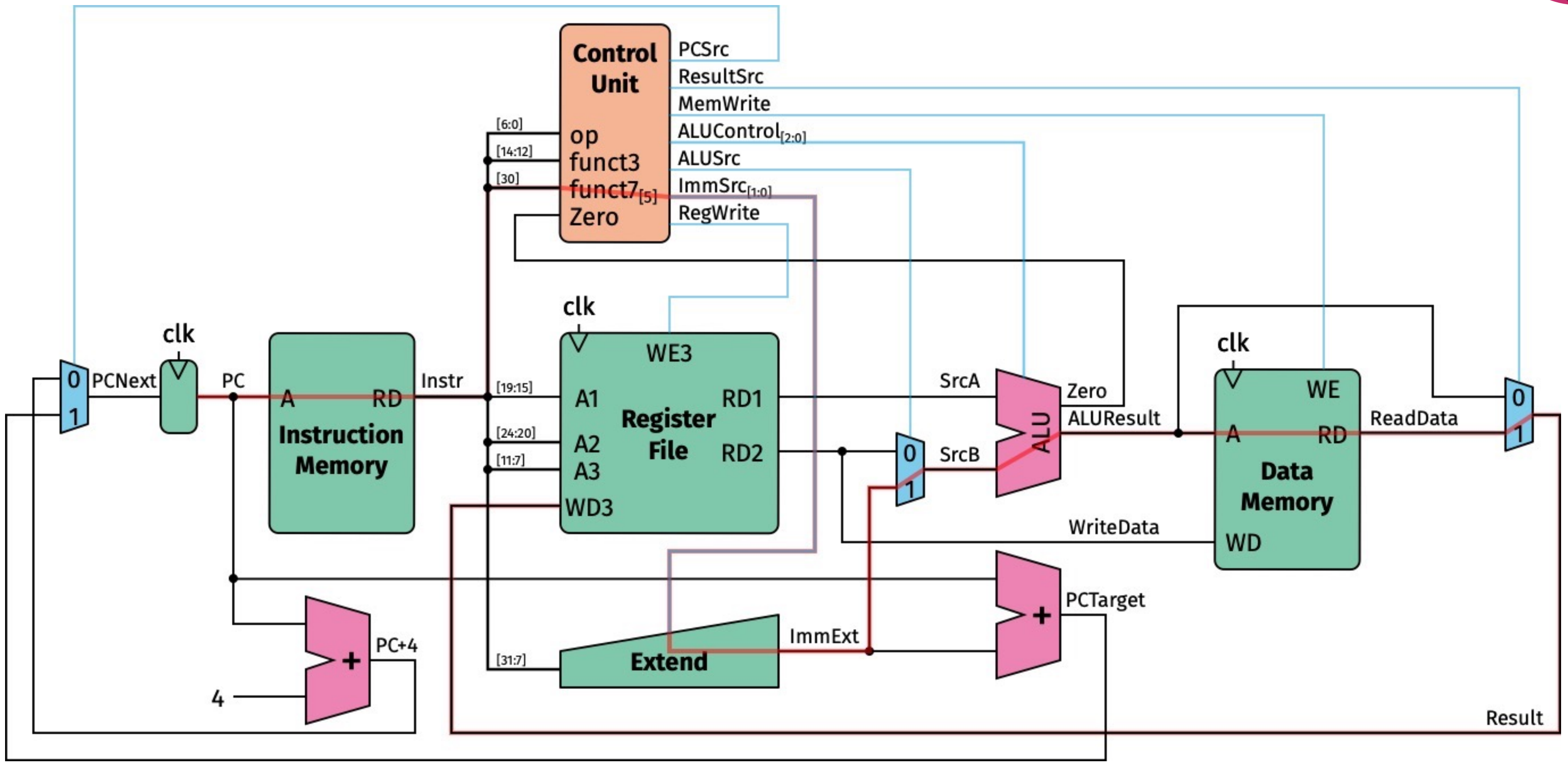
RISC-V Processor Performance

Cycle Time `lw` instruction



RISC-V Processor Performance

Cycle Time `imm` instruction



RISC-V Processor Performance

Cycle Time

Single-Cycle critical path:

- $T_{c\_single} = t_{PC} + t_{INST\_MEM} + \max[t_{RF_{read}}, t_{decode} + t_{ext} + t_{MUX}] + t_{ALU} + t_{DATA\_MEM} + t_{MUX} + t_{RF\_write}$

Typical, limiting path are:

- Memory, ALU, register file

$$T_{c\_single} = t_{PC} + t_{INST\_MEM} + t_{RF_{read}} + t_{ALU} + t_{DATA\_MEM} + t_{MUX} + t_{RF\_write}$$

RISC-V Processor Performance

Cycle Time

Element	Parameter	Delay (ps)
Programcounter read	t_{PC}	40
Register setup	t_{setup}	50
Multiplexer	t_{MUX}	30
AND-OR Gate	t_{AND_OR}	20
ALU	t_{ALU}	120
Decoder (Control Unit)	t_{dec}	25
Extend Unit	t_{ext}	35
Memory read	t_{MEM}	200
Register file read	t_{RF_read}	100
Register file write	t_{FR_write}	60

$$T_{c\_single} = t_{PC} + t_{INST\_MEM} + t_{RF_{read}} + t_{ALU} + t_{DATA\_MEM} + t_{MUX} + t_{RF\_write}$$

RISC-V Processor Performance

Cycle Time

Element	Parameter	Delay (ps)
Programcounter read	t_{PC}	40
Register setup	t_{setup}	50
Multiplexer	t_{MUX}	30
AND-OR Gate	t_{AND_OR}	20
ALU	t_{ALU}	120
Decoder (Control Unit)	t_{dec}	25
Extend Unit	t_{ext}	35
Memory read	t_{MEM}	200
Register file read	t_{RF_read}	100
Register file write	t_{FR_write}	60

$$T_{c\_single} = t_{PC} + t_{INST\_MEM} + t_{RF_{read}} + t_{ALU} + t_{DATA\_MEM} + t_{MUX} + t_{RF\_write}$$

$$T_{c\_single} = 40ps + 200ps + 100ps + 120ps + 200ps + 30ps + 60ps = 750ps$$

RISC-V Processor Performance

Program Execution Time

Calculate the executiontime of a program with 100 billion instructions:

$$T = IC * CPI * CT = \frac{IC * CPI}{f}$$

$$T = 10^{11} * 1 * 750ps = 75s$$

References

[1]
D. A. Patterson and J. L. Hennessy, *Computer Organization and Design - RISC-V Edition*, First Edition. Elsevier, 2017.

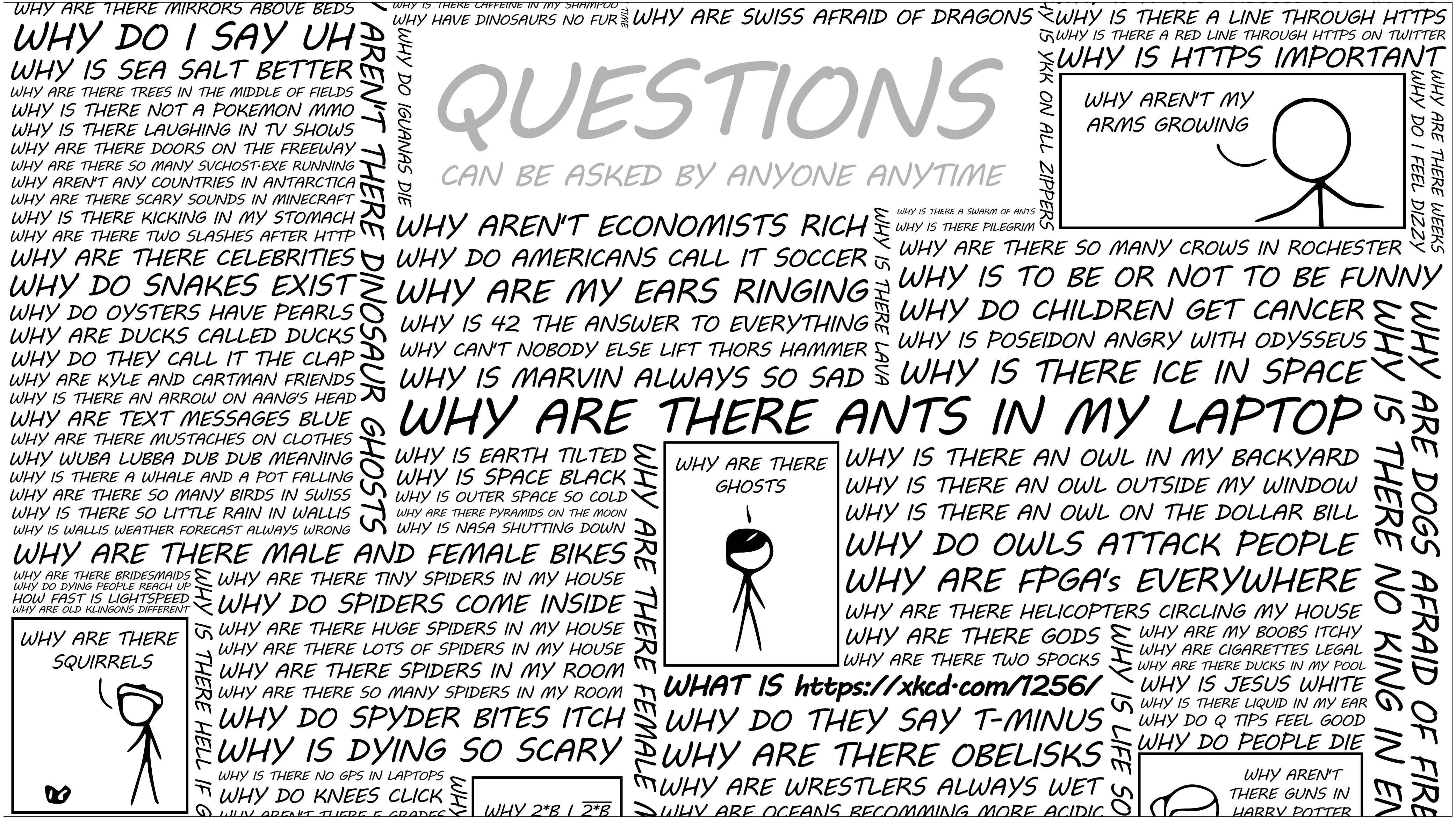
[2]
S. L. Harris and D. M. Harris, “Digital Design and Computer Architecture RISC-V Edition,” in *Digital Design and Computer Architecture*, First Edition., Elsevier, 2022, pp. IBC1–IBC2. doi: 10.1016/B978-0-12-820064-3.00025-8.

[3]
“Instruction cycle,” *Wikipedia*. Apr. 20, 2022. Accessed: May 29, 2022. [Online]. Available: https://en.wikipedia.org/w/index.php?title=Instruction_cycle&oldid=1083738942

[4]
F. Embeddev, “ISA Resources,” *Five EmbedDev*. https://www.five-embeddev.com//riscv-isa-manual/ (accessed Jun. 04, 2022).

[5]
A. Waterman, K. Asanovic, and F. Embeddev, “RISC-V Instruction Set Manual, Volume I: RISC-V User-Level ISA,” *Five EmbedDev*, 2019. https://www.five-embeddev.com//riscv-isa-manual/latest/riscv-spec.html (accessed Jun. 04, 2022).

[6]
F. Embeddev, “RISC-V Quick Reference,” *Five EmbedDev*, 2022. https://www.five-embeddev.com//quickref/tools.html (accessed Jun. 04, 2022).


WHY ARE THERE MIRRORS ABOVE BEDS
WHY DO I SAY UH
WHY IS SEA SALT BETTER
WHY ARE THERE TREES IN THE MIDDLE OF FIELDS
WHY IS THERE NOT A POKEMON MMO
WHY IS THERE LAUGHING IN TV SHOWS
WHY ARE THERE DOORS ON THE FREEWAY
WHY ARE THERE SO MANY SVCHOST.EXE RUNNING
WHY AREN'T ANY COUNTRIES IN ANTARCTICA
WHY ARE THERE SCARY SOUNDS IN MINECRAFT
WHY IS THERE KICKING IN MY STOMACH
WHY ARE THERE TWO SLASHES AFTER HTTP
WHY ARE THERE CELEBRITIES
WHY DO SNAKES EXIST
WHY DO OYSTERS HAVE PEARLS
WHY ARE DUCKS CALLED DUCKS
WHY DO THEY CALL IT THE CLAP
WHY ARE KYLE AND CARTMAN FRIENDS
WHY IS THERE AN ARROW ON AANG'S HEAD
WHY ARE TEXT MESSAGES BLUE
WHY ARE THERE MUSTACHES ON CLOTHES
WHY WUBA LUBBA DUB DUB MEANING
WHY IS THERE A WHALE AND A POT FALLING
WHY ARE THERE SO MANY BIRDS IN SWISS
WHY IS THERE SO LITTLE RAIN IN WALLIS
WHY IS WALLIS WEATHER FORECAST ALWAYS WRONG
WHY AREN'T THERE DINOSAUR GHOSTS
WHY IS THERE CAFFEINE IN MY SHAMPOO
WHY HAVE DINOSAURS NO FUR
TIME
WHY DO IGUANAS DIE
WHY ARE SWISS AFRAID OF DRAGONS
QUESTIONS
CAN BE ASKED BY ANYONE ANYTIME
WHY IS YKK ON ALL ZIPPERS
WHY IS THERE A LINE THROUGH HTTPS
WHY IS THERE A RED LINE THROUGH HTTPS ON TWITTER
WHY IS HTTPS IMPORTANT
WHY AREN'T MY ARMS GROWING
WHY ARE THERE WEEKS
WHY DO I FEEL DIZZY
WHY AREN'T ECONOMISTS RICH
WHY DO AMERICANS CALL IT SOCCER
WHY ARE MY EARS RINGING
WHY IS 42 THE ANSWER TO EVERYTHING
WHY CAN'T NOBODY ELSE LIFT THORS HAMMER
WHY IS MARVIN ALWAYS SO SAD
WHY IS THERE A SWARM OF ANTS
WHY IS THERE PILEGRIM
WHY IS THERE LAVA
WHY ARE THERE SO MANY CROWS IN ROCHESTER
WHY IS TO BE OR NOT TO BE FUNNY
WHY DO CHILDREN GET CANCER
WHY IS POSEIDON ANGRY WITH ODYSSEUS
WHY IS THERE ICE IN SPACE
WHY ARE THERE ANTS IN MY LAPTOP
WHY IS THERE NO KING IN EN
WHY ARE DOGS AFRAID OF FIRE
WHY IS EARTH TILTED
WHY IS SPACE BLACK
WHY IS OUTER SPACE SO COLD
WHY ARE THERE PYRAMIDS ON THE MOON
WHY IS NASA SHUTTING DOWN
WHY ARE THERE FEMALE A
WHY ARE THERE GHOSTS
WHY IS THERE AN OWL IN MY BACKYARD
WHY IS THERE AN OWL OUTSIDE MY WINDOW
WHY IS THERE AN OWL ON THE DOLLAR BILL
WHY DO OWLS ATTACK PEOPLE
WHY ARE FPGA's EVERYWHERE
WHY ARE THERE HELICOPTERS CIRCLING MY HOUSE
WHY ARE THERE GODS
WHY ARE THERE TWO SPOCKS
WHY ARE THERE MALE AND FEMALE BIKES
WHY ARE THERE BRIDESMAIDS
WHY DO DYING PEOPLE REACH UP
HOW FAST IS LIGHTSPEED
WHY ARE OLD KLINGONS DIFFERENT
WHY IS THERE HELL IF G
WHY ARE THERE TINY SPIDERS IN MY HOUSE
WHY DO SPIDERS COME INSIDE
WHY ARE THERE HUGE SPIDERS IN MY HOUSE
WHY ARE THERE LOTS OF SPIDERS IN MY HOUSE
WHY ARE THERE SPIDERS IN MY ROOM
WHY ARE THERE SO MANY SPIDERS IN MY ROOM
WHY DO SPYDER BITES ITCH
WHY IS DYING SO SCARY
WHY IS THERE NO GPS IN LAPTOPS
WHY DO KNEES CLICK
WHY ARE THERE SQUIRRELS
WHY 2*B | $\overline{2*B}$
WHAT IS https://xkcd.com/1256/
WHY DO THEY SAY T-MINUS
WHY ARE THERE OBELISKS
WHY ARE WRESTLERS ALWAYS WET
WHY IS LIFE SO
WHY ARE MY BOOBS ITCHY
WHY ARE CIGARETTES LEGAL
WHY ARE THERE DUCKS IN MY POOL
WHY IS JESUS WHITE
WHY IS THERE LIQUID IN MY EAR
WHY DO Q TIPS FEEL GOOD
WHY DO PEOPLE DIE
WHY AREN'T THERE GUNS IN

Haute Ecole d'Ingénierie
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Silvan Zahno silvan.zahno@hevs.ch