Architecture

Exercises Computer Architecture

1 Architecture

1.1 Stack-Architecture

Evaluate the expression $\frac{a+bc}{a+dc-e}$ using a stack-based processor evaluation stack.

a) Write pseudo code of the calculation.
b) How many direct and indirect memory references are needed in case of an infinite stacksize?
c) How many direct and indirect memory references are needed in case of a stacksize of 2?

arc/stack-01

1.2 Stack-Architecture

Evaluate the expression $\frac{(a+b)^2}{\pi} * (a + b + c)$ using a stack-based processor evaluation stack.

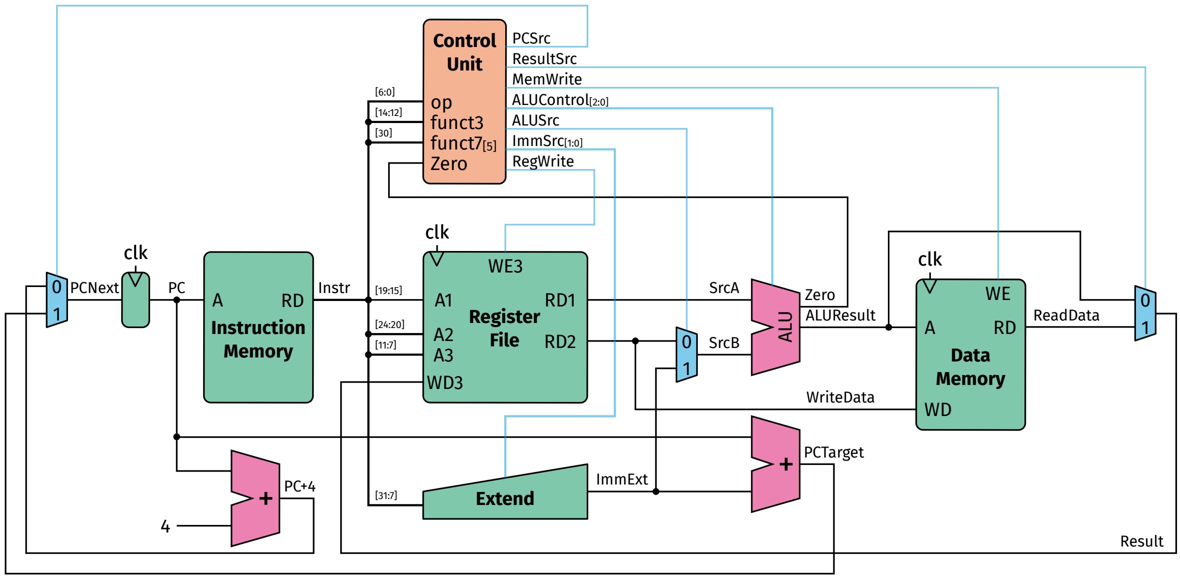
a) Write pseudo code of the calculation.
b) How many direct and indirect memory references are needed in case of a stacksize of 4?
c) How many direct and indirect memory references are needed in case of a stacksize of 3?
d) How many direct and indirect memory references are needed in case of a stacksize of 2?

arc/stack-02

2 Single-Cycle RISC-V

2.1 Single-Cycle Processor Operation

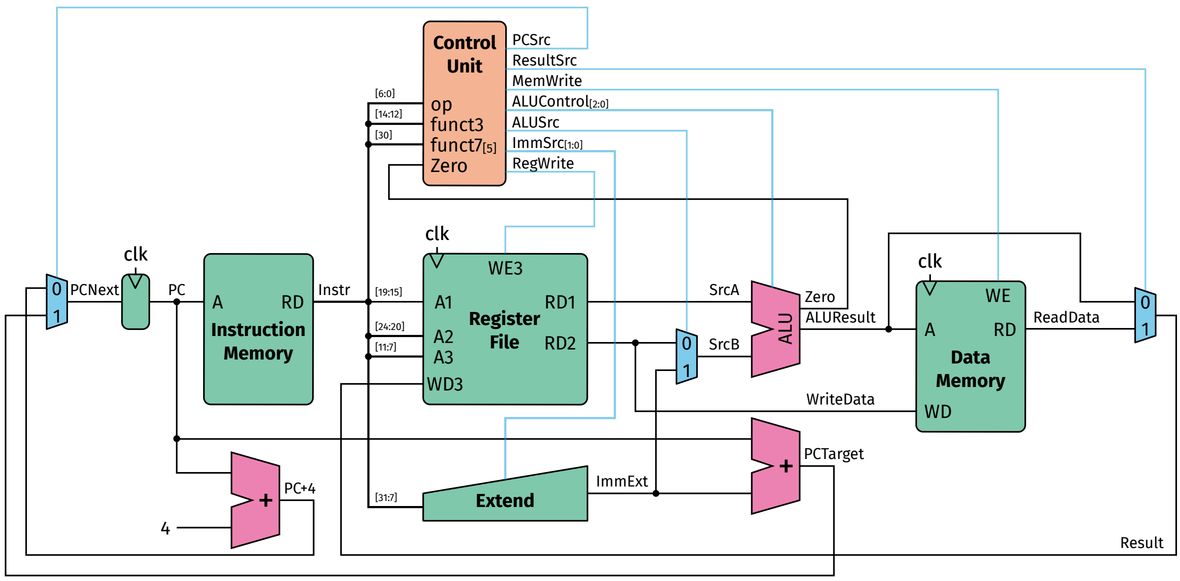
Determine the values of the control signals and the portions of the datapath that are used when executing an `and` instruction. Draw directly on the image the inner workings of the processor.



arc/scr-01

2.2 Extend Single Cycle with instruction `jal`

Show how to change the given RISC-V single-cycle processor to support the jump and link `jal` instruction. `jal` writes **`PC2+4`** to **`rd`** and changes the PC to the jump target address **`PC+imm`**.



arc/scr-02

2.3 Single Cycle Processor Performance

A single cycle processor build with a 7-nm CMOS manufacturing process has the following timing characteristics.

Element	Parameter	Delay(ps)
Register clk-to-Q	t_{pcq}	40
Register Setup	t_{setup}	50
Multiplexer	t_{mux}	30
AND-OR Gate	$t_{\text{AND\_OR}}$	20
ALU	t_{ALU}	120
Decoder (Control Unit)	t_{dec}	25
Extend Unit	t_{ext}	35
Memory Read	t_{mem}	200
Register File Read	t_{RFread}	100
Register File Setup	t_{RFSetup}	60

The program for the SPECINT2000 benchmark contains 100 billion instructions.

Calculate the execution time of the benchmark for this Single-Cycle Processor.

arc/scr-03

3 Multi-Cycle RISC-V

3.1 Multi Cycle Processor Performance

The program for the SPECINT2000 benchmark consists of approximately 25% loads, 10% stores, 11% branches, 2% jumps, and 52% R- or I-Type ALU Instructions.

Determine the average CPI for this benchmark for our developed Multi-Cycle Processor.

arc/mcr-01

3.2 Multi-Cycle Processor Performance

A multi cycle processor build with a 7-nm CMOS manufacturing process has the following timing characteristics.

Element	Parameter	Delay(ps)
Register clk-to-Q	t_{pc}	40
Register Setup	t_{setup}	50
Multiplexer	t_{mux}	30
AND-OR Gate	t_{AND_OR}	20
ALU	t_{ALU}	120
Decoder (Control Unit)	t_{dec}	25
Extend Unit	t_{ext}	35
Memory Read	t_{mem}	200
Register File Read	t_{RFread}	100
Register File Setup	$t_{RFSetup}$	60

The program for the SPECINT2000 benchmark contains 100 billion instructions. Use the CPI_{avg} from the previous task.

Calculate the execution time of the benchmark for this multi-cycle Processor.

arc/mcr-02