



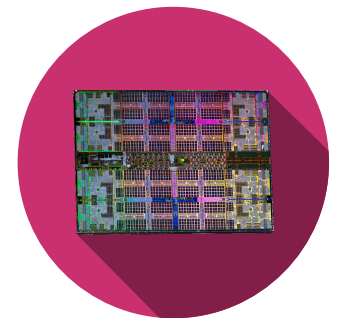
Computer Architecture

Micro-Architecture

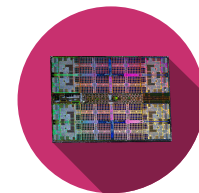
Arc

Information and Communication Systems program

Silvan Zahno silvan.zahno@hevs.ch

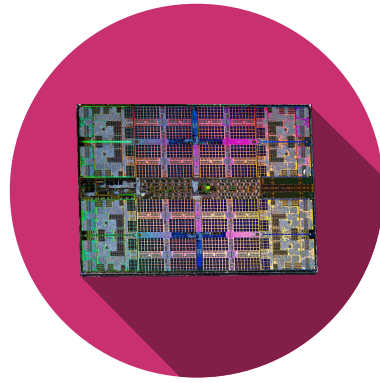


Recapitulation: CPU Performance Equation



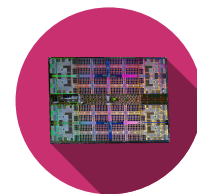
$$T = IC * CPI * CT = \frac{IC * CPI}{f}$$

- T = *Execution time*
- $IC = N_{instr}$ = # instructions executed (**I**nstruction **C**ount)
- CPI = **C**ycles **P**er **I**nstruction
- $CT = t_{cycle}$ = **C**ycle **T**ime = duration of clock cycle
- f = clock frequency = $\frac{1}{t_{cycle}}$



Architectures vs. Microarchitectures

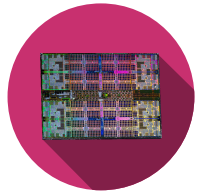
Architecture vs. Microarchitecture



- “Architecture”/Instruction Set Architecture:
 - Programmer visible state (Memory & Register) • Operations (Instructions and how they work)
 - Execution Semantics (interrupts)
 - Input/Output
 - Data Types/Sizes
- Microarchitecture/Organization:
 - Tradeoffs on how to implement ISA for some metric (Speed, Energy, Cost)
 - Examples: Pipeline depth, number of pipelines, cache size, silicon area, peak power, execution ordering, bus widths, ALU widths

Architecture vs. Microarchitecture

Same Architecture / Different Microarchitecture



AMD Phenom X4

- x86 Instruction Set
- Quad Core
- 125W
- Decode 3 Instructions/Cycle/Core
- 64KB L1 I Cache, 64KB L1 D Cache
- 512KB L2 Cache
- Out-of-order
- 2.6GHz

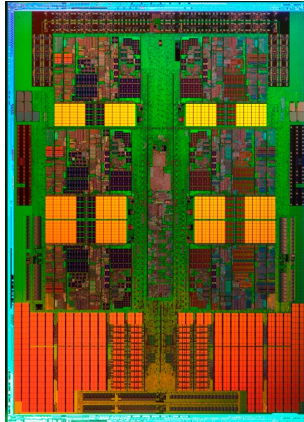


Image Credit: AMD CAR Arc

Intel Atom

- x86 Instruction Set
- Single Core
- 2W
- Decode 2 Instructions/Cycle/Core
- 32KB L1 I Cache, 24KB L1 D Cache
- 512KB L2 Cache
- In-order
- 1.6GHz

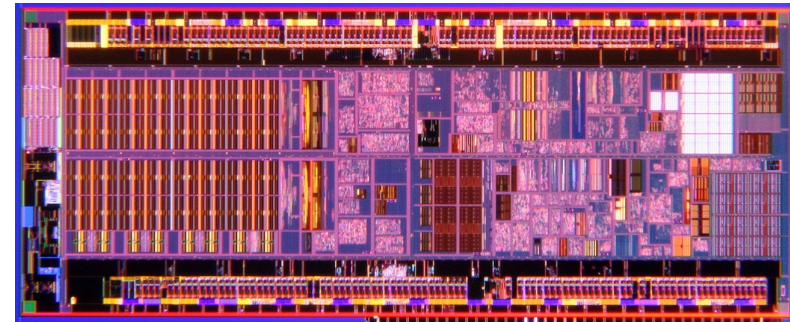
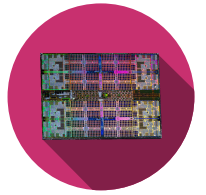


Image Credit: Intel 284

Architecture vs. Microarchitecture

Different Architecture / Different Microarchitecture



AMD Phenom X4

- X86 Instruction Set
- Quad Core
- 125W
- Decode 3 Instructions/Cycle/Core
- 64KB L1 I Cache, 64KB L1 D Cache
- 512KB L2 Cache
- Out-of-order
- 2.6GHz

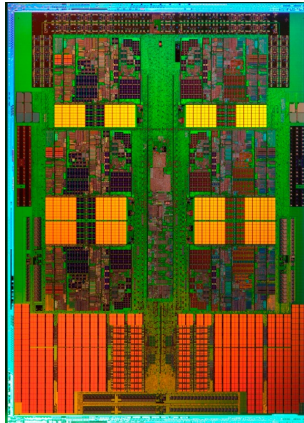


Image Credit: AMD CAR Arc

IBM POWER7

- Power Instruction Set
- Eight Core
- 200W
- Decode 6 Instructions/Cycle/Core
- 32KB L1 I Cache, 32KB L1 D Cache
- 256KB L2 Cache
- Out-of-order
- 4.25GHz

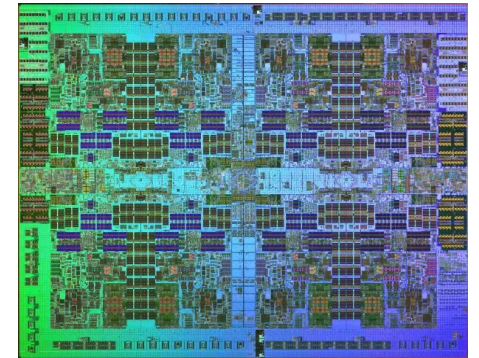
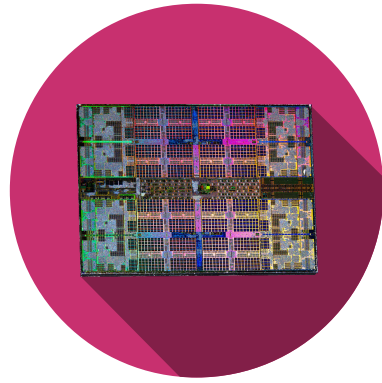


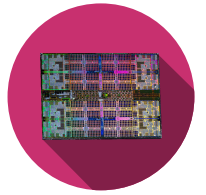
Image Credit: IBM 285



Machine Models

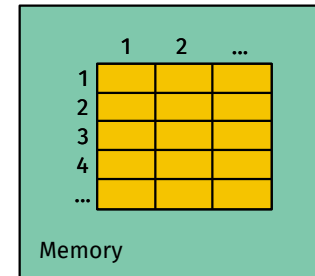
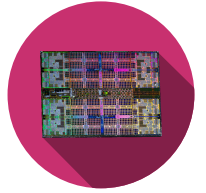
Machine Models

Elements



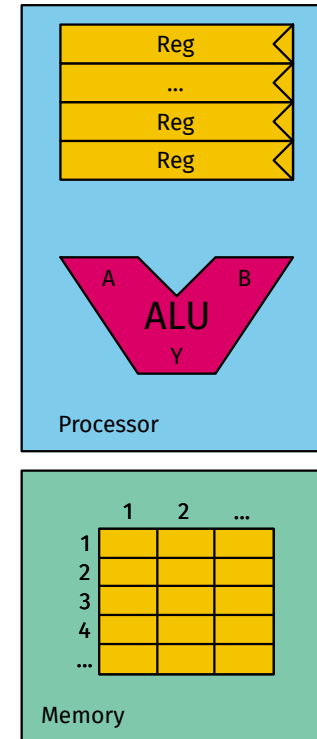
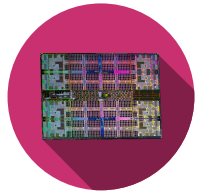
Machine Models

Elements



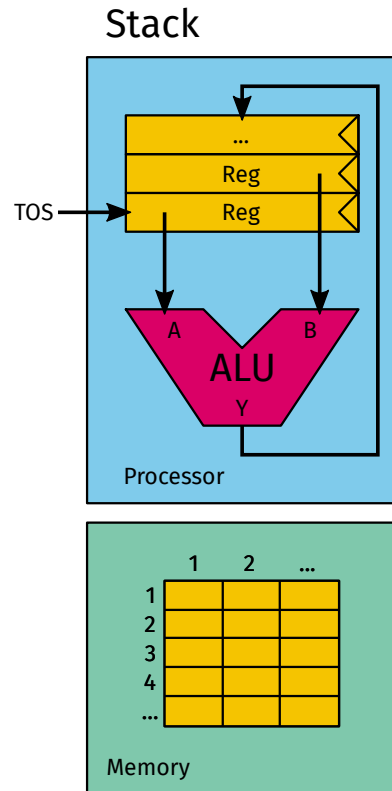
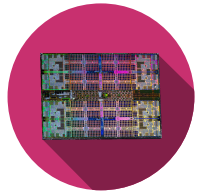
Machine Models

Elements



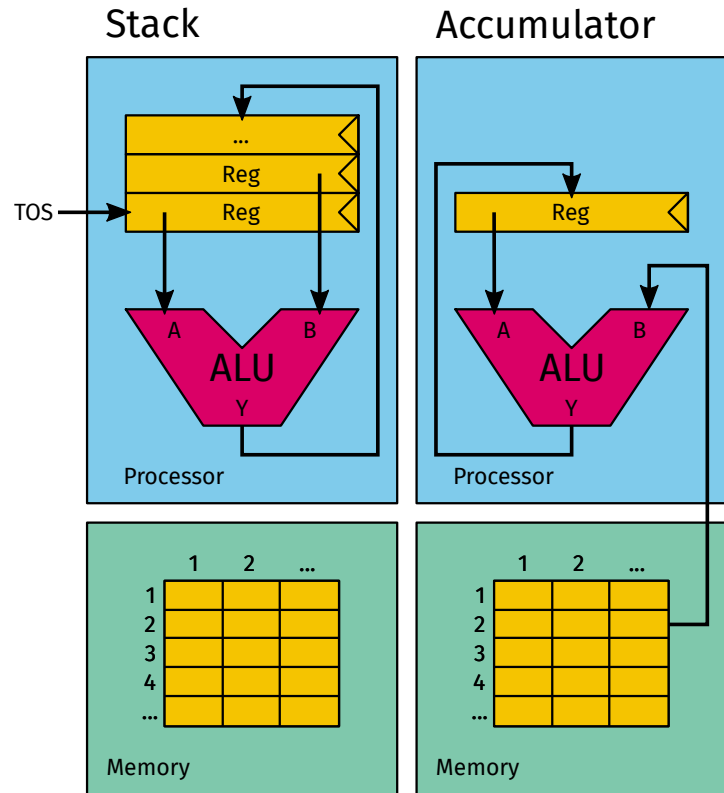
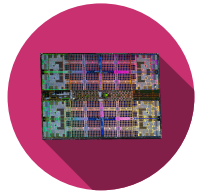
Machine Models

Elements



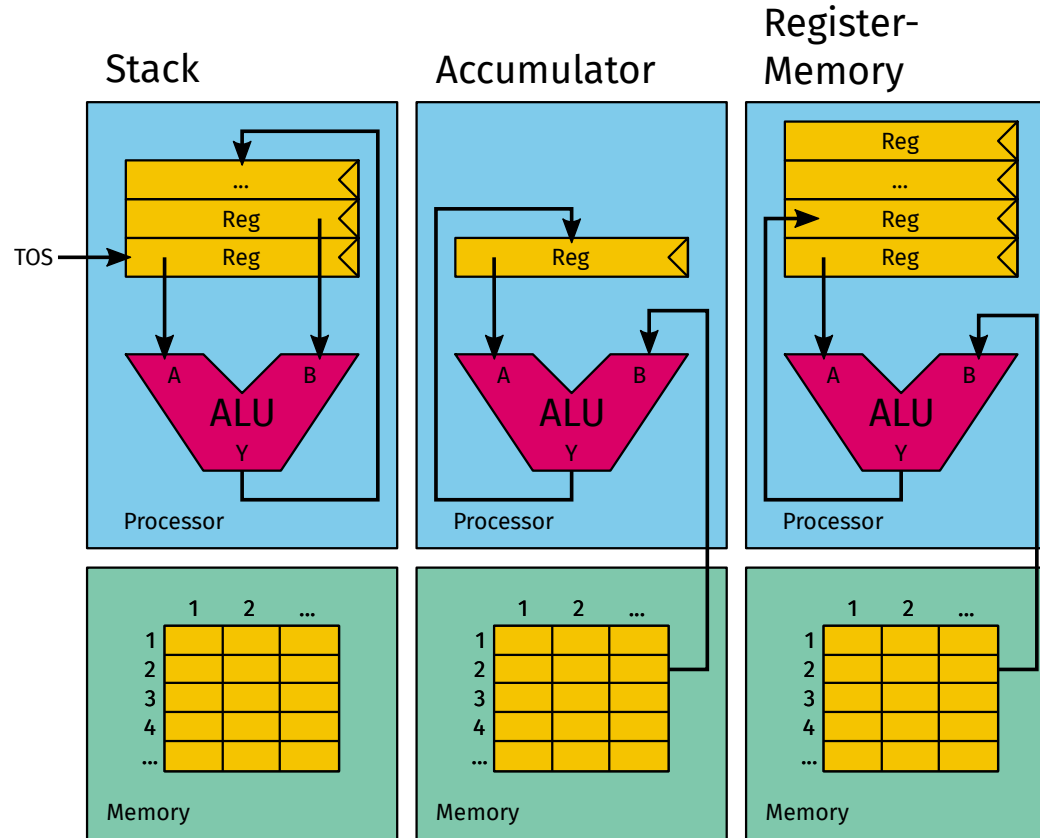
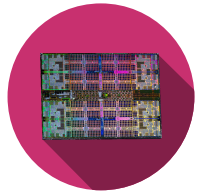
Machine Models

Elements



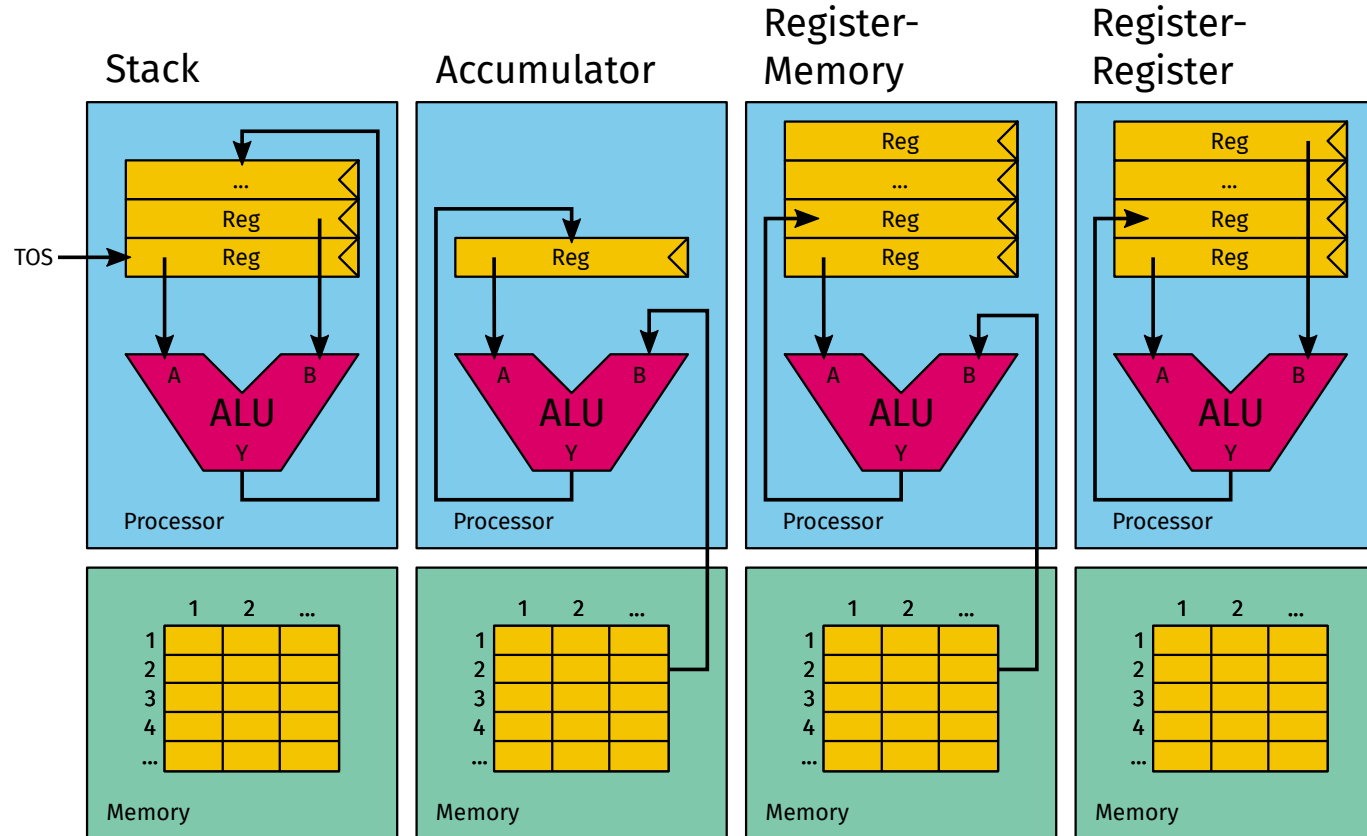
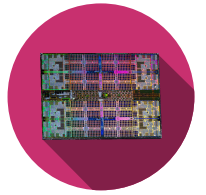
Machine Models

Elements



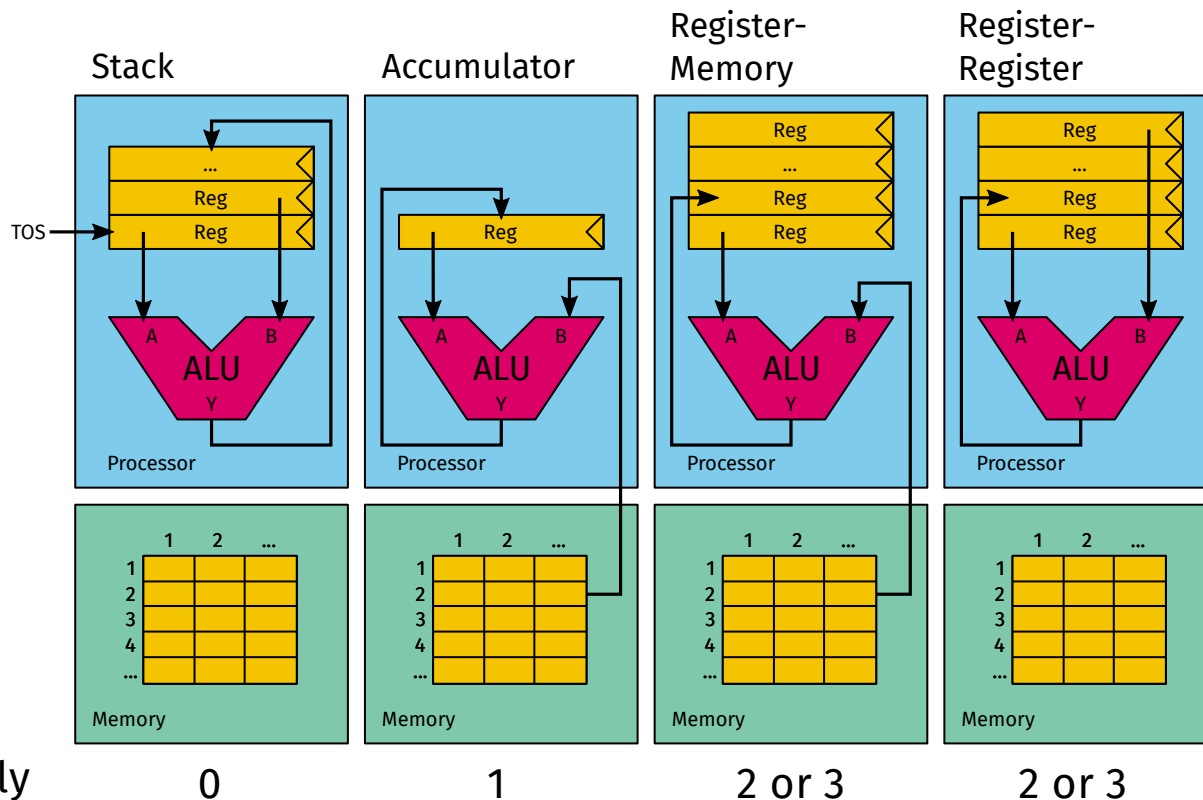
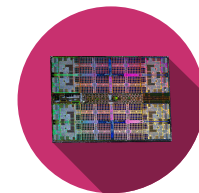
Machine Models

Elements



Machine Models

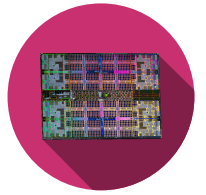
Elements



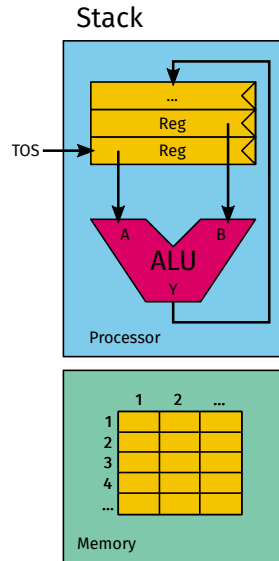
Number Explicitly
Named Operands:

Machine Models

Example Stack machine model

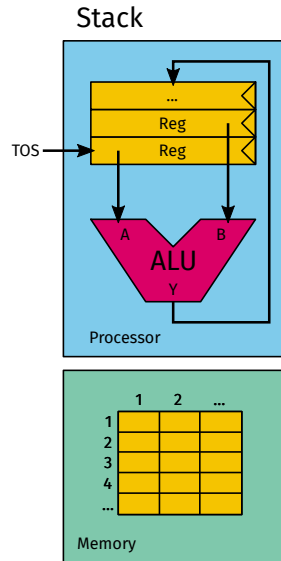
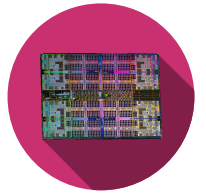


$$(a+b*c)/(a+d*c-e)$$



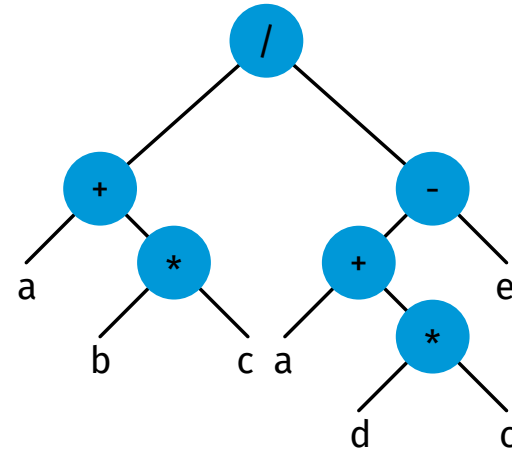
Machine Models

Example Stack machine model



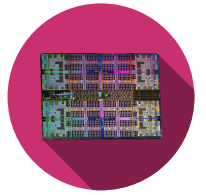
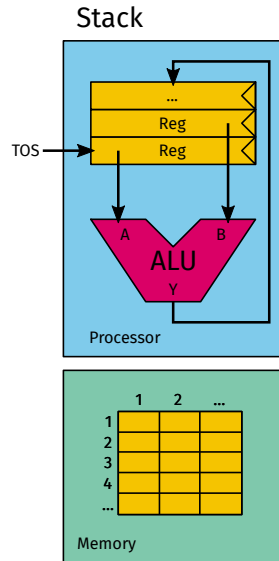
$(a+b*c)/(a+d*c-e)$

Parsetree



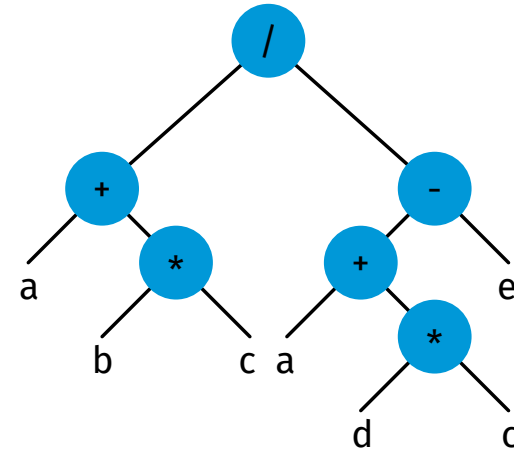
Machine Models

Example Stack machine model



$(a+b*c)/(a+d*c-e)$

Parsetree

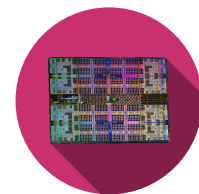


Reverse stack

abc*+adc*+e-/

Machine Models

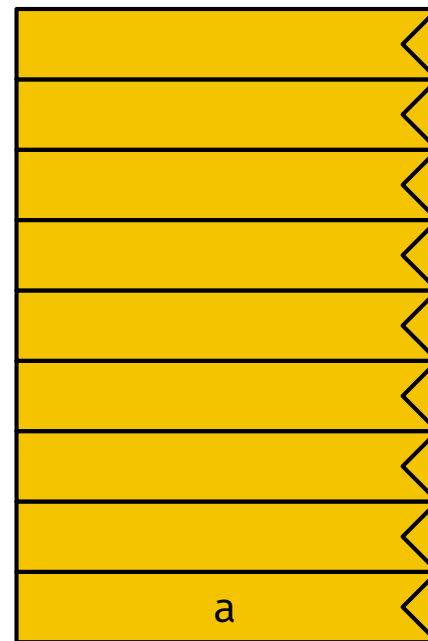
Example Stack machine model



Reverse stack

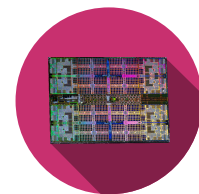
abc**adc**e- /

Program	stack	memory refs
push a	r0	a
push b	r0 r1	b
push c	r0 r1 r2	c
*	r0 r1	
+	r0	
push a	r0 r1	a
push d	r0 r1 r2	d
push c	r0 r1 r2 r3	c
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	e
-	r0 r1	
/	r0	



Machine Models

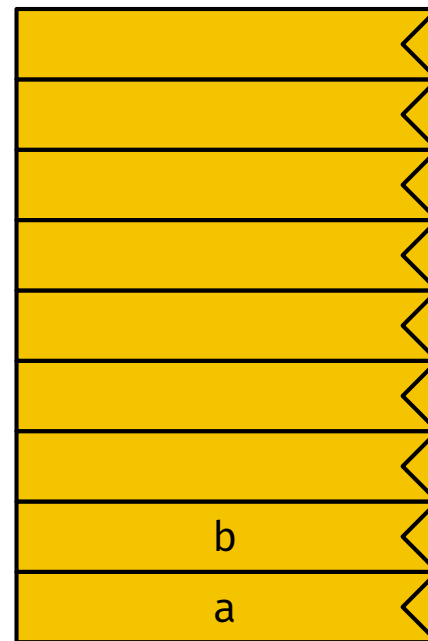
Example Stack machine model



Reverse stack

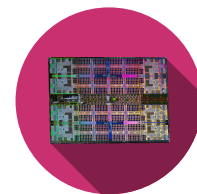
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push b	r0 r1	b
push c	r0 r1 r2	c
*	r0 r1	
+	r0	
push a	r0 r1	a
push d	r0 r1 r2	d
push c	r0 r1 r2 r3	c
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	e
-	r0 r1	
/	r0	



Machine Models

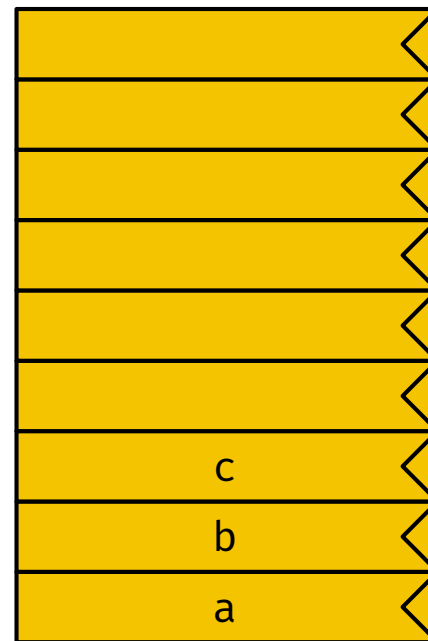
Example Stack machine model



Reverse stack

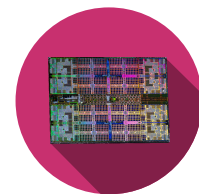
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push c	r0 r1 r2 r3	c
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	e
-	r0 r1	
/	r0	



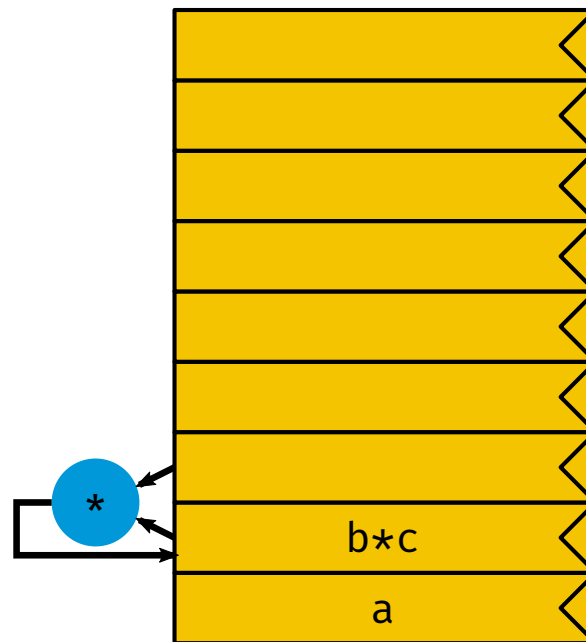
Machine Models

Example Stack machine model



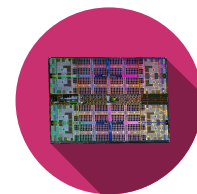
Reverse stack
abc**adc**e- /

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push c	r0 r1 r2	c
*	r0 r1	
+	r0	
push a	r0 r1	a
push d	r0 r1 r2	d
push c	r0 r1 r2 r3	c
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	e
-	r0 r1	
/	r0	



Machine Models

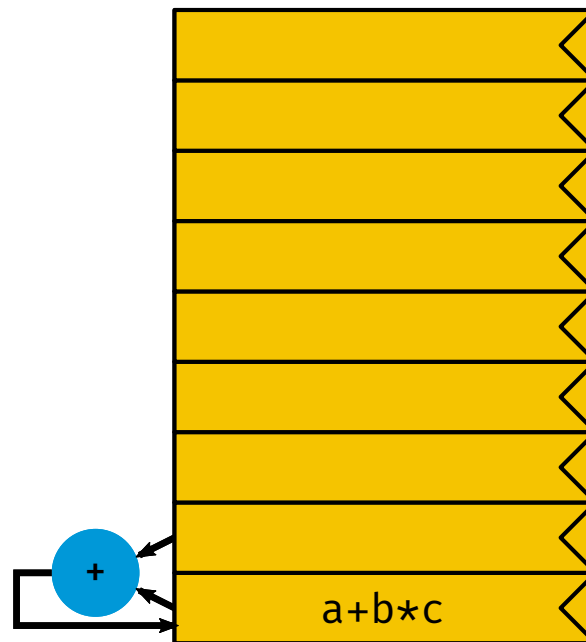
Example Stack machine model



Reverse stack

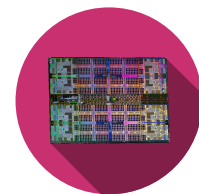
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push a	r0 r1	a
push d	r0 r1 r2	d
push c	r0 r1 r2 r3	c
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	e
-	r0 r1	
/	r0	



Machine Models

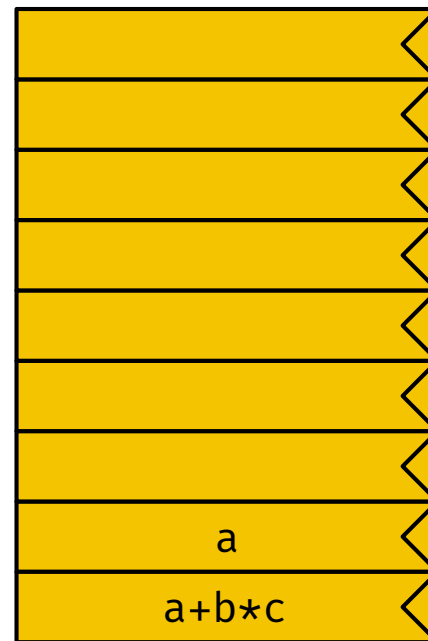
Example Stack machine model



Reverse stack

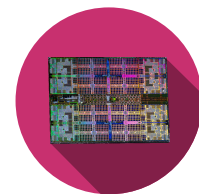
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+	r0	
push a	r0 r1	a
push d	r0 r1 r2	d
push c	r0 r1 r2 r3	c
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	e
-	r0 r1	
/	r0	



Machine Models

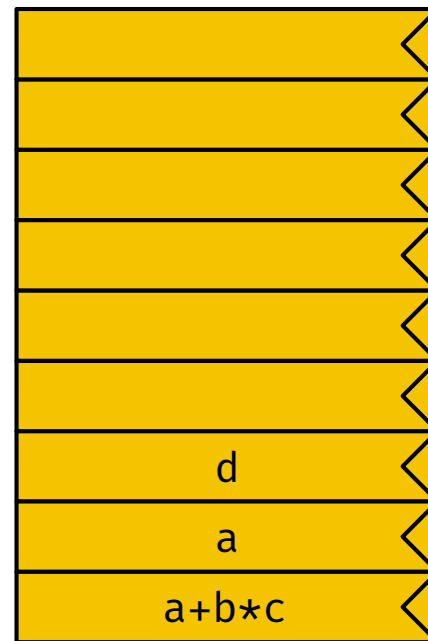
Example Stack machine model



Reverse stack

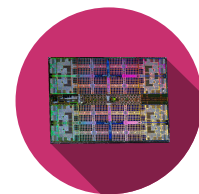
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*	r0 r1	
+	r0	
push a	r0 r1	a
push d	r0 r1 r2	d
push c	r0 r1 r2 r3	c
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	e
-	r0 r1	
/	r0	



Machine Models

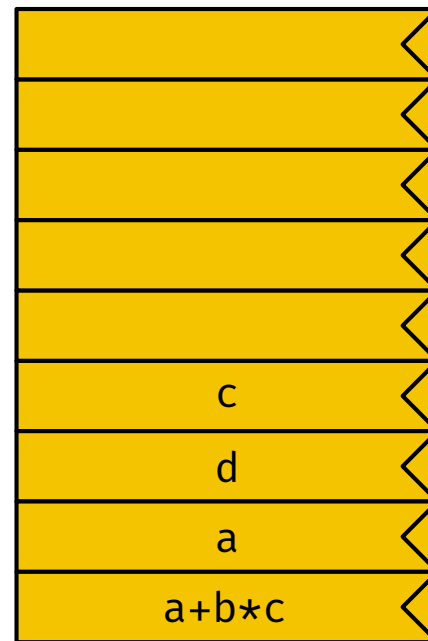
Example Stack machine model



Reverse stack

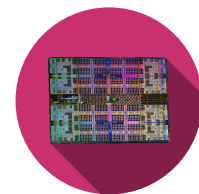
abc*+adc*+e-/

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push b	r0 r1	b
push c	r0 r1 r2	c
*	r0 r1	
+	r0	
push a	r0 r1	a
push d	r0 r1 r2	d
push c	r0 r1 r2 r3	c
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	e
-	r0 r1	
/	r0	



Machine Models

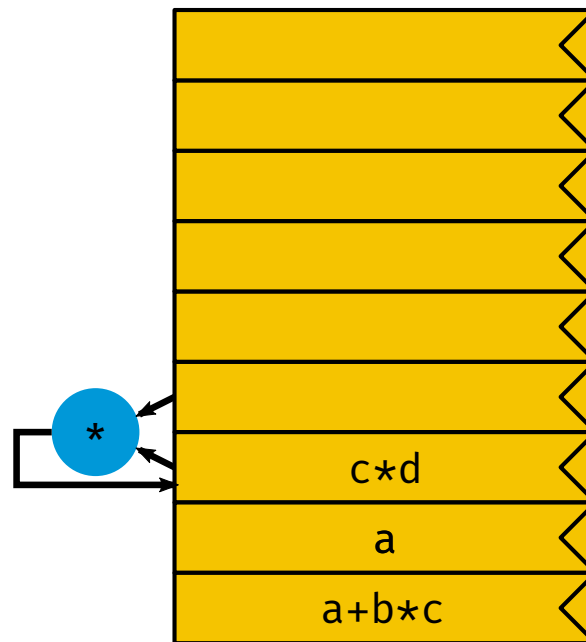
Example Stack machine model



Reverse stack

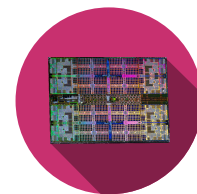
abc**adc**e- /

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push b	r0 r1	b
push c	r0 r1 r2	c
*	r0 r1	
+	r0	
push a	r0 r1	a
push d	r0 r1 r2	d
push c	r0 r1 r2 r3	c
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	e
-	r0 r1	
/	r0	



Machine Models

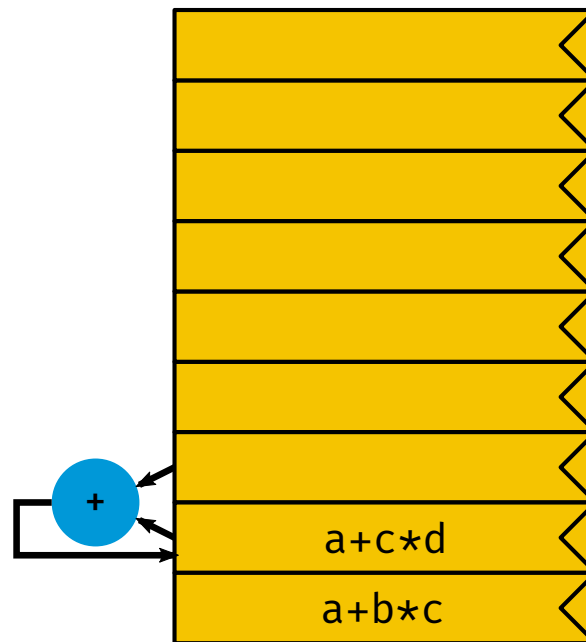
Example Stack machine model



Reverse stack

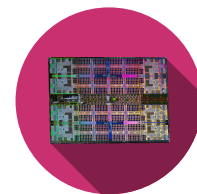
abc**adc**e- /

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push b	r0 r1	b
push c	r0 r1 r2	c
*	r0 r1	
+	r0	
push a	r0 r1	a
push d	r0 r1 r2	d
push c	r0 r1 r2 r3	c
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	e
-	r0 r1	
/	r0	



Machine Models

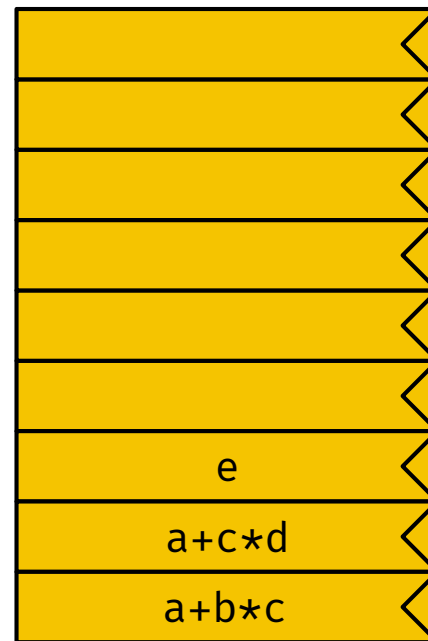
Example Stack machine model



Reverse stack

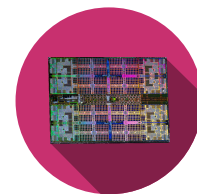
abc**adc**e- /

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push a	r0	a
push b	r0 r1	b
push c	r0 r1 r2	c
*	r0 r1	
+	r0	
push a	r0 r1	a
push d	r0 r1 r2	d
push c	r0 r1 r2 r3	c
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	e
-	r0 r1	
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Machine Models

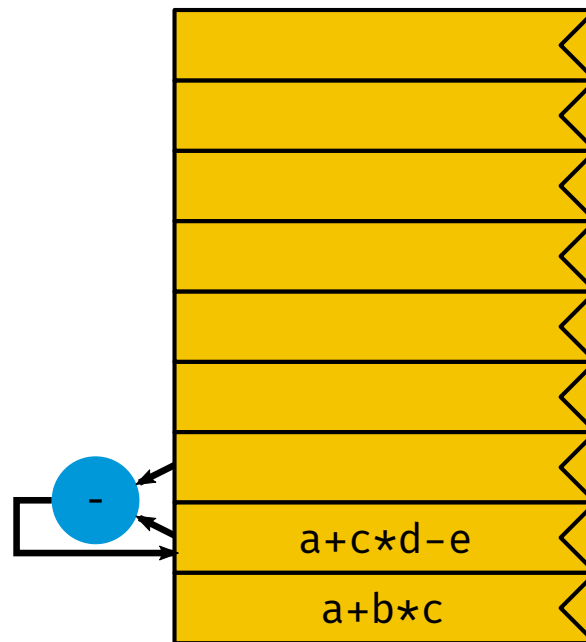
Example Stack machine model



Reverse stack

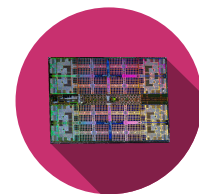
abc**adc**e-/-

Program	stack	memory refs
push a	r0	a
push b	r0 r1	b
push c	r0 r1 r2	c
*	r0 r1	
+	r0	
push a	r0 r1	a
push d	r0 r1 r2	d
push c	r0 r1 r2 r3	c
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	e
-	r0 r1	
/	r0	



Machine Models

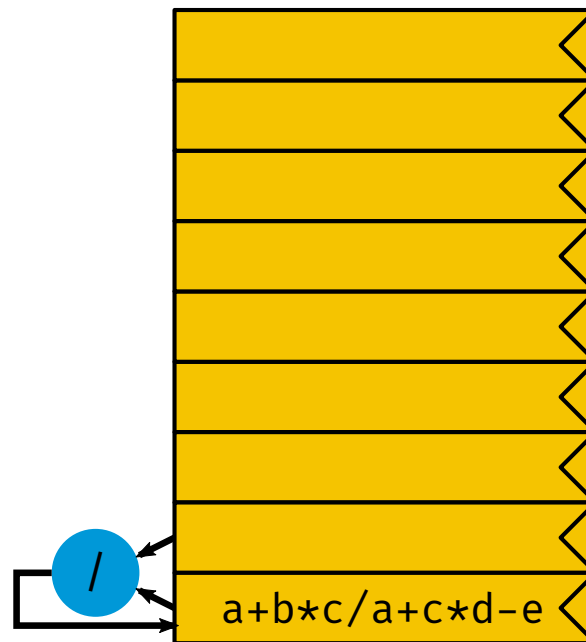
Example Stack machine model



Reverse stack

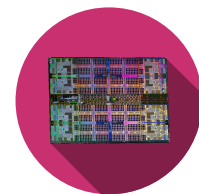
abc**adc**e- /

Program	stack	memory refs
push a	r0	a
push b	r0 r1	b
push c	r0 r1 r2	c
*	r0 r1	
+	r0	
push a	r0 r1	a
push d	r0 r1 r2	d
push c	r0 r1 r2 r3	c
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	e
-	r0 r1	
/	r0	



Machine Models

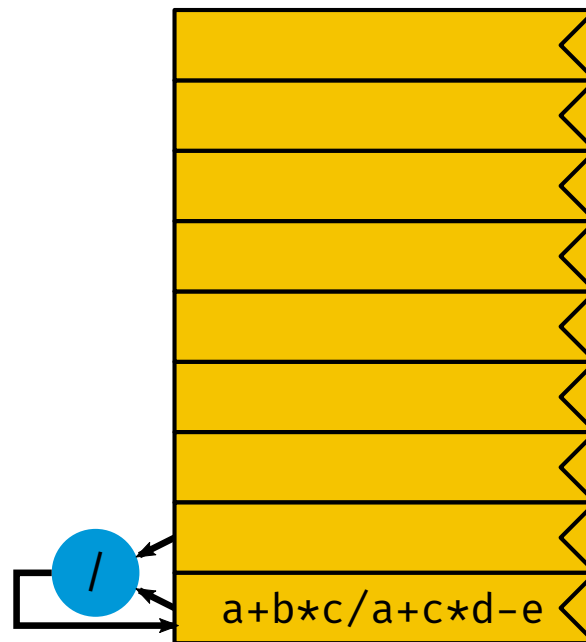
Example Stack machine model



Reverse stack

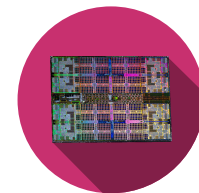
abc**adc**e- /

Program	stack	memory refs
push a	r0	a
push b	r0 r1	b
push c	r0 r1 r2	c
*	r0 r1	
+	r0	
push a	r0 r1	a
push d	r0 r1 r2	d
push c	r0 r1 r2 r3	c
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	e
-	r0 r1	
/	r0	



Machine Models

Example Stack machine model



Reverse stack

abc**adc**e- /

Program	stack	memory refs
push a	r0	a
push b	r0 r1	b
push c	r0 r1 r2	c
*	r0 r1	
+	r0	
push a	r0 r1	a
push d	r0 r1 r2	d
push c	r0 r1 r2 r3	c
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	e
-	r0 r1	
/	r0	

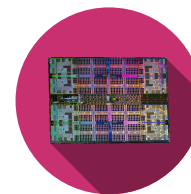
Not efficient use of registers

a & c are fetched twice

Machine Models

Exercise Stack machine model

Evaluate the stack in case of a stacksize of 2. How many memory references are there?

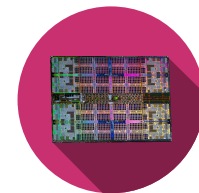


Reverse stack
abc*+adc*+e-/

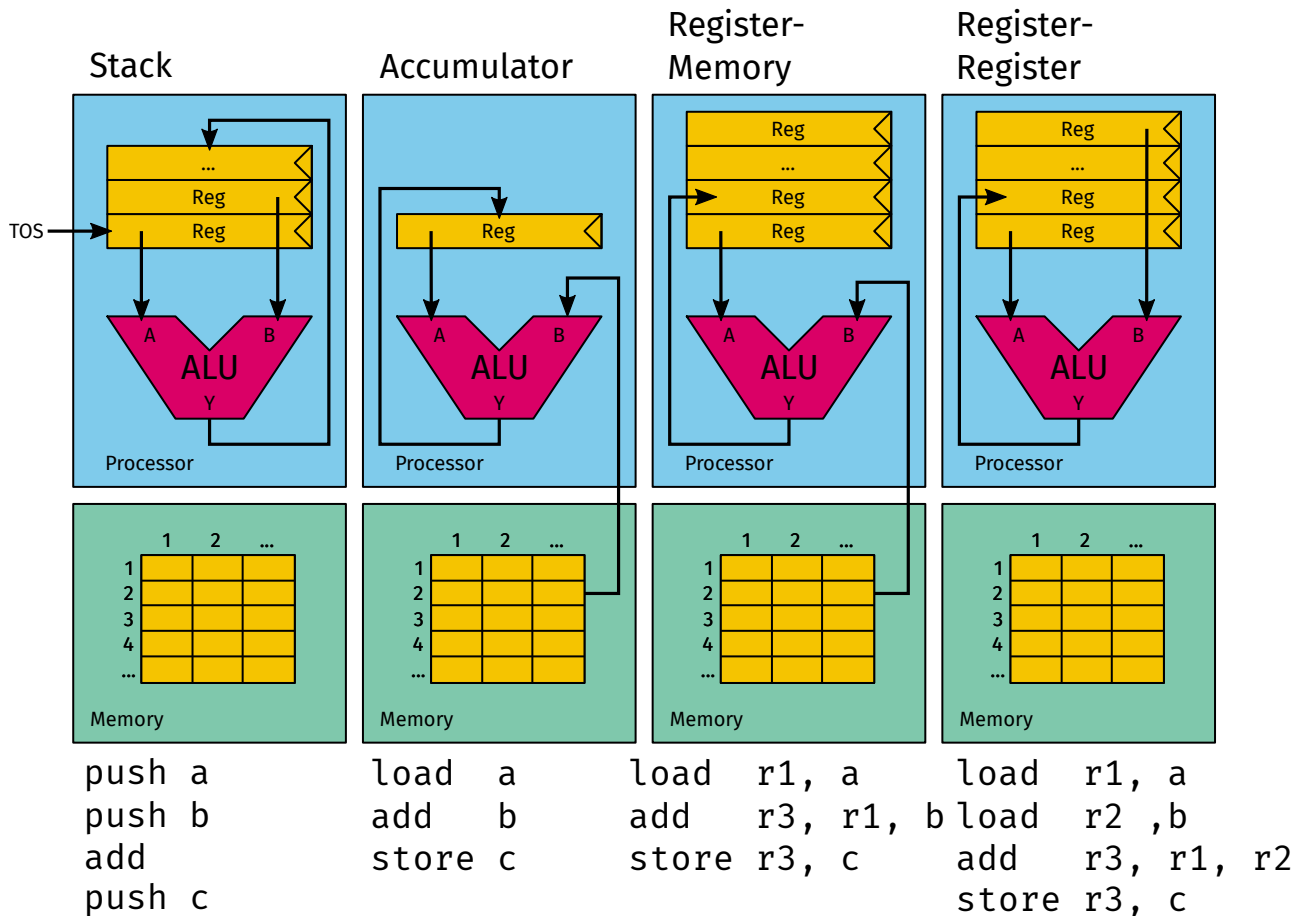
Program	stack (size = 2)	memory refs
push a	r0	
push b	r0 r1	
push c	r0 r1 r2	
*	r0 r1	
+	r0	
push a	r0 r1	
push d	r0 r1 r2	
push c	r0 r1 r2 r3	
*	r0 r1 r2	
+	r0 r1	
push e	r0 r1 r2	
-	r0 r1	
/	r0	

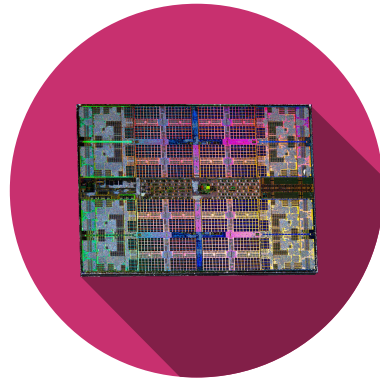
Machine Models

Summary



$c = a + b$





Data Architectures

Data Architectures

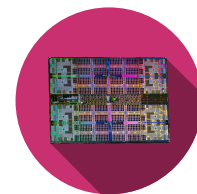
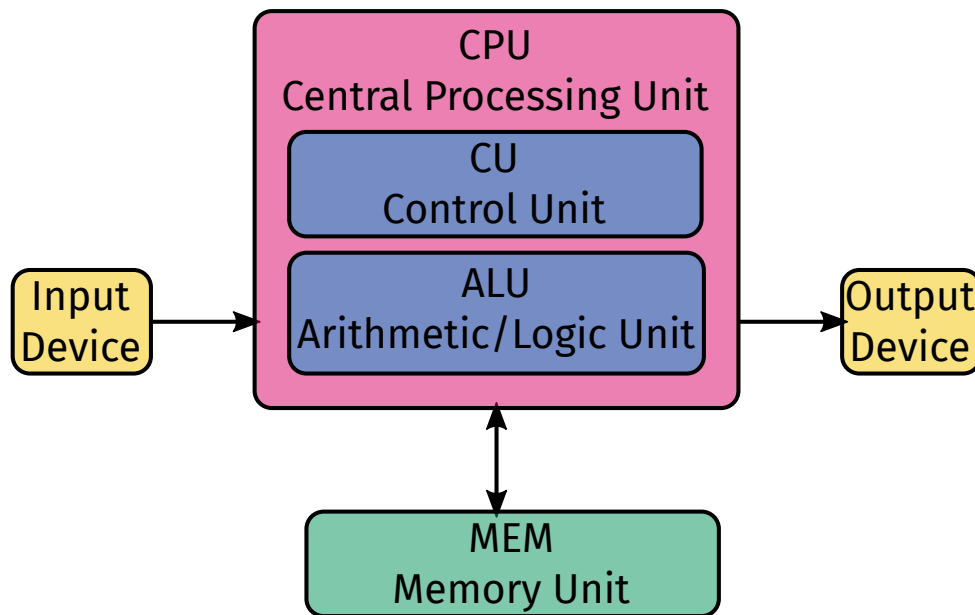
Von Neumann

- Same memory holds data and instructions
- A single set of address/data busses between CPU and memory

Advantages – Cheaper, less logic, less power consumption

Disadvantages – databus speed slower than harvard, bottleneck problems

Examples – All Intel x86, ARM7



Data Architectures

Von Neumann 4-step instruction cycle

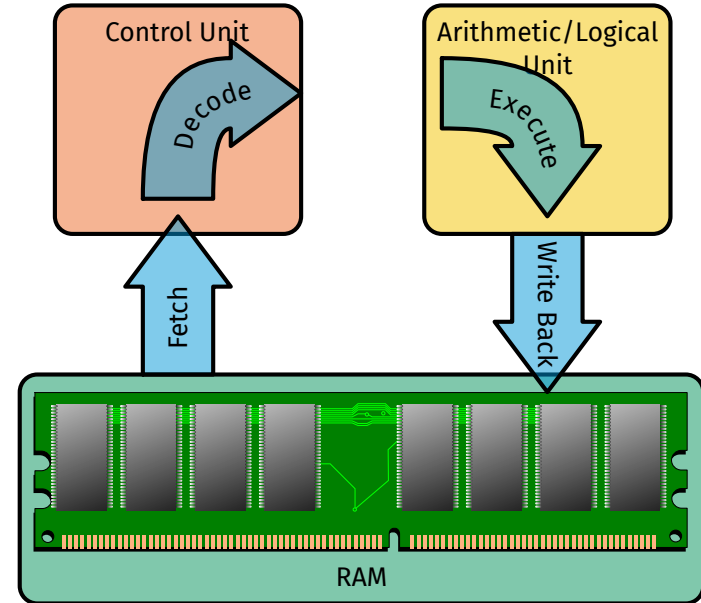
1. **Fetch** – the instruction from memory into the IR

1. Load the MAR with the PC
2. Place instruction into the MDR
3. Load IR with the MDR

2. **Decode** – Examined the IR and decides what to perform

3. **Execute** – Executes the operation

4. **Write Back** – Write the result back into memory



IR – Instruction Register

MAR – Memory address register

MDR – Memory data register

Data Architectures

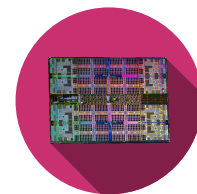
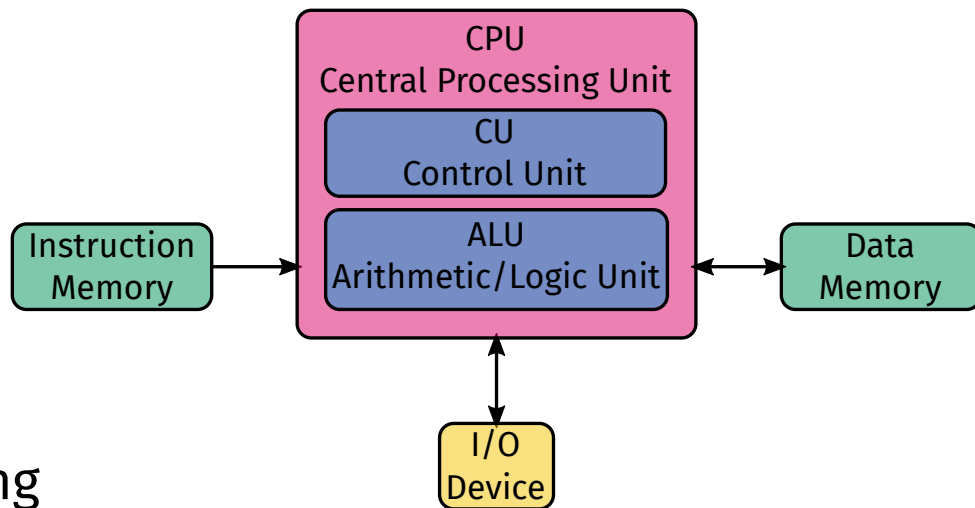
Harvard

- Separate memories for data and instructions
- Two sets of address/data busses between CPU and memory

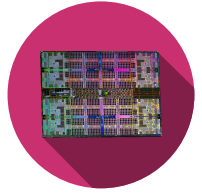
Advantages – greater memory bandwidth, different bit depth between instruction and data

Disadvantages – can't use self-modifying code

Examples – DSP, ARM9



References



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- [2]
D. Wentzlaff, “Computer Architecture ELE 475 / COS 475.” Princeton University, 2019.
- [3]
J. L. Hennessy and D. A. Patterson, *Computer Architecture: A Quantitative Approach*, 6th Edition. Elsevier, 2019.
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- [5]
S. L. Harris and D. M. Harris, “Digital Design and Computer Architecture RISC-V Edition,” in *Digital Design and Computer Architecture*, First Edition., Elsevier, 2022, pp. IBC1–IBC2. doi: [10.1016/B978-0-12-820064-3.00025-8](https://doi.org/10.1016/B978-0-12-820064-3.00025-8).
- [6]
TU Berlin: Course AES, (Oct. 22, 2018). Accessed: Jul. 18, 2022. [Online Video]. Available: <https://www.youtube.com/channel/UCPSsA8oxISBjidJsSPdpsjQ>
- [7]
“What’s the difference between Von-Neumann and Harvard architectures?” <https://www.microcontrollertips.com/difference-between-von-neumann-and-harvard-architectures/> (accessed Nov. 03, 2022).

WHY ARE THERE MIRRORS ABOVE BEDS

WHY DO I SAY UH

WHY IS SEA SALT BETTER

WHY ARE THERE TREES IN THE MIDDLE OF FIELDS

WHY IS THERE NOT A POKEMON MMO

WHY IS THERE LAUGHING IN TV SHOWS

WHY ARE THERE DOORS ON THE FREEWAY

WHY ARE THERE SO MANY SUCHOST-EXE RUNNING

WHY AREN'T ANY COUNTRIES IN ANTARCTICA

WHY ARE THERE SCARY SOUNDS IN MINECRAFT

WHY IS THERE KICKING IN MY STOMACH

WHY ARE THERE TWO SLASHES AFTER HTTP

WHY ARE THERE CELEBRITIES

WHY DO SNAKES EXIST

WHY DO OYSTERS HAVE PEARLS

WHY ARE DUCKS CALLED DUCKS

WHY DO THEY CALL IT THE CLAP

WHY ARE KYLE AND CARTMAN FRIENDS

WHY IS THERE AN ARROW ON AANG'S HEAD

WHY ARE TEXT MESSAGES BLUE

WHY ARE THERE MUSTACHES ON CLOTHES

WHY WUBA LUBBA DUB DUB MEANING

WHY IS THERE A WHALE AND A POT FALLING

WHY ARE THERE SO MANY BIRDS IN SWISS

WHY IS THERE SO LITTLE RAIN IN WALLIS

WHY IS WALLIS WEATHER FORECAST ALWAYS WRONG

WHY ARE THERE MALE AND FEMALE BIKES

WHY ARE THERE BRIDESMAIDS

WHY DO DYING PEOPLE REACH UP

HOW FAST IS LIGHTSPEED

WHY ARE OLD KLINGONS DIFFERENT

WHY ARE THERE TINY SPIDERS IN MY HOUSE

WHY DO SPIDERS COME INSIDE

WHY ARE THERE HUGE SPIDERS IN MY HOUSE

WHY ARE THERE LOTS OF SPIDERS IN MY HOUSE

WHY ARE THERE SPIDERS IN MY ROOM

WHY ARE THERE SO MANY SPIDERS IN MY ROOM

WHY DO SPYDER BITES ITCH

WHY IS DYING SO SCARY

WHY IS THERE NO GPS IN LAPTOPS

WHY DO KNEES CLICK

WHY AREN'T THERE 5 GRADES

WHY 2*B I 2*B

WHY ARE THERE GHOSTS

WHY ARE THERE ANTS

WHY ARE THERE PILEGRIMS

WHY ARE THERE SO MANY CROWS IN ROCHESTER

WHY IS TO BE OR NOT TO BE FUNNY

WHY IS THERE CAFFEINE IN MY SHAMPOO

WHY HAVE DINOSAURS NO FUR

WHY ARE SWISS AFRAID OF DRAGONS

WHY IS THERE A LINE THROUGH HTTPS

WHY IS THERE A RED LINE THROUGH HTTPS ON TWITTER

WHY IS HTTPS IMPORTANT

WHY AREN'T MY ARMS GROWING

WHY DO I FEEL DIZZY

WHY ARE THERE WEEKS

WHY DO IUGUANAS DIE

WHY AREN'T ECONOMISTS RICH

WHY DO AMERICANS CALL IT SOCCER

WHY ARE MY EARS RINGING

WHY IS 42 THE ANSWER TO EVERYTHING

WHY CAN'T NOBODY ELSE LIFT THORS HAMMER

WHY IS MARVIN ALWAYS SO SAD

WHY ARE THERE ANTS

WHY IS THERE A SWARM OF ANTS

WHY IS THERE PILEGRIM

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WHY DO OWLS ATTACK PEOPLE

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WHY ARE THERE GODS

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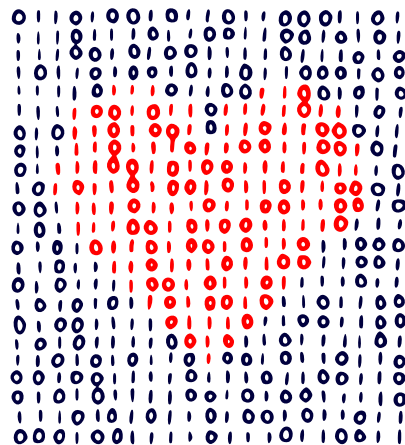
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QUESTIONS

CAN BE ASKED BY ANYONE ANYTIME

WHY IS THERE A LINE THROUGH HTTPS

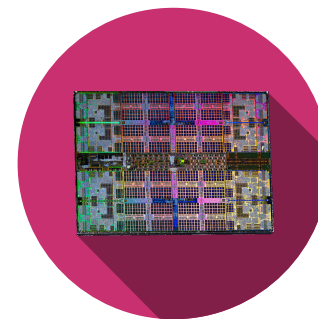
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Hes·so  **VALAIS
WALLIS**



Haute Ecole d'Ingénierie
Hochschule für Ingenieurwissenschaften



Silvan Zahno silvan.zahno@hevs.ch