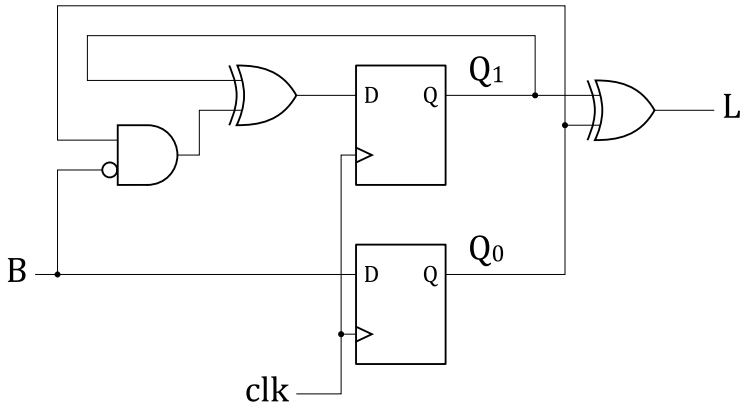
Statemachines

Exercises Digital Design

1 FSM - Moore machines

1.1 Graph of a state machine

The following figure shows the circuit of a state machine.

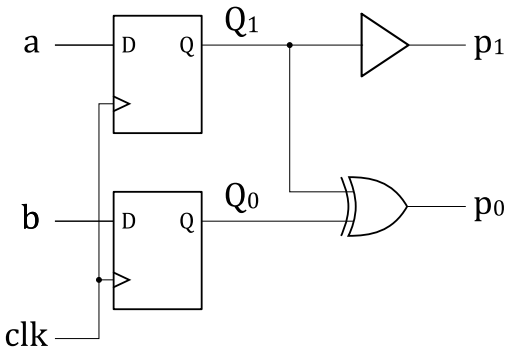


Draw the graph of this state machine.

fsm/moore-01

1.2 Graph of a state machine

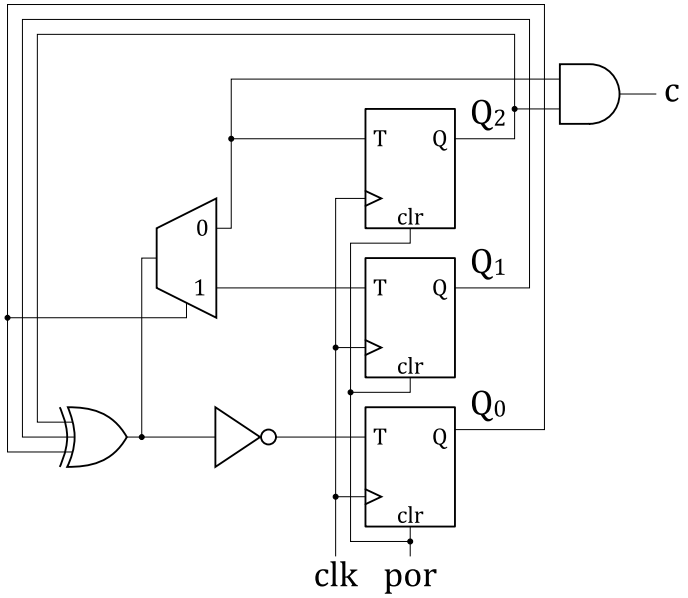
Draw the graph of the state machine in the following figure.



fsm/moore-02

1.3 Sequence of a counter

The following figure shows the circuit of a counter.

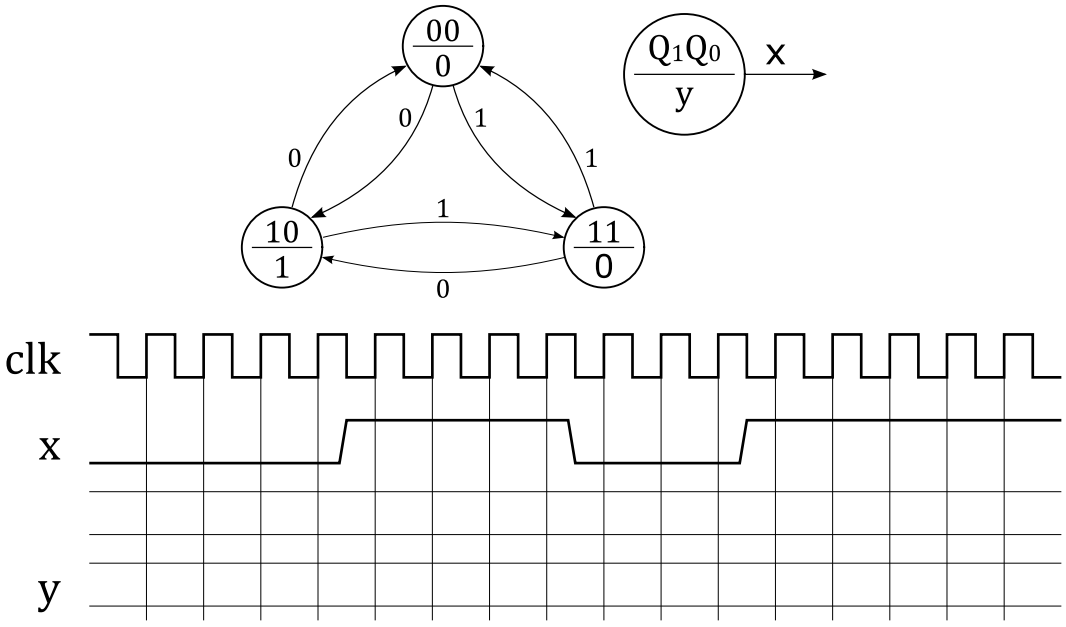


Enter the number sequence of this circuit.

fsm/moore-03

1.4 Temporal behavior of a state machine

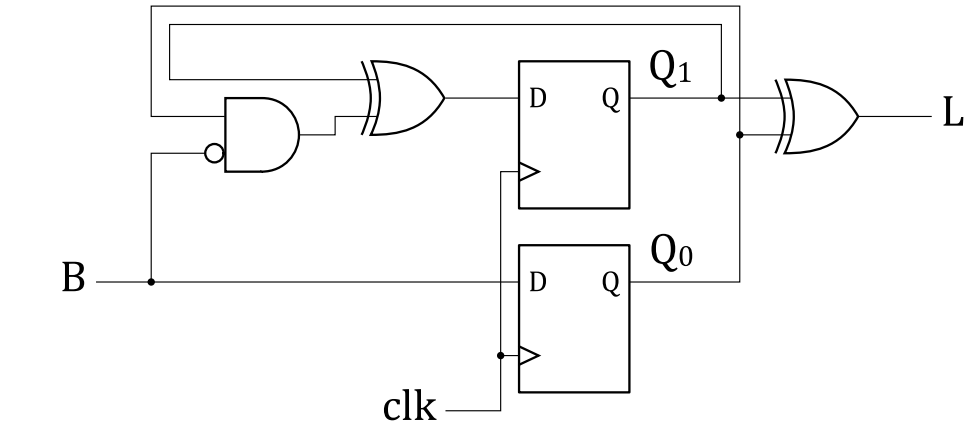
For the system defined by the following state graph, enter the temporal behavior of the output signals.
The circuit starts in the state **"00"**.

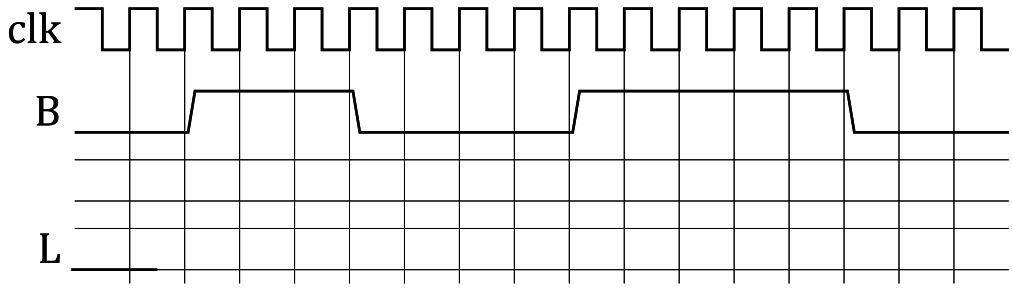


fsm/moore-04

1.5 Temporal behavior of a state machine

For the circuit of the following figure, enter the temporal behavior of the output signal.



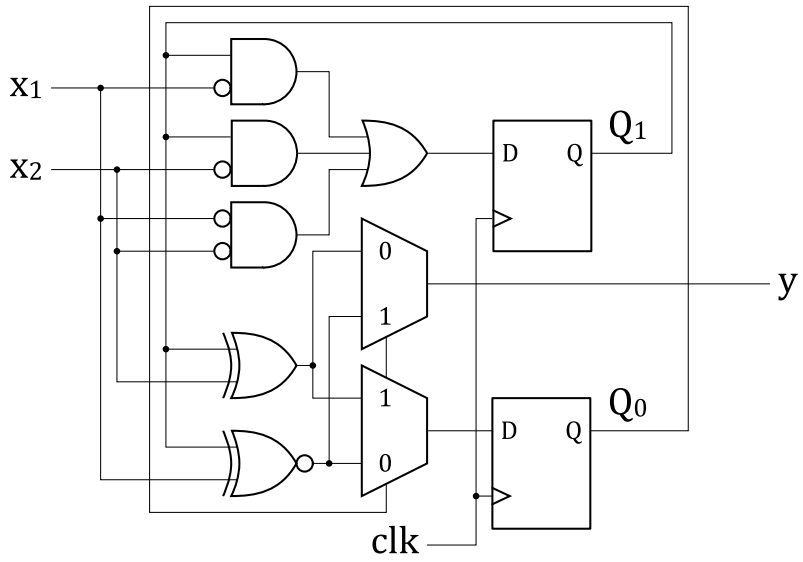


fsm/moore-05

2 FSM - Mealy machines

2.1 Graph of a state machine

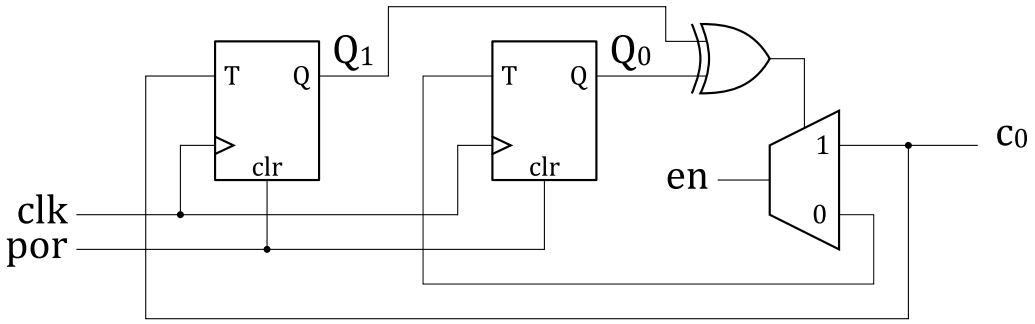
Draw the state graph of the circuit in the following figure.



fsm/mealy-01

2.2 Graph of a state machine

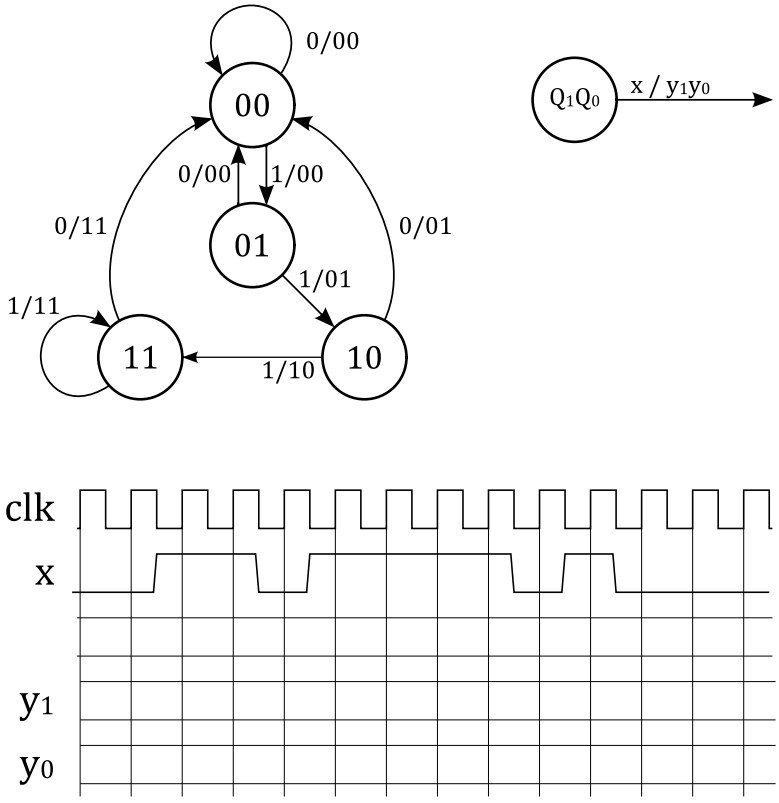
Draw the state graph of the circuit in the following figure.



fsm/mealy-02

2.3 Temporal behavior of a state machine

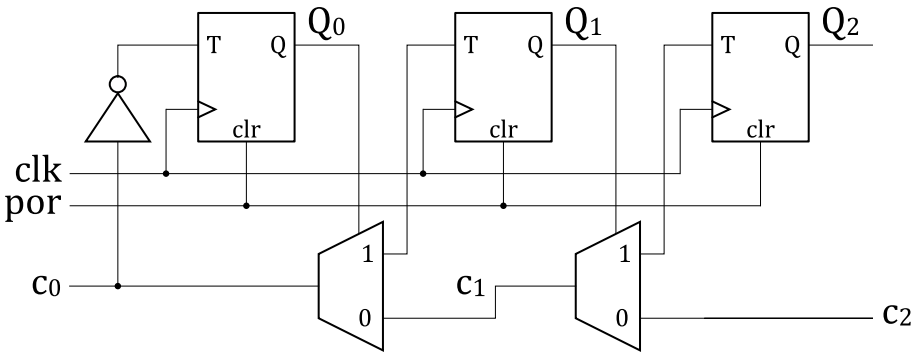
For the system defined by the following state graph, enter the temporal behavior of the output signals.



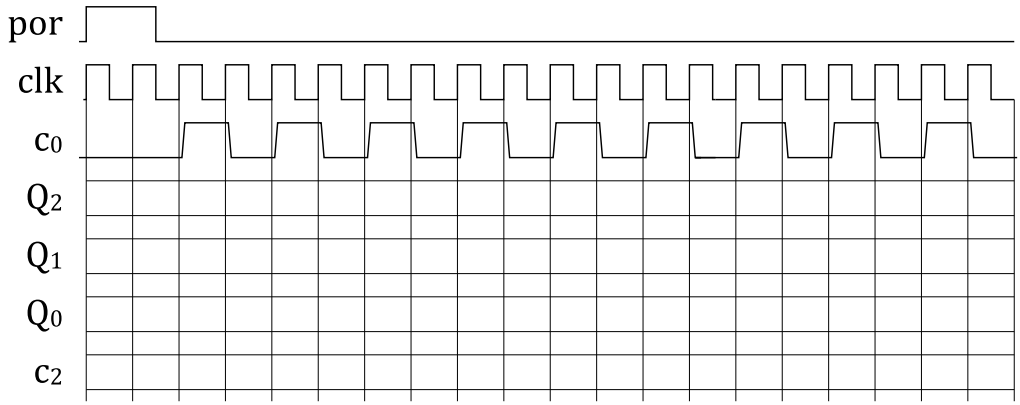
fsm/mealy-03

2.4 Iterative Counter

The following figure shows an iterative counter.



Draw the temporal behavior of the output signal c_2 in the figure below.

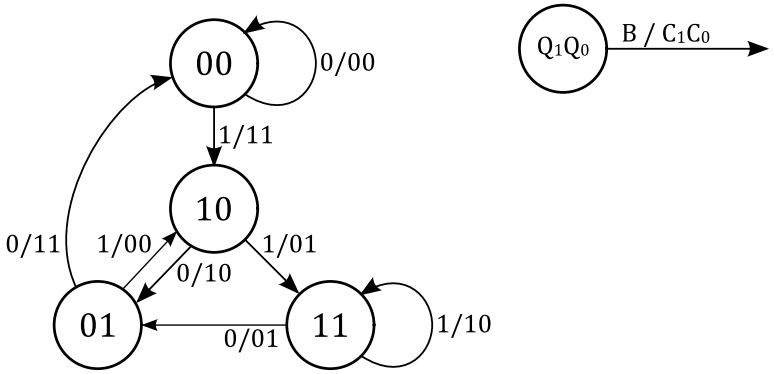


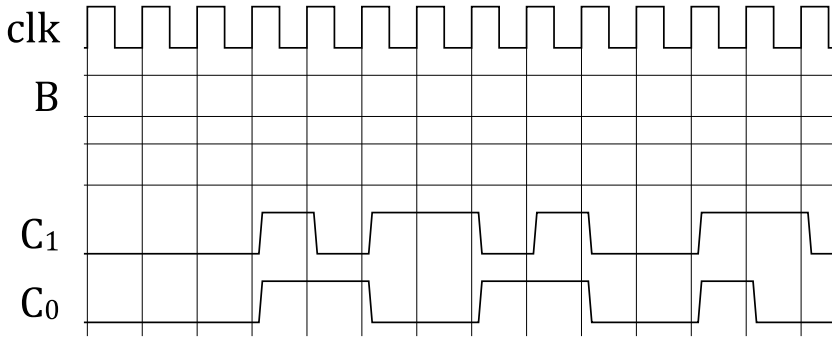
Explain whether this is a Moore or a Mealy machine. Give an example or proof of your explanation. Determine the number of bits of the counter that switch on each clock pulse. Give the name of this sequence.

fsm/mealy-04

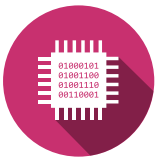
2.5 Temporal behavior of a state machine

For the system defined by the following state graph, enter the temporal behavior of the input signal.





fsm/mealy-05



3 FSM - State graph generation

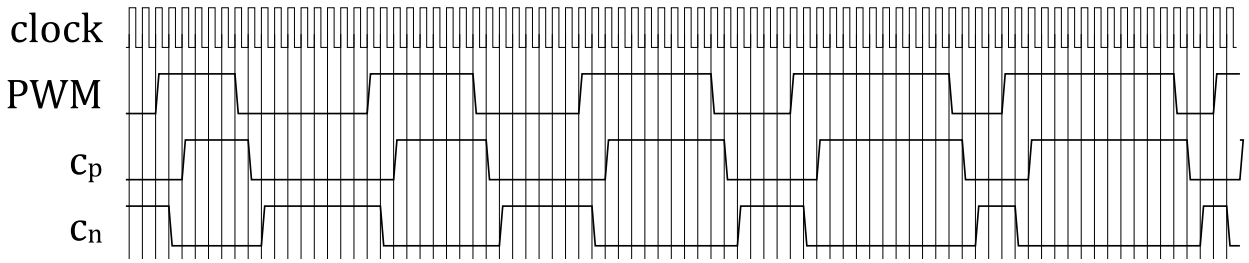
3.1 Operation Monitoring

An operation verification circuit (watchdog) determines whether a microprocessor is functioning correctly or whether it is lost in an endless loop.
To do this, the processor must send a **`heartbeat`** pulse to the watchdog at least once a second. If this is not the case, the watchdog activates the processor's restart signal **`resetProc`**. It will keep this control active for 1 second.
To measure the time, the watchdog receives a **`1hz`** input in the form of impulses, which occur once per second with a duration of one clock period. In contrast, the heartbeat pulse of the processor can last several clock pulses.
Draw the state graph of this watchdog.

fsm/fsm-01

3.2 Generator of non-overlapping control signals

A power electronics circuit generates a signal that switches an output either to a potential of +340 V or to a potential of −340 V. To avoid respective short circuits, the control circuit should be sequenced so that one switch is switched on one clock period later after the other has been switched off.
The generator of non-overlapping control signals receives the binary signal **`PWM`** and generates the control signals c_p and c_n for the two circuit breakers.



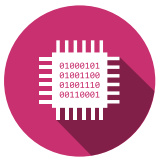
Draw the state graph of this generator of non-overlapping control signals.

fsm/fsm-02

3.3 Control of a Snack Machine

Draw the state graph of a control for a snack machine.
All selectable products cost 3 CHF. If a customer inserts a 1 CHF coin, the input **`coin1`** is activated for one cycle period. When a 2 CHF coin arrives, it is the input **`coin2`** which gives a pulse for one cycle period. As soon as the amount of 3 CHF is reached, the output **`open`** goes to **`'1'`** for one clock period.
The device does not return any money, but releases the additional amount for the next purchase.

fsm/fsm-03



3.4 Lighting control

Mit einem Druckknopf wird die Beleuchtung eines Raums bedient. Drückt man einmal auf den Knopf, so geht das Licht an. Drückt man ihn noch einmal geht das Licht wieder aus.
Zeichnen Sie den Zustandsgraph dieses Systems.

fsm/fsm-04

3.5 Detection of a rising edge

Draw the state graph of the detector of a rising edge of an input signal for the following two cases:

- the circuit provides a pulse that lasts a whole clock period,
- the circuit provides a pulse that starts when the rising edge of the input signal occurs and remains until the next rising edge of the clock signal.

fsm/fsm-05

3.6 Recognition of character strings

A circuit must recognize all words in a text that end with the character string **`"er "`**. In the text analysis system, it is preceded by another circuit that is controlled by the same clock signal and encodes the characters as follows with 2 bits each:

- **`"00"`** for the letter **`'e'`**,
- **`"01"`** for the letter **`'r'`**,
- **`"10"`** for a separator (space, punctuation mark),
- **`"11"`** for every other character.

A new character is encoded and transmitted at each clock period.
Draw the graph indicating the recognition of a word ending with the character string **`"er "`**. This should be indicated immediately after the transfer of the separator character.

fsm/fsm-06

3.7 Electronic lock

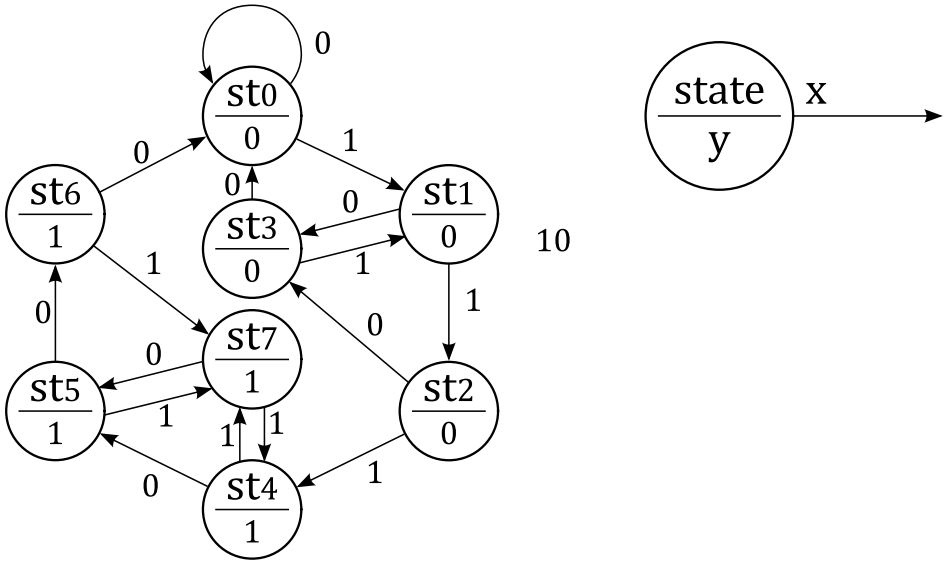
An electronic lock is controlled via a 10-part keypad, which supplies a binary code from 0 to 9 coded to 4 bits. The keypad still supplies a binary code 1111 if no key is printed. When a key is pressed, the circuit sends a pulse during a clock period, which produces a sound signal. As soon as the sequence 1 ⇨ 9 ⇨ 9 ⇨ 7 has been sent, the circuit activates a signal to open the door. This signal remains active until the door is closed again. A switch indicates the status of the door: **`'0'`** when the door is closed and **`'1'`** when it is open.
Draw the state graph of the system.

fsm/fsm-07

4 FSM - Graph reduction

4.1 Graph Simplification

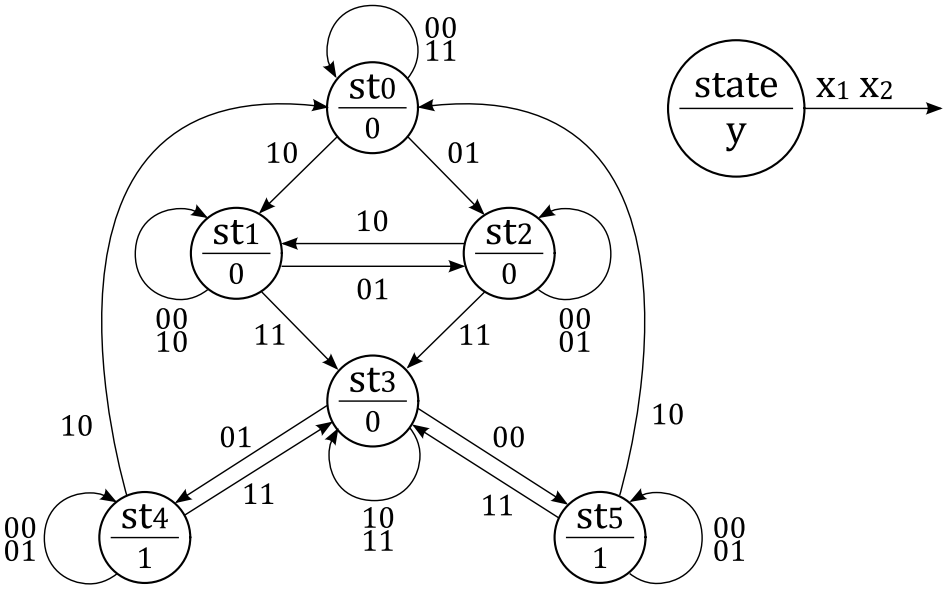
Redraw the graph in the following figure so that it has a minimum number of states.



fsm/reduction-01

4.2 Graph Simplification

Redraw the graph in the following figure so that it has a minimum number of states.



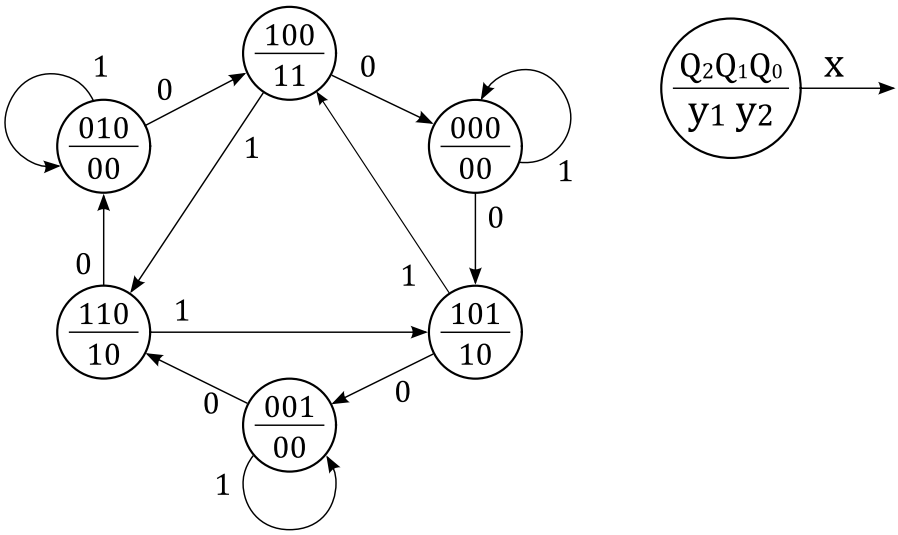
Determine the smallest required number of flip-flops for the corresponding circuit.

fsm/reduction-02

5 FSM - State coding

5.1 Logic Circuit

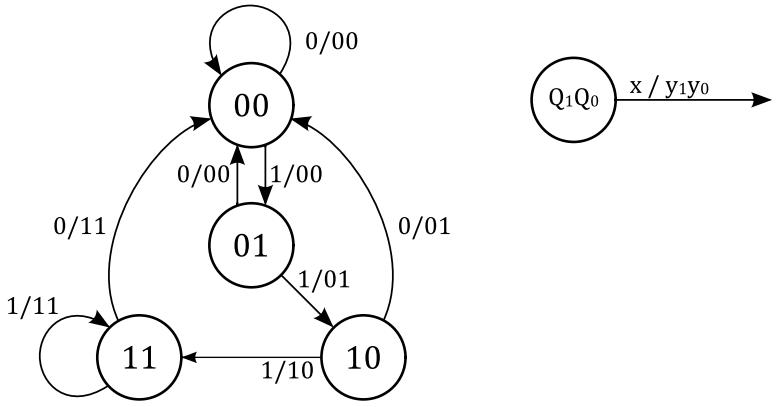
Draw the schematic of the circuit that creates the graph in the following figure.



fsm/coding-01

5.2 Logic Circuit

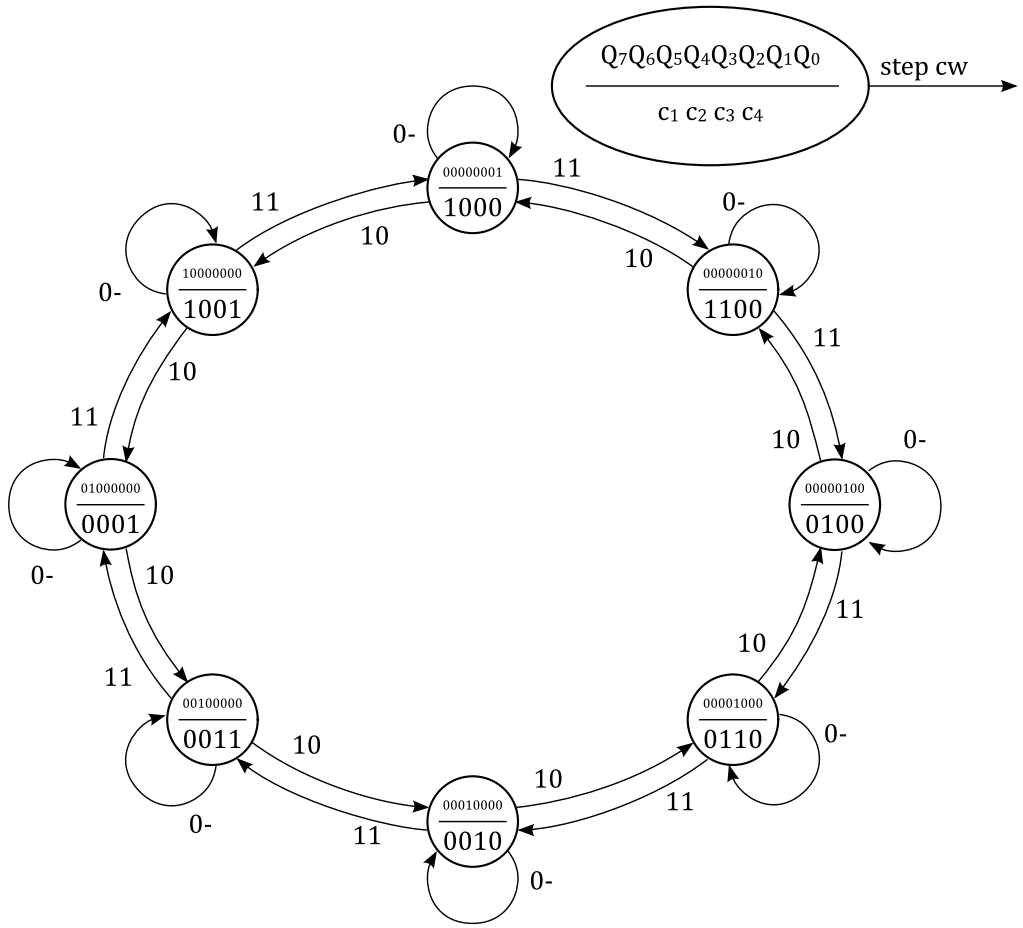
Draw the schematic of the circuit that creates the graph in the following figure.



fsm/coding-02

5.3 Logic Circuit

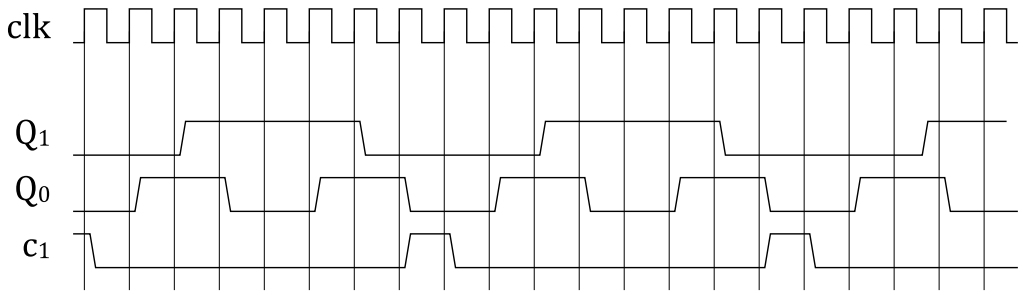
Draw the schematic of the circuit that creates the graph in the following figure.



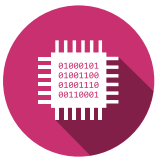
fsm/coding-03

5.4 Logic Circuit

Draw the schematic of the circuit that creates the sequence in the following figure.



fsm/coding-04



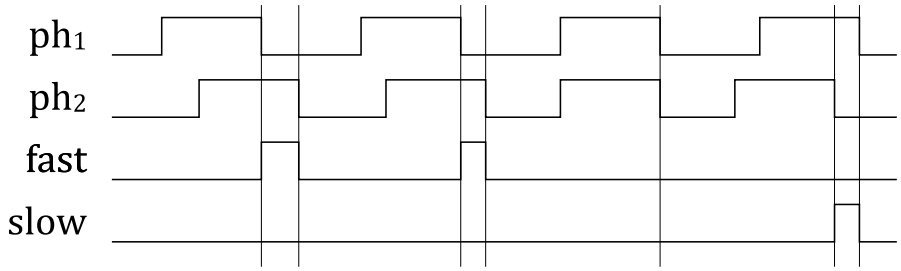
5.5 Detection of a falling edge

Draw the diagram of a Moore machine that detects a descending edge of an input signal.
Assume that the pulses of the input signal always last more than one clock period.

fsm/coding-05

5.6 Phase Detector

A generator controller must synchronize with the phase of the circuit at 50 Hz.
A phase detector is used for this. If the phase of the generator, ph_2, comes before the phase of the mains, ph_1, the detector activates the signal **`slow`**, which slows down the generator. If, on the other hand, ph_2 occurs after ph_1, the detector activates the **`fast`** signal, which accelerates the generator.
The following figure shows an example of the operation of the circuit to be developed.



Draw the state graph of the system, reduce it if necessary, propose an encoding 1 under m (one-hot) and create the schematic of the corresponding circuit.

fsm/coding-06