Introduction to the EDA Tools (IND)

Labor Digital Design

Contents

1 Objective

This first lab is intended to familiarize you with the automated development tools in electronics (Electronic Design Automation (EDA)). You will learn to use the circuit development tool **`Mentor HDL-Designer`** and the circuit simulator **`Mentor Modelsim`**, as well as the connection between the two. An example of a simple logic circuit with inverters, AND and OR gates will be created and simulated.

Figure 1: Mentor HDL Designer

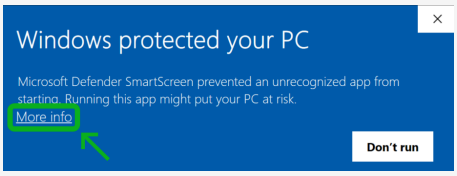
Figure 2: Mentor ModelSim

2 Introduction

Follow the steps below to download and set up the lab files:

- Download the required lab files via the following link (https://github.com/hei-synd-did/did-labs/archive/refs/heads/main.zip).
- Unzip the archive on your network drive: **`\\filer01.hevs.ch\FS_COURSES\102.1-DiD-102.2-CAr\<firstname.lastname>`**.
- Run the file **`did-labs/did-labs.bat`**.

If a security message appears (*only on the first run*), click on **`More Info`** and **`Run anyways`**



- After HDL Designer has opened, click on the **`Project`** tab.

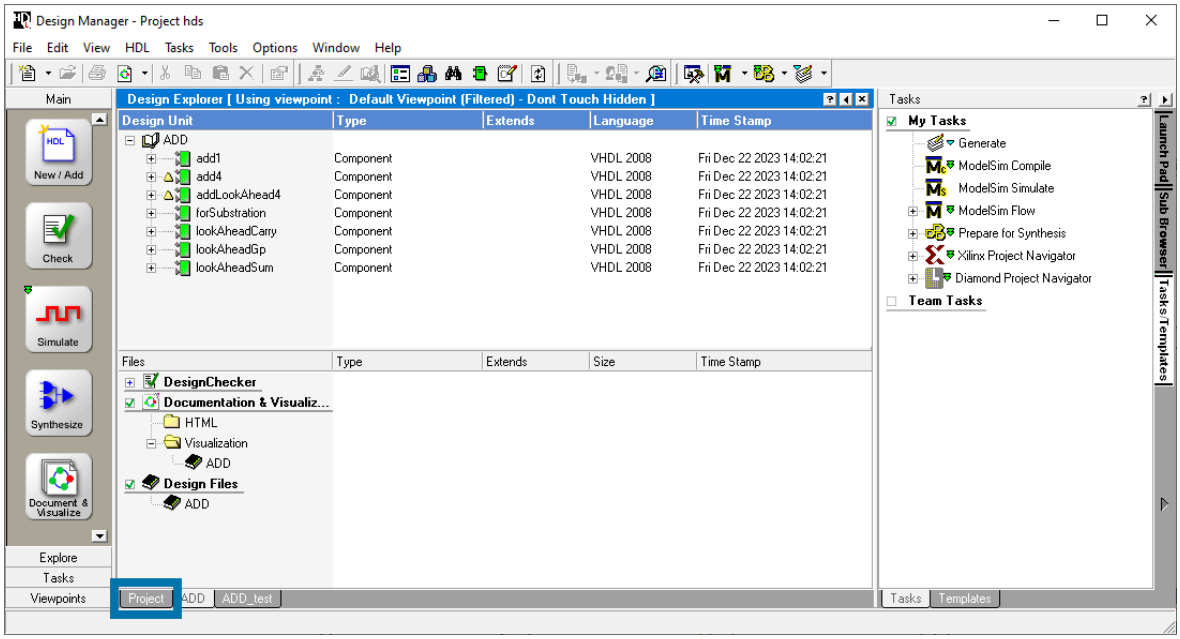
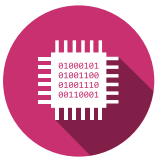


Figure 4: HDL Designer

- Double-click on the relevant libraries for the lab to open them. Each lab has 2 libraries that bear the abbreviation of the lab. In this lab "IND", they are the **`IND`** and **`IND_test`** libraries.

The files must not be left on the lab computers. They must be saved on a USB stick or on the **`\\filer01\...`**. Also share the files with your lab partner so that they can continue the work.



3 Combinatorial logic circuit

We will now move on to the actual circuit that needs to be implemented. A company has decided to check each of its purchases according to strict rules. An item may only be purchased if at least one of the following conditions is met:

- **`Condition A`**: the company's order books are full, the delivery time of the material is short and the company's stocks are low
- **`Condition B`**: the order books are not full, but the price and the company's stocks are low
- **`Condition C`**: the price is high, but the order books are full and the company's stocks are low
- **`Condition D`**: the company's stocks are low and the delivery time is short
- **`Condition E`**: the delivery time is long, but the price is low

Complete the truth table Table 1 according to the specification.

Deduce from the table a circuit composed of the basic gates AND, OR and inverter.

3.1 Design

Open the circuit under **`IND`** ⇨ **`selection`**. The input and output signals are already defined, as is the condition A (**`condition A`**).

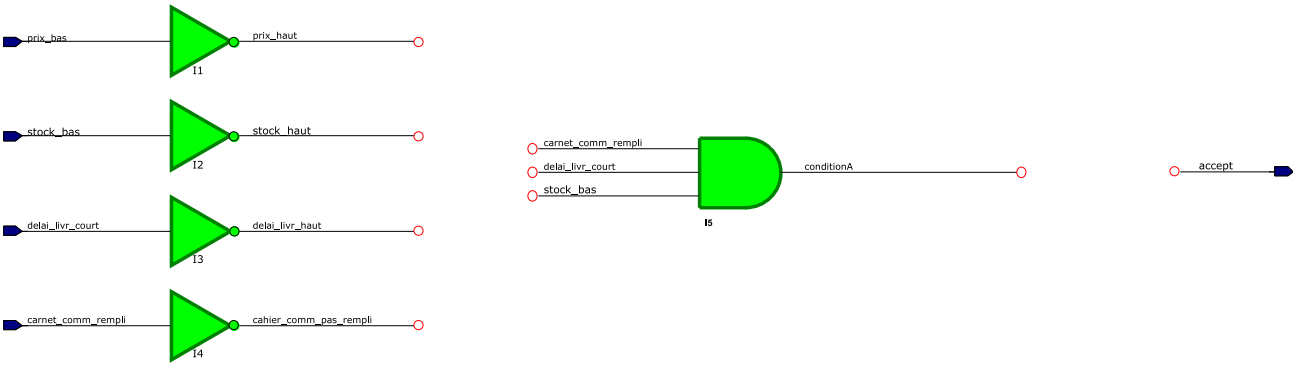
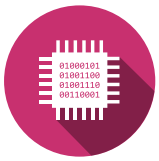
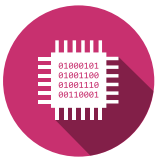


Figure 5: Circuit to complete



Order book full				Condition					Accept
				A	B	C	D	E	

Table 1: Truthtable



4 Circuit Editor

This section will guide you through the creation of a digital circuit.

Using inverters, AND and OR gates, draw the circuit you read from the truth table Table 1.

For detailed information on how to use HDL Designer and ModelSim, refer to the document **DiD-EDA-UserGuide-en.pdf** on Cyberlearn [1].

4.1 Components

Components are logical gates, constant signals such as logic_0 / logic_1, multiplexers, flip-flops ... as well as user-created blocks.

- Add a component by clicking on the button **`Add Component`**.

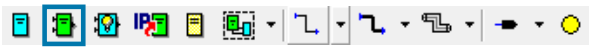


Figure 6: Add Component

- Search for the desired component in the **`gates`** library.
- Select the component and drag it into the circuit.

Add all components required for your circuit.

4.2 Signals

Signals are used to connect the inputs and outputs of the different blocks together. They can represent a bit (**std_ulogic**) or several bits (**std_ulogic_vector**, **signed**, **unsigned**). Signals can be connected by lines or by their names.

4.2.1 Adding a Signal

- Add a signal by clicking on the button **`Add Signal`**.

Figure 7: Add Signal

- After clicking on the button, a new signal can be created by clicking on the schematic.
- To confirm a new signal, connect an input and an output together or double-click to finish creating the signal.
- Press the **`ESC`** key to cancel the creation of a signal.

4.2.2 Changing the Signal Name

Double-click on a signal to change its name. The name of the signal can be changed in the **`text field`**.

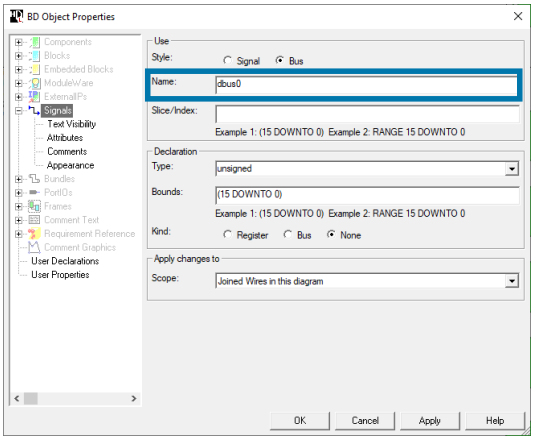


Figure 8: Edit Signal and Bus Properties

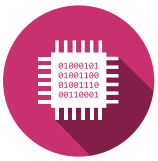
Signals with the same name are connected together! Signals with different names must be connected together via buffers.

4.3 Tasks

Create your schematic in a clear and readable way.

- Name each signal in the schematic.
- Set the display settings for the signal names.
- Make the schematic readable by connecting some signals by name and not by a wire.

It is important to always display the name of a signal. Incorrect manipulation sometimes changes the name automatically and this is not detectable without the signal name.



4.4 Layout

The circuit, once properly filled out, can be printed and/or exported as a PDF.

First:

Fill in the available frame.

Make all necessary changes to make this circuit as readable as possible.

To create the PDF or print, go to **`File`** ⇨ **`Page setup`** and use the following configuration:

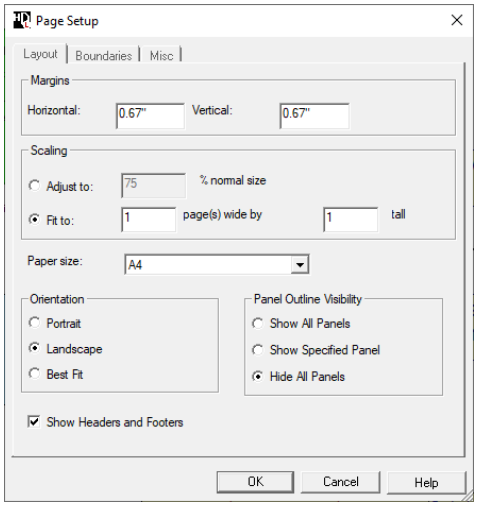
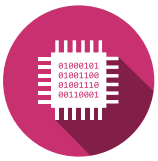


Figure 9: Page configuration

- Print the circuit on a physical printer or select **`Adobe PDF`** or **`Microsoft print to PDF`** to export the page as a **`PDF`**.

Export your circuit as a PDF.



5 Simulation

To ensure that the circuit works correctly, a simulation is performed testing all possible combinations of input signals.

5.1 Testbench

The simulation is located under **`IND_test`** ⇨ **`IND_tb`**.

The **`Testbench`** is composed of two parts:

- The circuit to be tested (**`DUT - Device Under Test`**), the circuit developed previously
- The tester generating the input signals for the DUT and checking the outputs.

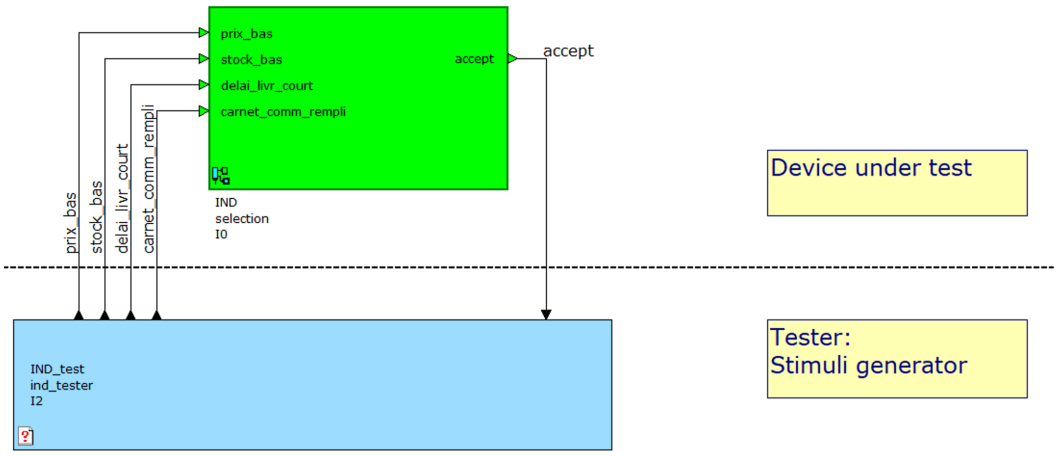


Figure 10: Generate VHDL

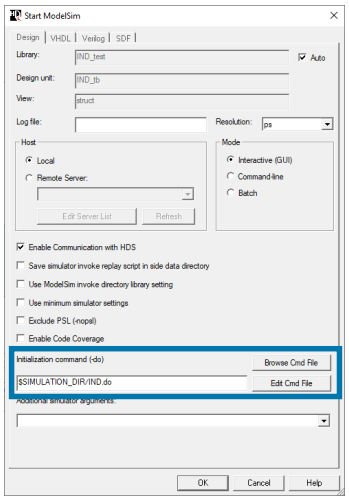
5.2 Simulator

Click on the button **`Generate and run entire ModelSim flow (Through Components)`** to start the simulation.

Figure 11: Generate VHDL

When the simulation is started, no block of the circuit must be selected.

- If the generation and compilation are successful, the following window will appear:



- Enter the **initialization command file** (***.do**), in this case **$SIMULATION_DIR/IND.do**. This file contains the information of the signals to be displayed.
- Click on **OK**.

> The ***.do** files are located in the **Simulation** directory, located at the root of **did-labs**.

If nothing happens when the simulation is started, check the log window. If the log window is not displayed:

- Right-click on the **Log Window** window.
- Click on **Maximize**.

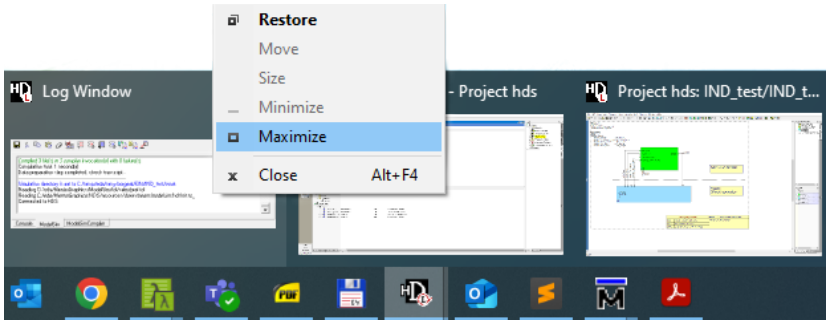


Figure 12: Display the log window

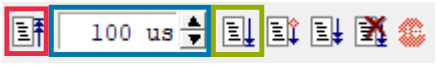
This window displays problems related to the compilation of the circuit that must be corrected to start the simulation.
Errors can be displayed in Red, Green or Black.

> Start the simulation program using the file **$SIMULATION_DIR/IND.do**.

5.2.1 Starting the simulation

The simulation is “stimulated” by the tester block with values.

> Open the testers file and determine the required simulation time.



- Enter the simulation time in the **Text field**.
- Click on the button **Start simulation**.
- With the button **Reset simulation** you can reset the simulation.

Start the simulation and check if the input and output signals are correct.

5.3 Display

The different elements of the simulation program **Mentor ModelSim** are shown in Figure 13:

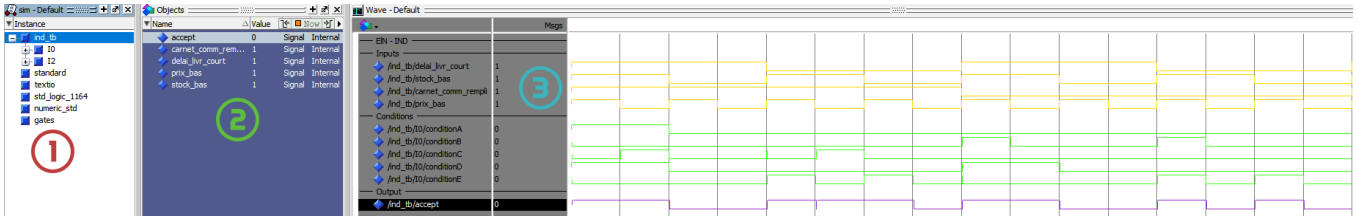


Figure 13: Simulation with only condition A

1. Hierarchy of the circuit, of each individual block window 1. By selecting a block, the associated signals are displayed in window 2.
2. Displays the available signals in the selected block. They can be dragged into window 3 (Drag&-Drop) to display them.
3. The **Wave** simulation window with the signals of the circuit.

5.3.1 Adding signals

Adding signals is done as described previously.

After adding signals, a restart of the simulation is necessary to display them.

Add the signals of the remaining 4 conditions in the simulation window.

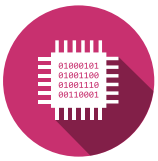
5.3.2 Time scale

By right-clicking on the time scale ⇨ **Grid, Timeline & Cursor control** you can change the time scale and the time marking grid.

Change the time scale to be displayed in nanoseconds.

5.3.3 Functionality control

To check the functionality of the circuit, the signals must be correlated with each other.



In some labs, the **Transcript** window at the bottom of **ModelSim** can also display information about automated tests.

Check if your simulation matches your truth table Table 1.

5.3.4 Saving the context

To be able to reopen the simulation with the previous settings, you can save the configuration by pressing **Ctrl + s** in the **Wave** window.

The generated **.do** file can be saved in the **Simulation** folder of the project.

Save the configuration of the simulation and overwrite the current file **IND.do**.

5.3.5 Printing the simulation

Like the schematic, simulation signals can be printed or exported as PDF via **File** ⇨ **Print...**.

A recommended print configuration is shown in Figure 14:

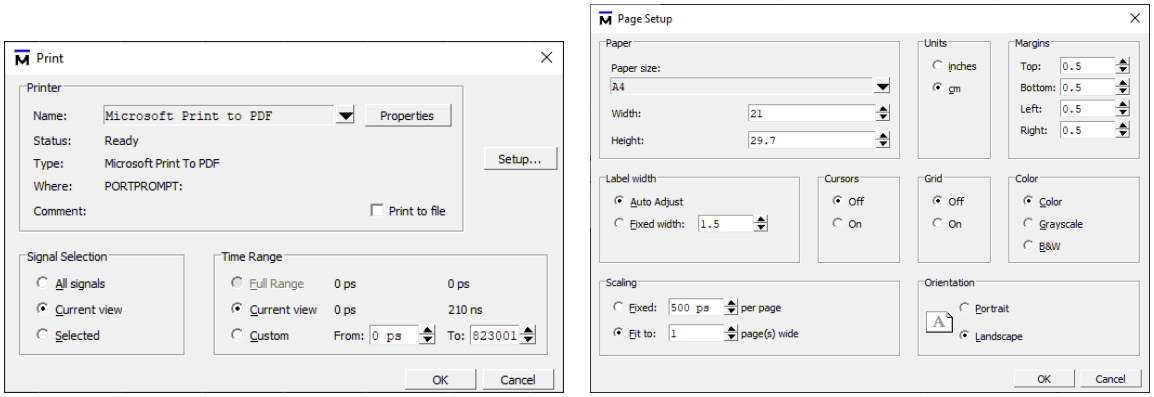


Figure 14: Recommended print configuration for the simulation

Export the result of the simulation as PDF.

5.4 Glitch

Glitches can appear on the output signal. One of these glitches is highlighted in Figure 15.

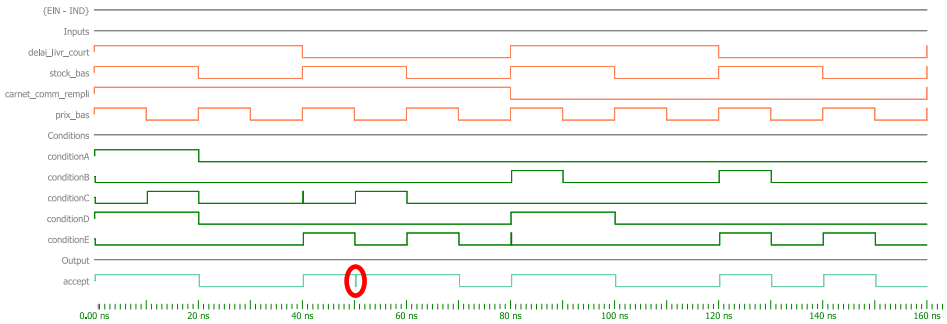
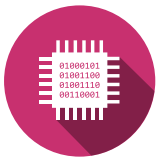


Figure 15: Glitch on the output signal

- Find these glitches in your simulation.
- Explain the reason for these glitches.



Bibliography

[1] A. A. Silvan, Zahno Rémy, Borgeat, "DiD EDA Userguide." 2024.