



# Synchronous counters

## Exercises Digital Design

## 1 | CNT - Counters by a power of 2

### 1.1 Downwards Counter

Using D flip-flops and combinational logic gates, create a synchronous down-counter with the sequence

$$15 \Rightarrow 14 \Rightarrow 13 \Rightarrow 12 \Rightarrow \dots 3 \Rightarrow 2 \Rightarrow 1 \Rightarrow 0 \Rightarrow 15 \Rightarrow 14 \Rightarrow \dots \quad (1)$$

Draw the complete schema.

*cnt/pow2-01*

### 1.2 Downwards Counter

Use T flip-flops and NAND gates to create a synchronous down-counter with the sequence

$$7 \Rightarrow 6 \Rightarrow 5 \Rightarrow 4 \Rightarrow 3 \Rightarrow 2 \Rightarrow 1 \Rightarrow 0 \Rightarrow 7 \Rightarrow 6 \Rightarrow \dots \quad (2)$$

Draw the complete schema.

*cnt/cnt-pow2-02*



## 2 | CNT - Counters by any number

### 2.1 Downwards Counter

Using D flip-flops and NAND gates, create a modulo-10 synchronous down-counter with the sequence

$$9 \Rightarrow 8 \Rightarrow 7 \Rightarrow 6 \Rightarrow \dots 3 \Rightarrow 2 \Rightarrow 1 \Rightarrow 0 \Rightarrow 9 \Rightarrow 8 \Rightarrow \dots \quad (3)$$

Draw the complete schema.

Draw the state graph with all states, including those outside the main loop.

*cnt/cnt-01*

### 2.2 Downwards Counter

Use D flip-flops and multiplexers to create a synchronous down-counter with the sequence

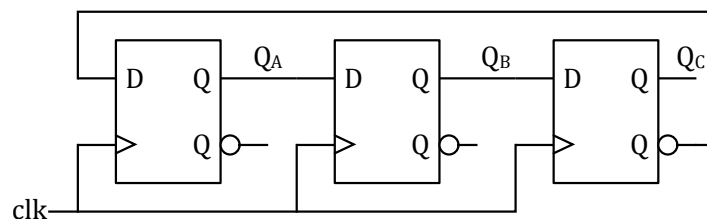
$$6 \Rightarrow 5 \Rightarrow 4 \Rightarrow 3 \Rightarrow 2 \Rightarrow 6 \Rightarrow \dots \quad (4)$$

Draw the complete circuit.

*cnt/cnt-02*

### 2.3 Johnson Counter

The following figure shows a Johnson counter.



This type of counter is of interest for high-speed systems. The circuit has one disadvantage: it has two independent sequences.

Eliminate the shortest sequence by changing the input function  $D_B$  of the second flip-flop.

*cnt/cnt-03*



## 3 | CNT - Iterative circuits

### 3.1 Counter with Synchronous Zeroing

Use D flip-flops and NAND gates to create a 4-bit counter with synchronous zero setting.

The counter has a control input **restart**. If **restart='1'**, the circuit sets itself to zero at the next active clock edge. If **restart='0'**, the circuit counts upwards.

*cnt/cnt-iterativ-01*

### 3.2 Counter with loading of a value

With the help of D flip-flops and NAND gates, you can create a 4-bit counter in which a new value can be loaded.

The counter has a control input **load** and a 4-bit data input. If **load='1'**, the circuit loads the data input. If **load='0'**, the circuit counts upwards.

*cnt/cnt-iterativ-02*

### 3.3 up-down counter

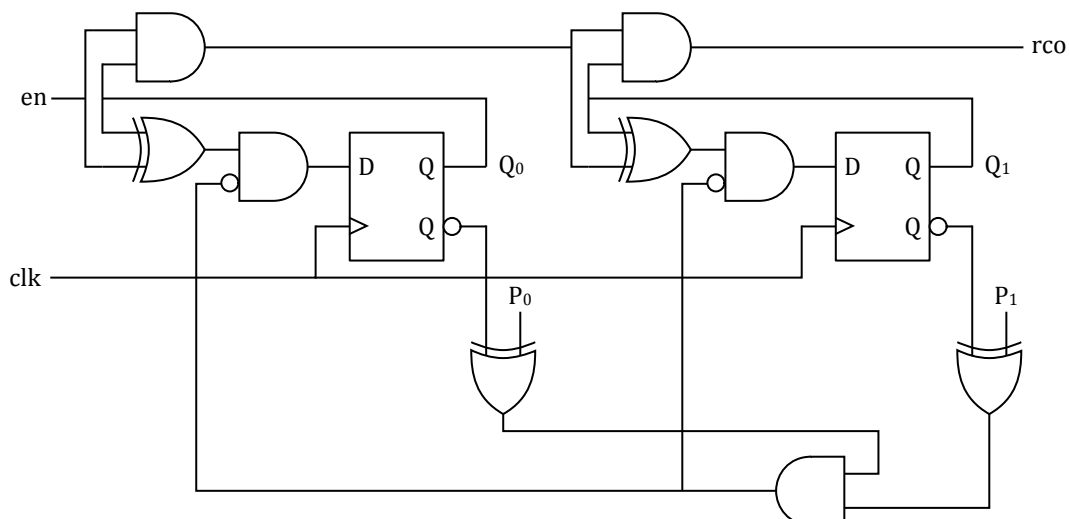
Create a 4-bit up-down counter using D flip-flops and NAND gates.

The up-down counter has a control input up  $\overline{\text{down}}$ . If up  $\overline{\text{down}} = '1'$ , the circuit counts upwards. If up  $\overline{\text{down}} = '0'$ , the circuit counts down.

*cnt/cnt-iterative-03*

### 3.4 Programmable Counter

The following figure shows the schematic of a programmable counter.



Determine the length of the counting sequence as a function of the input number  $[P_1, P_0]$ .

Modify this circuit to make the zero setting cascadable.

*cnt/cnt-iterativ-04*

