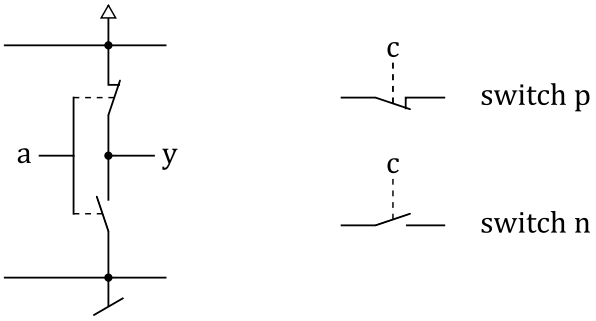
Logical states

Exercises Digital Design

1 | LST - Single-state logic gates

1.1 Switch Circuits

Determine the relationship between the input and output of the circuit in the following figure.

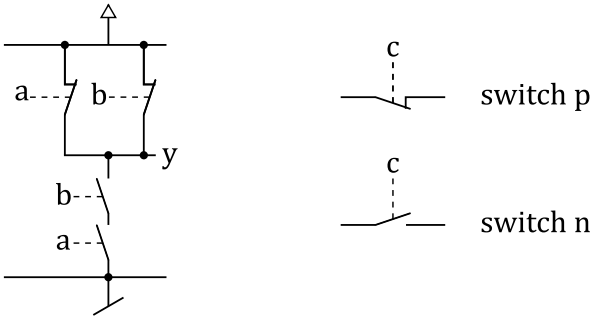


An n-type switch is closed if the control signal is at `'1'`. A p-type switch is open if the control signal is `'1'`.

lst/one-state-01-01

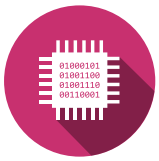
1.2 Switch Circuits

Determine the relationship between the input and output of the circuit in the following figure.



An n-type switch is closed if the control signal is at `'1'`. A p-type switch is open if the control signal is `'1'`.

lst/one-state-01-02



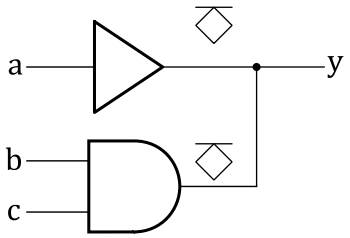
1.3 Switch Circuits

Using only switches, propose a scheme of an XOR gate with 2 inputs.

lst/one-state-01-03

1.4 Open-Source Circuit

Complete the circuit in the adjacent figure.
Enter the truth table of the output **y** as a function of the 3 inputs



lst/one-state-02-01

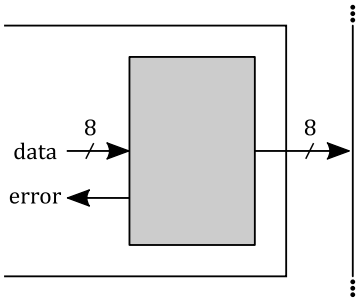
1.5 Alarm Circuit

Propose the scheme of a fire alarm circuit in a building.
The building contains 16 smoke sensors, which are placed in different rooms. These are linked together by a 3-wire cable: 2 for the power supply and 1 for the information transmission. The activation of a single sensor should cause a siren to sound.
One sensor provides a `'1'` when smoke is detected. The siren wails as soon as its control signal switches to `'1'`.

lst/one-state-02-02

1.6 Collision Detection

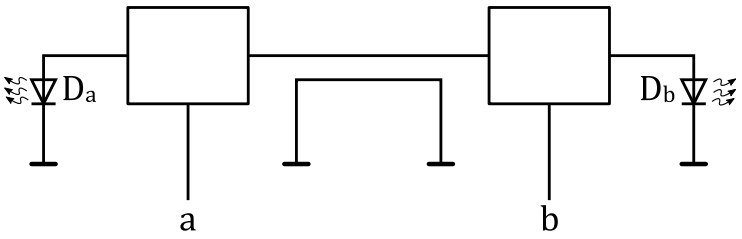
Draw the diagram of a bus interface where several blocks are able to write an 8-bit value on a common bus and control its value.
If the value on the line is different from the intended one, the bus interface sends an error indication signal to the block to let it know the transmission problem.
Propose a method to prioritize the data on the bus.



lst/one-state-02-03

1.7 Transmission of information on a single wire

Enter the inner schema of the blocks of the circuit of the following figure.



a	b	D_a	D_b
0	0	0	0
0	1	1	0
1	0	0	1
1	1	0	0

lst/one-state-02-04

2 | LST - Logic gates with high impedance output

2.1 Series linking of peripheral modules

Propose a scheme for linking components to a common data bus.
The system contains 3 components, each of which provides an 8-bit value. To select one of them, the system control creates an address coded to 2 bits. The mode of operation is as follows:

- if the address is 0, no component transmits a value,
- if the address is 1, block 1 transmits its value,
- if the address is 2, block 2 transmits its value,
- if the address is 3, block 3 transmits its value.

lst/hiz-01

2.2 Creation of a function Tristate circuits

Implement a 2 to 1 multiplexer using buffers with high impedance output (tri-state).

lst/hiz-02

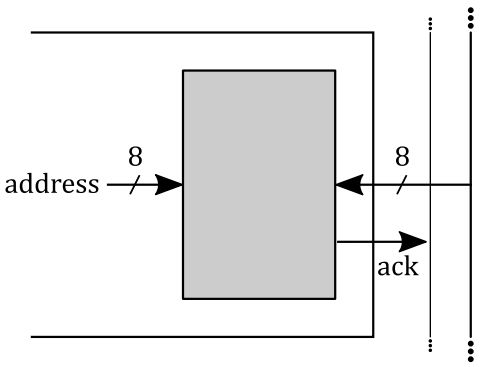
2.3 Creation of a function with the help of tristate circuits

Suggest the schema of an open-drain inverter based on tristate inverters.

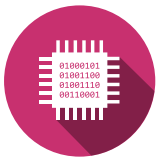
lst/hiz-03

2.4 Collision Detection

Propose the scheme of a bus interface where the blocks indicate their presence when their address appears.
If the address on the external bus is the same as that of the block, the bus interface indicates its presence on the **`ack`** (acknowledge) line, which is common to all blocks.
Propose a technique to add identical components to this system one by one during operation without having to configure them manually.

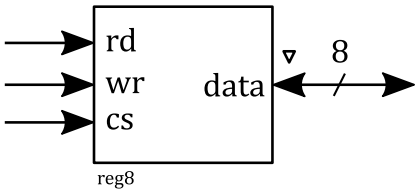


lst/hiz-04

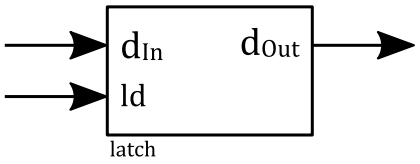


2.5 Register with bidirectional data bus

Enter the inner schema of an 8-bit register with bidirectional data bus.
The register is linked to a bidirectional data bus. For write access, an 8-bit value is placed on the data bus and the control signals **cs** (chip select) and **wr** (write) are activated. For a read access, the control signals **cs** and **rd** (read) are activated and the register places its stored value on the data bus.



The register is composed of 8 memory elements (latch) like the one in the adjacent figure. If the input **ld** (load) is active, the value d_{In} (data in) is stored in the element and this brings it directly to its output d_{Out} (data out). The storage element retains the value unchanged as long as **ld** does not remain active.
Use the generated component to create the schema of an 8-bit read/write memory.



lst/hiz-05