



# Memory elements and Flip-flops

## Exercises Digital Design

### Solution vs. Hints:



While not every response provided herein constitutes a comprehensive solution, some serve as helpful hints intended to guide you toward discovering the solution independently. In certain instances, only a portion of the solution is presented.

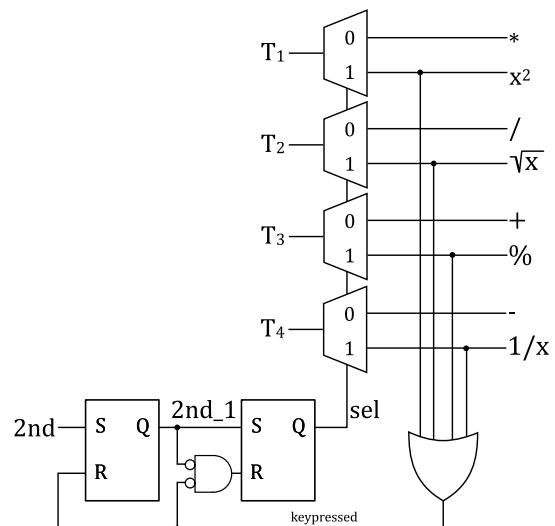
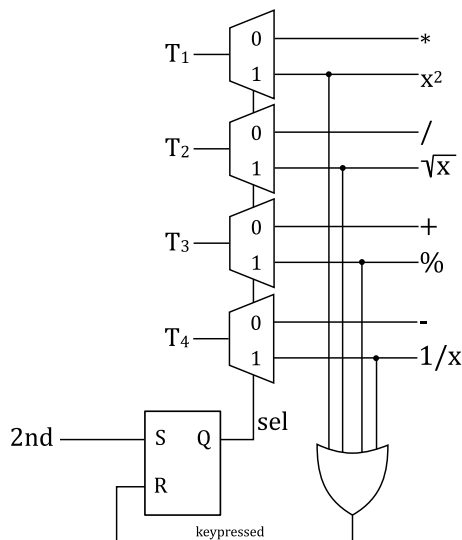
## 1 | LAT - Memory elements

### 1.1 Anti-bounce circuit

Switch on which one side is **Reset** and the other **Set**.

*lat/memory-01*

### 1.2 Key selection



*lat/memory-02*



### 1.3 Analysis of a memory element

It is a SR latch with inverted inputs

*lat/memory-03*

### 1.4 Memory Element

$$\begin{cases} g = 0 \Rightarrow s_n = 1 = r_n \Rightarrow \text{memorization} \\ g = 1 \Rightarrow \text{SR latch (set or reset)} \end{cases} \quad (1)$$

*lat/memory-04*

### 1.5 Synchronisation

Idea: Update the signal only at  $\begin{cases} \text{clk}=1 & \Rightarrow \text{D-Latch} \\ \text{rising\_edge} & \Rightarrow \text{D-FF} \end{cases}$

*lat/memory-05*



## 2 | LAT - Flip-flops

### 2.1 Detection of Transitions

Using a D-FF as delay element and compare the 2 signals together (XOR-2).

*lat/flipflop-01*

### 2.2 Shift Register

The output  $Y$  is the same as the input  $X$  with a delay of 4 clock period since there are 4 D-FF in the circuit.

*lat/flipflop-02*

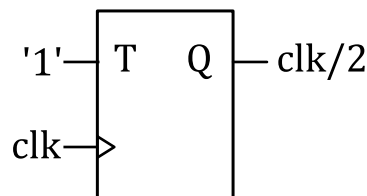
### 2.3 Flipflop, denoted by its characteristic equation

You need a D-FF and a multiplexer

*lat/flipflop-03*

### 2.4 Divider by 2

Only the solution for  $\frac{\text{clk}}{2}$  is shown.



*lat/flipflop-04*

### 2.5 Replacement of a Flip-Flop

#### 2.5.1.1 Equation

$$E : Q^+ = \overline{E}Q + ED$$

$$T : Q^+ = T \oplus Q \Rightarrow \overline{T}Q + T\overline{Q} \Rightarrow T\overline{Q} + \overline{T}Q \quad (2)$$

#### 2.5.1.2 Table

$T$	$Q$	$Q^+$	$E$	$D$
0	0	0	0	-
0	0	1	1	0
0	1	1	0	-
0	1	0	1	1
1	0	1	1	1
1	1	0	1	0

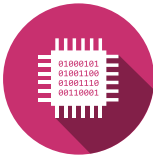
Two variants are possible:

$$\begin{cases} E = 1, D = T \oplus Q \\ E = T, D = \overline{Q} \end{cases} \quad (3)$$

*lat/flipflop-05*

### 2.6 Shift Register

The real question is build a D-FF with a T-FF (see ex.Section 2.5 for the flipflop and ex.Section 2.2 for the shift register)

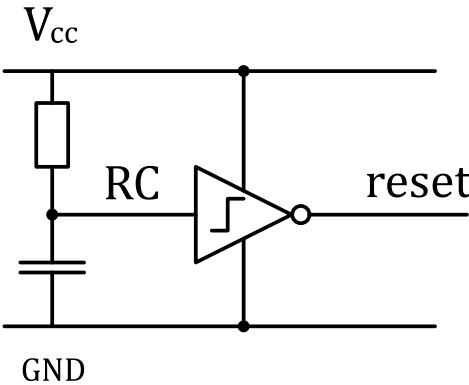


lat/flipflop-06

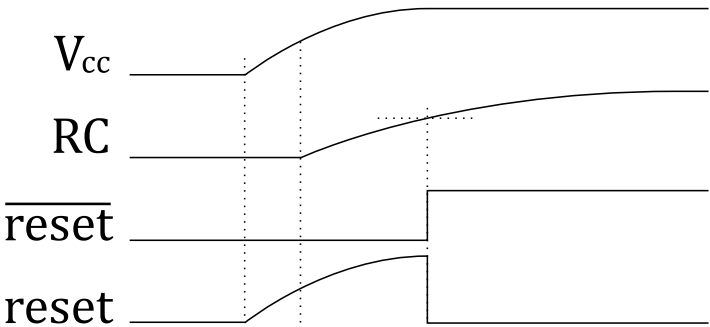
2.7 Asynchronous Zeroing

- RC-Circuit will be powered up with a delay
- Trigger converts the analog signal to a digital signal

Circuit

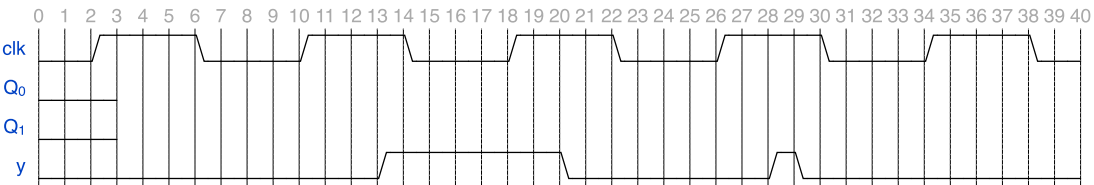


Schema



lat/flipflop-07

2.8 Asynchronous Circuit



lat/flipflop-08