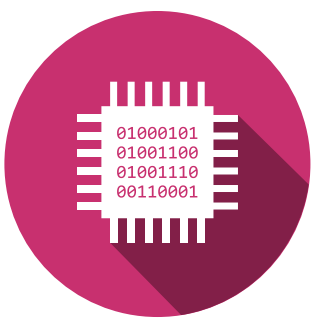
Hes·so VALAIS WALLIS
Haute Ecole d'Ingénierie
Hochschule für Ingenieurwissenschaften

Conception numérique (DiD)

Eléments de mémoire et bascule

LAT

Filière Systèmes industriels
Filière Energie et techniques environmentales
Filière Informatique et systèmes de communications



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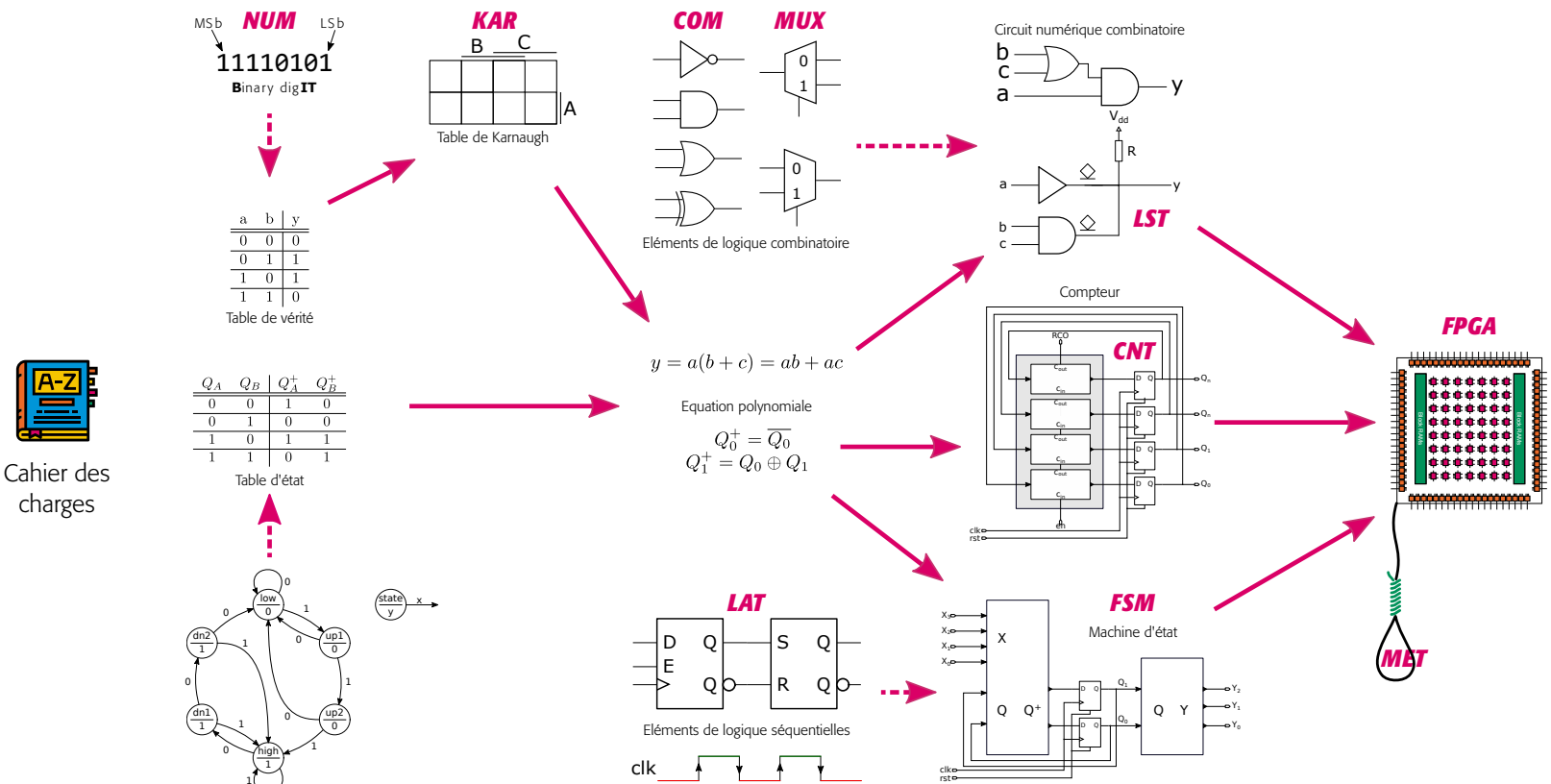
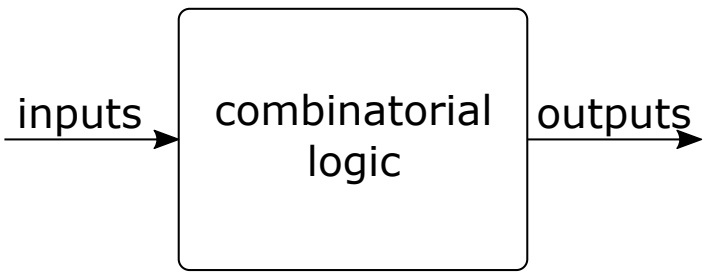
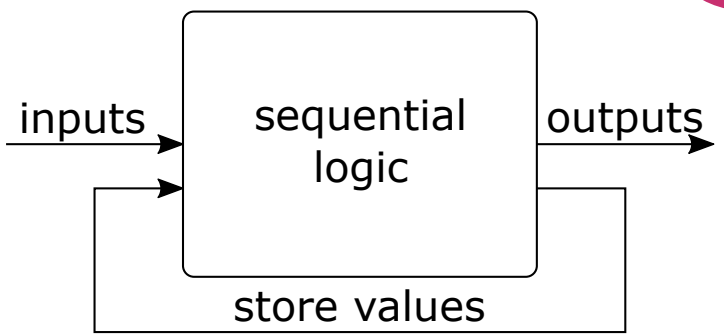
Christophe Bianchi christophe.bianchi@hevs.ch
François Corthay francois.corthay@hevs.ch

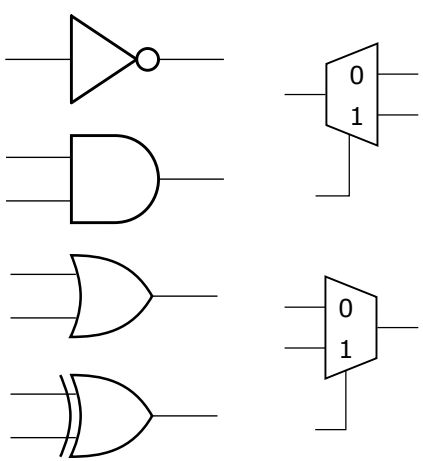
Situation du thème dans le cours

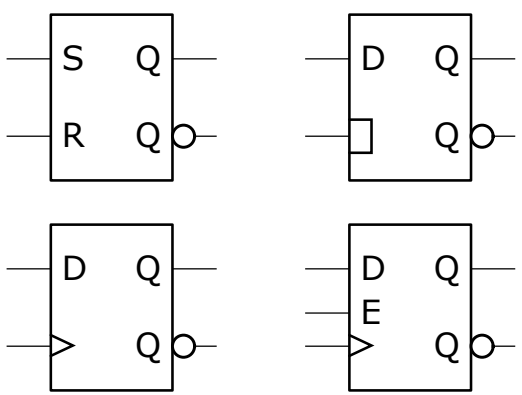


Logique combinatoire et séquentielle

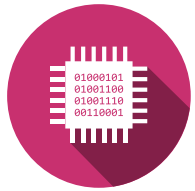








Contenu

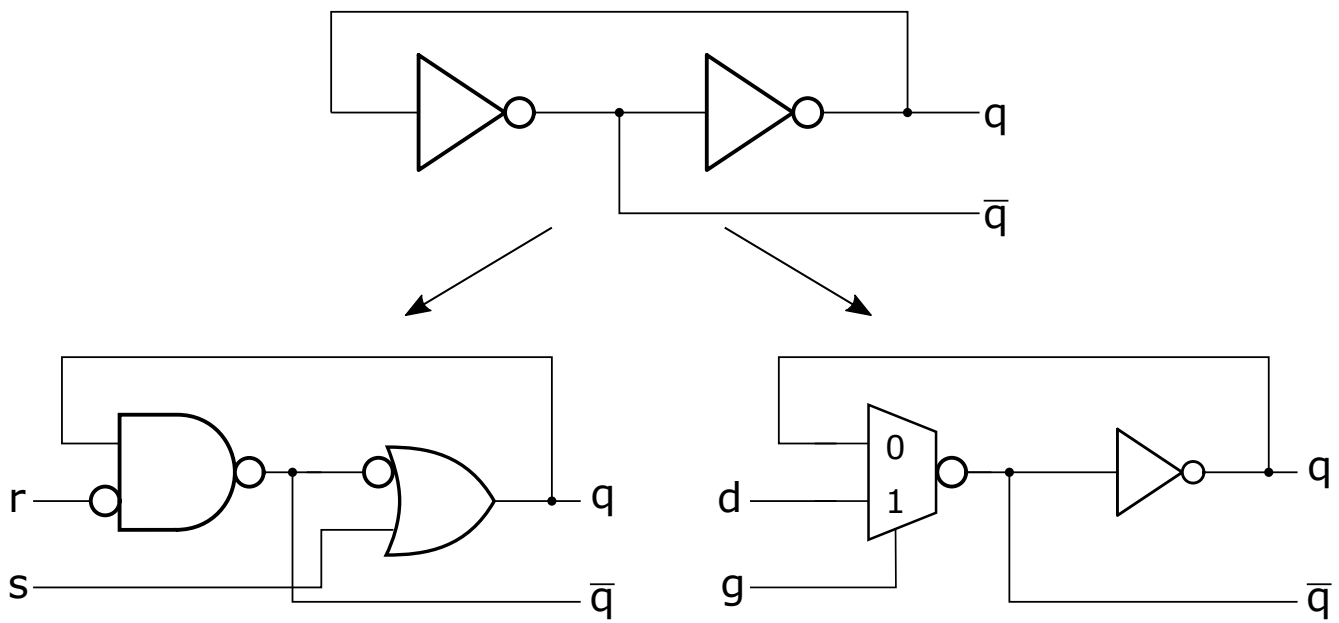


- **Eléments de mémoire (Latch)**
  - Elément de mémoire SR (SR-Latch)
  - Equation caractéristique
  - Elément de mémoire D (D-Latch)

- Bascules (FlipFlop)

Elément de mémoire SR

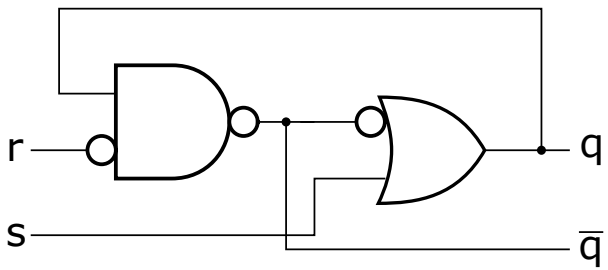
SR-Latch

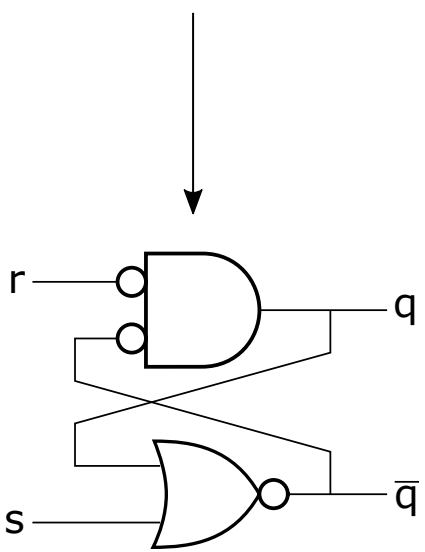


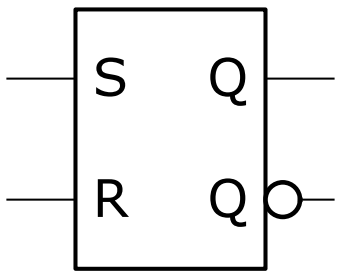
2 inverseurs couplés forment un élément de mémoire

Elément de mémoire SR

SR-Latch (set-reset)





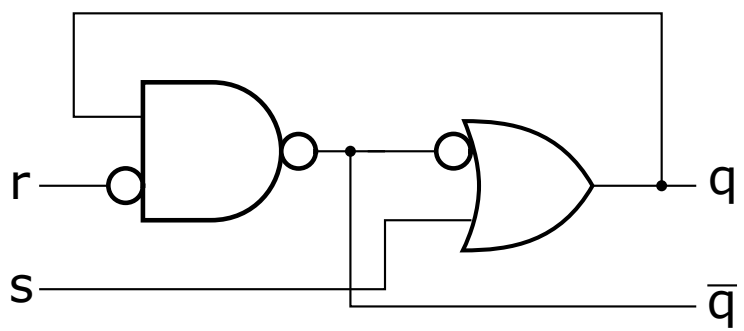


s	r	q	qn	Fonction
0	0	Inchangé		Mémorisation
0	1	0	1	Mise à 0 (reset)
1	0	1	0	Mise à 1 (set)
1	1	0	0	Interdit

Elément de mémoire SR

SR-Latch équation caractéristique

L’équation caractéristique décrit la fonctionnalité de l’élément de mémoire

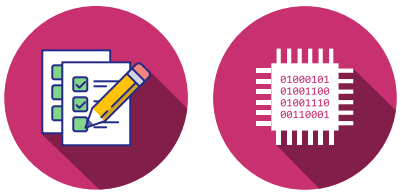


$$q = s + \overline{r}q$$

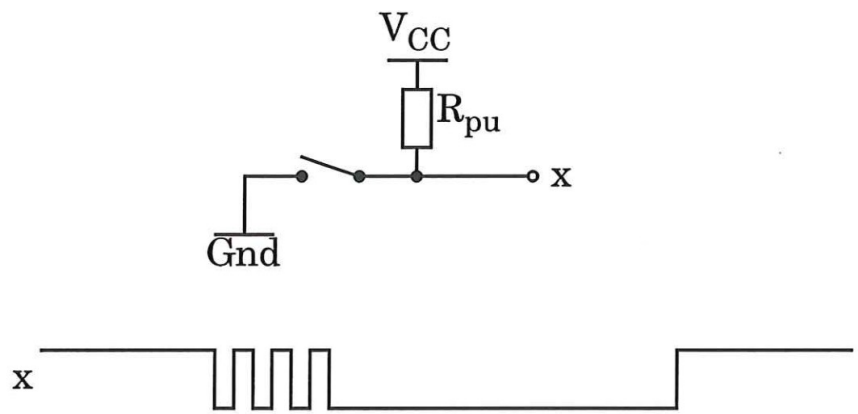
« q » des 2 côtés de l’équation montre la boucle de mémorisation (q=q pour s=0 et r=0)

Exercise 1.1 *(lat/memory-01)*

Circuit anti-rebonds

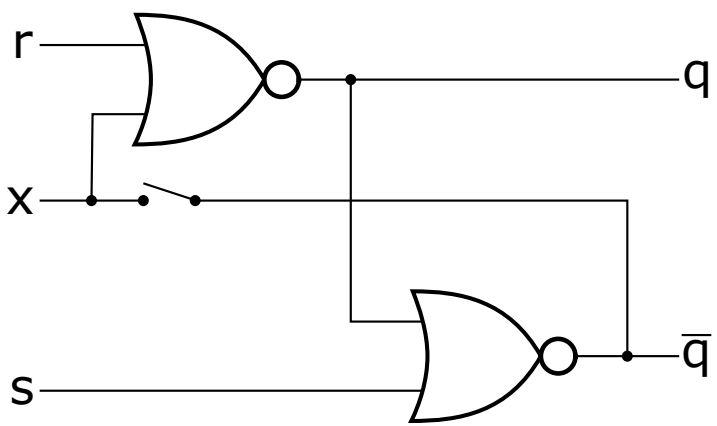


A l'aide d'un commutateur et d'un élément de mémoire, concevoir un circuit qui fournit un signal exempt de rebonds.



Elément de mémoire SR

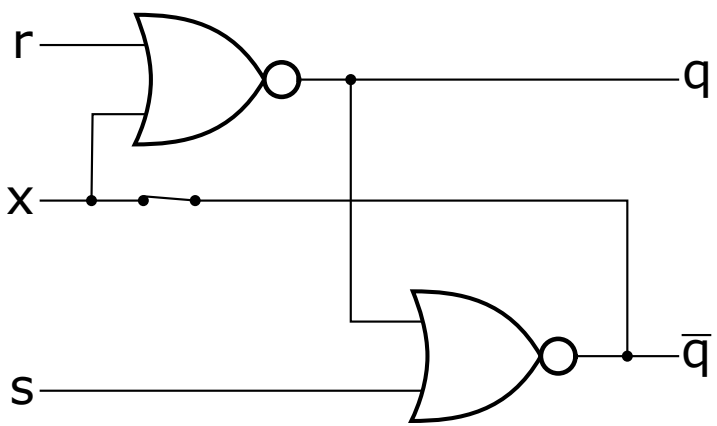
Analyse de fonctionnement (modèle combinatoire)



s	r	x	q	qn	
0	0	0	1	0	
0	0	1	0	1	
0	1	0	0	1	
0	1	1	0	1	
1	0	0	1	0	
1	0	1	0	0	
1	1	0	0	0	
1	1	1	0	0	

Elément de mémoire SR

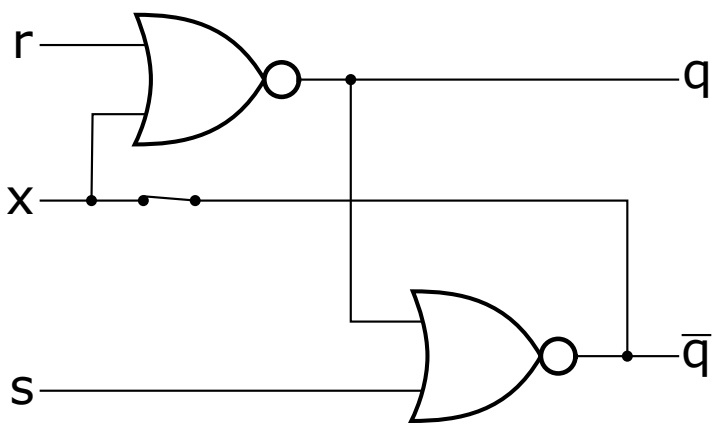
Analyse de fonctionnement (modèle combinatoire)



s	r	x	q	qn	Valide
0	0	0	1	0	✓
0	0	1	0	1	✓
0	1	0	0	1	×
0	1	1	0	1	✓
1	0	0	1	0	✓
1	0	1	0	0	×
1	1	0	0	0	✓
1	1	1	0	0	×

Elément de mémoire SR

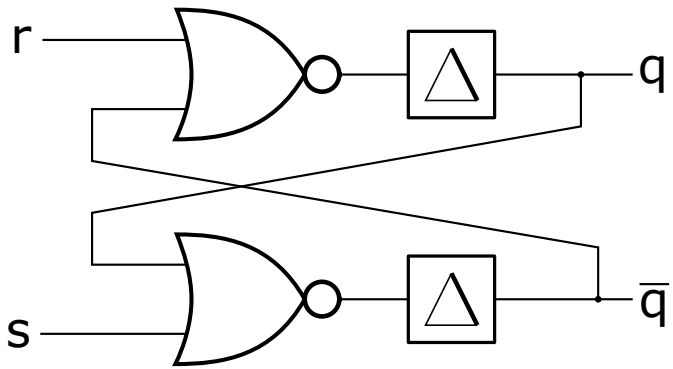
Analyse de fonctionnement (modèle combinatoire)

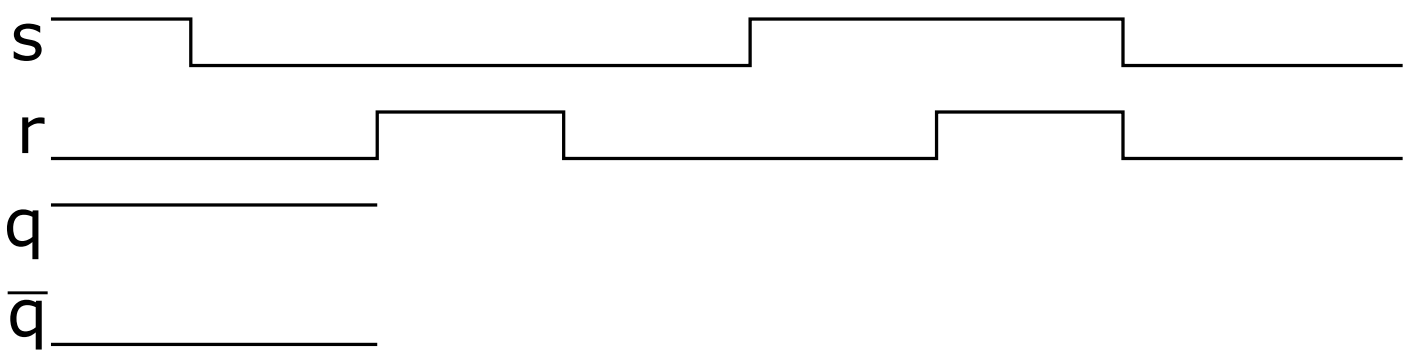


s	r		q	qn	Opération
0	0		1	0	Mémorisation
0	0		0	1	
0	1		0	1	reset
1	0		1	0	set
1	1		0	0	Interdit

Elément de mémoire SR

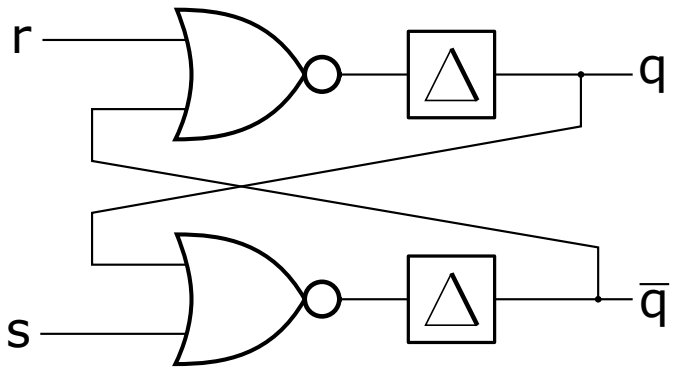
Analyse de fonctionnement (modèle temporel)

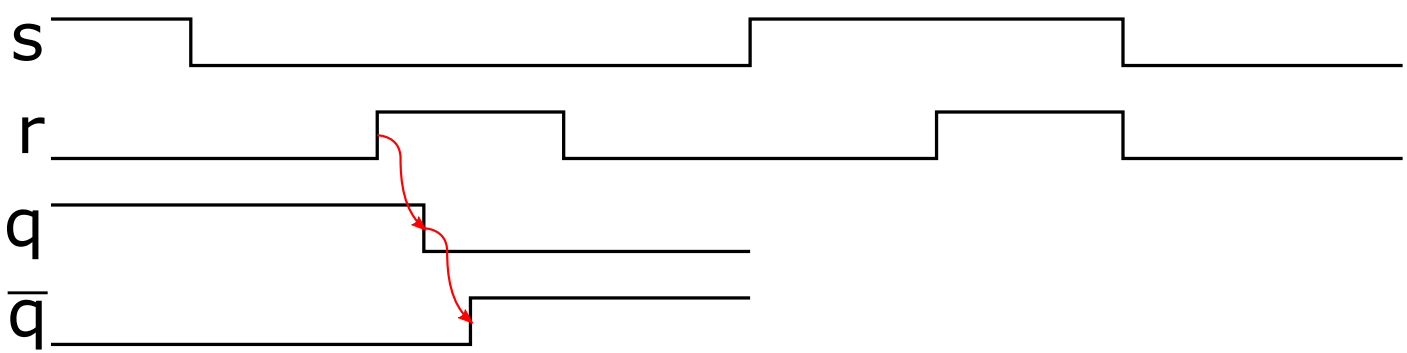




Elément de mémoire SR

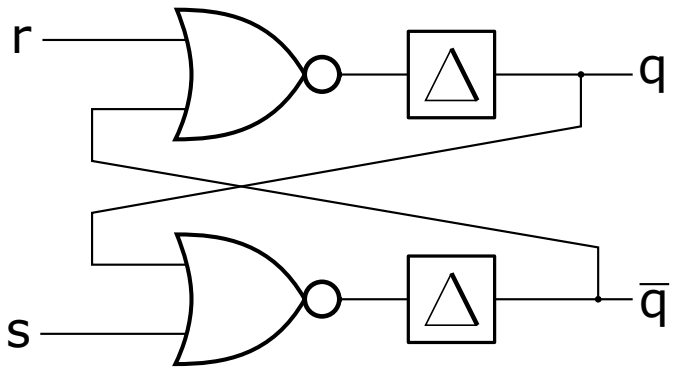
Analyse de fonctionnement (modèle temporel)

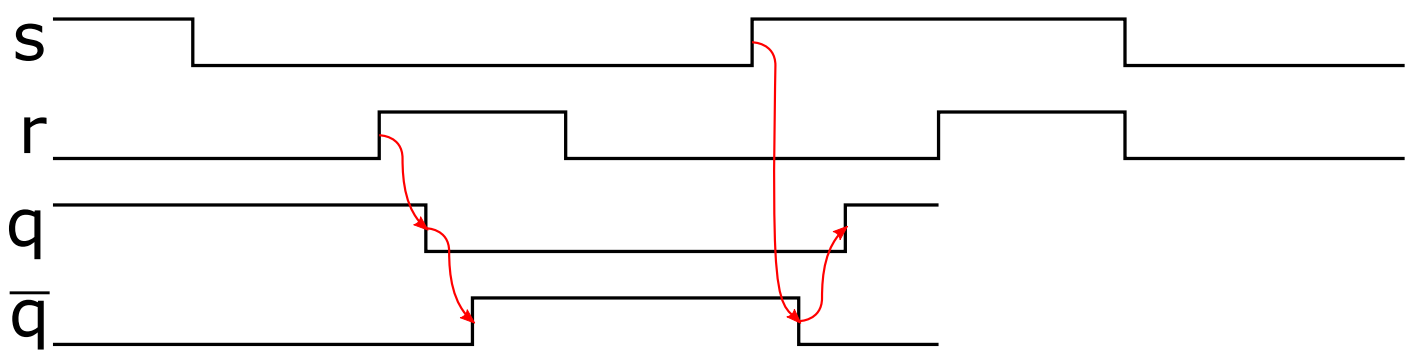




Elément de mémoire SR

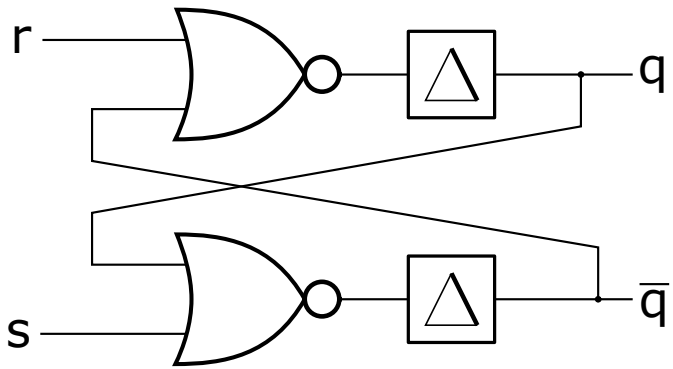
Analyse de fonctionnement (modèle temporel)

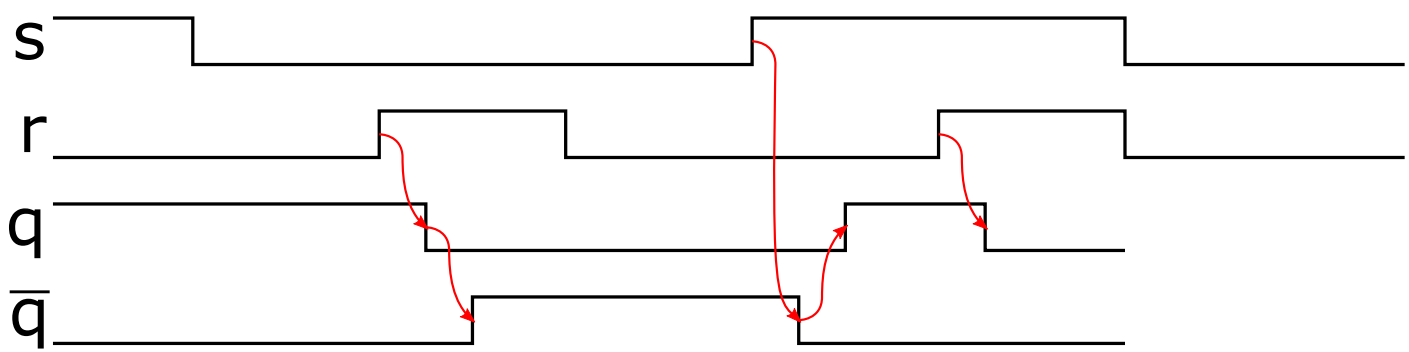




Elément de mémoire SR

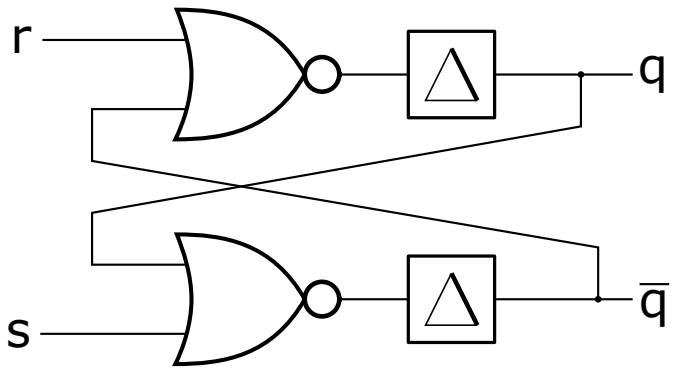
Analyse de fonctionnement (modèle temporel)

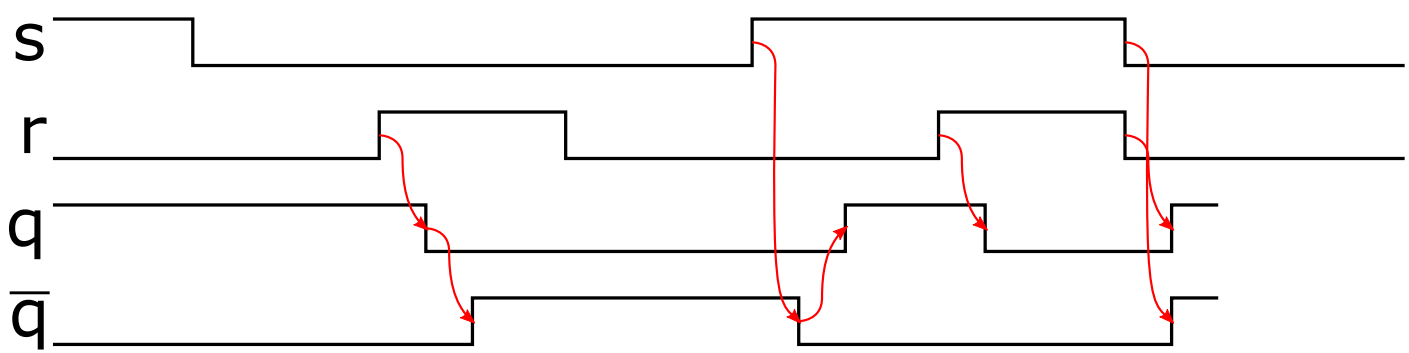




Elément de mémoire SR

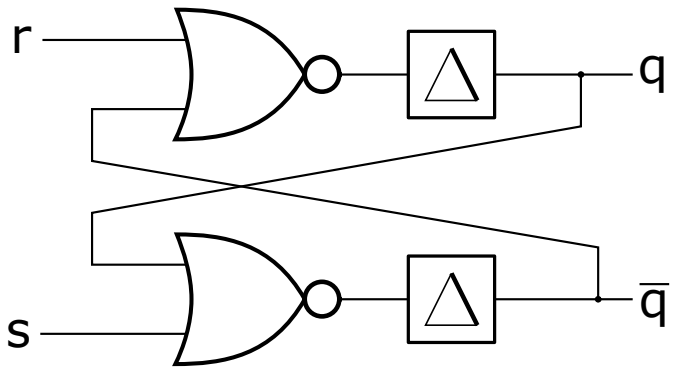
Analyse de fonctionnement (modèle temporel)

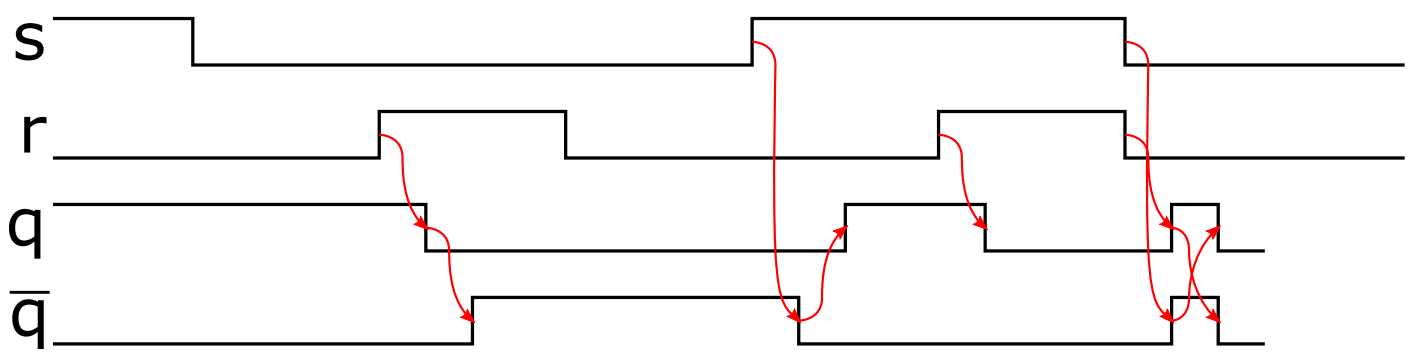




Elément de mémoire SR

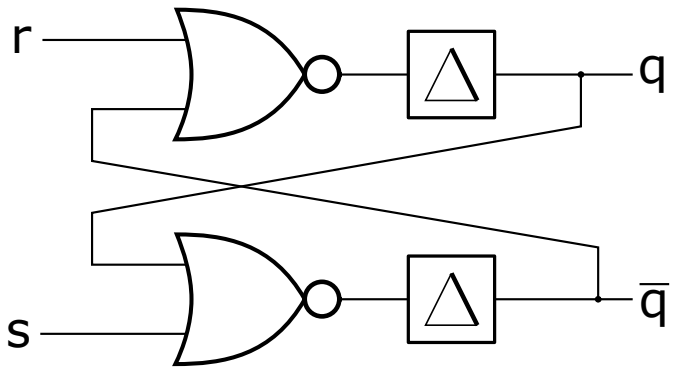
Analyse de fonctionnement (modèle temporel)

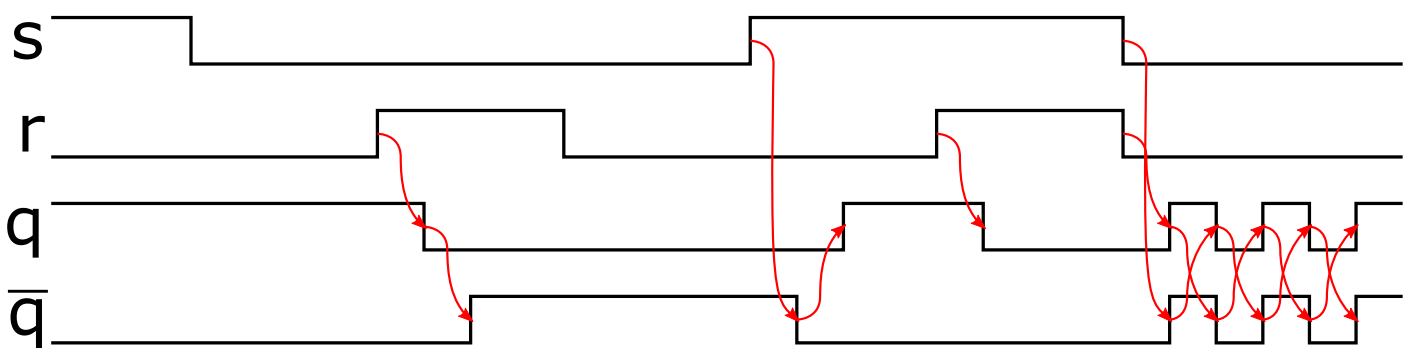




Elément de mémoire SR

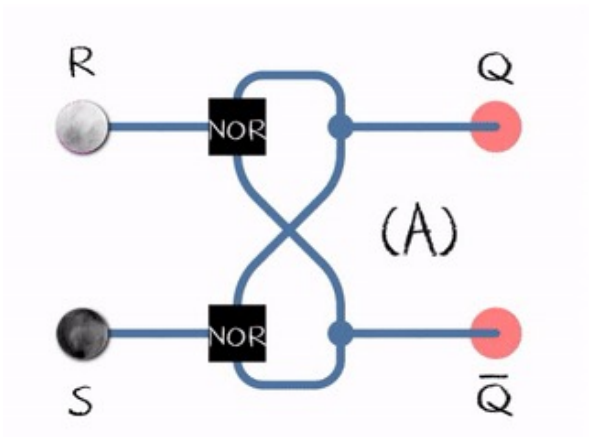
Analyse de fonctionnement (modèle temporel)

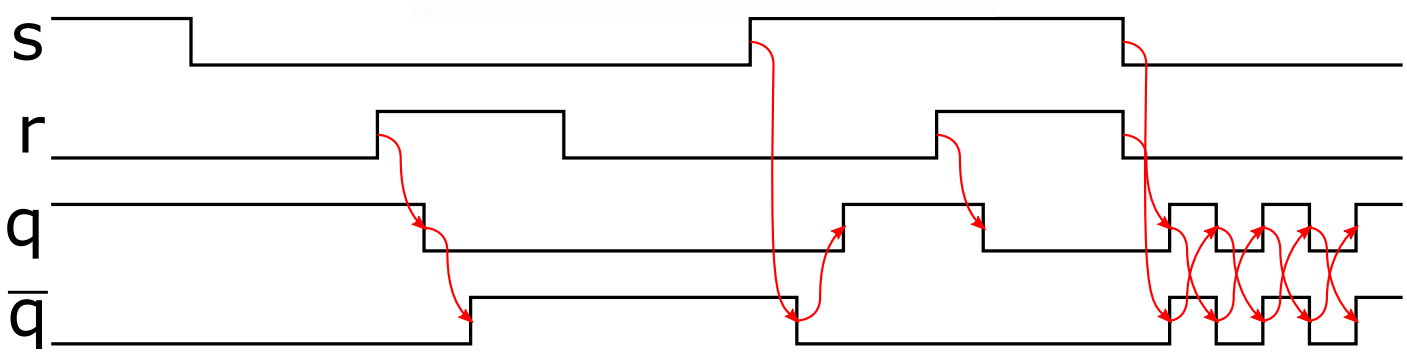




Elément de mémoire SR

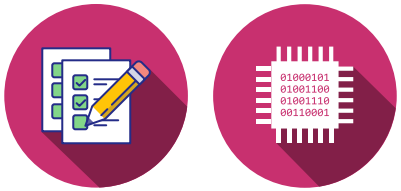
Analyse de fonctionnement (modèle temporel)





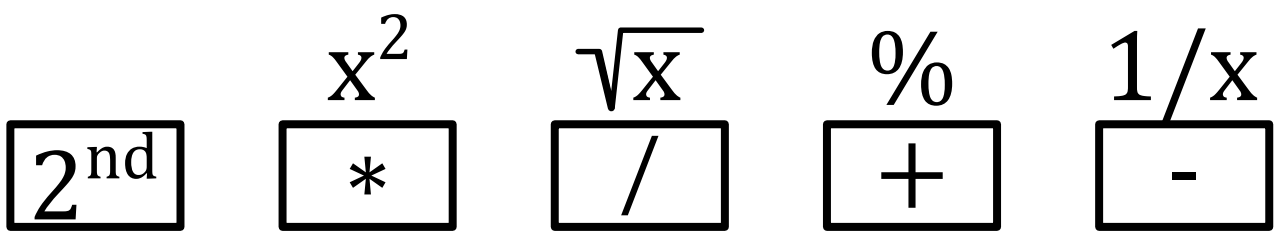
Exercise 1.2 *(lat/memory-02)*

Sélection de touches

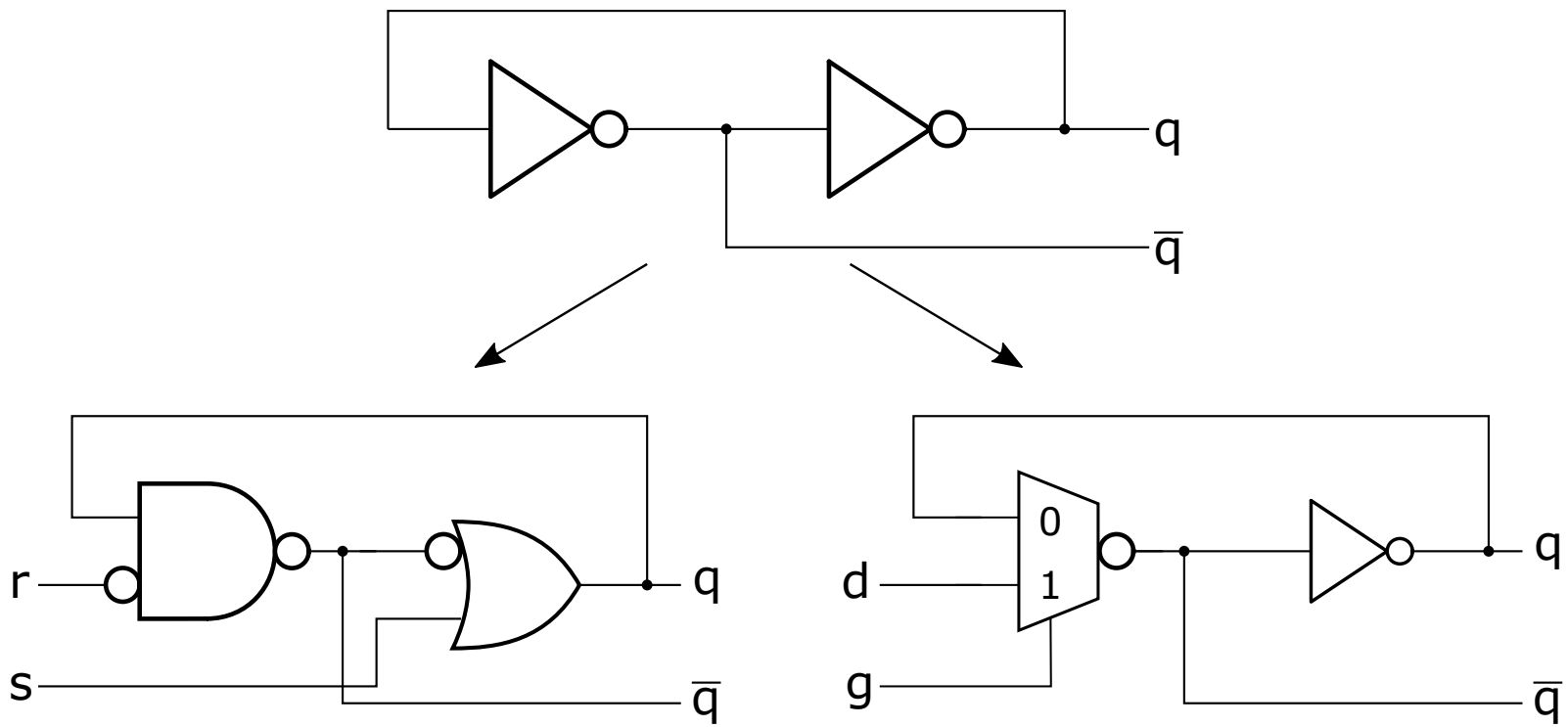


Un clavier de calculatrice comporte 5 touches pour sélectionner une opération parmi 8. L'opération x^2 est sélectionnée en appuyant sur la touche « 2^{nd} » puis sur la touche de multiplication $*$.

Concevoir un circuit à 8 sorties qui délivre une impulsion sur la sortie correspondant à la fonction désirée.

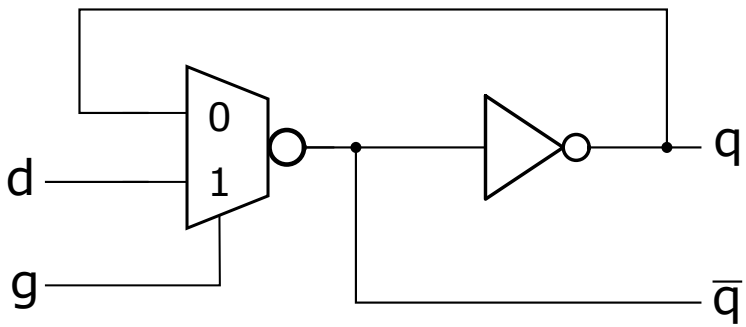


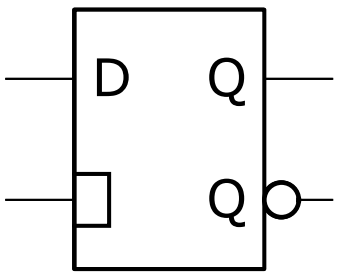
Eléments de mémoire



Eléments de mémoire

Eléments de mémoire D (D-Latch)



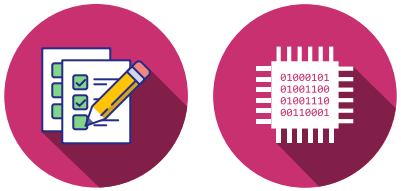


g	d	q	qn	Fonction
0	0	inchangé		Mémorisation
0	1			
1	0	0	1	Chargement de D
1	1	1	0	

$$q = gd + \overline{g}q$$

Exercise 1.5 *(lat/memory-05)*

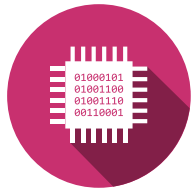
Synchronisation



Un système commandé par une horloge, génère un signal de sortie qui varie uniquement quand le signal d'horloge est à '0'.

Concevoir un circuit qui retarde ce signal jusqu'à ce que le signal d'horloge soit à '1'.

Contenu

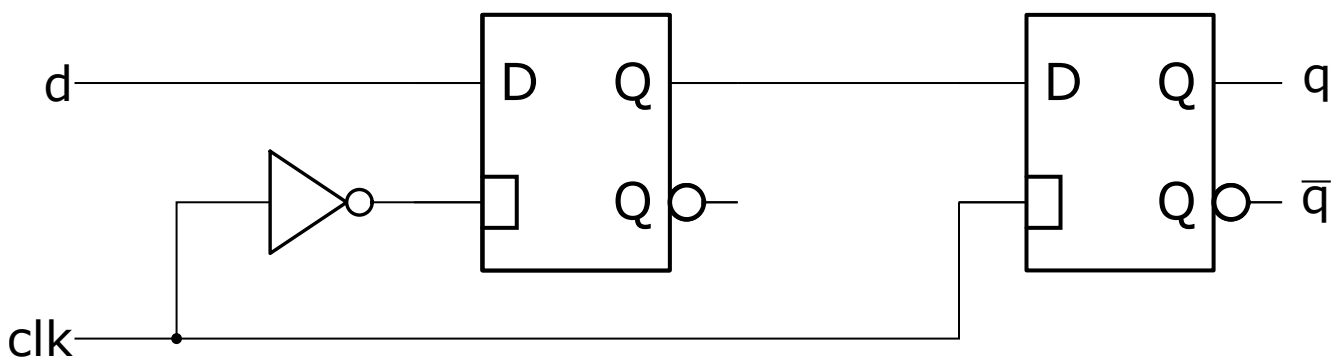


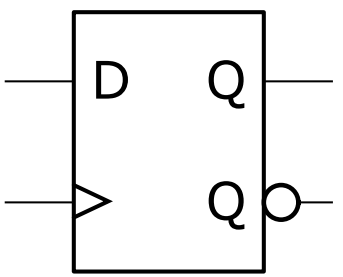
- Eléments de mémoire (Latch)
- **Bascules (FlipFlop)**
  - Bascule D (D-FlipFlop)
  - Equation caractéristique
  - Bascule SR (SR-FlipFlop)
  - Bascule E (E-FlipFlop)
  - Bascule T (T-FlipFlop)
  - Entrées asynchrones

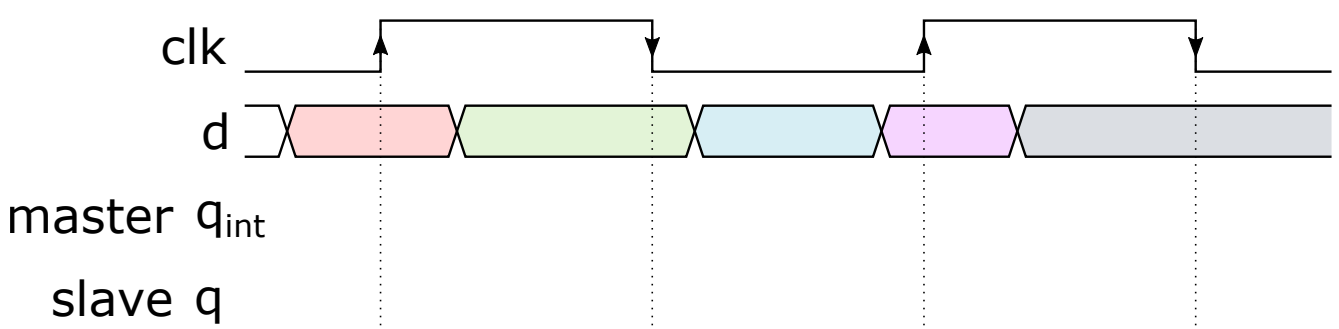
Bascules (FlipFlops)

Bascule D (D-FlipFlop)

Master-Slave Latch



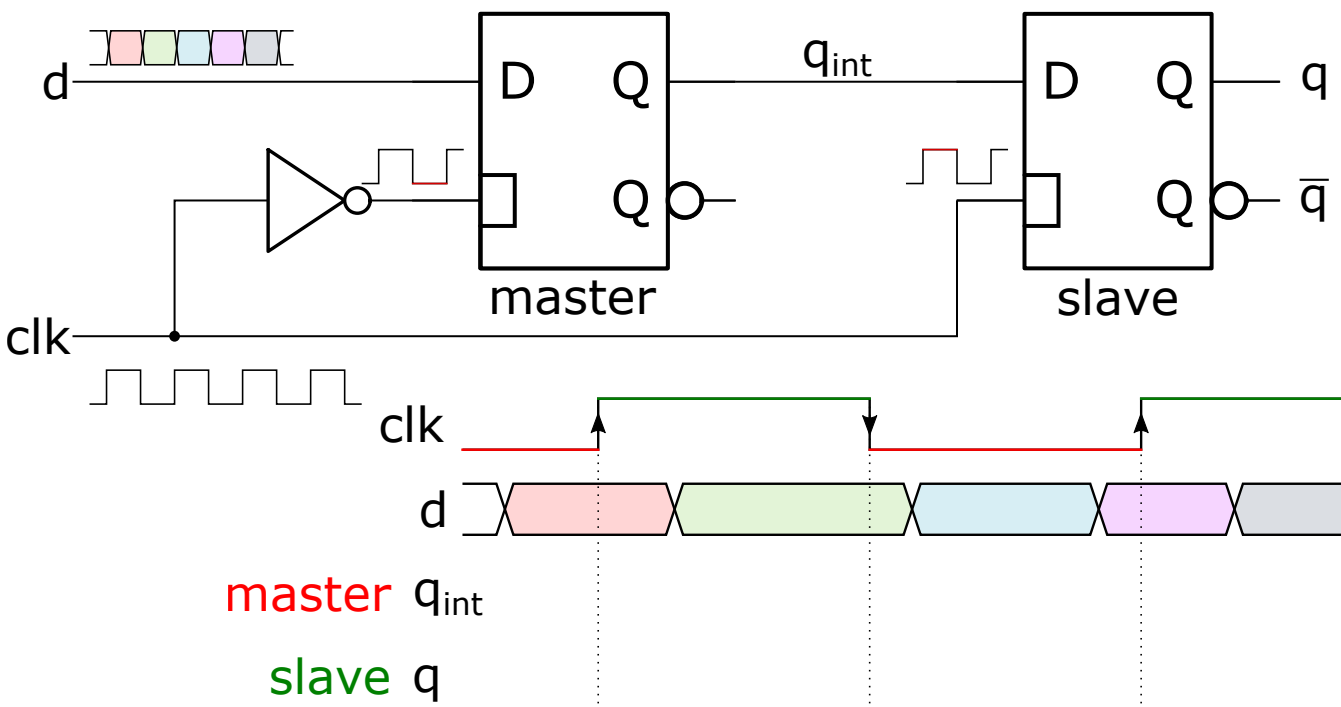


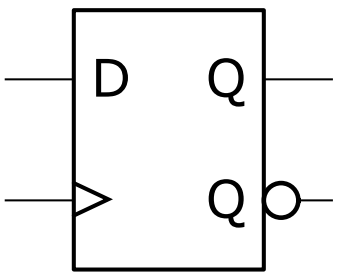


Bascules (FlipFlops)

Bascule D (D-FlipFlop)

Master-Slave Latch

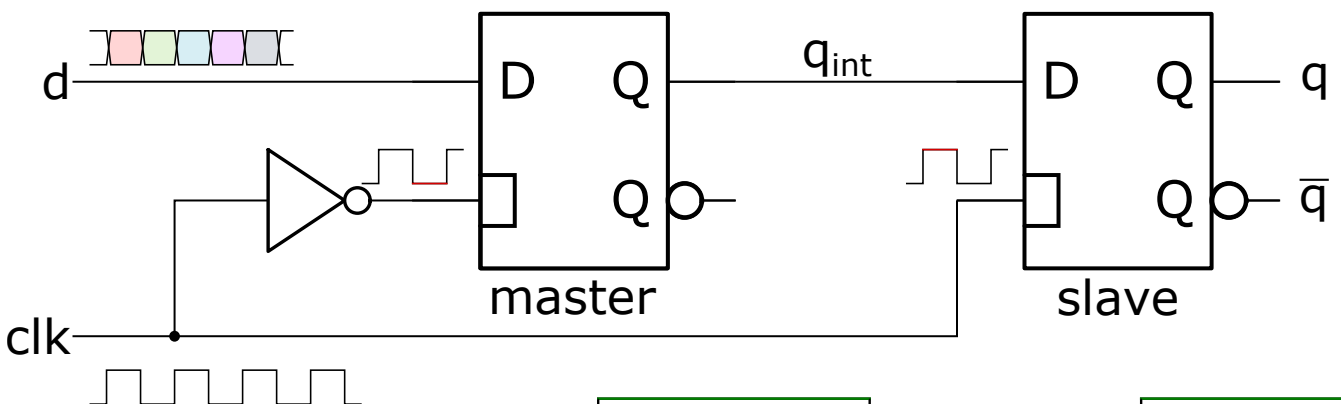


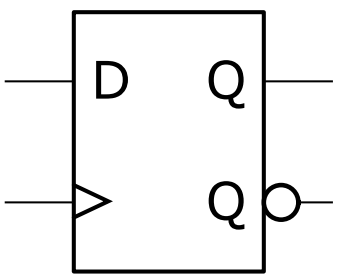


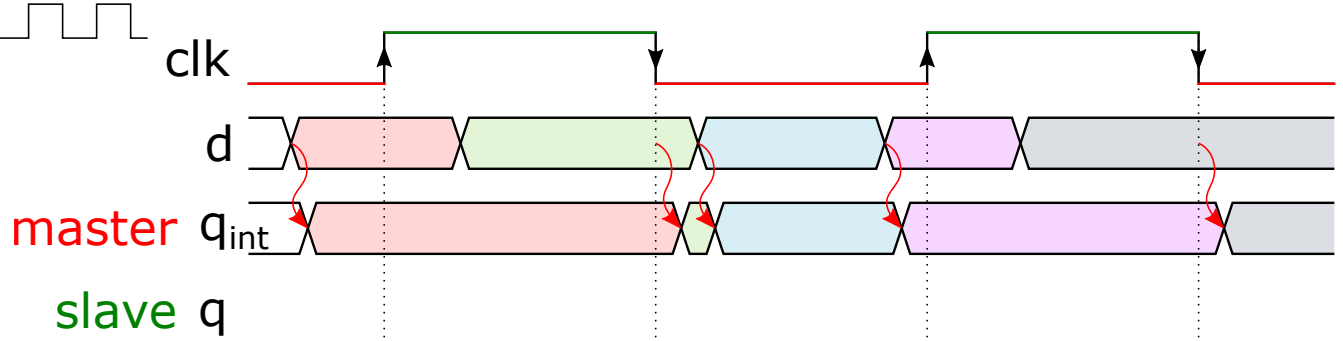
Bascules (FlipFlops)

Bascule D (D-FlipFlop)

Master-Slave Latch



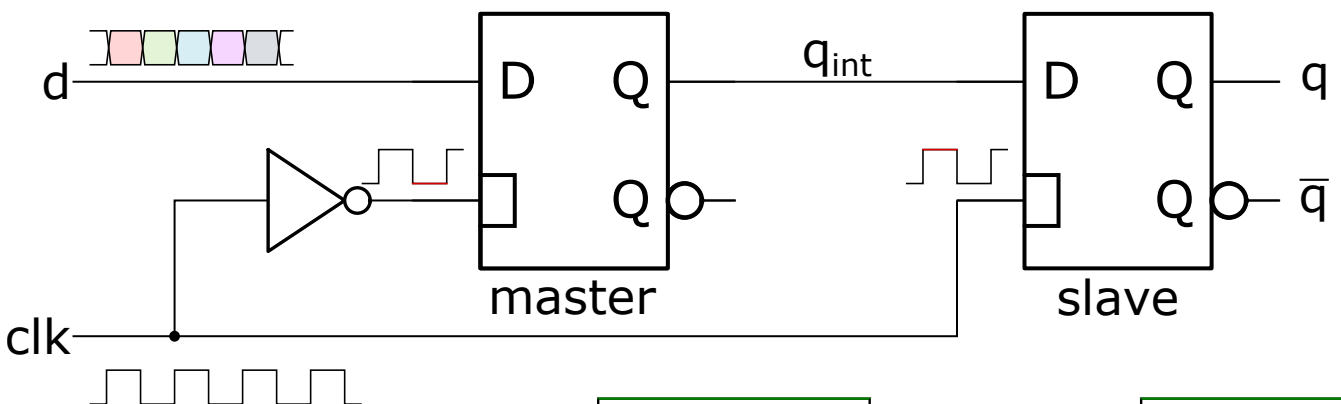


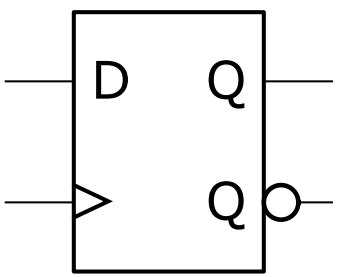


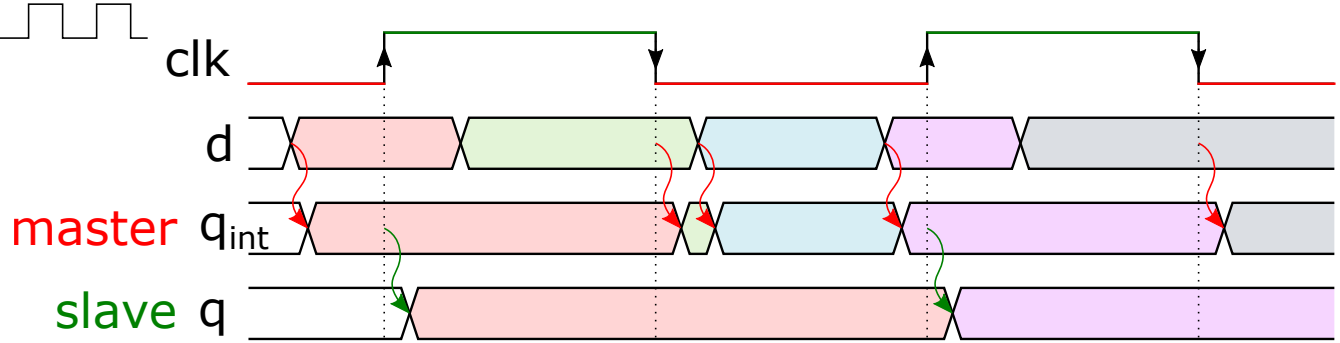
Bascules (FlipFlops)

Bascule D (D-FlipFlop)

Master-Slave Latch

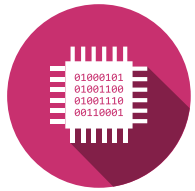




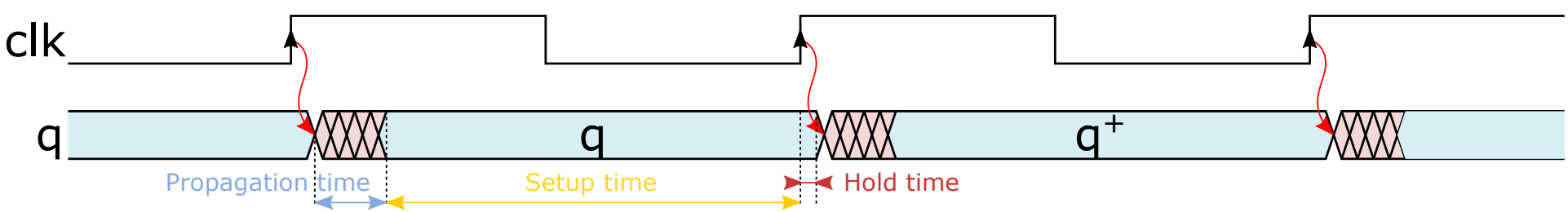


Bascules (FlipFlops)

Bascule D (D-FlipFlop)

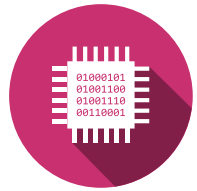


- Tous les signaux sont stables avant le flanc montant de l'horloge (respect du setup time et hold time)
- Après ce flanc montant, toutes les sorties des bascules changent, avec des retards divers (délai de propagation)
- La prochaine valeur que prend la sortie q au prochain flanc d'horloge se note "q+" (donnée par l'équation et le circuit situé sur l'entrée de la bascule)

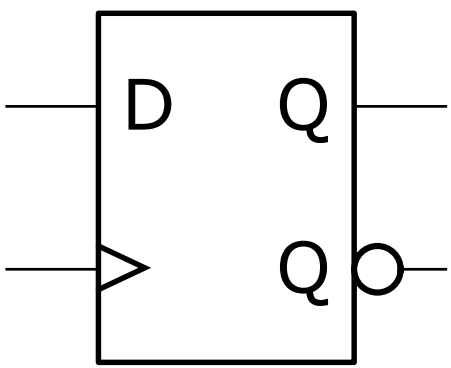


Bascule D (D-FlipFlop)

Equation caractéristique



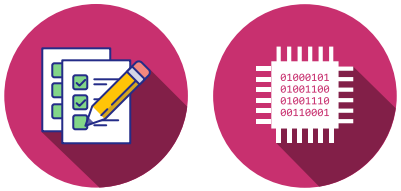
D	Q	Q^+	Fonction
0	0	0	Chargement de la valeur D au flanc montant de l'horloge
0	1	0	
1	0	1	
1	1	1	



$$q^+ = d$$

Exercise 2.1 *(lat/flipflop-01)*

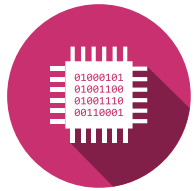
Détection des transitions



A l'aide d'une bascule D et de portes logiques, concevez un circuit qui détecte les transitions de son signal d'entrée.

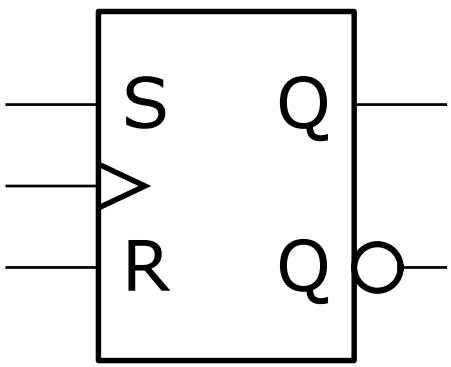
Bascules (FlipFlops)

Bascule SR (SR-FlipFlop)



Remplacée aujourd'hui par la bascule D

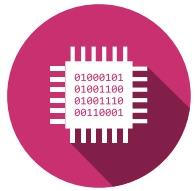
S	R	Q^+	Fonction
0	0	Q	Mémorisation
0	1	0	reset
1	0	1	set
1	1	1	-



$$q^+ = s + \overline{r}q$$

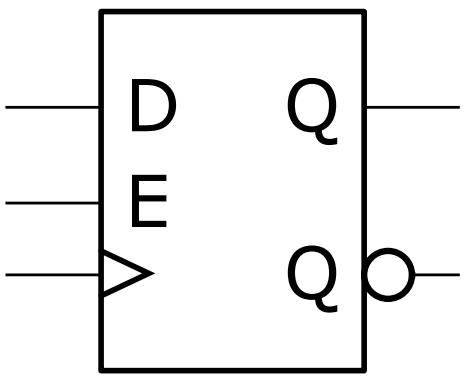
Bascules (FlipFlops)

Bascule E (E-FlipFlop)



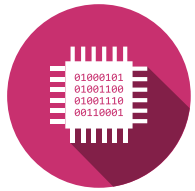
Permet le fonctionnement à différentes vitesses

E	D	Q^+	Fonction
0	0	Q	Mémorisation
0	1		
1	0	0	Chargement de D (Echanillonnage)
1	1	1	



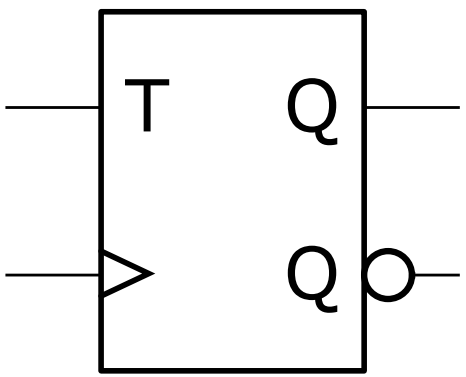
$$q^+ = ed + \overline{e}q$$

Bascules (FlipFlops)
Bascule T (T-FlipFlop)



Permet de simplifier le circuit d'un compteur

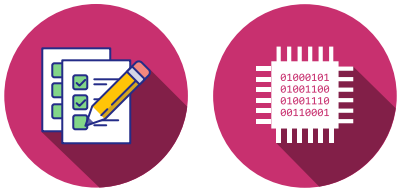
T	Q^+	Fonction
0	Q	Mémorisation
1	$\bar{Q}$	Inversion



$$q^+ = t \oplus q$$

Exercise 2.6 *(lat/flipflop-06)*

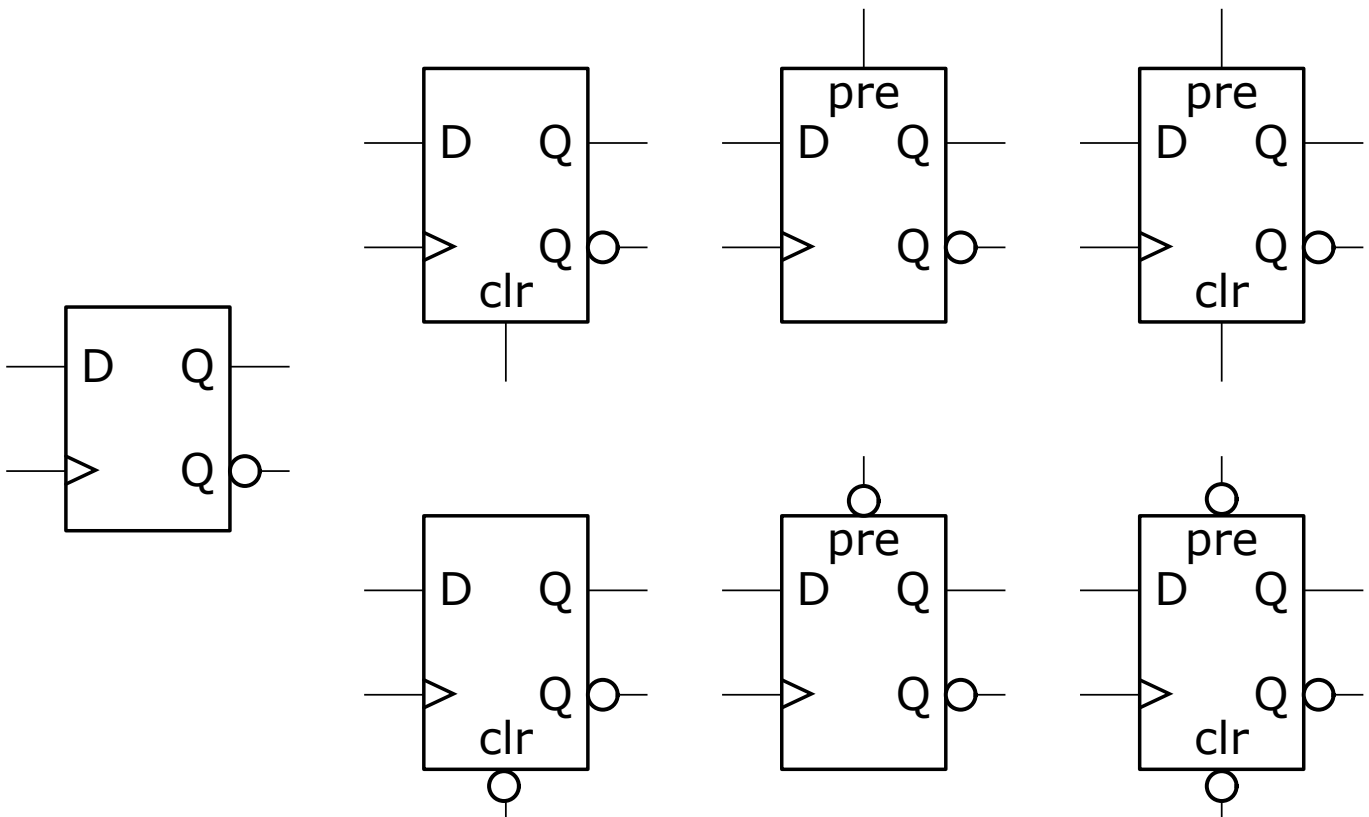
Registre de décalage



Réaliser un registre à décalage de 4 bits à l'aide de T-FlipFlop

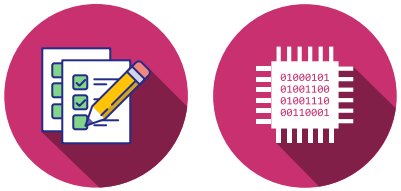
Bascules (FlipFlops)

Entrées asynchrones



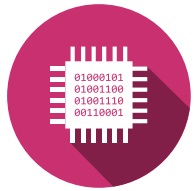
Exercise 2.7 *(lat/flipflop-07)*

Mise à zéro asynchrone



A l'aide d'un circuit RC et de portes logiques, créez un circuit d'initialisation des bascules à la mise sous tension de l'électronique.

Références

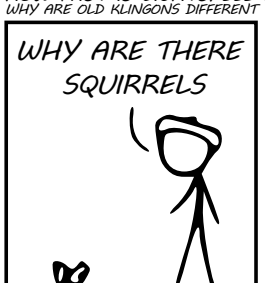


- [Wak00] (anglais) Présentation très complète
- [Kün97] (allemand) Bonne présentation
- [Max95] (français) Bonne présentation

QUESTIONS

CAN BE ASKED BY ANYONE ANYTIME

WHY ARE THERE MIRRORS ABOVE BEDS
WHY DO I SAY UH
WHY IS SEA SALT BETTER
WHY ARE THERE TREES IN THE MIDDLE OF FIELDS
WHY IS THERE NOT A POKEMON MMO
WHY IS THERE LAUGHING IN TV SHOWS
WHY ARE THERE DOORS ON THE FREEWAY
WHY ARE THERE SO MANY SVCHOST·EXE RUNNING
WHY AREN'T ANY COUNTRIES IN ANTARCTICA
WHY ARE THERE SCARY SOUNDS IN MINECRAFT
WHY IS THERE KICKING IN MY STOMACH
WHY ARE THERE TWO SLASHES AFTER HTTP
WHY ARE THERE CELEBRITIES
WHY DO SNAKES EXIST
WHY DO OYSTERS HAVE PEARLS
WHY ARE DUCKS CALLED DUCKS
WHY DO THEY CALL IT THE CLAP
WHY ARE KYLE AND CARTMAN FRIENDS
WHY IS THERE AN ARROW ON AANG'S HEAD
WHY ARE TEXT MESSAGES BLUE
WHY ARE THERE MUSTACHES ON CLOTHES
WHY WUBA LUBBA DUB DUB MEANING
WHY IS THERE A WHALE AND A POT FALLING
WHY ARE THERE SO MANY BIRDS IN SWISS
WHY IS THERE SO LITTLE RAIN IN WALLIS
WHY IS WALLIS WEATHER FORECAST ALWAYS WRONG
WHY ARE THERE MALE AND FEMALE BIKES
WHY ARE THERE BRIDESMAIDS
WHY DO DYING PEOPLE REACH UP
HOW FAST IS LIGHTSPEED
WHY ARE OLD KLINGONS DIFFERENT



WHY ARE THERE DINOSAUR GHOSTS
WHY IS THERE HELL IF

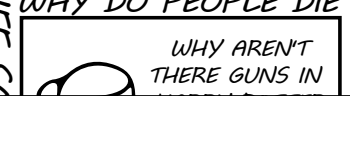
WHY DO IGUANAS DIE
WHY IS THERE CAFFEINE IN MY SHAMPOO
WHY HAVE DINOSAURS NO FUR
WHY DO TWINS HAVE DIFFERENT FINGERPRINTS
WHY ARE SWISS AFRAID OF DRAGONS
WHY AREN'T ECONOMISTS RICH
WHY DO AMERICANS CALL IT SOCCER
WHY ARE MY EARS RINGING
WHY IS 42 THE ANSWER TO EVERYTHING
WHY CAN'T NOBODY ELSE LIFT THORS HAMMER
WHY IS MARVIN ALWAYS SO SAD
WHY ARE THERE ANTS IN MY LAPTOP
WHY IS EARTH TILTED
WHY IS SPACE BLACK
WHY IS OUTER SPACE SO COLD
WHY ARE THERE PYRAMIDS ON THE MOON
WHY IS NASA SHUTTING DOWN
WHY ARE THERE TINY SPIDERS IN MY HOUSE
WHY DO SPIDERS COME INSIDE
WHY ARE THERE HUGE SPIDERS IN MY HOUSE
WHY ARE THERE LOTS OF SPIDERS IN MY HOUSE
WHY ARE THERE SPIDERS IN MY ROOM
WHY ARE THERE SO MANY SPIDERS IN MY ROOM
WHY DO SPYDER BITES ITCH
WHY IS DYING SO SCARY
WHY IS THERE NO GPS IN LAPTOPS
WHY DO KNEES CLICK

WHY ARE THERE FEMALE

WHY IS HTTPS CROSSED OUT IN RED
WHY IS THERE A LINE THROUGH HTTPS
WHY IS THERE A RED LINE THROUGH HTTPS ON TWITTER
WHY IS HTTPS IMPORTANT

WHY IS YKK ON ALL ZIPPERS
WHY ARE THERE WEEKS
WHY DO I FEEL DIZZY
WHY IS THERE A SWARM OF ANTS
WHY IS THERE PILEGRIM
WHY IS THERE LAVA
WHY ARE THERE SO MANY CROWS IN ROCHESTER
WHY IS TO BE OR NOT TO BE FUNNY
WHY DO CHILDREN GET CANCER
WHY IS POSEIDON ANGRY WITH ODYSSEUS
WHY IS THERE ICE IN SPACE
WHY IS THERE AN OWL IN MY BACKYARD
WHY IS THERE AN OWL OUTSIDE MY WINDOW
WHY IS THERE AN OWL ON THE DOLLAR BILL
WHY DO OWLS ATTACK PEOPLE
WHY ARE FPGA's EVERYWHERE
WHY ARE THERE HELICOPTERS CIRCLING MY HOUSE
WHY ARE THERE GODS
WHY ARE THERE TWO SPOCKS
WHAT IS https://xkcd.com/1256/
WHY DO THEY SAY T-MINUS
WHY ARE THERE OBELISKS
WHY ARE WRESTLERS ALWAYS WET

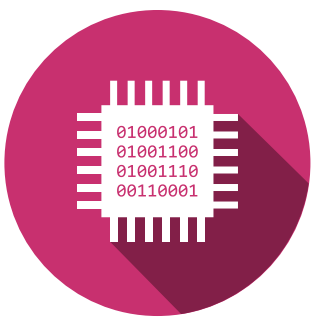
WHY IS LIFE SO
WHY ARE MY BOOBS ITCHY
WHY ARE CIGARETTES LEGAL
WHY ARE THERE DUCKS IN MY POOL
WHY IS JESUS WHITE
WHY IS THERE LIQUID IN MY EAR
WHY DO Q TIPS FEEL GOOD
WHY DO PEOPLE DIE



WHY ARE DOGS AFRAID OF FIR
WHY IS THERE NO KING IN E

Hes·so VALAIS WALLIS

Haute Ecole d'Ingénierie
Hochschule für Ingenieurwissenschaften



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