



# Synchronous counters

## Exercises Digital Design

### 1 | CNT - Counters by a power of 2

#### 1.1 Downwards Counter

Using D flip-flops and combinational logic gates, create a synchronous down-counter with the sequence

$$15 \Rightarrow 14 \Rightarrow 13 \Rightarrow 12 \Rightarrow \dots 3 \Rightarrow 2 \Rightarrow 1 \Rightarrow 0 \Rightarrow 15 \Rightarrow 14 \Rightarrow \dots \quad (1)$$

Draw the complete schema.

*cnt/pow2-01*

#### 1.2 Downwards Counter

Use T flip-flops and NAND gates to create a synchronous down-counter with the sequence

$$7 \Rightarrow 6 \Rightarrow 5 \Rightarrow 4 \Rightarrow 3 \Rightarrow 2 \Rightarrow 1 \Rightarrow 0 \Rightarrow 7 \Rightarrow 6 \Rightarrow \dots \quad (2)$$

Draw the complete schema.

*cnt/cnt-pow2-02*



## 2 | CNT - Counters by any number

### 2.1 Downwards Counter

Using D flip-flops and NAND gates, create a modulo-10 synchronous down-counter with the sequence

$$9 \Rightarrow 8 \Rightarrow 7 \Rightarrow 6 \Rightarrow \dots 3 \Rightarrow 2 \Rightarrow 1 \Rightarrow 0 \Rightarrow 9 \Rightarrow 8 \Rightarrow \dots \quad (3)$$

Draw the complete schema.

Draw the state graph with all states, including those outside the main loop.

*cnt/cnt-01*

### 2.2 Downwards Counter

Use D flip-flops and multiplexers to create a synchronous down-counter with the sequence

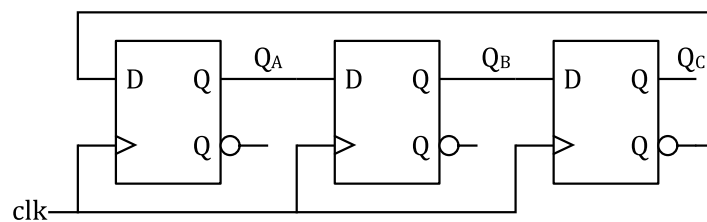
$$6 \Rightarrow 5 \Rightarrow 4 \Rightarrow 3 \Rightarrow 2 \Rightarrow 6 \Rightarrow \dots \quad (4)$$

Draw the complete circuit.

*cnt/cnt-02*

### 2.3 Johnson Counter

The following figure shows a Johnson counter.



This type of counter is of interest for high-speed systems. The circuit has one disadvantage: it has two independent sequences.

Eliminate the shortest sequence by changing the input function  $D_B$  of the second flip-flop.

*cnt/cnt-03*

### 3.1 Counter with Synchronous Zeroing

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*cnt/cnt-iterativ-01*

### 3.2 Counter with loading of a value

*cnt/cnt-iterativ-02*

### 3.3 up-down counter

*cnt/cnt-iterative-03*

### 3.4 Programmable Counter

The logic diagram shows a 2-bit counter with two D flip-flops, labeled  $Q_0$  and  $Q_1$ . The circuit has three inputs:  $en$  (enable),  $clk$  (clock), and  $rco$  (reset/clear). The output of the first flip-flop is  $Q_0$ , and the output of the second flip-flop is  $Q_1$ . The circuit also includes two OR gates, two AND gates, and two inverters. The  $en$  input is connected to the clock inputs of both flip-flops. The  $rco$  input is connected to the reset inputs of both flip-flops. The  $Q_0$  output is connected to the  $D$  input of the first flip-flop. The  $Q_1$  output is connected to the  $D$  input of the second flip-flop. The  $Q_0$  output is also connected to the  $P_0$  output of the first OR gate. The  $Q_1$  output is connected to the  $P_1$  output of the second OR gate. The  $Q_0$  output is also connected to the  $P_1$  output of the second OR gate. The  $Q_1$  output is also connected to the  $P_0$  output of the first OR gate. The  $Q_0$  output is also connected to the  $P_1$  output of the second OR gate. The  $Q_1$  output is also connected to the  $P_0$  output of the first OR gate.

*cnt/cnt-iterativ-04*