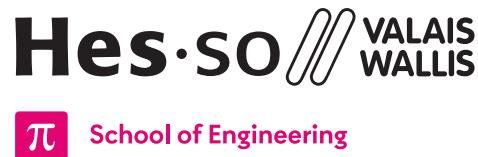


Cursor (Cur)

Lecture Digital Design (DiD)



Orientation: Systems Engineering (Synd)

Specialisation: Infotronics (IT)

Course: Digital Design (DiD)

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1 | Introduction

The goal of this project is to apply the acquired knowledge in a practical example at the end of the semester. It involves controlling a DC motor to precisely move a carriage along a lead screw to predefined positions. This positioning system can be seen in [Figure 1](#).

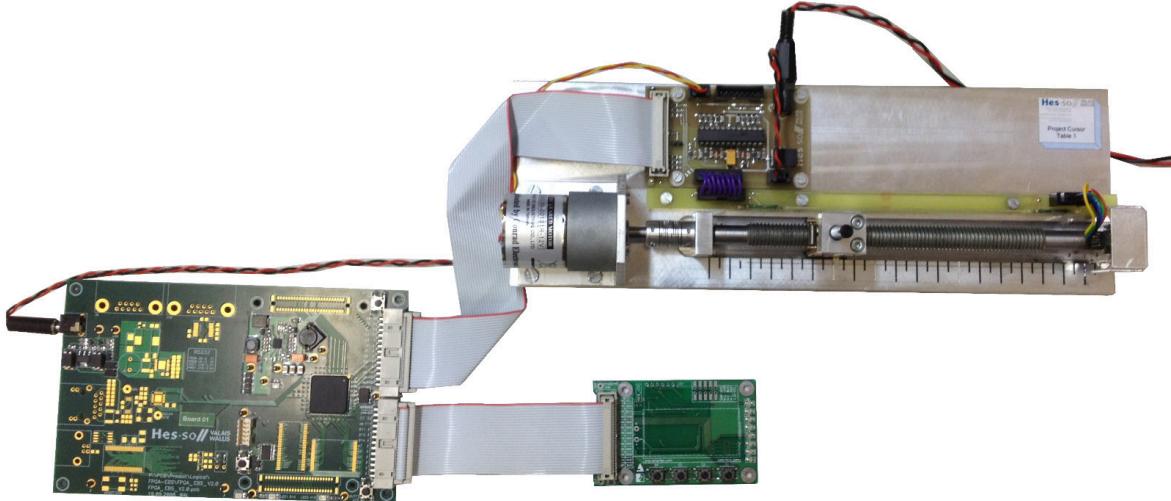


Figure 1 - Hardware setup Cursor (EBS2)

The minimum specifications (see [Section 2](#)) must be met, but students are encouraged to implement additional features. For example, an [Liquid Crystal Display \(LCD\)](#) screen can be used to display various information.



Implementing extra features will provide additional points in the final evaluation.



2 | Specification

2.1 Functions

The basic functions are defined as follows:

- When the **restart** button is pressed, the cursor moves to the start position indicated by a reed relay (Section 3.4) located near the DC motor (Section 3.2.1).
- When the Position₁ button is pressed, the cursor must first accelerate smoothly to position 1 (p_1), then move at full speed and finally decelerate smoothly to stop at position 1 (p_1). This can be done from the start position or from position 2, see Figure 2.
- When the Position₂ button is pressed, the cursor must first accelerate smoothly to position 2 (p_2), then move at full speed and finally decelerate smoothly to stop at position 2 (p_2), see Figure 2.

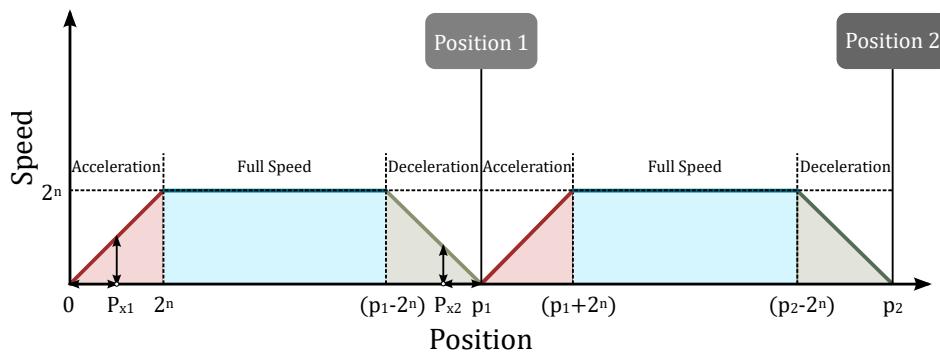


Figure 2 - Cursor speed diagram

The target positions are:

- Position 0 (p_0 , reset position) = 3.3 - 3.5 cm following mechanical assemblies
- Position 1 (p_1) = 8 cm
- Position 2 (p_2) = 12 cm

2.2 Circuit

To accomplish the task, the following circuit is provided to move the carriage.

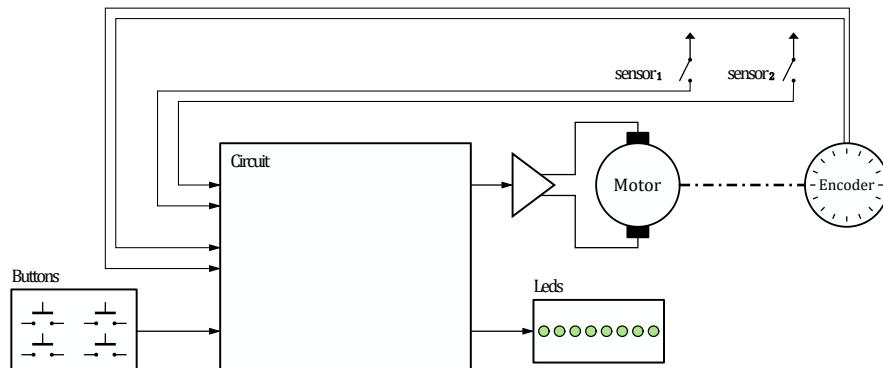


Figure 3 - Cursor circuit



2.3 Circuit

The circuit works as follows:

- The DC motor ([Section 3.2.1](#)) is controlled by the three signals motorOn , side_1 , side_2 :
 - The motor is activated when the signal motorOn is set to 1 and must be reset to 0 when the motor should not run.
 - Its speed is controlled by a [Pulse Width Modulation \(PWM\)](#) modulation applied either to the signal side_1 or to the signal side_2 depending on the desired direction of rotation.
- Two reed relays ([Section 3.4](#)) sensor₁ and sensor₂ are placed at the ends of the rail [1]. They detect the presence of the cursor carriage by indicating the presence of a magnet with a 1.
- The encoder ([Section 3.3](#)) is used to track, respectively count the position of the cursor. Its three outputs, encoder_A, encoder_B and encoder_I, allow tracking the movements of the screw. The A and B outputs alternate between 0 and 1 during movements with a phase shift of 90° between them, which allows determining the direction of movement. The I output generates a 1 pulse at each complete turn of the screw.
- Three buttons are used to control the system: restart, go₁ and go₂. An additional button, button₄, can be used for optional functions. When one of the buttons is pressed, the corresponding signal switches to 1.
- The pins testOut can be used to output additional information from the system, for example to connect them to the [Light Emitting Diodes \(LEDs\)](#) for debugging or visualization purposes.
- The signal testMode is set to 1 during simulation. This can be used to shorten the counters used for signal generation during tests to speed them up.

The empty toplevel design ([cursor-toplevel-empty.pdf](#)) shows all signals connected to the [Field Programmable Gate Array \(FPGA\)](#) board [Figure 4](#).

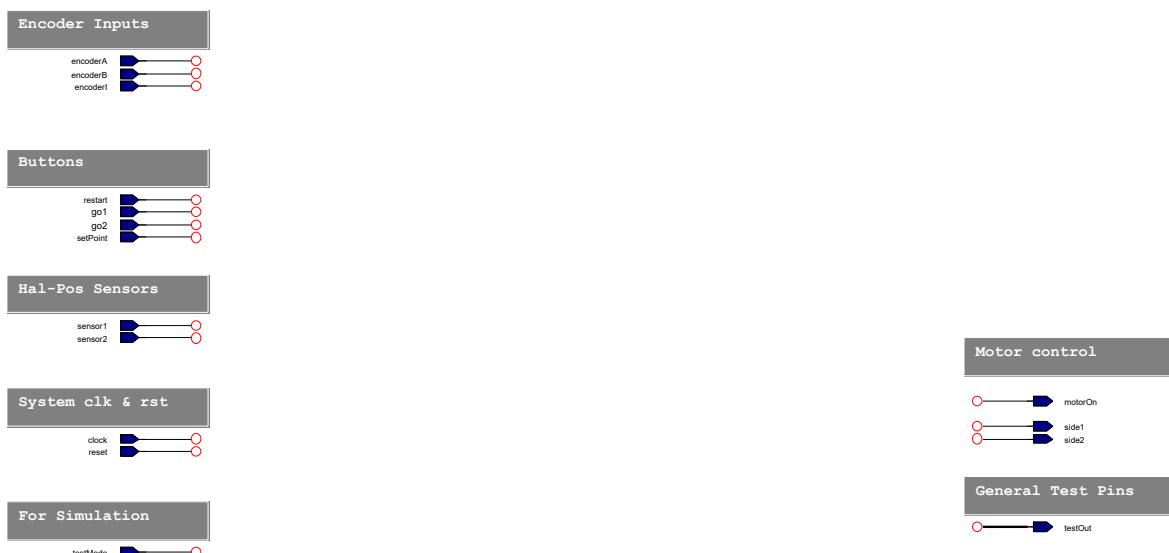


Figure 4 - Empty Toplevel Circuit



2.4 Scenario (example)

In [Figure 5](#), three different scenarios are presented. First, the restart button is pressed and the carriage moves at full speed to the start position (sensor_1). The other two scenarios go_2 and go_1 move the carriage to the position $_2$ and position $_1$ respectively, a variable **PWM** signal is applied to the signals side_2 and side_1 to accelerate and decelerate the carriage.

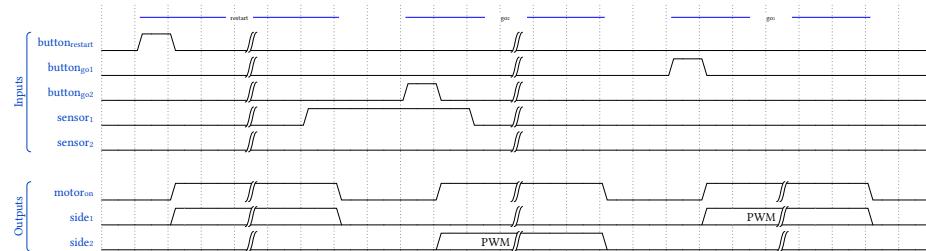


Figure 5 - Scenario cursor



The above scenarios are examples. It is up to the students to complete them.

2.5 HDL-Designer Project

A predefined HDL-Designer project can be downloaded or cloned from [Cyberlearn](#) or [Github](#). The file structure of the project looks as follows:

```

did_cursor
+--Board/          # Project and files for programming the FPGA
|   +--concat/     # Complete VHDL file including PIN-UCF file
|   +--ise/         # Xilinx ISE project
+--Cursor/          # Library for the components of the student solution
+--Cursor_test/    # Library for the simulation testbenches
+--doc/             # Folder with additional documents relevant to the project
|   +--Board/       # All schematics of the hardware boards
|   +--Components/ # All data sheets of hardware components
+--img/              # Pictures
+--Libs/             # External libraries which can be used e.g. gates, io, sequential
+--Prefs/            # HDL-Designer settings
+--Scripts/          # HDL-Designer scripts
+--Simulation/      # Modelsim simulation files

```



The path of the project folder must not contain spaces.



In the project folder **doc/** many important information can be found. Datasheets, project evaluation as well as help documents for HDL-Designer to name just a few.



3 | Components

The system consists of 3 different hardware boards, visible in the [Figure 1](#).

- A carriage assembly with a [Printed Circuit Board \(PCB\)](#) board that controls the motor and reads the sensors ([Figure 6](#))
- A [FPGA](#) development board ([Figure 14](#) or [Figure 15](#))
- A control board with 4 buttons and 8 [LEDs](#) ([Figure 16](#))

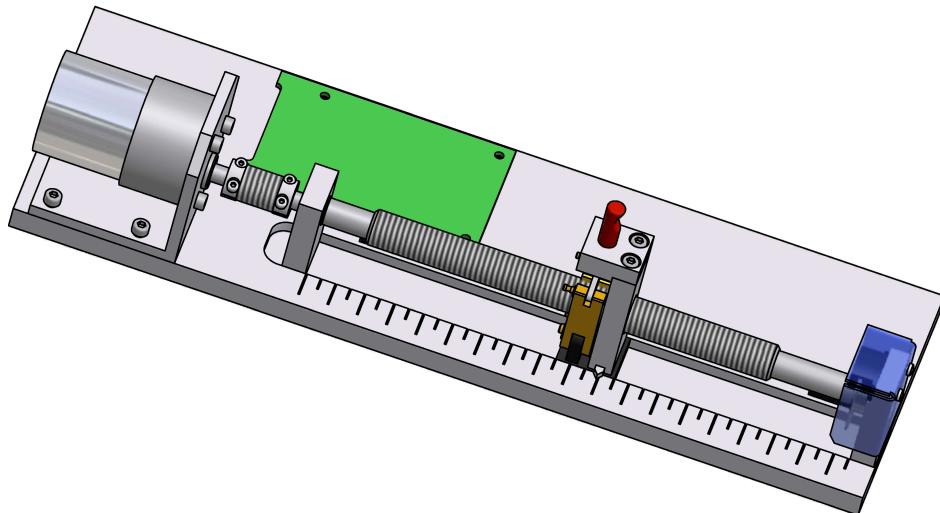


Figure 6 - Cursor carriage assembly

3.1 Carriage

The carriage structure includes the DC motor, the two reed relays [Section 3.4](#) as well as the carriage and the lead screw. The lead screw thread size is M12x1.75, meaning that a distance of 1.75mm is covered per revolution ([Figure 7](#)).

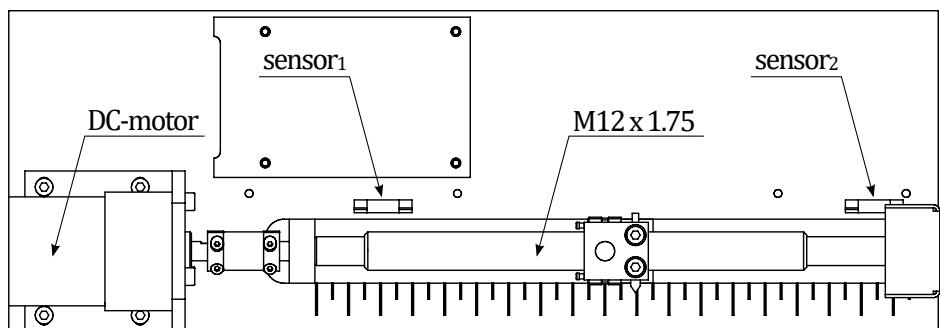


Figure 7 - Detailed assembly of the cursor carriage

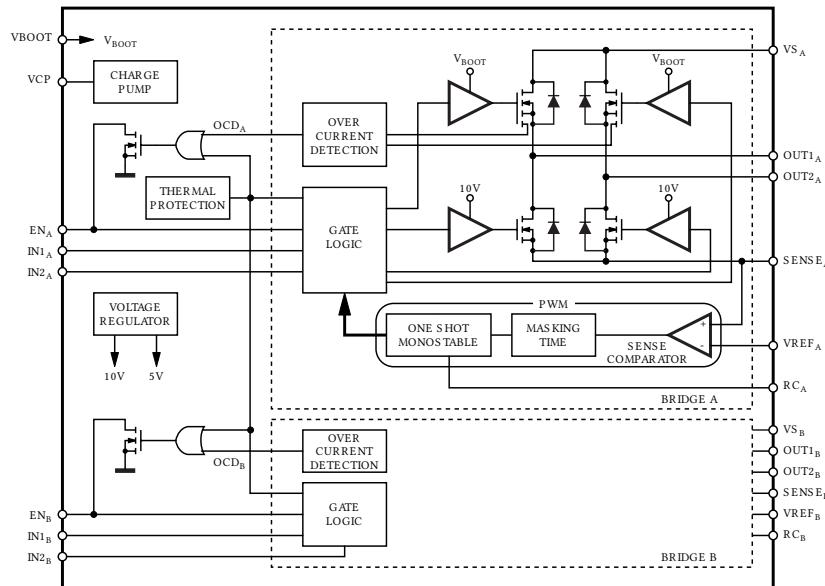
3.2 Motor control circuit

The DC motor of the carriage is powered by 12V. The power board has an H-bridge that is controlled by digital signals. On the power board, a 5V regulator generates the voltage powering the [FPGA](#) board [\[2\]](#).



3.2.1 Direct current motor

The DC motor is controlled by an H-bridge driver L6207 [3], see figure [Figure 8](#). The maximum switching frequency of the H-bridge is 100kHz. This should be taken into account when creating the [PWM](#) signal.



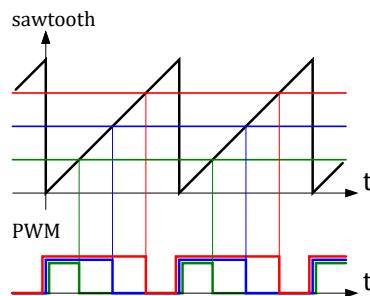
[Figure 8 - Block diagram of the L6207N H-bridge circuit \[3\]](#)

To adjust the speed of the DC motor, a [PWM](#) signal must be applied to the side₁ or side₂ signals, the maximum frequency being 100kHz. The longer the voltage is applied to the motor, the faster it turns. Powering either side₁ or side₂ controls the direction of the motor.

PWM - Implementation strategy

One strategy is to create a sawtooth counter ($0, 1, 2 \dots 2^N - 2, 2^N - 1, 0, 1, \dots$) and compare its value to a threshold. The rule is to output '1' when the counter value is less than the threshold, and '0' otherwise. By changing it, the duty cycle of the [PWM](#) signal is altered. In this way, the frequency of the [PWM](#) signal is defined by the speed of the counter (sawtooth), and the duty cycle is defined by the threshold value.

In the [Figure 9](#), the motor turns slower with the [green signal](#) than with the [blue signal](#) and than with the [red signal](#).



[Figure 9 - PWM signals](#)



The more steps (bits) the PWM has, the more precise the speed control is. However, too many steps may result in no notable speed difference due to control systems and motor characteristics. A good basis is to use 8 bits for the PWM resolution, giving 256 speed levels from 0 to 255.

Ramps - Implementation strategies

To create acceleration and deceleration ramps, a common method is to use a trapezoidal speed profile. This profile consists of three phases: acceleration, constant speed, and deceleration as shown under [Figure 10](#).

Multiple strategies exist to create such ramps. Typically, they are based on the time. But such system requires a feedback loop as long as a position control loop.

An easier, acceptable solution is to base the ramps on the position as $v_x = m * x + b$.

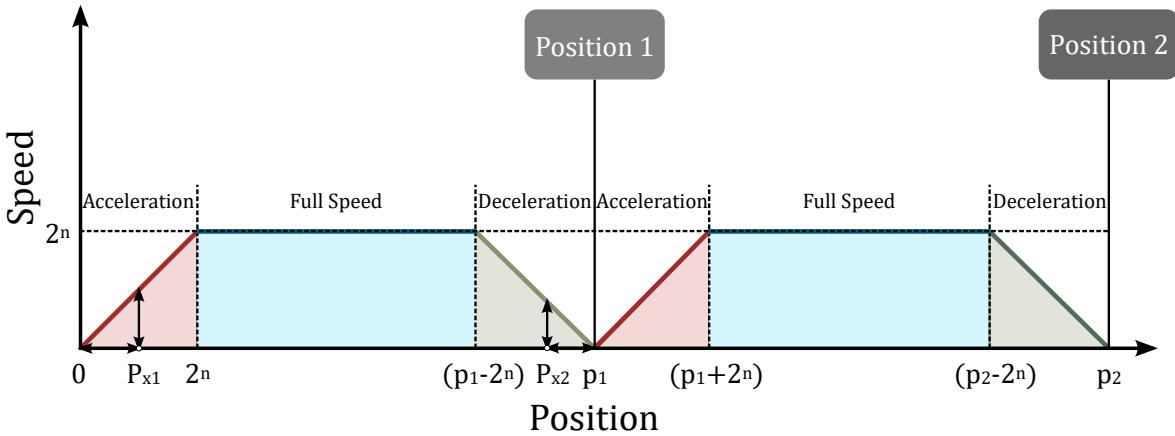


Figure 10 - Cursor speed diagram

3.3 Encoder

The angle of the lead screw can be measured using an [incremental encoder](#). The model used in the assembly is an AEDB-9140-A12 [4] with 2 feedback channels with 500 [Counts per Revolution \(CPR\)](#) (counts per revolution) per channel, represented in the [Figure 12](#).



Figure 11 - Encoder AEDB-9140-A12 [4]

Encoders - Implementation strategy

It is possible to use it in two ways:

- By using a single channel, which gives a resolution of $500 \frac{\text{pulses}}{\text{revolution}}$ i.e. $1'000 \frac{\text{edges}}{\text{revolution}}$ if counting both rising and falling edges.
- By using both channels as a [QEI \(Quadrature Encoder Interface\)](#), counting the rising and falling edges of both channels, increasing the resolution to $2000 \frac{\text{edges}}{\text{revolution}}$. This interfacing also allows to detect the rotation direction of the motor and is a common way to control DC motors with feedback encoders in the industry.

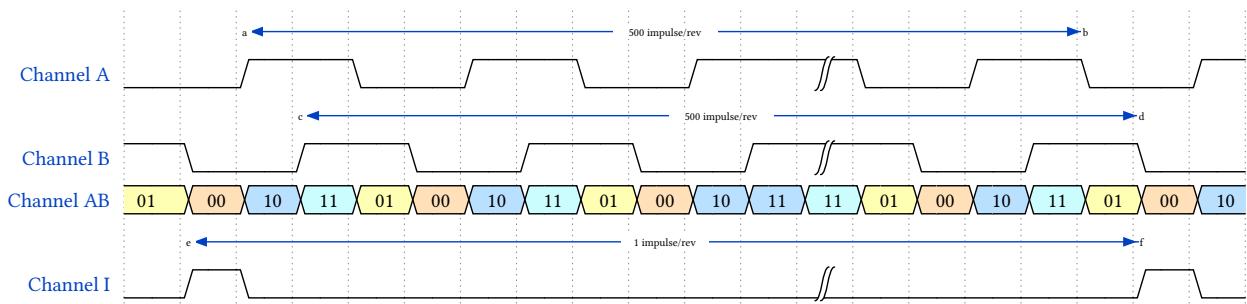


Figure 12 - Signals of incremental encoders

3.4 Reed relay

The reed relay is a switch toggled using electromagnets [1]. When a magnet is near the sensor, the contact closes (Figure 13). 2 reed relays are used (sensor₁ and sensor₂) to identify the left and right limits of the carriage.

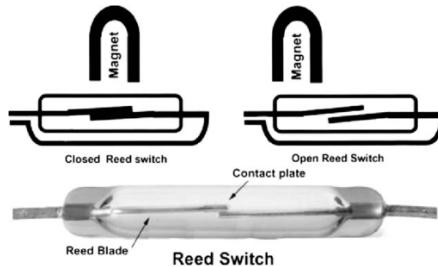


Figure 13 - Reed relay [5]

The signals sensor₁ and sensor₂ are '1' when the contact is closed (magnet nearby), otherwise '0'.

3.5 FPGA board

The main board is the school's FPGA-EBS 2 laboratory development board [6]. It hosts a **Xilinx Spartan xc3s500e FPGA** [7], [8] and has many different interfaces (**Universal Asynchronous Receiver Transmitter (UART)**, **Universal Serial Bus (USB)**, Ethernet, etc.). The oscillator used produces a clock signal (**clock**) with a frequency of $f_{\text{clk}} = 66\text{MHz}$ [9].

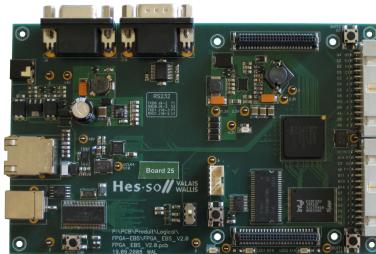
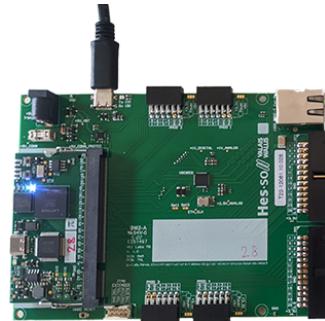


Figure 14 - FPGA board [6]

On the EBS3 board, the oscillator used produces a clock signal (**clock**) with a frequency of $f_{\text{clk}} = 100\text{MHz}$, reduced by PLL to $f_{\text{clk}} = 60\text{MHz}$.

Figure 15 - [FPGA board \[10\]](#)

The simulators are set by default for the EBS3 boards. To change them, open a testbench block **xxx_tb** and double-click on the **Pre-User** declarations (top left of the page) to modify the **clockFrequency** variable according to the desired clock value.

3.6 Buttons and LEDs

The board with the buttons and [LEDs \[11\]](#) is connected to the [FPGA](#) board. It has 4 buttons and 8 [LEDs](#) that can be used in the design. This board is equipped with an [LCD](#) display [\[12\], \[13\]](#).

Figure 16 - [Button-LEDs-LCD board \[11\]](#)



4 | Evaluation

In the **doc/** folder, the file **evaluation-bewertung-cursor.pdf** shows the detailed evaluation scheme, [Table 1](#).

The final grade includes the report, the code as well as a presentation of your system.

Evaluated aspects	Points
Report	55
Introduction	3
Specification	5
Project	20
Verification and validation	10
Integration	9
Conclusion	3
Formal aspects of the report	5
Functionality of the circuit	30
Quality of the solution	10
Presentation	10
Total	105

Table 1 - Evaluation grid



The evaluation grid already gives indications about the structure of the report. For a good report, consult the document “How to write a project report” [\[14\]](#).



5 | First steps

To start the project, proceed as follows:

- Read the specifications and information above carefully.
- Check the hardware and test the pre-programmed program.
- Browse through the documents in the **doc/** folder of your project.
- Develop a detailed functional diagram. You should be able to explain the signals and their functions.
- Implement and simulate the different blocks.
- Test the solution on the printed circuit board and find any errors .

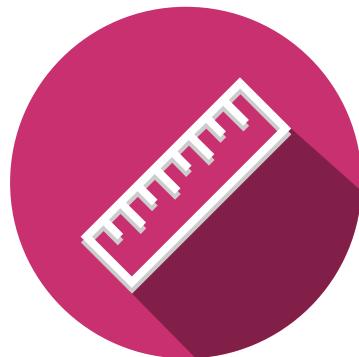
5.1 Tips

Here are some additional tips to avoid problems and time loss:

- Divide the problem into different blocks, use the empty Toplevel document (**cursor-toplevel-empty.pdf**) for this. It is recommended to have a balanced mix between the number of components and the size/complexity of the components.
- Analyze the different input and output signals, for this it is recommended to use the data sheets.
- Follow the DiD chapter “Methodology for the development of digital circuits (MET)” when creating the system [15].
- It is recommended to realize the system incrementally, for example:



Don't forget to have fun.





Glossary

CPR – Counts per Revolution [9](#)

FPGA – Field Programmable Gate Array [5, 7, 10, 11](#)

LCD – Liquid Crystal Display [3, 11](#)

LED – Light Emitting Diode [5, 7, 11](#)

PCB – Printed Circuit Board [7](#)

PWM – Pulse Width Modulation [5, 6, 8](#)

UART – Universal Asynchronous Receiver Transmitter [10](#)

USB – Universal Serial Bus [10](#)



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