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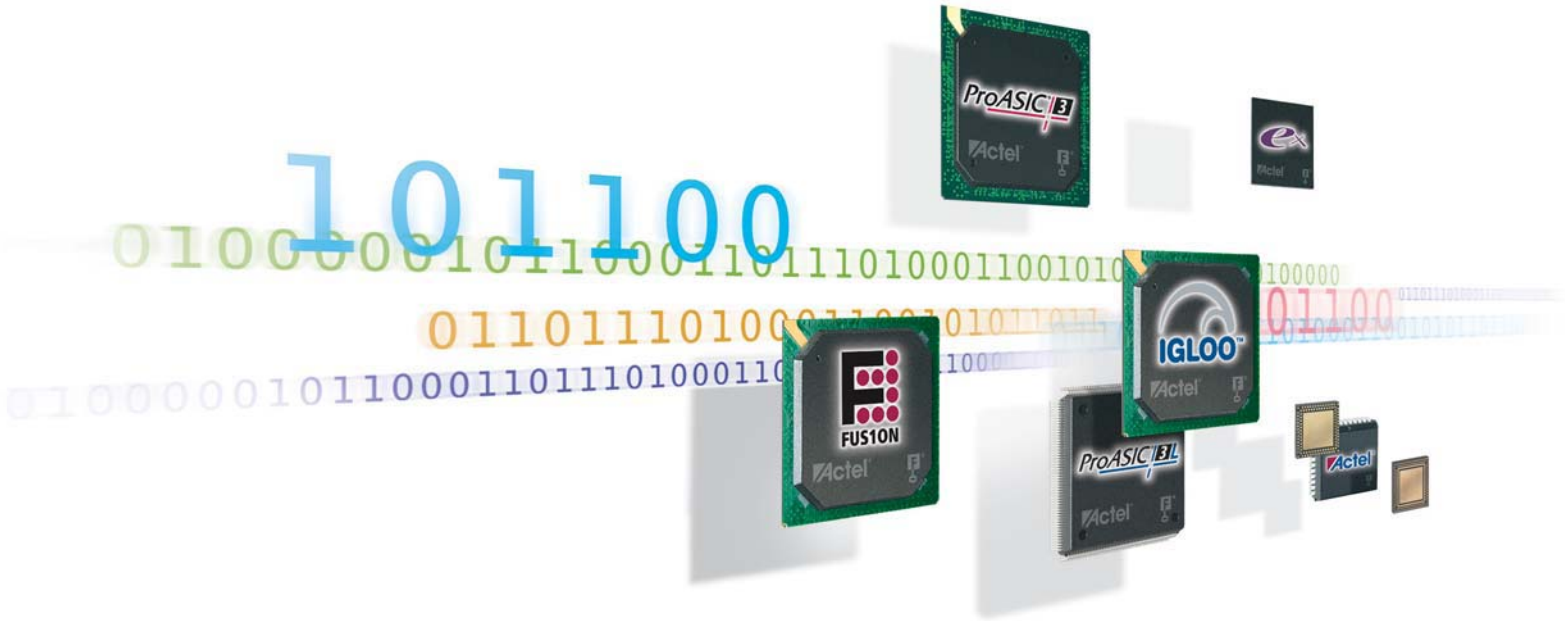
IGLOO® Handbook



Actel®
POWER MATTERS

IGLOO®
With Flash Freeze

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Low-Power Flash Device Handbooks Introduction

Device Handbooks contain all the information available to help designers understand and use Actel's devices. Handbook chapters are grouped into sections on the website to simplify navigation. Each chapter of the handbook can be viewed as an individual PDF file.

At the top of the handbook web page, you will see a zip file for each product family. This file contains the complete device handbook. Please register for product updates to be notified when a section of the handbook changes.

Versions

Device handbook chapters may have different version numbers. Actel's goal is to provide customers with the latest information in a timely matter. As a result, the handbook chapters will be updated independently of the handbook.

Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," and "Production". The definition of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advanced or production) and contains general product information. This document gives an overview of specific device and family information.

Advanced

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Unmarked (production)

This version contains information that is considered to be final.

Export Administration Regulations (EAR)

The products described in this document are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

Part Number and Revision Date

Part Number 51700094-001-0

Revised January 2008

Section I – IGLOO Datasheet

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v1.1

IGLOO Low-Power Flash FPGAs
with Flash*Freeze Technology

FlashLock

Features and Benefits

Low Power
- 1.2 V to 1.5 V Core Voltage Support for Low Power
- Supports Single-Voltage System Operation
- 5 µW Power Consumption in Flash*Freeze Mode
- Low-Power Active FPGA Operation
- Flash*Freeze Technology Enables Ultra-Low Power Consumption while Maintaining FPGA Content
- Easy Entry to / Exit from Ultra-Low-Power Flash*Freeze Mode

High Capacity
- 15 k to 1 Million System Gates
- Up to 144 kbits of True Dual-Port SRAM
- Up to 300 User I/Os

Reprogrammable Flash Technology
- 130-nm, 7-Layer Metal, Flash-Based CMOS Process
- Live-at-Power-Up (LAPU) Level 0 Support
- Single-Chip Solution
- Retains Programmed Design When Powered Off

In-System Programming (ISP) and Security
- Secure ISP Using On-Chip 128-Bit Advanced Encryption Standard (AES) Decryption (except ARM®-enabled IGLOO® devices) via JTAG (IEEE 1532–compliant)[1]
- FlashLock® to Secure FPGA Contents

High-Performance Routing Hierarchy
- Segmented, Hierarchical Routing and Clock Structure

Advanced I/O
- 700 Mbps DDR, LVDS-Capable I/Os (AGL250 and above)
- 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operation
- Bank-Selectable I/O Voltages—up to 4 Banks per Chip
- Single-Ended I/O Standards: LVTTL, LVCMOS 3.3 V / 2.5 V / 1.8 V / 1.5 V / 1.2 V, 3.3 V PCI / 3.3 V PCI-X[1], and LVCMOS 2.5 V / 5.0 V Input[1]
- Differential I/O Standards: LVPECL, LVDS, BLVDS, and M-LVDS (AGL250 and above)
- I/O Registers on Input, Output, and Enable Paths
- Hot-Swappable and Cold-Sparing I/Os‡
- Programmable Output Slew Rate[1] and Drive Strength
- Weak Pull-Up/-Down
- IEEE 1149.1 (JTAG) Boundary Scan Test
- Pin-Compatible Packages across the IGLOO Family

Clock Conditioning Circuit (CCC) and PLL[1]
- Six CCC Blocks, One with an Integrated PLL
- Configurable Phase Shift, Multiply/Divide, Delay Capabilities, and External Feedback
- Wide Input Frequency Range (1.5 MHz up to 250 MHz)

Embedded Memory
- 1 kbit of FlashROM User Nonvolatile Memory
- SRAMs and FIFOs with Variable-Aspect-Ratio 4,608-Bit[1] RAM Blocks (×1, ×2, ×4, ×9, and ×18 organizations)
- True Dual-Port SRAM (except ×18)[1]

ARM Processor Support in IGLOO FPGAs
- M1 IGLOO Devices—Cortex™-M1 Soft Processor Available with or without Debug

IGLOO Product Family

IGLOO Devices	AGL015	AGL030	AGL060	AGL125	AGL250	AGL600	AGL1000
ARM-Enabled IGLOO Devices					M1AGL250	M1AGL600	M1AGL1000
System Gates	15 k	30 k	60 k	125 k	250 k	600 k	1 M
Typical Equivalent Macrocells	128	256	512	1,024	–	–	–
VersaTiles (D-flip-flops)	384	768	1,536	3,072	6,144	13,824	24,576
Flash*Freeze Mode (typical, µW)	5	5	10	16	24	36	53
RAM kbits (1,024 bits)	–	–	18	36	36	108	144
4,608-Bit Blocks	–	–	4	8	8	24	32
FlashROM Bits	1 k	1 k	1 k	1 k	1 k	1 k	1 k
Secure (AES) ISP[4]	–	–	Yes	Yes	Yes	Yes	Yes
Integrated PLL in CCCs	–	–	1	1	1	1	1
VersaNet Globals[1]	6	6	18	18	18	18	18
I/O Banks	2	2	2	2	4	4	4
Maximum User I/Os	49	81	96	133	143	235	300
Package Pins CS QFN VQFP FBGA	QN68	UC81, CS81 QN132 VQ100	CS121 QN132 [3] VQ100 FG144 [3]	CS196 QN132 VQ100 FG144	CS196 [5] QN132 [3,5] VQ100 FG144	CS281 FG144, FG256, FG484	CS281 FG144, FG256, FG484

Notes:
1. *Six chip (main) and twelve quadrant global networks are available for AGL060 and above.*
2. *For higher densities and support of additional features, refer to the* IGLOOe Low-Power Flash FPGAs with Flash*Freeze Technology *handbook.*
3. *Device/package support TBD.*
4. *AES is not available for ARM-enabled IGLOO devices.*
5. *The M1AGL250 device does not support this package.*

1 AGL015 and AGL030 devices do not support this feature.

‡ Supported only by AGL015 and AGL030 devices.

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I/Os Per Package[1]

IGLOO Devices	AGL015	AGL030	AGL060	AGL125	AGL250		AGL600		AGL1000	
ARM-Enabled IGLOO Devices					M1AGL250 [2, 3]		M1AGL600		M1AGL1000	
	I/O Type									
Package	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O [2]	Differential I/O Pairs	Single-Ended I/O [2]	Differential I/O Pairs	Single-Ended I/O [2]	Differential I/O Pairs
QN68	49	–	–	–	–	–	–	–	–	–
UC81	–	66	–	–	–	–	–	–	–	–
CS81	–	66	–	–	–	–	–	–	–	–
CS121	–	–	96	–	–	–	–	–	–	–
VQ100	–	77	71	71	68	13	–	–	–	–
QN132	–	81	80 [8]	84	87 [8]	19 [8]	–	–	–	–
CS196	–	–	–	133	143	30	–	–	–	–
FG144	–	–	96 [8]	97	97	24	97	25	97	25
FG256	–	–	–	–	–	–	177	43	177	44
CS281	–	–	–	–	–	–	215	53	215	53
FG484	–	–	–	–	–	–	235	60	300	74

Notes:

1. *When considering migrating your design to a lower- or higher-density device, refer to the* IGLOO Low-Power Flash FPGAs *handbook to ensure compliance with design and board migration requirements.*
2. *Each used differential I/O pair reduces the number of single-ended I/Os available by two.*
3. *The M1AGL250 device does not support QN132 or CS196 packages. Refer to the* IGLOO Low-Power Flash FPGAs *handbook for position assignments of the 15 LVPECL pairs.*
4. *FG256 and FG484 are footprint-compatible packages.*
5. *When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not used as a regular I/O, the number of single-ended user I/Os available is reduced by one.*
6. *"G" indicates RoHS-compliant packages. Refer to "IGLOO Ordering Information" on page III for the location of the "G" in the part number.*
7. *Device/package support TBD.*

IGLOO FPGAs Package Sizes Dimensions

Package	UC81	CS81	CS121	QN68	QN132	CS196	CS281	FG144	VQ100	FG256	FG484
Length × Width (mm\mm)	4 × 4	5 × 5	6 × 6	8 × 8	8 × 8	8 × 8	10 × 10	13 × 13	14 × 14	17 × 17	23 × 23
Nominal Area (mm^2)	16	25	36	64	64	64	100	169	196	289	529
Pitch (mm)	0.4	0.5	0.5	0.4	0.5	0.5	0.5	1.0	0.5	1.0	1.0
Height (mm)	0.80	0.80	0.99	0.90	0.75	1.20	1.05	1.45	1.00	1.60	2.23

IGLOO Ordering Information

AGL1000 V2 – FG G 144 I

Application (Temperature Range)
- Blank = Commercial (0°C to +70°C Ambient Temperature)
- I = Industrial (–40°C to +85°C Ambient Temperature)
- PP = Pre-Production
- ES = Engineering Sample (Room Temperature Only)

Package Lead Count

Lead-Free Packaging
- Blank = Standard Packaging
- G = RoHS-Compliant Packaging

Package Type
- UC = Micro Chip Scale Package (0.4 mm pitch)
- CS = Chip Scale Package (0.4 mm and 0.5 mm pitches)
- QN = Quad Flat Pack No Leads (0.4 mm and 0.5 mm pitch)
- VQ = Very Thin Quad Flat Pack (0.5 mm pitch)
- FG = Fine Pitch Ball Grid Array (1.0 mm pitch)

Speed Grade
- F = 20% Slower than Standard*
- Blank = Standard

Supply Voltage
- 2 = 1.2 V to 1.5 V
- 5 = 1.5 V only

Part Number

IGLOO Devices
- AGL015 = 15,000 System Gates
- AGL030 = 30,000 System Gates
- AGL060 = 60,000 System Gates
- AGL125 = 125,000 System Gates
- AGL250 = 250,000 System Gates
- AGL600 = 600,000 System Gates
- AGL1000 = 1,000,000 System Gates

IGLOO Devices with Cortex-M1
- M1AGL250 = 250,000 System Gates
- M1AGL600 = 600,000 System Gates
- M1AGL1000 = 1,000,000 System Gates

Notes:

1. *Marking Information: IGLOO V2 devices do not have V2 marking, but IGLOO V5 devices are marked accordingly.*
2. *The DC and switching characteristics for the –F speed grade targets are based only on simulation.*
   The characteristics provided for the –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in the commercial temperature range.

Temperature Grade Offerings

Package	AGL015	AGL030	AGL060	AGL125	AGL250	AGL600	AGL1000
					M1AGL250 [4]	M1AGL600	M1AGL1000
QN68	C, I	–	–	–	–	–	–
UC81	–	C, I	–	–	–	–	–
CS81	–	C, I	–	–	–	–	–
CS121	–	–	C, I	–	–	–	–
VQ100	–	C, I	C, I	C, I	C, I	–	–
QN132	–	C, I	C, I [3]	C, I	C, I [3]	–	–
CS196	–	–	–	C, I	C, I	–	–
FG144	–	–	C, I [3]	C, I	C, I	C, I	C, I
FG256	–	–	–	–	–	C, I	C, I
CS281	–	–	–	–	–	C, I	C, I
FG484	–	–	–	–	–	C, I	C, I

Notes:

1. *C = Commercial temperature range: 0°C to 70°C ambient temperature.*
2. *I = Industrial temperature range: –40°C to 85°C ambient temperature.*
3. *Device/package support TBD.*
4. *The M1AGL250 device does not support FG256 or QN132 packages.*

Speed Grade and Temperature Grade Matrix

Temperature Grade	–F [1]	Std.
C [2]	✓	✓
I [3]	–	✓

Notes:

1. *The characteristics provided for the –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in the commercial temperature range.*
2. *C = Commercial temperature range: 0°C to 70°C ambient temperature.*
3. *I = Industrial temperature range: –40°C to 85°C ambient temperature.*

References made to IGLOO devices also apply to ARM-enabled IGLOOe devices. The ARM-enabled part numbers start with M1 (Cortex-M1).

Contact your local Actel representative for device availability:
http://www.actel.com/contact/default.aspx.

AGL015 and AGL030

The AGL015 and AGL030 are architecturally compatible; there are no RAM or PLL features.

1 – IGLOO Device Family Overview

General Description

The IGLOO family of flash FPGAs, based on a 130-nm flash process, offers the lowest power FPGA, a single-chip solution, small footprint packages, reprogrammability, and an abundance of advanced features.

The Flash*Freeze technology used in IGLOO devices enables entering and exiting an ultra-low-power mode that consumes as little as 5 µW while retaining SRAM and register data. Flash*Freeze technology simplifies power management through I/O and clock management with rapid recovery to operation mode.

The Low Power Active capability (static idle) allows for ultra-low-power consumption (from 12 µW) while the IGLOO device is completely functional in the system. This allows the IGLOO device to control system power management based on external inputs (e.g., scanning for keyboard stimulus) while consuming minimal power.

Nonvolatile flash technology gives IGLOO devices the advantage of being a secure, low power, single-chip solution that is live at power-up (LAPU). IGLOO is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

IGLOO devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on an integrated phase-locked loop (PLL). The AGL015 and AGL030 devices have no PLL or RAM support. IGLOO devices have up to 1 million system gates, supported with up to 144 kbits of true dual-port SRAM and up to 300 user I/Os.

M1 IGLOO devices support the high-performance, 32-bit Cortex-M1 processor developed by ARM for implementation in FPGAs. Cortex-M1 is a soft processor that is fully implemented in the FPGA fabric. It has a three-stage pipeline that offers a good balance between low-power consumption and speed when implemented in an M1 IGLOO device. The processor runs the ARMv6-M instruction set, has a configurable nested interrupt controller, and can be implemented with or without the debug block. Cortex-M1 is available for free from Actel for use in M1 IGLOO FPGAs.

The ARM-enabled devices have Actel ordering numbers that begin with M1AGL and do not support AES decryption.

Flash*Freeze Technology

The IGLOO device offers unique Flash*Freeze technology, allowing the device to enter and exit ultra-low-power Flash*Freeze mode. IGLOO devices do not need additional components to turn off I/Os or clocks while retaining the design information, SRAM content, and registers. Flash*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of IGLOO V2 devices to support a wide range of core voltage (1.2 V to 1.5 V) allows further reduction in power consumption, thus achieving the lowest total system power.

When the IGLOO device enters Flash*Freeze mode, the device automatically shuts off the clocks and inputs to the FPGA core; when the device exits Flash*Freeze mode, all activity resumes and data is retained.

The availability of low-power modes, combined with reprogrammability, a single-chip and single-voltage solution, and availability of small-footprint, high pin-count packages, make IGLOO devices the best fit for portable electronics.

Flash Advantages

Low Power

Flash-based IGLOO devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. IGLOO devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

IGLOO devices also have low dynamic power consumption to further maximize power savings; power is even further reduced by the use of a 1.2 V core voltage.

Low dynamic power consumption, combined with low static power consumption and Flash*Freeze technology, gives the IGLOO device the lowest total system power offered by any FPGA.

Security

The nonvolatile, flash-based IGLOO devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. IGLOO devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

IGLOO devices utilize a 128-bit flash-based lock and a separate AES key to secure programmed intellectual property and configuration data. In addition, all FlashROM data in IGLOO devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. IGLOO devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. IGLOO devices with AES-based security allow for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. The contents of a programmed IGLOO device cannot be read back, although secure design verification is possible.

Security, built into the FPGA fabric, is an inherent component of the IGLOO family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The IGLOO family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected and secure, making remote ISP possible. An IGLOO device provides the most impenetrable security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based IGLOO FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Live at Power-Up

The Actel flash-based IGLOO devices support Level 0 of the LAPU classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The LAPU feature of flash-based IGLOO devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the IGLOO device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based IGLOO devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

IGLOO flash FPGAs allow the user to quickly enter and exit Flash*Freeze mode. This is done almost instantly (within 1 µs) and the device retains configuration and data in registers and RAM. Unlike SRAM-based FPGAs the device does not need to reload configuration and design state from

external memory components; instead it retains all necessary information to resume operation immediately.

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, Flash-based IGLOO devices allow all functionality to be live at power-up; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The IGLOO family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the IGLOO family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/communications, computing, and avionics markets.

Firm-Error Immunity

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of IGLOO flash-based FPGAs. Once it is programmed, the flash cell configuration element of IGLOO FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Advanced Flash Technology

The IGLOO family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

IGLOO family FPGAs utilize design and process techniques to minimize power consumption in all modes of operation.

Advanced Architecture

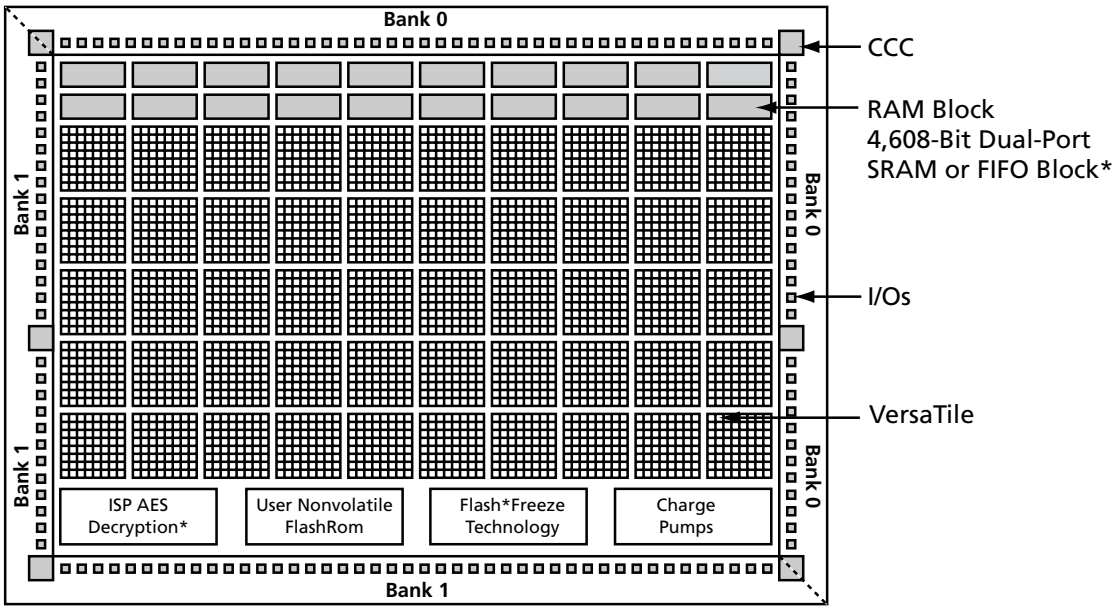
The proprietary IGLOO architecture provides granularity comparable to standard-cell ASICs. The IGLOO device consists of five distinct and programmable architectural features (Figure 1-1 on page 1-4 and Figure 1-2 on page 1-4):

- Flash*Freeze technology
- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory†
- Extensive CCCs and PLLs†
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the IGLOO core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Actel ProASIC® family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

† *The AGL015 and AGL030 do not support PLL or SRAM.*

In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of IGLOO devices via an IEEE 1532 JTAG interface.



* *Not supported by AGL015 and AGL030 devices*

Figure 1-1 • **IGLOO Device Architecture Overview with Two I/O Banks (AGL015, AGL030, AGL060, and AGL125)**

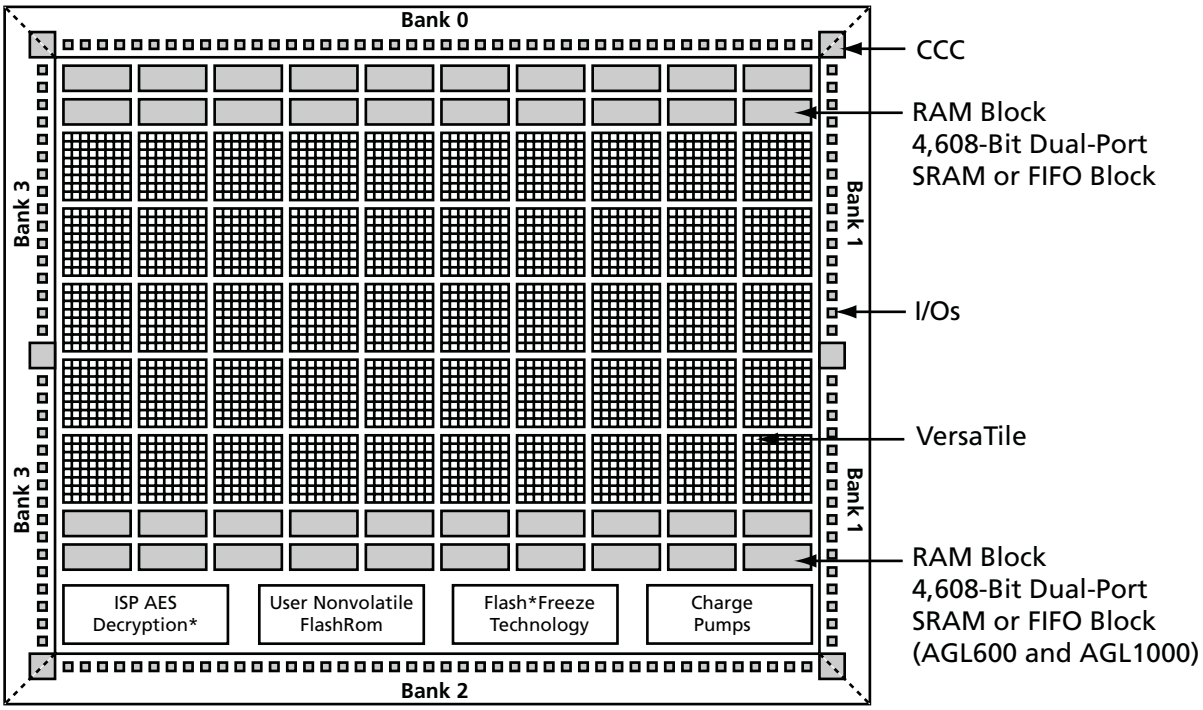


Figure 1-2 • **IGLOO Device Architecture Overview with Four I/O Banks (AGL250, AGL600, and AGL1000)**

Flash*Freeze Technology

The IGLOO device has an ultra-low power static mode, called Flash*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash*Freeze technology enables the user to quickly (within 1 µs) enter and exit Flash*Freeze mode by activating the Flash*Freeze pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and can be toggling without impact on power consumption, clocks can still be driven or can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and states. I/O states are tristated during Flash*Freeze mode or can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL, and the device consumes as little as 5 µW in this mode.

Flash*Freeze technology allows the user to switch to active mode on demand, thus simplifying the power management of the device.

The Flash*Freeze pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. It is also possible to use the Flash*Freeze pin as a regular I/O if Flash*Freeze mode usage is not planned, which is advantageous because of the inherent low power static (as low as 12 µW) and dynamic capabilities of the IGLOO device. Refer to Figure 1-3 for an illustration of entering/exiting Flash*Freeze mode.

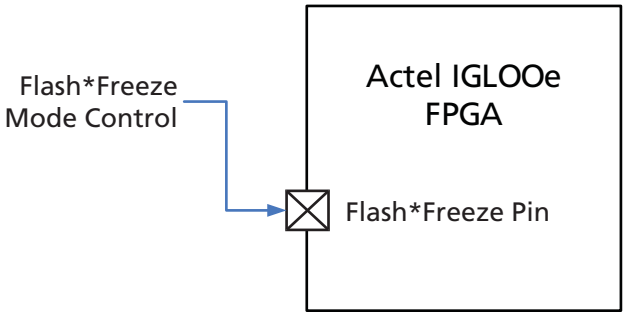


Figure 1-3 • **IGLOO Flash*Freeze Mode**

VersaTiles

The IGLOO core consists of VersaTiles, which have been enhanced beyond the ProASIC^PLUS® core tiles. The IGLOO VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-4 for VersaTile configurations.

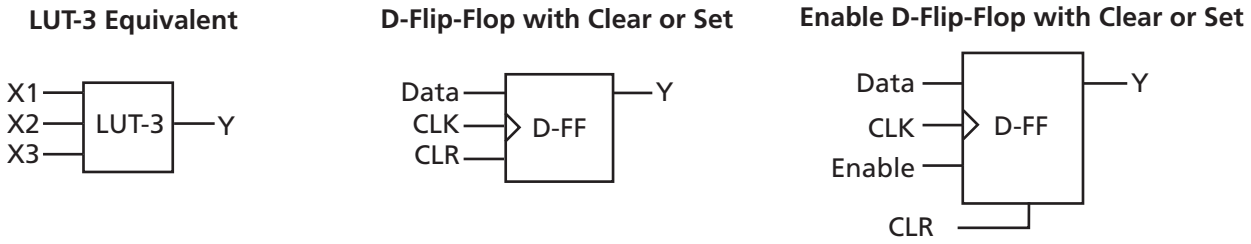


Figure 1-4 • **VersaTile Configurations**

User Nonvolatile FlashROM

Actel IGLOO devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard IGLOO IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in the AGL015 and AGL030 devices), as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The Actel IGLOO development software solutions, Libero® Integrated Design Environment (IDE) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Actel Libero IDE and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

IGLOO devices (except the AGL015 and AGL030 devices) have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro (except in the AGL015 and AGL030 devices).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

IGLOO devices provide designers with very flexible clock conditioning circuit (CCC) capabilities. Each member of the IGLOO family contains six CCCs. One CCC (center west side) has a PLL. The AGL015 and AGL030 do not have a PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides. One CCC (center west side) has a PLL.

All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz up to 250 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% ± 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time is 300 µs (for PLL only)
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × 250 MHz / f_{OUT_CCC} (for PLL only)

Global Clocking

IGLOO devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

I/Os with Advanced I/O Standards

The IGLOO family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V). IGLOO FPGAs support many different I/O standards—single-ended and differential.

The I/Os are organized into banks, with two or four banks per device. The configuration of these banks determines the I/O standards supported.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications
- Double-Data-Rate applications—DDR LVDS, BLVDS, and M-LVDS I/Os for point-to-point communications

IGLOO banks for the AGL250 device and above support LVPECL, LVDS, BLVDS, and M-LVDS. BLVDS and M-LVDS can support up to 20 loads.

Part Number and Revision Date

Part Number 51700095-001-4
Revised July 2008

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v1.1)	Page
v1.0 (March 2008)	As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2 V / 1.5 V to 1.2 V to 1.5 V.	N/A
51700095-001-3 (March 2008)	This document was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview.	N/A
51700095-001-2 (February 2008)	The "Low Power" section was updated to change "1.2 V and 1.5 V Core Voltage" to "1.2 V and 1.5 V Core and I/O Voltage." The text "(from 12 µW)" was removed from "Low-Power Active FPGA Operation." 1.2_V was added to the list of core and I/O voltages in the "Advanced I/O" and "I/Os with Advanced I/O Standards" sections.	I I, 1-7
	The "Embedded Memory" section was updated to remove the footnote reference from the section heading and place it instead after "4,608-Bit" and "True Dual-Port SRAM (except ×18)."	I
51700095-001-1 (January 2008)	This document was updated to include AGL015 device information. QN68 is a new package that was added because it is offered in the AGL015. The following sections were updated: "Features and Benefits" "IGLOO Ordering Information" "Temperature Grade Offerings" "IGLOO Product Family" "IGLOO FPGAs Package Sizes Dimensions" "AGL015 and AGL030" note "IGLOO Device Family Overview"	N/A
	The "Temperature Grade Offerings" table was updated to include M1AGL600.	IV
	In the "IGLOO Ordering Information" table, the QN package measurements were updated to include both 0.4 mm and 0.5 mm.	III
	In the "General Description" section, the number of I/Os was updated from 288 to 300.	1-5
51700095-001-0 (January 2008)	The "Low Power" section was updated to change the description of low-power active FPGA operation to "from 12 µW" from "from 25 µW." The same update was made in the "General Description" section and the "Flash*Freeze Technology" section.	I, 1-1, 1-5
Advance v0.7 (November 2007)	This document was previously in datasheet Advance v0.7. As a result of moving to the handbook format, Actel has restarted the version numbers. The new version number is 51700095-001-0.	N/A

Previous Version	Changes in Current Version (v1.1)	Page
Advance v0.6 (November 2007)	Table 1 • IGLOO Product Family, the "I/Os Per Package1" table, and the Temperature Grade Offerings table were updated to reflect the following: CS196 is now supported for AGL250; device/package support for QN132 is to be determined for AGL250; the CS281 package was added for AGL600 and AGL1000.	i, ii, iv
	Table 2 • IGLOO FPGAs Package Sizes Dimensions is new, and package sizes were removed from the "I/Os Per Package1" table.	ii
	The "I/Os Per Package1"table was updated to reflect 77 instead of 79 single-ended I/Os for the VG100 package for AGL030.	ii
Advance v0.6 (November 2007)	A note was added to "IGLOO Ordering Information" regarding marking information.	iii
Advance v0.5 (September 2007)	Table 1 • IGLOO Product Family, the "I/Os Per Package1" table, and the "IGLOO Ordering Information", and the Temperature Grade Offerings table were updated to add the UC81 package.	i, ii, iii, iv
Advance v0.4 (September 2007)	Table 1 • IGLOO Product Family was updated for AGL030 in the Package Pins section to change CS181 to CS81.	i
Advance v0.3 (August 2007)	Cortex-M1 device information was added to Table 1 • IGLOO Product Family, the "I/Os Per Package1" table, "IGLOO Ordering Information", and Temperature Grade Offerings.	i, ii, iii, iv
	The number of single-ended I/Os for the CS81 package for AGL030 was updated to 66 in the "I/Os Per Package1" table.	ii
Advance v0.2 (July 2007)	In Table 1 • IGLOO Product Family, the CS81 package was added for AGL030. The CS196 was replaced by the CS121 for AGL060. Table note 3 was moved to the specific packages to which it applies for AGL060: QN132 and FG144.	i
	The CS81 and CS121 packages were added to the "I/Os Per Package1" table. The number of single-ended I/Os was removed for the CS196 package in AGL060. Table note 6 was moved to the specific packages to which it applies for AGL060: QN132 and FG144.	ii
	The CS81 and CS121 packages were added to the Temperature Grade Offerings table. The temperature grade offerings were removed for the CS196 package in AGL060. Table note 3 was moved to the specific packages to which it applies for AGL060: QN132 and FG144.	iv
Advance v0.1	The words "ambient temperature" were added to the temperature range in the "IGLOO Ordering Information", Temperature Grade Offerings, and "Speed Grade and Temperature Grade Matrix" sections.	iii, iv

Rate This Document

2 – IGLOO DC and Switching Characteristics

General Specifications

DC and switching characteristics for –F speed grade targets are based only on simulation.

The characteristics provided for the –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in the commercial temperature range.

Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

Table 2-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
V_{CC}	DC core supply voltage	–0.3 to 1.65	V
V_{JTAG}	JTAG DC voltage	–0.3 to 3.75	V
V_{PUMP}	Programming voltage	–0.3 to 3.75	V
V_{CCPLL}	Analog power supply (PLL)	–0.3 to 1.65	V
V_{CCI} and VMV [3]	DC I/O buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (V_{CCI} + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
T_{STG} [2]	Storage Temperature	–65 to +150	°C
T_J [2]	Junction Temperature	+125	°C

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4 on page 2-3.*
2. *For flash programming and retention, maximum limits refer to Table 2-3 on page 2-2, and for recommended operating limits, refer to Table 2-2 on page 2-2.*
3. *VMV pins must be connected to the corresponding V_{CCI} pins. See Pin Descriptions for further information.*

Table 2-2 • **Recommended Operating Conditions** [4]

Symbol	Parameter		Commercial	Industrial	Units
T_A	Ambient Temperature		0 to +70 [6]	–40 to +85 [7]	°C
T_J	Junction Temperature [8]		0 to + 85	–40 to +100	°C
V_{CC} [3]	1.5 V DC core supply voltage[1]		1.425 to 1.575	1.425 to 1.575	V
	1.2 V–1.5 V wide range core voltage[2]		1.14 to 1.575	1.14 to 1.575	V
V_{JTAG}	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
V_{PUMP}	Programming voltage	Programming Mode	3.15 to 3.45	3.15 to 3.45	V
		Operation[5]	0 to 3.45	0 to 3.45	V
V_{CCPLL} [9]	Analog power supply (PLL)	1.5 V DC core supply voltage[1]	1.4 to 1.6	1.4 to 1.6	V
		1.2 V–1.5 V wide range core voltage[2]	1.14 to 1.575	1.14 to 1.575	V
V_{CCI} and VMV [10]	1.2 V DC core supply voltage[2]		1.14 to 1.26	1.14 to 1.26	V
	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V wide range DC supply voltage[11]		2.7 to 3.6	2.7 to 3.6	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V

Notes:

1. *For IGLOO® V5 devices*
2. *For IGLOO V2 devices only, operating at $V_{CCI} \geq V_{CC}$*
3. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-24 on page 2-23. V_{CCI} should be at the same voltage within a given I/O bank.*
4. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
5. *V_{PUMP} can be left floating during operation (not programming mode).*
6. *Maximum T_J = 85 °C.*
7. *Maximum T_J = 100 °C.*
8. *To ensure targeted reliability standards are met across ambient and junction operating temperatures, Actel recommends that the user follow best design practices using Actel's timing and power simulation tools.*
9. *V_{CCPLL} pins should be tied to V_{CC} pins. See Pin Descriptions for further information.*
10. *VMV pins must be connected to the corresponding V_{CCI} pins. See Pin Descriptions for further information.*
11. *3.3 V wide range is compliant to the JDEC8a specification and supports 3.0 V V_{CCI} operation.*

Table 2-3 • **Flash Programming Limits – Retention, Storage, and Operating Temperature**[1]

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T_{STG} (°C) [2]	Maximum Operating Junction Temperature T_J (°C) [2]
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

Notes:

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*
2. *These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.*

Table 2-4 • **Overshoot and Undershoot Limits [1]**

V_{CCI}	Average V_{CCI}–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at junction temperature at 85°C.*
2. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*
3. *This table does not provide PCI overshoot/undershoot limits.*

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every IGLOO device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-1 on page 2-4 and Figure 2-2 on page 2-5.

There are five regions to consider during power-up.

IGLOO I/Os are activated only if ALL of the following three conditions are met:

1. V_{CC} and V_{CCI} are above the minimum specified trip points (Figure 2-1 on page 2-4 and Figure 2-2 on page 2-5).
2. $V_{CCI} > V_{CC} – 0.75$ V (typical)
3. Chip is in the operating mode.

V_{CCI} Trip Point:
Ramping up (V5 devices): 0.6 V < trip_point_up < 1.2 V
Ramping down (V5 Devices): 0.5 V < trip_point_down < 1.1 V
Ramping up (V2 devices): 0.75 V < trip_point_up < 1.05 V
Ramping down (V2 devices): 0.65 V < trip_point_down < 0.95 V

V_{CC} Trip Point:
Ramping up (V5 devices): 0.6 V < trip_point_up < 1.1 V
Ramping down (V5 devices): 0.5 V < trip_point_down < 1.0 V
Ramping up (V2 devices): 0.65 V < trip_point_up < 1.05 V
Ramping down (V2 devices): 0.55 V < trip_point_down < 0.95 V

V_{CC} and V_{CCI} ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to V_{CCI}.
- JTAG supply, PLL power supplies, and charge pump V_{PUMP} supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

Actel recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until V_{CC} and V_{CCPLX} exceed brownout activation levels (see Figure 2-1 and Figure 2-2 on page 2-5 for more details).

When PLL power supply voltage and/or VCC levels drop below the V_{CC} brownout levels (0.75 V ± 0.25 V for V5 devices, and 0.75 V ± 0.2 V for V2 devices), the PLL output lock signal goes low and/or the output clock is lost. Refer to the Brownout Voltage section in the *Power-Up/-Down Behavior of Low-Power Flash Devices* chapter of the *ProASIC®3* and *ProASIC3E* handbooks for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

To make sure the transition from input buffers to output buffers is clean, ensure that there is no path longer than 100 ns from input buffer to output buffer in your design.

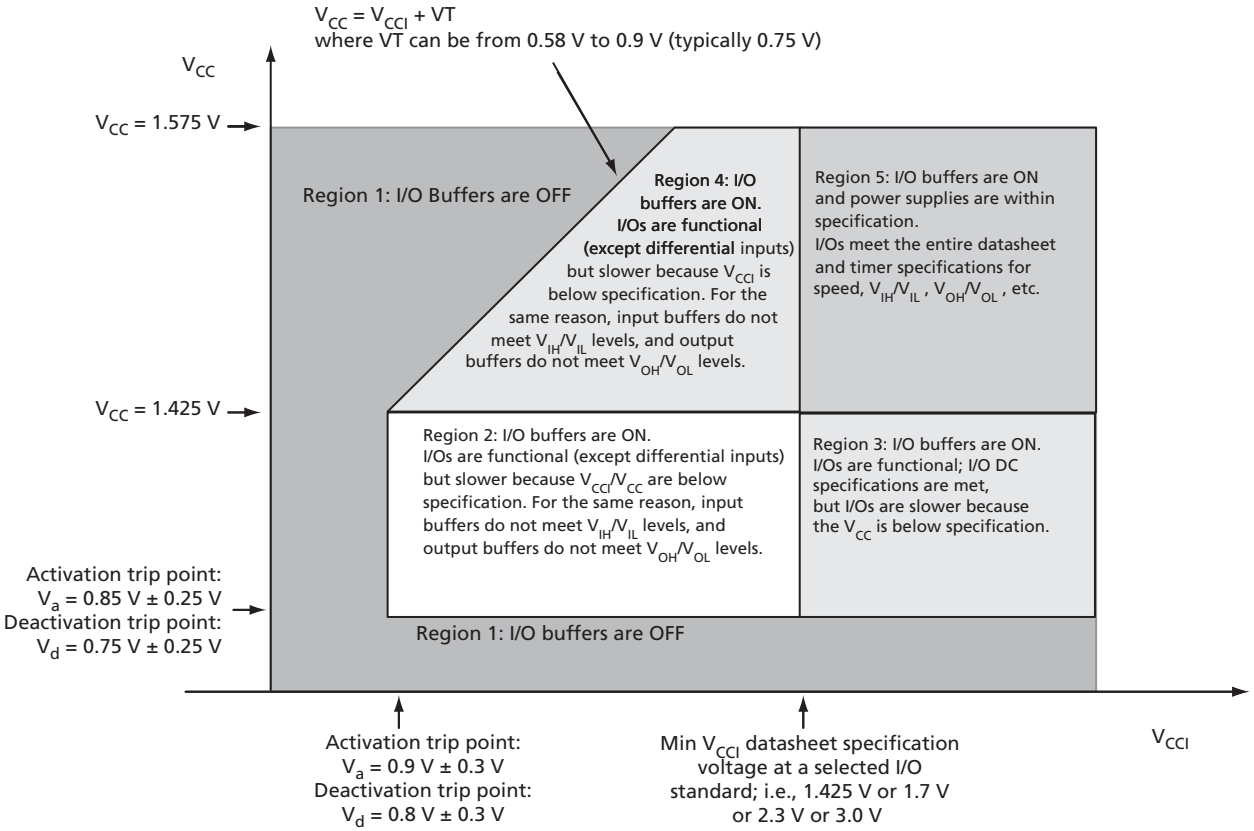


Figure 2-1 • **V5 Devices – I/O State as a Function of V_{CCI} and V_{CC} Voltage Levels**

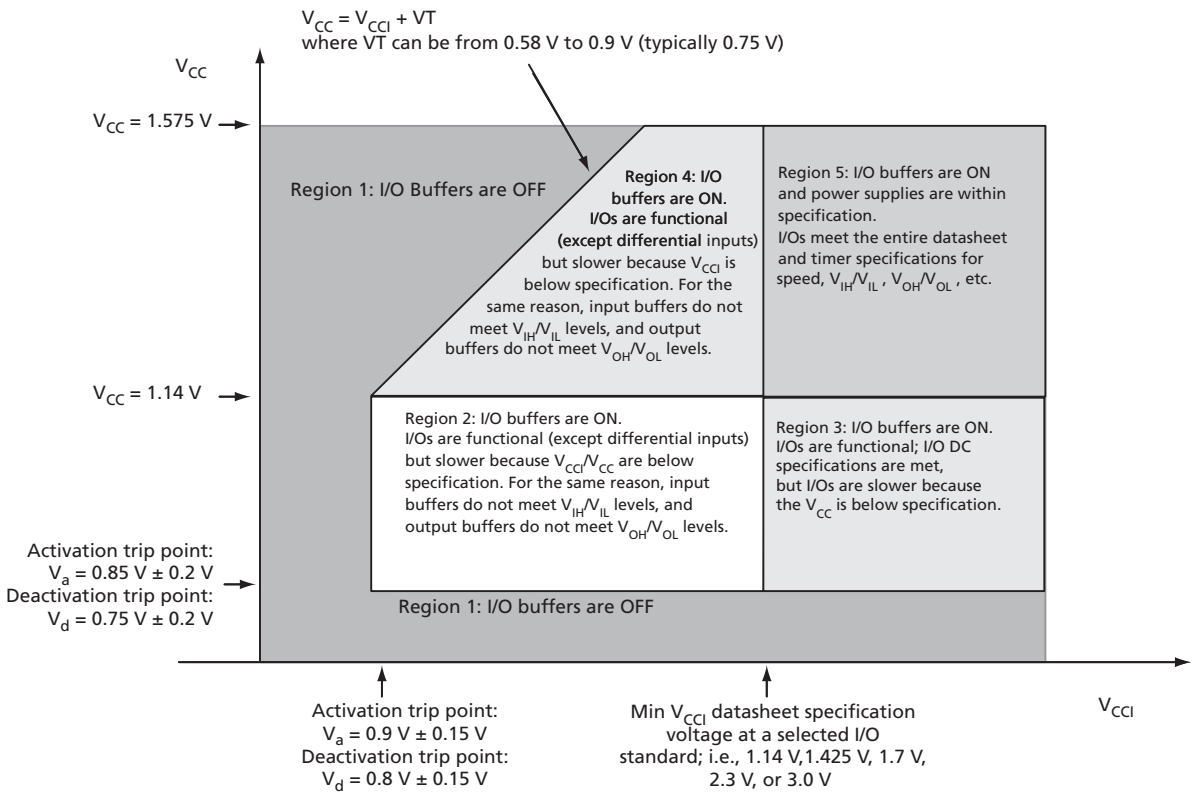


Figure 2-2 • **V2 Devices – I/O State as a Function of V_{CCI} and V_{CC} Voltage Levels**

Thermal Characteristics

Introduction

The temperature variable in the Actel Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ 2-1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A \qquad \textit{EQ 2-1}$$

where:

T_A = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Table 2-5 on page 2-6.

P = Power dissipation

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates. The absolute maximum junction temperature is 110°C. EQ 2-2 shows a sample calculation of the absolute maximum power dissipation allowed for a 484-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{100\text{°C} - 70\text{°C}}{20.5\text{°C/W}} = 1.463\ \text{W}$$

EQ 2-2

Table 2-5 • **Package Thermal Resistivities**

Package Type	Device	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 200 ft./min.	θ_{ja} 500 ft./min.	Units
Quad Flat No Lead	AGL015	68	TBD	TBD	TBD	TBD	C/W
	AGL030	132	0.4	21.4	16.8	15.3	C/W
	AGL060	132	0.3	21.2	16.6	15.0	C/W
	AGL125	132	0.2	21.1	16.5	14.9	C/W
	AGL250	132	0.1	21.0	16.4	14.8	C/W
Very Thin Quad Flat Pack (VQFP)	All devices	100	10.0	35.3	29.4	27.1	C/W
Chip Scale Package (CSP)	All devices	196		57.8	47.6	43.3	C/W
Fine Pitch Ball Grid Array (FBGA)	See note*	144	3.8	26.9	22.9	21.5	C/W
	See note*	256	3.8	26.6	22.8	21.5	C/W
	See note*	484	3.2	20.5	17.0	15.9	C/W
	See note*	896	2.4	13.6	10.4	9.4	C/W
	AGL060	144	18.6	55.2	49.4	47.2	C/W
	AGL1000	144	6.3	31.6	26.2	24.2	C/W
	AGL250	256	12.0	38.6	34.7	33.0	C/W
	AGL1000	256	6.6	28.1	24.4	22.7	C/W
	AGL1000	484	8.0	23.3	19.0	16.7	C/W

* *This information applies to all IGLOO devices except those listed below. Detailed device/package thermal information for all IGLOO devices will be available in future revisions of the datasheet.*

Temperature and Voltage Derating Factors

Table 2-6 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70°C, V_{CC} = 1.425 V)**
For IGLOO V2 or V5 devices, 1.5 V DC Core Supply Voltage

Array Voltage V_{CC} (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	110°C
1.425	0.95	0.96	0.98	1.00	1.01	1.02
1.5	0.88	0.89	0.91	0.93	0.93	0.94
1.575	0.82	0.84	0.85	0.87	0.88	0.89

Table 2-7 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70°C, V_{CC} = 1.14 V)**
For IGLOO V2, 1.2 V DC Core Supply Voltage

Array Voltage V_{CC} (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	110°C
1.14	0.97	0.98	0.99	1.00	1.01	1.01
1.2	0.86	0.87	0.89	0.89	0.90	0.91
1.26	0.79	0.80	0.81	0.82	0.83	0.83

Calculating Power Dissipation

Quiescent Supply Current

Quiescent supply current (I_{DD}) calculation depends on multiple factors, including operating voltages (V_{CC}, V_{CCI}, and V_{JTAG}), operating temperature, system clock frequency, and power modes usage. Actel recommends using the PowerCalculator and SmartPower software estimation tools to evaluate the projected static and active power based on the user design, power mode usage, operating voltage, and temperature.

Table 2-8 • **Quiescent Supply Current (I_{DD}) Characteristics, IGLOO Flash*Freeze Mode***

	Core Voltage	AGL015	AGL030	AGL060	AGL125	AGL250	AGL600	AGL1000	Units
Typical (25°C)	1.2 V	4	4	8	13	20	30	44	µA
	1.5 V	6	6	10	18	34	72	127	µA

* *I_{DD} includes V_{CC}, V_{PUMP}, V_{CCI}, V_{JTAG}, and V_{CCPLL} currents. Values do not include I/O static contribution (P_{DC6} and P_{DC7}).*

Table 2-9 • **Quiescent Supply Current (I_{DD}) Characteristics, IGLOO Sleep Mode (V_{CC} = 0 V)***

	Core Voltage	AGL015	AGL030	AGL060	AGL125	AGL250	AGL600	AGL1000	Units
V_{CCI}/V_{JTAG} = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	1.7	1.7	1.7	1.7	µA
V_{CCI}/V_{JTAG} = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	1.8	1.8	1.8	1.8	µA
V_{CCI} / V_{JTAG} = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	1.9	1.9	1.9	1.9	µA
V_{CCI} / V_{JTAG} = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	2.2	2.2	2.2	2.2	µA
V_{CCI} / V_{JTAG} = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	2.5	2.5	2.5	2.5	µA

* *I_{DD} includes V_{CC}, V_{PUMP}, and V_{CCPLL} currents. Values do not include I/O static contribution (P_{DC6} and P_{DC7}).*

Table 2-10 • **Quiescent Supply Current (I_{DD}) Characteristics, IGLOO Shutdown Mode (V_{CC}, V_{CCI} = 0 V)***

	Core Voltage	AGL015	AGL030	Units
Typical (25°C)	1.2 V / 1.5 V	0	0	µA

* *I_{DD} includes V_{CC}, V_{PUMP}, V_{CCI}, V_{JTAG}, and V_{CCPLL} currents. Values do not include I/O static contribution (P_{DC6} and P_{DC7}).*

Table 2-11 • **Quiescent Supply Current (I_{DD}), No IGLOO Flash*Freeze Mode[1]**

	Core Voltage	AGL015	AGL030	AGL060	AGL125	AGL250	AGL600	AGL1000	Units
I_{CCA} Current[2]									
Typical (25°C)	1.2 V	5	6	10	13	18	28	42	µA
	1.5 V	14	16	20	28	44	82	137	µA
I_{CCI} or I_{JTAG} Current[3, 4]									
V_{CCI}/V_{JTAG} = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	1.7	1.7	1.7	1.7	µA
V_{CCI} / V_{JTAG} = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	1.8	1.8	1.8	1.8	µA
V_{CCI}/V_{JTAG} = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	1.9	1.9	1.9	1.9	µA
V_{CCI}/V_{JTAG} = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	2.2	2.2	2.2	2.2	µA
V_{CCI}/V_{JTAG} = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	2.5	2.5	2.5	2.5	µA

Notes:

1. *To calculate total device I_{DD}, multiply the number of banks used by I_{CCI} and add I_{CCA} contribution.*
2. *Includes V_{CC}, V_{PUMP} and V_{CCPLL} currents.*
3. *Per V_{CCI} or V_{JTAG} bank*
4. *Values do not include I/O static contribution (P_{DC6} and P_{DC7}).*

Power per I/O Pin

Table 2-12 • **Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to Advanced I/O Banks**

	V_{CCI} (V)	Static Power P_{DC6} (mW)[1]	Dynamic Power P_{AC9} (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	16.27
2.5 V LVCMOS	2.5	–	4.65
1.8 V LVCMOS	1.8	–	1.61
1.5 V LVCMOS (JESD8-11)	1.5	–	0.96
1.2 V LVCMOS[3]	1.2	–	0.58
3.3 V PCI	3.3	–	17.67
3.3 V PCI-X	3.3	–	17.67
Differential			
LVDS	2.5	2.26	0.89
LVPECL	3.3	5.72	1.63

Notes:

1. *P_{DC6} is the static power (where applicable) measured on V_{CCI}.*
2. *P_{AC9} is the total dynamic power measured on V_{CCI}.*
3. *Applicable for IGLOO V2 devices only*

Table 2-13 • **Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to Standard Plus I/O Banks**

	V_{CCI} (V)	Static Power P_{DC6} (mW)[1]	Dynamic Power P_{AC9} (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	16.41
2.5 V LVCMOS	2.5	–	4.75
1.8 V LVCMOS	1.8	–	1.66
1.5 V LVCMOS (JESD8-11)	1.5	–	1.00
1.2 V LVCMOS[3]	1.2	–	0.61
3.3 V PCI	3.3	–	17.78
3.3 V PCI-X	3.3	–	17.78

Notes:

1. *P_{DC6} is the static power (where applicable) measured on V_{CCI}.*
2. *P_{AC9} is the total dynamic power measured on V_{CCI}.*
3. *Applicable for IGLOO V2 devices only.*

Table 2-14 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to Standard I/O Banks

	V_{CCI} (V)	Static Power P_{DC6} (mW)[1]	Dynamic Power P_{AC9} (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	17.24
2.5 V LVCMOS	2.5	–	5.64
1.8 V LVCMOS	1.8	–	2.63
1.5 V LVCMOS (JESD8-11)	1.5	–	1.97
1.2 V LVCMOS[3]	1.2	–	0.57

Notes:

1. *P_{DC6} is the static power (where applicable) measured on V_{CCI}.*
2. *P_{AC9} is the total dynamic power measured on V_{CCI}.*
3. *Applicable for IGLOO V2 devices only.*

Table 2-15 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1] Applicable to Advanced I/O Banks

	C_{LOAD} (pF)	V_{CCI} (V)	Static Power P_{DC7} (mW)[2]	Dynamic Power P_{AC10} (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	5	3.3	–	136.95
2.5 V LVCMOS	5	2.5	–	76.84
1.8 V LVCMOS	5	1.8	–	49.31
1.5 V LVCMOS (JESD8-11)	5	1.5	–	33.36
1.2 V LVCMOS[4]	5	1.2		16.24
3.3 V PCI	10	3.3	–	194.05
3.3 V PCI-X	10	3.3	–	194.05
Differential				
LVDS	–	2.5	7.74	78.72
LVPECL	–	3.3	19.54	143.99

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *P_{DC7} is the static power (where applicable) measured on V_{CCI}.*
3. *P_{AC10} is the total dynamic power measured on V_{CCI}.*
4. *Applicable for IGLOO V2 devices only.*

Table 2-16 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1] Applicable to Standard Plus I/O Banks

	C_{LOAD} (pF)	V_{CCI} (V)	Static Power P_{DC7} (mW)[2]	Dynamic Power P_{AC10} (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	5	3.3	–	122.16
2.5 V LVCMOS	5	2.5	–	68.37
1.8 V LVCMOS	5	1.8	–	34.53
1.5 V LVCMOS (JESD8-11)	5	1.5	–	23.66
1.2 V LVCMOS[4]	5	1.2	–	14.90
3.3 V PCI	10	3.3	–	181.06
3.3 V PCI-X	10	3.3	–	181.06

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *P_{DC7} is the static power (where applicable) measured on V_{CCI}.*
3. *P_{AC10} is the total dynamic power measured on V_{CCI}.*
4. *Applicable for IGLOO V2 devices only.*

Table 2-17 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1] Applicable to Standard I/O Banks

	C_{LOAD} (pF)	V_{CCI} (V)	Static Power P_{DC7} (mW)[2]	Dynamic Power P_{AC10} (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	5	3.3	–	104.38
2.5 V LVCMOS	5	2.5	–	59.86
1.8 V LVCMOS	5	1.8	–	31.26
1.5 V LVCMOS (JESD8-11)	5	1.5	–	21.96
1.2 V LVCMOS[4]	5	1.2	–	13.49

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *P_{DC7} is the static power (where applicable) measured on V_{CCI}.*
3. *P_{AC10} is the total dynamic power measured on V_{CCI}.*
4. *Applicable for IGLOO V2 devices only.*

Power Consumption of Various Internal Resources

Table 2-18 • **Different Components Contributing to Dynamic Power Consumption in IGLOO Devices For IGLOO V2 or V5 Devices, 1.5 V DC Core Supply Voltage**

Parameter	Definition	Device Specific Dynamic Power (µW/MHz)						
		AGL1000	AGL600	AGL250	AGL125	AGL060	AGL030	AGL015
P_{AC1}	Clock contribution of a Global Rib	14.48	12.77	11.03	11.03	9.3	9.3	9.3
P_{AC2}	Clock contribution of a Global Spine	2.48	1.85	1.58	0.81	0.81	0.41	0.41
P_{AC3}	Clock contribution of a VersaTile row	0.81						
P_{AC4}	Clock contribution of a VersaTile used as a sequential module	0.11						
P_{AC5}	First contribution of a VersaTile used as a sequential module	0.057						
P_{AC6}	Second contribution of a VersaTile used as a sequential module	0.207						
P_{AC7}	Contribution of a VersaTile used as a combinatorial module	0.17						
P_{AC8}	Average contribution of a routing net	0.7						
P_{AC9}	Contribution of an I/O input pin (standard-dependent)	See Table 2-12 on page 2-9 through Table 2-14 on page 2-10.						
P_{AC10}	Contribution of an I/O output pin (standard-dependent)	See Table 2-15 on page 2-10 through Table 2-17 on page 2-11.						
P_{AC11}	Average contribution of a RAM block during a read operation	25.00						
P_{AC12}	Average contribution of a RAM block during a write operation	30.00						
P_{AC13}	Dynamic PLL contribution	2.70						

* *For a different output load, drive strength, or slew rate, Actel recommends using the Actel power spreadsheet calculator or SmartPower tool in Actel Libero® Integrated Design Environment (IDE).*

Table 2-19 • **Different Components Contributing to the Static Power Consumption in IGLOO Devices For IGLOO V2 or V5 Devices, 1.5 V DC Core Supply Voltage**

Parameter	Definition	Device-Specific Static Power (mW)						
		AGL1000	AGL600	AGL250	AGL125	AGL060	AGL030	AGL015
P_{DC1}	Array static power in Active mode	See Table 2-11 on page 2-8.						
P_{DC2}	Array static power in Static (Idle) mode	See Table 2-10 on page 2-7.						
P_{DC3}	Array static power in Flash*Freeze mode	See Table 2-8 on page 2-7.						
P_{DC4}	Static PLL contribution	1.84						
P_{DC5}	Bank quiescent power (V_{CCI}-dependent)	See Table 2-11 on page 2-8.						
P_{DC6}	I/O input pin static power (standard-dependent)	See Table 2-12 on page 2-9 through Table 2-14 on page 2-10.						
P_{DC7}	I/O output pin static power (standard-dependent)	See Table 2-15 on page 2-10 through Table 2-17 on page 2-11.						

Table 2-20 • **Different Components Contributing to Dynamic Power Consumption in IGLOO Devices For IGLOO V2 Devices, 1.2 V DC Core Supply Voltage**

Parameter	Definition	Device Specific Dynamic Power (µW/MHz)						
		AGL1000	AGL600	AGL250	AGL125	AGL060	AGL030	AGL015
P_{AC1}	Clock contribution of a Global Rib	9.28	8.19	7.07	7.07	5.96	5.96	5.96
P_{AC2}	Clock contribution of a Global Spine	1.59	1.19	1.01	0.52	0.52	0.26	0.26
P_{AC3}	Clock contribution of a VersaTile row	0.52						
P_{AC4}	Clock contribution of a VersaTile used as a sequential module	0.07						
P_{AC5}	First contribution of a VersaTile used as a sequential module	0.045						
P_{AC6}	Second contribution of a VersaTile used as a sequential module	0.186						
P_{AC7}	Contribution of a VersaTile used as a combinatorial module	0.11						
P_{AC8}	Average contribution of a routing net	0.45						
P_{AC9}	Contribution of an I/O input pin (standard-dependent)	See Table 2-12 on page 2-9 through Table 2-14 on page 2-10.						
P_{AC10}	Contribution of an I/O output pin (standard-dependent)	See Table 2-15 on page 2-10 through Table 2-17 on page 2-11.						
P_{AC11}	Average contribution of a RAM block during a read operation	25.00						
P_{AC12}	Average contribution of a RAM block during a write operation	30.00						
P_{AC13}	Dynamic PLL contribution	2.10						

* *For a different output load, drive strength, or slew rate, Actel recommends using the Actel power spreadsheet calculator or SmartPower tool in Libero IDE.*

Table 2-21 • **Different Components Contributing to the Static Power Consumption in IGLOO Device For IGLOO V2 Devices, 1.2 V DC Core Supply Voltage**

Parameter	Definition	Device Specific Static Power (mW)						
		AGL1000	AGL600	AGL250	AGL125	AGL060	AGL030	AGL015
P_{DC1}	Array static power in Active mode	See Table 2-11 on page 2-8.						
P_{DC2}	Array static power in Static (Idle) mode	See Table 2-10 on page 2-7.						
P_{DC3}	Array static power in Flash*Freeze mode	See Table 2-8 on page 2-7.						
P_{DC4}	Static PLL contribution	0.90						
P_{DC5}	Bank quiescent power (V_{CCI}-Dependent)	See Table 2-11 on page 2-8.						
P_{DC6}	I/O input pin static power (standard-dependent)	See Table 2-12 on page 2-9 through Table 2-14 on page 2-10.						
P_{DC7}	I/O output pin static power (standard-dependent)	See Table 2-15 on page 2-10 through Table 2-17 on page 2-11.						

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Actel Libero IDE software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-22 on page 2-18.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-23 on page 2-18.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-23 on page 2-18. The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—P_{TOTAL}

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

$P_{STAT} = (P_{DC1}$ or P_{DC2} or $P_{DC3}) + N_{BANKS} * P_{DC5} + N_{INPUTS} * P_{DC6} + N_{OUTPUTS} * P_{DC7}$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

N_{BANKS} is the number of I/O banks powered in the design.

Total Dynamic Power Consumption—P_{DYN}

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$

Global Clock Contribution—P_{CLOCK}

$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * P_{AC3} + N_{S\text{-}CELL} * P_{AC4}) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in Table 2-22 on page 2-18.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in Table 2-22 on page 2-18.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

P_{AC1}, P_{AC2}, P_{AC3}, and P_{AC4} are device-dependent.

Sequential Cells Contribution—$P_{S\text{-}CELL}$

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (P_{AC5} + \alpha_1 / 2 * P_{AC6}) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-22 on page 2-18.

F_{CLK} is the global clock signal frequency.

Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha_1 / 2 * P_{AC7} * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-22 on page 2-18.

F_{CLK} is the global clock signal frequency.

Routing Net Contribution—P_{NET}

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 / 2 * P_{AC8} * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-22 on page 2-18.

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution—P_{INPUTS}

$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-22 on page 2-18.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * P_{AC10} * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-22 on page 2-18.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-23 on page 2-18.

F_{CLK} is the global clock signal frequency.

RAM Contribution—P_{MEMORY}

$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + P_{AC12} * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-23 on page 2-18.

PLL Contribution—P_{PLL}

$P_{PLL} = P_{DC4} + P_{AC13} * F_{CLKOUT}$

F_{CLKOUT} is the output clock frequency.[1]

1. *If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC13} * F_{CLKOUT}$ product) to the total PLL contribution.*

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 2-22 • **Toggle Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 2-23 • **Enable Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%

User I/O Characteristics

Timing Model

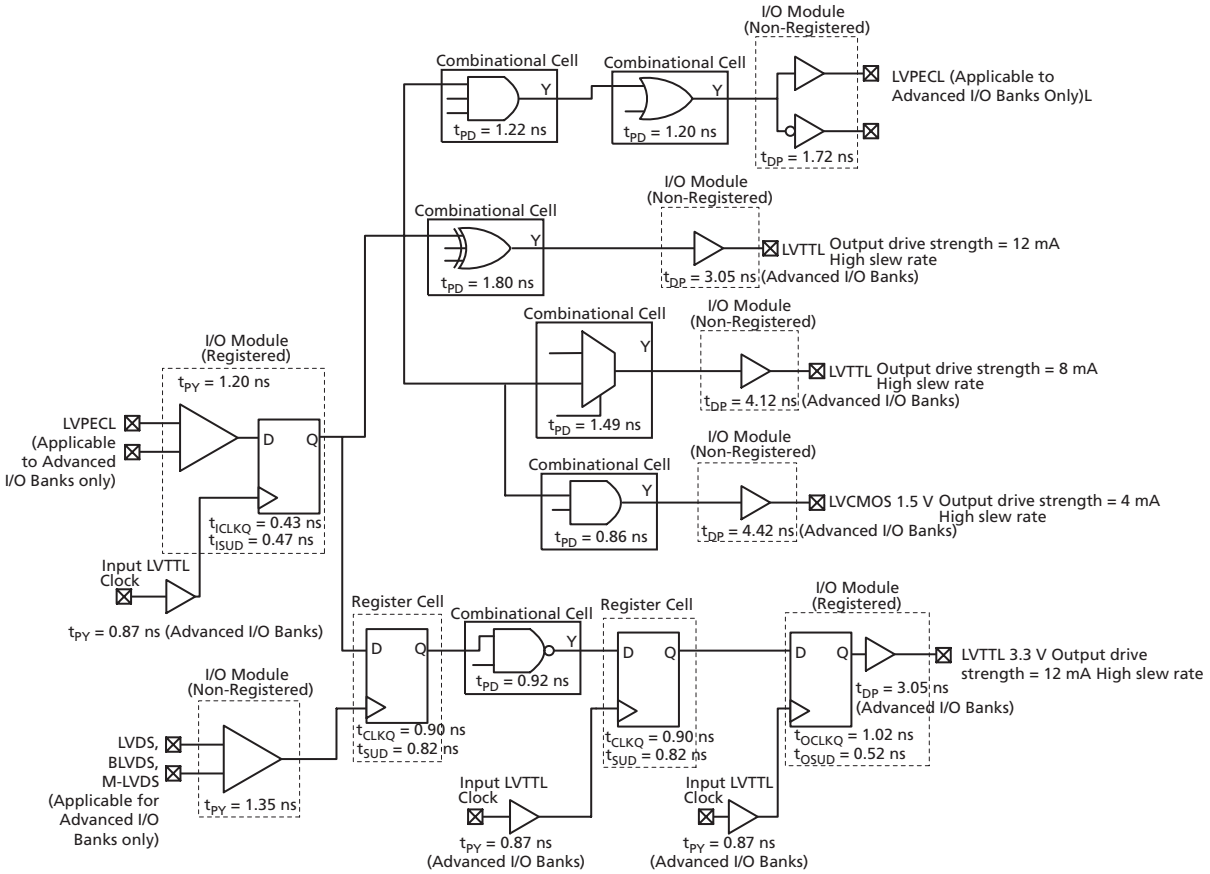


Figure 2-3 • **Timing Model**
Operating Conditions: Std. Speed, Commercial Temperature Range (T_J = 70°C), Worst-Case V_{CC} = 1.425 V, for DC 1.5 V Core Voltage, Applicable to V2 and V5 Devices

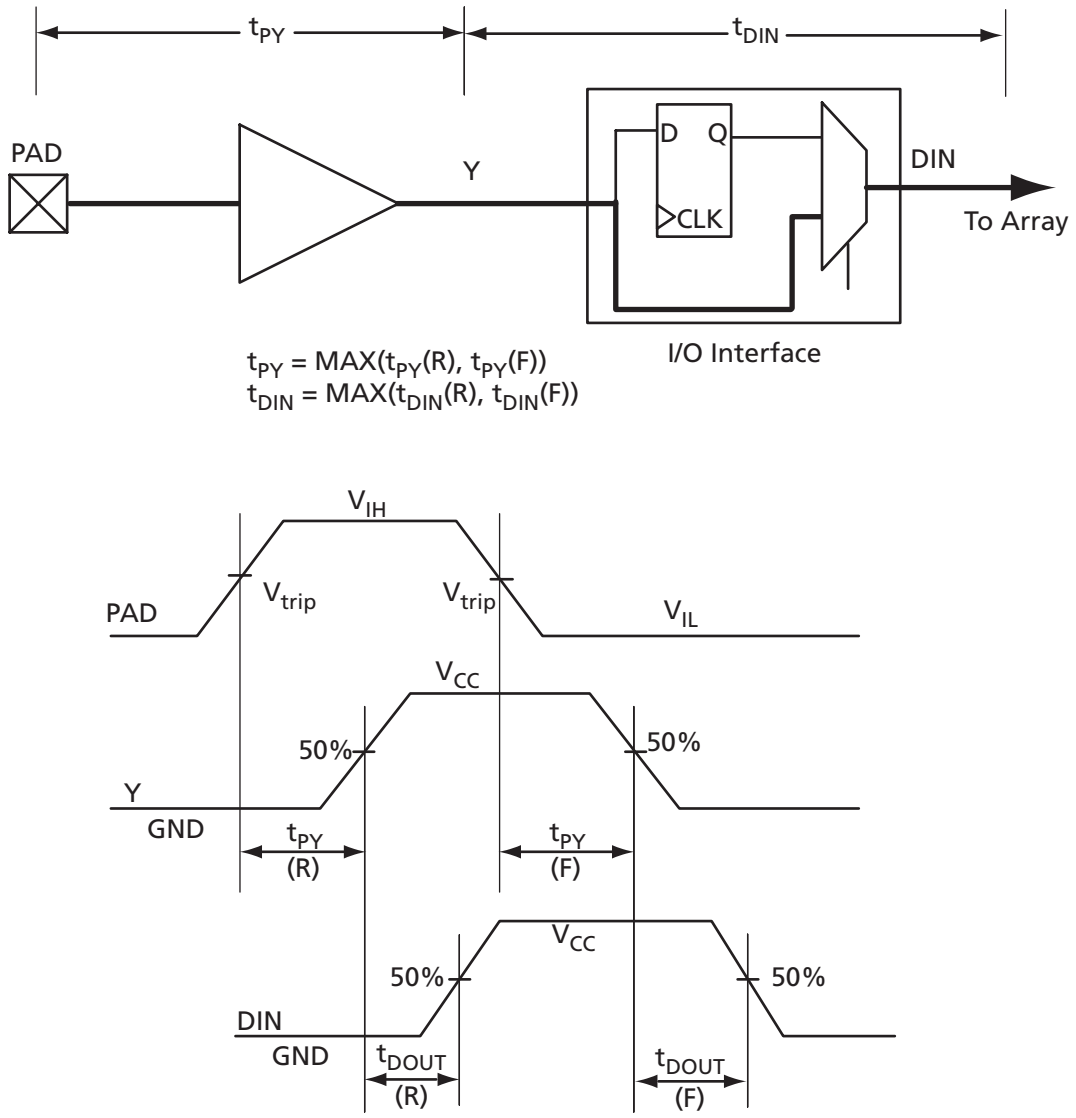


Figure 2-4 • **Input Buffer Timing Model and Delays (example)**

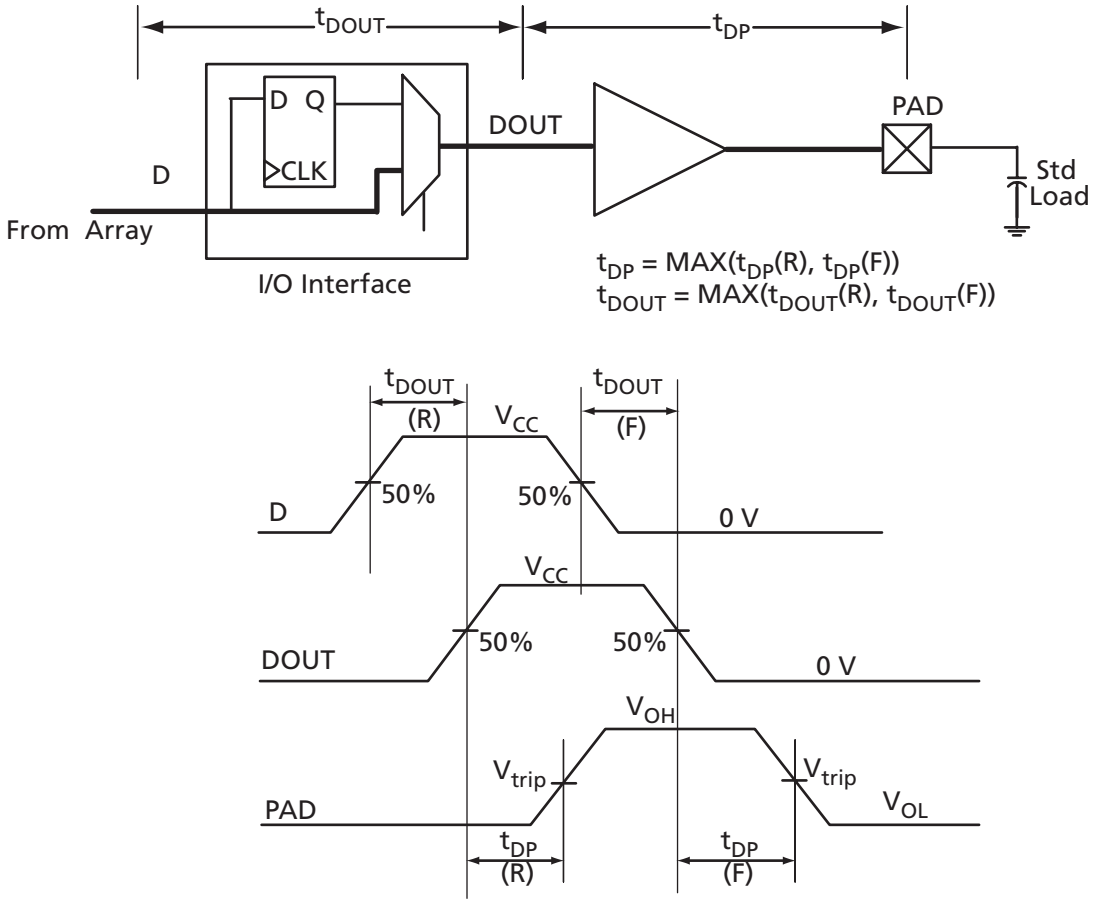


Figure 2-5 • **Output Buffer Model and Delays (example)**

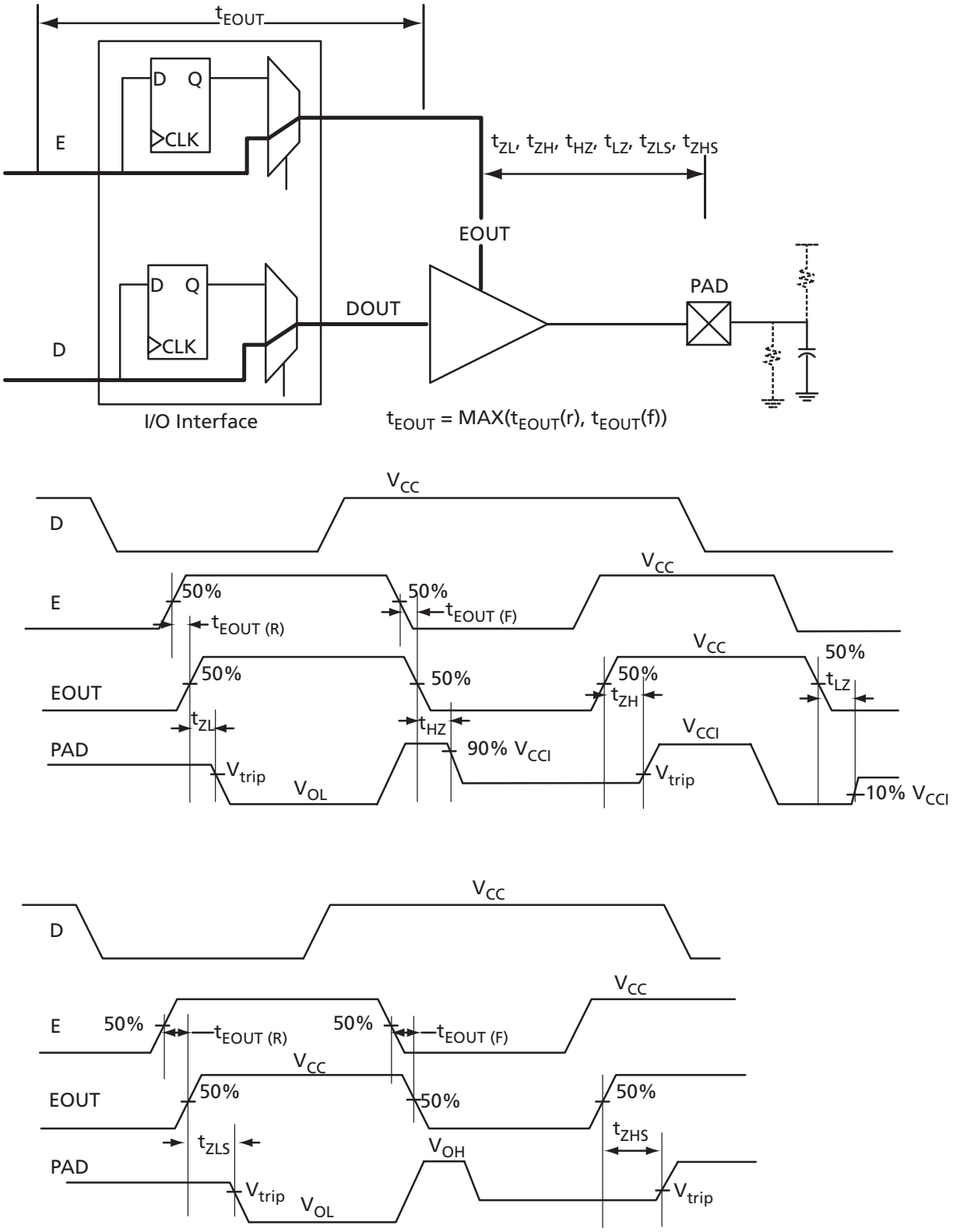


Figure 2-6 • **Tristate Output Buffer Timing Model and Delays (example)**

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-24 • **Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings Applicable to Advanced I/O Banks**

I/O Standard	Drive Strength	Slew Rate	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}[1]	I_{OH}[1]
			Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range	Any[2]	High	–0.3	0.8	2	3.6	0.2	V_{CCI} – 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	12	12
1.5 V LVCMOS	12 mA	High	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	12	12
1.2 V LVCMOS[3]	2 mA	High	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.26	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2
3.3 V PCI	Per PCI specifications									
3.3 V PCI-X	Per PCI-X specifications									

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *All LVMCOS 3.3 V software macros support LVCMOS 3.3 V wide range as specificied in the JDEC8a specification.*
3. *Applicable to V2 Devices only.*

Table 2-25 • **Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings Applicable to Standard Plus I/O Banks**

I/O Standard	Drive Strength	Slew Rate	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
			Min., V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range	Any[2]	High	–0.3	0.8	2	3.6	0.2	V_{CCI} – 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	8 mA	High	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	8	8
1.5 V LVCMOS	4 mA	High	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	4	4
1.2 V LVCMOS[3]	2 mA	High	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.26	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2
3.3 V PCI	Per PCI specifications									
3.3 V PCI-X	Per PCI-X specifications									

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *All LVMCOS 3.3 V software macros support LVCMOS 3.3 V wide range as specificied in the JDEC8a specification.*
3. *Applicable to V2 Devices only.*

Table 2-26 • **Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings Applicable to Standard I/O Banks**

I/O Standard	Drive Strength	Slew Rate	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}[1]	I_{OH}[1]
			Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	High	–0.3	0.8	2	3.6	0.4	2.4	8	8
3.3 V LVCMOS Wide Range	Any[2]	High	–0.3	0.8	2	3.6	0.2	V_{CCI} – 0.2	0.1	0.1
2.5 V LVCMOS	8 mA	High	–0.3	0.7	1.7	2.7	0.7	1.7	8	8
1.8 V LVCMOS	4 mA	High	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	4	4
1.5 V LVCMOS	2 mA	High	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2
1.2 V LVCMOS[3]	1 mA	High	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.26	0.25 * V_{CCI}	0.75 * V_{CCI}	1	1

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *All LVMCOS 3.3 V software macros support LVCMOS 3.3 V wide range as specificied in the JDEC8a specification.*
3. *Applicable to V2 Devices only.*

Table 2-27 • **Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions**

DC I/O Standards	Commercial[1]		Industrial[2]	
	I_{IL}	I_{IH}	I_{IL}	I_{IH}
	µA	µA	µA	µA
3.3 V LVTTL / 3.3 V LVCMOS	10	10	15	15
3.3 V LVCMOS Wide Range	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
1.2 V LVCMOS[3]	10	10	15	15
3.3 V PCI	10	10	15	15
3.3 V PCI-X	10	10	15	15

Notes:

1. *Commercial range (0°C < T_A < 70°C)*
2. *Industrial range (–40°C < T_A < 85°C)*
3. *Applicable to V2 Devices only.*

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-28 • **Summary of AC Measuring Points**

Standard	Measuring Trip Point (V_{trip})
3.3 V LVTTL / 3.3 V LVCMOS	1.4 V
2.5 V LVCMOS	1.2 V
1.8 V LVCMOS	0.90 V
1.5 V LVCMOS	0.75 V
1.2 V LVCMOS	0.60 V
3.3 V PCI	0.285 * V_{CCI} (RR)
	0.615 * V_{CCI} (FF)
3.3 V PCI-X	0.285 * V_{CCI} (RR)
	0.615 * V_{CCI} (FF)

Table 2-29 • **I/O AC Parameter Definitions**

Parameter	Parameter Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{HZ}	Enable to Pad delay through the Output Buffer—HIGH to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to HIGH
t_{LZ}	Enable to Pad delay through the Output Buffer—LOW to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to LOW
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to HIGH
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to LOW

Table 2-30 • **Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V Applicable to Advanced I/O Banks**

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	5 pF	–	0.97	2.09	0.19	0.85	0.66	2.13	1.67	2.67	3.04	5.66	5.20	ns
2.5 V LVCMOS	12 mA	High	5 pF	–	0.97	2.09	0.19	1.07	0.66	2.13	1.82	2.73	2.93	5.66	5.35	ns
1.8 V LVCMOS	12 mA	High	5 pF	–	0.97	2.24	0.19	1.01	0.66	2.28	1.99	3.02	3.39	5.81	5.52	ns
1.5 V LVCMOS	12 mA	High	5 pF	–	0.97	2.50	0.19	1.17	0.66	2.55	2.26	3.20	3.48	6.08	5.79	ns
3.3 V PCI	Per PCI spec	High	10pF	25 [2]	0.97	2.32	0.19	0.73	0.66	2.36	1.77	2.67	3.04	5.89	5.30	ns
3.3 V PCI-X	Per PCI-X spec	High	10pF	25 [2]	0.97	2.32	0.19	0.70	0.66	2.36	1.77	2.67	3.04	5.89	5.30	ns
LVDS	24 mA	High	–	–	0.97	1.67	0.19	1.31	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	0.97	1.67	0.19	1.16	–	–	–	–	–	–	–	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-62 for connectivity. This resistor is not required during normal operation.*

Table 2-31 • Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V Applicable to Standard Plus I/O Banks

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	5 pF	–	0.97	1.75	0.19	0.85	0.66	1.78	1.39	2.36	2.79	5.31	4.92	ns
2.5 V LVCMOS	12 mA	High	5 pF	–	0.97	1.75	0.19	1.08	0.66	1.78	1.51	2.38	2.69	5.32	5.04	ns
1.8 V LVCMOS	8 mA	High	5 pF	–	0.97	1.97	0.19	1.01	0.66	2.01	1.76	2.46	2.66	5.54	5.29	ns
1.5 V LVCMOS	4 mA	High	5 pF	–	0.97	2.25	0.19	1.17	0.66	2.29	1.99	2.53	2.68	5.82	5.52	ns
3.3 V PCI	Per PCI spec	High	10pF	25 [2]	0.97	1.96	0.19	0.73	0.66	2.00	1.50	2.36	2.79	5.53	5.03	ns
3.3 V PCI-X	Per PCI-X spec	High	10pF	25 [2]	0.97	1.96	0.19	0.70	0.66	2.00	1.50	2.36	2.79	5.53	5.03	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-62 for connectivity. This resistor is not required during normal operation.*

Table 2-32 • Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V Applicable to Standard I/O Banks

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	High	5 pF	–	0.97	1.85	0.19	0.83	0.66	1.88	1.45	1.96	2.26	ns
2.5 V LVCMOS	8 mA	High	5 pF	–	0.97	1.88	0.19	1.04	0.66	1.92	1.62	1.95	2.14	ns
1.8 V LVCMOS	4 mA	High	5 pF	–	0.97	2.18	0.19	0.98	0.66	2.22	1.93	1.96	2.06	ns
1.5 V LVCMOS	2 mA	High	5 pF	–	0.97	2.51	0.19	1.13	0.66	2.56	2.20	1.99	2.03	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-62 for connectivity. This resistor is not required during normal operation.*

Table 2-33 • **Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V Applicable to Advanced I/O Banks**

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	5 pF	–	1.55	2.66	0.26	0.98	1.10	2.71	2.18	3.23	3.92	8.52	7.99	ns
2.5 V LVCMOS	12 mA	High	5 pF	–	1.55	2.63	0.26	1.20	1.10	2.68	2.30	3.28	3.77	8.48	8.10	ns
1.8 V LVCMOS	12 mA	High	5 pF	–	1.55	2.71	0.26	1.11	1.10	2.76	2.44	3.56	4.17	8.57	8.24	ns
1.5 V LVCMOS	12 mA	High	5 pF	–	1.55	2.95	0.26	1.27	1.10	3.00	2.70	3.74	4.21	8.81	8.51	ns
1.2 V LVCMOS	2 mA	High	5 p	–	1.55	3.61	0.26	1.58	1.10	3.45	3.33	3.94	3.66	9.05	8.93	ns
3.3 V PCI	Per PCI spec	High	10pF	25 [2]	1.55	2.90	0.26	0.86	1.10	2.95	2.29	3.23	3.92	8.76	8.10	ns
3.3 V PCI-X	Per PCI-X spec	High	10pF	25 [2]	1.55	2.90	0.25	0.86	1.10	2.95	2.29	3.23	3.92	8.76	8.10	ns
LVDS	24 mA	High	–	–	1.55	2.19	0.25	1.52	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	1.55	2.24	0.25	1.37	–	–	–	–	–	–	–	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-62 for connectivity. This resistor is not required during normal operation.*

Table 2-34 • **Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V Applicable to Standard Plus I/O Banks**

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	5 pF	–	1.55	2.30	0.26	0.97	1.10	2.34	1.87	2.91	3.62	8.15	7.67	ns
2.5 V LVCMOS	12 mA	High	5 pF	–	1.55	2.28	0.26	1.20	1.10	2.32	1.95	2.92	3.50	8.13	7.75	ns
1.8 V LVCMOS	8 mA	High	5 pF	–	1.55	2.42	0.26	1.11	1.10	2.47	2.16	2.98	3.38	8.28	7.97	ns
1.5 V LVCMOS	4 mA	High	5 pF	–	1.55	2.67	0.26	1.27	1.10	2.72	2.39	3.05	3.36	8.53	8.20	ns
1.2 V LVCMOS	2 mA	High	5 pF	–	1.55	3.23	0.26	1.58	1.10	3.09	2.76	3.30	3.49	8.69	8.36	ns
3.3 V PCI	Per PCI spec	High	10pF	25 [2]	1.55	2.52	0.26	0.85	1.10	2.57	1.98	2.91	3.62	8.37	7.78	ns
3.3 V PCI-X	Per PCI-X spec	High	10pF	25 [2]	1.55	2.52	0.25	0.85	1.10	2.57	1.98	2.91	3.62	8.37	7.78	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-62 for connectivity. This resistor is not required during normal operation.*

Table 2-35 • **Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V Applicable to Standard I/O Banks**

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	High	5 pF	–	1.55	2.37	0.26	0.94	1.10	2.42	1.92	2.39	2.94	ns
2.5 V LVCMOS	8 mA	High	5 pF	–	1.55	2.38	0.26	1.15	1.10	2.42	2.05	2.37	2.79	ns
1.8 V LVCMOS	4 mA	High	5 pF	–	1.55	2.60	0.26	1.08	1.10	2.64	2.33	2.37	2.61	ns
1.5 V LVCMOS	2 mA	High	5 pF	–	1.55	2.91	0.26	1.22	1.10	2.96	2.60	2.39	2.54	ns
1.2 V LVCMOS	1 mA	High	5 pF	–	1.55	3.60	0.26	1.52	1.10	3.45	3.04	2.52	2.50	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-62 for connectivity. This resistor is not required during normal operation.*

Detailed I/O DC Characteristics

Table 2-36 • **Input Capacitance**

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	V_{IN} = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	V_{IN} = 0, f = 1.0 MHz		8	pF

Table 2-37 • **I/O Output Buffer Maximum Resistances[1] Applicable to Advanced I/O Banks**

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
1.8 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
1.2 V LVCMOS	2 mA	TBD	TBD
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at http://www.actel.com/download/ibis/default.aspx.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

Table 2-38 • **I/O Output Buffer Maximum Resistances[1] Applicable to Standard Plus I/O Banks**

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	25	75
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
1.2 V LVCMOS	2 mA	TBD	TBD
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at http://www.actel.com/download/ibis/default.aspx.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

Table 2-39 • **I/O Output Buffer Maximum Resistances[1]**
Applicable to Standard I/O Banks

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
1.5 V LVCMOS	2 mA	200	224
1.2 V LVCMOS	1 mA	TBD	TBD

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at http://www.actel.com/download/ibis/default.aspx.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} – V_{OHspec}) / I_{OHspec}$

Table 2-40 • **I/O Weak Pull-Up/Pull-Down Resistances**
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

	$R_{(WEAK\ PULL\text{-}UP)}$[1] (Ω)		$R_{(WEAK\ PULL\text{-}DOWN)}$[2] (Ω)	
V_{CCI}	Min.	Max.	Min.	Max.
3.3 V	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k
1.2 V	TBD	TBD	TBD	TBD

Notes:

1. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (V_{OLspec}) / I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$
2. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} – V_{OHspec}) / I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$

Table 2-41 • **I/O Short Currents I_{OSH}/I_{OSL} Applicable to Advanced I/O Banks**

	Drive Strength	I_{OSL} (mA)*	I_{OSH} (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
1.2 V LVCMOS	2 mA	TBD	TBD
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	103	109

* $T_J = 100°C$

Table 2-42 • **I/O Short Currents I_{OSH}/I_{OSL} Applicable to Standard Plus I/O Banks**

	Drive Strength	I_{OSL} (mA)*	I_{OSH} (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	103	109
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
	12 mA	65	74
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	35	44
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
1.2 V LVCMOS	2 mA	TBD	TBD
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	103	109

* *T_J = 100°C*

Table 2-43 • **I/O Short Currents I_{OSH}/I_{OSL} Applicable to Standard I/O Banks**

	Drive Strength	I_{OSL} (mA)*	I_{OSH} (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
1.5 V LVCMOS	2 mA	13	16
1.2 V LVCMOS	1 mA	TBD	TBD

* *T_J = 100°C*

The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 110°C, the short current condition would have to be sustained for more than three months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-44 • **Short Current Event Duration before Failure**

Temperature	Time before Failure
–40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months
110°C	3 months

Table 2-45 • **I/O Input Rise Time, Fall Time, and Related I/O Reliability**

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS	No requirement	10 ns *	20 years (110°C)
LVDS/BLVDS/M-LVDS/ LVPECL	No requirement	10 ns *	10 years (100°C)

* *The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Actel recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer. Furthermore, all LVCMOS 3.3 V software macros comply with LVCMOS 3.3 V wide range as specified in the JESD8a specification.

Table 2-46 • **Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks**

3.3 V LVTTL / 3.3 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	10	10
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	132	127	10	10
24 mA	–0.3	0.8	2	3.6	0.4	2.4	24	24	268	181	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-47 • **Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks**

3.3 V LVTTL / 3.3 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	103	109	10	10
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	103	109	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-48 • **Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks**

3.3 V LVTTL / 3.3 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-49 • **Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range Applicable to Advanced, Standard Plus, and Standard I/O Banks**

3.3 V LVCMOS Wide Range	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	µA[2]	µA[2]
All[2]	–0.3	0.8	2	3.6	0.2	V_{CCI} – 0.2	0.1	0.1	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *All LVMCOS 3.3 V software macros support LVCMOS 3.3 V wide range as specificied in the JDEC8a specification.*

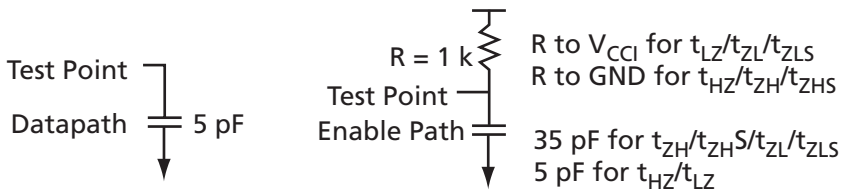


Figure 2-7 • **AC Loading**

Table 2-50 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	3.3	1.4	5

* *Measuring point = V_{trip}. See Table 2-28 on page 2-25 for a complete table of trip points.*

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-51 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.97	4.46	0.19	0.85	0.66	4.55	3.88	2.24	2.19	8.08	7.41	ns
6 mA	Std.	0.97	3.74	0.19	0.85	0.66	3.81	3.36	2.49	2.63	7.34	6.89	ns
8 mA	Std.	0.97	3.74	0.19	0.85	0.66	3.81	3.36	2.49	2.63	7.34	6.89	ns
12 mA	Std.	0.97	3.23	0.19	0.85	0.66	3.29	2.97	2.66	2.91	6.82	6.50	ns
16 mA	Std.	0.97	3.08	0.19	0.85	0.66	3.13	2.88	2.70	2.99	6.66	6.41	ns
24 mA	Std.	0.97	3.00	0.19	0.85	0.66	3.05	2.90	2.74	3.27	6.58	6.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-52 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.97	2.73	0.19	0.85	0.66	2.78	2.21	2.25	2.31	6.31	5.74	ns
6 mA	Std.	0.97	2.31	0.19	0.85	0.66	2.36	1.84	2.50	2.76	5.89	5.37	ns
8 mA	Std.	0.97	2.31	0.19	0.85	0.66	2.36	1.84	2.50	2.76	5.89	5.37	ns
12 mA	Std.	0.97	2.09	0.19	0.85	0.66	2.13	1.67	2.67	3.04	5.66	5.20	ns
16 mA	Std.	0.97	2.05	0.19	0.85	0.66	2.09	1.63	2.70	3.12	5.62	5.16	ns
24 mA	Std.	0.97	2.07	0.19	0.85	0.66	2.11	1.59	2.75	3.41	5.64	5.12	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-53 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.97	3.94	0.19	0.85	0.66	4.01	3.45	1.98	2.02	7.54	6.98	ns
6 mA	Std.	0.97	3.24	0.19	0.85	0.66	3.30	2.98	2.20	2.42	6.83	6.51	ns
8 mA	Std.	0.97	3.24	0.19	0.85	0.66	3.30	2.98	2.20	2.42	6.83	6.51	ns
12 mA	Std.	0.97	2.76	0.19	0.85	0.66	2.81	2.62	2.36	2.68	6.35	6.15	ns
16 mA	Std.	0.97	2.76	0.19	0.85	0.66	2.81	2.62	2.36	2.68	6.35	6.15	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-54 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.97	2.32	0.19	0.85	0.66	2.36	1.89	1.98	2.13	5.89	5.42	ns
6 mA	Std.	0.97	1.94	0.19	0.85	0.66	1.98	1.56	2.20	2.53	5.51	5.09	ns
8 mA	Std.	0.97	1.94	0.19	0.85	0.66	1.98	1.56	2.20	2.53	5.51	5.09	ns
12 mA	Std.	0.97	1.75	0.19	0.85	0.66	1.78	1.39	2.36	2.79	5.31	4.92	ns
16 mA	Std.	0.97	1.75	0.19	0.85	0.66	1.78	1.39	2.36	2.79	5.31	4.92	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-55 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	3.80	0.19	0.83	0.66	3.87	3.40	1.74	1.78	ns
4 mA	Std.	0.97	3.80	0.19	0.83	0.66	3.87	3.40	1.74	1.78	ns
6 mA	Std.	0.97	3.15	0.19	0.83	0.66	3.20	2.93	1.96	2.17	ns
8 mA	Std.	0.97	3.15	0.19	0.83	0.66	3.20	2.93	1.96	2.17	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-56 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	2.19	0.19	0.83	0.66	2.23	1.79	1.74	1.87	ns
4 mA	Std.	0.97	2.19	0.19	0.83	0.66	2.23	1.79	1.74	1.87	ns
6 mA	Std.	0.97	1.85	0.19	0.83	0.66	1.88	1.45	1.96	2.26	ns
8 mA	Std.	0.97	1.85	0.19	0.83	0.66	1.88	1.45	1.96	2.26	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Applies to 1.2 V DC Core Voltage

Table 2-57 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	1.55	5.11	0.26	0.98	1.10	5.21	4.47	2.80	3.01	11.01	10.28	ns
6 mA	Std.	1.55	4.37	0.26	0.98	1.10	4.45	3.93	3.05	3.46	10.26	9.74	ns
8 mA	Std.	1.55	4.37	0.26	0.98	1.10	4.45	3.93	3.05	3.46	10.26	9.74	ns
12 mA	Std.	1.55	3.84	0.26	0.98	1.10	3.91	3.53	3.23	3.75	9.72	9.34	ns
16 mA	Std.	1.55	3.68	0.26	0.98	1.10	3.75	3.44	3.27	3.83	9.56	9.25	ns
24 mA	Std.	1.55	3.60	0.26	0.98	1.10	3.67	3.46	3.31	4.12	9.48	9.27	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-58 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	1.55	3.32	0.26	0.98	1.10	3.38	2.75	2.80	3.16	9.19	8.56	ns
6 mA	Std.	1.55	2.90	0.26	0.98	1.10	2.95	2.37	3.06	3.62	8.76	8.18	ns
8 mA	Std.	1.55	2.90	0.26	0.98	1.10	2.95	2.37	3.06	3.62	8.76	8.18	ns
12 mA	Std.	1.55	2.66	0.26	0.98	1.10	2.71	2.18	3.23	3.92	8.52	7.99	ns
16 mA	Std.	1.55	2.62	0.26	0.98	1.10	2.67	2.15	3.27	3.99	8.48	7.95	ns
24 mA	Std.	1.55	2.64	0.26	0.98	1.10	2.69	2.10	3.32	4.29	8.50	7.91	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

Table 2-59 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	1.55	4.55	0.26	0.97	1.10	4.64	3.98	2.52	2.81	10.44	9.79	ns
6 mA	Std.	1.55	3.83	0.26	0.97	1.10	3.90	3.50	2.75	3.22	9.71	9.31	ns
8 mA	Std.	1.55	3.83	0.26	0.97	1.10	3.90	3.50	2.75	3.22	9.71	9.31	ns
12 mA	Std.	1.55	3.34	0.26	0.97	1.10	3.40	3.13	2.92	3.49	9.21	8.94	ns
16 mA	Std.	1.55	3.34	0.26	0.97	1.10	3.40	3.13	2.92	3.49	9.21	8.94	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-60 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	1.55	2.88	0.26	0.97	1.10	2.93	2.38	2.52	2.94	8.74	8.19	ns
6 mA	Std.	1.55	2.49	0.26	0.97	1.10	2.54	2.04	2.75	3.36	8.35	7.85	ns
8 mA	Std.	1.55	2.49	0.26	0.97	1.10	2.54	2.04	2.75	3.36	8.35	7.85	ns
12 mA	Std.	1.55	2.30	0.26	0.97	1.10	2.34	1.87	2.91	3.62	8.15	7.67	ns
16 mA	Std.	1.55	2.30	0.26	0.97	1.10	2.34	1.87	2.91	3.62	8.15	7.67	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

Table 2-61 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	4.38	0.26	0.94	1.10	4.46	3.91	2.16	2.43	ns
4 mA	Std.	1.55	4.38	0.26	0.94	1.10	4.46	3.91	2.16	2.43	ns
6 mA	Std.	1.55	3.71	0.26	0.94	1.10	3.78	3.43	2.39	2.83	ns
8 mA	Std.	1.55	3.71	0.26	0.94	1.10	3.78	3.43	2.39	2.83	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-62 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	2.73	0.26	0.94	1.10	2.78	2.26	2.16	2.54	ns
4 mA	Std.	1.55	2.73	0.26	0.94	1.10	2.78	2.26	2.16	2.54	ns
6 mA	Std.	1.55	2.37	0.26	0.94	1.10	2.42	1.92	2.39	2.94	ns
8 mA	Std.	1.55	2.37	0.26	0.94	1.10	2.42	1.92	2.39	2.94	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications. It uses a 5 V–tolerant input buffer and push-pull output buffer.

Table 2-63 • **Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks**

2.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	16	18	10	10
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	10	10
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	32	37	10	10
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	10	10
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	10	10
16 mA	–0.3	0.7	1.7	2.7	0.7	1.7	16	16	83	87	10	10
24 mA	–0.3	0.7	1.7	2.7	0.7	1.7	24	24	169	124	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-64 • **Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks**

2.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	16	18	10	10
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	10	10
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	32	37	10	10
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	10	10
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-65 • **Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks**

2.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	16	18	10	10
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	10	10
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	32	37	10	10
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

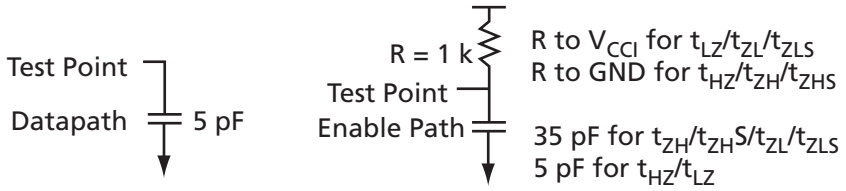


Figure 2-8 • **AC Loading**

Table 2-66 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	2.5	1.2	5

* *Measuring point = V_{trip}. See Table 2-28 on page 2-25 for a complete table of trip points.*

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-67 • **2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.97	4.96	0.19	1.07	0.66	5.05	4.58	2.26	1.99	8.58	8.11	ns
6 mA	Std.	0.97	4.15	0.19	1.07	0.66	4.23	3.93	2.54	2.51	7.76	7.46	ns
8 mA	Std.	0.97	4.15	0.19	1.07	0.66	4.23	3.93	2.54	2.51	7.76	7.46	ns
12 mA	Std.	0.97	3.57	0.19	1.07	0.66	3.64	3.46	2.73	2.83	7.17	6.99	ns
16 mA	Std.	0.97	3.39	0.19	1.07	0.66	3.45	3.35	2.77	2.92	6.98	6.88	ns
24 mA	Std.	0.97	3.37	0.19	1.07	0.66	3.37	3.37	2.83	3.25	6.90	6.90	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-68 • **2.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.97	2.77	0.19	1.07	0.66	2.82	2.59	2.26	2.08	6.35	6.12	ns
6 mA	Std.	0.97	2.34	0.19	1.07	0.66	2.38	2.07	2.54	2.60	5.91	5.60	ns
8 mA	Std.	0.97	2.34	0.19	1.07	0.66	2.38	2.07	2.54	2.60	5.91	5.60	ns
12 mA	Std.	0.97	2.09	0.19	1.07	0.66	2.13	1.82	2.73	2.93	5.66	5.35	ns
16 mA	Std.	0.97	2.04	0.19	1.07	0.66	2.08	1.77	2.77	3.01	5.61	5.31	ns
24 mA	Std.	0.97	2.05	0.19	1.07	0.66	2.09	1.71	2.83	3.35	5.62	5.24	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-69 • **2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.97	4.42	0.19	1.08	0.66	4.50	4.09	1.96	1.85	8.03	7.62	ns
6 mA	Std.	0.97	3.62	0.19	1.08	0.66	3.69	3.51	2.21	2.31	7.22	7.04	ns
8 mA	Std.	0.97	3.62	0.19	1.08	0.66	3.69	3.51	2.21	2.31	7.22	7.04	ns
12 mA	Std.	0.97	3.08	0.19	1.08	0.66	3.14	3.08	2.39	2.61	6.67	6.61	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-70 • 2.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.97	2.36	0.19	1.08	0.66	2.40	2.21	1.96	1.92	5.93	5.74	ns
6 mA	Std.	0.97	1.97	0.19	1.08	0.66	2.00	1.74	2.21	2.39	5.53	5.27	ns
8 mA	Std.	0.97	1.97	0.19	1.08	0.66	2.00	1.74	2.21	2.39	5.53	5.27	ns
12 mA	Std.	0.97	1.75	0.19	1.08	0.66	1.78	1.51	2.38	2.69	5.32	5.04	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-71 • 2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	4.27	0.19	1.04	0.66	4.35	4.06	1.71	1.62	ns
4 mA	Std.	0.97	4.27	0.19	1.04	0.66	4.35	4.06	1.71	1.62	ns
6 mA	Std.	0.97	3.54	0.19	1.04	0.66	3.60	3.47	1.95	2.07	ns
8 mA	Std.	0.97	3.54	0.19	1.04	0.66	3.60	3.47	1.95	2.07	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-72 • 2.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	2.24	0.19	1.04	0.66	2.28	2.08	1.71	1.68	ns
4 mA	Std.	0.97	2.24	0.19	1.04	0.66	2.28	2.08	1.71	1.68	ns
6 mA	Std.	0.97	1.88	0.19	1.04	0.66	1.92	1.62	1.95	2.14	ns
8 mA	Std.	0.97	1.88	0.19	1.04	0.66	1.92	1.62	1.95	2.14	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Applies to 1.2 V Core Voltage

Table 2-73 • **2.5 V LCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	1.55	5.58	0.26	1.20	1.10	5.68	5.14	2.80	2.78	11.49	10.95	ns
6 mA	Std.	1.55	4.75	0.26	1.20	1.10	4.84	4.47	3.09	3.31	10.65	10.28	ns
8 mA	Std.	1.55	4.75	0.26	1.20	1.10	4.84	4.47	3.09	3.31	10.65	10.28	ns
12 mA	Std.	1.55	4.15	0.26	1.20	1.10	4.23	3.99	3.28	3.65	10.04	9.80	ns
16 mA	Std.	1.55	3.97	0.26	1.20	1.10	4.04	3.88	3.33	3.74	9.85	9.69	ns
24 mA	Std.	1.55	3.90	0.26	1.20	1.10	3.96	3.90	3.38	4.07	9.77	9.71	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-74 • **2.5 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	1.55	3.32	0.26	1.20	1.10	3.38	3.09	2.80	2.89	9.19	8.90	ns
6 mA	Std.	1.55	2.88	0.26	1.20	1.10	2.93	2.56	3.09	3.43	8.74	8.37	ns
8 mA	Std.	1.55	2.88	0.26	1.20	1.10	2.93	2.56	3.09	3.43	8.74	8.37	ns
12 mA	Std.	1.55	2.63	0.26	1.20	1.10	2.68	2.30	3.28	3.77	8.48	8.10	ns
16 mA	Std.	1.55	2.58	0.26	1.20	1.10	2.63	2.25	3.33	3.86	8.44	8.06	ns
24 mA	Std.	1.55	2.59	0.26	1.20	1.10	2.64	2.19	3.39	4.21	8.45	8.00	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

Table 2-75 • **2.5 V LCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	1.55	5.01	0.26	1.20	1.10	5.11	4.60	2.49	2.60	10.92	10.41	ns
6 mA	Std.	1.55	4.20	0.26	1.20	1.10	4.28	4.00	2.74	3.08	10.08	9.81	ns
8 mA	Std.	1.55	4.20	0.26	1.20	1.10	4.28	4.00	2.74	3.08	10.08	9.81	ns
12 mA	Std.	1.55	3.64	0.26	1.20	1.10	3.71	3.56	2.92	3.39	9.52	9.36	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-76 • **2.5 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	1.55	2.90	0.26	1.20	1.10	2.95	2.66	2.48	2.70	8.76	8.47	ns
6 mA	Std.	1.55	2.50	0.26	1.20	1.10	2.54	2.18	2.74	3.19	8.35	7.99	ns
8 mA	Std.	1.55	2.50	0.26	1.20	1.10	2.54	2.18	2.74	3.19	8.35	7.99	ns
12 mA	Std.	1.55	2.28	0.26	1.20	1.10	2.32	1.95	2.92	3.50	8.13	7.75	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

Table 2-77 • **2.5 V LCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	4.84	0.26	1.15	1.10	4.93	4.56	2.12	2.22	ns
4 mA	Std.	1.55	4.84	0.26	1.15	1.10	4.93	4.56	2.12	2.22	ns
6 mA	Std.	1.55	4.08	0.26	1.15	1.10	4.16	3.96	2.37	2.69	ns
8 mA	Std.	1.55	4.08	0.26	1.15	1.10	4.16	3.96	2.37	2.69	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-78 • **2.5 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	2.75	0.26	1.15	1.10	2.80	2.53	2.12	2.31	ns
4 mA	Std.	1.55	2.75	0.26	1.15	1.10	2.80	2.53	2.12	2.31	ns
6 mA	Std.	1.55	2.38	0.26	1.15	1.10	2.42	2.05	2.37	2.79	ns
8 mA	Std.	1.55	2.38	0.26	1.15	1.10	2.42	2.05	2.37	2.79	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-79 • **Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks**

1.8 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	2	2	9	11	10	10
4 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	4	4	17	22	10	10
6 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	6	6	35	44	10	10
8 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	8	8	45	51	10	10
12 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	12	12	91	74	10	10
16 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	16	16	91	74	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-80 • **Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks**

1.8 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	2	2	9	11	10	10
4 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	4	4	17	22	10	10
6 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	6	6	35	44	10	10
8 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	8	8	35	44	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-81 • **Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks**

1.8 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	2	2	9	11	10	10
4 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.9	0.45	V_{CCI} – 0.45	4	4	17	22	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

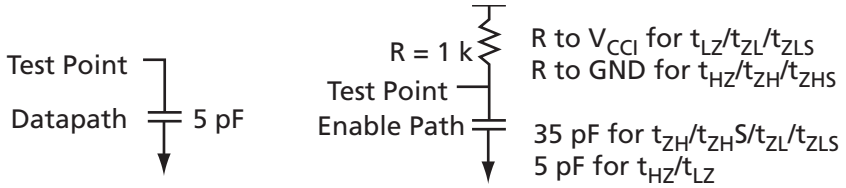


Figure 2-9 • **AC Loading**

Table 2-82 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.8	0.9	5

* *Measuring point = V_{trip}. See Table 2-28 on page 2-25 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-83 • **1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	6.38	0.19	1.01	0.66	6.49	5.92	2.33	1.56	10.03	9.45	ns
4 mA	Std.	0.97	5.35	0.19	1.01	0.66	5.45	5.04	2.67	2.38	8.98	8.57	ns
6 mA	Std.	0.97	4.62	0.19	1.01	0.66	4.70	4.43	2.90	2.78	8.23	7.96	ns
8 mA	Std.	0.97	4.37	0.19	1.01	0.66	4.45	4.30	2.95	2.89	7.98	7.83	ns
12 mA	Std.	0.97	4.31	0.19	1.01	0.66	4.37	4.31	3.03	3.29	7.90	7.84	ns
16 mA	Std.	0.97	4.31	0.19	1.01	0.66	4.37	4.31	3.03	3.29	7.90	7.84	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-84 • **1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	3.24	0.19	1.01	0.66	3.20	3.24	2.33	1.61	6.73	6.78	ns
4 mA	Std.	0.97	2.62	0.19	1.01	0.66	2.67	2.50	2.66	2.46	6.20	6.04	ns
6 mA	Std.	0.97	2.31	0.19	1.01	0.66	2.35	2.14	2.89	2.87	5.88	5.67	ns
8 mA	Std.	0.97	2.25	0.19	1.01	0.66	2.29	2.07	2.95	2.98	5.82	5.60	ns
12 mA	Std.	0.97	2.24	0.19	1.01	0.66	2.28	1.99	3.02	3.39	5.81	5.52	ns
16 mA	Std.	0.97	2.24	0.19	1.01	0.66	2.28	1.99	3.02	3.39	5.81	5.52	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-85 • **1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	5.78	0.19	1.01	0.66	5.89	5.31	1.95	1.46	9.42	8.84	ns
4 mA	Std.	0.97	4.75	0.19	1.01	0.66	4.84	4.53	2.25	2.21	8.37	8.06	ns
6 mA	Std.	0.97	4.07	0.19	1.01	0.66	4.14	3.97	2.46	2.57	7.67	7.50	ns
8 mA	Std.	0.97	4.07	0.19	1.01	0.66	4.14	3.97	2.46	2.57	7.67	7.50	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-86 • 1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.75	0.19	1.01	0.66	2.79	2.75	1.94	1.51	6.32	6.28	ns
4 mA	Std.	0.97	2.25	0.19	1.01	0.66	2.29	2.09	2.24	2.29	5.82	5.62	ns
6 mA	Std.	0.97	1.97	0.19	1.01	0.66	2.01	1.76	2.46	2.66	5.54	5.29	ns
8 mA	Std.	0.97	1.97	0.19	1.01	0.66	2.01	1.76	2.46	2.66	5.54	5.29	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-87 • 1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	5.63	0.19	0.98	0.66	5.73	5.29	1.68	1.24	ns
4 mA	Std.	0.97	4.69	0.19	0.98	0.66	4.78	4.51	1.97	1.98	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-88 • 1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	2.62	0.19	0.98	0.66	2.67	2.59	1.67	1.29	ns
4 mA	Std.	0.97	2.18	0.19	0.98	0.66	2.22	1.93	1.96	2.06	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

1.2 V DC Core Voltage

Table 2-89 • **1.8 V LCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	6.96	0.26	1.11	1.10	7.09	6.49	2.85	2.27	12.89	12.29	ns
4 mA	Std.	1.55	5.90	0.26	1.11	1.10	6.01	5.57	3.20	3.12	11.82	11.38	ns
6 mA	Std.	1.55	5.15	0.26	1.11	1.10	5.24	4.95	3.44	3.54	11.05	10.76	ns
8 mA	Std.	1.55	4.89	0.26	1.11	1.10	4.98	4.81	3.49	3.65	10.79	10.62	ns
12 mA	Std.	1.55	4.83	0.26	1.11	1.10	4.90	4.83	3.57	4.06	10.71	10.64	ns
16 mA	Std.	1.55	4.83	0.26	1.11	1.10	4.90	4.83	3.57	4.06	10.71	10.64	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-90 • **1.8 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.73	0.26	1.11	1.10	3.71	3.73	2.85	2.32	9.52	9.54	ns
4 mA	Std.	1.55	3.11	0.26	1.11	1.10	3.16	2.97	3.19	3.21	8.97	8.78	ns
6 mA	Std.	1.55	2.78	0.26	1.11	1.10	2.84	2.60	3.43	3.63	8.64	8.40	ns
8 mA	Std.	1.55	2.72	0.26	1.11	1.10	2.77	2.52	3.49	3.74	8.58	8.33	ns
12 mA	Std.	1.55	2.71	0.26	1.11	1.10	2.76	2.44	3.56	4.17	8.57	8.24	ns
16 mA	Std.	1.55	2.71	0.26	1.11	1.10	2.76	2.44	3.56	4.17	8.57	8.24	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

Table 2-91 • **1.8 V LCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	6.31	0.26	1.11	1.10	6.43	5.81	2.46	2.14	12.24	11.62	ns
4 mA	Std.	1.55	5.26	0.26	1.11	1.10	5.35	5.01	2.77	2.91	11.16	10.82	ns
6 mA	Std.	1.55	4.55	0.26	1.11	1.10	4.64	4.44	2.98	3.29	10.45	10.25	ns
8 mA	Std.	1.55	4.55	0.26	1.11	1.10	4.64	4.44	2.98	3.29	10.45	10.25	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-92 • **1.8 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.21	0.26	1.11	1.10	3.26	3.18	2.45	2.18	9.07	8.99	ns
4 mA	Std.	1.55	2.71	0.26	1.11	1.10	2.76	2.50	2.76	2.99	8.56	8.31	ns
6 mA	Std.	1.55	2.42	0.26	1.11	1.10	2.47	2.16	2.98	3.38	8.28	7.97	ns
8 mA	Std.	1.55	2.42	0.26	1.11	1.10	2.47	2.16	2.98	3.38	8.28	7.97	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

Table 2-93 • **1.8 V LCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	6.13	0.26	1.08	1.10	6.24	5.79	2.07	1.77	ns
4 mA	Std.	1.55	5.16	0.26	1.08	1.10	5.26	4.99	2.37	2.53	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-94 • **1.8 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	3.05	0.26	1.08	1.10	3.11	3.01	2.07	1.81	ns
4 mA	Std.	1.55	2.60	0.26	1.08	1.10	2.64	2.33	2.37	2.61	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 2-95 • **Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks**

1.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2	13	16	10	10
4 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	4	4	25	33	10	10
6 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	6	6	32	39	10	10
8 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	8	8	66	55	10	10
12 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	12	12	66	55	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-96 • **Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks**

1.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2	13	16	10	10
4 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	4	4	25	33	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-97 • **Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks**

1.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.575	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2	13	16	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

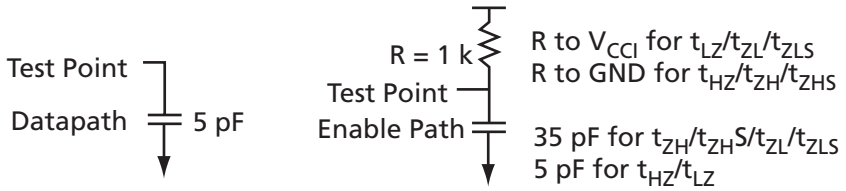


***Figure 2-10* • AC Loading**

***Table 2-98* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.5	0.75	5

* *Measuring point = V_{trip}. See Table 2-28 on page 2-25 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

***Table 2-99* • 1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	6.62	0.19	1.17	0.66	6.74	6.05	2.79	2.31	10.28	9.58	ns
4 mA	Std.	0.97	5.74	0.19	1.17	0.66	5.85	5.33	3.06	2.78	9.38	8.86	ns
6 mA	Std.	0.97	5.43	0.19	1.17	0.66	5.53	5.18	3.12	2.90	9.06	8.71	ns
8 mA	Std.	0.97	5.35	0.19	1.17	0.66	5.45	5.19	3.21	3.36	8.98	8.72	ns
12 mA	Std.	0.97	5.35	0.19	1.17	0.66	5.45	5.19	3.21	3.36	8.98	8.72	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

***Table 2-100* • 1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.97	0.19	1.17	0.66	3.03	2.89	2.78	2.40	6.56	6.43	ns
4 mA	Std.	0.97	2.60	0.19	1.17	0.66	2.64	2.44	3.05	2.88	6.18	5.97	ns
6 mA	Std.	0.97	3.63	0.19	1.17	0.66	3.62	3.63	3.06	3.00	7.15	7.16	ns
8 mA	Std.	0.97	2.50	0.19	1.17	0.66	2.55	2.26	3.20	3.48	6.08	5.79	ns
12 mA	Std.	0.97	2.50	0.19	1.17	0.66	2.55	2.26	3.20	3.48	6.08	5.79	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-101 **• 1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	5.93	0.19	1.17	0.66	6.04	5.46	2.30	2.15	9.57	8.99	ns
4 mA	Std.	0.97	5.11	0.19	1.17	0.66	5.20	4.79	2.54	2.58	8.73	8.32	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-102 **• 1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.58	0.19	1.17	0.66	2.63	2.40	2.29	2.24	6.16	5.94	ns
4 mA	Std.	0.97	2.25	0.19	1.17	0.66	2.29	1.99	2.53	2.68	5.82	5.52	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-103 **• 1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	5.88	0.19	1.13	0.66	5.99	5.45	1.99	1.93	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-104 **• 1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	2.51	0.19	1.13	0.66	2.56	2.20	1.99	2.03	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

1.2 V DC Core Voltage

***Table 2-105* • 1.5 V LCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	7.16	0.26	1.27	1.10	7.29	6.60	3.32	3.01	13.10	12.41	ns
4 mA	Std.	1.55	6.26	0.26	1.27	1.10	6.37	5.86	3.59	3.49	12.18	11.67	ns
6 mA	Std.	1.55	5.93	0.26	1.27	1.10	6.04	5.70	3.65	3.62	11.85	11.51	ns
8 mA	Std.	1.55	5.85	0.26	1.27	1.10	5.96	5.72	3.75	4.10	11.77	11.52	ns
12 mA	Std.	1.55	5.85	0.26	1.27	1.10	5.96	5.72	3.75	4.10	11.77	11.52	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

***Table 2-106* • 1.5 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.43	0.26	1.27	1.10	3.49	3.36	3.31	3.10	9.30	9.16	ns
4 mA	Std.	1.55	3.04	0.26	1.27	1.10	3.10	2.89	3.58	3.59	8.91	8.70	ns
6 mA	Std.	1.55	4.11	0.26	1.27	1.10	4.10	4.11	3.59	3.72	9.91	9.92	ns
8 mA	Std.	1.55	2.95	0.26	1.27	1.10	3.00	2.70	3.74	4.21	8.81	8.51	ns
12 mA	Std.	1.55	2.95	0.26	1.27	1.10	3.00	2.70	3.74	4.21	8.81	8.51	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

***Table 2-107* • 1.5 V LCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	6.42	0.26	1.27	1.10	6.54	5.95	2.81	2.81	12.35	11.76	ns
4 mA	Std.	1.55	5.58	0.26	1.27	1.10	5.68	5.27	3.06	3.25	11.49	11.08	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

***Table 2-108* • 1.5 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.01	0.26	1.27	1.10	3.07	2.81	2.80	2.90	8.88	8.62	ns
4 mA	Std.	1.55	2.67	0.26	1.27	1.10	2.72	2.39	3.05	3.36	8.53	8.20	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

***Table 2-109* • 1.5 V LCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	6.35	0.26	1.22	1.10	6.46	5.93	2.39	2.45	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

***Table 2-110* • 1.5 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	2.91	0.26	1.22	1.10	2.96	2.60	2.39	2.54	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

1.2 V LVCMOS (JESD8-12A)

Low-Voltage CMOS for 1.2 V complies with the LVCMOS standard JESD8-12A for general purpose 1.2 V applications. It uses a 1.2 V input buffer and a push-pull output buffer.

***Table 2-111* • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks**

1.2 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}[1]	I_{OSL}[1]	I_{IL}[2]	I_{IH}[2]
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA	Max., mA	µA	µA
2 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.26	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2	TBD	TBD	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

***Table 2-112* • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks**

1.2 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}[1]	I_{OSL}[1]	I_{IL}[2]	I_{IH}[2]
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA	Max., mA	µA	µA
2 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.26	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2	TBD	TBD	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

***Table 2-113* • Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks**

1.2 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}[1]	I_{OSL}[1]	I_{IL}[2]	I_{IH}[2]
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA	Max., mA	µA	µA
1 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	1.26	0.25 * V_{CCI}	0.75 * V_{CCI}	1	1	TBD	TBD	10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

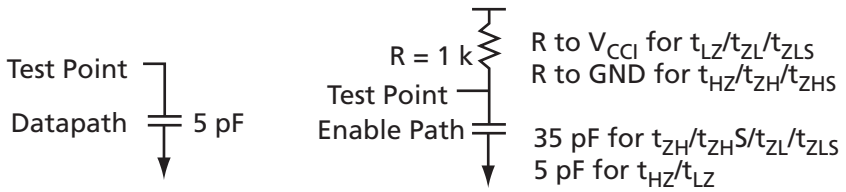


***Figure 2-11* • AC Loading**

***Table 2-114* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.2	0.6	5

* *Measuring point = V_{trip}. See Table 2-28 on page 2-25 for a complete table of trip points.*

Timing Characteristics

1.2 V DC Core Voltage

***Table 2-115* • 1.2 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	6.62	0.19	1.17	0.66	6.74	6.05	2.79	2.31	10.28	9.58	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

***Table 2-116* • 1.2 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.14 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.61	0.26	1.58	1.10	3.45	3.33	3.94	3.66	9.05	8.93	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-117* • 1.2 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.14 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	7.60	0.26	1.58	1.10	7.27	6.52	3.31	3.36	12.86	12.12	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

***Table 2-118* • 1.2 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.14 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.23	0.26	1.58	1.10	3.09	2.76	3.30	3.49	8.69	8.36	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-119* • 1.2 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.14 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
1 mA	Std.	1.55	8.58	0.26	1.52	1.10	8.21	7.36	2.52	2.40	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

***Table 2-120* • 1.2 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.14 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
1 mA	Std.	1.55	3.60	0.26	1.52	1.10	3.45	3.04	2.52	2.50	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

***Table 2-121* • Minimum and Maximum DC Input and Output Levels Applicable to Advanced and Standard Plus I/Os**

3.3 V PCI/PCI-X	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSH}	I_{OSL}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
Per PCI specification	Per PCI curves										10	10

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Actel loadings for enable path characterization are described in Figure 2-12.

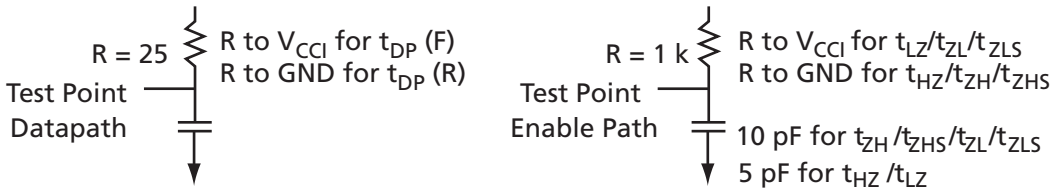


***Figure 2-12* • AC Loading**

AC loadings are defined per PCI/PCI-X specifications for the datapath; Actel loading for tristate is described in Table 2-122.

***Table 2-122* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	3.3	0.285 * V_{CCI} for $t_{DP(R)}$ 0.615 * V_{CCI} for $t_{DP(F)}$	10

* *Measuring point = V_{trip}. See Table 2-28 on page 2-25 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

***Table 2-123* • 3.3 V PCI/PCI-X**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Advanced I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.97	2.32	0.19	0.70	0.66	2.36	1.77	2.67	3.04	5.89	5.30	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

***Table 2-124* • 3.3 V PCI/PCI-X**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Plus I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.97	1.96	0.19	0.70	0.66	2.00	1.50	2.36	2.79	5.53	5.03	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

***Table 2-125* • 3.3 V PCI/PCI-X**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Advanced I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	2.90	0.25	0.86	1.10	2.95	2.29	3.23	3.92	8.76	8.10	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

***Table 2-126* • 3.3 V PCI/PCI-X**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Plus I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.55	2.52	0.25	0.85	1.10	2.57	1.98	2.91	3.62	8.37	7.78	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by Actel Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-13. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, IGLOO also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

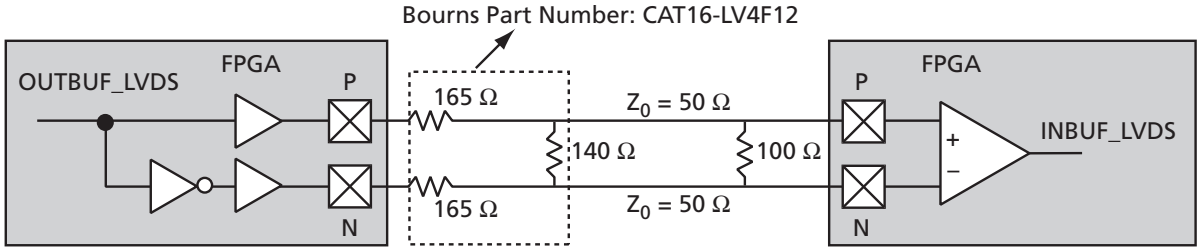


Figure 2-13 • **LVDS Circuit Diagram and Board-Level Implementation**

Table 2-127 • **Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Typ.	Max.	Units
V_{CCI}	Supply Voltage	2.375	2.5	2.625	V
V_{OL}	Output LOW Voltage	0.9	1.075	1.25	V
V_{OH}	Output HIGH Voltage	1.25	1.425	1.6	V
I_{OL} [4]	Output Lower Current	0.65	0.91	1.16	mA
I_{OH} [4]	Output HIGH Current	0.65	0.91	1.16	mA
V_I	Input Voltage	0		2.925	V
I_{IH} [3]	Input HIGH Leakage Current			10	µA
I_{IL} [3]	Input LOW Leakage Current			10	µA
V_{ODIFF}	Differential Output Voltage	250	350	450	mV
V_{OCM}	Output Common-Mode Voltage	1.125	1.25	1.375	V
V_{ICM}	Input Common-Mode Voltage	0.05	1.25	2.35	V
V_{IDIFF}	Input Differential Voltage	100	350		mV

Notes:

1. *± 5%*
2. *Differential input voltage = ±350 mV.*
3. *Currents are measured at 85°C junction temperature.*
4. *I_{OL}/I_{OH} is defined by V_{ODIFF}/(resistor network).*

Table 2-128 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)
1.075	1.325	Cross point

* *Measuring point = V_{trip}. See Table 2-28 on page 2-25 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-129 • **LVDS – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Standard Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.97	1.67	0.19	1.31	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 and Table 2-7 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-130 • **LVDS – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Standard Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	1.55	2.19	0.25	1.52	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 and Table 2-7 on page 2-7 for derating values.

BLVDS/M-LVDS

Bus LVDS (BLVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Actel LVDS drivers provide the higher drive current required by BLVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Actel LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-14. The input and output buffer delays are available in the LVDS section in Table 2-129 on page 2-65 and Table 2-130 on page 2-65.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: R_S = 60 Ω and R_T = 70 Ω, given Z_0 = 50 Ω (2") and Z_{stub} = 50 Ω (~1.5").

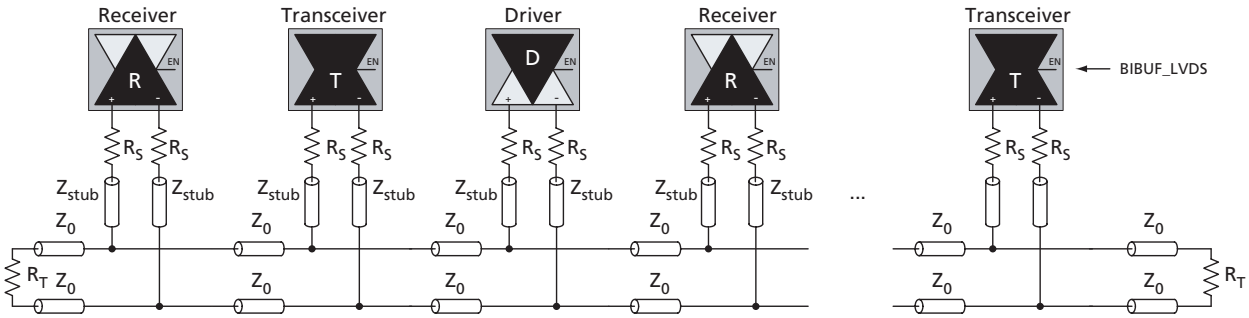


Figure 2-14 • **BLVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers**

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-15. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

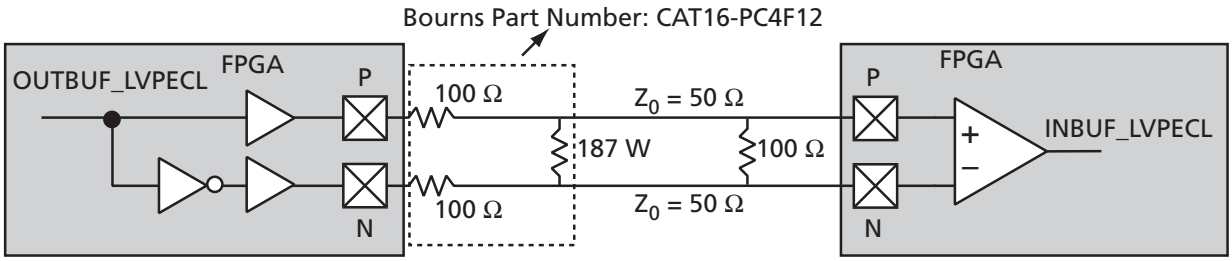


Figure 2-15 • **LVPECL Circuit Diagram and Board-Level Implementation**

Table 2-131 • **Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
V_{CCI}	Supply Voltage	3.0		3.3		3.6		V
V_{OL}	Output LOW Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{OH}	Output HIGH Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{IL}, V_{IH}	Input LOW, Input HIGH Voltages	0	3.3	0	3.6	0	3.9	V
V_{ODIFF}	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
V_{OCM}	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
V_{ICM}	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
V_{IDIFF}	Input Differential Voltage	300		300		300		mV

Table 2-132 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)
1.64	1.94	Cross point

* *Measuring point = V_{trip}. See Table 2-28 on page 2-87 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 2-133 • **LVPECL – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.97	1.67	0.19	1.16	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-134 • **LVPECL – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	1.55	2.24	0.25	1.37	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

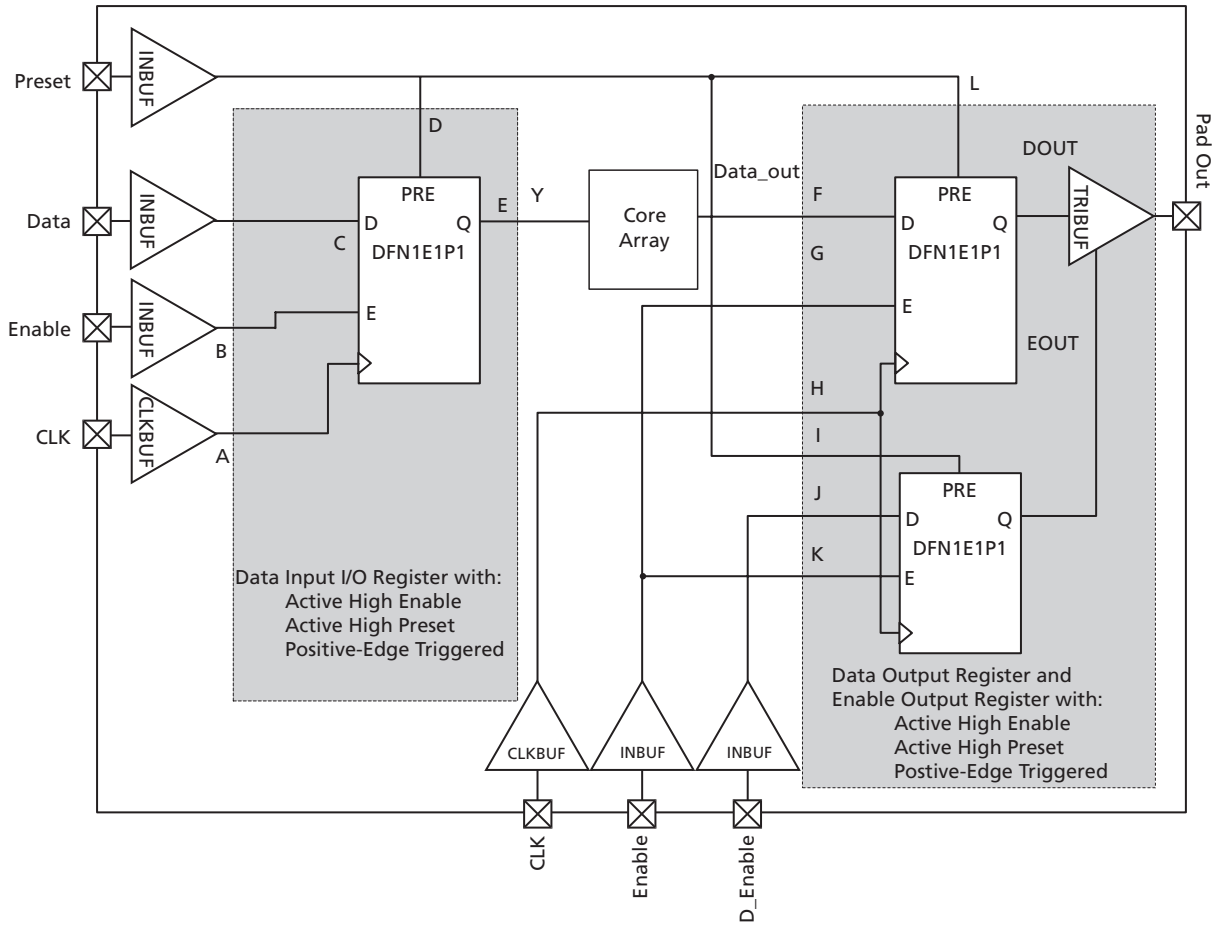


Figure 2-16 • **Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

Table 2-135 • **Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

* *See Figure 2-16 on page 2-68 for more information.*

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

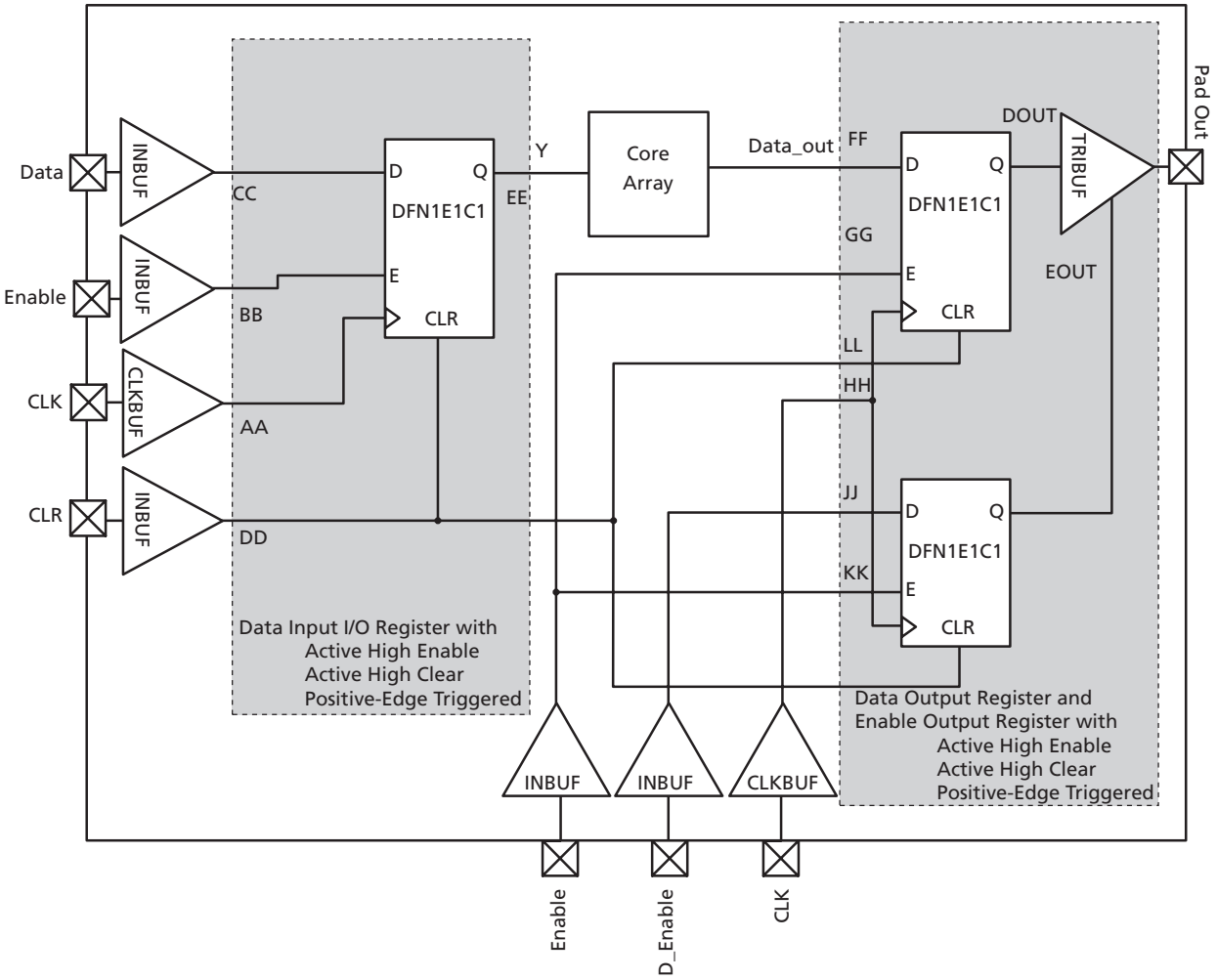


Figure 2-17 • **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

Table 2-136 • **Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

* *See Figure 2-17 on page 2-70 for more information.*

Input Register

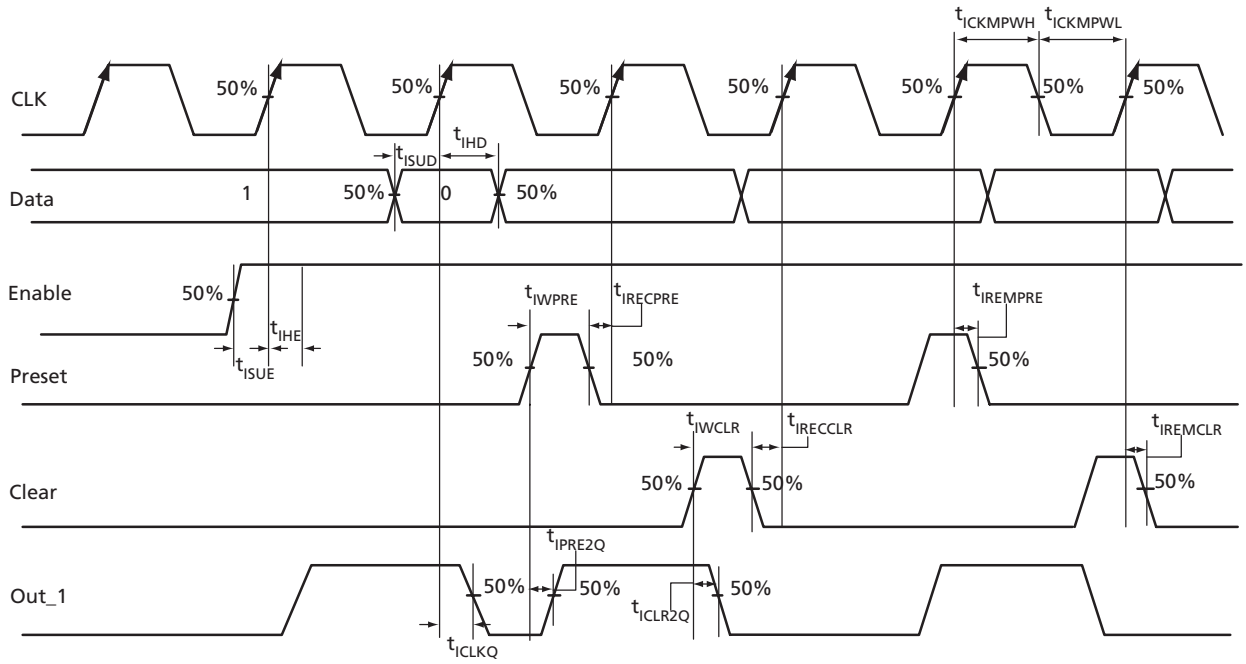


Figure 2-18 • **Input Register Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-137 • **Input Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.42	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.47	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.67	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.79	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.79	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width HIGH for the Input Data Register	0.31	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width LOW for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

Table 2-138 • Input Data Register Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.68	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.97	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	1.02	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	1.19	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	1.19	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width HIGH for the Input Data Register	0.31	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width LOW for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Output Register

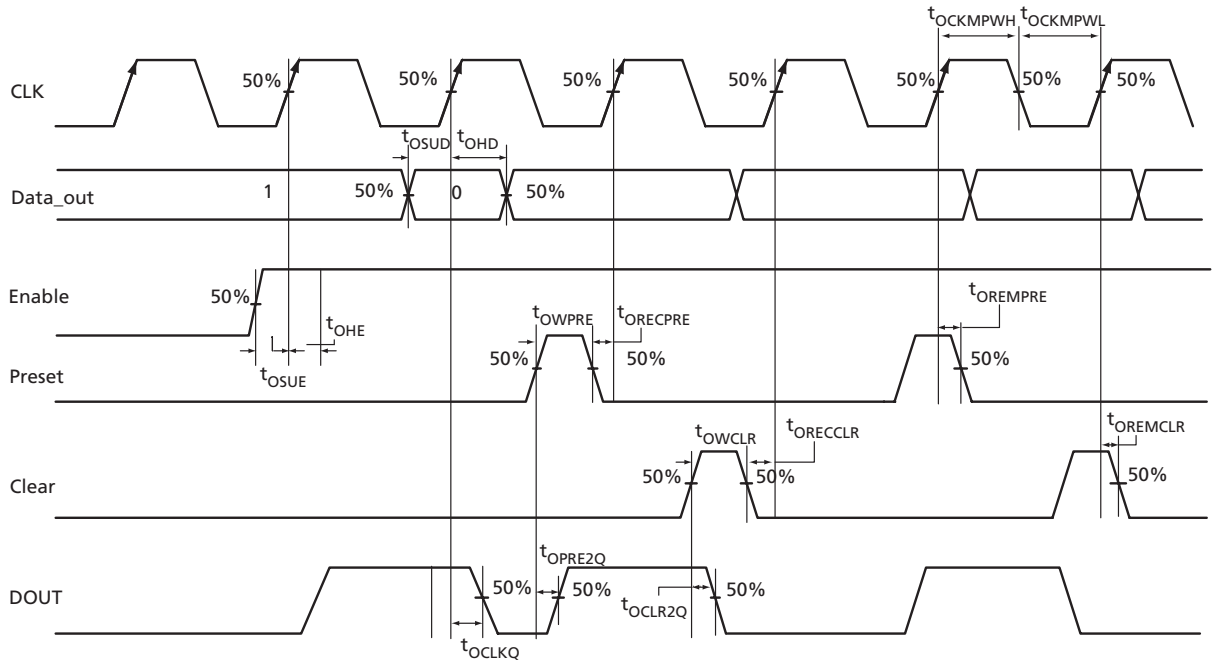


Figure 2-19 • Output Register Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

***Table 2-139* • Output Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	1.00	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.51	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.70	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	1.34	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	1.34	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Data Register	0.31	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width LOW for the Output Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

***Table 2-140* • Output Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	1.52	ns
t_{OSUD}	Data Setup Time for the Output Data Register	1.15	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	1.11	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	1.96	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	1.96	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Data Register	0.31	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width LOW for the Output Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Output Enable Register

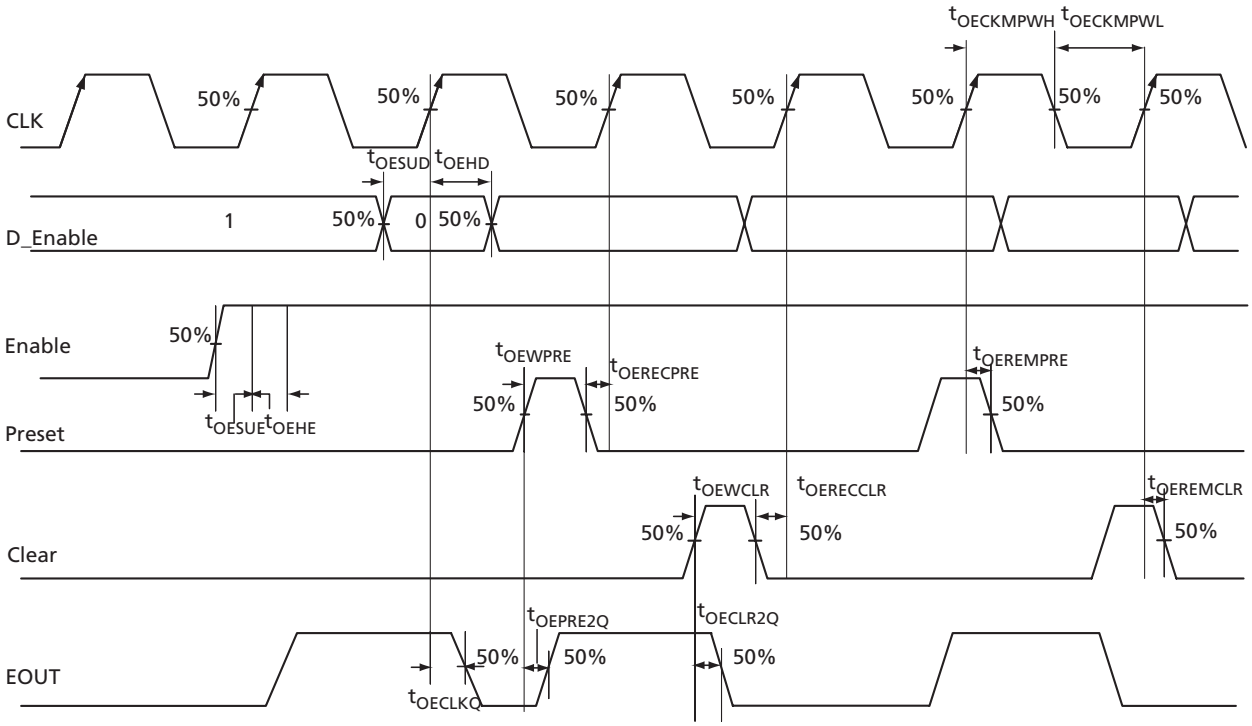


Figure 2-20 • **Output Enable Register Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-141 • **Output Enable Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.75	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.51	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.73	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	1.13	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	1.13	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.31	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

***Table 2-142* • Output Enable Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	1.10	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	1.15	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	1.22	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	1.65	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	1.65	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.31	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

DDR Module Specifications

Input DDR Module

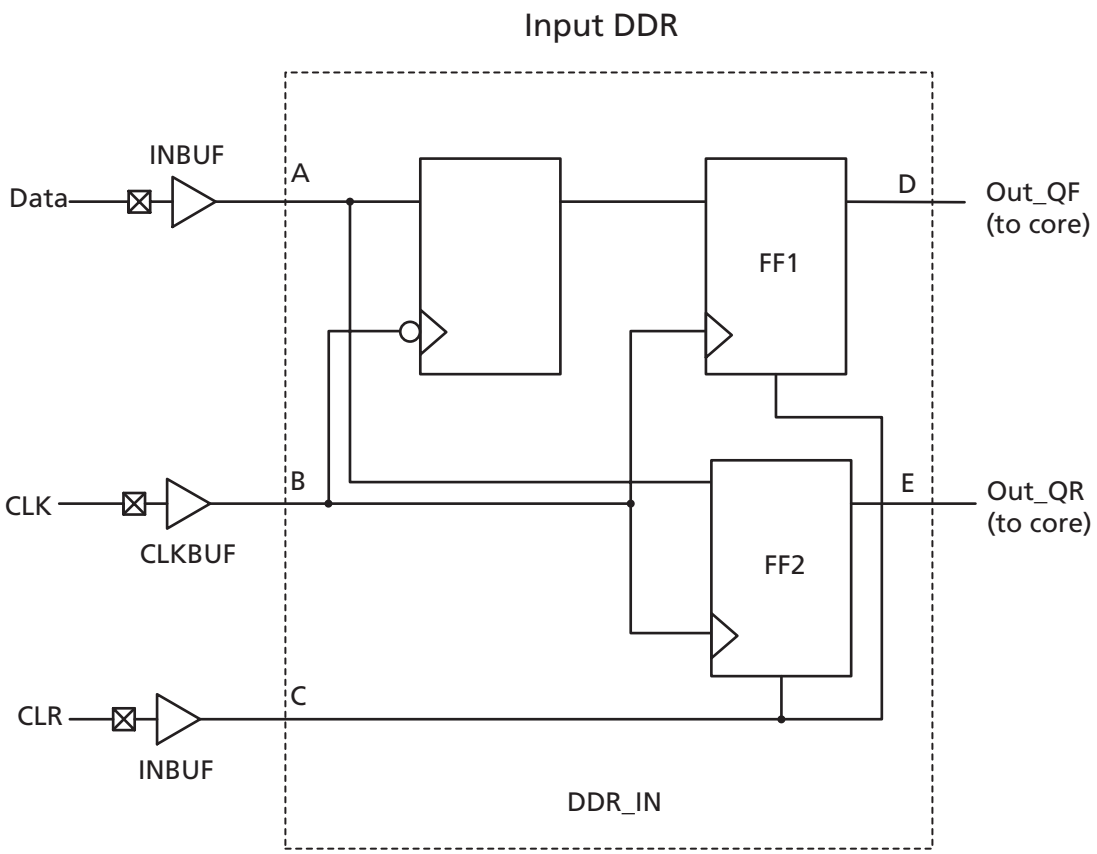


Figure 2-21 **• Input DDR Timing Model**

Table 2-143 **• Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

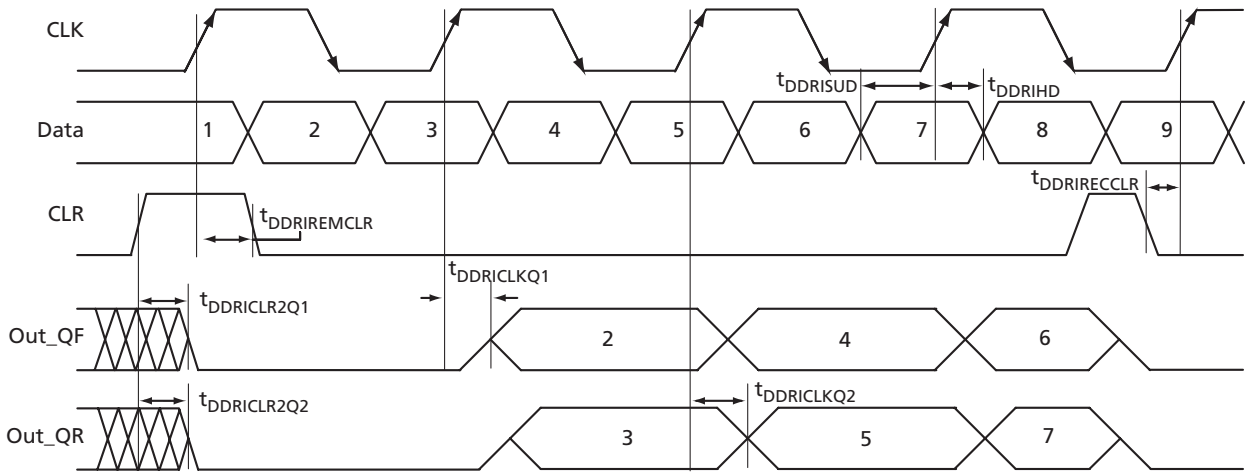


Figure 2-22 **• Input DDR Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-144 **• Input DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.25 V

Parameter	Description	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.48	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.65	ns
$t_{DDRISUD1}$	Data Setup for Input DDR (negedge)	0.50	ns
$t_{DDRISUD2}$	Data Setup for Input DDR (posedge)	0.40	ns
$t_{DDRIHD1}$	Data Hold for Input DDR (negedge)	0.00	ns
$t_{DDRIHD2}$	Data Hold for Input DDR (posedge)	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.82	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.98	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.23	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width HIGH for Input DDR	0.31	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width LOW for Input DDR	0.28	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	TBD	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-145 • Input DDR Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.76	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.94	ns
$t_{DDRISUD1}$	Data Setup for Input DDR (negedge)	0.93	ns
$t_{DDRISUD2}$	Data Setup for Input DDR (posedge)	0.84	ns
$t_{DDRIHD1}$	Data Hold for Input DDR (negedge)	0.00	ns
$t_{DDRIHD2}$	Data Hold for Input DDR (posedge)	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	1.23	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	1.42	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.24	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width HIGH for Input DDR	0.31	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width LOW for Input DDR	0.28	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	TBD	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Output DDR Module

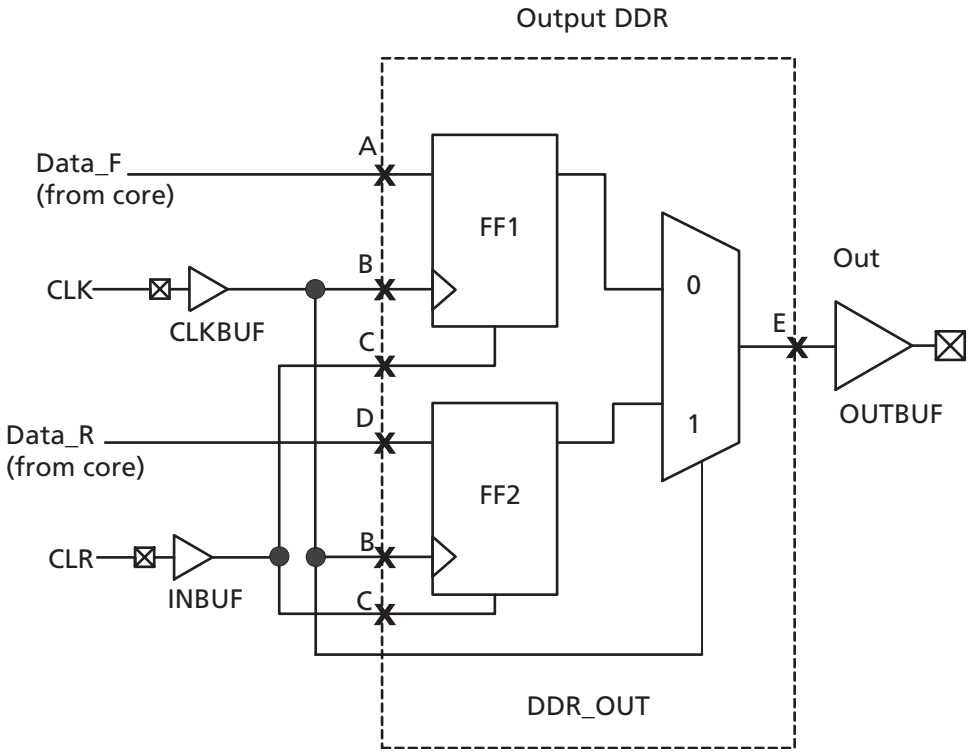


Figure 2-23 • **Output DDR Timing Model**

Table 2-146 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

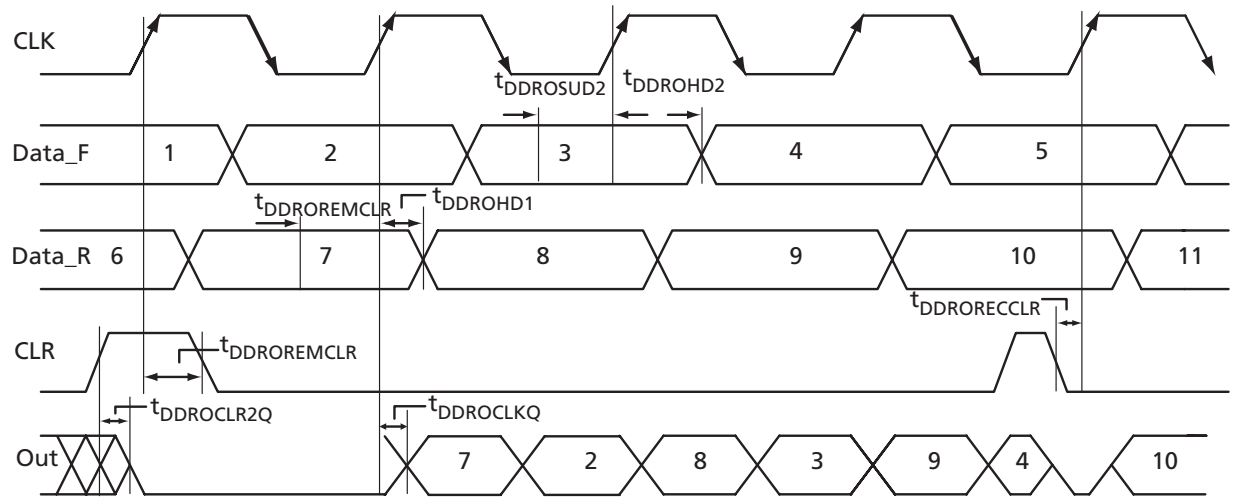


Figure 2-24 **• Output DDR Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-147 **• Output DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	1.07	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.67	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.67	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	1.38	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.23	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.31	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width LOW for the Output DDR	0.28	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	TBD	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

***Table 2-148* • Output DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	1.60	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	1.09	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	1.16	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	1.99	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.24	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.31	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width LOW for the Output DDR	0.28	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	TBD	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The IGLOO library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

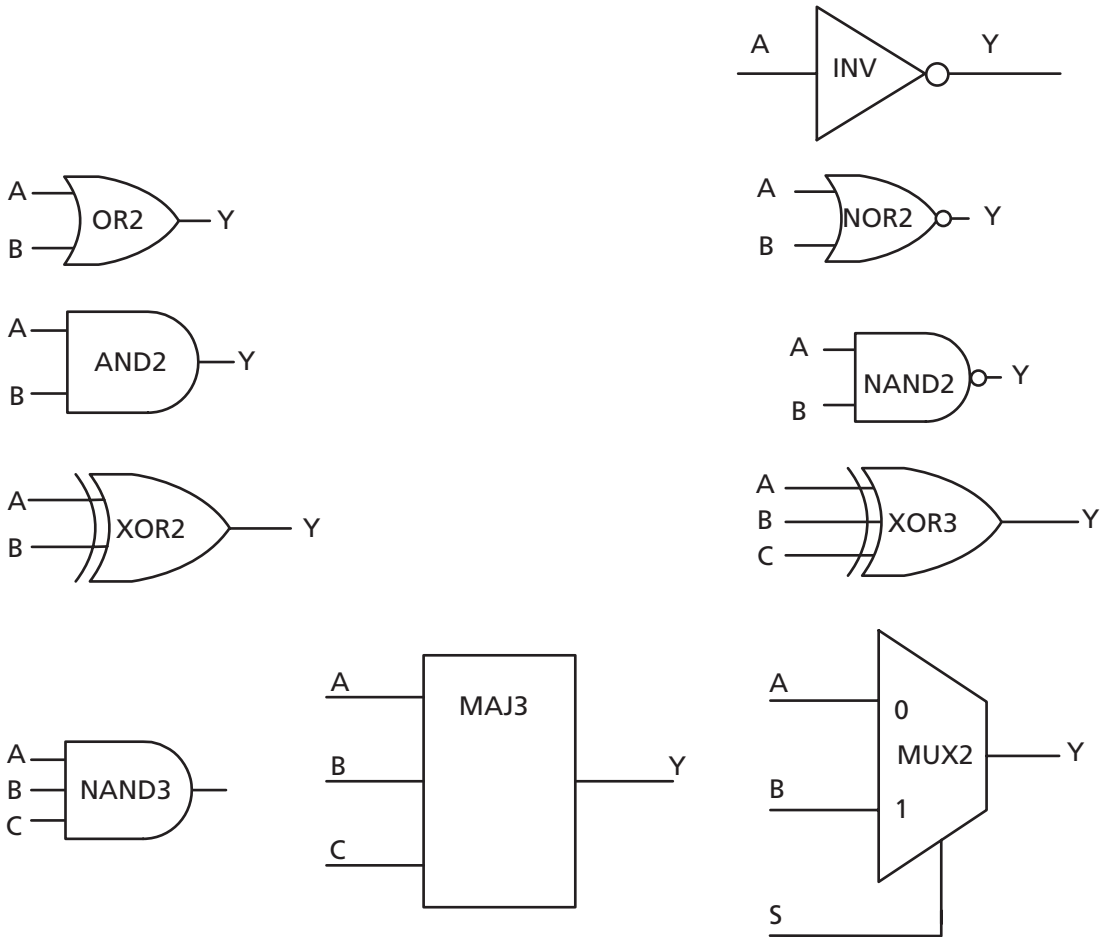


Figure 2-25 • **Sample of Combinatorial Cells**

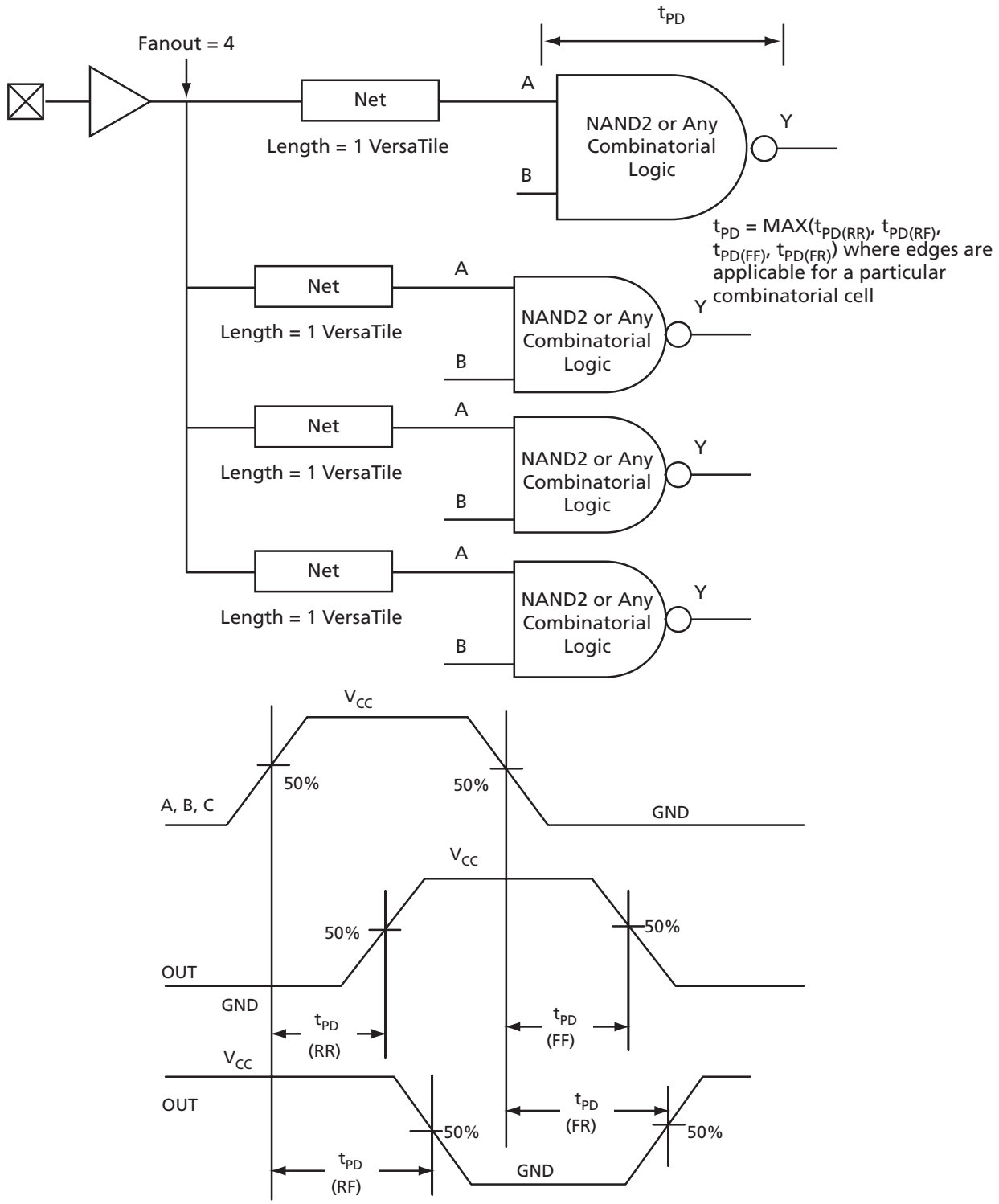


Figure 2-26 • **Timing Model and Waveforms**

Timing Characteristics

1.5 V DC Core Voltage

***Table 2-149* • Combinatorial Cell Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	Y =!A	t_{PD}	0.80	ns
AND2	Y = A · B	t_{PD}	0.84	ns
NAND2	Y = !(A · B)	t_{PD}	0.90	ns
OR2	Y = A + B	t_{PD}	1.19	ns
NOR2	Y = !(A + B)	t_{PD}	1.10	ns
XOR2	Y = A ⊕ B	t_{PD}	1.37	ns
MAJ3	Y = MAJ(A , B, C)	t_{PD}	1.33	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	1.79	ns
MUX2	Y = A !S + B S	t_{PD}	1.48	ns
AND3	Y = A · B · C	t_{PD}	1.21	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

***Table 2-150* • Combinatorial Cell Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	Y = !A	t_{PD}	1.34	ns
AND2	Y = A · B	t_{PD}	1.43	ns
NAND2	Y = !(A · B)	t_{PD}	1.59	ns
OR2	Y = A + B	t_{PD}	2.30	ns
NOR2	Y = !(A + B)	t_{PD}	2.07	ns
XOR2	Y = A ⊕ B	t_{PD}	2.46	ns
MAJ3	Y = MAJ(A , B, C)	t_{PD}	2.46	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	3.12	ns
MUX2	Y = A !S + B S	t_{PD}	2.83	ns
AND3	Y = A · B · C	t_{PD}	2.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

VersaTile Specifications as a Sequential Module

The IGLOO library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

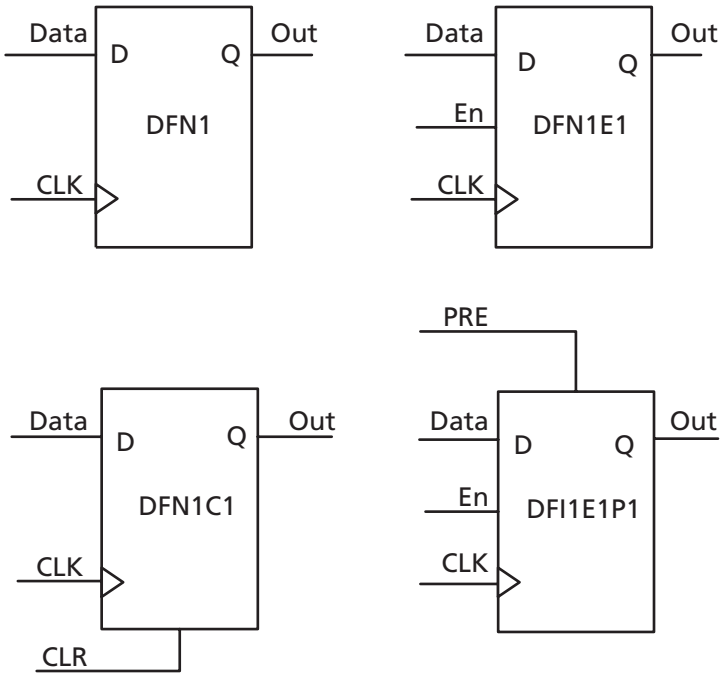


Figure 2-27 **• Sample of Sequential Cells**

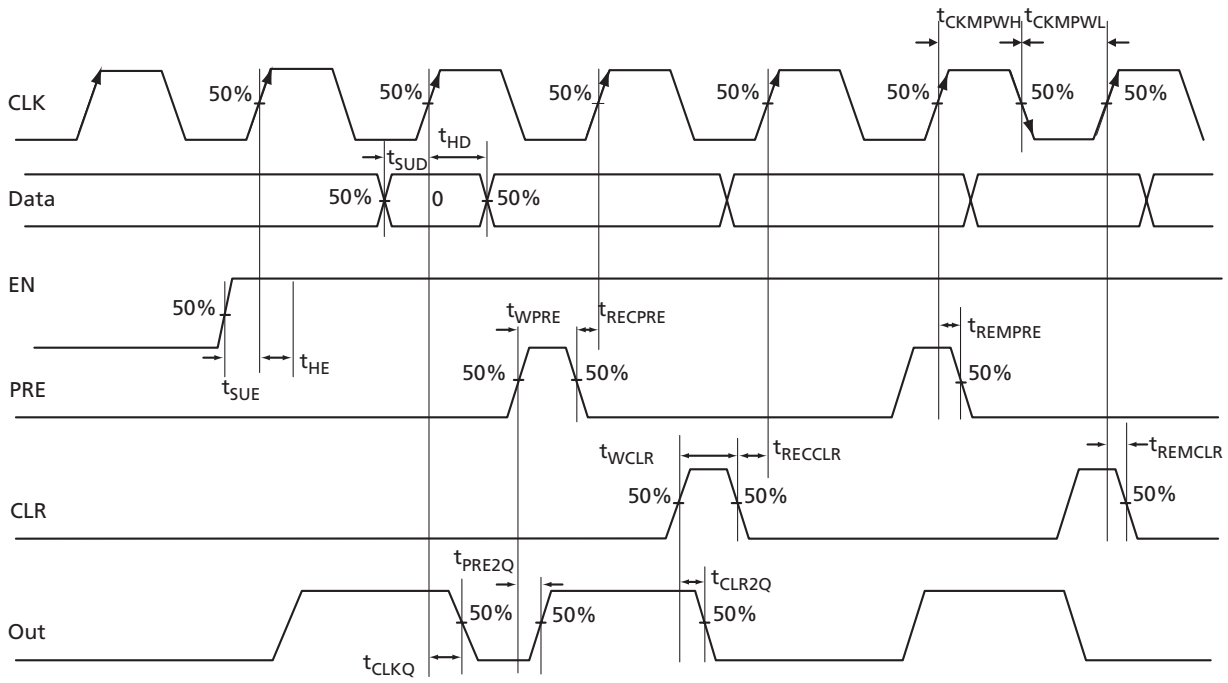


Figure 2-28 • **Timing Model and Waveforms**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-151 • **Register Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.89	ns
t_{SUD}	Data Setup Time for the Core Register	0.81	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.73	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.60	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.62	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.23	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width HIGH for the Core Register	0.56	ns
t_{CKMPWL}	Clock Minimum Pulse Width LOW for the Core Register	0.56	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

***Table 2-152* • Register Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	1.61	ns
t_{SUD}	Data Setup Time for the Core Register	1.17	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	1.29	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.87	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.89	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.24	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.46	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.46	ns
t_{CKMPWH}	Clock Minimum Pulse Width HIGH for the Core Register	0.95	ns
t_{CKMPWL}	Clock Minimum Pulse Width LOW for the Core Register	0.95	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Global Resource Characteristics

AGL250 Clock Tree Topology

Clock delays are device-specific. Figure 2-29 is an example of a global tree used for clock routing. The global tree presented in Figure 2-29 is driven by a CCC located on the west side of the AGL250 device. It is used to drive all D-flip-flops in the device.

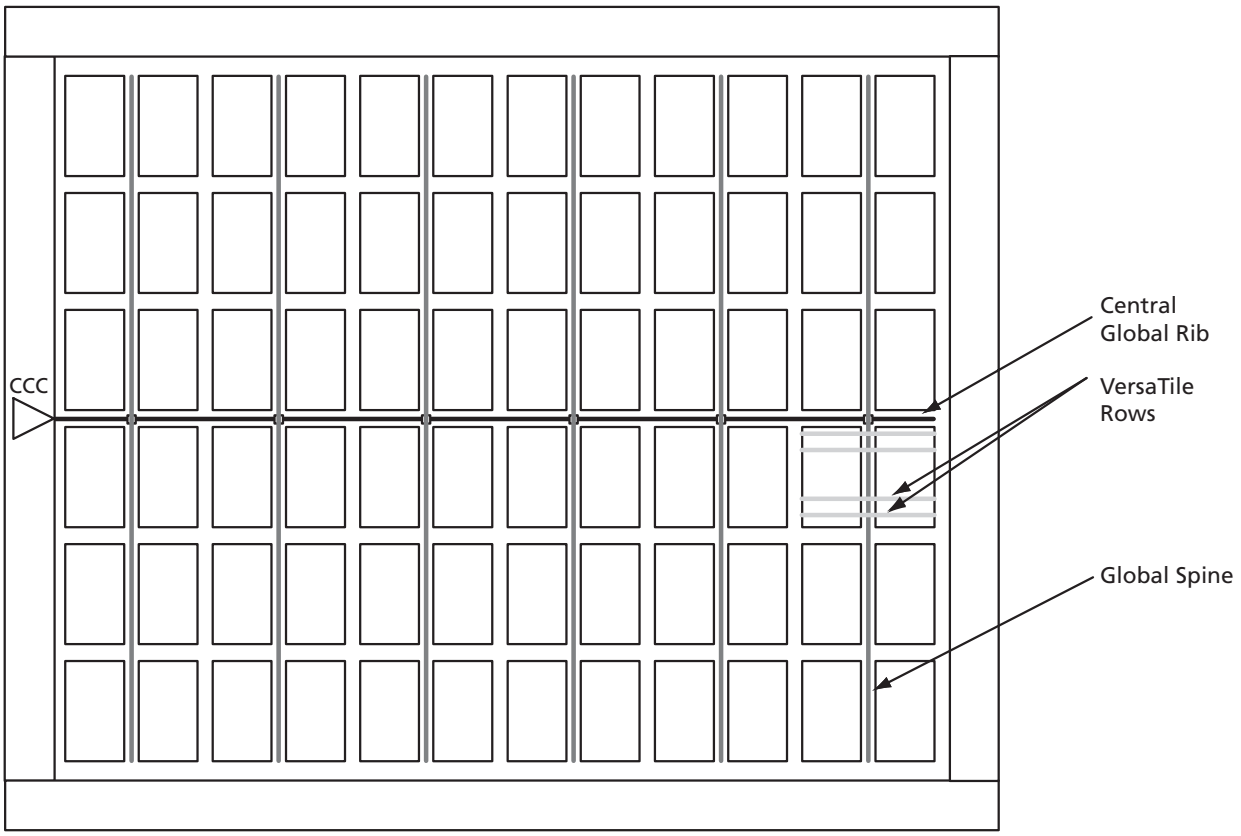


Figure 2-29 **• Example of Global Tree Use in an AGL250 Device for Clock Routing**

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-98. Table 2-153 to Table 2-166 on page 2-97 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

1.5 V DC Core Voltage

***Table 2-153* • AGL015 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	1.21	1.42	ns
t_{RCKH}	Input HIGH Delay for Global Clock	1.23	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-154* • AGL030 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	1.21	1.42	ns
t_{RCKH}	Input HIGH Delay for Global Clock	1.23	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-155* • AGL060 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	1.33	1.55	ns
t_{RCKH}	Input HIGH Delay for Global Clock	1.35	1.62	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-156* • AGL125 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	1.36	1.71	ns
t_{RCKH}	Input HIGH Delay for Global Clock	1.39	1.82	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-157* • AGL250 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	1.39	1.73	ns
t_{RCKH}	Input HIGH Delay for Global Clock	1.41	1.84	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.43	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-158* • AGL600 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	1.48	1.82	ns
t_{RCKH}	Input HIGH Delay for Global Clock	1.52	1.94	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.42	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-159 • **AGL1000 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	1.55	1.89	ns
t_{RCKH}	Input HIGH Delay for Global Clock	1.60	2.02	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.42	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

1.2 V DC Core Voltage

***Table 2-160* • AGL015 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	1.79	2.09	ns
t_{RCKH}	Input HIGH Delay for Global Clock	1.87	2.26	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.39	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-161* • AGL030 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	1.80	2.09	ns
t_{RCKH}	Input HIGH Delay for Global Clock	1.88	2.27	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.39	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-162* • AGL060 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	2.04	2.33	ns
t_{RCKH}	Input HIGH Delay for Global Clock	2.10	2.51	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.40	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-163* • AGL125 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	2.08	2.54	ns
t_{RCKH}	Input HIGH Delay for Global Clock	2.15	2.77	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.62	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-164* • AGL250 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	2.11	2.57	ns
t_{RCKH}	Input HIGH Delay for Global Clock	2.19	2.81	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.62	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-165* • AGL600 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	2.22	2.67	ns
t_{RCKH}	Input HIGH Delay for Global Clock	2.32	2.93	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.61	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-166 • **AGL1000 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.14 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	2.31	2.76	ns
t_{RCKH}	Input HIGH Delay for Global Clock	2.42	3.03	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.61	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Clock Conditioning Circuits

CCC Electrical Specifications

Timing Characteristics

***Table 2-167* • IGLOO CCC/PLL Specification**
For IGLOO V2 or V5 Devices, 1.5 V DC Core Supply Voltage

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		250	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		250	MHz
Delay Increments in Programmable Delay Blocks [1, 2]		360		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL[3]			100	ns
Input Cycle-to-Cycle Jitter (peak magnitude)			1	ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}	Maximum Peak-to-Peak Period Jitter			
	1 Global Network Used	External FB Used	3 Global Networks Used	
0.75 MHz to 24 MHz	0.50%	0.75%	0.70%	
24 MHz to 100 MHz	1.00%	1.50%	1.20%	
100 MHz to 250 MHz	2.50%	3.75%	2.75%	
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter				
LockControl = 0			2.5	ns
LockControl = 1			1.5	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2, 4]	1.25		15.65	ns
Delay Range in Block: Programmable Delay 2 [1, 2, 4]	0.025		15.65	ns
Delay Range in Block: Fixed Delay [1, 2, 4]		3.5		ns

Notes:

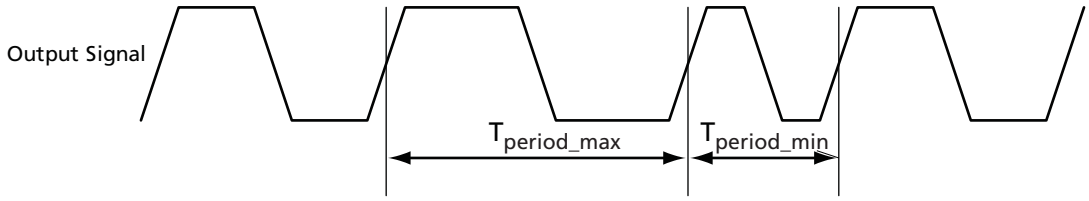
1. *This delay is a function of voltage and temperature. See Table 2-6 on page 2-6 and Table 2-7 on page 2-7 for deratings.*
2. *T_J = 25°C, V_{CC} = 1.5 V*
3. *Maximum value obtained for a Std. speed grade device in Worst-Case Commercial Conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
4. *For the definitions of Type 1 and Type 2, refer to the PLL Block Diagram in the Clock Conditioning Circuits in IGLOO and ProASIC3 Devices chapter of the handbook.*
5. *The AGL030 device does not support PLL.*
6. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*

***Table 2-168* • IGLOO CCC/PLL Specification**
For IGLOO V2 Devices, 1.2 V DC Core Supply Voltage

Parameter	Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		160	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		160	MHz
Delay Increments in Programmable Delay Blocks [1, 2]		580		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Serial Clock (SCLK) for Dynamic PLL[3]			60	ns
Input Cycle-to-Cycle Jitter (peak magnitude)			0.25	ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}	Maximum Peak-to-Peak Period Jitter			
	1 Global Network Used	External FB Used	3 Global Networks Used	
0.75 MHz to 24 MHz	0.50%	0.75%	0.70%	
24 MHz to 100 MHz	1.00%	1.50%	1.20%	
100 MHz to 160 MHz	2.50%	3.75%	2.75%	
Acquisition Time				
LockControl = 0			300	µs
LockControl = 1			6.0	ms
Tracking Jitter				
LockControl = 0			4	ns
LockControl = 1			3	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2, 4]	2.3		20.86	ns
Delay Range in Block: Programmable Delay 2 [1, 2, 4]	0.025		20.86	ns
Delay Range in Block: Fixed Delay [1, 2, 4]		5.7		ns

Notes:

1. *This delay is a function of voltage and temperature. See Table 2-6 on page 2-6 and Table 2-7 on page 2-7 for deratings.*
2. *T_J = 25°C, V_{CC} = 1.5 V*
3. *Maximum value obtained for a Std. speed grade device in Worst-Case Commercial Conditions. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
4. *For the definitions of Type 1 and Type 2, refer to the PLL Block Diagram in the Clock Conditioning Circuits in IGLOO and ProASIC3 Devices chapter of the handbook.*
5. *The AGL030 device does not support PLL.*
6. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*



Note: Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period_max} - T_{period_min}$.

***Figure 2-30* • Peak-to-Peak Jitter Definition**

Embedded SRAM and FIFO Characteristics

SRAM

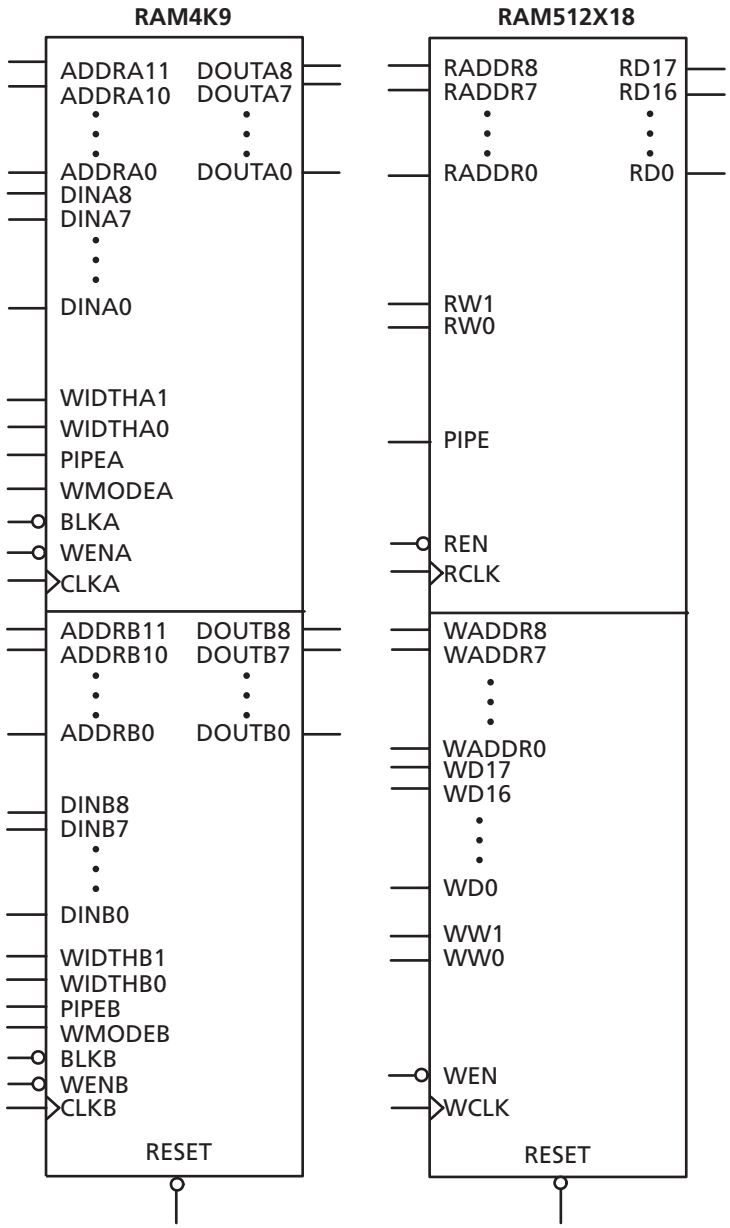


Figure 2-31 • **RAM Models**

Timing Waveforms

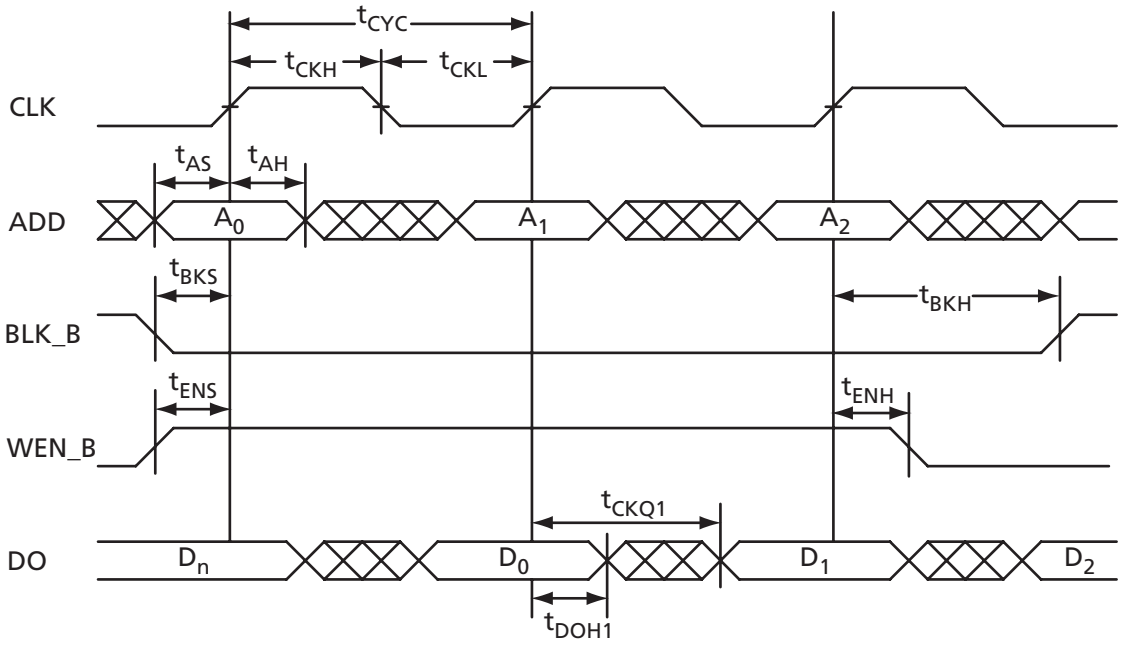


Figure 2-32 • **RAM Read for Pass-Through Output**

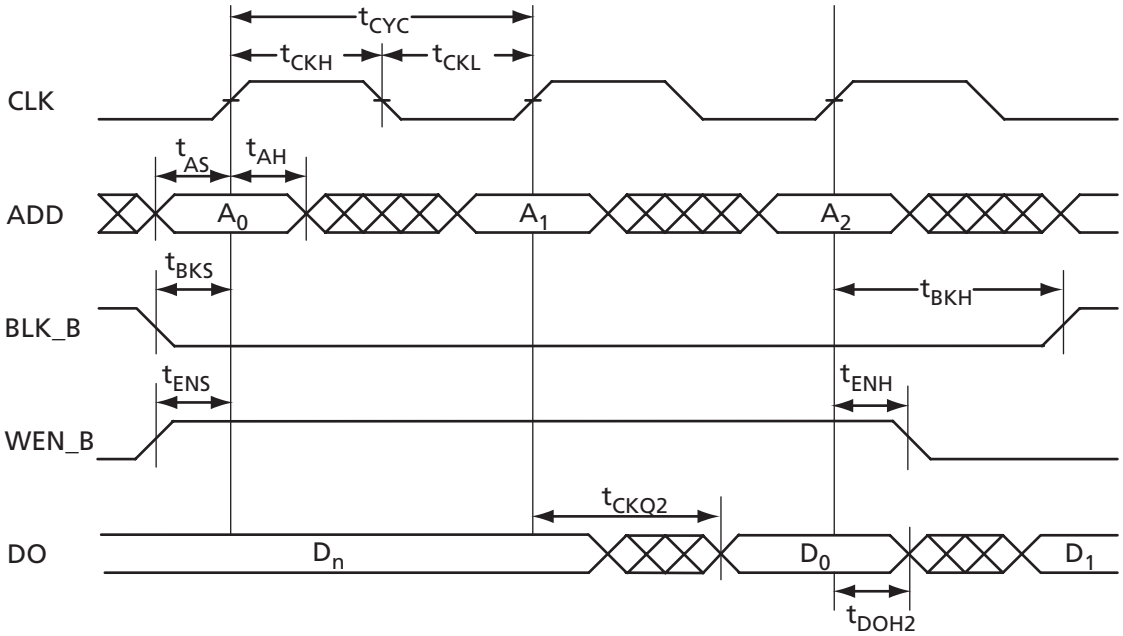


Figure 2-33 • **RAM Read for Pipelined Output**

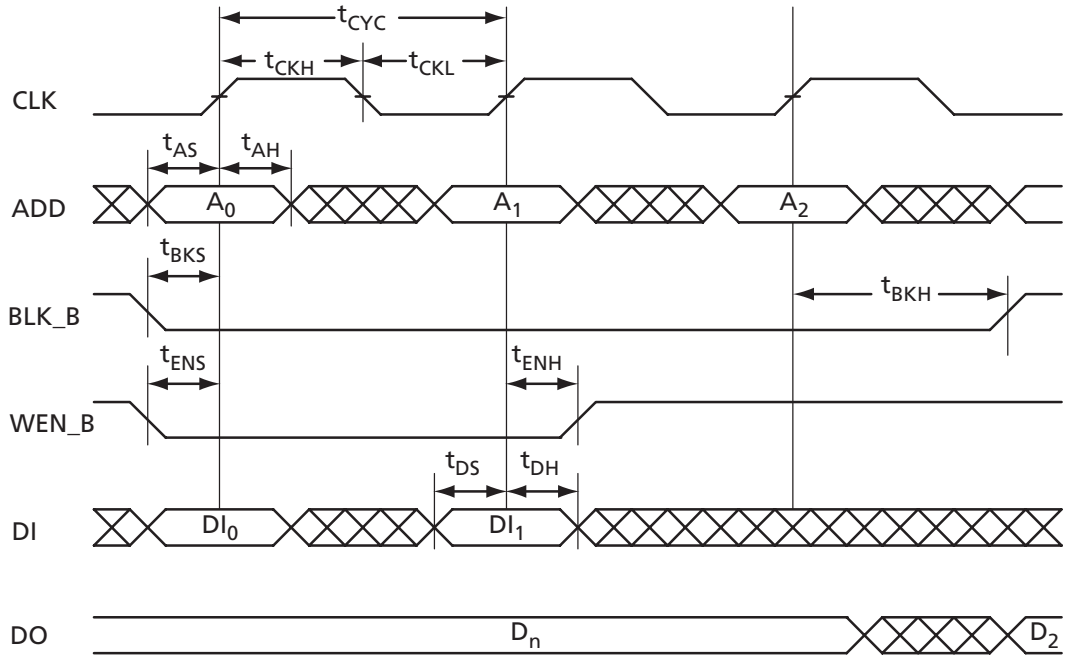


Figure 2-34 • **RAM Write, Output Retained (WMODE = 0)**

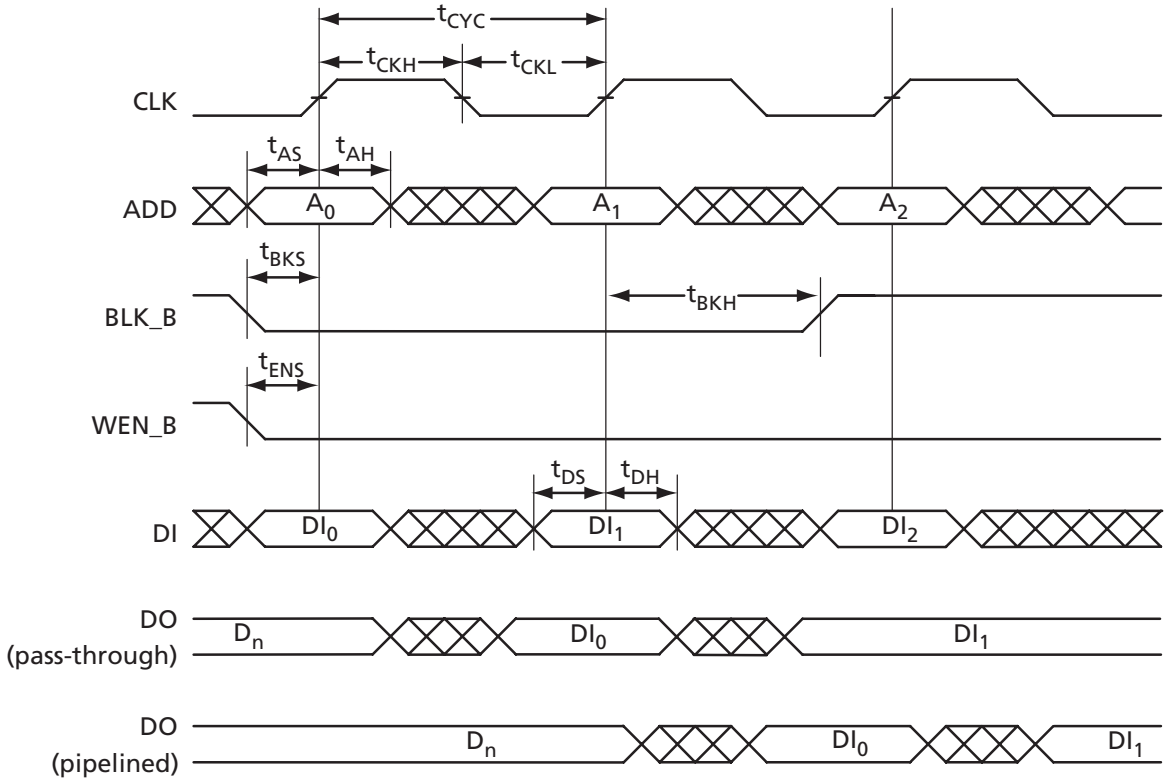


Figure 2-35 • **RAM Write, Output as Write Data (WMODE = 1)**

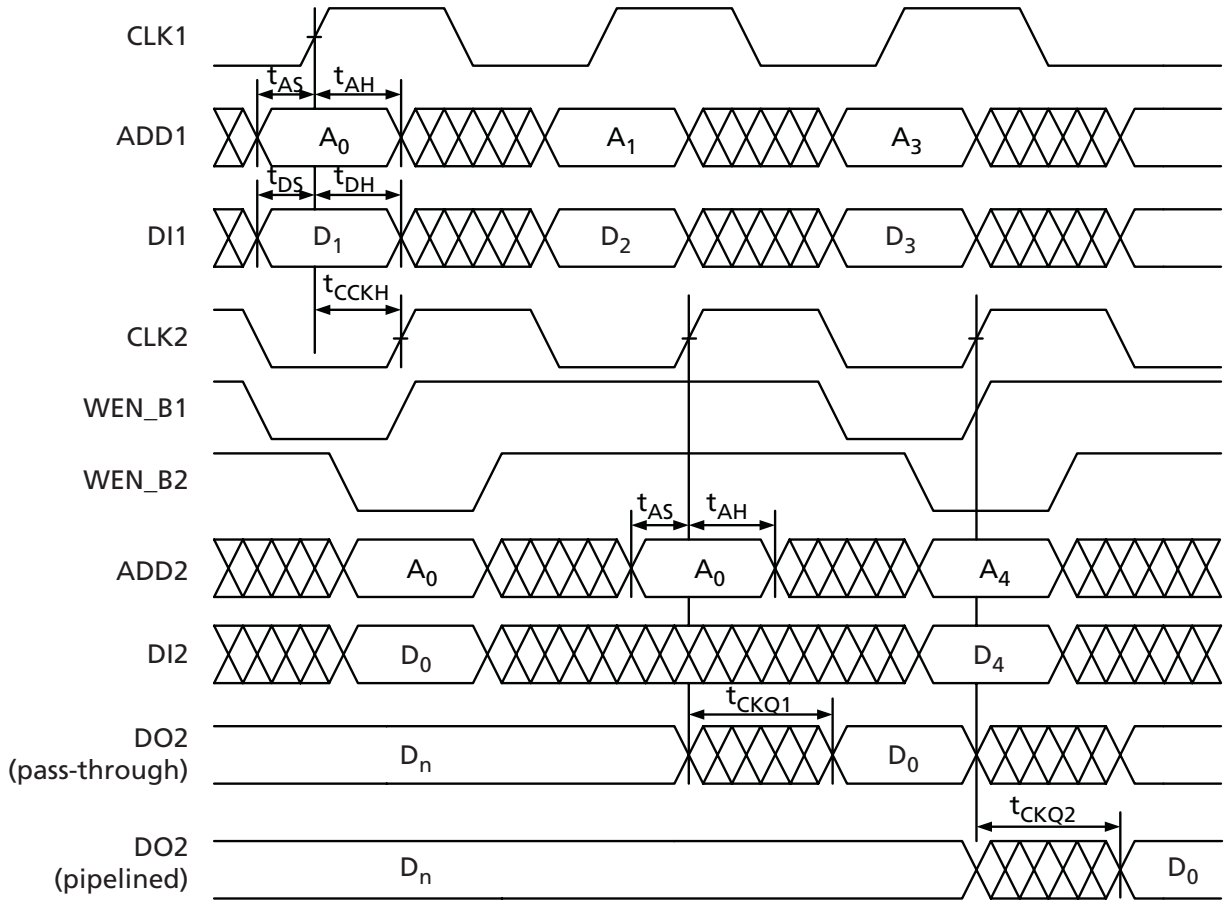


Figure 2-36 • **Write Access after Write onto Same Address**

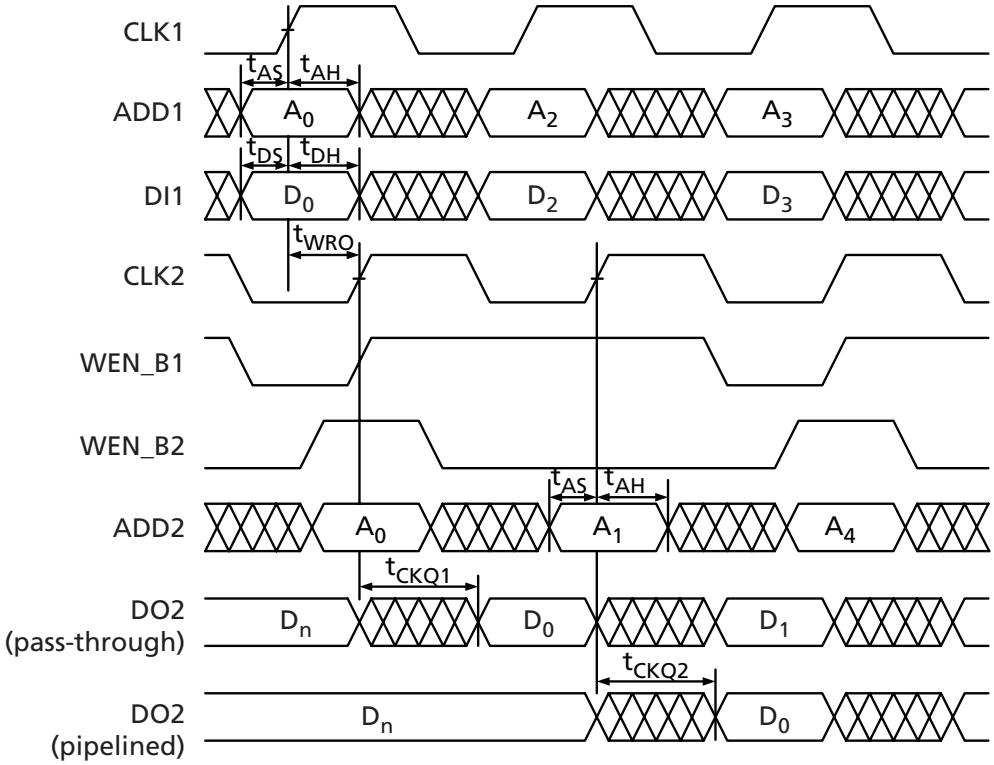


Figure 2-37 • **Read Access after Write onto Same Address**

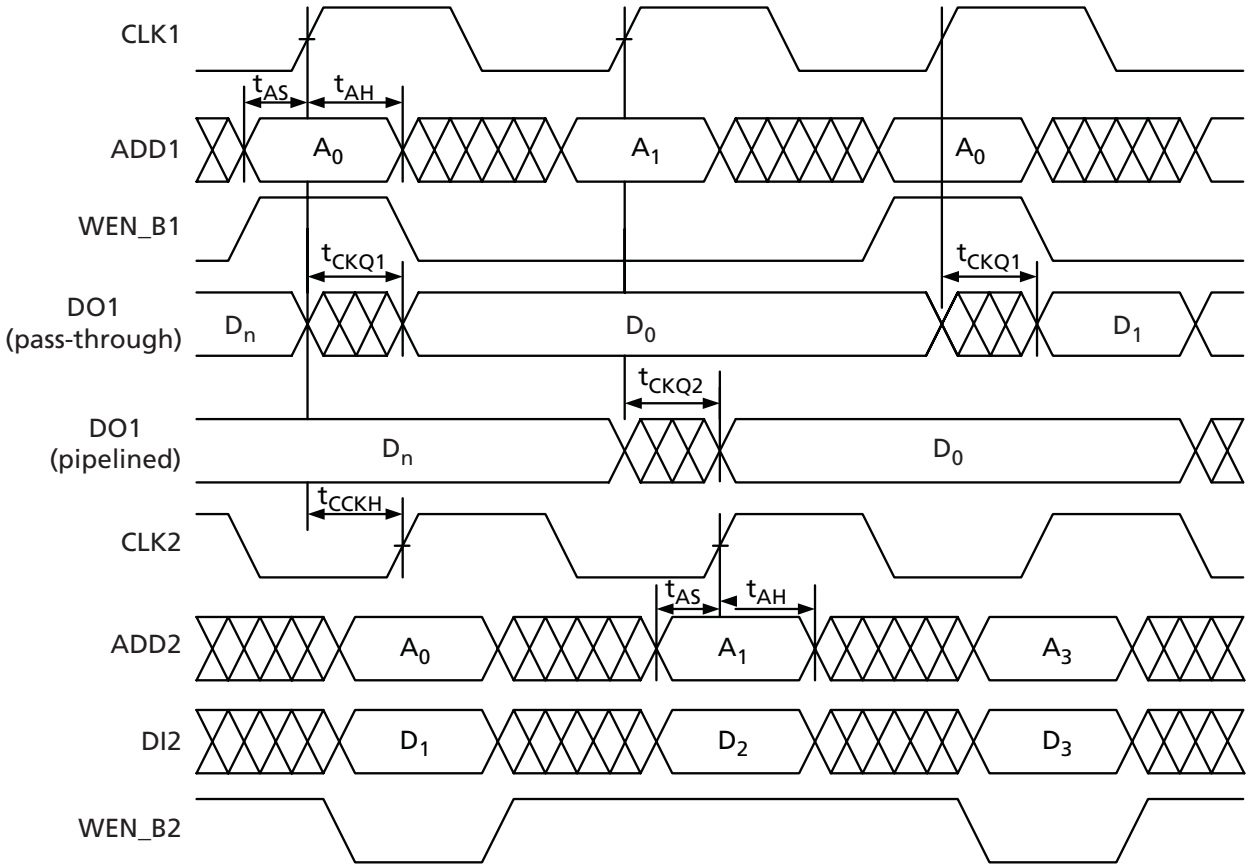


Figure 2-38 **• Write Access after Read onto Same Address**

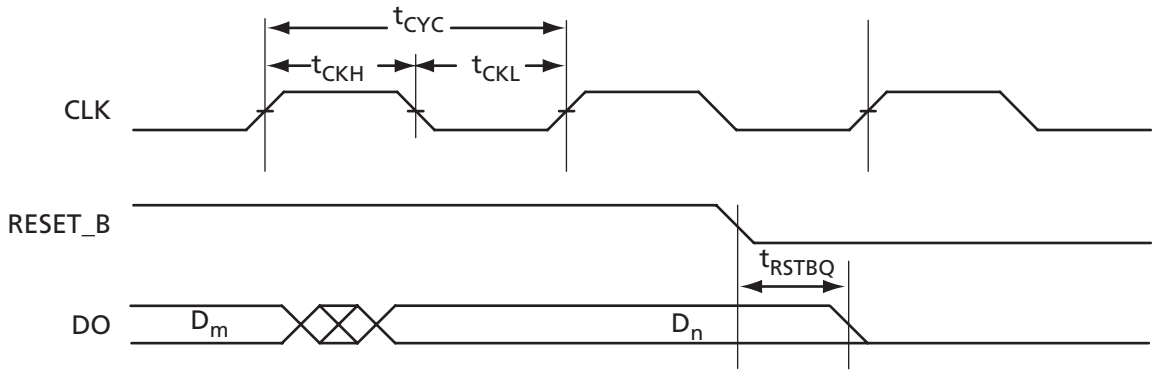


Figure 2-39 **• RAM Reset**

Timing Characteristics

1.5 V DC Core Voltage

***Table 2-169* • RAM4K9**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	0.83	ns
t_{AH}	Address hold time	0.16	ns
t_{ENS}	REN_B, WEN_B setup time	0.81	ns
t_{ENH}	REN_B, WEN_B hold time	0.16	ns
t_{BKS}	BLK_B setup time	1.65	ns
t_{BKH}	BLK_B hold time	0.16	ns
t_{DS}	Input data (DI) setup time	0.71	ns
t_{DH}	Input data (DI) hold time	0.36	ns
t_{CKQ1}	Clock HIGH to new data valid on DO (output retained, WMODE = 0)	3.53	ns
	Clock HIGH to new data valid on DO (flow-through, WMODE = 1)	3.06	ns
t_{CKQ2}	Clock HIGH to new data valid on DO (pipelined)	1.81	ns
t_{WRO}	Address collision clk-to-clk delay for reliable read access after write on same address	TBD	ns
t_{CCKH}	Address collision clk-to-clk delay for reliable write access after write/read on same address	TBD	ns
t_{RSTBQ}	RESET_B LOW to data out LOW on DO (flow-through)	2.06	ns
	RESET_B LOW to data out LOW on DO (pipelined)	2.06	ns
$t_{REMRSTB}$	RESET_B removal	0.61	ns
$t_{RECRSTB}$	RESET_B recovery	3.21	ns
$t_{MPWRSTB}$	RESET_B minimum pulse width	0.68	ns
t_{CYC}	Clock cycle time	6.24	ns
F_{MAX}	Maximum frequency	160	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-170 • **RAM512X18**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	0.83	ns
t_{AH}	Address hold time	0.16	ns
t_{ENS}	REN_B, WEN_B setup time	0.73	ns
t_{ENH}	REN_B, WEN_B hold time	0.08	ns
t_{DS}	Input data (DI) setup time	0.71	ns
t_{DH}	Input data (DI) hold time	0.36	ns
t_{CKQ1}	Clock HIGH to new data valid on DO (output retained, WMODE = 0)	4.21	ns
t_{CKQ2}	Clock HIGH to new data valid on DO (pipelined)	1.71	ns
t_{WRO}	Address collision clk-to-clk delay for reliable read access after write on same address	TBD	ns
t_{CCKH}	Address collision clk-to-clk delay for reliable write access after write/read on same address	TBD	ns
t_{RSTBQ}	RESET_B LOW to data out LOW on DO (flow-through)	2.06	ns
	RESET_B LOW to data out LOW on DO (pipelined)	2.06	ns
$t_{REMRSTB}$	RESET_B removal	0.61	ns
$t_{RECRSTB}$	RESET_B recovery	3.21	ns
$t_{MPWRSTB}$	RESET_B minimum pulse width	0.68	ns
t_{CYC}	Clock cycle time	6.24	ns
F_{MAX}	Maximum frequency	160	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

***Table 2-171* • RAM4K9**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	1.53	ns
t_{AH}	Address hold time	0.29	ns
t_{ENS}	REN_B, WEN_B setup time	1.50	ns
t_{ENH}	REN_B, WEN_B hold time	0.29	ns
t_{BKS}	BLK_B setup time	3.05	ns
t_{BKH}	BLK_B hold time	0.29	ns
t_{DS}	Input data (DI) setup time	1.33	ns
t_{DH}	Input data (DI) hold time	0.66	ns
t_{CKQ1}	Clock HIGH to new data valid on DO (output retained, WMODE = 0)	6.61	ns
	Clock HIGH to new data valid on DO (flow-through, WMODE = 1)	5.72	ns
t_{CKQ2}	Clock HIGH to new data valid on DO (pipelined)	3.38	ns
t_{WRO}	Address collision clk-to-clk delay for reliable read access after write on same address	TBD	ns
t_{CCKH}	Address collision clk-to-clk delay for reliable write access after write/read on same address	TBD	ns
t_{RSTBQ}	RESET_B LOW to data out LOW on DO (flow-through)	3.86	ns
	RESET_B LOW to data out LOW on DO (pipelined)	3.86	ns
$t_{REMRSTB}$	RESET_B removal	1.12	ns
$t_{RECRSTB}$	RESET_B recovery	5.93	ns
$t_{MPWRSTB}$	RESET_B minimum pulse width	1.18	ns
t_{CYC}	Clock cycle time	10.90	ns
F_{MAX}	Maximum frequency	92	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-172 • **RAM512X18**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	1.53	ns
t_{AH}	Address hold time	0.29	ns
t_{ENS}	REN_B, WEN_B setup time	1.36	ns
t_{ENH}	REN_B, WEN_B hold time	0.15	ns
t_{DS}	Input data (DI) setup time	1.33	ns
t_{DH}	Input data (DI) hold time	0.66	ns
t_{CKQ1}	Clock HIGH to new data valid on DO (output retained, WMODE = 0)	7.88	ns
t_{CKQ2}	Clock HIGH to new data valid on DO (pipelined)	3.20	ns
t_{WRO}	Address collision clk-to-clk delay for reliable read access after write on same address	TBD	ns
t_{CCKH}	Address collision clk-to-clk delay for reliable write access after write/read on same address	TBD	ns
t_{RSTBQ}	RESET_B LOW to data out LOW on DO (flow through)	3.86	ns
	RESET_B LOW to data out LOW on DO (pipelined)	3.86	ns
$t_{REMRSTB}$	RESET_B removal	1.12	ns
$t_{RECRSTB}$	RESET_B recovery	5.93	ns
$t_{MPWRSTB}$	RESET_B minimum pulse width	1.18	ns
t_{CYC}	Clock cycle time	10.90	ns
F_{MAX}	Maximum frequency	92	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

FIFO

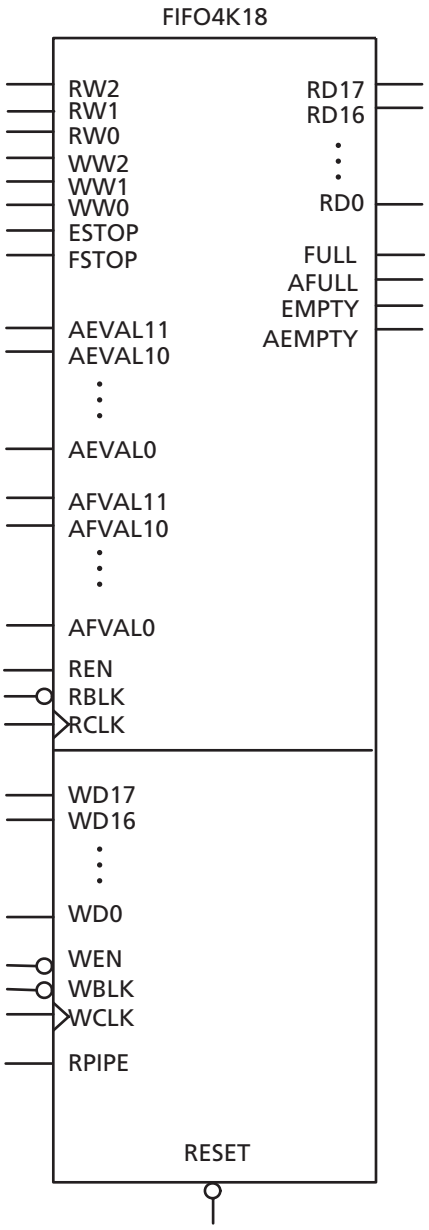


Figure 2-40 • **FIFO Model**

Timing Waveforms

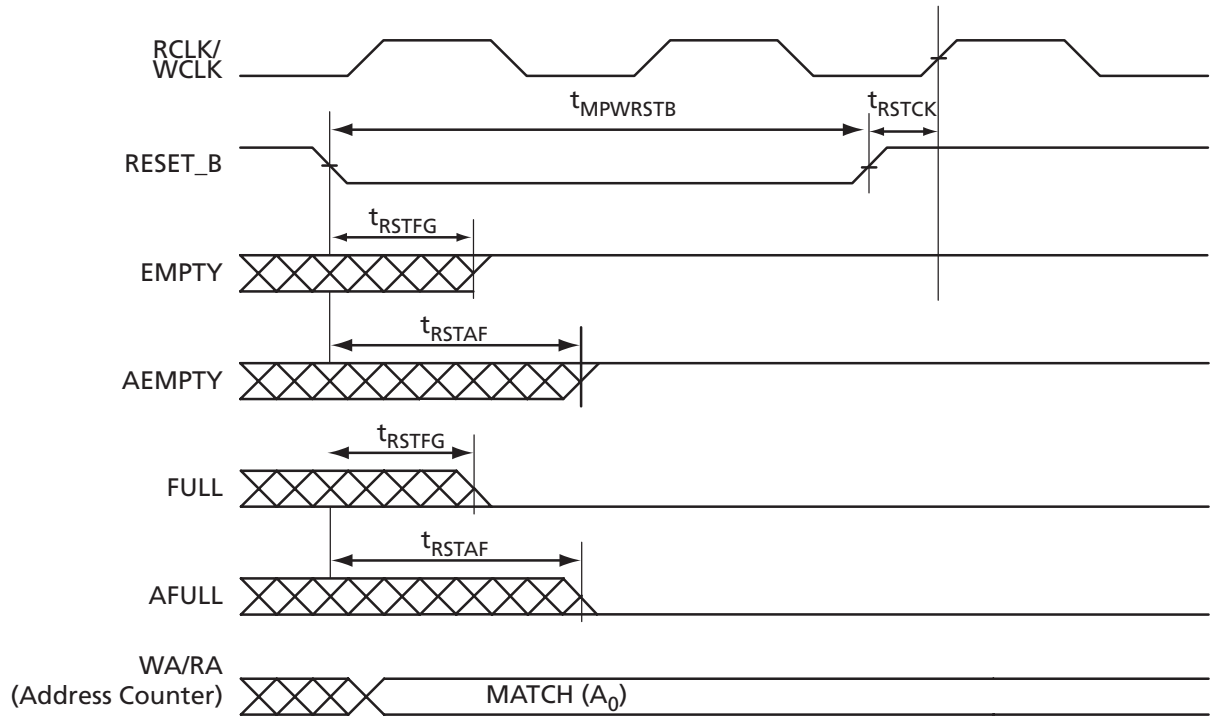


Figure 2-41 **• FIFO Reset**

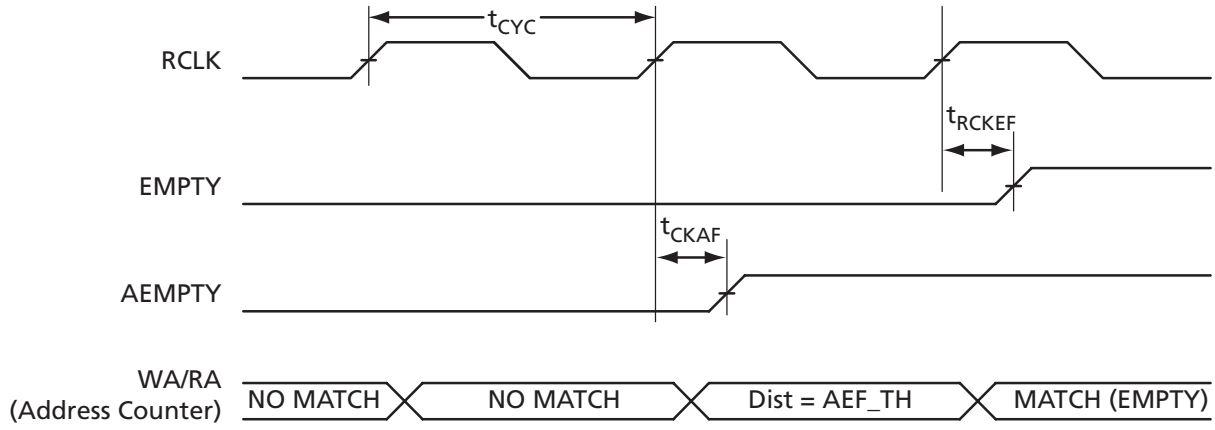


Figure 2-42 **• FIFO EMPTY Flag and AEMPTY Flag Assertion**

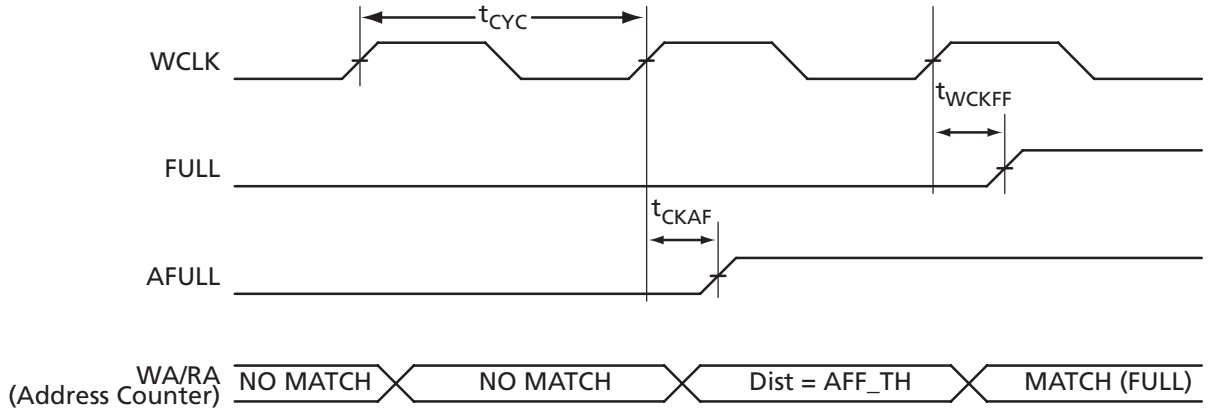


***Figure 2-43* • FIFO FULL Flag and AFULL Flag Assertion**

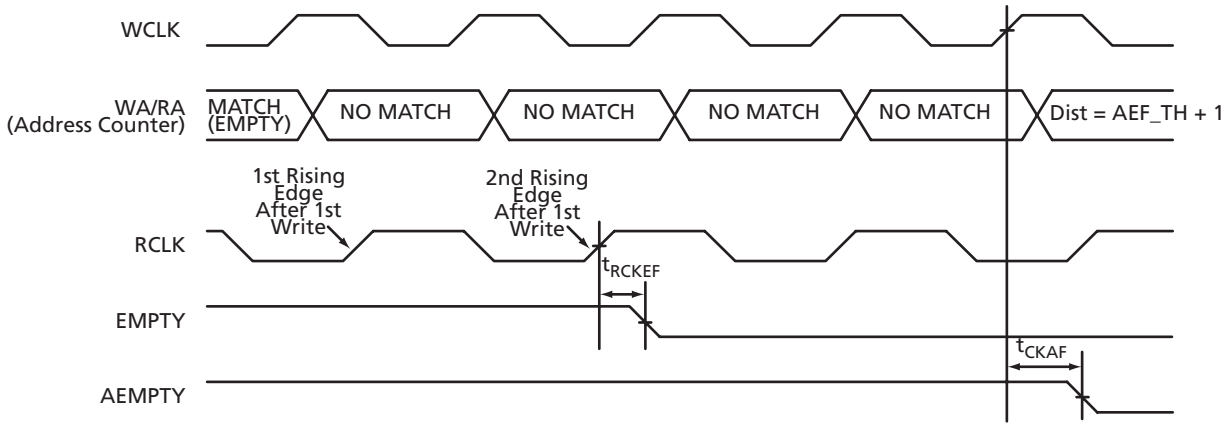


***Figure 2-44* • FIFO EMPTY Flag and AEMPTY Flag Deassertion**

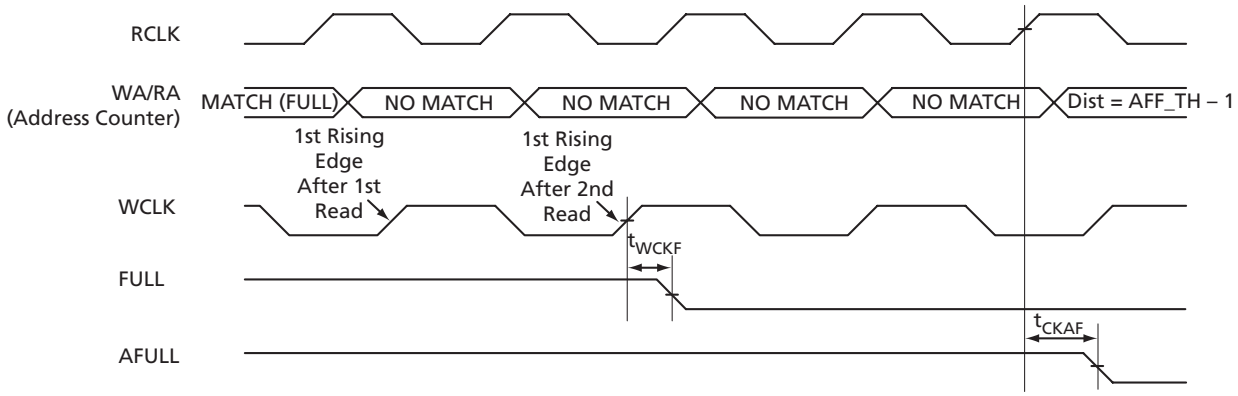


***Figure 2-45* • FIFO FULL Flag and AFULL Flag Deassertion**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-173 • **FIFO**

Worst Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	Std.	Units
t_{ENS}	REN_B, WEN_B Setup Time	1.99	ns
t_{ENH}	REN_B, WEN_B Hold Time	0.16	ns
t_{BKS}	BLK_B Setup Time	0.30	ns
t_{BKH}	BLK_B Hold Time	0.00	ns
t_{DS}	Input Data (DI) Setup Time	0.76	ns
t_{DH}	Input Data (DI) Hold Time	0.25	ns
t_{CKQ1}	Clock HIGH to New Data Valid on DO (flow-through)	3.33	ns
t_{CKQ2}	Clock HIGH to New Data Valid on DO (pipelined)	1.80	ns
t_{RCKEF}	RCLK HIGH to Empty Flag Valid	3.53	ns
t_{WCKFF}	WCLK HIGH to Full Flag Valid	3.35	ns
t_{CKAF}	Clock HIGH to Almost Empty/Full Flag Valid	12.85	ns
t_{RSTFG}	RESET_B LOW to Empty/Full Flag Valid	3.48	ns
t_{RSTAF}	RESET_B LOW to Almost Empty/Full Flag Valid	12.72	ns
t_{RSTBQ}	RESET_B LOW to Data Out LOW on DO (flow-through)	2.02	ns
	RESET_B LOW to Data Out LOW on DO (pipelined)	2.02	ns
$t_{REMRSTB}$	RESET_B Removal	0.61	ns
$t_{RECRSTB}$	RESET_B Recovery	3.21	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.68	ns
t_{CYC}	Clock Cycle Time	6.24	ns
F_{MAX}	Maximum Frequency for FIFO	160	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.2 V DC Core Voltage

***Table 2-174* • FIFO**
Worst Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.14 V

Parameter	Description	Std.	Units
t_{ENS}	REN_B, WEN_B Setup Time	4.13	ns
t_{ENH}	REN_B, WEN_B Hold Time	0.31	ns
t_{BKS}	BLK_B Setup Time	0.47	ns
t_{BKH}	BLK_B Hold Time	0.00	ns
t_{DS}	Input Data (DI) Setup Time	1.56	ns
t_{DH}	Input Data (DI) Hold Time	0.49	ns
t_{CKQ1}	Clock HIGH to New Data Valid on DO (flow-through)	6.80	ns
t_{CKQ2}	Clock HIGH to New Data Valid on DO (pipelined)	3.62	ns
t_{RCKEF}	RCLK HIGH to Empty Flag Valid	7.23	ns
t_{WCKFF}	WCLK HIGH to Full Flag Valid	6.85	ns
t_{CKAF}	Clock HIGH to Almost Empty/Full Flag Valid	26.61	ns
t_{RSTFG}	RESET_B LOW to Empty/Full Flag Valid	7.12	ns
t_{RSTAF}	RESET_B LOW to Almost Empty/Full Flag Valid	26.33	ns
t_{RSTBQ}	RESET_B LOW to Data Out LOW on DO (flow-through)	4.09	ns
	RESET_B LOW to Data Out LOW on DO (pipelined)	4.09	ns
$t_{REMRSTB}$	RESET_B Removal	1.23	ns
$t_{RECRSTB}$	RESET_B Recovery	6.58	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	1.18	ns
t_{CYC}	Clock Cycle Time	10.90	ns
F_{MAX}	Maximum Frequency for FIFO	92	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Embedded FlashROM Characteristics

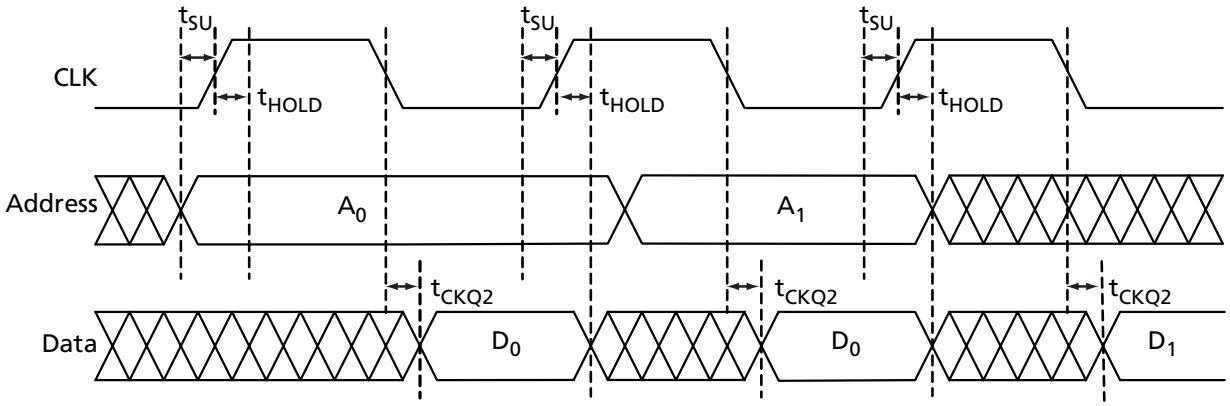


Figure 2-46 **• Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-175 **• Embedded FlashROM Access Time**
Worst Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.57	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	34.14	ns
F_{MAX}	Maximum Clock Frequency	15	MHz

1.2 V DC Core Voltage

Table 2-176 **• Embedded FlashROM Access Time**
Worst Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.14 V

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.59	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	52.90	ns
F_{MAX}	Maximum Clock Frequency	10	MHz

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-19 for more details.

Timing Characteristics

***Table 2-177* • JTAG 1532**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.00	ns
t_{DIHD}	Test Data Input Hold Time	2.00	ns
t_{TMSSU}	Test Mode Select Setup Time	1.00	ns
t_{TMDHD}	Test Mode Select Hold Time	2.00	ns
t_{TCK2Q}	Clock to Q (data out)	8.00	ns
t_{RSTB2Q}	Reset to Q (data out)	25.00	ns
F_{TCKMAX}	TCK Maximum Frequency	15	MHz
$t_{TRSTREM}$	ResetB Removal Time	0.58	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.00	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

***Table 2-178* • JTAG 1532**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	Std.	Units
t_{DISU}	Test Data Input Setup Time	1.50	ns
t_{DIHD}	Test Data Input Hold Time	3.00	ns
t_{TMSSU}	Test Mode Select Setup Time	1.50	ns
t_{TMDHD}	Test Mode Select Hold Time	3.00	ns
t_{TCK2Q}	Clock to Q (data out)	11.00	ns
t_{RSTB2Q}	Reset to Q (data out)	30.00	ns
F_{TCKMAX}	TCK Maximum Frequency	9.00	MHz
$t_{TRSTREM}$	ResetB Removal Time	1.18	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.00	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Part Number and Revision Date

Part Number 51700095-002-3
Revised August 2008

List of Changes

The following table lists critical changes that were made in the current version of the chapter.

Previous Version	Changes in Current Version (Advance v0.4)	Page
Advance v0.3 (July 2008)	3.0 V LVCMOS wide range support data was added to Table 2-2 · Recommended Operating Conditions [4].	2-2
	3.3 V LVCMOS wide range support data was added to Table 2-24 · Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings to Table 2-26 · Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings.	2-23 to 2-24
	3.3 V LVCMOS wide range support data was added to Table 2-27 · Summary of Maximum and Minimum DC Input Levels.	2-24
	3.3 V LVCMOS wide range support text was added to Table 2-49 · Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range.	2-37
	Table 2-49 · Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range is new.	2-37
Advance v0.2 (July 2008)	As a result of the Libero IDE v8.4 release, Actel now offers a wide range of core voltage support. The document was updated to change 1.2 V / 1.5 V to 1.2 V to 1.5 V.	N/A
Advance v0.1 (January 2008)	Tables have been updated to reflect default values in the software. The default I/O capacitance is 5 pF. Tables have been updated to include the LVCMOS 1.2 V I/O set. DDR Tables have two additional data points added to reflect both edges for Input DDR setup and hold time. The power data table has been updated to match SmartPower data rather then simulation values. AGL015 global clock delays have been added.	N/A
	Table 2-1 · Absolute Maximum Ratings was updated to combine the V_{CCI} and VMV parameters in one row. The word "output" from the parameter description for V_{CCI} and VMV, and table note 3 was added.	2-1
Advance v0.1 (January 2008)	Table 2-2 · Recommended Operating Conditions [4] was updated to add references to tables notes 4, 6, 7, and 8. VMV was added to the V_{CCI} parameter row, and table note 9 was added.	2-2
	In Table 2-3 · Flash Programming Limits – Retention, Storage, and Operating Temperature1, the maximum operating junction temperature was changed from 110° to 100°.	2-2
	VMV was removed from Table 2-4 · Overshoot and Undershoot Limits 1. The table title was modified to remove "as measured on quiet I/Os." Table note 2 was revised to remove "estimated SSO density over cycles." Table note 3 was revised to remove "refers only to overshoot/undershoot limits for simultaneous switching I/Os."	2-3
	The "PLL Behavior at Brownout Condition" section is new.	2-4

Previous Version	Changes in Current Version (Advance v0.4)	Page
Advance v0.1 (continued)	Figure 2-2 · V2 Devices – I/O State as a Function of V_{CCI} and V_{CC} Voltage Levels is new.	2-5
	EQ 2-2 was updated. The temperature was changed to 100°C, and therefore the end result changed.	2-6
	The table notes for Table 2-8 · Quiescent Supply Current (I_{DD}) Characteristics, IGLOO Flash*Freeze Mode*, Table 2-9 · Quiescent Supply Current (I_{DD}) Characteristics, IGLOO Sleep Mode (VCC = 0 V)*, and Table 2-10 · Quiescent Supply Current (I_{DD}) Characteristics, IGLOO Shutdown Mode (VCC, VCCI = 0 V)* were updated to remove VMV and include P_{DC6} and P_{DC7}. V_{CCI} and V_{JTAG} were removed from the statement about I_{DD} in the table note for Table 2-9 · Quiescent Supply Current (I_{DD}) Characteristics, IGLOO Sleep Mode (VCC = 0 V)*.	2-7
	Note 2 of Table 2-11 · Quiescent Supply Current (I_{DD}), No IGLOO Flash*Freeze Mode1 was updated to include V_{CCPLL}. Note 4 was updated to include P_{DC6} and P_{DC7}.	2-8
	Table 2-12 · Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings, Table 2-13 · Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings, Table 2-14 · Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings, and Table 2-15 · Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings1 were updated to change P_{DC2} to P_{DC6} and P_{DC3} to P_{DC7}. The table notes were updated to reflect that power was measured on V_{CCI}.	2-9 through 2-10
	Table 2-19 · Different Components Contributing to the Static Power Consumption in IGLOO Devices and Table 2-21 · Different Components Contributing to the Static Power Consumption in IGLOO Device were updated to add P_{DC6} and P_{DC7}, and to change the definition for P_{DC5} to bank quiescent power. Subtitles were added to indicate type of devices and core supply voltage.	2-13, 2-15
	The "Total Static Power Consumption—P_{STAT}" section was updated to revise the calculation of P_{STAT}, including P_{DC6} and P_{DC7}.	2-16
	In Table 2-18 · Different Components Contributing to Dynamic Power Consumption in IGLOO Devices, the description for P_{AC13} was changed from Static to Dynamic.	2-12
	Footnote 1 was updated to include information about P_{AC13}. The PLL Contribution equation was changed from: $P_{PLL} = P_{AC13} + P_{AC14} * F_{CLKOUT}$ to $P_{PLL} = P_{DC4} + P_{AC13} * F_{CLKOUT}$.	2-17
Advance v0.6 (November 2007)	The "Timing Model" was updated to be consistent with the revised timing numbers.	2-19
	In Table 2-26 · Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings, T_J was changed to T_A in notes 1 and 2.	2-24
	All AC Loading figures for single-ended I/O standards were changed from Datapaths at 35 pF to 5 pF.	N/A
	The "1.2 V LVCMOS (JESD8-12A)" section is new.	2-59
	This document was previously in datasheet Advance v0.7. As a result of moving to the handbook format, Actel has restarted the version numbers. The new version number is Advance v0.1.	N/A

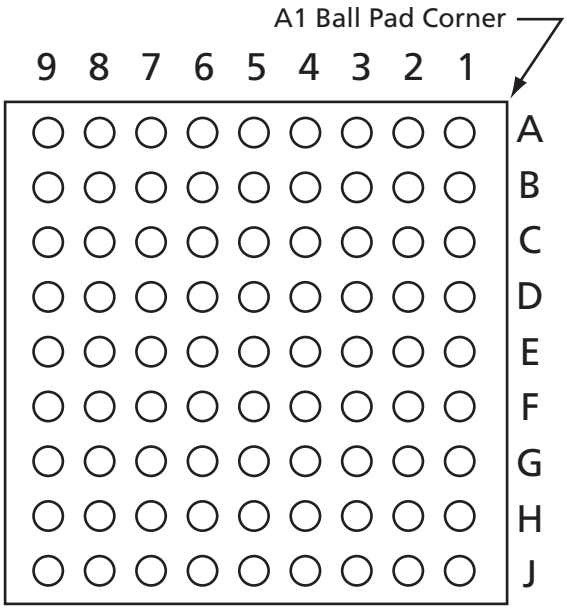
Previous Version	Changes in Current Version (Advance v0.4)	Page
Advance v0.6 (continued)	Table 2-4 • IGLOO CCC/PLL Specification and Table 2-5 • IGLOO CCC/PLL Specification were updated.	2-19, 2-20
	The former Table 2-16 • Maximum I/O Frequency for Single-Ended and Differential I/Os in All Banks in IGLOO Devices (maximum drive strength and high slew selected) was removed.	N/A
	The "During Flash*Freeze Mode" section was updated to include information about the output of the I/O to the FPGA core.	2-57
	Table 2-31 • Flash*Freeze Pin Location in IGLOO Family Packages (device-independent) was updated to add UC81 and CS281. Flash*Freeze pins were assigned for CS81, CS121, and CS196.	2-61
	Figure 2-40 • Flash*Freeze Mode Type 2 – Timing Diagram was updated to modify the LSICC Signal.	2-55
	Information regarding calculation of the quiescent supply current was added to the "Quiescent Supply Current" section.	3-6
	Table 3-8 • Quiescent Supply Current (I_{DD}) Characteristics, IGLOO Flash*Freeze Mode† was updated.	3-6
	Table 3-9 • Quiescent Supply Current (I_{DD}) Characteristics, IGLOO Sleep Mode (VCC = 0 V)† was updated.	3-6
	Table 3-11 • Quiescent Supply Current (I_{DD}), No IGLOO Flash*Freeze Mode1 was updated.	3-7
	Table 3-115 • Minimum and Maximum DC Input and Output Levels was updated.	3-58
	Table 3-156 • JTAG 1532 was updated and Table 3-155 • JTAG 1532 is new.	3-104
Advance v0.3 (August 2007)	The "Power Conservation Techniques" section was updated to recommend that unused I/O signals be left floating.	2-51
Advance v0.2 (July 2007)	The CS81 and CS121 packages were added to Table 2-31 • Flash*Freeze Pin Location in IGLOO Family Packages (device-independent).	2-61
Advance v0.1	The T_J parameter in Table 3-2 • Recommended Operating Conditions was changed to T_A, ambient temperature, and table notes 4–6 were added.	3-2

Actel Safety Critical, Life Support, and High-Reliability Applications Policy

The Actel products described in this advance status datasheet may not have completed Actel's qualification process. Actel may amend or enhance products during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any Actel product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult Actel's Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of Actel's products is available on the Actel website at http://www.actel.com/documents/ORT_Report.pdf. Actel also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local Actel sales office for additional reliability information.

3 – Package Pin Assignments

81-Pin µCSP



Note: This is the bottom view of the package.

Note

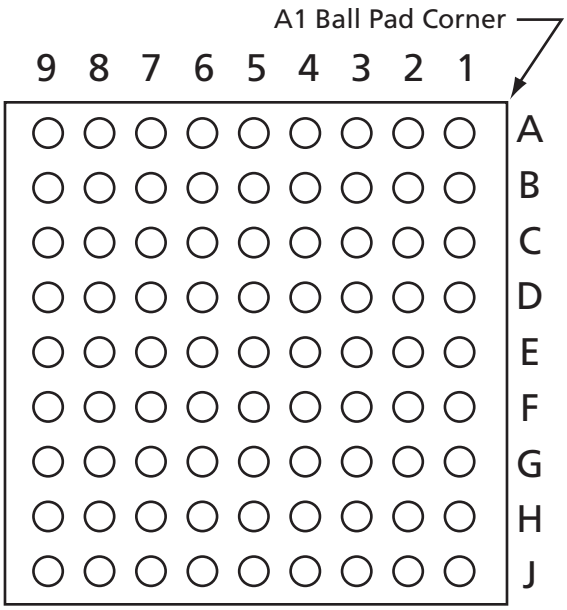
For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

81-Pin µCSP	
Pin Number	AGL030 Function
A1	IO00RSB0
A2	IO02RSB0
A3	IO06RSB0
A4	IO11RSB0
A5	IO16RSB0
A6	IO19RSB0
A7	IO22RSB0
A8	IO24RSB0
A9	IO26RSB0
B1	IO81RSB1
B2	IO04RSB0
B3	IO10RSB0
B4	IO13RSB0
B5	IO15RSB0
B6	IO20RSB0
B7	IO21RSB0
B8	IO28RSB0
B9	IO25RSB0
C1	IO79RSB1
C2	IO80RSB1
C3	IO08RSB0
C4	IO12RSB0
C5	IO17RSB0
C6	IO14RSB0
C7	IO18RSB0
C8	IO29RSB0
C9	IO27RSB0
D1	IO74RSB1
D2	IO76RSB1
D3	IO77RSB1
D4	V_{CC}
D5	$V_{CCIB}0$
D6	GND
D7	IO23RSB0
D8	IO31RSB0
D9	IO30RSB0

81-Pin µCSP	
Pin Number	AGL030 Function
E1	GEB0/IO71RSB1
E2	GEA0/IO72RSB1
E3	GEC0/IO73RSB1
E4	$V_{CCI}B1$
E5	V_{CC}
E6	$V_{CCI}B0$
E7	GDC0/IO32RSB0
E8	GDA0/IO33RSB0
E9	GDB0/IO34RSB0
F1	IO68RSB1
F2	IO67RSB1
F3	IO64RSB1
F4	GND
F5	$V_{CCI}B1$
F6	IO47RSB1
F7	IO36RSB0
F8	IO38RSB0
F9	IO40RSB0
G1	IO65RSB1
G2	IO66RSB1
G3	IO57RSB1
G4	IO53RSB1
G5	IO49RSB1
G6	IO45RSB1
G7	IO46RSB1
G8	V_{JTAG}
G9	TRST
H1	IO62RSB1
H2	FF/IO60RSB1
H3	IO58RSB1
H4	IO54RSB1
H5	IO48RSB1
H6	IO43RSB1
H7	IO42RSB1
H8	TDI
H9	TDO

81-Pin µCSP	
Pin Number	AGL030 Function
J1	IO63RSB1
J2	IO61RSB1
J3	IO59RSB1
J4	IO56RSB1
J5	IO52RSB1
J6	IO44RSB1
J7	TCK
J8	TMS
J9	V_{PUMP}

81-Pin CSP



Note: This is the bottom view of the package.

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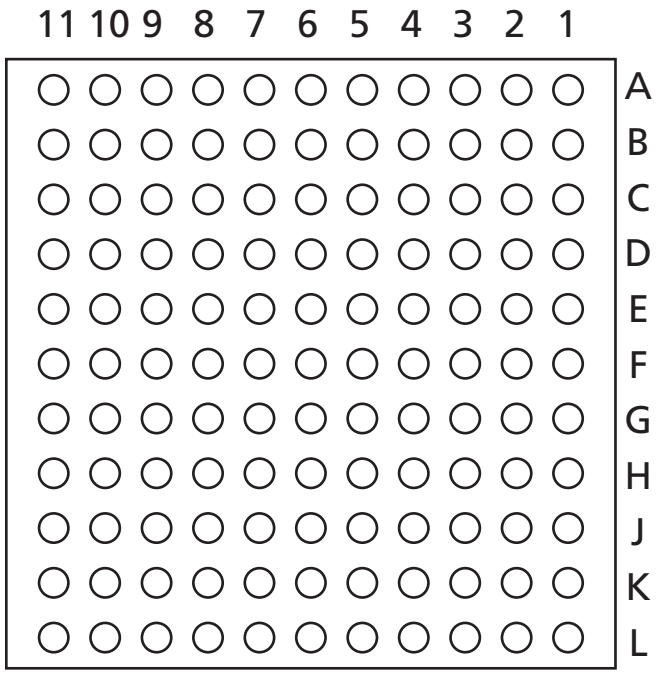
81-Pin CSP	
Pin Number	AGL030 Function
A1	IO00RSB0
A2	IO02RSB0
A3	IO06RSB0
A4	IO11RSB0
A5	IO16RSB0
A6	IO19RSB0
A7	IO22RSB0
A8	IO24RSB0
A9	IO26RSB0
B1	IO81RSB1
B2	IO04RSB0
B3	IO10RSB0
B4	IO13RSB0
B5	IO15RSB0
B6	IO20RSB0
B7	IO21RSB0
B8	IO28RSB0
B9	IO25RSB0
C1	IO79RSB1
C2	IO80RSB1
C3	IO08RSB0
C4	IO12RSB0
C5	IO17RSB0
C6	IO14RSB0
C7	IO18RSB0
C8	IO29RSB0
C9	IO27RSB0
D1	IO74RSB1
D2	IO76RSB1
D3	IO77RSB1
D4	V_{CC}
D5	V_{CCI}B0
D6	GND
D7	IO23RSB0
D8	IO31RSB0
D9	IO30RSB0

81-Pin CSP	
Pin Number	AGL030 Function
E1	GEB0/IO71RSB1
E2	GEA0/IO72RSB1
E3	GEC0/IO73RSB1
E4	V_{CCI}B1
E5	V_{CC}
E6	V_{CCI}B0
E7	GDC0/IO32RSB0
E8	GDA0/IO33RSB0
E9	GDB0/IO34RSB0
F1	IO68RSB1
F2	IO67RSB1
F3	IO64RSB1
F4	GND
F5	V_{CCI}B1
F6	IO47RSB1
F7	IO36RSB0
F8	IO38RSB0
F9	IO40RSB0
G1	IO65RSB1
G2	IO66RSB1
G3	IO57RSB1
G4	IO53RSB1
G5	IO49RSB1
G6	IO44RSB1
G7	IO46RSB1
G8	V_{JTAG}
G9	TRST
H1	IO62RSB1
H2	FF/IO60RSB1
H3	IO58RSB1
H4	IO54RSB1
H5	IO48RSB1
H6	IO43RSB1
H7	IO42RSB1
H8	TDI
H9	TDO

81-Pin CSP	
Pin Number	AGL030 Function
J1	IO63RSB1
J2	IO61RSB1
J3	IO59RSB1
J4	IO56RSB1
J5	IO52RSB1
J6	IO45RSB1
J7	TCK
J8	TMS
J9	V_{PUMP}

121-Pin CSP



Note: This is the bottom view of the package.

Note

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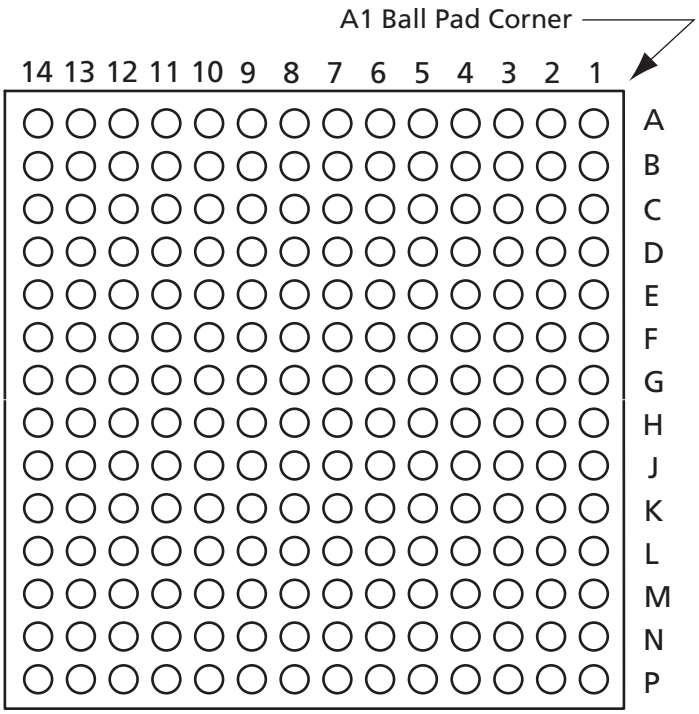
121-Pin CSP	
Pin Number	AGL060 Function
A1	GNDQ
A2	IO01RSB0
A3	GAA1/IO03RSB0
A4	GAC1/IO07RSB0
A5	IO15RSB0
A6	IO13RSB0
A7	IO17RSB0
A8	GBB1/IO22RSB0
A9	GBA1/IO24RSB0
A10	GNDQ
A11	VMV0
B1	GAA2/IO95RSB1
B2	IO00RSB0
B3	GAA0/IO02RSB0
B4	GAC0/IO06RSB0
B5	IO08RSB0
B6	IO12RSB0
B7	IO16RSB0
B8	GBC1/IO20RSB0
B9	GBB0/IO21RSB0
B10	GBB2/IO27RSB0
B11	GBA2/IO25RSB0
C1	IO89RSB1
C2	GAC2/IO91RSB1
C3	GAB1/IO05RSB0
C4	GAB0/IO04RSB0
C5	IO09RSB0
C6	IO14RSB0
C7	GBA0/IO23RSB0
C8	GBC0/IO19RSB0
C9	IO26RSB0
C10	IO28RSB0
C11	GBC2/IO29RSB0
D1	IO88RSB1
D2	IO90RSB1
D3	GAB2/IO93RSB1
D4	IO10RSB0
D5	IO11RSB0
D6	IO18RSB0
D7	IO32RSB0
D8	IO31RSB0

121-Pin CSP	
Pin Number	AGL060 Function
D9	GCA2/IO41RSB0
D10	IO30RSB0
D11	IO33RSB0
E1	IO87RSB1
E2	GFC0/IO85RSB1
E3	IO92RSB1
E4	IO94RSB1
E5	V_{CC}
E6	V_{CCI}B0
E7	GND
E8	GCC0/IO36RSB0
E9	IO34RSB0
E10	GCB1/IO37RSB0
E11	GCC1/IO35RSB0
F1	V_{COMPLF}
F2	GFB0/IO83RSB1
F3	GFA0/IO82RSB1
F4	GFC1/IO86RSB1
F5	V_{CCI}B1
F6	V_{CC}
F7	V_{CCI}B0
F8	GCB2/IO42RSB0
F9	GCC2/IO43RSB0
F10	GCB0/IO38RSB0
F11	GCA1/IO39RSB0
G1	V_{CCPLF}
G2	GFB2/IO79RSB1
G3	GFA1/IO81RSB1
G4	GFB1/IO84RSB1
G5	GND
G6	V_{CCI}B1
G7	V_{CC}
G8	GDC0/IO46RSB0
G9	GDA1/IO49RSB0
G10	GDB0/IO48RSB0
G11	GCA0/IO40RSB0
H1	IO75RSB1
H2	IO76RSB1
H3	GFC2/IO78RSB1
H4	GFA2/IO80RSB1
H5	IO77RSB1

121-Pin CSP	
Pin Number	AGL060 Function
H6	GEC2/IO66RSB1
H7	IO54RSB1
H8	GDC2/IO53RSB1
H9	V_{JTAG}
H10	TRST
H11	IO44RSB0
J1	GEC1/IO74RSB1
J2	GEC0/IO73RSB1
J3	GEB1/IO72RSB1
J4	GEA0/IO69RSB1
J5	FF/GEB2/IO67RSB1
J6	IO62RSB1
J7	GDA2/IO51RSB1
J8	GDB2/IO52RSB1
J9	TDI
J10	TDO
J11	GDC1/IO45RSB0
K1	GEB0/IO71RSB1
K2	GEA1/IO70RSB1
K3	GEA2/IO68RSB1
K4	IO64RSB1
K5	IO60RSB1
K6	IO59RSB1
K7	IO56RSB1
K8	TCK
K9	TMS
K10	V_{PUMP}
K11	GDB1/IO47RSB0
L1	VMV1
L2	GNDQ
L3	IO65RSB1
L4	IO63RSB1
L5	IO61RSB1
L6	IO58RSB1
L7	IO57RSB1
L8	IO55RSB1
L9	GNDQ
L10	GDA0/IO50RSB0
L11	VMV1

196-Pin CSP



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

196-Pin CSP	
Pin Number	AGL125 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAC0/IO04RSB0
A4	GAC1/IO05RSB0
A5	IO09RSB0
A6	IO15RSB0
A7	IO18RSB0
A8	IO22RSB0
A9	IO27RSB0
A10	GBC0/IO35RSB0
A11	GBB0/IO37RSB0
A12	GBB1/IO38RSB0
A13	GBA1/IO40RSB0
A14	GND
B1	V_{CCIB1}
B2	VMV0
B3	GAA1/IO01RSB0
B4	GAB1/IO03RSB0
B5	GND
B6	IO16RSB0
B7	IO20RSB0
B8	IO24RSB0
B9	IO28RSB0
B10	GND
B11	GBC1/IO36RSB0
B12	GBA0/IO39RSB0
B13	GBA2/IO41RSB0
B14	GBB2/IO43RSB0
C1	GAC2/IO128RSB1
C2	GAB2/IO130RSB1
C3	GNDQ
C4	V_{CCIB0}
C5	GAB0/IO02RSB0
C6	IO14RSB0
C7	V_{CCIB0}
C8	NC

196-Pin CSP	
Pin Number	AGL125 Function
C9	IO23RSB0
C10	IO29RSB0
C11	V_{CCIB0}
C12	IO42RSB0
C13	GNDQ
C14	IO44RSB0
D1	IO127RSB1
D2	IO129RSB1
D3	GAA2/IO132RSB1
D4	IO126RSB1
D5	IO06RSB0
D6	IO13RSB0
D7	IO19RSB0
D8	IO21RSB0
D9	IO26RSB0
D10	IO31RSB0
D11	IO30RSB0
D12	VMV0
D13	IO46RSB0
D14	GBC2/IO45RSB0
E1	IO125RSB1
E2	GND
E3	IO131RSB1
E4	V_{CCIB1}
E5	NC
E6	IO08RSB0
E7	IO17RSB0
E8	IO12RSB0
E9	IO11RSB0
E10	NC
E11	V_{CCIB0}
E12	IO32RSB0
E13	GND
E14	IO34RSB0
F1	IO124RSB1
F2	IO114RSB1

196-Pin CSP	
Pin Number	AGL125 Function
F3	IO113RSB1
F4	IO112RSB1
F5	IO111RSB1
F6	NC
F7	V_{CC}
F8	V_{CC}
F9	NC
F10	IO07RSB0
F11	IO25RSB0
F12	IO10RSB0
F13	IO33RSB0
F14	IO47RSB0
G1	GFB1/IO121RSB1
G2	GFA0/IO119RSB1
G3	GFA2/IO117RSB1
G4	V_{COMPLF}
G5	GFC0/IO122RSB1
G6	V_{CC}
G7	GND
G8	GND
G9	V_{CC}
G10	GCC0/IO52RSB0
G11	GCB1/IO53RSB0
G12	GCA0/IO56RSB0
G13	IO48RSB0
G14	GCC2/IO59RSB0
H1	GFB0/IO120RSB1
H2	GFA1/IO118RSB1
H3	V_{CCPLF}
H4	GFB2/IO116RSB1
H5	GFC1/IO123RSB1
H6	V_{CC}
H7	GND
H8	GND
H9	V_{CC}
H10	GCC1/IO51RSB0

196-Pin CSP	
Pin Number	AGL125 Function
H11	GCB0/IO54RSB0
H12	GCA1/IO55RSB0
H13	IO49RSB0
H14	GCA2/IO57RSB0
J1	GFC2/IO115RSB1
J2	IO110RSB1
J3	IO94RSB1
J4	IO93RSB1
J5	IO89RSB1
J6	NC
J7	V_{CC}
J8	V_{CC}
J9	NC
J10	IO60RSB0
J11	GCB2/IO58RSB0
J12	IO50RSB0
J13	GDC1/IO61RSB0
J14	GDC0/IO62RSB0
K1	IO99RSB1
K2	GND
K3	IO95RSB1
K4	V_{CCIB1}
K5	NC
K6	IO86RSB1
K7	IO80RSB1
K8	IO74RSB1
K9	IO72RSB1
K10	NC
K11	V_{CCIB0}
K12	GDA1/IO65RSB0
K13	GND
K14	GDB1/IO63RSB0
L1	GEB1/IO107RSB1
L2	GEC1/IO109RSB1
L3	GEC0/IO108RSB1
L4	IO96RSB1

196-Pin CSP	
Pin Number	AGL125 Function
L5	IO91RSB1
L6	IO90RSB1
L7	IO83RSB1
L8	IO81RSB1
L9	IO71RSB1
L10	IO70RSB1
L11	V_{PUMP}
L12	V_{JTAG}
L13	GDA0/IO66RSB0
L14	GDB0/IO64RSB0
M1	GEB0/IO106RSB1
M2	GEA1/IO105RSB1
M3	GNDQ
M4	V_{CCIB1}
M5	IO92RSB1
M6	IO88RSB1
M7	NC
M8	V_{CCIB1}
M9	IO76RSB1
M10	GDB2/IO68RSB1
M11	V_{CCIB1}
M12	VMV1
M13	TRST
M14	V_{CCIB0}
N1	GEA0/IO104RSB1
N2	VMV1
N3	GEC2/IO101RSB1
N4	IO100RSB1
N5	GND
N6	IO87RSB1
N7	IO82RSB1
N8	IO78RSB1
N9	IO73RSB1
N10	GND
N11	TCK
N12	TDI

196-Pin CSP	
Pin Number	AGL125 Function
N13	GNDQ
N14	TDO
P1	GND
P2	GEA2/IO103RSB1
P3	FF/GEB2/IO102RSB1
P4	IO98RSB1
P5	IO97RSB1
P6	IO85RSB1
P7	IO84RSB1
P8	IO79RSB1
P9	IO77RSB1
P10	IO75RSB1
P11	GDC2/IO69RSB1
P12	GDA2/IO67RSB1
P13	TMS
P14	GND

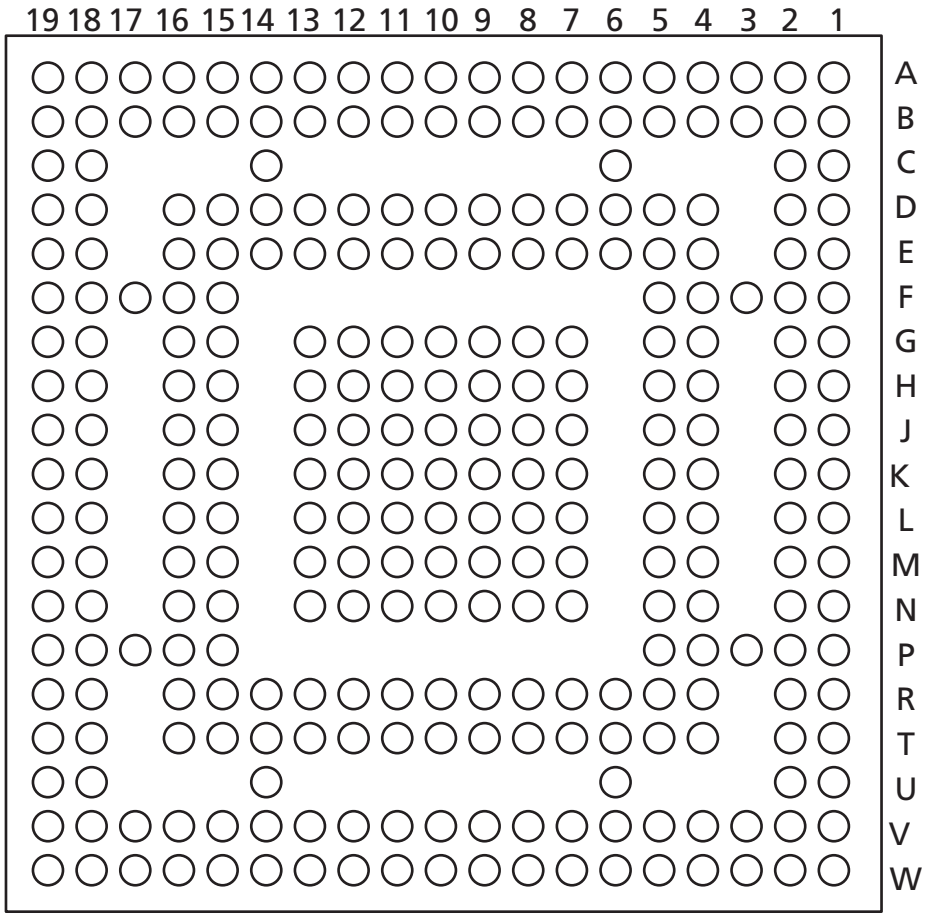
196-Pin CSP		196-Pin CSP		196-Pin CSP	
Pin Number	AGL250 Function	Pin Number	AGL250 Function	Pin Number	AGL250 Function
A1	GND	C9	IO30RSB0	F3	IO111PDB3
A2	GAA0/IO00RSB0	C10	IO33RSB0	F4	IO111NDB3
A3	GAC0/IO04RSB0	C11	V_{CCI}B0	F5	IO113NPB3
A4	GAC1/IO05RSB0	C12	IO41NPB1	F6	IO06RSB0
A5	IO10RSB0	C13	GNDQ	F7	V_{CC}
A6	IO13RSB0	C14	IO42NDB1	F8	V_{CC}
A7	IO17RSB0	D1	IO116VDB3	F9	IO28RSB0
A8	IO19RSB0	D2	IO117VDB3	F10	IO54PDB1
A9	IO23RSB0	D3	GAA2/IO118UDB3	F11	IO54NDB1
A10	GBC0/IO35RSB0	D4	IO113PPB3	F12	IO47NDB1
A11	GBB0/IO37RSB0	D5	IO08RSB0	F13	IO47PDB1
A12	GBB1/IO38RSB0	D6	IO14RSB0	F14	IO45NDB1
A13	GBA1/IO40RSB0	D7	IO15RSB0	G1	GFB1/IO109PDB3
A14	GND	D8	IO18RSB0	G2	GFA0/IO108NDB3
B1	V_{CCI}B3	D9	IO25RSB0	G3	GFA2/IO107PPB3
B2	VMV0	D10	IO32RSB0	G4	V_{COMPLF}
B3	GAA1/IO01RSB0	D11	IO44PPB1	G5	GFC0/IO110NDB3
B4	GAB1/IO03RSB0	D12	VMV1	G6	V_{CC}
B5	GND	D13	IO43NDB1	G7	GND
B6	IO12RSB0	D14	GBC2/IO43PDB1	G8	GND
B7	IO16RSB0	E1	IO112PDB3	G9	V_{CC}
B8	IO22RSB0	E2	GND	G10	GCC0/IO48NDB1
B9	IO24RSB0	E3	IO118VDB3	G11	GCB1/IO49PDB1
B10	GND	E4	V_{CCI}B3	G12	GCA0/IO50NDB1
B11	GBC1/IO36RSB0	E5	IO114USB3	G13	IO53NDB1
B12	GBA0/IO39RSB0	E6	IO07RSB0	G14	GCC2/IO53PDB1
B13	GBA2/IO41PPB1	E7	IO09RSB0	H1	GFB0/IO109NDB3
B14	GBB2/IO42PDB1	E8	IO21RSB0	H2	GFA1/IO108PDB3
C1	GAC2/IO116UDB3	E9	IO31RSB0	H3	V_{CCPLF}
C2	GAB2/IO117UDB3	E10	IO34RSB0	H4	GFB2/IO106PPB3
C3	GNDQ	E11	V_{CCI}B1	H5	GFC1/IO110PDB3
C4	V_{CCI}B0	E12	IO44NPB1	H6	V_{CC}
C5	GAB0/IO02RSB0	E13	GND	H7	GND
C6	IO11RSB0	E14	IO45PDB1	H8	GND
C7	V_{CCI}B0	F1	IO112NDB3	H9	V_{CC}
C8	IO20RSB0	F2	IO107NPB3	H10	GCC1/IO48PDB1

196-Pin CSP	
Pin Number	AGL250 Function
H11	GCB0/IO49NDB1
H12	GCA1/IO50PDB1
H13	IO51NDB1
H14	GCA2/IO51PDB1
J1	GFC2/IO105PDB3
J2	IO104PPB3
J3	IO106NPB3
J4	IO103PDB3
J5	IO103NDB3
J6	IO80RSB2
J7	V_{CC}
J8	V_{CC}
J9	IO64RSB2
J10	IO56PDB1
J11	GCB2/IO52PDB1
J12	IO52NDB1
J13	GDC1/IO58UDB1
J14	GDC0/IO58VDB1
K1	IO105NDB3
K2	GND
K3	IO104NPB3
K4	V_{CCI}B3
K5	IO101PPB3
K6	IO91RSB2
K7	IO81RSB2
K8	IO73RSB2
K9	IO77RSB2
K10	IO56NDB1
K11	V_{CCI}B1
K12	GDA1/IO60UPB1
K13	GND
K14	GDB1/IO59UDB1
L1	GEB1/IO99PDB3
L2	GEC1/IO100PDB3
L3	GEC0/IO100NDB3
L4	IO101NPB3

196-Pin CSP	
Pin Number	AGL250 Function
L5	IO89RSB2
L6	IO92RSB2
L7	IO75RSB2
L8	IO66RSB2
L9	IO65RSB2
L10	IO71RSB2
L11	V_{PUMP}
L12	V_{JTAG}
L13	GDA0/IO60VPB1
L14	GDB0/IO59VDB1
M1	GEB0/IO99NDB3
M2	GEA1/IO98PPB3
M3	GNDQ
M4	V_{CCI}B2
M5	IO88RSB2
M6	IO87RSB2
M7	IO82RSB2
M8	V_{CCI}B2
M9	IO67RSB2
M10	GDB2/IO62RSB2
M11	V_{CCI}B2
M12	VMV2
M13	TRST
M14	V_{CCI}B1
N1	GEA0/IO98NPB3
N2	VMV3
N3	GEC2/IO95RSB2
N4	IO94RSB2
N5	GND
N6	IO86RSB2
N7	IO78RSB2
N8	IO74RSB2
N9	IO69RSB2
N10	GND
N11	TCK
N12	TDI

196-Pin CSP	
Pin Number	AGL250 Function
N13	GNDQ
N14	TDO
P1	GND
P2	GEA2/IO97RSB2
P3	GEB2/IO96RSB2
P4	IO90RSB2
P5	IO85RSB2
P6	IO83RSB2
P7	IO79RSB2
P8	IO76RSB2
P9	IO72RSB2
P10	IO68RSB2
P11	GDC2/IO63RSB2
P12	GDA2/IO61RSB2
P13	TMS
P14	GND

281-Pin CSP



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

281-Pin CSP	
Pin Number	AGL600 Function
A1	GND
A2	GAB0/IO02RSB0
A3	GAC1/IO05RSB0
A4	IO07RSB0
A5	IO10RSB0
A6	IO14RSB0
A7	IO18RSB0
A8	IO21RSB0
A9	IO22RSB0
A10	V_{CCI}B0
A11	IO33RSB0
A12	IO40RSB0
A13	IO37RSB0
A14	IO48RSB0
A15	IO51RSB0
A16	IO53RSB0
A17	GBC1/IO55RSB0
A18	GBA0/IO58RSB0
A19	GND
B1	GAA2/IO174PPB3
B2	V_{CCI}B0
B3	GAB1/IO03RSB0
B4	GAC0/IO04RSB0
B5	IO06RSB0
B6	GND
B7	IO15RSB0
B8	IO20RSB0
B9	IO23RSB0
B10	IO24RSB0
B11	IO36RSB0
B12	IO35RSB0
B13	IO44RSB0
B14	GND
B15	IO52RSB0
B16	GBC0/IO54RSB0
B17	GBA1/IO59RSB0

281-Pin CSP	
Pin Number	AGL600 Function
B18	V_{CCI}B1
B19	IO61NDB1
C1	GAB2/IO173PPB3
C2	IO174NPB3
C6	IO12RSB0
C14	IO50RSB0
C18	IO60NPB1
C19	GBB2/IO61PDB1
D1	IO170PPB3
D2	IO172NPB3
D4	GAA0/IO00RSB0
D5	GAA1/IO01RSB0
D6	IO09RSB0
D7	IO16RSB0
D8	IO19RSB0
D9	IO26RSB0
D10	GND
D11	IO34RSB0
D12	IO45RSB0
D13	IO49RSB0
D14	IO47RSB0
D15	GBB0/IO56RSB0
D16	GBA2/IO60PPB1
D18	GBC2/IO62PPB1
D19	IO66NPB1
E1	IO169NPB3
E2	IO171PPB3
E4	IO171NPB3
E5	IO08RSB0
E6	IO11RSB0
E7	IO13RSB0
E8	IO17RSB0
E9	IO25RSB0
E10	IO30RSB0
E11	IO41RSB0
E12	IO42RSB0

281-Pin CSP	
Pin Number	AGL600 Function
E13	IO46RSB0
E14	GBB1/IO57RSB0
E15	IO62NPB1
E16	IO63PPB1
E18	IO64PPB1
E19	IO65NPB1
F1	IO168NPB3
F2	GND
F3	IO169PPB3
F4	IO170NPB3
F5	IO173NPB3
F15	IO63NPB1
F16	IO65PPB1
F17	IO64NPB1
F18	GND
F19	IO68PPB1
G1	IO167NPB3
G2	IO165NDB3
G4	IO168PPB3
G5	IO167PPB3
G7	GAC2/IO172PPB3
G8	VCCIB0
G9	IO28RSB0
G10	IO32RSB0
G11	IO43RSB0
G12	VCCIB0
G13	IO66PPB1
G15	IO67NDB1
G16	IO67PDB1
G18	GCC0/IO69NPB1
G19	GCB1/IO70PPB1
H1	GFB0/IO163NPB3
H2	IO165PDB3
H4	GFC1/IO164PPB3
H5	GFB1/IO163PPB3
H7	V_{CCI}B3

281-Pin CSP	
Pin Number	AGL600 Function
H8	V_{CC}
H9	V_{CCI}B0
H10	V_{CC}
H11	V_{CCI}B0
H12	V_{CC}
H13	V_{CCI}B1
H15	IO68NPB1
H16	GCB0/IO70NPB1
H18	GCA1/IO71PPB1
H19	GCA2/IO72PPB1
J1	V_{COMPLF}
J2	GFA0/IO162NDB3
J4	V_{CCPLF}
J5	GFC0/IO164NPB3
J7	GFA2/IO161PDB3
J8	V_{CCI}B3
J9	GND
J10	GND
J11	GND
J12	V_{CCI}B1
J13	GCC1/IO69PPB1
J15	GCA0/IO71NPB1
J16	GCB2/IO73PPB1
J18	IO72NPB1
J19	IO75PSB1
K1	V_{CCI}B3
K2	GFA1/IO162PDB3
K4	GND
K5	IO159NPB3
K7	IO161NDB3
K8	V_{CC}
K9	GND
K10	GND
K11	GND
K12	V_{CC}
K13	GCC2/IO74PPB1

281-Pin CSP	
Pin Number	AGL600 Function
K15	IO73NPB1
K16	GND
K18	IO74NPB1
K19	V_{CCI}B1
L1	GFB2/IO160PDB3
L2	IO160NDB3
L4	GFC2/IO159PPB3
L5	IO153PPB3
L7	IO153NPB3
L8	V_{CCI}B3
L9	GND
L10	GND
L11	GND
L12	V_{CCI}B1
L13	IO76PPB1
L15	IO76NPB1
L16	IO77PPB1
L18	IO78NPB1
L19	IO77NPB1
M1	IO158PDB3
M2	IO158NDB3
M4	IO154NPB3
M5	IO152PPB3
M7	V_{CCI}B3
M8	V_{CC}
M9	V_{CCI}B2
M10	V_{CC}
M11	V_{CCI}B2
M12	V_{CC}
M13	VCCIB1
M15	IO79NPB1
M16	IO81NPB1
M18	IO79PPB1
M19	IO78PPB1
N1	IO154PPB3
N2	IO152NPB3

281-Pin CSP	
Pin Number	AGL600 Function
N4	IO150PPB3
N5	IO148NPB3
N7	GEA2/IO143RSB2
N8	VCCIB2
N9	IO117RSB2
N10	IO115RSB2
N11	IO114RSB2
N12	VCCIB2
N13	V_{PUMP}
N15	IO82PPB1
N16	IO85PPB1
N18	IO82NPB1
N19	IO81PPB1
P1	IO151PDB3
P2	GND
P3	IO151NDB3
P4	IO149PPB3
P5	GEA0/IO144NPB3
P15	IO83NDB1
P16	IO83PDB1
P17	GDC1/IO86PPB1
P18	GND
P19	IO85NPB1
R1	IO150NPB3
R2	IO149NPB3
R4	GEC1/IO146PPB3
R5	GEB1/IO145PPB3
R6	IO138RSB2
R7	IO127RSB2
R8	IO123RSB2
R9	IO118RSB2
R10	IO111RSB2
R11	IO106RSB2
R12	IO103RSB2
R13	IO97RSB2
R14	IO95RSB2

281-Pin CSP	
Pin Number	AGL600 Function
R15	IO94RSB2
R16	GDA1/IO88PPB1
R18	GDB0/IO87NPB1
R19	GDC0/IO86NPB1
T1	IO148PPB3
T2	GEC0/IO146NPB3
T4	GEB0/IO145NPB3
T5	IO132RSB2
T6	IO136RSB2
T7	IO130RSB2
T8	IO126RSB2
T9	IO120RSB2
T10	GND
T11	IO113RSB2
T12	IO104RSB2
T13	IO101RSB2
T14	IO98RSB2
T15	GDC2/IO91RSB2
T16	TMS
T18	V_{JTAG}
T19	GDB1/IO87PPB1
U1	IO147PDB3
U2	GEA1/IO144PPB3
U6	IO131RSB2
U14	IO99RSB2
U18	TRST
U19	GDA0/IO88NPB1
V1	IO147NDB3
V2	V_{CCI}B3
V3	GEC2/IO141RSB2
V4	IO140RSB2
V5	IO135RSB2
V6	GND
V7	IO125RSB2
V8	IO122RSB2
V9	IO116RSB2

281-Pin CSP	
Pin Number	AGL600 Function
V10	IO112RSB2
V11	IO110RSB2
V12	IO108RSB2
V13	IO102RSB2
V14	GND
V15	IO93RSB2
V16	GDA2/IO89RSB2
V17	TDI
V18	V_{CCI}B2
V19	TDO
W1	GND
W2	FF/GEB2/IO142RSB2
W3	IO139RSB2
W4	IO137RSB2
W5	IO134RSB2
W6	IO133RSB2
W7	IO128RSB2
W8	IO124RSB2
W9	IO119RSB2
W10	V_{CCI}B2
W11	IO109RSB2
W12	IO107RSB2
W13	IO105RSB2
W14	IO100RSB2
W15	IO96RSB2
W16	IO92RSB2
W17	GDB2/IO90RSB2
W18	TCK
W19	GND

281-Pin CSP		281-Pin CSP		281-Pin CSP	
Pin Number	AGL1000 Function	Pin Number	AGL1000 Function	Pin Number	AGL1000 Function
A1	GND	B18	V_{CCI}B1	E13	IO53RSB0
A2	GAB0/IO02RSB0	B19	IO79NDB1	E14	GBB1/IO75RSB0
A3	GAC1/IO05RSB0	C1	GAB2/IO224PPB3	E15	IO80NPB1
A4	IO13RSB0	C2	IO225NPB3	E16	IO85PPB1
A5	IO11RSB0	C6	IO18RSB0	E18	IO83PPB1
A6	IO16RSB0	C14	IO63RSB0	E19	IO84NPB1
A7	IO20RSB0	C18	IO78NPB1	F1	IO214NPB3
A8	IO24RSB0	C19	GBB2/IO79PDB1	F2	GND
A9	IO29RSB0	D1	IO219PPB3	F3	IO217PPB3
A10	V_{CCI}B0	D2	IO223NPB3	F4	IO219NPB3
A11	IO39RSB0	D4	GAA0/IO00RSB0	F5	IO224NPB3
A12	IO45RSB0	D5	GAA1/IO01RSB0	F15	IO85NPB1
A13	IO48RSB0	D6	IO15RSB0	F16	IO84PPB1
A14	IO58RSB0	D7	IO19RSB0	F17	IO83NPB1
A15	IO61RSB0	D8	IO27RSB0	F18	GND
A16	IO62RSB0	D9	IO32RSB0	F19	IO90PPB1
A17	GBC1/IO73RSB0	D10	GND	G1	IO212NPB3
A18	GBA0/IO76RSB0	D11	IO38RSB0	G2	IO211NDB3
A19	GND	D12	IO44RSB0	G4	IO214PPB3
B1	GAA2/IO225PPB3	D13	IO47RSB0	G5	IO212PPB3
B2	V_{CCI}B0	D14	IO60RSB0	G7	GAC2/IO223PPB3
B3	GAB1/IO03RSB0	D15	GBB0/IO74RSB0	G8	V_{CCI}B0
B4	GAC0/IO04RSB0	D16	GBA2/IO78PPB1	G9	IO30RSB0
B5	IO12RSB0	D18	GBC2/IO80PPB1	G10	IO37RSB0
B6	GND	D19	IO88NPB1	G11	IO43RSB0
B7	IO21RSB0	E1	IO217NPB3	G12	V_{CCI}B0
B8	IO26RSB0	E2	IO221PPB3	G13	IO88PPB1
B9	IO34RSB0	E4	IO221NPB3	G15	IO89NDB1
B10	IO35RSB0	E5	IO10RSB0	G16	IO89PDB1
B11	IO36RSB0	E6	IO14RSB0	G18	GCC0/IO91NPB1
B12	IO46RSB0	E7	IO25RSB0	G19	GCB1/IO92PPB1
B13	IO52RSB0	E8	IO28RSB0	H1	GFB0/IO208NPB3
B14	GND	E9	IO31RSB0	H2	IO211PDB3
B15	IO59RSB0	E10	IO33RSB0	H4	GFC1/IO209PPB3
B16	GBC0/IO72RSB0	E11	IO42RSB0	H5	GFB1/IO208PPB3
B17	GBA1/IO77RSB0	E12	IO49RSB0	H7	V_{CCI}B3

281-Pin CSP	
Pin Number	AGL1000 Function
H8	V_{CC}
H9	V_{CCI}B0
H10	V_{CC}
H11	V_{CCI}B0
H12	V_{CC}
H13	V_{CCI}B1
H15	IO90NPB1
H16	GCB0/IO92NPB1
H18	GCA1/IO93PPB1
H19	GCA2/IO94PPB1
J1	V_{COMPLF}
J2	GFA0/IO207NDB3
J4	V_{CCPLF}
J5	GFC0/IO209NPB3
J7	GFA2/IO206PDB3
J8	V_{CCI}B3
J9	GND
J10	GND
J11	GND
J12	V_{CCI}B1
J13	GCC1/IO91PPB1
J15	GCA0/IO93NPB1
J16	GCB2/IO95PPB1
J18	IO94NPB1
J19	IO102PSB1
K1	V_{CCI}B3
K2	GFA1/IO207PDB3
K4	GND
K5	IO204NPB3
K7	IO206NDB3
K8	V_{CC}
K9	GND
K10	GND
K11	GND
K12	V_{CC}
K13	GCC2/IO96PPB1

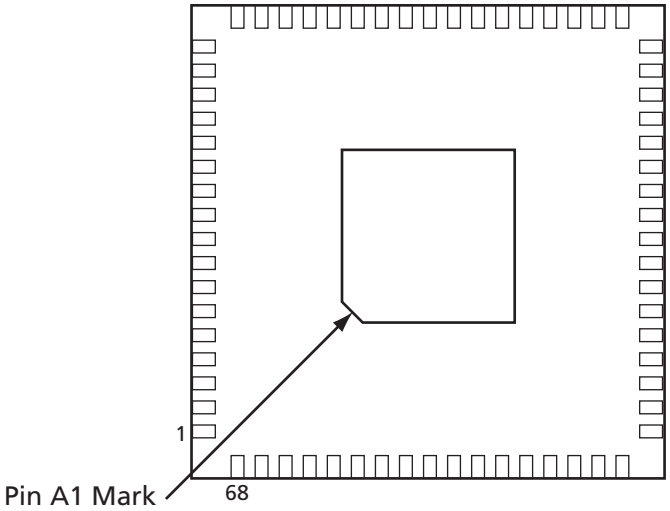
281-Pin CSP	
Pin Number	AGL1000 Function
K15	IO95NPB1
K16	GND
K18	IO96NPB1
K19	V_{CCI}B1
L1	GFB2/IO205PDB3
L2	IO205NDB3
L4	GFC2/IO204PPB3
L5	IO203PPB3
L7	IO203NPB3
L8	V_{CCI}B3
L9	GND
L10	GND
L11	GND
L12	V_{CCI}B1
L13	IO103PPB1
L15	IO103NPB1
L16	IO97PPB1
L18	IO98NPB1
L19	IO97NPB1
M1	IO202PDB3
M2	IO202NDB3
M4	IO201NPB3
M5	IO198PPB3
M7	V_{CCI}B3
M8	V_{CC}
M9	V_{CCI}B2
M10	V_{CC}
M11	V_{CCI}B2
M12	V_{CC}
M13	V_{CCI}B1
M15	IO104NPB1
M16	IO100NPB1
M18	IO104PPB1
M19	IO98PPB1
N1	IO201PPB3
N2	IO198NPB3

281-Pin CSP	
Pin Number	AGL1000 Function
N4	IO196PPB3
N5	IO197NPB3
N7	GEA2/IO187RSB2
N8	V_{CCI}B2
N9	IO155RSB2
N10	IO154RSB2
N11	IO150RSB2
N12	V_{CCI}B2
N13	V_{PUMP}
N15	IO107PPB1
N16	IO105PPB1
N18	IO107NPB1
N19	IO100PPB1
P1	IO195PDB3
P2	GND
P3	IO195NDB3
P4	IO194PPB3
P5	GEA0/IO188NPB3
P15	IO108NDB1
P16	IO108PDB1
P17	GDC1/IO111PPB1
P18	GND
P19	IO105NPB1
R1	IO196NPB3
R2	IO194NPB3
R4	GEC1/IO190PPB3
R5	GEB1/IO189PPB3
R6	IO184RSB2
R7	IO173RSB2
R8	IO168RSB2
R9	IO160RSB2
R10	IO151RSB2
R11	IO141RSB2
R12	IO136RSB2
R13	IO127RSB2
R14	IO124RSB2

281-Pin CSP	
Pin Number	AGL1000 Function
R15	IO122RSB2
R16	GDA1/IO113PPB1
R18	GDB0/IO112NPB1
R19	GDC0/IO111NPB1
T1	IO197PPB3
T2	GEC0/IO190NPB3
T4	GEB0/IO189NPB3
T5	IO181RSB2
T6	IO172RSB2
T7	IO171RSB2
T8	IO156RSB2
T9	IO159RSB2
T10	GND
T11	IO139RSB2
T12	IO138RSB2
T13	IO129RSB2
T14	IO123RSB2
T15	GDC2/IO116RSB2
T16	TMS
T18	V_{JTAG}
T19	GDB1/IO112PPB1
U1	IO193PDB3
U2	GEA1/IO188PPB3
U6	IO167RSB2
U14	IO128RSB2
U18	TRST
U19	GDA0/IO113NPB1
V1	IO193NDB3
V2	V_{CCI}B3
V3	GEC2/IO185RSB2
V4	IO182RSB2
V5	IO175RSB2
V6	GND
V7	IO161RSB2
V8	IO143RSB2
V9	IO146RSB2

281-Pin CSP	
Pin Number	AGL1000 Function
V10	IO145RSB2
V11	IO144RSB2
V12	IO134RSB2
V13	IO133RSB2
V14	GND
V15	IO119RSB2
V16	GDA2/IO114RSB2
V17	TDI
V18	V_{CCI}B2
V19	TDO
W1	GND
W2	FF/GEB2/IO186RSB2
W3	IO183RSB2
W4	IO176RSB2
W5	IO170RSB2
W6	IO162RSB2
W7	IO157RSB2
W8	IO152RSB2
W9	IO149RSB2
W10	V_{CCI}B2
W11	IO140RSB2
W12	IO135RSB2
W13	IO130RSB2
W14	IO125RSB2
W15	IO120RSB2
W16	IO118RSB2
W17	GDB2/IO115RSB2
W18	TCK
W19	GND

68-Pin QFN



Notes:

1. *This is the bottom view of the package.*
2. *The die attach paddle center of the package is tied to ground (GND).*

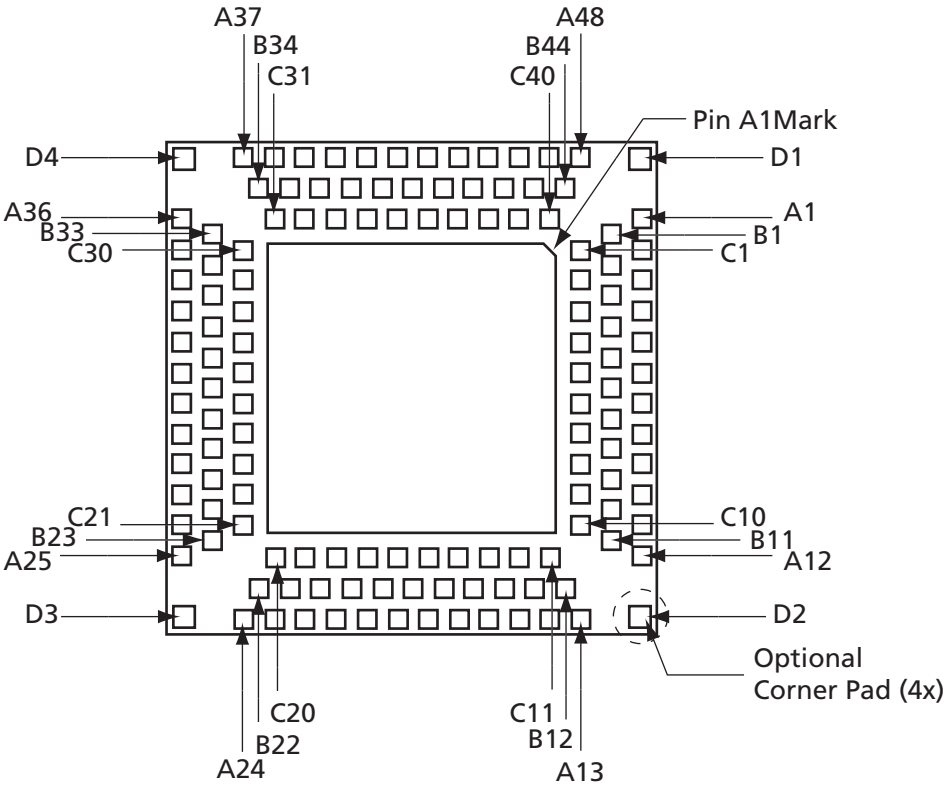
Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

68-Pin QFN	
Pin Number	AGL015 Function
1	IO82RSB1
2	IO80RSB1
3	IO78RSB1
4	IO76RSB1
5	GEC0/IO73RSB1
6	GEA0/IO72RSB1
7	GEB0/IO71RSB1
8	V_{CC}
9	GND
10	V_{CCI}B1
11	IO68RSB1
12	IO67RSB1
13	IO66RSB1
14	IO65RSB1
15	IO64RSB1
16	IO63RSB1
17	IO62RSB1
18	FF/IO60RSB1
19	IO58RSB1
20	IO56RSB1
21	IO54RSB1
22	IO52RSB1
23	IO51RSB1
24	V_{CC}
25	GND
26	V_{CCI}B1
27	IO50RSB1
28	IO48RSB1
29	IO46RSB1
30	IO44RSB1
31	IO42RSB1
32	TCK
33	TDI
34	TMS
35	V_{PUMP}
36	TDO

68-Pin QFN	
Pin Number	AGL015 Function
37	TRST
38	V_{JTAG}
39	IO40RSB0
40	IO37RSB0
41	GDB0/IO34RSB0
42	GDA0/IO33RSB0
43	GDC0/IO32RSB0
44	V_{CCI}B0
45	GND
46	V_{CC}
47	IO31RSB0
48	IO29RSB0
49	IO28RSB0
50	IO27RSB0
51	IO25RSB0
52	IO24RSB0
53	IO22RSB0
54	IO21RSB0
55	IO19RSB0
56	IO17RSB0
57	IO15RSB0
58	IO14RSB0
59	V_{CCI}B0
60	GND
61	V_{CC}
62	IO12RSB0
63	IO10RSB0
64	IO08RSB0
65	IO06RSB0
66	IO04RSB0
67	IO02RSB0
68	IO00RSB0

132-Pin QFN



Notes:

1. *This is the bottom view of the package.*
2. *The die attach paddle center of the package is tied to ground (GND).*

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

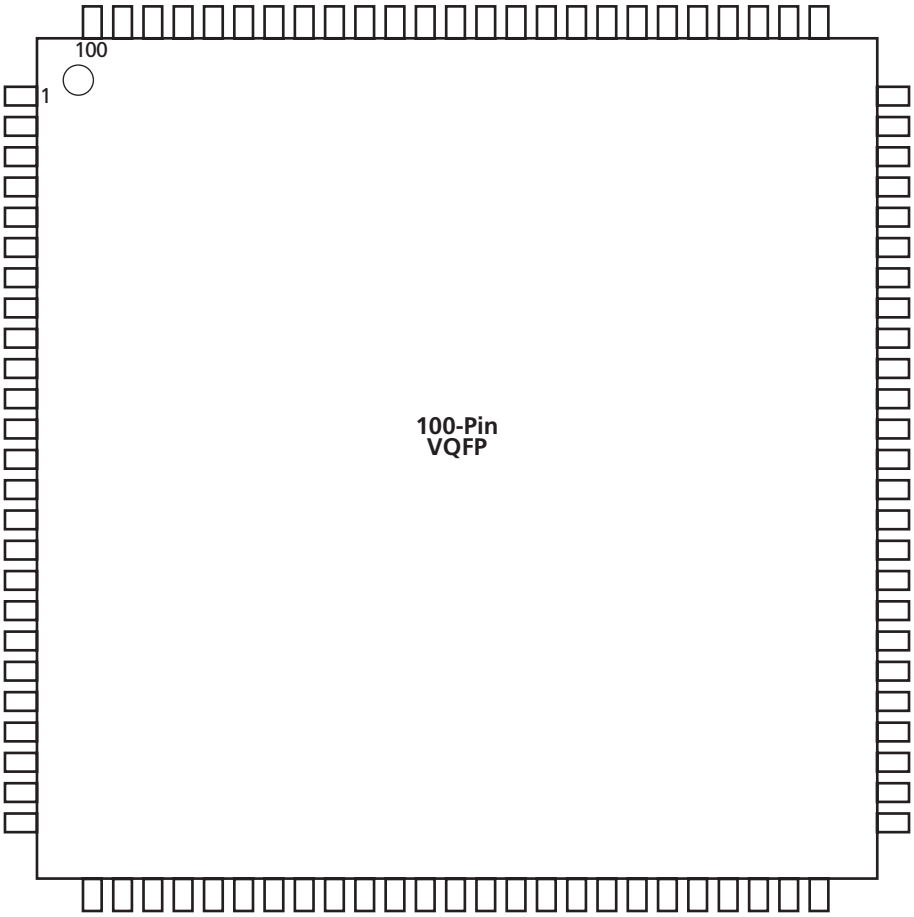
132-Pin QFN		132-Pin QFN		132-Pin QFN	
Pin Number	AGL030 Function	Pin Number	AGL030 Function	Pin Number	AGL030 Function
A1	IO80RSB1	A37	IO22RSB0	B25	GND
A2	IO77RSB1	A38	IO19RSB0	B26	NC
A3	NC	A39	NC	B27	IO37RSB0
A4	IO76RSB1	A40	IO18RSB0	B28	GND
A5	GEC0/IO73RSB1	A41	IO16RSB0	B29	GDA0/IO33RSB0
A6	NC	A42	IO14RSB0	B30	NC
A7	GEB0/IO71RSB1	A43	V_{CC}	B31	GND
A8	IO69RSB1	A44	IO11RSB0	B32	IO29RSB0
A9	NC	A45	IO08RSB0	B33	IO26RSB0
A10	V_{CC}	A46	IO06RSB0	B34	IO23RSB0
A11	IO67RSB1	A47	IO05RSB0	B35	IO20RSB0
A12	IO64RSB1	A48	IO02RSB0	B36	GND
A13	IO59RSB1	B1	IO81RSB1	B37	IO17RSB0
A14	IO56RSB1	B2	IO78RSB1	B38	IO15RSB0
A15	NC	B3	GND	B39	GND
A16	IO55RSB1	B4	IO75RSB1	B40	IO12RSB0
A17	IO53RSB1	B5	NC	B41	IO09RSB0
A18	V_{CC}	B6	GND	B42	GND
A19	IO50RSB1	B7	IO70RSB1	B43	IO04RSB0
A20	IO48RSB1	B8	NC	B44	IO01RSB0
A21	IO45RSB1	B9	GND	C1	IO82RSB1
A22	IO44RSB1	B10	IO66RSB1	C2	IO79RSB1
A23	IO43RSB1	B11	IO63RSB1	C3	NC
A24	TDI	B12	FF/IO60RSB1	C4	IO74RSB1
A25	TRST	B13	IO57RSB1	C5	GEA0/IO72RSB1
A26	IO40RSB0	B14	GND	C6	NC
A27	NC	B15	IO54RSB1	C7	NC
A28	IO39RSB0	B16	IO52RSB1	C8	V_{CCI}B1
A29	IO38RSB0	B17	GND	C9	IO65RSB1
A30	IO36RSB0	B18	IO49RSB1	C10	IO62RSB1
A31	IO35RSB0	B19	IO46RSB1	C11	IO61RSB1
A32	GDC0/IO32RSB0	B20	GND	C12	IO58RSB1
A33	NC	B21	IO42RSB1	C13	NC
A34	V_{CC}	B22	TMS	C14	NC
A35	IO30RSB0	B23	TDO	C15	IO51RSB1
A36	IO27RSB0	B24	IO41RSB0	C16	V_{CCI}B1

132-Pin QFN	
Pin Number	**AGL030 Function**
C17	IO47RSB1
C18	NC
C19	TCK
C20	NC
C21	V_{PUMP}
C22	V_{JTAG}
C23	NC
C24	NC
C25	NC
C26	GDB0/IO34RSB0
C27	NC
C28	V_{CCI}B0
C29	IO28RSB0
C30	IO25RSB0
C31	IO24RSB0
C32	IO21RSB0
C33	NC
C34	NC
C35	V_{CCI}B0
C36	IO13RSB0
C37	IO10RSB0
C38	IO07RSB0
C39	IO03RSB0
C40	IO00RSB0
D1	GND
D2	GND
D3	GND
D4	GND

132-Pin QFN		132-Pin QFN		132-Pin QFN	
Pin Number	AGL125 Function	Pin Number	AGL125 Function	Pin Number	AGL125 Function
A1	GAB2/IO69RSB1	A37	GBB1/IO38RSB0	B25	GND
A2	IO130RSB1	A38	GBC0/IO35RSB0	B26	NC
A3	V_{CCI}B1	A39	V_{CCI}B0	B27	GCB2/IO58RSB0
A4	GFC1/IO126RSB1	A40	IO28RSB0	B28	GND
A5	GFB0/IO123RSB1	A41	IO22RSB0	B29	GCB0/IO54RSB0
A6	V_{CCPLF}	A42	IO18RSB0	B30	GCC1/IO51RSB0
A7	GFA1/IO121RSB1	A43	IO14RSB0	B31	GND
A8	GFC2/IO118RSB1	A44	IO11RSB0	B32	GBB2/IO43RSB0
A9	IO115RSB1	A45	IO07RSB0	B33	VMV0
A10	V_{CC}	A46	V_{CC}	B34	GBA0/IO39RSB0
A11	GEB1/IO110RSB1	A47	GAC1/IO05RSB0	B35	GBC1/IO36RSB0
A12	GEA0/IO107RSB1	A48	GAB0/IO02RSB0	B36	GND
A13	GEC2/IO104RSB1	B1	IO68RSB1	B37	IO26RSB0
A14	IO100RSB1	B2	GAC2/IO131RSB1	B38	IO21RSB0
A15	V_{CC}	B3	GND	B39	GND
A16	IO99RSB1	B4	GFC0/IO125RSB1	B40	IO13RSB0
A17	IO96RSB1	B5	V_{COMPLF}	B41	IO08RSB0
A18	IO94RSB1	B6	GND	B42	GND
A19	IO91RSB1	B7	GFB2/IO119RSB1	B43	GAC0/IO04RSB0
A20	IO85RSB1	B8	IO116RSB1	B44	GNDQ
A21	IO79RSB1	B9	GND	C1	GAA2/IO67RSB1
A22	V_{CC}	B10	GEB0/IO109RSB1	C2	IO132RSB1
A23	GDB2/IO71RSB1	B11	VMV1	C3	V_{CC}
A24	TDI	B12	FF/GEB2/IO105RSB1	C4	GFB1/IO124RSB1
A25	TRST	B13	IO101RSB1	C5	GFA0/IO122RSB1
A26	GDC1/IO61RSB0	B14	GND	C6	GFA2/IO120RSB1
A27	V_{CC}	B15	IO98RSB1	C7	IO117RSB1
A28	IO60RSB0	B16	IO95RSB1	C8	V_{CCI}B1
A29	GCC2/IO59RSB0	B17	GND	C9	GEA1/IO108RSB1
A30	GCA2/IO57RSB0	B18	IO87RSB1	C10	GNDQ
A31	GCA0/IO56RSB0	B19	IO81RSB1	C11	GEA2/IO106RSB1
A32	GCB1/IO53RSB0	B20	GND	C12	IO103RSB1
A33	IO49RSB0	B21	GNDQ	C13	V_{CCI}B1
A34	V_{CC}	B22	TMS	C14	IO97RSB1
A35	IO44RSB0	B23	TDO	C15	IO93RSB1
A36	GBA2/IO41RSB0	B24	GDC0/IO62RSB0	C16	IO89RSB1

132-Pin QFN	
Pin Number	**AGL125 Function**
C17	IO83RSB1
C18	V_{CCI}B1
C19	TCK
C20	VMV1
C21	V_{PUMP}
C22	V_{JTAG}
C23	V_{CCI}B0
C24	NC
C25	NC
C26	GCA1/IO55RSB0
C27	GCC0/IO52RSB0
C28	V_{CCI}B0
C29	IO42RSB0
C30	GNDQ
C31	GBA1/IO40RSB0
C32	GBB0/IO37RSB0
C33	V_{CC}
C34	IO24RSB0
C35	IO19RSB0
C36	IO16RSB0
C37	IO10RSB0
C38	V_{CCI}B0
C39	GAB1/IO03RSB0
C40	VMV0
D1	GND
D2	GND
D3	GND
D4	GND

100-Pin VQFP



Note: This is the top view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

100-Pin VQFP	
Pin Number	AGL030 Function
1	GND
2	IO82RSB1
3	IO81RSB1
4	IO80RSB1
5	IO79RSB1
6	IO78RSB1
7	IO77RSB1
8	IO76RSB1
9	GND
10	IO75RSB1
11	IO74RSB1
12	GEC0/IO73RSB1
13	GEA0/IO72RSB1
14	GEB0/IO71RSB1
15	IO70RSB1
16	IO69RSB1
17	V_{CC}
18	V_{CCI}B1
19	IO68RSB1
20	IO67RSB1
21	IO66RSB1
22	IO65RSB1
23	IO64RSB1
24	IO63RSB1
25	IO62RSB1
26	IO61RSB1
27	FF/IO60RSB1
28	IO59RSB1
29	IO58RSB1
30	IO57RSB1
31	IO56RSB1
32	IO55RSB1
33	IO54RSB1
34	IO53RSB1
35	IO52RSB1
36	IO51RSB1

100-Pin VQFP	
Pin Number	AGL030 Function
37	V_{CC}
38	GND
39	V_{CCI}B1
40	IO49RSB1
41	IO47RSB1
42	IO46RSB1
43	IO45RSB1
44	IO44RSB1
45	IO43RSB1
46	IO42RSB1
47	TCK
48	TDI
49	TMS
50	NC
51	GND
52	V_{PUMP}
53	NC
54	TDO
55	TRST
56	V_{JTAG}
57	IO41RSB0
58	IO40RSB0
59	IO39RSB0
60	IO38RSB0
61	IO37RSB0
62	IO36RSB0
63	GDB0/IO34RSB0
64	GDA0/IO33RSB0
65	GDC0/IO32RSB0
66	V_{CCI}B0
67	GND
68	V_{CC}
69	IO31RSB0
70	IO30RSB0
71	IO29RSB0
72	IO28RSB0

100-Pin VQFP	
Pin Number	AGL030 Function
73	IO27RSB0
74	IO26RSB0
75	IO25RSB0
76	IO24RSB0
77	IO23RSB0
78	IO22RSB0
79	IO21RSB0
80	IO20RSB0
81	IO19RSB0
82	IO18RSB0
83	IO17RSB0
84	IO16RSB0
85	IO15RSB0
86	IO14RSB0
87	V_{CCI}B0
88	GND
89	V_{CC}
90	IO12RSB0
91	IO10RSB0
92	IO08RSB0
93	IO07RSB0
94	IO06RSB0
95	IO05RSB0
96	IO04RSB0
97	IO03RSB0
98	IO02RSB0
99	IO01RSB0
100	IO00RSB0

100-Pin VQFP	
Pin Number	AGL060 Function
1	GND
2	GAA2/IO51RSB1
3	IO52RSB1
4	GAB2/IO53RSB1
5	IO95RSB1
6	GAC2/IO94RSB1
7	IO93RSB1
8	IO92RSB1
9	GND
10	GFB1/IO87RSB1
11	GFB0/IO86RSB1
12	V_{COMPLF}
13	GFA0/IO85RSB1
14	V_{CCPLF}
15	GFA1/IO84RSB1
16	GFA2/IO83RSB1
17	V_{CC}
18	V_{CCI}B1
19	GEC1/IO77RSB1
20	GEB1/IO75RSB1
21	GEB0/IO74RSB1
22	GEA1/IO73RSB1
23	GEA0/IO72RSB1
24	VMV1
25	GNDQ
26	GEA2/IO71RSB1
27	FF/GEB2/IO70RSB1
28	GEC2/IO69RSB1
29	IO68RSB1
30	IO67RSB1
31	IO66RSB1
32	IO65RSB1
33	IO64RSB1
34	IO63RSB1
35	IO62RSB1
36	IO61RSB1

100-Pin VQFP	
Pin Number	AGL060 Function
37	V_{CC}
38	GND
39	V_{CCI}B1
40	IO60RSB1
41	IO59RSB1
42	IO58RSB1
43	IO57RSB1
44	GDC2/IO56RSB1
45	GDB2/IO55RSB1
46	GDA2/IO54RSB1
47	TCK
48	TDI
49	TMS
50	VMV1
51	GND
52	V_{PUMP}
53	NC
54	TDO
55	TRST
56	V_{JTAG}
57	GDA1/IO49RSB0
58	GDC0/IO46RSB0
59	GDC1/IO45RSB0
60	GCC2/IO43RSB0
61	GCB2/IO42RSB0
62	GCA0/IO40RSB0
63	GCA1/IO39RSB0
64	GCC0/IO36RSB0
65	GCC1/IO35RSB0
66	V_{CCI}B0
67	GND
68	V_{CC}
69	IO31RSB0
70	GBC2/IO29RSB0
71	GBB2/IO27RSB0
72	IO26RSB0

100-Pin VQFP	
Pin Number	AGL060 Function
73	GBA2/IO25RSB0
74	VMV0
75	GNDQ
76	GBA1/IO24RSB0
77	GBA0/IO23RSB0
78	GBB1/IO22RSB0
79	GBB0/IO21RSB0
80	GBC1/IO20RSB0
81	GBC0/IO19RSB0
82	IO18RSB0
83	IO17RSB0
84	IO15RSB0
85	IO13RSB0
86	IO11RSB0
87	V_{CCI}B0
88	GND
89	V_{CC}
90	IO10RSB0
91	IO09RSB0
92	IO08RSB0
93	GAC1/IO07RSB0
94	GAC0/IO06RSB0
95	GAB1/IO05RSB0
96	GAB0/IO04RSB0
97	GAA1/IO03RSB0
98	GAA0/IO02RSB0
99	IO01RSB0
100	IO00RSB0

100-Pin VQFP	
Pin Number	AGL125 Function
1	GND
2	GAA2/IO67RSB1
3	IO68RSB1
4	GAB2/IO69RSB1
5	IO132RSB1
6	GAC2/IO131RSB1
7	IO130RSB1
8	IO129RSB1
9	GND
10	GFB1/IO124RSB1
11	GFB0/IO123RSB1
12	V_{COMPLF}
13	GFA0/IO122RSB1
14	V_{CCPLF}
15	GFA1/IO121RSB1
16	GFA2/IO120RSB1
17	V_{CC}
18	V_{CCI}B1
19	GEC0/IO111RSB1
20	GEB1/IO110RSB1
21	GEB0/IO109RSB1
22	GEA1/IO108RSB1
23	GEA0/IO107RSB1
24	VMV1
25	GNDQ
26	GEA2/IO106RSB1
27	FF/GEB2/IO105RSB1
28	GEC2/IO104RSB1
29	IO102RSB1
30	IO100RSB1
31	IO99RSB1
32	IO97RSB1
33	IO96RSB1
34	IO95RSB1
35	IO94RSB1
36	IO93RSB1

100-Pin VQFP	
Pin Number	AGL125 Function
37	V_{CC}
38	GND
39	V_{CCI}B1
40	IO87RSB1
41	IO84RSB1
42	IO81RSB1
43	IO75RSB1
44	GDC2/IO72RSB1
45	GDB2/IO71RSB1
46	GDA2/IO70RSB1
47	TCK
48	TDI
49	TMS
50	VMV1
51	GND
52	V_{PUMP}
53	NC
54	TDO
55	TRST
56	V_{JTAG}
57	GDA1/IO65RSB0
58	GDC0/IO62RSB0
59	GDC1/IO61RSB0
60	GCC2/IO59RSB0
61	GCB2/IO58RSB0
62	GCA0/IO56RSB0
63	GCA1/IO55RSB0
64	GCC0/IO52RSB0
65	GCC1/IO51RSB0
66	V_{CCI}B0
67	GND
68	V_{CC}
69	IO47RSB0
70	GBC2/IO45RSB0
71	GBB2/IO43RSB0
72	IO42RSB0

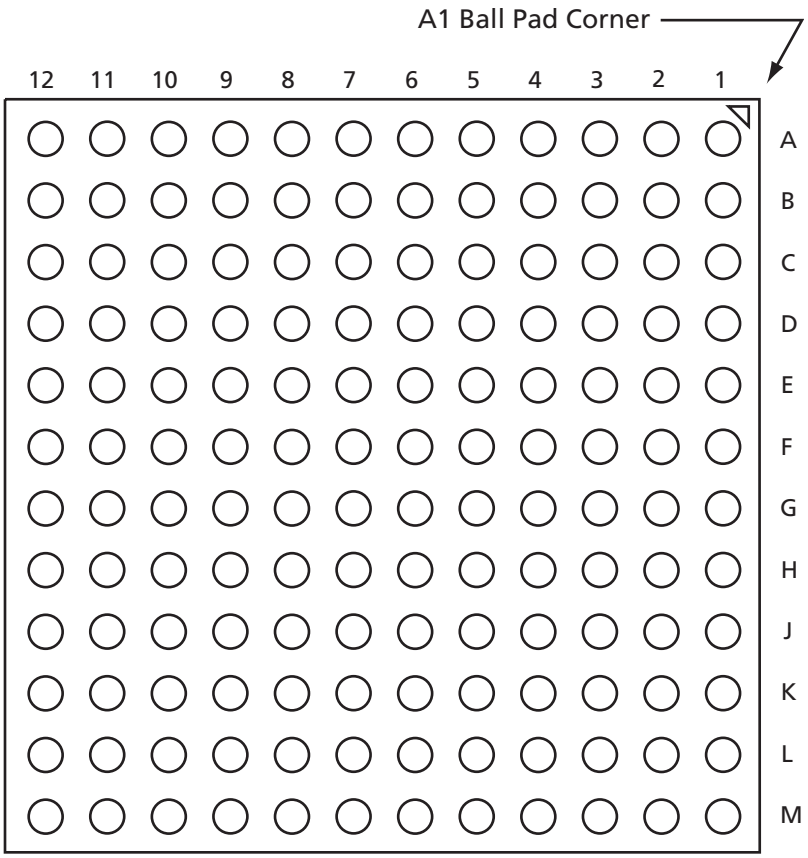
100-Pin VQFP	
Pin Number	AGL125 Function
73	GBA2/IO41RSB0
74	VMV0
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO32RSB0
83	IO28RSB0
84	IO25RSB0
85	IO22RSB0
86	IO19RSB0
87	V_{CCI}B0
88	GND
89	V_{CC}
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	IO09RSB0
94	IO07RSB0
95	GAC1/IO05RSB0
96	GAC0/IO04RSB0
97	GAB1/IO03RSB0
98	GAB0/IO02RSB0
99	GAA1/IO01RSB0
100	GAA0/IO00RSB0

100-Pin VQFP	
Pin Number	AGL250 Function
1	GND
2	GAA2/IO118UDB3
3	IO118VDB3
4	GAB2/IO117UDB3
5	IO117VDB3
6	GAC2/IO116UDB3
7	IO116VDB3
8	IO112PSB3
9	GND
10	GFB1/IO109PDB3
11	GFB0/IO109NDB3
12	V_{COMPLF}
13	GFA0/IO108NPB3
14	V_{CCPLF}
15	GFA1/IO108PPB3
16	GFA2/IO107PSB3
17	V_{CC}
18	V_{CCI}B3
19	GFC2/IO105PSB3
20	GEC1/IO100PDB3
21	GEC0/IO100NDB3
22	GEA1/IO98PDB3
23	GEA0/IO98NDB3
24	VMV3
25	GNDQ
26	GEA2/IO97RSB2
27	FF/GEB2/IO96RSB2
28	GEC2/IO95RSB2
29	IO93RSB2
30	IO92RSB2
31	IO91RSB2
32	IO90RSB2
33	IO88RSB2
34	IO86RSB2
35	IO85RSB2
36	IO84RSB2

100-Pin VQFP	
Pin Number	AGL250 Function
37	V_{CC}
38	GND
39	V_{CCI}B2
40	IO77RSB2
41	IO74RSB2
42	IO71RSB2
43	GDC2/IO63RSB2
44	GDB2/IO62RSB2
45	GDA2/IO61RSB2
46	GNDQ
47	TCK
48	TDI
49	TMS
50	VMV2
51	GND
52	V_{PUMP}
53	NC
54	TDO
55	TRST
56	V_{JTAG}
57	GDA1/IO60USB1
58	GDC0/IO58VDB1
59	GDC1/IO58UDB1
60	IO52NDB1
61	GCB2/IO52PDB1
62	GCA1/IO50PDB1
63	GCA0/IO50NDB1
64	GCC0/IO48NDB1
65	GCC1/IO48PDB1
66	V_{CCI}B1
67	GND
68	V_{CC}
69	IO43NDB1
70	GBC2/IO43PDB1
71	GBB2/IO42PSB1
72	IO41NDB1

100-Pin VQFP	
Pin Number	AGL250 Function
73	GBA2/IO41PDB1
74	VMV1
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO29RSB0
83	IO27RSB0
84	IO25RSB0
85	IO23RSB0
86	IO21RSB0
87	V_{CCI}B0
88	GND
89	V_{CC}
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	GAC1/IO05RSB0
94	GAC0/IO04RSB0
95	GAB1/IO03RSB0
96	GAB0/IO02RSB0
97	GAA1/IO01RSB0
98	GAA0/IO00RSB0
99	GNDQ
100	VMV0

144-Pin FBGA



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

144-Pin FBGA	
Pin Number	AGL125 Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO11RSB0
A6	GND
A7	IO18RSB0
A8	V_{CC}
A9	IO25RSB0
A10	GBA0/IO39RSB0
A11	GBA1/IO40RSB0
A12	GNDQ
B1	GAB2/IO69RSB1
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO08RSB0
B6	IO14RSB0
B7	IO19RSB0
B8	IO22RSB0
B9	GBB0/IO37RSB0
B10	GBB1/IO38RSB0
B11	GND
B12	VMV0
C1	IO132RSB1
C2	GFA2/IO120RSB1
C3	GAC2/IO131RSB1
C4	V_{CC}
C5	IO10RSB0
C6	IO12RSB0
C7	IO21RSB0
C8	IO24RSB0
C9	IO27RSB0
C10	GBA2/IO41RSB0
C11	IO42RSB0
C12	GBC2/IO45RSB0

144-Pin FBGA	
Pin Number	AGL125 Function
D1	IO128RSB1
D2	IO129RSB1
D3	IO130RSB1
D4	GAA2/IO67RSB1
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO35RSB0
D8	GBC1/IO36RSB0
D9	GBB2/IO43RSB0
D10	IO28RSB0
D11	IO44RSB0
D12	GCB1/IO53RSB0
E1	V_{CC}
E2	GFC0/IO125RSB1
E3	GFC1/IO126RSB1
E4	V_{CCI}B1
E5	IO68RSB1
E6	V_{CCI}B0
E7	V_{CCI}B0
E8	GCC1/IO51RSB0
E9	V_{CCI}B0
E10	V_{CC}
E11	GCA0/IO56RSB0
E12	IO46RSB0
F1	GFB0/IO123RSB1
F2	V_{COMPLF}
F3	GFB1/IO124RSB1
F4	IO127RSB1
F5	GND
F6	GND
F7	GND
F8	GCC0/IO52RSB0
F9	GCB0/IO54RSB0
F10	GND
F11	GCA1/IO55RSB0
F12	GCA2/IO57RSB0

144-Pin FBGA	
Pin Number	AGL125 Function
G1	GFA1/IO121RSB1
G2	GND
G3	V_{CCPLF}
G4	GFA0/IO122RSB1
G5	GND
G6	GND
G7	GND
G8	GDC1/IO61RSB0
G9	IO48RSB0
G10	GCC2/IO59RSB0
G11	IO47RSB0
G12	GCB2/IO58RSB0
H1	V_{CC}
H2	GFB2/IO119RSB1
H3	GFC2/IO118RSB1
H4	GEC1/IO112RSB1
H5	V_{CC}
H6	IO50RSB0
H7	IO60RSB0
H8	GDB2/IO71RSB1
H9	GDC0/IO62RSB0
H10	V_{CCI}B0
H11	IO49RSB0
H12	V_{CC}
J1	GEB1/IO110RSB1
J2	IO115RSB1
J3	V_{CCI}B1
J4	GEC0/IO111RSB1
J5	IO116RSB1
J6	IO117RSB1
J7	V_{CC}
J8	TCK
J9	GDA2/IO70RSB1
J10	TDO
J11	GDA1/IO65RSB0
J12	GDB1/IO63RSB0

144-Pin FBGA	
Pin Number	**AGL125 Function**
K1	GEB0/IO109RSB1
K2	GEA1/IO108RSB1
K3	GEA0/IO107RSB1
K4	GEA2/IO106RSB1
K5	IO100RSB1
K6	IO98RSB1
K7	GND
K8	IO73RSB1
K9	GDC2/IO72RSB1
K10	GND
K11	GDA0/IO66RSB0
K12	GDB0/IO64RSB0
L1	GND
L2	VMV1
L3	FF/GEB2/IO105RSB1
L4	IO102RSB1
L5	V_{CCI}B1
L6	IO95RSB1
L7	IO85RSB1
L8	IO74RSB1
L9	TMS
L10	V_{JTAG}
L11	VMV1
L12	TRST
M1	GNDQ
M2	GEC2/IO104RSB1
M3	IO103RSB1
M4	IO101RSB1
M5	IO97RSB1
M6	IO94RSB1
M7	IO86RSB1
M8	IO75RSB1
M9	TDI
M10	V_{CCI}B1
M11	V_{PUMP}
M12	GNDQ

144-Pin FBGA	
Pin Number	AGL250 Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO16RSB0
A6	GND
A7	IO29RSB0
A8	V_{CC}
A9	IO33RSB0
A10	GBA0/IO39RSB0
A11	GBA1/IO40RSB0
A12	GNDQ
B1	GAB2/IO117UDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO14RSB0
B6	IO19RSB0
B7	IO22RSB0
B8	IO30RSB0
B9	GBB0/IO37RSB0
B10	GBB1/IO38RSB0
B11	GND
B12	VMV1
C1	IO117VDB3
C2	GFA2/IO107PPB3
C3	GAC2/IO116UDB3
C4	V_{CC}
C5	IO12RSB0
C6	IO17RSB0
C7	IO24RSB0
C8	IO31RSB0
C9	IO34RSB0
C10	GBA2/IO41PDB1
C11	IO41NDB1
C12	GBC2/IO43PPB1

144-Pin FBGA	
Pin Number	AGL250 Function
D1	IO112NDB3
D2	IO112PDB3
D3	IO116VDB3
D4	GAA2/IO118UPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO35RSB0
D8	GBC1/IO36RSB0
D9	GBB2/IO42PDB1
D10	IO42NDB1
D11	IO43NPB1
D12	GCB1/IO49PPB1
E1	V_{CC}
E2	GFC0/IO110NDB3
E3	GFC1/IO110PDB3
E4	V_{CCI}B3
E5	IO118VPB3
E6	V_{CCI}B0
E7	V_{CCI}B0
E8	GCC1/IO48PDB1
E9	V_{CCI}B1
E10	V_{CC}
E11	GCA0/IO50NDB1
E12	IO51NDB1
F1	GFB0/IO109NPB3
F2	V_{COMPLF}
F3	GFB1/IO109PPB3
F4	IO107NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO48NDB1
F9	GCB0/IO49NPB1
F10	GND
F11	GCA1/IO50PDB1
F12	GCA2/IO51PDB1

144-Pin FBGA	
Pin Number	AGL250 Function
G1	GFA1/IO108PPB3
G2	GND
G3	V_{CCPLF}
G4	GFA0/IO108NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO58UPB1
G9	IO53NDB1
G10	GCC2/IO53PDB1
G11	IO52NDB1
G12	GCB2/IO52PDB1
H1	V_{CC}
H2	GFB2/IO106PDB3
H3	GFC2/IO105PSB3
H4	GEC1/IO100PDB3
H5	V_{CC}
H6	IO79RSB2
H7	IO65RSB2
H8	GDB2/IO62RSB2
H9	GDC0/IO58VPB1
H10	V_{CCI}B1
H11	IO54PSB1
H12	V_{CC}
J1	GEB1/IO99PDB3
J2	IO106NDB3
J3	V_{CCI}B3
J4	GEC0/IO100NDB3
J5	IO88RSB2
J6	IO81RSB2
J7	V_{CC}
J8	TCK
J9	GDA2/IO61RSB2
J10	TDO
J11	GDA1/IO60UDB1
J12	GDB1/IO59UDB1

144-Pin FBGA	
Pin Number	**AGL250 Function**
K1	GEB0/IO99NDB3
K2	GEA1/IO98PDB3
K3	GEA0/IO98NDB3
K4	GEA2/IO97RSB2
K5	IO90RSB2
K6	IO84RSB2
K7	GND
K8	IO66RSB2
K9	GDC2/IO63RSB2
K10	GND
K11	GDA0/IO60VDB1
K12	GDB0/IO59VDB1
L1	GND
L2	VMV3
L3	FF/GEB2/IO96RSB2
L4	IO91RSB2
L5	V_{CCI}B2
L6	IO82RSB2
L7	IO80RSB2
L8	IO72RSB2
L9	TMS
L10	V_{JTAG}
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO95RSB2
M3	IO92RSB2
M4	IO89RSB2
M5	IO87RSB2
M6	IO85RSB2
M7	IO78RSB2
M8	IO76RSB2
M9	TDI
M10	V_{CCI}B2
M11	V_{PUMP}
M12	GNDQ

144-Pin FBGA	
Pin Number	AGL600 Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO10RSB0
A6	GND
A7	IO34RSB0
A8	V_{CC}
A9	IO50RSB0
A10	GBA0/IO58RSB0
A11	GBA1/IO59RSB0
A12	GNDQ
B1	GAB2/IO173PDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO13RSB0
B6	IO19RSB0
B7	IO31RSB0
B8	IO39RSB0
B9	GBB0/IO56RSB0
B10	GBB1/IO57RSB0
B11	GND
B12	VMV1
C1	IO173NDB3
C2	GFA2/IO161PPB3
C3	GAC2/IO172PDB3
C4	V_{CC}
C5	IO16RSB0
C6	IO25RSB0
C7	IO28RSB0
C8	IO42RSB0
C9	IO45RSB0
C10	GBA2/IO60PDB1
C11	IO60NDB1
C12	GBC2/IO62PPB1

144-Pin FBGA	
Pin Number	AGL600 Function
D1	IO169PDB3
D2	IO169NDB3
D3	IO172NDB3
D4	GAA2/IO174PPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO54RSB0
D8	GBC1/IO55RSB0
D9	GBB2/IO61PDB1
D10	IO61NDB1
D11	IO62NPB1
D12	GCB1/IO70PPB1
E1	V_{CC}
E2	GFC0/IO164NDB3
E3	GFC1/IO164PDB3
E4	V_{CCI}B3
E5	IO174NPB3
E6	V_{CCI}B0
E7	V_{CCI}B0
E8	GCC1/IO69PDB1
E9	V_{CCI}B1
E10	V_{CC}
E11	GCA0/IO71NDB1
E12	IO72NDB1
F1	GFB0/IO163NPB3
F2	V_{COMPLF}
F3	GFB1/IO163PPB3
F4	IO161NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO69NDB1
F9	GCB0/IO70NPB1
F10	GND
F11	GCA1/IO71PDB1
F12	GCA2/IO72PDB1

144-Pin FBGA	
Pin Number	AGL600 Function
G1	GFA1/IO162PPB3
G2	GND
G3	VCCPLF
G4	GFA0/IO162NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO86PPB1
G9	IO74NDB1
G10	GCC2/IO74PDB1
G11	IO73NDB1
G12	GCB2/IO73PDB1
H1	V_{CC}
H2	GFB2/IO160PDB3
H3	GFC2/IO159PSB3
H4	GEC1/IO146PDB3
H5	V_{CC}
H6	IO80PDB1
H7	IO80NDB1
H8	GDB2/IO90RSB2
H9	GDC0/IO86NPB1
H10	V_{CCI}B1
H11	IO84PSB1
H12	V_{CC}
J1	GEB1/IO145PDB3
J2	IO160NDB3
J3	V_{CCI}B3
J4	GEC0/IO146NDB3
J5	IO129RSB2
J6	IO131RSB2
J7	V_{CC}
J8	TCK
J9	GDA2/IO89RSB2
J10	TDO
J11	GDA1/IO88PDB1
J12	GDB1/IO87PDB1

144-Pin FBGA	
Pin Number	**AGL600 Function**
K1	GEB0/IO145NDB3
K2	GEA1/IO144PDB3
K3	GEA0/IO144NDB3
K4	GEA2/IO143RSB2
K5	IO119RSB2
K6	IO111RSB2
K7	GND
K8	IO94RSB2
K9	GDC2/IO91RSB2
K10	GND
K11	GDA0/IO88NDB1
K12	GDB0/IO87NDB1
L1	GND
L2	VMV3
L3	FF/GEB2/IO142RSB2
L4	IO136RSB2
L5	V_{CCI}B2
L6	IO115RSB2
L7	IO103RSB2
L8	IO97RSB2
L9	TMS
L10	V_{JTAG}
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO141RSB2
M3	IO138RSB2
M4	IO123RSB2
M5	IO126RSB2
M6	IO134RSB2
M7	IO108RSB2
M8	IO99RSB2
M9	TDI
M10	V_{CCI}B2
M11	V_{PUMP}
M12	GNDQ

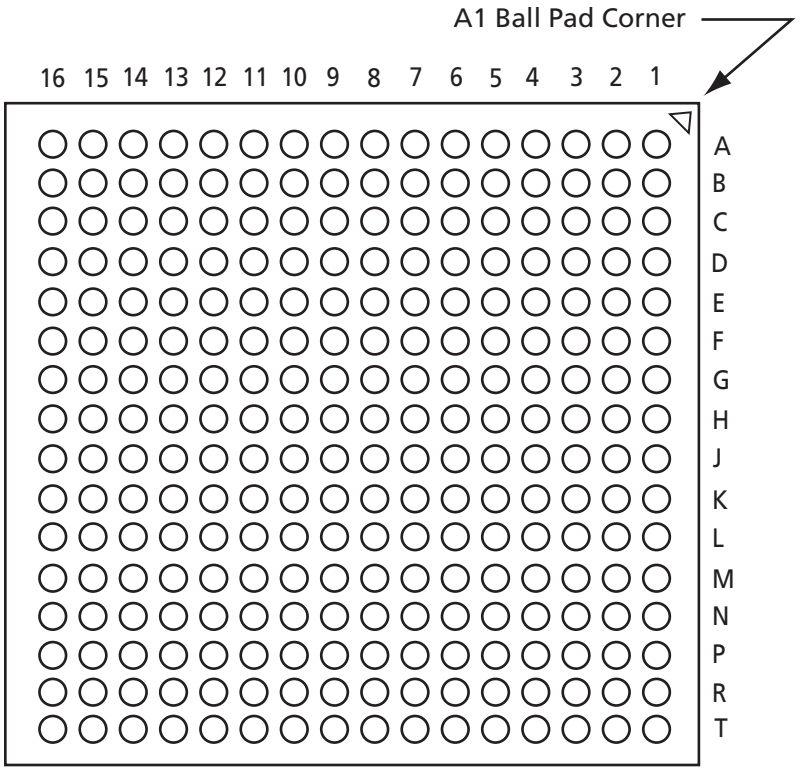
144-Pin FBGA	
Pin Number	AGL1000 Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO10RSB0
A6	GND
A7	IO44RSB0
A8	V_{CC}
A9	IO69RSB0
A10	GBA0/IO76RSB0
A11	GBA1/IO77RSB0
A12	GNDQ
B1	GAB2/IO224PDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO13RSB0
B6	IO26RSB0
B7	IO35RSB0
B8	IO60RSB0
B9	GBB0/IO74RSB0
B10	GBB1/IO75RSB0
B11	GND
B12	VMV1
C1	IO224NDB3
C2	GFA2/IO206PPB3
C3	GAC2/IO223PDB3
C4	V_{CC}
C5	IO16RSB0
C6	IO29RSB0
C7	IO32RSB0
C8	IO63RSB0
C9	IO66RSB0
C10	GBA2/IO78PDB1
C11	IO78NDB1
C12	GBC2/IO80PPB1

144-Pin FBGA	
Pin Number	AGL1000 Function
D1	IO213PDB3
D2	IO213NDB3
D3	IO223NDB3
D4	GAA2/IO225PPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO72RSB0
D8	GBC1/IO73RSB0
D9	GBB2/IO79PDB1
D10	IO79NDB1
D11	IO80NPB1
D12	GCB1/IO92PPB1
E1	V_{CC}
E2	GFC0/IO209NDB3
E3	GFC1/IO209PDB3
E4	V_{CCI}B3
E5	IO225NPB3
E6	V_{CCI}B0
E7	V_{CCI}B0
E8	GCC1/IO91PDB1
E9	V_{CCI}B1
E10	V_{CC}
E11	GCA0/IO93NDB1
E12	IO94NDB1
F1	GFB0/IO208NPB3
F2	V_{COMPLF}
F3	GFB1/IO208PPB3
F4	IO206NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO91NDB1
F9	GCB0/IO92NPB1
F10	GND
F11	GCA1/IO93PDB1
F12	GCA2/IO94PDB1

144-Pin FBGA	
Pin Number	AGL1000 Function
G1	GFA1/IO207PPB3
G2	GND
G3	V_{CCPLF}
G4	GFA0/IO207NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO111PPB1
G9	IO96NDB1
G10	GCC2/IO96PDB1
G11	IO95NDB1
G12	GCB2/IO95PDB1
H1	V_{CC}
H2	GFB2/IO205PDB3
H3	GFC2/IO204PSB3
H4	GEC1/IO190PDB3
H5	V_{CC}
H6	IO105PDB1
H7	IO105NDB1
H8	GDB2/IO115RSB2
H9	GDC0/IO111NPB1
H10	V_{CCI}B1
H11	IO101PSB1
H12	V_{CC}
J1	GEB1/IO189PDB3
J2	IO205NDB3
J3	V_{CCI}B3
J4	GEC0/IO190NDB3
J5	IO160RSB2
J6	IO157RSB2
J7	V_{CC}
J8	TCK
J9	GDA2/IO114RSB2
J10	TDO
J11	GDA1/IO113PDB1
J12	GDB1/IO112PDB1

144-Pin FBGA	
Pin Number	**AGL1000 Function**
K1	GEB0/IO189NDB3
K2	GEA1/IO188PDB3
K3	GEA0/IO188NDB3
K4	GEA2/IO187RSB2
K5	IO169RSB2
K6	IO152RSB2
K7	GND
K8	IO117RSB2
K9	GDC2/IO116RSB2
K10	GND
K11	GDA0/IO113NDB1
K12	GDB0/IO112NDB1
L1	GND
L2	VMV3
L3	FF/GEB2/IO186RSB2
L4	IO172RSB2
L5	V_{CCI}B2
L6	IO153RSB2
L7	IO144RSB2
L8	IO140RSB2
L9	TMS
L10	V_{JTAG}
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO185RSB2
M3	IO173RSB2
M4	IO168RSB2
M5	IO161RSB2
M6	IO156RSB2
M7	IO145RSB2
M8	IO141RSB2
M9	TDI
M10	V_{CCI}B2
M11	V_{PUMP}
M12	GNDQ

256-Pin FBGA



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

256-Pin FBGA	
Pin Number	AGL600 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO11RSB0
A6	IO16RSB0
A7	IO18RSB0
A8	IO28RSB0
A9	IO34RSB0
A10	IO37RSB0
A11	IO41RSB0
A12	IO43RSB0
A13	GBB1/IO57RSB0
A14	GBA0/IO58RSB0
A15	GBA1/IO59RSB0
A16	GND
B1	GAB2/IO173PDB3
B2	GAA2/IO174PDB3
B3	GNDQ
B4	GAB1/IO03RSB0
B5	IO13RSB0
B6	IO14RSB0
B7	IO21RSB0
B8	IO27RSB0
B9	IO32RSB0
B10	IO38RSB0
B11	IO42RSB0
B12	GBC1/IO55RSB0
B13	GBB0/IO56RSB0
B14	IO52RSB0
B15	GBA2/IO60PDB1
B16	IO60NDB1
C1	IO173NDB3
C2	IO174NDB3
C3	VMV3
C4	IO07RSB0
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0

256-Pin FBGA	
Pin Number	AGL600 Function
C7	IO20RSB0
C8	IO24RSB0
C9	IO33RSB0
C10	IO39RSB0
C11	IO44RSB0
C12	GBC0/IO54RSB0
C13	IO51RSB0
C14	VMV0
C15	IO61NPB1
C16	IO63PDB1
D1	IO171NDB3
D2	IO171PDB3
D3	GAC2/IO172PDB3
D4	IO06RSB0
D5	GNDQ
D6	IO10RSB0
D7	IO19RSB0
D8	IO26RSB0
D9	IO30RSB0
D10	IO40RSB0
D11	IO45RSB0
D12	GNDQ
D13	IO50RSB0
D14	GBB2/IO61PPB1
D15	IO53RSB0
D16	IO63NDB1
E1	IO166PDB3
E2	IO167NPB3
E3	IO172NDB3
E4	IO169NDB3
E5	VMV0
E6	V_{CCI}B0
E7	V_{CCI}B0
E8	IO25RSB0
E9	IO31RSB0
E10	V_{CCI}B0
E11	V_{CCI}B0
E12	VMV1

256-Pin FBGA	
Pin Number	AGL600 Function
E13	GBC2/IO62PDB1
E14	IO67PPB1
E15	IO64PPB1
E16	IO66PDB1
F1	IO166NDB3
F2	IO168NPB3
F3	IO167PPB3
F4	IO169PDB3
F5	V_{CCI}B3
F6	GND
F7	V_{CC}
F8	V_{CC}
F9	V_{CC}
F10	V_{CC}
F11	GND
F12	V_{CCI}B1
F13	IO62NDB1
F14	IO64NPB1
F15	IO65PPB1
F16	IO66NDB1
G1	IO165NDB3
G2	IO165PDB3
G3	IO168PPB3
G4	GFC1/IO164PPB3
G5	V_{CCI}B3
G6	V_{CC}
G7	GND
G8	GND
G9	GND
G10	GND
G11	V_{CC}
G12	V_{CCI}B1
G13	GCC1/IO69PPB1
G14	IO65NPB1
G15	IO75PDB1
G16	IO75NDB1
H1	GFB0/IO163NPB3
H2	GFA0/IO162NDB3

256-Pin FBGA	
Pin Number	AGL600 Function
H3	GFB1/IO163PPB3
H4	V_{COMPLF}
H5	GFC0/IO164NPB3
H6	V_{CC}
H7	GND
H8	GND
H9	GND
H10	GND
H11	V_{CC}
H12	GCC0/IO69NPB1
H13	GCB1/IO70PPB1
H14	GCA0/IO71NPB1
H15	IO67NPB1
H16	GCB0/IO70NPB1
J1	GFA2/IO161PPB3
J2	GFA1/IO162PDB3
J3	VCCPLF
J4	IO160NDB3
J5	GFB2/IO160PDB3
J6	V_{CC}
J7	GND
J8	GND
J9	GND
J10	GND
J11	V_{CC}
J12	GCB2/IO73PPB1
J13	GCA1/IO71PPB1
J14	GCC2/IO74PPB1
J15	IO80PPB1
J16	GCA2/IO72PDB1
K1	GFC2/IO159PDB3
K2	IO161NPB3
K3	IO156PPB3
K4	IO129RSB2
K5	V_{CCI}B3
K6	V_{CC}
K7	GND
K8	GND

256-Pin FBGA	
Pin Number	AGL600 Function
K9	GND
K10	GND
K11	V_{CC}
K12	V_{CCI}B1
K13	IO73NPB1
K14	IO80NPB1
K15	IO74NPB1
K16	IO72NDB1
L1	IO159NDB3
L2	IO156NPB3
L3	IO151PPB3
L4	IO158PSB3
L5	V_{CCI}B3
L6	GND
L7	V_{CC}
L8	V_{CC}
L9	V_{CC}
L10	V_{CC}
L11	GND
L12	V_{CCI}B1
L13	GDB0/IO87NPB1
L14	IO85NDB1
L15	IO85PDB1
L16	IO84PDB1
M1	IO150PDB3
M2	IO151NPB3
M3	IO147NPB3
M4	GEC0/IO146NPB3
M5	VMV3
M6	V_{CCI}B2
M7	V_{CCI}B2
M8	IO117RSB2
M9	IO110RSB2
M10	V_{CCI}B2
M11	V_{CCI}B2
M12	VMV2
M13	IO94RSB2
M14	GDB1/IO87PPB1

256-Pin FBGA	
Pin Number	AGL600 Function
M15	GDC1/IO86PDB1
M16	IO84NDB1
N1	IO150NDB3
N2	IO147PPB3
N3	GEC1/IO146PPB3
N4	IO140RSB2
N5	GNDQ
N6	GEA2/IO143RSB2
N7	IO126RSB2
N8	IO120RSB2
N9	IO108RSB2
N10	IO103RSB2
N11	IO99RSB2
N12	GNDQ
N13	IO92RSB2
N14	V_{JTAG}
N15	GDC0/IO86NDB1
N16	GDA1/IO88PDB1
P1	GEB1/IO145PDB3
P2	GEB0/IO145NDB3
P3	VMV2
P4	IO138RSB2
P5	IO136RSB2
P6	IO131RSB2
P7	IO124RSB2
P8	IO119RSB2
P9	IO107RSB2
P10	IO104RSB2
P11	IO97RSB2
P12	VMV1
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO88NDB1
R1	GEA1/IO144PDB3
R2	GEA0/IO144NDB3
R3	IO139RSB2
R4	GEC2/IO141RSB2

256-Pin FBGA	
Pin Number	**AGL600 Function**
R5	IO132RSB2
R6	IO127RSB2
R7	IO121RSB2
R8	IO114RSB2
R9	IO109RSB2
R10	IO105RSB2
R11	IO98RSB2
R12	IO96RSB2
R13	GDB2/IO90RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO137RSB2
T3	FF/GEB2/IO142RSB2
T4	IO134RSB2
T5	IO125RSB2
T6	IO123RSB2
T7	IO118RSB2
T8	IO115RSB2
T9	IO111RSB2
T10	IO106RSB2
T11	IO102RSB2
T12	GDC2/IO91RSB2
T13	IO93RSB2
T14	GDA2/IO89RSB2
T15	TMS
T16	GND

256-Pin FBGA	
Pin Number	AGL1000 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO16RSB0
A6	IO22RSB0
A7	IO28RSB0
A8	IO35RSB0
A9	IO45RSB0
A10	IO50RSB0
A11	IO55RSB0
A12	IO61RSB0
A13	GBB1/IO75RSB0
A14	GBA0/IO76RSB0
A15	GBA1/IO77RSB0
A16	GND
B1	GAB2/IO224PDB3
B2	GAA2/IO225PDB3
B3	GNDQ
B4	GAB1/IO03RSB0
B5	IO17RSB0
B6	IO21RSB0
B7	IO27RSB0
B8	IO34RSB0
B9	IO44RSB0
B10	IO51RSB0
B11	IO57RSB0
B12	GBC1/IO73RSB0
B13	GBB0/IO74RSB0
B14	IO71RSB0
B15	GBA2/IO78PDB1
B16	IO81PDB1
C1	IO224NDB3
C2	IO225NDB3
C3	VMV3
C4	IO11RSB0
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0

256-Pin FBGA	
Pin Number	AGL1000 Function
C7	IO25RSB0
C8	IO36RSB0
C9	IO42RSB0
C10	IO49RSB0
C11	IO56RSB0
C12	GBC0/IO72RSB0
C13	IO62RSB0
C14	VMV0
C15	IO78NDB1
C16	IO81NDB1
D1	IO222NDB3
D2	IO222PDB3
D3	GAC2/IO223PDB3
D4	IO223NDB3
D5	GNDQ
D6	IO23RSB0
D7	IO29RSB0
D8	IO33RSB0
D9	IO46RSB0
D10	IO52RSB0
D11	IO60RSB0
D12	GNDQ
D13	IO80NDB1
D14	GBB2/IO79PDB1
D15	IO79NDB1
D16	IO82NSB1
E1	IO217PDB3
E2	IO218PDB3
E3	IO221NDB3
E4	IO221PDB3
E5	VMV0
E6	V_{CCI}B0
E7	V_{CCI}B0
E8	IO38RSB0
E9	IO47RSB0
E10	V_{CCI}B0
E11	V_{CCI}B0
E12	VMV1

256-Pin FBGA	
Pin Number	AGL1000 Function
E13	GBC2/IO80PDB1
E14	IO83PPB1
E15	IO86PPB1
E16	IO87PDB1
F1	IO217NDB3
F2	IO218NDB3
F3	IO216PDB3
F4	IO216NDB3
F5	V_{CCI}B3
F6	GND
F7	V_{CC}
F8	V_{CC}
F9	V_{CC}
F10	V_{CC}
F11	GND
F12	V_{CCI}B1
F13	IO83NPB1
F14	IO86NPB1
F15	IO90PPB1
F16	IO87NDB1
G1	IO210PSB3
G2	IO213NDB3
G3	IO213PDB3
G4	GFC1/IO209PPB3
G5	V_{CCI}B3
G6	V_{CC}
G7	GND
G8	GND
G9	GND
G10	GND
G11	V_{CC}
G12	V_{CCI}B1
G13	GCC1/IO91PPB1
G14	IO90NPB1
G15	IO88PDB1
G16	IO88NDB1
H1	GFB0/IO208NPB3
H2	GFA0/IO207NDB3

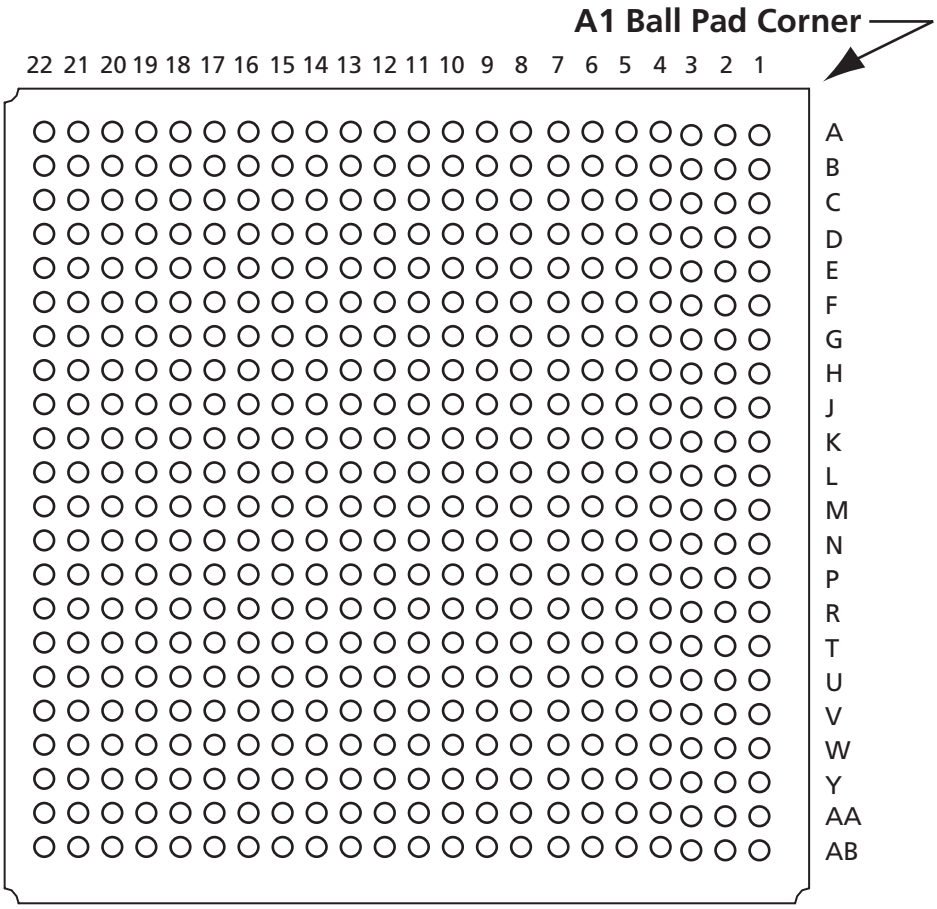
256-Pin FBGA	
Pin Number	AGL1000 Function
H3	GFB1/IO208PPB3
H4	V_{COMPLF}
H5	GFC0/IO209NPB3
H6	V_{CC}
H7	GND
H8	GND
H9	GND
H10	GND
H11	V_{CC}
H12	GCC0/IO91NPB1
H13	GCB1/IO92PPB1
H14	GCA0/IO93NPB1
H15	IO96NPB1
H16	GCB0/IO92NPB1
J1	GFA2/IO206PSB3
J2	GFA1/IO207PDB3
J3	V_{CCPLF}
J4	IO205NDB3
J5	GFB2/IO205PDB3
J6	V_{CC}
J7	GND
J8	GND
J9	GND
J10	GND
J11	V_{CC}
J12	GCB2/IO95PPB1
J13	GCA1/IO93PPB1
J14	GCC2/IO96PPB1
J15	IO100PPB1
J16	GCA2/IO94PSB1
K1	GFC2/IO204PDB3
K2	IO204NDB3
K3	IO203NDB3
K4	IO203PDB3
K5	V_{CCI}B3
K6	V_{CC}
K7	GND
K8	GND

256-Pin FBGA	
Pin Number	AGL1000 Function
K9	GND
K10	GND
K11	V_{CC}
K12	V_{CCI}B1
K13	IO95NPB1
K14	IO100NPB1
K15	IO102NDB1
K16	IO102PDB1
L1	IO202NDB3
L2	IO202PDB3
L3	IO196PPB3
L4	IO193PPB3
L5	V_{CCI}B3
L6	GND
L7	V_{CC}
L8	V_{CC}
L9	V_{CC}
L10	V_{CC}
L11	GND
L12	V_{CCI}B1
L13	GDB0/IO112NPB1
L14	IO106NDB1
L15	IO106PDB1
L16	IO107PDB1
M1	IO197NSB3
M2	IO196NPB3
M3	IO193NPB3
M4	GEC0/IO190NPB3
M5	VMV3
M6	V_{CCI}B2
M7	V_{CCI}B2
M8	IO147RSB2
M9	IO136RSB2
M10	V_{CCI}B2
M11	V_{CCI}B2
M12	VMV2
M13	IO110NDB1
M14	GDB1/IO112PPB1

256-Pin FBGA	
Pin Number	AGL1000 Function
M15	GDC1/IO111PDB1
M16	IO107NDB1
N1	IO194PSB3
N2	IO192PPB3
N3	GEC1/IO190PPB3
N4	IO192NPB3
N5	GNDQ
N6	GEA2/IO187RSB2
N7	IO161RSB2
N8	IO155RSB2
N9	IO141RSB2
N10	IO129RSB2
N11	IO124RSB2
N12	GNDQ
N13	IO110PDB1
N14	V_{JTAG}
N15	GDC0/IO111NDB1
N16	GDA1/IO113PDB1
P1	GEB1/IO189PDB3
P2	GEB0/IO189NDB3
P3	VMV2
P4	IO179RSB2
P5	IO171RSB2
P6	IO165RSB2
P7	IO159RSB2
P8	IO151RSB2
P9	IO137RSB2
P10	IO134RSB2
P11	IO128RSB2
P12	VMV1
P13	TCK
P14	V_{PUMP}
P15	TRST
P16	GDA0/IO113NDB1
R1	GEA1/IO188PDB3
R2	GEA0/IO188NDB3
R3	IO184RSB2
R4	GEC2/IO185RSB2

256-Pin FBGA	
Pin Number	**AGL1000 Function**
R5	IO168RSB2
R6	IO163RSB2
R7	IO157RSB2
R8	IO149RSB2
R9	IO143RSB2
R10	IO138RSB2
R11	IO131RSB2
R12	IO125RSB2
R13	GDB2/IO115RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO183RSB2
T3	FF/GEB2/IO186RSB2
T4	IO172RSB2
T5	IO170RSB2
T6	IO164RSB2
T7	IO158RSB2
T8	IO153RSB2
T9	IO142RSB2
T10	IO135RSB2
T11	IO130RSB2
T12	GDC2/IO116RSB2
T13	IO120RSB2
T14	GDA2/IO114RSB2
T15	TMS
T16	GND

484-Pin FBGA



Note: This is the bottom view of the package.

Note

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484-Pin FBGA	
Pin Number	AGL600 Function
A1	GND
A2	GND
A3	V_{CCI}B0
A4	NC
A5	NC
A6	IO09RSB0
A7	IO15RSB0
A8	NC
A9	NC
A10	IO22RSB0
A11	IO23RSB0
A12	IO29RSB0
A13	IO35RSB0
A14	NC
A15	NC
A16	IO46RSB0
A17	IO48RSB0
A18	NC
A19	NC
A20	V_{CCI}B0
A21	GND
A22	GND
AA1	GND
AA2	V_{CCI}B3
AA3	NC
AA4	NC
AA5	NC
AA6	IO135RSB2
AA7	IO133RSB2
AA8	NC
AA9	NC
AA10	NC
AA11	NC
AA12	NC
AA13	NC
AA14	NC

484-Pin FBGA	
Pin Number	AGL600 Function
AA15	NC
AA16	IO101RSB2
AA17	NC
AA18	NC
AA19	NC
AA20	NC
AA21	V_{CCI}B1
AA22	GND
AB1	GND
AB2	GND
AB3	V_{CCI}B2
AB4	NC
AB5	NC
AB6	IO130RSB2
AB7	IO128RSB2
AB8	IO122RSB2
AB9	IO116RSB2
AB10	NC
AB11	NC
AB12	IO113RSB2
AB13	IO112RSB2
AB14	NC
AB15	NC
AB16	IO100RSB2
AB17	IO95RSB2
AB18	NC
AB19	NC
AB20	V_{CCI}B2
AB21	GND
AB22	GND
B1	GND
B2	V_{CCI}B3
B3	NC
B4	NC
B5	NC
B6	IO08RSB0

484-Pin FBGA	
Pin Number	AGL600 Function
B7	IO12RSB0
B8	NC
B9	NC
B10	IO17RSB0
B11	NC
B12	NC
B13	IO36RSB0
B14	NC
B15	NC
B16	IO47RSB0
B17	IO49RSB0
B18	NC
B19	NC
B20	NC
B21	V_{CCI}B1
B22	GND
C1	V_{CCI}B3
C2	NC
C3	NC
C4	NC
C5	GND
C6	NC
C7	NC
C8	V_{CC}
C9	V_{CC}
C10	NC
C11	NC
C12	NC
C13	NC
C14	V_{CC}
C15	V_{CC}
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC

484-Pin FBGA	
Pin Number	AGL600 Function
C21	NC
C22	V_{CCI}B1
D1	NC
D2	NC
D3	NC
D4	GND
D5	GAA0/IO00RSB0
D6	GAA1/IO01RSB0
D7	GAB0/IO02RSB0
D8	IO11RSB0
D9	IO16RSB0
D10	IO18RSB0
D11	IO28RSB0
D12	IO34RSB0
D13	IO37RSB0
D14	IO41RSB0
D15	IO43RSB0
D16	GBB1/IO57RSB0
D17	GBA0/IO58RSB0
D18	GBA1/IO59RSB0
D19	GND
D20	NC
D21	NC
D22	NC
E1	NC
E2	NC
E3	GND
E4	GAB2/IO173PDB3
E5	GAA2/IO174PDB3
E6	GNDQ
E7	GAB1/IO03RSB0
E8	IO13RSB0
E9	IO14RSB0
E10	IO21RSB0
E11	IO27RSB0
E12	IO32RSB0

484-Pin FBGA	
Pin Number	AGL600 Function
E13	IO38RSB0
E14	IO42RSB0
E15	GBC1/IO55RSB0
E16	GBB0/IO56RSB0
E17	IO52RSB0
E18	GBA2/IO60PDB1
E19	IO60NDB1
E20	GND
E21	NC
E22	NC
F1	NC
F2	NC
F3	NC
F4	IO173NDB3
F5	IO174NDB3
F6	VMV3
F7	IO07RSB0
F8	GAC0/IO04RSB0
F9	GAC1/IO05RSB0
F10	IO20RSB0
F11	IO24RSB0
F12	IO33RSB0
F13	IO39RSB0
F14	IO44RSB0
F15	GBC0/IO54RSB0
F16	IO51RSB0
F17	VMV0
F18	IO61NPB1
F19	IO63PDB1
F20	NC
F21	NC
F22	NC
G1	IO170NDB3
G2	IO170PDB3
G3	NC
G4	IO171NDB3

484-Pin FBGA	
Pin Number	AGL600 Function
G5	IO171PDB3
G6	GAC2/IO172PDB3
G7	IO06RSB0
G8	GNDQ
G9	IO10RSB0
G10	IO19RSB0
G11	IO26RSB0
G12	IO30RSB0
G13	IO40RSB0
G14	IO45RSB0
G15	GNDQ
G16	IO50RSB0
G17	GBB2/IO61PPB1
G18	IO53RSB0
G19	IO63NDB1
G20	NC
G21	NC
G22	NC
H1	NC
H2	NC
H3	V_{CC}
H4	IO166PDB3
H5	IO167NPB3
H6	IO172NDB3
H7	IO169NDB3
H8	VMV0
H9	V_{CCI}B0
H10	V_{CCI}B0
H11	IO25RSB0
H12	IO31RSB0
H13	V_{CCI}B0
H14	V_{CCI}B0
H15	VMV1
H16	GBC2/IO62PDB1
H17	IO67PPB1
H18	IO64PPB1

484-Pin FBGA	
Pin Number	AGL600 Function
H19	IO66PDB1
H20	V_{CC}
H21	NC
H22	NC
J1	NC
J2	NC
J3	NC
J4	IO166NDB3
J5	IO168NPB3
J6	IO167PPB3
J7	IO169PDB3
J8	V_{CCI}B3
J9	GND
J10	V_{CC}
J11	V_{CC}
J12	V_{CC}
J13	V_{CC}
J14	GND
J15	V_{CCI}B1
J16	IO62NDB1
J17	IO64NPB1
J18	IO65PPB1
J19	IO66NDB1
J20	NC
J21	IO68PDB1
J22	IO68NDB1
K1	IO157PDB3
K2	IO157NDB3
K3	NC
K4	IO165NDB3
K5	IO165PDB3
K6	IO168PPB3
K7	GFC1/IO164PPB3
K8	V_{CCI}B3
K9	V_{CC}
K10	GND

484-Pin FBGA	
Pin Number	AGL600 Function
K11	GND
K12	GND
K13	GND
K14	V_{CC}
K15	VvB1
K16	GCC1/IO69PPB1
K17	IO65NPB1
K18	IO75PDB1
K19	IO75NDB1
K20	NC
K21	IO76NDB1
K22	IO76PDB1
L1	NC
L2	IO155PDB3
L3	NC
L4	GFB0/IO163NPB3
L5	GFA0/IO162NDB3
L6	GFB1/IO163PPB3
L7	V_{COMPLF}
L8	GFC0/IO164NPB3
L9	V_{CC}
L10	GND
L11	GND
L12	GND
L13	GND
L14	V_{CC}
L15	GCC0/IO69NPB1
L16	GCB1/IO70PPB1
L17	GCA0/IO71NPB1
L18	IO67NPB1
L19	GCB0/IO70NPB1
L20	IO77PDB1
L21	IO77NDB1
L22	IO78NPB1
M1	NC
M2	IO155NDB3

484-Pin FBGA	
Pin Number	AGL600 Function
M3	IO158NPB3
M4	GFA2/IO161PPB3
M5	GFA1/IO162PDB3
M6	V_{CCPLF}
M7	IO160NDB3
M8	GFB2/IO160PDB3
M9	V_{CC}
M10	GND
M11	GND
M12	GND
M13	GND
M14	V_{CC}
M15	GCB2/IO73PPB1
M16	GCA1/IO71PPB1
M17	GCC2/IO74PPB1
M18	IO80PPB1
M19	GCA2/IO72PDB1
M20	IO79PPB1
M21	IO78PPB1
M22	NC
N1	IO154NDB3
N2	IO154PDB3
N3	NC
N4	GFC2/IO159PDB3
N5	IO161NPB3
N6	IO156PPB3
N7	IO129RSB2
N8	V_{CCI}B3
N9	V_{CC}
N10	GND
N11	GND
N12	GND
N13	GND
N14	V_{CC}
N15	V_{CCI}B1
N16	IO73NPB1

484-Pin FBGA	
Pin Number	AGL600 Function
N17	IO80NPB1
N18	IO74NPB1
N19	IO72NDB1
N20	NC
N21	IO79NPB1
N22	NC
P1	NC
P2	IO153PDB3
P3	IO153NDB3
P4	IO159NDB3
P5	IO156NPB3
P6	IO151PPB3
P7	IO158PPB3
P8	V_{CCI}B3
P9	GND
P10	V_{CC}
P11	V_{CC}
P12	V_{CC}
P13	V_{CC}
P14	GND
P15	V_{CCI}B1
P16	GDB0/IO87NPB1
P17	IO85NDB1
P18	IO85PDB1
P19	IO84PDB1
P20	NC
P21	IO81PDB1
P22	NC
R1	NC
R2	NC
R3	V_{CC}
R4	IO150PDB3
R5	IO151NPB3
R6	IO147NPB3
R7	GEC0/IO146NPB3
R8	VMV3

484-Pin FBGA	
Pin Number	AGL600 Function
R9	V_{CCI}B2
R10	V_{CCI}B2
R11	IO117RSB2
R12	IO110RSB2
R13	V_{CCI}B2
R14	V_{CCI}B2
R15	VMV2
R16	IO94RSB2
R17	GDB1/IO87PPB1
R18	GDC1/IO86PDB1
R19	IO84NDB1
R20	V_{CC}
R21	IO81NDB1
R22	IO82PDB1
T1	IO152PDB3
T2	IO152NDB3
T3	NC
T4	IO150NDB3
T5	IO147PPB3
T6	GEC1/IO146PPB3
T7	IO140RSB2
T8	GNDQ
T9	GEA2/IO143RSB2
T10	IO126RSB2
T11	IO120RSB2
T12	IO108RSB2
T13	IO103RSB2
T14	IO99RSB2
T15	GNDQ
T16	IO92RSB2
T17	V_{JTAG}
T18	GDC0/IO86NDB1
T19	GDA1/IO88PDB1
T20	NC
T21	IO83PDB1
T22	IO82NDB1

484-Pin FBGA	
Pin Number	AGL600 Function
U1	IO149PDB3
U2	IO149NDB3
U3	NC
U4	GEB1/IO145PDB3
U5	GEB0/IO145NDB3
U6	VMV2
U7	IO138RSB2
U8	IO136RSB2
U9	IO131RSB2
U10	IO124RSB2
U11	IO119RSB2
U12	IO107RSB2
U13	IO104RSB2
U14	IO97RSB2
U15	VMV1
U16	TCK
U17	V_{PUMP}
U18	TRST
U19	GDA0/IO88NDB1
U20	NC
U21	IO83NDB1
U22	NC
V1	NC
V2	NC
V3	GND
V4	GEA1/IO144PDB3
V5	GEA0/IO144NDB3
V6	IO139RSB2
V7	GEC2/IO141RSB2
V8	IO132RSB2
V9	IO127RSB2
V10	IO121RSB2
V11	IO114RSB2
V12	IO109RSB2
V13	IO105RSB2
V14	IO98RSB2

484-Pin FBGA	
Pin Number	**AGL600 Function**
V15	IO96RSB2
V16	GDB2/IO90RSB2
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	NC
W1	NC
W2	IO148PDB3
W3	NC
W4	GND
W5	IO137RSB2
W6	FF/GEB2/IO142RSB2
W7	IO134RSB2
W8	IO125RSB2
W9	IO123RSB2
W10	IO118RSB2
W11	IO115RSB2
W12	IO111RSB2
W13	IO106RSB2
W14	IO102RSB2
W15	GDC2/IO91RSB2
W16	IO93RSB2
W17	GDA2/IO89RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	V_{CCI}B3
Y2	IO148NDB3
Y3	NC
Y4	NC
Y5	GND
Y6	NC

484-Pin FBGA	
Pin Number	**AGL600 Function**
Y7	NC
Y8	V_{CC}
Y9	V_{CC}
Y10	NC
Y11	NC
Y12	NC
Y13	NC
Y14	V_{CC}
Y15	V_{CC}
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	V_{CCI}B1

484-Pin FBGA	
Pin Number	AGL1000 Function
A1	GND
A2	GND
A3	V_{CCI}B0
A4	IO07RSB0
A5	IO09RSB0
A6	IO13RSB0
A7	IO18RSB0
A8	IO20RSB0
A9	IO26RSB0
A10	IO32RSB0
A11	IO40RSB0
A12	IO41RSB0
A13	IO53RSB0
A14	IO59RSB0
A15	IO64RSB0
A16	IO65RSB0
A17	IO67RSB0
A18	IO69RSB0
A19	NC
A20	V_{CCI}B0
A21	GND
A22	GND
AA1	GND
AA2	V_{CCI}B3
AA3	NC
AA4	IO181RSB2
AA5	IO178RSB2
AA6	IO175RSB2
AA7	IO169RSB2
AA8	IO166RSB2
AA9	IO160RSB2
AA10	IO152RSB2
AA11	IO146RSB2
AA12	IO139RSB2
AA13	IO133RSB2
AA14	NC

484-Pin FBGA	
Pin Number	AGL1000 Function
AA15	NC
AA16	IO122RSB2
AA17	IO119RSB2
AA18	IO117RSB2
AA19	NC
AA20	NC
AA21	V_{CCI}B1
AA22	GND
AB1	GND
AB2	GND
AB3	V_{CCI}B2
AB4	IO180RSB2
AB5	IO176RSB2
AB6	IO173RSB2
AB7	IO167RSB2
AB8	IO162RSB2
AB9	IO156RSB2
AB10	IO150RSB2
AB11	IO145RSB2
AB12	IO144RSB2
AB13	IO132RSB2
AB14	IO127RSB2
AB15	IO126RSB2
AB16	IO123RSB2
AB17	IO121RSB2
AB18	IO118RSB2
AB19	NC
AB20	V_{CCI}B2
AB21	GND
AB22	GND
B1	GND
B2	V_{CCI}B3
B3	NC
B4	IO06RSB0
B5	IO08RSB0
B6	IO12RSB0

484-Pin FBGA	
Pin Number	AGL1000 Function
B7	IO15RSB0
B8	IO19RSB0
B9	IO24RSB0
B10	IO31RSB0
B11	IO39RSB0
B12	IO48RSB0
B13	IO54RSB0
B14	IO58RSB0
B15	IO63RSB0
B16	IO66RSB0
B17	IO68RSB0
B18	IO70RSB0
B19	NC
B20	NC
B21	V_{CCI}B1
B22	GND
C1	V_{CCI}B3
C2	IO220PDB3
C3	NC
C4	NC
C5	GND
C6	IO10RSB0
C7	IO14RSB0
C8	V_{CC}
C9	V_{CC}
C10	IO30RSB0
C11	IO37RSB0
C12	IO43RSB0
C13	NC
C14	V_{CC}
C15	V_{CC}
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC

484-Pin FBGA	
Pin Number	AGL1000 Function
C21	NC
C22	V_{CCI}B1
D1	IO219PDB3
D2	IO220NDB3
D3	NC
D4	GND
D5	GAA0/IO00RSB0
D6	GAA1/IO01RSB0
D7	GAB0/IO02RSB0
D8	IO16RSB0
D9	IO22RSB0
D10	IO28RSB0
D11	IO35RSB0
D12	IO45RSB0
D13	IO50RSB0
D14	IO55RSB0
D15	IO61RSB0
D16	GBB1/IO75RSB0
D17	GBA0/IO76RSB0
D18	GBA1/IO77RSB0
D19	GND
D20	NC
D21	NC
D22	NC
E1	IO219NDB3
E2	NC
E3	GND
E4	GAB2/IO224PDB3
E5	GAA2/IO225PDB3
E6	GNDQ
E7	GAB1/IO03RSB0
E8	IO17RSB0
E9	IO21RSB0
E10	IO27RSB0
E11	IO34RSB0
E12	IO44RSB0

484-Pin FBGA	
Pin Number	AGL1000 Function
E13	IO51RSB0
E14	IO57RSB0
E15	GBC1/IO73RSB0
E16	GBB0/IO74RSB0
E17	IO71RSB0
E18	GBA2/IO78PDB1
E19	IO81PDB1
E20	GND
E21	NC
E22	IO84PDB1
F1	NC
F2	IO215PDB3
F3	IO215NDB3
F4	IO224NDB3
F5	IO225NDB3
F6	VMV3
F7	IO11RSB0
F8	GAC0/IO04RSB0
F9	GAC1/IO05RSB0
F10	IO25RSB0
F11	IO36RSB0
F12	IO42RSB0
F13	IO49RSB0
F14	IO56RSB0
F15	GBC0/IO72RSB0
F16	IO62RSB0
F17	VMV0
F18	IO78NDB1
F19	IO81NDB1
F20	IO82PPB1
F21	NC
F22	IO84NDB1
G1	IO214NDB3
G2	IO214PDB3
G3	NC
G4	IO222NDB3

484-Pin FBGA	
Pin Number	AGL1000 Function
G5	IO222PDB3
G6	GAC2/IO223PDB3
G7	IO223NDB3
G8	GNDQ
G9	IO23RSB0
G10	IO29RSB0
G11	IO33RSB0
G12	IO46RSB0
G13	IO52RSB0
G14	IO60RSB0
G15	GNDQ
G16	IO80NDB1
G17	GBB2/IO79PDB1
G18	IO79NDB1
G19	IO82NPB1
G20	IO85PDB1
G21	IO85NDB1
G22	NC
H1	NC
H2	NC
H3	V_{CC}
H4	IO217PDB3
H5	IO218PDB3
H6	IO221NDB3
H7	IO221PDB3
H8	VMV0
H9	V_{CCI}B0
H10	V_{CCI}B0
H11	IO38RSB0
H12	IO47RSB0
H13	V_{CCI}B0
H14	V_{CCI}B0
H15	VMV1
H16	GBC2/IO80PDB1
H17	IO83PPB1
H18	IO86PPB1

484-Pin FBGA	
Pin Number	AGL1000 Function
H19	IO87PDB1
H20	V_{CC}
H21	NC
H22	NC
J1	IO212NDB3
J2	IO212PDB3
J3	NC
J4	IO217NDB3
J5	IO218NDB3
J6	IO216PDB3
J7	IO216NDB3
J8	V_{CCI}B3
J9	GND
J10	V_{CC}
J11	V_{CC}
J12	V_{CC}
J13	V_{CC}
J14	GND
J15	V_{CCI}B1
J16	IO83NPB1
J17	IO86NPB1
J18	IO90PPB1
J19	IO87NDB1
J20	NC
J21	IO89PDB1
J22	IO89NDB1
K1	IO211PDB3
K2	IO211NDB3
K3	NC
K4	IO210PPB3
K5	IO213NDB3
K6	IO213PDB3
K7	GFC1/IO209PPB3
K8	V_{CCI}B3
K9	V_{CC}
K10	GND

484-Pin FBGA	
Pin Number	AGL1000 Function
K11	GND
K12	GND
K13	GND
K14	V_{CC}
K15	V_{CCI}B1
K16	GCC1/IO91PPB1
K17	IO90NPB1
K18	IO88PDB1
K19	IO88NDB1
K20	IO94NPB1
K21	IO98NDB1
K22	IO98PDB1
L1	NC
L2	IO200PDB3
L3	IO210NPB3
L4	GFB0/IO208NPB3
L5	GFA0/IO207NDB3
L6	GFB1/IO208PPB3
L7	V_{COMPLF}
L8	GFC0/IO209NPB3
L9	V_{CC}
L10	GND
L11	GND
L12	GND
L13	GND
L14	V_{CC}
L15	GCC0/IO91NPB1
L16	GCB1/IO92PPB1
L17	GCA0/IO93NPB1
L18	IO96NPB1
L19	GCB0/IO92NPB1
L20	IO97PDB1
L21	IO97NDB1
L22	IO99NPB1
M1	NC
M2	IO200NDB3

484-Pin FBGA	
Pin Number	AGL1000 Function
M3	IO206NDB3
M4	GFA2/IO206PDB3
M5	GFA1/IO207PDB3
M6	V_{CCPLF}
M7	IO205NDB3
M8	GFB2/IO205PDB3
M9	V_{CC}
M10	GND
M11	GND
M12	GND
M13	GND
M14	V_{CC}
M15	GCB2/IO95PPB1
M16	GCA1/IO93PPB1
M17	GCC2/IO96PPB1
M18	IO100PPB1
M19	GCA2/IO94PPB1
M20	IO101PPB1
M21	IO99PPB1
M22	NC
N1	IO201NDB3
N2	IO201PDB3
N3	NC
N4	GFC2/IO204PDB3
N5	IO204NDB3
N6	IO203NDB3
N7	IO203PDB3
N8	V_{CCI}B3
N9	V_{CC}
N10	GND
N11	GND
N12	GND
N13	GND
N14	V_{CC}
N15	V_{CCI}B1
N16	IO95NPB1

484-Pin FBGA	
Pin Number	AGL1000 Function
N17	IO100NPB1
N18	IO102NDB1
N19	IO102PDB1
N20	NC
N21	IO101NPB1
N22	IO103PDB1
P1	NC
P2	IO199PDB3
P3	IO199NDB3
P4	IO202NDB3
P5	IO202PDB3
P6	IO196PPB3
P7	IO193PPB3
P8	V_{CCI}B3
P9	GND
P10	V_{CC}
P11	V_{CC}
P12	V_{CC}
P13	V_{CC}
P14	GND
P15	V_{CCI}B1
P16	GDB0/IO112NPB1
P17	IO106NDB1
P18	IO106PDB1
P19	IO107PDB1
P20	NC
P21	IO104PDB1
P22	IO103NDB1
R1	NC
R2	IO197PPB3
R3	V_{CC}
R4	IO197NPB3
R5	IO196NPB3
R6	IO193NPB3
R7	GEC0/IO190NPB3
R8	VMV3

484-Pin FBGA	
Pin Number	AGL1000 Function
R9	V_{CCI}B2
R10	V_{CCI}B2
R11	IO147RSB2
R12	IO136RSB2
R13	V_{CCI}B2
R14	V_{CCI}B2
R15	VMV2
R16	IO110NDB1
R17	GDB1/IO112PPB1
R18	GDC1/IO111PDB1
R19	IO107NDB1
R20	V_{CC}
R21	IO104NDB1
R22	IO105PDB1
T1	IO198PDB3
T2	IO198NDB3
T3	NC
T4	IO194PPB3
T5	IO192PPB3
T6	GEC1/IO190PPB3
T7	IO192NPB3
T8	GNDQ
T9	GEA2/IO187RSB2
T10	IO161RSB2
T11	IO155RSB2
T12	IO141RSB2
T13	IO129RSB2
T14	IO124RSB2
T15	GNDQ
T16	IO110PDB1
T17	V_{JTAG}
T18	GDC0/IO111NDB1
T19	GDA1/IO113PDB1
T20	NC
T21	IO108PDB1
T22	IO105NDB1

484-Pin FBGA	
Pin Number	AGL1000 Function
U1	IO195PDB3
U2	IO195NDB3
U3	IO194NPB3
U4	GEB1/IO189PDB3
U5	GEB0/IO189NDB3
U6	VMV2
U7	IO179RSB2
U8	IO171RSB2
U9	IO165RSB2
U10	IO159RSB2
U11	IO151RSB2
U12	IO137RSB2
U13	IO134RSB2
U14	IO128RSB2
U15	VMV1
U16	TCK
U17	V_{PUMP}
U18	TRST
U19	GDA0/IO113NDB1
U20	NC
U21	IO108NDB1
U22	IO109PDB1
V1	NC
V2	NC
V3	GND
V4	GEA1/IO188PDB3
V5	GEA0/IO188NDB3
V6	IO184RSB2
V7	GEC2/IO185RSB2
V8	IO168RSB2
V9	IO163RSB2
V10	IO157RSB2
V11	IO149RSB2
V12	IO143RSB2
V13	IO138RSB2
V14	IO131RSB2

484-Pin FBGA	
Pin Number	AGL1000 Function
V15	IO125RSB2
V16	GDB2/IO115RSB2
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	IO109NDB1
W1	NC
W2	IO191PDB3
W3	NC
W4	GND
W5	IO183RSB2
W6	FF/GEB2/IO186RSB2
W7	IO172RSB2
W8	IO170RSB2
W9	IO164RSB2
W10	IO158RSB2
W11	IO153RSB2
W12	IO142RSB2
W13	IO135RSB2
W14	IO130RSB2
W15	GDC2/IO116RSB2
W16	IO120RSB2
W17	GDA2/IO114RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	V_{CCI}B3
Y2	IO191NDB3
Y3	NC
Y4	IO182RSB2
Y5	GND
Y6	IO177RSB2

484-Pin FBGA	
Pin Number	AGL1000 Function
Y7	IO174RSB2
Y8	V_{CC}
Y9	V_{CC}
Y10	IO154RSB2
Y11	IO148RSB2
Y12	IO140RSB2
Y13	NC
Y14	V_{CC}
Y15	V_{CC}
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	V_{CCI}B1

Part Number and Revision Date

Part Number 51700095-003-5
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List of Changes

The following table lists critical changes that were made in the current version of the chapter.

Previous Version	Changes in Current Version (v1.5)	Page
v1.4 (June 2008)	Pin numbers were added to the "68-Pin QFN" package diagram. Note 2 was added below the diagram.	3-19
	The "132-Pin QFN" package diagram was updated to include D1 to D4. In addition, note 1 was changed from top view to bottom view, and note 2 is new.	3-21
v1.3 (February 2008)	The "68-Pin QFN" package drawing was updated to include numbers on pins 1 and 68.	3-19
	The "281-Pin CSP" package and pin table was added for AGL1000.	3-16
v1.2 (February 2008)	The "196-Pin CSP" package and pin table was added for AGL250.	3-10
v1.1 (January 2008)	The "68-Pin QFN" section is new.	3-19
v1.0 (January 2008)	The "196-Pin CSP" package and pin table was added for AGL125.	3-7
Advance v0.7 (November 2007)	This document was previously in datasheet Advance v0.7. As a result of moving to the handbook format, Actel has restarted the version numbers. The new version number is v1.0.	N/A
Advance v0.6 (November 2007)	The "121-Pin CSP" and "281-Pin CSP" packages are new.	4-5, 4-7
	The "81-Pin CSP" table for the AGL030 device was updated to change the G6 pin function to IO44RSB1 and the JG pin function to IO45RSB1.	4-4
	The "121-Pin CSP" table for the AGL060 device is new.	4-6
	The "256-Pin FBGA" table for the AGL1000 device is new.	4-34
	The "281-Pin CSP" table for the AGL 600 device is new.	4-8
	The "100-Pin VQFP" table for the AGL060 device is new.	4-18
	The "144-Pin FBGA" table for the AGL250 device is new.	4-24
	The "144-Pin FBGA" table for the AGL1000 device is new.	4-28
	The "484-Pin FBGA" table for the AGL600 device is new.	4-38
	The "484-Pin FBGA" table for the AGL1000 device is new.	4-43
Advance v0.5 (September 2007)	The "81-Pin µCSP" table for the AGL030 device is new.	4-3
	The "81-Pin CSP" table for the AGL030 device is new.	4-1

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advance," and "Production". The definition of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Unmarked (production)

This version contains information that is considered to be final.

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Section II – Core Architecture

Actel®
POWER MATTERS

*Low-Power Flash Technology and Flash*Freeze Mode*

Actel®
POWER MATTERS

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1 – Core Architecture of IGLOO and ProASIC3 Devices

Device Architecture

Advanced Flash Switch

Unlike SRAM FPGAs, the low-power flash devices use a live-at-power-up ISP flash switch as their programming element. Flash cells are distributed throughout the device to provide nonvolatile, reconfigurable programming to connect signal lines to the appropriate VersaTile inputs and outputs. In the flash switch, two transistors share the floating gate, which stores the programming information (Figure 1-1). One is the sensing transistor, which is only used for writing and verification of the floating gate voltage. The other is the switching transistor. The latter is used to connect or separate routing nets, or to configure VersaTile logic. It is also used to erase the floating gate. Dedicated high-performance lines are connected as required using the flash switch for fast, low-skew, global signal distribution throughout the device core. Maximum core utilization is possible for virtually any design. The use of the flash switch technology also removes the possibility of firm errors, which are increasingly common in SRAM-based FPGAs.

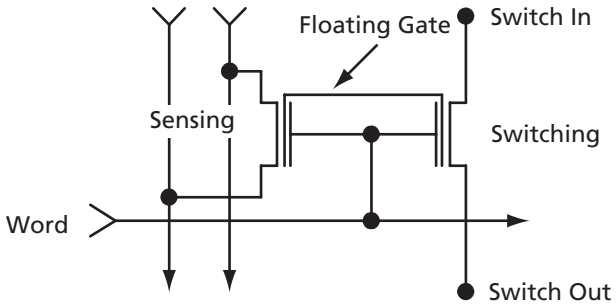


Figure 1-1 • **Flash-Based Switch**

IGLOO and ProASIC3 Core Architecture Support

The low-power flash families listed in Table 1-1 support the architecture features described in this document.

Table 1-1 • **Low-Power Flash Families**

Family[1]	Description	Timing Numbers[2]
IGLOO®	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*IGLOO DC and Switching Characteristics*
IGLOO PLUS	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology and enhanced I/O capabilities	*IGLOO PLUS DC and Switching Characteristics*
IGLOOe	IGLOO devices enhanced with higher density, five additional PLLs, and additional I/O standards	*IGLOOe DC and Switching Characteristics*
ProASIC®3L	Low-power, high-performance 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*ProASIC3L DC and Switching Characteristics*
ProASIC3	Low-power, high-performance 1.5 V FPGAs	*ProASIC3 DC and Switching Characteristics*
ProASIC3E	ProASIC3 enhanced with higher density, six additional PLLs, and additional I/O standards	*ProASIC3E DC and Switching Characteristics*
ProASIC3 Automotive	Low-power, high-performance FPGAs qualified for automotive applications	*Automotive ProASIC3 DC and Switching Characteristics*

Notes:

1. *The family names are linked to the appropriate product brief.*
2. *The timing number links go to the relevant timing numbers in the datasheet.*

Actel's low-power flash devices (listed in Table 1-1) provide a selection of low-power, secure, live-at-power-up, single-chip solutions. The nonvolatile flash-based devices do not require a boot PROM and incorporate FlashLock® technology, which provides a unique combination of reprogrammability and design security without external overhead. Only low-power flash FPGAs can offer these advantages.

Actel IGLOO PLUS FPGAs are the industry-leading 1.2 V ultra-low-power programmable logic devices (PLDs) and consume 90% less static power and over 50% less dynamic power than PLD alternatives, while ProASIC3L devices offer a balance of low power and higher performance.

Flash*Freeze technology used in IGLOO, IGLOO PLUS, and ProASIC3L devices enables easy entry to and exit from the ultra-low power mode, which consumes as little as 5 µW, while retaining SRAM and register data. IGLOO PLUS also offers the ability to hold I/O state in Flash*Freeze mode. Flash*Freeze technology simplifies power management through I/O and clock management without the need to turn off voltages, I/Os, or clocks at the system level. Entering and exiting Flash*Freeze mode takes less than 1 µs.

IGLOO Terminology

In documentation, the term IGLOO families or IGLOO devices refers to all IGLOO families as listed in Table 1-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

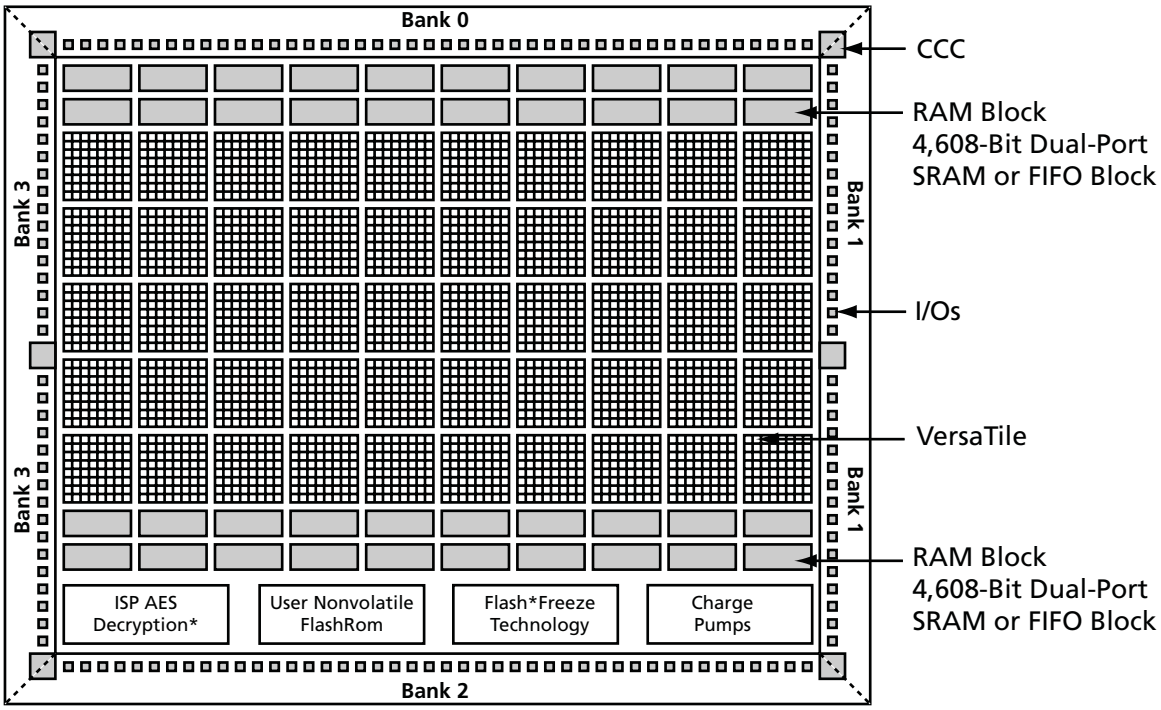
ProASIC3 Terminology

In documentation, the term ProASIC3 families or ProASIC3 devices refers to all ProASIC3 families as listed in Table 1-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

Device Overview

The low-power flash devices consist of multiple distinct programmable architectural features (Figure 1-2 on page 1-3 through Figure 1-4 on page 1-4):

- FPGA fabric/core (VersaTiles)
- Routing and clock resources (VersaNets)
- FlashROM
- Dedicated SRAM and/or FIFO
  - 15 k and 30 k gate devices do not support SRAM or FIFO.
  - Automotive devices do not support FIFO operation
- I/O Structures
- Flash*Freeze technology and low-power modes



*Note: Flash*Freeze technology only applies to IGLOO and ProASIC3L families.*

Figure 1-2 • **IGLOO and ProASIC3/L Device Architecture Overview with Four I/O Banks (AGL600 device is shown)**

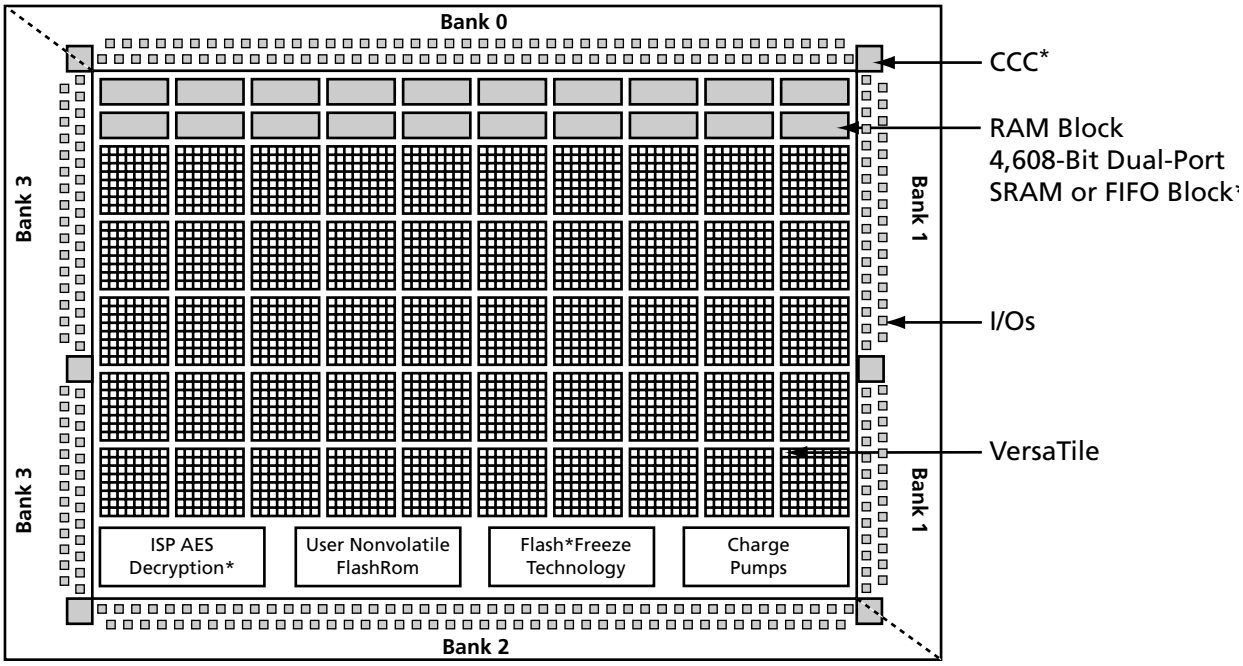
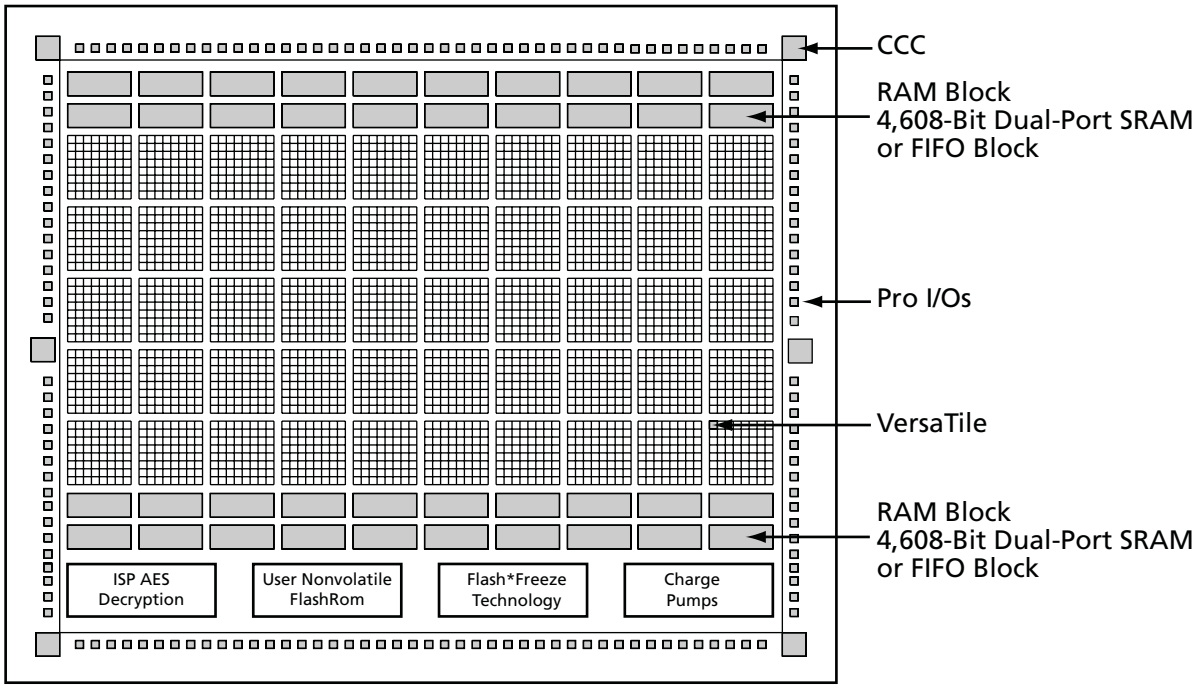


Figure 1-3 • **IGLOO PLUS Device Architecture Overview with Four I/O Banks**



*Note: Flash*Freeze technology only applies to IGLOOe devices.*

Figure 1-4 • **IGLOOe and ProASIC3E Device Architecture Overview (AGLE600 device is shown)**

Core Architecture

VersaTile

The proprietary IGLOO and ProASIC3 device architectures provide granularity comparable to gate arrays. The device core consists of a sea-of-VersaTiles architecture.

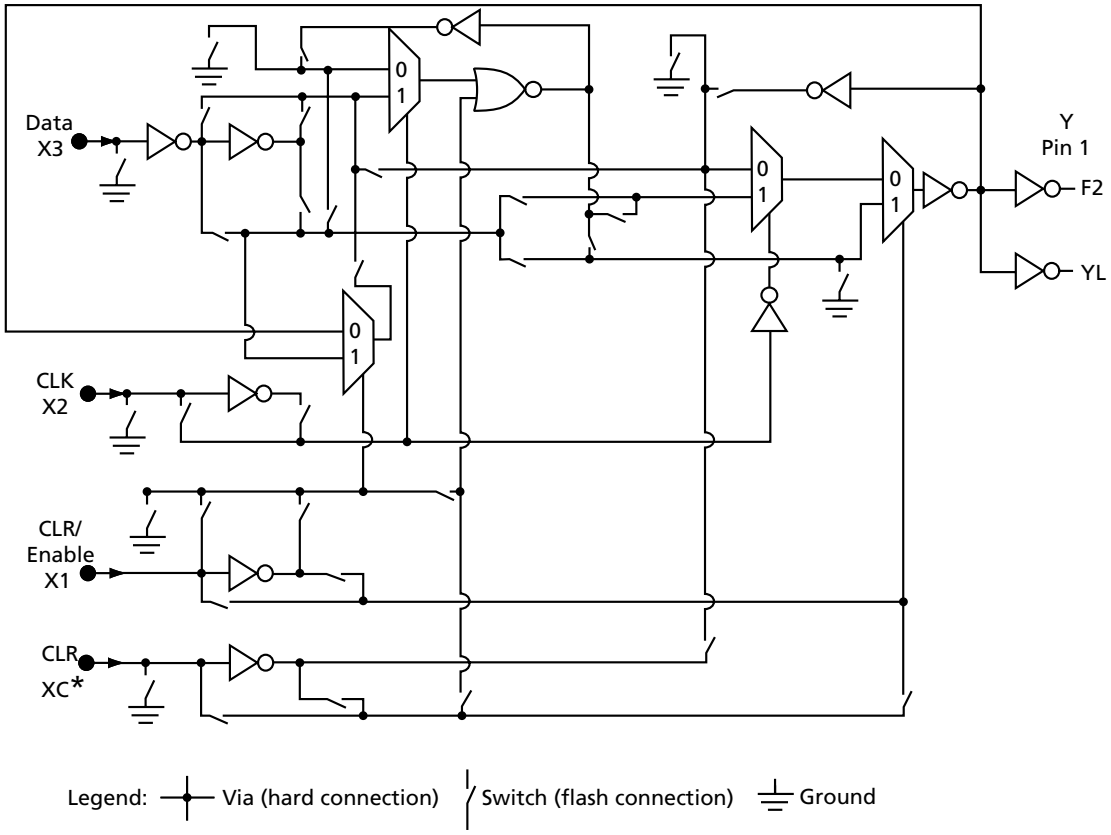
As illustrated in Figure 1-5, there are four inputs in a logic VersaTile cell, and each VersaTile can be configured using the appropriate flash switch connections:

- Any 3-input logic function
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set (on a 4th input)

VersaTiles can flexibly map the logic and sequential gates of a design. The inputs of the VersaTile can be inverted (allowing bubble pushing), and the output of the tile can connect to high-speed, very-long-line routing resources. VersaTiles and larger functions can be connected with any of the four levels of routing hierarchy.

When the VersaTile is used as an enable D-flip-flop, SET/CLR is supported by a fourth input. The SET/CLR signal can only be routed to this fourth input over the VersaNet (global) network. However, if, in the user's design, the SET/CLR signal is not routed over the VersaNet network, a compile warning message will be given, and the intended logic function will be implemented by two VersaTiles instead of one.

The output of the VersaTile is F2 when the connection is to the ultra-fast local lines, or YL when the connection is to the efficient long-line or very-long-line resources.



* *This input can only be connected to the global clock distribution network.*

Figure 1-5 • **Low-Power Flash Device Core VersaTile**

Array Coordinates

During many place-and-route operations in the Actel Designer software tool, it is possible to set constraints that require array coordinates. Table 1-2 provides array coordinates of core cells and memory blocks for ProASIC3 and IGLOO devices. Table 1-3 provides the information for IGLOO PLUS devices. The array coordinates are measured from the lower left (0, 0) They can be used in region constraints for specific logic groups/blocks, designated by a wildcard, and can contain core cells, memories, and I/Os.

I/O and cell coordinates are used for placement constraints. Two coordinate systems are needed because there is not a one-to-one correspondence between I/O cells and core cells. In addition, the I/O coordinate system changes depending on the die/package combination. It is not listed in Table 1-2. The Designer ChipPlanner tool provides the array coordinates of all I/O locations. I/O and cell coordinates are used for placement constraints. However, I/O placement is easier by package pin assignment.

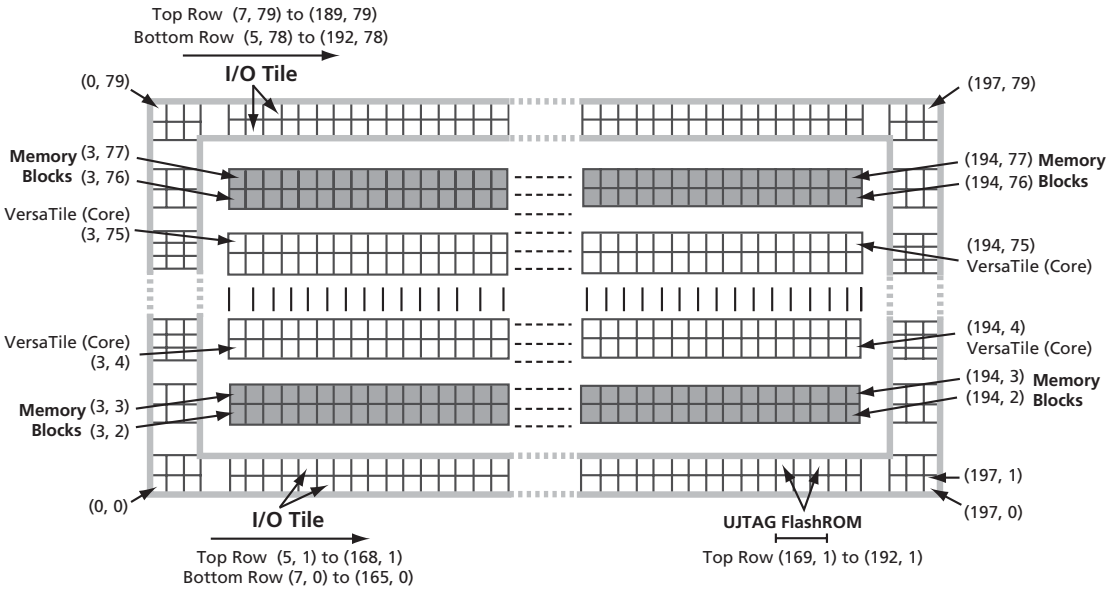
Figure 1-6 on page 1-7 illustrates the array coordinates of a 600 k gate device. For more information on how to use array coordinates for region/placement constraints, see the *Designer User's Guide* or online help (available in the software) for software tools.

Table 1-2 • **IGLOO and ProASIC3 Array Coordinates**

Device		VersaTiles				Memory Rows		Entire Die	
		Min.		Max.		Bottom	Top	Min.	Max.
ProASIC3/ ProASIC3L	**IGLOO**	**x**	**y**	**x**	**y**	**(x, y)**	**(x, y)**	**(x, y)**	**(x, y)**
A3P015	AGL015	3	2	34	13	None	None	(0, 0)	(37, 15)
A3P030	AGL030	3	3	66	13	None	None	(0, 0)	(69, 15)
A3P060	AGL060	3	2	66	25	None	(3, 26)	(0, 0)	(69, 29)
A3P125	AGL125	3	2	130	25	None	(3, 26)	(0, 0)	(133, 29)
A3P250/L	AGL250	3	2	130	49	None	(3, 50)	(0, 0)	(133, 53)
A3P400		3	2	194	49	None	(3, 50)	(0, 0)	(197, 53)
A3P600/L	AGL600	3	4	194	75	(3, 2)	(3, 76)	(0, 0)	(197, 79)
A3P1000/L	AGL1000	3	4	258	99	(3, 2)	(3, 100)	(0, 0)	(261, 103)
A3PE600	AGLE600	3	4	194	75	(3, 2)	(3, 76)	(0, 0)	(197, 79)
A3PE1500		3	4	322	123	(3, 2)	(3, 124)	(0, 0)	(325, 127)
A3PE3000/L	AGLE3000	3	6	450	173	(3, 2) or (3, 4)	(3, 174) or (3, 176)	(0, 0)	(453, 179)

Table 1-3 • **IGLOO PLUS Array Coordinates**

Device	VersaTiles				Memory Rows		Entire Die	
	Min.		Max.		Bottom	Top	Min.	Max.
IGLOO PLUS	**x**	**y**	**x**	**y**	**(x, y)**	**(x, y)**	**(x, y)**	**(x, y)**
AGLP030	2	3	67	13	None	None	(0, 0)	(69, 15)
AGLP060	2	2	67	25	None	(3, 26)	(0, 0)	(69, 29)
AGLP125	2	2	131	25	None	(3, 26)	(0, 0)	(133, 29)



Note: The vertical I/O tile coordinates are not shown. West-side coordinates are {(0, 2) to (2, 2)} to {(0, 77) to (2, 77)}; east-side coordinates are {(195, 2) to (197, 2)} to {(195, 77) to (197, 77)}.

Figure 1-6 • **Array Coordinates for AGL600, AGLE600, A3P600, and A3PE600**

Routing Architecture

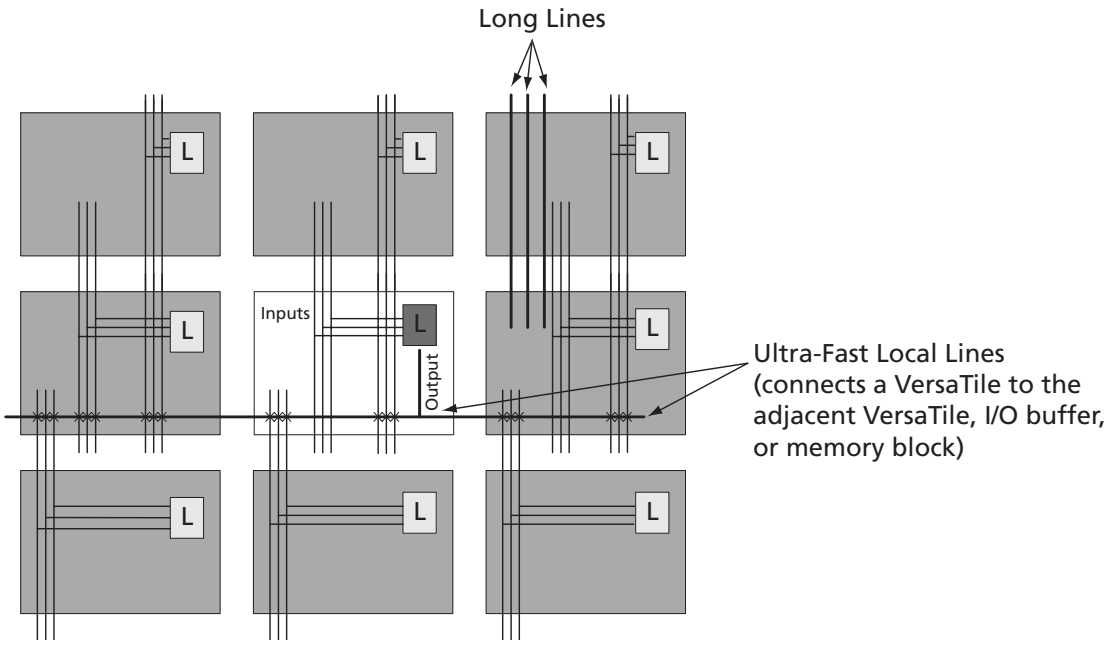
The routing structure of low-power flash devices is designed to provide high performance through a flexible four-level hierarchy of routing resources: ultra-fast local resources; efficient long-line resources; high-speed, very-long-line resources; and the high-performance VersaNet networks.

The ultra-fast local resources are dedicated lines that allow the output of each VersaTile to connect directly to every input of the eight surrounding VersaTiles (Figure 1-7 on page 1-8). The exception to this is that the SET/CLR input of a VersaTile configured as a D-flip-flop is driven only by the VersaTile global network.

The efficient long-line resources provide routing for longer distances and higher-fanout connections. These resources vary in length (spanning one, two, or four VersaTiles), run both vertically and horizontally, and cover the entire device (Figure 1-8 on page 1-9). Each VersaTile can drive signals onto the efficient long-line resources, which can access every input of every VersaTile. Routing software automatically inserts active buffers to limit loading effects.

The high-speed, very-long-line resources, which span the entire device with minimal delay, are used to route very long or high-fanout nets: length ±12 VersaTiles in the vertical direction and length ±16 in the horizontal direction from a given core VersaTile (Figure 1-9 on page 1-9). Very long lines in low-power flash devices have been enhanced over those in previous ProASIC families. This provides a significant performance boost for long-reach signals.

The high-performance VersaNet global networks are low-skew, high-fanout nets that are accessible from external pins or internal logic. These nets are typically used to distribute clocks, resets, and other high-fanout nets requiring minimum skew. The VersaNet networks are implemented as clock trees, and signals can be introduced at any junction. These can be employed hierarchically, with signals accessing every input of every VersaTile. For more details on VersaNets, refer to *Global Resources in Actel Low-Power Flash Devices.*



Note: Input to the core cell for the D-flip-flop set and reset is only available via the VersaNet global network connection.

Figure 1-7 • **Ultra-Fast Local Lines Connected to the Eight Nearest Neighbors**

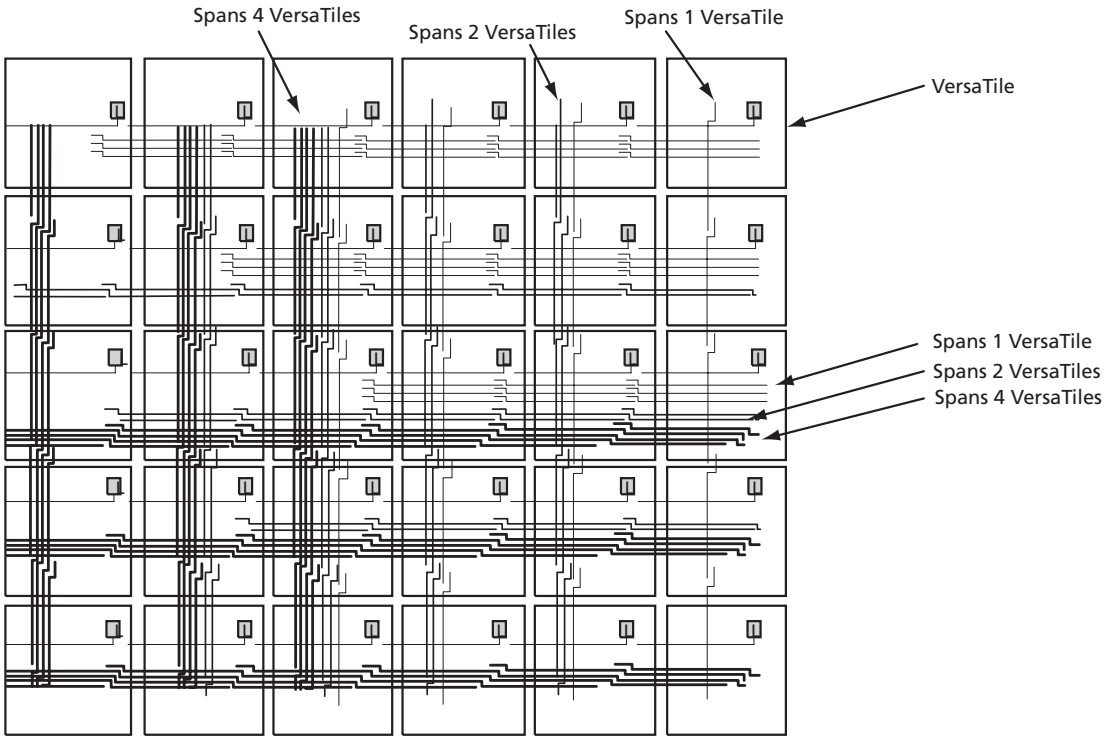


Figure 1-8 • **Efficient Long-Line Resources**

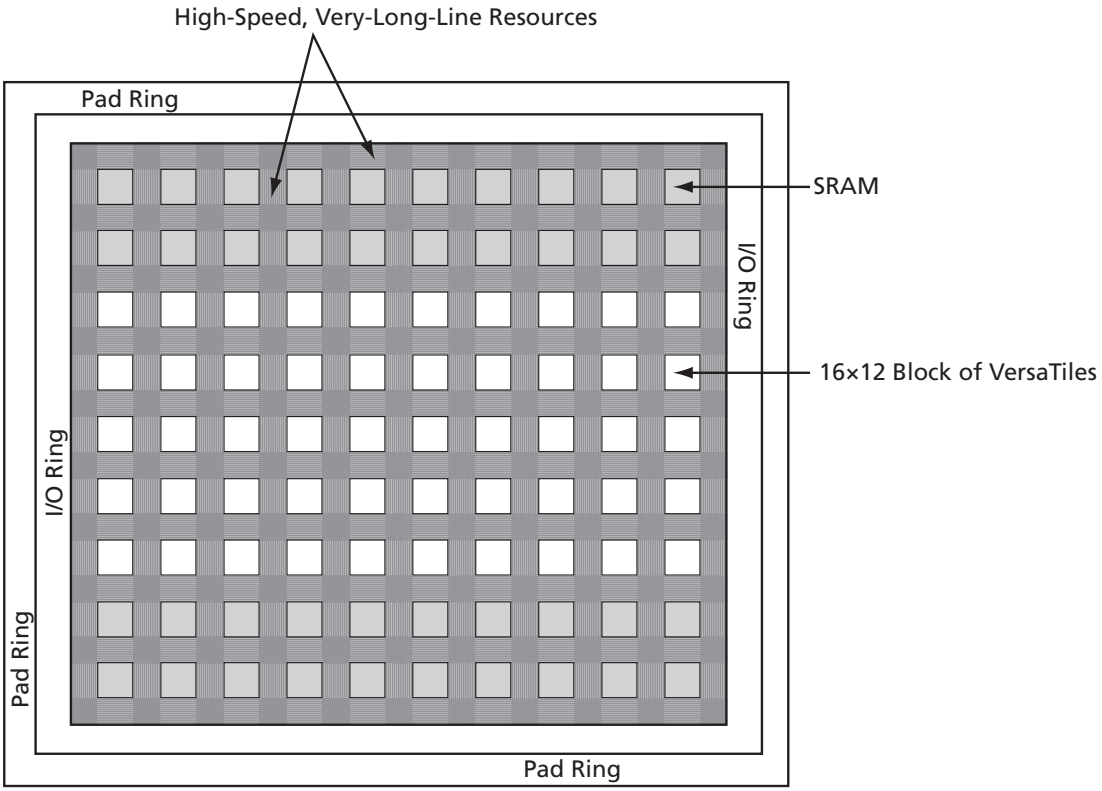


Figure 1-9 • **Very-Long-Line Resources**

Related Documents

Handbook Documents

Global Resources in Actel Low-Power Flash Devices

http://www.actel.com/documents/LPD_Glorbal_HBs.pdf

User's Guides

Designer User's Guide

http://www.actel.com/documents/designer_ug.pdf

Part Number and Revision Date

This document contains content extracted from the Device Architecture section of the datasheet. To improve usability for customers, the device architecture information has now been split into handbook sections, which also include usage information. No technical changes were made to the content unless explicitly listed.

Part Number 51700094-002-2

Revised June 2008

List of Changes

The following table lists critical changes that were made in the current version of the chapter.

Previous Version	Changes in Current Version (v1.2)	Page
v1.1 (March 2008)	The following changes were made to the family descriptions in Table 1-1 · Low-Power Flash Families: • ProASIC3L was updated to include 1.5 V. • The number of PLLs for ProASIC3E was changed from five to six.	1-2
v1.0 (January 2008)	Table 1-1 · Low-Power Flash Families and the accompanying text was updated to include the IGLOO PLUS family. The "IGLOO Terminology" section and "ProASIC3 Terminology" section are new.	1-2
	The "Device Overview" section was updated to note that 15 k devices do not support SRAM or FIFO.	1-3
	Figure 1-3 · IGLOO PLUS Device Architecture Overview with Four I/O Banks is new.	1-4
	Table 1-2 · IGLOO and ProASIC3 Array Coordinates was updated to add A3P015 and AGL015.	1-6
	Table 1-3 · IGLOO PLUS Array Coordinates is new.	1-6

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2 – Flash*Freeze Technology and Low-Power Modes in IGLOO, IGLOO PLUS, and ProASIC3L Devices

Flash*Freeze Technology and Low-Power Modes

Actel IGLOO,® IGLOO PLUS, and ProASIC®3L FPGAs with Flash*Freeze technology are designed to meet the most demanding power and area challenges of today's portable electronics products with a reprogrammable, small-footprint, full-featured flash FPGA. The IGLOO, IGLOO PLUS, and ProASIC3L families offer lower power consumption in static and dynamic modes, by utilizing the unique Flash*Freeze technology, than any other FPGA or CPLD.

IGLOO, IGLOO PLUS, and ProASIC3L devices offer various power-saving modes that enable every system to utilize modes that achieve the lowest total system power. Low-Power Active capability (static idle) allows for ultra-low power consumption while the device is operational in the system by maintaining SRAM, registers, I/Os, and logic functions.

Flash*Freeze technology provides an ultra-low-power static mode (Flash*Freeze mode) that retains all SRAM and register information with rapid recovery to Active (operating) mode. IGLOO PLUS has an additional feature when operating in Flash*Freeze mode, allowing it to retain I/O states as well as SRAM and register states. The mechanism enables the user to quickly (within 1 µs) enter and exit Flash*Freeze mode by activating the Flash*Freeze (FF) pin while all power supplies are kept in their original states. In addition, I/Os and clocks connected to the FPGA can still be driven or toggling without impact on device power consumption. While in Flash*Freeze mode, the device retains all core register states and SRAM information. This mode can be configured so that no power is consumed by the I/O banks, clocks, JTAG pins, or PLLs, and the IGLOO or IGLOO PLUS device consumes as little as 5 µW.

This document describes how to use Flash*Freeze mode and several other power-saving modes to reduce power consumption for power-conscious electronics design.

Power Conservation Techniques

IGLOO, IGLOO PLUS, and ProASIC3L FPGAs provide many ways to conserve power; however, there are also many design techniques that can be used to reduce power on the board. Actel recommends that the user tie any unused power supplies (such as V_{CCPLL}, V_{CCI}, VMV, V_{JTAG}, and V_{PUMP}) to the ground plane and leave unused I/O signals floating. Unused I/Os are configured by the software as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

Using low-voltage CMOS I/O standard signals and the lowest drive strength will reduce switching and result in lower power consumption in Active mode.

Actel's Flash Families Support the Flash*Freeze Feature

The low-power flash families listed in Table 2-1 support the Flash*Freeze feature and the functions described in this document.

Table 2-1 • **Low-Power Flash Families**

Family[1]	Description	Timing Numbers[2]
IGLOO	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*IGLOO DC and Switching Characteristics*
IGLOO PLUS	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology and enhanced I/O capabilities	*IGLOO PLUS DC and Switching Characteristics*
IGLOOe	IGLOO devices enhanced with higher density, five additional PLLs, and additional I/O standards	*IGLOOe DC and Switching Characteristics*
ProASIC3L	Low-power, high-performance 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*ProASIC3L DC and Switching Characteristics*

Notes:

1. *The family names are linked to the appropriate product brief.*
2. *The timing number links go to the relevant timing numbers in the datasheet.*

Actel's low-power flash devices (listed in Table 2-1) provide a selection of low-power, secure, live-at-power-up, single-chip solutions. The nonvolatile flash-based devices do not require a boot PROM and incorporate FlashLock® technology, which provides a unique combination of reprogrammability and design security without external overhead. Only low-power flash FPGAs can offer these advantages.

Actel IGLOO PLUS FPGAs are the industry-leading 1.2 V ultra-low-power programmable logic devices (PLDs) and consume 90% less static power and over 50% less dynamic power than PLD alternatives, while ProASIC3L devices offer a balance of low power and higher performance.

Flash*Freeze technology used in IGLOO, IGLOO PLUS, and ProASIC3L devices enables easy entry to and exit from the ultra-low power mode, which consumes as little as 5 µW, while retaining SRAM and register data. IGLOO PLUS also offers the ability to hold I/O state in Flash*Freeze mode. Flash*Freeze technology simplifies power management through I/O and clock management without the need to turn off voltages, I/Os, or clocks at the system level. Entering and exiting Flash*Freeze mode takes less than 1 µs.

IGLOO Terminology

In documentation, the term IGLOO families or IGLOO devices refers to all IGLOO families as listed in Table 2-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

ProASIC3 Terminology

In documentation, the term ProASIC3 families or ProASIC3 devices refers to all ProASIC3 families as listed in Table 2-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

Low-Power Modes Overview

Table 2-2 summarizes the low-power modes that achieve power consumption reduction when the FPGA or system is idle.

Table 2-2 • **Power Modes Summary**

Mode		V_{CCI}	V_{CC}	Core	Clocks	ULSICC Macro	To Enter Mode	To Resume Operation	Trigger
Active		On	On	On	On	N/A	Initiate clock	None	–
Static	Idle	On	On	On	Off	N/A	Stop clock	Initiate clock	External
	Flash*Freeze type 1	On	On	On	On*	N/A	Assert FF pin	Deassert FF pin	External
	Flash*Freeze type 2	On	On	On	On*	Used to enter Flash*Freeze mode	Assert FF pin and assert LSICC	Deassert FF pin	External
Sleep		On	Off	Off	Off	N/A	Shut down V_{CC}	Turn on V_{CC} supply	External
Shutdown		Off	Off	Off	Off	N/A	Shut down V_{CC} and V_{CCI} supplies	Turn on V_{CC} and V_{CCI} supplies	External

** External clocks can be left toggling while the device is in Flash*Freeze mode. Clocks generated by the embedded PLL will be turned off automatically.*

Static (Idle) Mode

In Static (Idle) mode, none of the clock inputs is switching, and static power is the only power consumed by the device. This mode can be achieved by switching off the incoming clocks to the FPGA benefitting from reduced power consumption. In addition, I/Os draw only minimal leakage current. In this mode, embedded SRAM, I/Os, and registers retain their values so the device can enter and exit this mode just by switching the clocks on or off.

If the device embedded PLL is used as the clock source, Static (Idle) mode can easily be entered by pulling LOW the PLL POWERDOWN pin (active low), which will turn off the PLL.

Flash*Freeze Mode

IGLOO, IGLOO PLUS, and ProASIC3L FPGAs offer an ultra-low static power mode to reduce power consumption while preserving the state of the registers, SRAM contents, and I/O states (IGLOO PLUS only) without switching off any power supplies, inputs, or input clocks.

Flash*Freeze technology enables the user to switch to Flash*Freeze mode within 1 µs, thus simplifying low-power design implementation. The Flash*Freeze (FF) pin (active low) is a dedicated pin used to enter or exit Flash*Freeze mode directly, or the pin can be routed internally to the FPGA core to allow the user's logic to decide if and when it is safe to transition to this mode. If the FF pin is not used, it can be used as a regular I/O.

The FF pin has a built-in glitch filter to prevent entering or exiting Flash*Freeze mode accidentally.

There are two ways to use Flash*Freeze mode.

- In Flash*Freeze type 1, entering and exiting the mode is exclusively controlled by the assertion and deassertion of the FF pin.
- In Flash*Freeze mode type 2, entering the mode is controlled by both the FF pin AND the user-defined LSICC signal available in the ULSICC macro. Exiting the mode is controlled by either the FF pin OR the user-defined LSICC signal.

Refer to Table 2-3 for Flash*Freeze (FF) pin and LSICC signal assertion and deassertion values.

Table 2-3 • **Flash*Freeze Mode Type 1 and Type 2 – Signal Assertion and Deassertion Values**

Signal	Assertion Value	Deassertion Value
Flash*Freeze (FF) pin	Logic 0	Logic 1
LSICC signal	Logic 1	Logic 0

Notes:

1. *The Flash*Freeze (FF) pin is an active-low signal, and LSICC is an active-high signal.*
2. *The LSICC signal is used only in Flash*Freeze mode type 2.*

Flash*Freeze Type 1: Control by Dedicated Flash*Freeze Pin

The device enters Flash*Freeze mode 1 µs after the dedicated FF pin is asserted (logic 0), and returns to normal operation when the FF pin is deasserted (logic 1) (Figure 2-1 on page 2-5). In this mode, FF pin assertion or deassertion is the only condition that determines entering or exiting Flash*Freeze mode after 1 µs.

In Actel Libero® Integrated Design Environment (IDE) v8.2 and before, this mode is implemented by enabling Flash*Freeze mode (default setting) in the Compile options of the Actel Designer software. To simplify usage of Flash*Freeze mode, beginning with Libero IDE v8.3 an INBUF_FF I/O buffer should be used to identify the Flash*Freeze input. Actel recommends that you switch to the new implementation.

In Libero IDE v8.3, there are two methods for implementing Flash*Freeze Type 1:

1. Using the Flash*Freeze SmartDesign core

   Select the Type 1 option from the user interface.

   Generating a design from this IP and integrating it with your design later will guarantee that you have a Type 1 design.
2. Manual instantiation of INBUF_FF

   Instantiate an INBUF_FF in your design and leave the output of INBUF_FF unconnected.

The FF pin threshold voltages are defined by V_{CCI} and the supported single-ended I/O standard in the corresponding I/O bank. Figure 2-1 shows the concept of FF pin control in Flash*Freeze mode type 1.

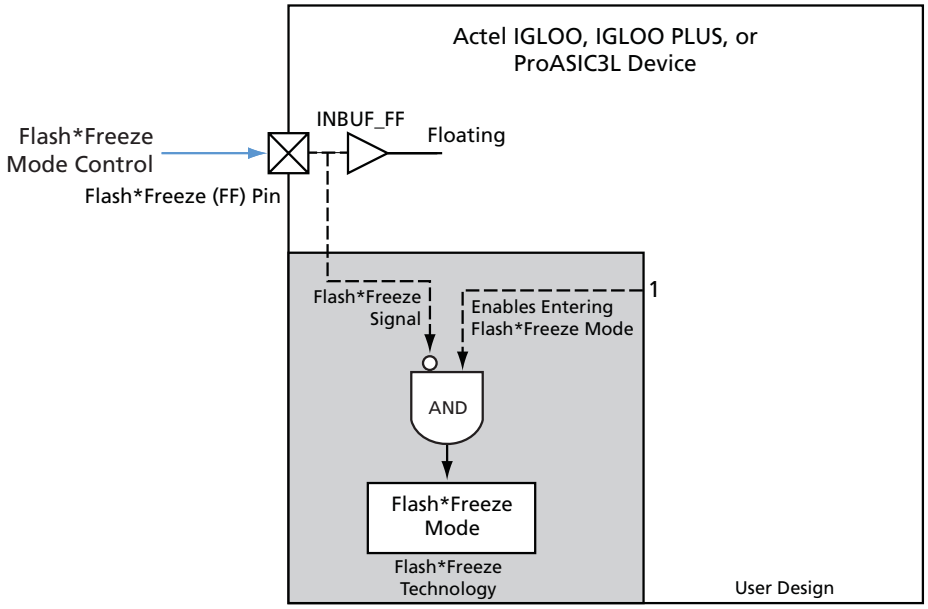

Figure 2-1 • **Flash*Freeze Mode Type 1 – Controlled by the Flash*Freeze Pin**

Figure 2-2 shows the timing diagram for entering and exiting Flash*Freeze mode type 1.

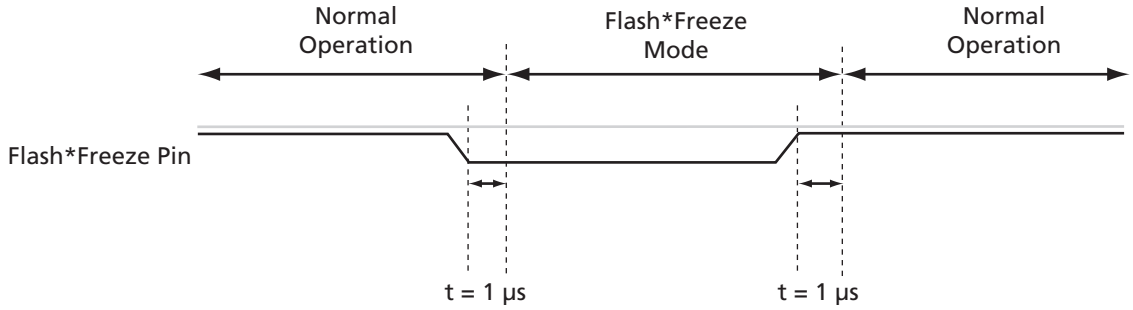

Figure 2-2 • **Flash*Freeze Mode Type 1 – Timing Diagram**

Flash*Freeze Type 2: Control by Dedicated Flash*Freeze Pin and Internal Logic

The device can enter Flash*Freeze mode by activating the FF pin together with other user-defined control logic or delay circuitry within the FPGA core (Figure 2-3 on page 2-7). This method enables the design to perform important activities before allowing the device to enter Flash*Freeze mode, such as transitioning into a safe state or completing the processing of a critical event. The device will only enter Flash*Freeze mode when the Flash*Freeze pin is asserted (logic 0) and the ULSICC macro input signal, called the LSICC signal, is asserted (logic 1). One condition is not sufficient to enter Flash*Freeze mode type 2; both the FF pin and LSICC signal must be asserted.

When Flash*Freeze type 2 is implemented in the design, the ULSICC macro needs to be instantiated by the user. There are no functional differences with the device whether the ULSICC macro is instantiated or not and whether the LSICC signal is asserted or deasserted. The LSICC signal is used only to control entering Flash*Freeze mode. Figure 2-4 on page 2-7 shows the timing diagram for entering and exiting Flash*Freeze mode type 2.

After exiting Flash*Freeze mode type 2 by deasserting the Flash*Freeze pin, the LSICC signal needs to be deasserted by the user design. This will prevent entering Flash*Freeze mode by asserting the Flash*Freeze pin only.

Type 2 Software Implementation for Libero IDE v8.2 and Earlier

Follow the steps below for Flash*Freeze type 2 implementation:

1. Enable Flash*Freeze mode (default setting) by selecting Compile in the Designer software.
2. Create a PDC file to assign the user-defined input port signal to the dedicated FF pin.

   Example: `set_io mysignal -flash_freeze "yes"`
3. Connect the user input signal to any user logic. For example, connect the delay elements of the clock conditioning circuitry or the input of the finite state machine.
4. Instantiate the ULSICC macro in the design. The ULSICC controls entering the Flash*Freeze mode by asserting (logic 1) the input of the ULSICC macro (the LSICC signal) when the FF pin is asserted (logic 0).
5. After deasserting the FF pin and exiting Flash*Freeze mode, deassert the LSICC signal (logic 0). This allows the core logic to control entry into Flash*Freeze mode type 2.

Type 2 Software Implementation for Libero IDE v8.3

There are two methods for implementing a Type 2 design:

Using a Flash*Freeze SmartDesign Core

1. Select the Type 2 option from the user interface.
2. Use advanced features of state saving and housekeeping if your design needs them (optional).

Generating a design from this IP and later integrating it with your design will guarantee that you have Type 2.

Manual Instantiation of INBUF_FF

Referring to the Flash*Freeze application note is highly recommended.

1. Instantiate INBUF_FF in your design.
2. Connect INBUF_FF to the Flash*Freeze signal that may be driving the delayed logic.
3. Instantiate the ULSCC macro.

Users can also assert the input of the LSICC signal internally during normal operation. In this case, there is no difference between Flash*Freeze mode type 1 and type 2, and the FF pin exclusively controls entering and exiting Flash*Freeze mode.

In Flash*Freeze mode type 2 operation, entering Flash*Freeze mode is done within 1 µs after asserting the last signal that triggers Flash*Freeze mode (FF pin or LSICC signal), assuming one of the signals is already asserted. In Flash*Freeze mode type 1 operation, entering Flash*Freeze mode is done within 1 µs after asserting the FF pin only.

In Flash*Freeze mode type 1 and type 2, exiting Flash*Freeze mode is done within 1 µs after deasserting the FF pin only.

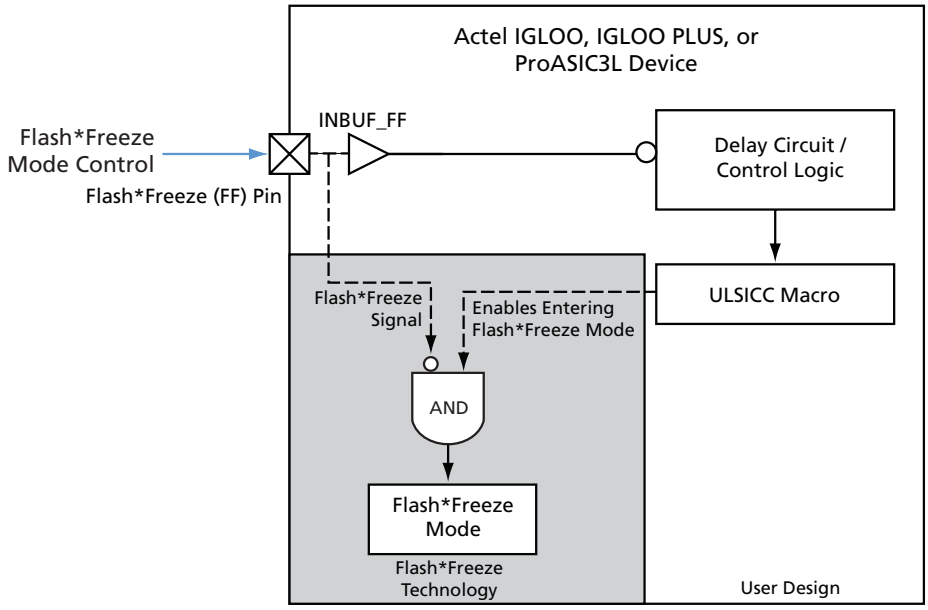

Figure 2-3 • **Flash*Freeze Mode Type 2 – Controlled by Flash*Freeze Pin and Internal Logic (LSICC signal)**

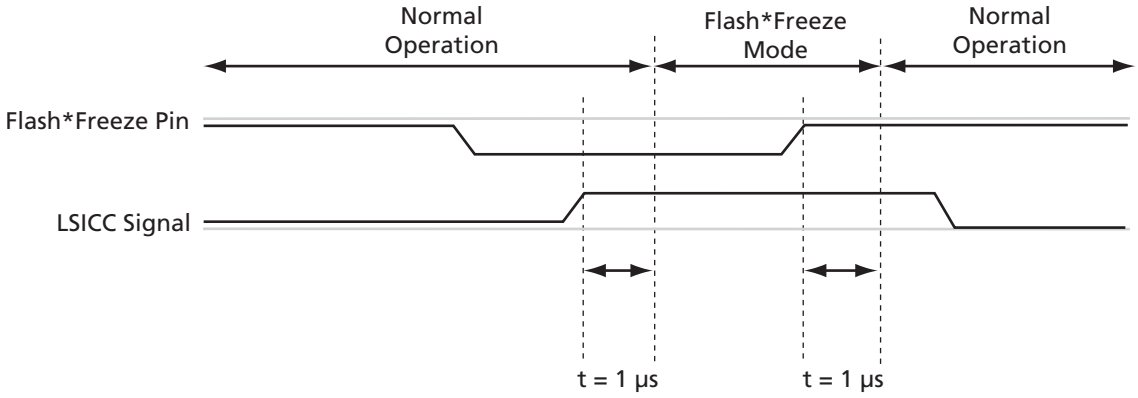

Figure 2-4 • **Flash*Freeze Mode Type 2 – Timing Diagram**

Table 2-4 summarizes the Flash*Freeze mode implementations.

Table 2-4 • **Flash*Freeze Mode Usage**

Flash*Freeze Mode Type	Description	Flash*Freeze Pin State	Instantiate ULSICC Macro	LSICC Signal	Operating Mode
1	Flash*Freeze mode is controlled only by the FF pin.	Deasserted	No	N/A	Normal operation
		Asserted	No	N/A	Flash*Freeze mode
2	Flash*Freeze mode is controlled by the FF pin and LSICC signal.	"Don't care"	Yes	Deasserted	Normal operation
		Deasserted	Yes	"Don't care"	Normal operation
		Asserted	Yes	Asserted	Flash*Freeze mode

*Note: Refer to Table 2-3 on page 2-4 for Flash*Freeze pin and LSICC signal assertion and deassertion values.*

IGLOO and ProASIC3L I/O State in Flash*Freeze Mode

In IGLOO and ProASIC3L devices, when the device enters Flash*Freeze mode, I/Os will become tristated. If the weak pull-up or pull-down feature is used, the I/Os will maintain the configured weak pull-up or pull-down status. This feature enables the design to set the I/O state to a certain level that is determined by the pull-up/-down configuration. For example, use the output buffer and enable weak pull-down to drive a signal LOW to an external component while the IGLOO device is in Flash*Freeze mode.

Table 2-5 shows the I/O pad state based on the configuration and buffer type.

Note that configuring weak pull-up or pull-down for the FF pin is not allowed. The FF pin can be configured as a Schmitt trigger input in IGLOOe devices.

Table 2-5 • **IGLOO and ProASIC3L Flash*Freeze Mode (type 1 and type 2)—I/O Pad State**

Buffer Type		Internal Weak Pull-Up/-Down	I/O Pad State in Flash*Freeze Mode
Input		Enabled	Weak pull-up/pull-down*
		Disabled	Tristate*
Output		Enabled	Weak pull-up/pull-down
		Disabled	Tristate
Tristate output buffer	E = 0 (tristate)	N/A	Tristate
	E = 1 (output)	N/A	Tristate
Bidirectional	E = 0 (input)	Enabled	Weak pull-up/pull-down*
		Disabled	Tristate*
	E = 1 (output)	Enabled	Weak pull-up/pull-down
		Disabled	Tristate

* *Internal core logic driven by this input buffer will be tied to logic 1 as long as the device is in Flash*Freeze mode.*

IGLOO PLUS I/O State in Flash*Freeze Mode

In IGLOO PLUS devices, users have multiple options on how to configure I/Os during Flash*Freeze mode:

1. Hold the previous state
2. Set to HIGH or LOW
3. Tristate

The I/O configuration must be configured by the user in the I/O Attribute Editor, and can be done on a pin-by-pin basis. The output hold feature will hold the output in the last registered state using the internal weak pull-up or pull-down resistor when the FF pin is asserted. Users can also predefine a fixed weak pull-up or pull-down value for I/Os during Flash*Freeze mode. If the weak pull-up or pull-down feature is used, the I/Os will maintain the configured weak pull-up or pull-down status. For example, use the output buffer and enable weak pull-down to drive a signal LOW to an external component while the device is in Flash*Freeze mode. In the third configuration, all I/Os will be tristated in Flash*Freeze mode.

Table 2-6 shows the I/O pad state based on the configuration and buffer type.
Note that configuring weak pull-up or pull-down for the FF pin is not allowed.

Table 2-6 • **IGLOO PLUS Flash*Freeze Mode (type 1 and type 2)—I/O Pad State**

Buffer Type		Hold State	I/O Pad Weak Pull-Up/-Down	I/O Pad State
Input		Enabled	Enabled	Weak pull-up/pull-down[2]
		Disabled	Disabled	Weak pull-up/pull-down[1]
		Enabled	Disabled	Tristate[2]
		Disabled	Disabled	Tristate[1]
Output		Enabled	Enabled	Weak pull to hold state
		Disabled	Enabled	Weak pull-up/pull-down
		Enabled	Disabled	Weak pull to hold state
		Disabled	Disabled	Tristate
Tristate output buffer	E = 0 (tristate)	N/A	N/A	Tristate
	E = 1 (output)	Enabled	Enabled	Weak pull to hold state
		Disabled	Enabled	Weak pull-up/pull-down
		Disabled	Disabled	Tristate
Bidirectional	E = 0 (input)	Enabled	Enabled	Weak pull-up/pull-down[2]
		Disabled	Enabled	Weak pull-up/pull-down[1]
		Enabled	Disabled	Tristate[2]
		Disabled	Disabled	Tristate[1]
	E = 1 (output)	Enabled	Enabled	Weak pull to hold state[3]
		Disabled	Enabled	Weak pull-up/pull-down
		Enabled	Disabled	Weak pull to hold state[3]
		Disabled	Disabled	Tristate

Notes:

1. *Internal core logic driven by this input buffer will be tied to logic 1 as long as the device is in Flash*Freeze mode.*
2. *Internal core logic driven by this input buffer will be set to the value this I/O had when entering Flash*Freeze mode.*
3. *Internal core logic driven by the input portion of the bidirectional buffer will be set to the hold state.*

Flash*Freeze Mode Design Considerations

Entering Flash*Freeze Mode

- The device was designed and optimized to enter Flash*Freeze mode only when power supplies are stable. If the device is being powered up while the FF pin is asserted (Flash*Freeze mode type 1) or both FF pin and LSICC signal are asserted (Flash*Freeze mode type 2), the device is expected to enter Flash*Freeze mode within 5 µs after the I/Os and FPGA core have reached their activation levels.
- If the device is already powered up and then the FF pin is asserted, the device will enter Flash*Freeze mode within 1 µs (type 1). In Flash*Freeze mode type 2 operation, entering Flash*Freeze mode is done within 1 µs after both FF pin and LSICC signal are asserted. Exiting Flash*Freeze mode is done within 1 µs after deasserting the FF pin only.
- If an embedded PLL is used, entering Flash*Freeze mode will automatically power down the PLL.
- The PLL output clocks will stop toggling within 1 µs after the assertion of the FF pin in type 1, or after both FF pin and LSICC signal are asserted in type 2. At the same time, I/Os will transition into the state specified in Table 2-6 on page 2-9. The user design must ensure it is safe to enter Flash*Freeze mode.

During Flash*Freeze Mode

- Inputs and input clocks to the FPGA can toggle without any impact on static power consumption, assuming weak pull-up or pull-down is not selected.
- If weak pull-up or pull-down is selected and the input is driven to the opposite direction, power dissipation will occur.
- Any toggling signals will be charging and discharging the package pin capacitance.
- IGLOO and ProASIC3L outputs will be tristated unless the I/O is configured with weak pull-up or pull-down. The output of the I/O to the FPGA core is logic HIGH (1) regardless of whether the I/O pin is configured with a weak pull-up or pull-down. Refer to Table 2-5 on page 2-8 for more information.
- IGLOO PLUS output behavior will be based on the configuration defined by the user. Refer to Table 2-6 on page 2-9 for a description of output behavior during Flash*Freeze mode.
- The JTAG circuit is active; however, JTAG operations, such as JTAG commands, JTAG bypass, programming, and authentication, cannot be executed. The device must exit Flash*Freeze mode before JTAG commands can be sent. TCK should be static to avoid extra power consumption from the JTAG state machine.
- The FF pin must be externally driven (deasserted) for the device to stay in Flash*Freeze mode.
- The FF pin is still active; i.e., the pin is used to exit Flash*Freeze mode when deasserted.

Exiting Flash*Freeze Mode

- If the embedded PLL is used, the user design must allow maximum acquisition time for the PLL to acquire the lock signal.

Sleep and Shutdown Modes

Sleep Mode

Actel IGLOO, IGLOO PLUS, and ProASIC3L FPGAs support Sleep mode when device functionality is not required. In Sleep mode, the FPGA core voltage supply (V_{CC}) is turned off (either grounded or floated) while other power supplies are left on, resulting in the FPGA core being turned off to reduce power consumption. While the device is in Sleep mode, the rest of the system can still be operating and driving the input buffers of the device. The driven inputs do not pull up the internal power planes, and the current draw is limited to minimal leakage current.

Table 2-7 shows the power supply status in Sleep mode. When the V_{CC} power supply is powered off, the corresponding power pin can be left floating or grounded.

Table 2-7 • **Sleep Mode—Power Supply Requirement for IGLOO, IGLOO PLUS, and ProASIC3L Devices**

Power Supplies	Power Supply State
V_{CC}	Powered off
V_{CCI} = VMV	Powered on
V_{JTAG}	Powered on
V_{PUMP}	Powered on

Refer to the "Power-Up/-Down Behavior" section on page 2-12 for more information about I/O states during Sleep mode and the timing diagram for entering and exiting Sleep mode.

Shutdown Mode

Shutdown mode is supported for all IGLOO PLUS, AGL015, AGL030, AGLE600, AGLE3000, and A3PE3000L devices. Shutdown mode can be used by turning off all power supplies when the device function is not needed. Cold-sparing and hot-insertion features enable these devices to be powered down without turning off the entire system. When power returns, the live-at-power-up feature enables operation of the device after reaching the voltage activation point.

Using Sleep and Shutdown Modes in the System

Depending on the power supply and the components used in an application, there are many ways to power on or off the power supplies connected to the device. For example, Figure 2-5 shows how a microprocessor can be used to control a power FET. Actel recommends that power FETs with low resistance be used to perform the switching action.

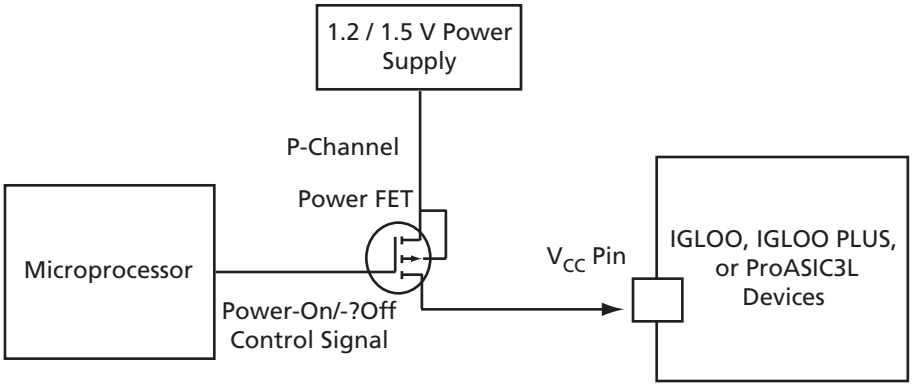

Figure 2-5 • **Controlling Power-On/-Off State Using Microprocessor and Power FET**

Figure 2-6 shows how a microprocessor can be used with a voltage regulator's shutdown pin to turn on or off the power supplies connected to the device.

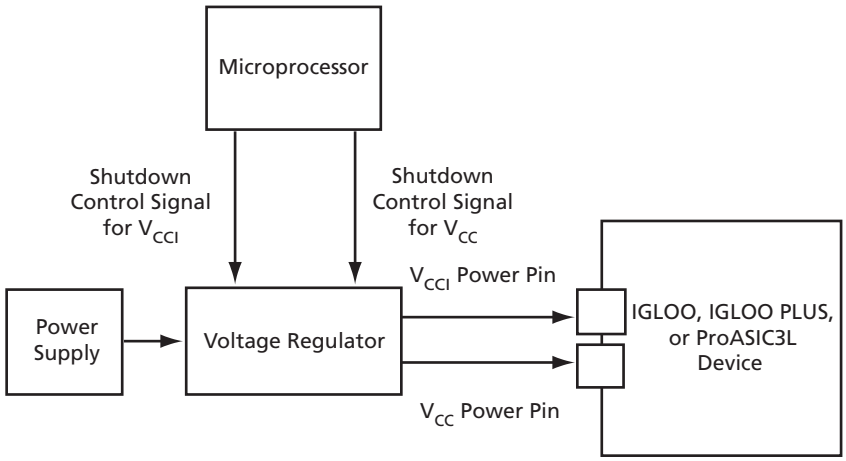

Figure 2-6 • **Controlling Power-On/-Off State Using Microprocessor and Voltage Regulator**

Power-Up/-Down Behavior

By design, all IGLOO, IGLOO PLUS, or ProASIC3L I/Os are in tristate mode before device power-up. The I/Os remain tristated until the last voltage supply (V_{CC} or V_{CCI}) is powered to its activation level. After the last supply reaches its functional level, the outputs exit the tristate mode and drive the logic at the input of the output buffer. The behavior of user I/Os is independent of the V_{CC} and V_{CCI} sequence or the state of other voltage supplies of the FPGA (V_{PUMP} and V_{JTAG}). During power-down, device I/Os become tristated once the first power supply (V_{CC} or V_{CCI}) drops below its deactivation voltage level. The I/O behavior during power-down is also independent of voltage supply sequencing.

Figure 2-7 shows a timing diagram when the V_{CC} power supply crosses the activation and deactivation trip points in a typical application when the V_{CC} power supply ramp-rate is 100 µs (ramping from 0 V to 1.5 V in this example). This is the timing diagram for the FPGA entering and exiting Sleep mode, as this function is dependent on powering V_{CC} down or up. Depending on the ramp-rate of the power supply and board-level configurations, the user can easily calculate how long it will take for the core to become inactive or active. For more information, refer to *Power-Up/-Down Behavior of Low-Power Flash Devices*.

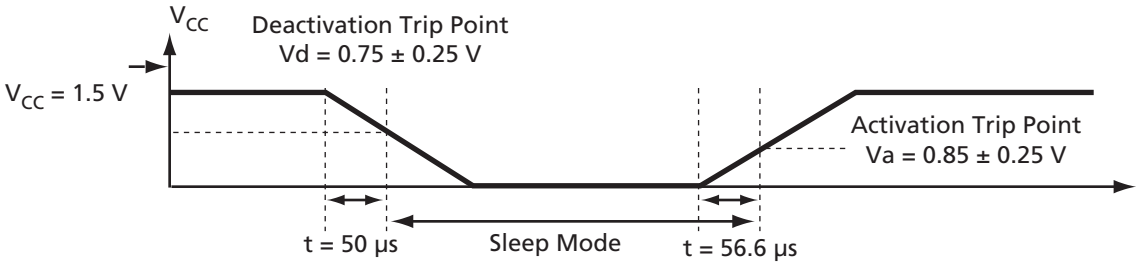

Figure 2-7 • **Entering and Exiting Sleep Mode, Typical Timing Diagram**

Context Save and Restore in Sleep or Shutdown Mode

In Sleep mode or Shutdown mode, the contents of the SRAM, state of the I/Os, and state of the registers are lost when the power is powered off if no other measure is taken. A low-cost external serial EEPROM can be used to save and restore the contents of the device when entering and exiting Sleep mode or Shutdown mode. In the *Embedded SRAM Initialization Using External Serial EEPROM* application note, detailed information and a reference design are provided for initializing the embedded SRAM using an external serial EEPROM. The user can easily customize the reference design to save and restore the FPGA state when entering and exiting Sleep mode or Shutdown mode. The microcontroller will need to manage this activity; hence, before powering down V_{CC}, the data will be read from the FPGA and stored externally. In a similar way, after the FPGA is powered up, the microcontroller will allow the FPGA to load the data from external memory and restore its original state.

Flash*Freeze Pin Locations

Refer to the *Pin Descriptions* section for information regarding Flash*Freeze pin location on the available packages. The Flash*Freeze pin location is independent of device, allowing migration to larger or smaller devices while maintaining the same pin location on the board.

Prototyping for IGLOO and ProASIC3L Devices Using ProASIC3

Prototyping in ProASIC3 does not apply for the IGLOO PLUS family. The IGLOO, ProASIC3L, and ProASIC3 families are architecturally compatible with the exception of the Flash*Freeze technology implementation and the Flash*Freeze pin available on the IGLOO and ProASIC3L devices. For example, the AGL125 user can start prototyping with the A3P125, since the devices share the same features and pinout, except for the Flash*Freeze pin. The pin in that location for ProASIC3 devices is an I/O pin.

If Flash*Freeze mode will be used in the IGLOO or ProASIC3L device, prototyping using the equivalent ProASIC3 device could implement a Flash*Freeze testing pin at the same location in the ProASIC3 package as the actual Flash*Freeze pin on the IGLOO or ProASIC3L device, as listed in Table 2-8.

You can use the Flash*Freeze testing pin on ProASIC3 devices to activate the ULSICC macro internally. Migrating to the IGLOO device is easy, as the timing of the externally controlled ULSICC macro is similar to that of the Flash*Freeze pin. Keep in mind that the activation trigger for the ULSICC macro is active high, whereas the activation trigger for the Flash*Freeze pin is active low. This means that to emulate entering Flash*Freeze mode using the ULSICC macro in a ProASIC3 device, the external signal should be inverted at the input.

If Flash*Freeze mode will not be used, the Flash*Freeze pin can still be used as a regular user I/O, making it possible to use the same PCB for both the IGLOO and ProASIC3L families. Table 2-8 provides detailed information on prototyping for IGLOO and ProASIC3L families.

Table 2-8 • **Prototyping/Migration Solutions**

Scenario	Board-Level	Software/Designer
Prototype with existing ProASIC3 devices and plan to migrate to IGLOO or ProASIC3L devices to take advantage of ultra-low power consumption. Flash*Freeze feature is not needed.	Since the Flash*Freeze pin is not used, the board layout is the same for all IGLOO and ProASIC3 families. **Note:** Use 1.5 V V_{CC} for IGLOO and ProASIC3. IGLOO and ProASIC3L can support both 1.5 V and 1.2 V core voltage. The 1.2 V core voltage results in lower power consumption.	1. *Open the ProASIC3 ADB file in Designer.* 2. *Export the netlist and PDC files.* 3. *Create a new ADB file targeting the IGLOO or ProASIC3L device and import the files created in step 2.* 4. *Run **Compile** (disable Flash*Freeze mode), run **Layout**, and perform post-layout simulation and timing analysis.*
Prototype with existing ProASIC3 devices and plan to migrate to IGLOO or ProASIC3L devices to take advantage of ultra-low power consumption. Flash*Freeze mode will be used to reduce power consumption when device function is not needed. ULSICC mode is optional.	Users must ensure the equivalent Flash*Freeze pin location is not used as a user I/O. **Note:** Use 1.5 V V_{CC} for IGLOO and ProASIC3. IGLOO and ProASIC3L can support both 1.5 V and 1.2 V core voltage. The 1.2 V core voltage results in lower power consumption.	1. *Open the ProASIC3 ADB file in Designer.* 2. *Export the netlist and PDC files.* 3. *If needed, create a PDC file to define the Flash*Freeze mode I/O state and port name for the Flash*Freeze pin.* 4. *Create a new ADB file targeting the IGLOO or ProASIC3L devices and import the files created in step 2.* 5. *Run **Compile** (enable Flash*Freeze mode), run **Layout**, and perform post-layout simulation and timing analysis.*

Note: Device migration is not supported for IGLOO PLUS devices.

Export Files

To export the netlist and constraint files from Designer, follow the steps below:

1. Export the Netlist in Designer.

   File > **Export** > **Netlist Files** > *.edn

2. Export the PDC file in Designer.

   File > **Export** > **Constraint Files** > *.pdc > select **Complete placement information** (Figure 2-8).

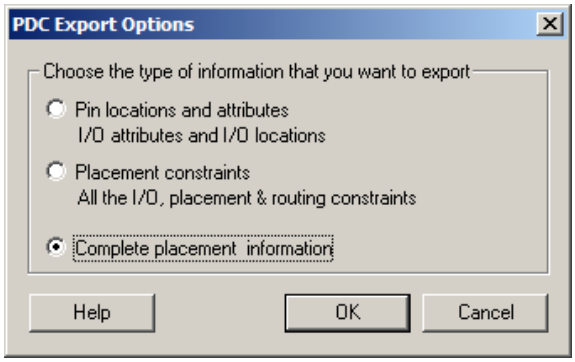

Figure 2-8 • **Export Netlist**

Table 2-9 and Table 2-10 on page 2-16 show the device-to-device and packages compatibility list.

Table 2-9 • **Device Migration—IGLOO Supported Packages in ProASIC3 Devices**

Package	A3P030 AGL030	A3P060 AGL060	A3P125 AGL125	A3P250 AGL250	A3P600 AGL600	A3P1000 AGL1000	A3PE600 AGLE600	A3PE3000 AGLE3000
QN132	✓	✓	✓	✓				
VQ100	✓	✓	✓	✓				
FG144		✓	✓	✓	✓	✓		
CS196		IGLOO/e devices only						
FG256				ProASIC3 only	✓	✓	✓	
FG484					✓	✓	✓	✓
FG896								✓

Note: Device migration is not supported for IGLOO PLUS devices.

Table 2-10 • **Device Migration—ProASIC3L Supported Packages in ProASIC3 Devices**

Package	A3P250 A3P250L	A3P600 A3P600L	A3P1000 A3P1000L	A3PE3000 A3PE3000L
VQ100	✓			
PQ208	✓	✓	✓	✓
FG144	✓	✓	✓	
FG256	✓	✓	✓	
FG324				ProASIC3L only
FG484		✓	✓	✓
FG896				✓

Note: Device migration is not supported for IGLOO PLUS devices.

Conclusion

Actel IGLOO, IGLOO PLUS, and ProASIC3L families are architected to achieve ultra-low power consumption based on enhanced nonvolatile and live-at-power-up flash-based technology. Power consumption can be reduced further by using Static —Flash*Freeze or user low Static (Idle)—Sleep, or Shutdown power modes. All these features result in a low-power, cost-effective, single-chip solution designed specifically for power-sensitive and battery-operated electronics applications.

Related Documents

Application Notes

Embedded SRAM Initialization Using External Serial EEPROM

http://www.actel.com/documents/EmbeddedSRAMInit_AN.pdf

Handbook Documents

Power-Up/-Down Behavior of Low-Power Flash Devices

http://www.actel.com/LPD_PowerUp_HBs.pdf

Pin Descriptions

http://www.actel.com/documents/LPD_PinDescriptions_HBs.pdf

Part Number and Revision Date

This document contains content extracted from the Device Architecture section of the datasheet, combined with content previously published as an application note describing features and functions of the device. To improve usability for customers, the device architecture information has now been combined with usage information to reduce duplication and possible inconsistencies in published information. No technical changes were made to the datasheet content unless explicitly listed. Changes to the application note content were made only to be consistent with existing datasheet information.

Part Number 51700094-004-3

Revised June 2008

List of Changes

The following table lists critical changes that were made in the current version of the chapter.

Previous Version	Changes in Current Version (v1.3)	Page
v1.2 (March 2008)	The family description for ProASIC3L in Table 2-1 · Low-Power Flash Families was updated to include 1.5 V.	2-2
v1.1 (February 2008)	The part number for this document was changed from 51700094-003-1 to 51700094-004-2.	N/A
	The title of the document was changed to "Flash*Freeze Technology and Low-Power Modes in IGLOO, IGLOO PLUS, and ProASIC3L Devices."	N/A
	The "Flash*Freeze Technology and Low-Power Modes" section was updated to remove the parenthetical phrase, "from 25 µW," in the second paragraph. The following sentence was added to the third paragraph: "IGLOO PLUS has an additional feature when operating in Flash*Freeze mode, allowing it to retain I/O states as well as SRAM and register states."	2-1
	The "Power Conservation Techniques" section was updated to add V_{JTAG} to the parenthetical list of power supplies that should be tied to the ground plane if unused. Additional information was added regarding how the software configures unused I/Os.	2-1
	Table 2-1 · Low-Power Flash Families and the accompanying text was updated to include the IGLOO PLUS family. The "IGLOO Terminology" section and "ProASIC3 Terminology" section are new.	2-2
	The "Flash*Freeze Mode" section was revised to include that I/O states are preserved in Flash*Freeze mode for IGLOO PLUS devices. The last sentence in the second paragraph was changed to, "If the FF pin is not used, it can be used as a regular I/O." The following sentence was added for Flash*Freeze mode type 2: "Exiting the mode is controlled by either the FF pin OR the user-defined LSICC signal."	2-4
	The "Flash*Freeze Type 1: Control by Dedicated Flash*Freeze Pin" section was revised to change instructions for implementing this mode, including instructions for implementation with Libero IDE v8.3.	2-4
	Figure 2-1 · Flash*Freeze Mode Type 1 – Controlled by the Flash*Freeze Pin was updated.	2-5
	The "Type 2 Software Implementation for Libero IDE v8.2 and Earlier" section was renamed from "Type 2 Software Implementation."	2-6
	The "Type 2 Software Implementation for Libero IDE v8.3" section is new.	2-6
	Figure 2-3 · Flash*Freeze Mode Type 2 – Controlled by Flash*Freeze Pin and Internal Logic (LSICC signal) was updated.	2-7
	Figure 2-4 · Flash*Freeze Mode Type 2 – Timing Diagram was revised to show deasserting LSICC after the device has exited Flash*Freeze mode.	2-7
	The "IGLOO PLUS I/O State in Flash*Freeze Mode" section was added to include information for IGLOO PLUS devices. Table 2-6 · IGLOO PLUS Flash*Freeze Mode (type 1 and type 2)—I/O Pad State is new.	2-8, 2-9
	The "During Flash*Freeze Mode" section was revised to include a new bullet pertaining to output behavior for IGLOO PLUS. The bullet on JTAG operation was revised to provide more detail.	2-10
	Figure 2-5 · Controlling Power-On/-Off State Using Microprocessor and Power FET and Figure 2-6 · Controlling Power-On/-Off State Using Microprocessor and Voltage Regulator were updated to include IGLOO PLUS.	2-11, 2-12

Previous Version	Changes in Current Version (v1.3)	Page
v1.1 (continued)	The first sentence of the "Shutdown Mode" section was updated to list the devices for which it is supported.	2-11
	The first paragraph of the "Power-Up/-Down Behavior" section was revised. The second sentence was changed to, "The I/Os remain tristated until the last voltage supply (V_{CC} or V_{CCI}) is powered to its activation level." The word "activation" replaced the word "functional." The sentence, "During power-down, device I/Os become tristated once the first power supply (V_{CC} or V_{CCI}) drops below its deactivation voltage level" was revised. The word "deactivation" replaced the word "brownout."	2-12
	The "Prototyping for IGLOO and ProASIC3L Devices Using ProASIC3" section was revised to state that prototyping in ProASIC3 does not apply for the IGLOO PLUS family.	2-14
	Table 2-8 · Prototyping/Migration Solutions, Table 2-9 · Device Migration—IGLOO Supported Packages in ProASIC3 Devices, and Table 2-10 · Device Migration—ProASIC3L Supported Packages in ProASIC3 Devices were updated with a table note stating that device migration is not supported for IGLOO PLUS devices.	2-14, 2-16
	The text following Table 2-10 · Device Migration—ProASIC3L Supported Packages in ProASIC3 Devices was moved to a new section: the "Flash*Freeze Pin Locations" section.	2-13
v1.0 (January 2008)	Table 2-1 · Low-Power Flash Families was updated to remove the ProASIC3, ProASIC3E, and Automotive ProASIC3 families, which were incorrectly included.	2-2
51900147-2/5.07	Detailed descriptions of low-power modes are described in the advanced datasheets. This application note was updated to describe how to use the features in an IGLOO/e application.	N/A
	Figure 2-1 · Flash*Freeze Mode Type 1 – Controlled by the Flash*Freeze Pin was updated.	2-5
	Figure 2-2 · Flash*Freeze Mode Type 1 – Timing Diagram is new.	2-5
	Steps 4 and 5 are new in the "Type 2 Software Implementation for Libero IDE v8.2 and Earlier" section.	2-6
51900147-1/3.07	In the following sentence, located in the "Flash*Freeze Mode" section, the bold text was changed from active high to active low. The Flash*Freeze pin (**active low**) is a dedicated pin used to enter or exit Flash*Freeze mode directly, or alternatively the pin can be routed internally to the FPGA core to allow the user's logic to decide if it is safe to transition to this mode.	2-4
	Figure 2-2 · Flash*Freeze Mode Type 1 – Timing Diagram was updated.	2-5
	Information about ULSICC was added to the "Prototyping for IGLOO and ProASIC3L Devices Using ProASIC3" section.	2-14
51900147-0/8.06	In the "Flash*Freeze Mode" section, "active high" was changed to "active low."	2-4
	The "Prototyping for IGLOO and ProASIC3L Devices Using ProASIC3" section was updated with information concerning the Flash*Freeze pin.	2-14

Global Resources and Clock Conditioning

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3 – Global Resources in Actel Low-Power Flash Devices

Introduction

Actel IGLOO,® Fusion, and ProASIC®3 FPGA devices offer a powerful, low-delay VersaNet global network scheme and have extensive support for multiple clock domains. In addition to the Clock Conditioning Circuits (CCCs) and phase-locked loops (PLLs), there is a comprehensive global clock distribution network called a VersaNet global network. Each logical element (VersaTile) input and output port has access to these global networks. The VersaNet global networks can be used to distribute low-skew clock signals or high-fanout nets. In addition, these highly segmented VersaNet global networks offer users the flexibility to create low-skew local networks using spines. This document describes VersaNet global networks and discusses how to assign signals to these global networks and spines in a design flow. Details concerning low-power flash device PLLs are described in *Clock Conditioning Circuits in IGLOO and ProASIC3 Devices*. This document describes the low-power flash devices' global architecture and uses of these global networks in designs.

Global Architecture

Low-power flash devices offer powerful and flexible control of circuit timing through the use of analog circuitry. Each chip has up to six CCCs, some with PLLs.

- In IGLOOe, ProASIC3EL, and ProASIC3E devices, all CCCs have PLLs—hence, 6 PLLs per device.
- In IGLOO, IGLOO PLUS, ProASIC3L, and ProASIC3 devices, the west CCC contains a PLL core (except in 15 k and 30 k devices).

Each PLL includes delay lines, a phase shifter (0°, 90°, 180°, 270°), and clock multipliers/dividers. Each CCC has all the circuitry needed for the selection and interconnection of inputs to the VersaNet global network. The east and west CCCs each have access to three VersaNet global lines on each side of the chip (six global lines total). The CCCs at the four corners each have access to three quadrant global lines in each quadrant of the chip (except in 15 k gate and 30 k gate devices).

In 15 k and 30 k gate devices, all six VersaNet global lines are driven from three southern I/Os, located toward the east and west sides. Each of these tiles can be configured to select a central I/O on its respective side or an internal routed signal as the input signal. 15 k and 30 k gate devices do not support any clock conditioning circuitry, nor do they contain the VersaNet global network concept of top and bottom spines.

The flexible use of the VersaNet global network allows the designer to address several design requirements. User applications that are clock-resource-intensive can easily route external or gated internal clocks using VersaNet global routing networks. Designers can also drastically reduce delay penalties and minimize resource usage by mapping critical, high-fanout nets to the VersaNet global network.

The following sections give an overview of the VersaNet global network, the structure of the global network, and the clock aggregation feature that enables a design to have very low clock skew using spines.

Global Resource Support in Low-Power Devices

The low-power flash families listed in Table 3-1 support the global resources and the functions described in this document.

Table 3-1 • **Low-Power Flash Families**

Family[1]	Description	Timing Numbers[2]
IGLOO	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*IGLOO DC and Switching Characteristics*
IGLOO PLUS	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology and enhanced I/O capabilities	*IGLOO PLUS DC and Switching Characteristics*
IGLOOe	IGLOO devices enhanced with higher density, five additional PLLs, and additional I/O standards	*IGLOOe DC and Switching Characteristics*
ProASIC3L	Low-power, high-performance 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*ProASIC3L DC and Switching Characteristics*
ProASIC3	Low-power, high-performance 1.5 V FPGAs	*ProASIC3 DC and Switching Characteristics*
ProASIC3E	ProASIC3 enhanced with higher density, six additional PLLs, and additional I/O standards	*ProASIC3E DC and Switching Characteristics*
ProASIC3 Automotive	Low-power, high-performance FPGAs qualified for Automotive applications	*Automotive ProASIC3 DC and Switching Characteristics*
Fusion	Low-power mixed-signal Programmable System Chip (PSC)	*Fusion DC and Power Characteristics*

Notes:

1. *The family names are linked to the appropriate product brief.*
2. *The timing number links go to the relevant timing numbers in the datasheet.*

Actel's low-power flash devices (listed in Table 3-1) provide a selection of low-power, secure, live-at-power-up, single-chip solutions. The nonvolatile flash-based devices do not require a boot PROM and incorporate FlashLock® technology, which provides a unique combination of reprogrammability and design security without external overhead. Only low-power flash FPGAs can offer these advantages.

Actel IGLOO PLUS FPGAs are the industry-leading 1.2 V ultra-low-power programmable logic devices (PLDs) and consume 90% less static power and over 50% less dynamic power than PLD alternatives, while ProASIC3L devices offer a balance of low power and higher performance.

Flash*Freeze technology used in IGLOO, IGLOO PLUS, and ProASIC3L devices enables easy entry to and exit from the ultra-low power mode, which consumes as little as 5 µW, while retaining SRAM and register data. IGLOO PLUS also offers the ability to hold I/O state in Flash*Freeze mode. Flash*Freeze technology simplifies power management through I/O and clock management without the need to turn off voltages, I/Os, or clocks at the system level. Entering and exiting Flash*Freeze mode takes less than 1 µs.

The Actel Fusion® family, based on the highly successful ProASIC3 flash FPGA architecture, has been designed as a high-performance, mixed-signal Programmable System Chip. Fusion supports many peripherals, including embedded flash memory, analog-to-digital converter (ADC), high-drive outputs, RC and crystal oscillators, and real-time counter (RTC). The total available on-chip memory, including the flash array blocks, is greater than that found in SRAM FPGAs.

IGLOO Terminology

In documentation, the term IGLOO families or IGLOO devices refers to all IGLOO families as listed in Table 3-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

ProASIC3 Terminology

In documentation, the term ProASIC3 families or ProASIC3 devices refers to all ProASIC3 families as listed in Table 3-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

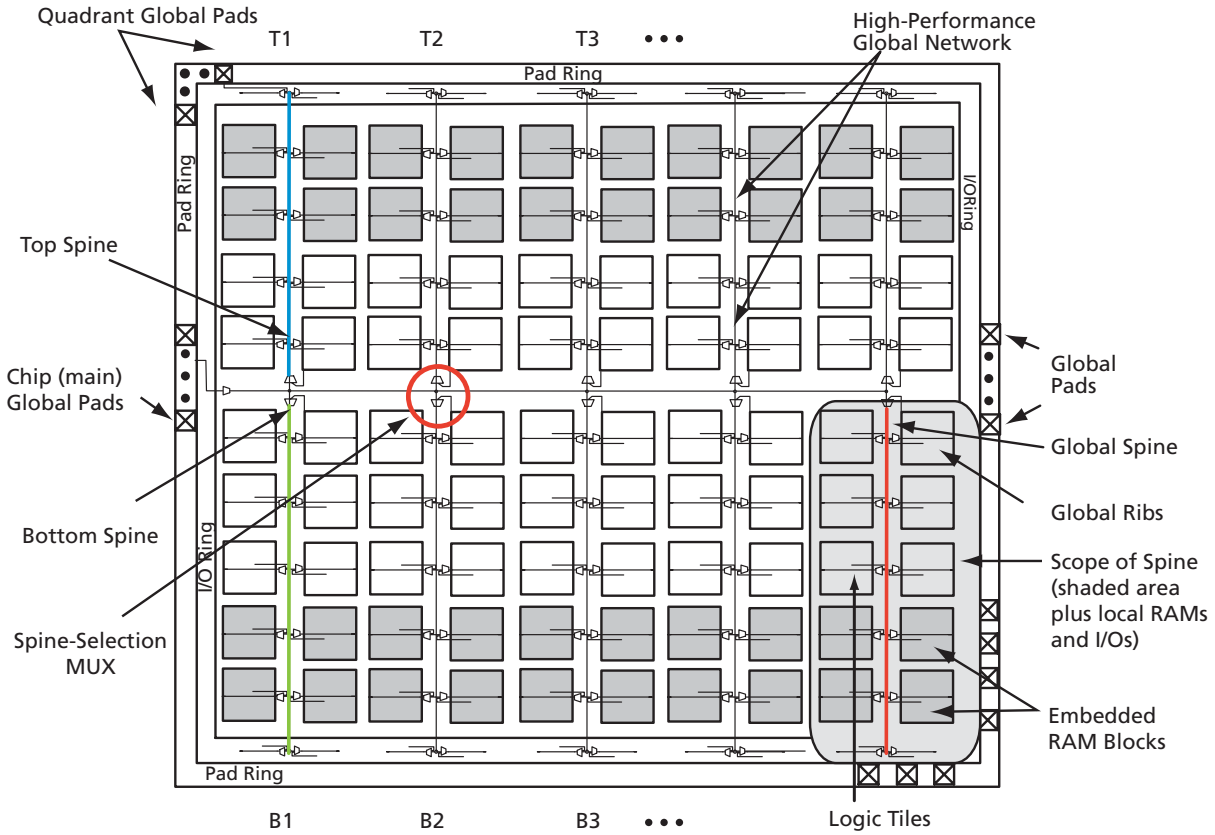
VersaNet Global Network Distribution

One of the architectural benefits of low-power flash architecture is the set of powerful, low-delay VersaNet global networks that can access the VersaTiles, SRAM, and I/O tiles of the device. Each device offers a chip global network with six global lines that are distributed from the center of the FPGA array. In addition, each device, (except the 15 k and 30 k gate device), has four quadrant global networks, each with three regional global line resources. These quadrant global networks can only drive a signal inside their own quadrant. Each core VersaTile has access to nine global line resources—three quadrant and six chip-wide (main) global networks—and a total of 18 globals are available on the device (3 × 4 regional from each quadrant and 6 global).

Figure 3-1 shows simplified device architecture, and Figure 3-2 on page 3-4 shows an overview of the VersaNet global networks.

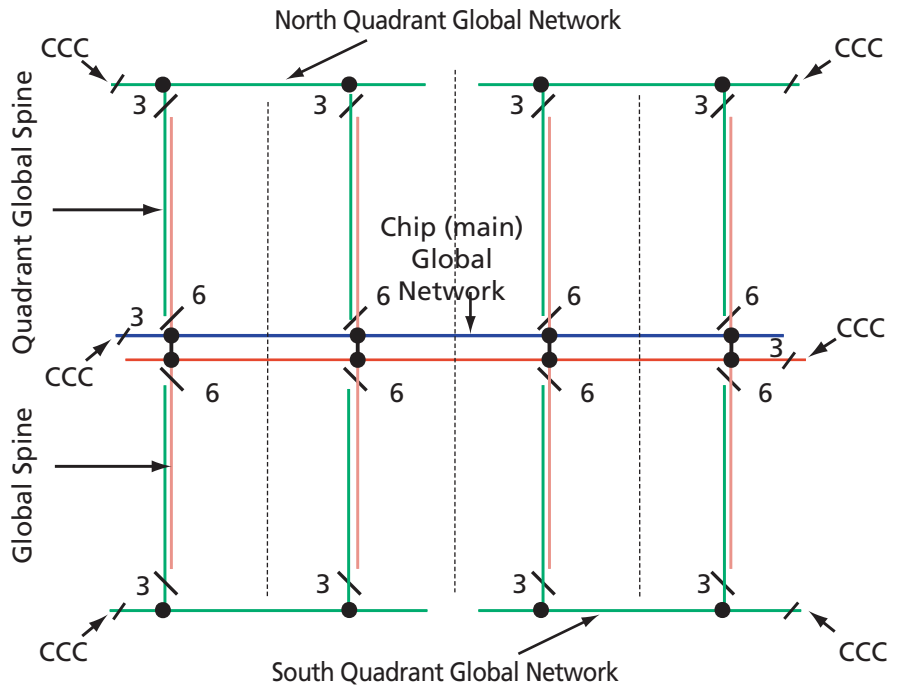
The VersaNet global networks are segmented and consist of VersaNet global networks, spines, global ribs, and global multiplexers (MUXes), as shown in Figure 3-1. The global networks are driven from the global rib at the center of the die or quadrant global networks at the north or south side of the die. The global network uses the MUX trees to access the spine, and the spine uses the clock ribs to access the VersaTile. Access is available to the chip or quadrant global networks and the spines through the global MUXes. Access to the spine using the global MUXes is explained in the "Spine Architecture" section on page 3-4.

These VersaNet global networks offer fast, low-skew routing resources for high-fanout nets, including clock signals. In addition, these highly segmented global networks offer users the flexibility to create low-skew local networks using spines for up to 252 internal/external clocks or other high-fanout nets in low-power flash devices. Optimal usage of these low-skew networks can result in significant improvement in design performance.



Note: Not applicable to 15 k and 30 k gate devices

Figure 3-1 • **Overview of VersaNet Global Network and Device Architecture**



Note: Not applicable to 15 k and 30 k gate devices.

Figure 3-2 • **Simplified VersaNet Global Network**

Spine Architecture

The low-power flash device architecture allows the VersaNet global networks to be segmented. Each of these networks contains spines (the vertical branches of the global network tree) and ribs that can reach all the VersaTiles inside its region. The nine spines available in a vertical column reside in global networks with two separate regions of scope: the quadrant global network, which has three spines, and the chip (main) global network, which has six spines. Note that there are three quadrant spines in each quadrant of the device (except in 15 k and 30 k gate devices). There are four quadrant global network regions per device. In 15 k and 30 k gate devices, there is no quadrant clock network, so there are only six spines in each spine tree. The spines are the vertical branches of the global network tree, shown in Figure 3-2.

Each spine in a vertical column of a chip (main) global network is further divided into two equal-length spine segments: one in the top and one in the bottom half of the die (except in 15 k and 30 k gate devices).

Top and bottom spine segments radiating from the center of a device have the same height. However, just as in the ProASIC$^{PLUS®}$ family, signals assigned only to the top and bottom spine cannot access the middle two rows of the die. The spines for quadrant clock networks do not cross the middle of the die and cannot access the middle two rows of the architecture.

Each spine and its associated ribs cover a certain area of the device (the "scope" of the spine; see Figure 3-2). Each spine is accessed by the dedicated global network MUX tree architecture, which defines how a particular spine is driven—either by the signal on the global network from a CCC, for example, or by another net defined by the user. Details of the chip (main) global network spine-selection MUX are presented in Figure 3-4 on page 3-7. The spine drivers for each spine are located in the middle of the die.

Quadrant spines can be driven from user I/Os on the north and south sides of the die. The ability to drive spines in the quadrant global networks can have a significant effect on system performance for high-fanout inputs to a design. Access to the top quadrant spine regions is from the top of the die, and access to the bottom quadrant spine regions is from the bottom of the die. The A3PE3000 device has 28 clock trees and each tree has nine spines; this flexible global network architecture enables users to map up to 252 different internal/external clocks in an A3PE3000 device.

Table 3-2 • **Globals/Spines/Rows for IGLOO and ProASIC3 Devices**

ProASIC3/ ProASIC3L Devices	IGLOO Devices	Chip Globals	Quadrant Globals (4×3)	Clock Trees	Globals/ Spines per Tree	Total Spines per Device	VersaTiles in Each Tree	Total VersaTiles	Rows in Each Spine
A3P015	AGL015	6	0	1	9	9	384	384	12
A3P030	AGL030	6	0	2	9	18	384	768	12
A3P060	AGL060	6	12	4	9	36	384	1,536	12
A3P125	AGL125	6	12	8	9	72	384	3,072	12
A3P250/L	AGL250	6	12	8	9	72	768	6,144	24
A3P400		6	12	12	9	108	768	9,216	24
A3P600/L	AGL600	6	12	12	9	108	1,152	13,824	36
A3P1000/L	AGL1000	6	12	16	9	144	1,536	24,576	48
A3PE600	AGLE600	6	12	12	9	108	1,120	13,440	35
A3PE1500		6	12	20	9	180	1,888	37,760	59
A3PE3000/L	AGLE3000	6	12	28	9	252	2,656	74,368	83

Table 3-3 • **Globals/Spines/Rows for IGLOO PLUS Devices**

IGLOO PLUS Devices	Chip Globals	Quadrant Globals (4×3)	Clock Trees	Globals/ Spines per Tree	Total Spines per Device	VersaTiles in Each Tree	Total VersaTiles	Rows in Each Spine
AGLP030	6	0	2	9	18	384*	792	12
AGLP060	6	12	4	9	36	384*	1,584	12
AGLP125	6	12	8	9	72	384*	3,120	12

*Note: *Clock trees that are located at far left and far right will support more VersaTiles.*

Table 3-4 • **Globals/Spines/Rows for Fusion Devices**

Fusion Device	Chip Globals	Quadrant Globals (4×3)	Clock Trees	Globals/ Spines per Tree	Total Spines per Device	VersaTiles in Each Tree	Total VersaTiles	Rows in Each Spine
AFS090	6	12	6	9	54	384	2,304	12
AFS250	6	12	8	9	72	768	6,144	24
AFS600	6	12	12	9	108	1,152	13,824	36
AFS1500	6	12	20	9	180	1,920	38,400	60

Spine Access

The physical location of each spine is identified by the letter 'T' (top) or 'B' (bottom) and an accompanying number (T*n* or B*n*). The number *n* indicates the horizontal location of the spine; 1 refers to the first spine on the left side of the die. Since there are six chip spines in each spine tree, there are up to six spines available for each combination of 'T' (or 'B') and *n* (for example, six T1 spines). Similarly, there are three quadrant spines available for each combination of 'T' (or 'B') and *n* (for example, four T1 spines), as shown in Figure 3-3 on page 3-6.

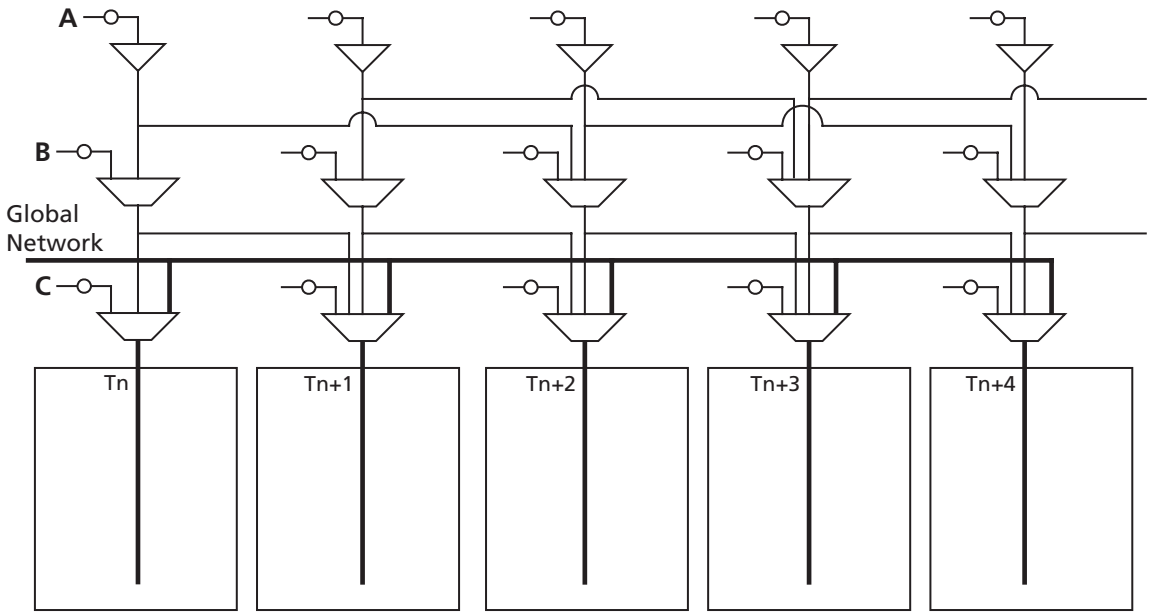


Figure 3-3 • **Chip Global Aggregation**

Spines are also called local clocks, and are accessed by the dedicated global MUX architecture. These MUXes define how a particular spine is driven. Refer to Figure 3-4 on page 3-7 for the global MUX architecture. The MUXes for each chip global spine are located in the middle of the die. Access to the top and bottom chip global spine is available from the middle of the die. There is no control dependency between the top and bottom spines. If a top spine, T1, of a chip global network is assigned to a net, B1 is not wasted and can be used by the global clock network. The signal assigned only to the top or bottom spine cannot access the middle two rows of the architecture. However, if a spine is using the top and bottom at the same time (T1 and B1, for instance), the previous restriction is lifted.

The MUXes for each quadrant global spine are located in the north and south sides of the die. Access to the top and bottom quadrant global spines is available from the north and south sides of the die. Since the MUXes for quadrant spines are located in the north and south sides of the die, you should not try to drive T1 and B1 quadrant spines from the same signal.

Using Clock Aggregation

Clock aggregation allows for multi-spine clock domains to be assigned using hardwired connections, without adding any extra skew. A MUX tree, shown in Figure 3-4, provides the necessary flexibility to allow long lines, local resources, or I/Os to access domains of one, two, or four global spines. Signal access to the clock aggregation system is achieved through long-line resources in the central rib in the center of the die, and also through local resources in the north and south ribs, allowing I/Os to feed directly into the clock system. As Figure 3-5 indicates, this access system is contiguous.

There is no break in the middle of the chip for the north and south I/O VersaNet access. This is different from the quadrant clocks located in these ribs, which only reach the middle of the rib.

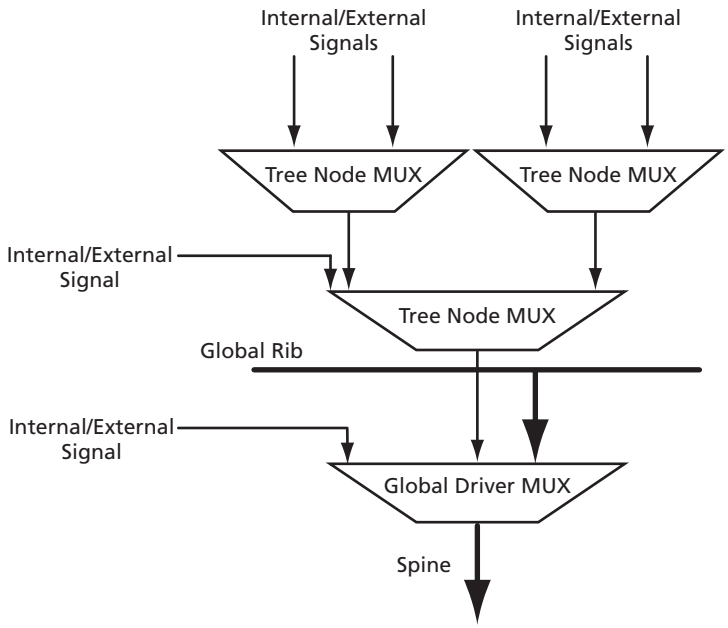


Figure 3-4 • **Spine Selection MUX of Global Tree**

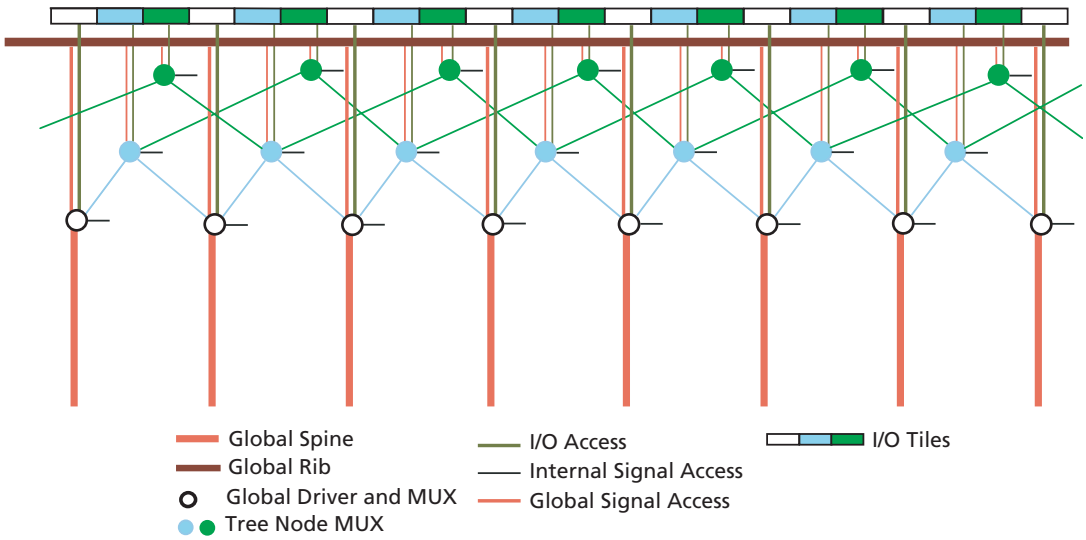


Figure 3-5 • **Clock Aggregation Tree Architecture**

Clock Aggregation Architecture

This clock aggregation feature allows a balanced clock tree, which improves clock skew. The physical regions for clock aggregation are defined from left to right and shift by one spine. For chip global networks, there are three types of clock aggregation available, as shown in Figure 3-6:

- Long lines that can drive up to four adjacent spines
- Long lines that can drive up to two adjacent spines
- Long lines that can drive one spine

There are three types of clock aggregation available for the quadrant spines, as shown in Figure 3-6:

- I/Os or local resources that can drive up to four adjacent spines
- I/Os or local resources that can drive up to two adjacent spines
- I/Os or local resources that can drive one spine
- As an example, A3PE600 and AFS600 devices have twelve spine locations: T1, T2, T3, T4, T5, T6, B1, B2, B3, B4, B5, and B6. Table 3-5 shows the clock aggregation you can have in A3PE600 and AFS600.

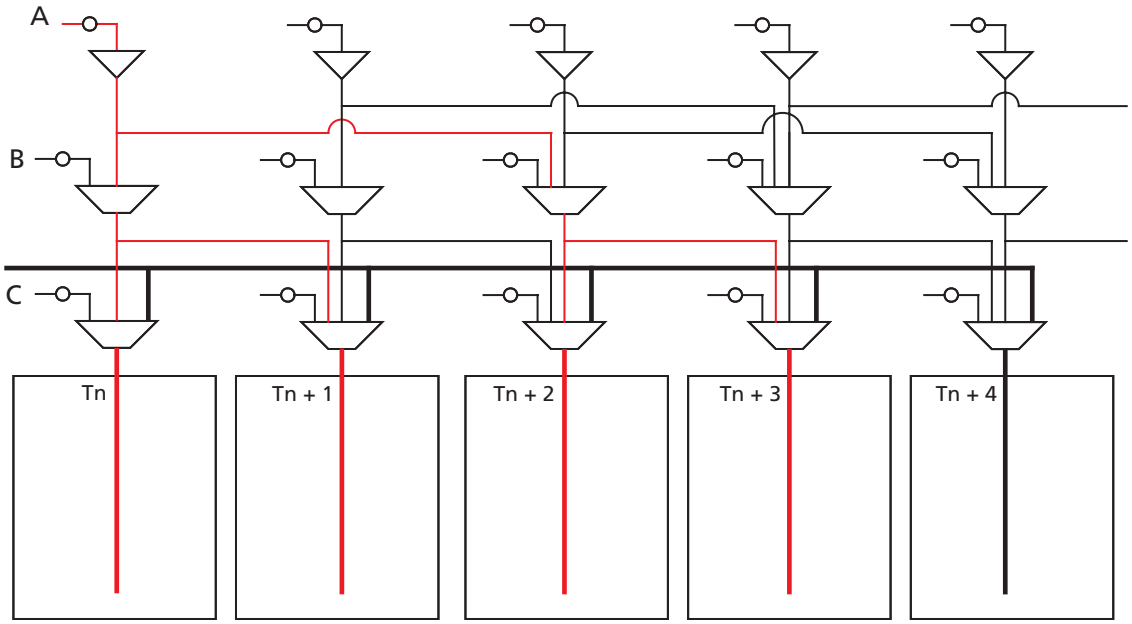


Figure 3-6 • **Four Spines Aggregation**

Table 3-5 • **Spine Aggregation in A3PE600 or AFS600**

Clock Aggregation	Spine
1 spine	T1, T2, T3, T4, T5, T6, B1, B2, B3, B4, B5, B6
2 spines	T1:T2, T2:T3, T3:T4, T4:T5, T5:T6, B1:B2, B2:B3, B3:B4, B4:B5, B5:B6
4 spines	B1:B4, B2:B5, B3:B6, T1:T4, T2:T5, T3:T6

The clock aggregation for the quadrant spines can cross over from the left to right quadrant, but not from top to bottom. The quadrant spine assignment T1:T4 is legal, but the quadrant spine assignment T1:B1 is not legal. Note that this clock aggregation is hardwired. You can always assign signals to spine T1 and B2 by instantiating a buffer, but this may add skew in the signal.

I/O Banks and Global I/Os

The following sections give an overview of naming conventions and other related I/O information.

Naming of Global I/Os

In low-power flash devices, the global I/Os have access to certain clock conditioning circuitry and have direct access to the global network. Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities to those of regular I/Os. Due to the comprehensive and flexible nature of the I/Os in low-power flash devices, a naming scheme is used to show the details of the I/O. The global I/O uses the generic name Gmn/IOuxwByVz. Refer to the I/O Structure section of the handbook for the device that you are using for more information on this naming convention.

Figure 3-7 represents the global input pins connection to the northwest CCC or northwest quadrant global networks for a low-power flash device. Each global buffer, as well as the PLL reference clock, can be driven from one of the following:

- 3 dedicated single-ended I/Os using a hardwired connection
- 2 dedicated differential I/Os using a hardwired connection
- The FPGA core

Since each bank can have a different I/O standard, the user should be careful to choose the correct global I/O for the design. There are 54 global pins available to access 18 global networks. For the single-ended and voltage-referenced I/O standards, you can use any of these three available I/Os to access the global network. For differential I/O standards such as LVDS and LVPECL, the I/O macro needs to be placed on GAA0 and GAA1 or a similar location. The unassigned global I/Os can be used as regular I/Os. Note that pin names starting with GF and GC are associated with the chip global networks, and GA, GB, GD, and GE are used for quadrant global networks.

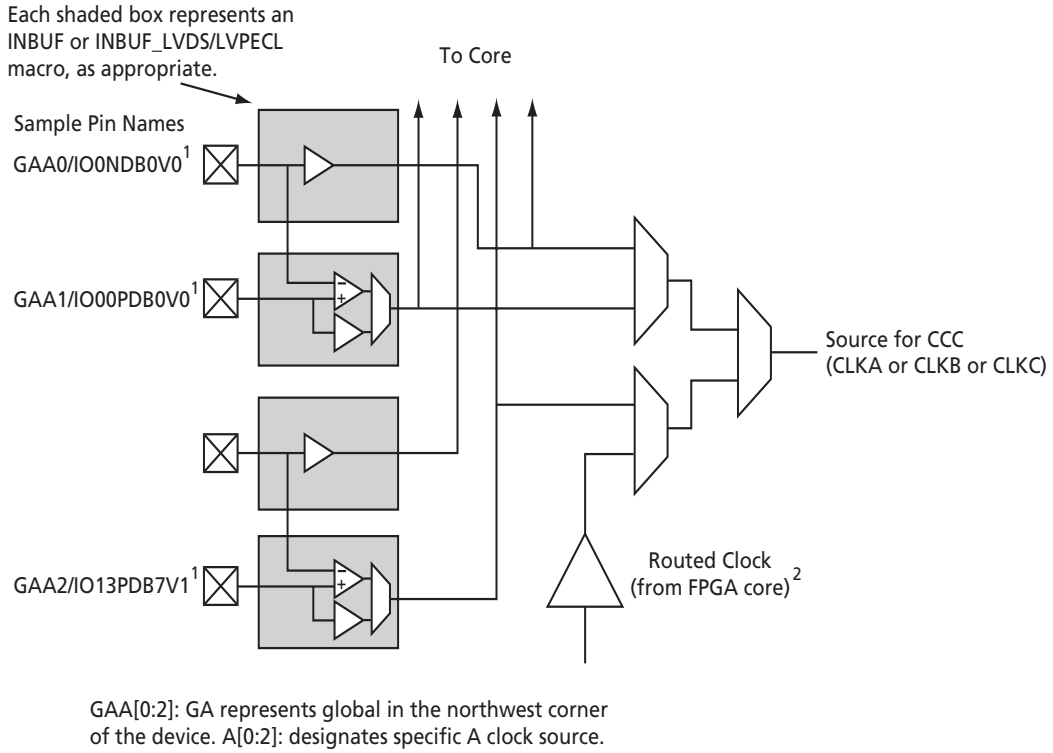


Figure 3-7 • **Global I/O Overview**

Unused Global I/O Configuration

The unused clock inputs behave similarly to the unused Pro I/Os. The Actel Designer software automatically configures the unused global pins as inputs with pull-up resistors if they are not used as regular I/O.

I/O Banks and Global I/O Standards

In low-power flash devices, any I/O or internal logic can be used to drive the global network. However, only the global macro placed at the global pins will use the hardwired connection between the I/O and global network. Global signal (signal driving a global macro) assignment to I/O banks is no different from regular I/O assignment to I/O banks with the exception that you are limited to the pin placement location available. Only global signals compatible with both the V_{CCI} and V_{REF} standards can be assigned to the same bank.

Design Recommendations

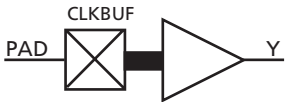
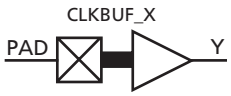
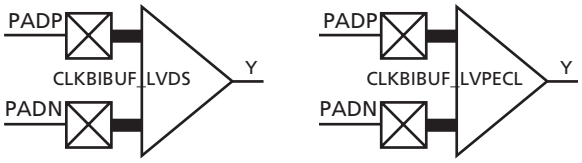
The following sections provide design flow recommendations for using a global network in a design.

- "Global Macros and I/O Standards"
- "Using Global Macros in Synplicity" on page 3-12
- "Global Promotion and Demotion Using PDC" on page 3-13
- "Spine Assignment" on page 3-14
- "Designer Flow for Global Assignment" on page 3-15
- "Simple Design Example" on page 3-17
- "Global Management in PLL Design" on page 3-19
- "Using Spines of Occupied Global Networks" on page 3-20

Global Macros and I/O Standards

Low-power flash devices have six chip global networks and four quadrant clock networks. However, the same clock macros are used for assigning signals to chip globals and quadrant globals. Depending on the clock macro placement or assignment in the Physical Design Constraint (PDC) file or MultiView Navigator (MVN), the signal will use the chip global network or quadrant network. Table 3-6 on page 3-11 lists the clock macros available for low-power flash devices. Refer to the *IGLOO, Fusion and ProASIC3 Macro Library Guide* for details.

Table 3-6 • **Clock Macros**

Macro Name	Description	Symbol
CLKBUF	Input macro for Clock Network	
CLKBUF_x	Input macro for Clock Network with specific I/O standard	
CLKBUF_LVDS/ LVPECL	LVDS or LVPECL input macro for Clock Network	
CLKINT	Internal clock interface	
CLKBIBUF	Bidirectional macro with input dedicated to routed Clock Network	

Use these available macros to assign a signal to the global network. In addition to these global macros, PLL and CLKDLY macros can also drive the global networks. Use I/O–standard–specific clock macros (CLKBUF_x) to instantiate a specific I/O standard for the global signals. Table 3-7 shows the list of these I/O–standard–specific macros. Note that if you use these I/O–standard–specific clock macros, you cannot change the I/O standard later in the design stage. If you use the regular CLKBUF macro, you can use MVN or the PDC file in Designer to change the I/O standard. The default I/O standard for CLKBUF is LVTTL in the current Actel Libero® Integrated Design Environment (IDE) and Designer software.

Table 3-7 • **I/O Standards within CLKBUF**

Name	Description
CLKBUF_LVCMOS5	LVCMOS clock buffer with 5.0 V CMOS voltage level
CLKBUF_LVCMOS33	LVCMOS clock buffer with 3.3 V CMOS voltage level
CLKBUF_LVCMOS25	LVCMOS clock buffer with 2.5 V CMOS voltage level[1]
CLKBUF_LVCMOS18	LVCMOS clock buffer with 1.8 V CMOS voltage level
CLKBUF_LVCMOS15	LVCMOS clock buffer with 1.5 V CMOS voltage level
CLKBUF_LVCMOS12	LVCMOS clock buffer with 1.2 V CMOS voltage level
CLKBUF_PCI	PCI clock buffer
CLKBUF_PCIX	PCIX clock buffer
CLKBUF_GTL25	GTL clock buffer with 2.5 V CMOS voltage level[1]
CLKBUF_GTL33	GTL clock buffer with 3.3 V CMOS voltage level[1]

Notes:

1. *Supported in only the IGLOOe and ProASIC3E devices*
2. *By default, the CLKBUF macro uses the 3.3 V LVTTL I/O technology.*

Table 3-7 • **I/O Standards within CLKBUF (continued)**

Name	Description
CLKBUF_GTLP25	GTL+ clock buffer with 2.5 V CMOS voltage level[1]
CLKBUF_GTLP33	GTL+ clock buffer with 3.3 V CMOS voltage level[1]
CLKBUF_ HSTL _I	HSTL Class I clock buffer[1]
CLKBUF_ HSTL _II	HSTL Class II clock buffer[1]
CLKBUF_SSTL2_I	SSTL2 Class I clock buffer[1]
CLKBUF_SSTL2_II	SSTL2 Class II clock buffer[1]
CLKBUF_SSTL3_I	SSTL3 Class I clock buffer[1]
CLKBUF_SSTL3_II	SSTL3 Class II clock buffer[1]

Notes:

1. *Supported in only the IGLOOe and ProASIC3E devices*
2. *By default, the CLKBUF macro uses the 3.3 V LVTTL I/O technology.*

The current synthesis tool libraries only infer the CLKBUF or CLKINT macros in the netlist. All other global macros must be instantiated manually into your HDL code. The following is an example of CLKBUF_LVCMOS25 global macro instantiations that you can copy and paste into your code:

VHDL

```
component clkbuf_lvcmos25
  port (pad : in std_logic; y : out std_logic);
end component

begin
-- concurrent statements
u2 : clkbuf_lvcmos25 port map (pad =>  ext_clk, y => int_clk);
end
```

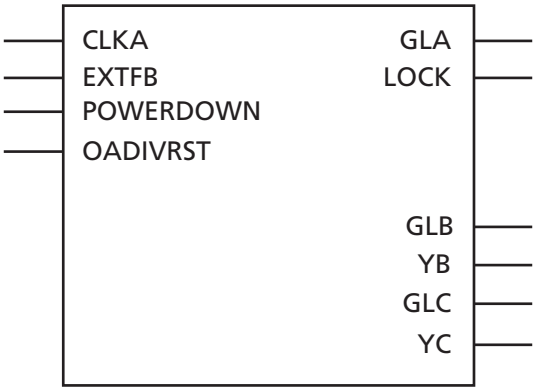
Verilog

```
module design (______);

input _____;
output ______;

clkbuf_lvcmos25 u2 (.y(int_clk), .pad(ext_clk);

endmodule
```

Using Global Macros in Synplicity

The Synplify® synthesis tool automatically inserts global buffers for nets with high fanout during synthesis. By default, Synplicity® puts six global macros (CLKBUF or CLKINT) in the netlist, including any global instantiation or PLL macro. Synplify always honors your global macro instantiation. If you have a PLL (only primary output is used) in the design, Synplify adds five more global buffers in the netlist. Synplify uses the following global counting rule to add global macros in the netlist:

1. CLKBUF: 1 global buffer
2. CLKINT: 1 global buffer
3. CLKDLY: 1 global buffer
4. PLL: 1 to 3 global buffers
   - GLA, GLB, GLC, YB, and YC are counted as 1 buffer.
   - GLB or YB is used or both are counted as 1 buffer.
   - GLC or YC is used or both are counted as 1 buffer.



Note: OAVDIVRST exists only in the Fusion PLL.

Figure 3-8 • **PLLs in Low-Power Flash Devices**

You can use the syn_global_buffers attribute in Synplify to specify a maximum number of global macros to be inserted in the netlist. This can also be used to restrict the number of global buffers inserted. In the Synplicity 8.1 version, a new attribute, syn_global_minfanout, has been added for low-power flash devices. This enables you to promote only the high-fanout signal to global. However, be aware that you can only have six signals assigned to chip global networks, and the rest of the global signals should be assigned to quadrant global networks. So, if the netlist has 18 global macros, the remaining 12 global macros should have fanout that allows the instances driven by these globals to be placed inside a quadrant.

Global Promotion and Demotion Using PDC

The HDL source file or schematic is the preferred place for defining which signals should be assigned to a clock network using clock macro instantiation. This method is preferred because it is guaranteed to be honored by the synthesis tools and Designer software and stop any replication on this net by the synthesis tool. Note that a signal with fanout may have logic replication if it is not promoted to global during synthesis. In that case, the user cannot promote that signal to global using PDC. See Synplicity Help for details on using this attribute. To help you with global management, Designer allows you to promote a signal to a global network or demote a global macro to a regular macro from the user netlist using the compile options and/or PDC commands.

The following are the PDC constraints you can use to promote a signal to a global network:

1. PDC syntax to promote a regular net to a chip global clock:

   ```
   assign_global_clock –net netname
   ```

   The following will happen during promotion of a regular signal to a global network:

   – If the net is external, the net will be driven by a CLKINT inserted automatically by Compile.
   – The I/O macro will not be changed to CLKBUF macros.
   – If the net is an internal net, the net will be driven by a CLKINT inserted automatically by Compile.

2. PDC syntax to promote a net to a quadrant clock:

   ```
   assign_local_clock –net netname –type quadrant UR|UL|LR|LL
   ```

   This follows the same rule as the chip global clock network.

The following PDC command demotes the clock nets to regular nets.

```
unassign_global_clock -net netname
```

The following will happen during demotion of a global signal to regular nets:

- CLKBUF_x becomes INBUF_x; CLKINT is removed from the netlist.
- The essential global macro, such as the output of the Clock Conditioning Circuit, cannot be demoted.
- No automatic buffering will happen.

Since no automatic buffering happens when a signal is demoted, this net may have a high delay due to large fanout. This may have a negative effect on the quality of the results. Actel recommends that the automatic global demotion only be used on small-fanout nets. Use clock networks for high-fanout nets to improve timing and routability.

Spine Assignment

The low-power flash device architecture allows the global networks to be segmented and used as clock spines. These spines, also called local clocks, enable the use of PDC or MVN to assign a signal to a spine.

PDC syntax to promote a net to a spine/local clock:

```
assign_local_clock –net netname –type [quadrant|chip] Tn|Bn|Tn:Bm
```

If the net is driven by a clock macro, Designer automatically demotes the clock net to a regular net before it is assigned to a spine. Nets driven by a PLL or CLKDLY macro cannot be assigned to a local clock.

When assigning a signal to a spine or quadrant global network using PDC (pre-compile), the Designer software will legalize the shared instances. The number of shared instances to be legalized can be controlled by compile options. If these networks are created in MVN (only quadrant globals can be created), no legalization is done (as it is post-compile). Designer does not do legalization between non-clock nets.

As an example, consider two nets, net_clk and net_reset, driving the same flip-flop. The following PDC constraints are used:

```
assign_local_clock –net net_clk –type chip T3
assign_local_clock –net net_reset –type chip T1:T2
```

During Compile, Designer adds a buffer in the reset net and places it in the T1 or T2 region, and places the flip-flop in the T3 spine region (Figure 3-9).

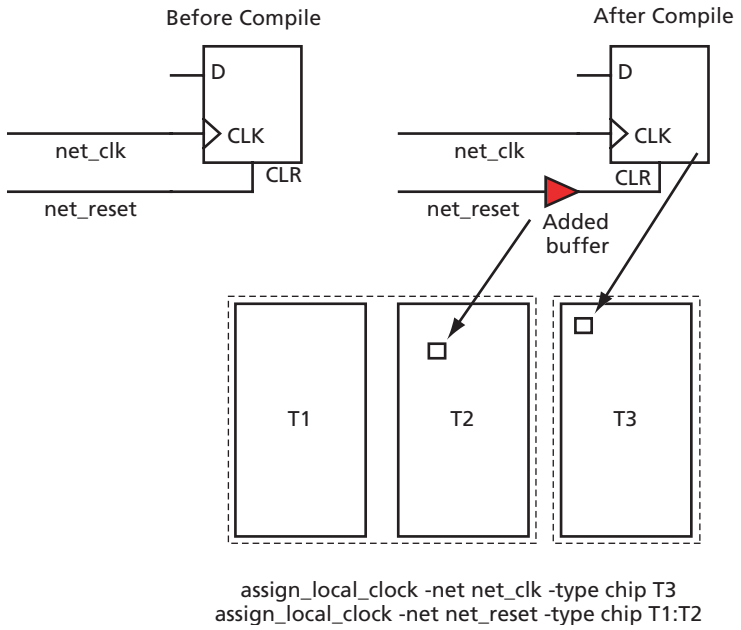


Figure 3-9 • **Adding a Buffer for Shared Instances**

You can control the maximum number of shared instances allowed for the legalization to take place using the Compile Option dialog box shown in Figure 3-10. Refer to Libero IDE / Designer online help for details on the Compile Option dialog box. A large number of shared instances most likely indicates a floorplanning problem that you should address.

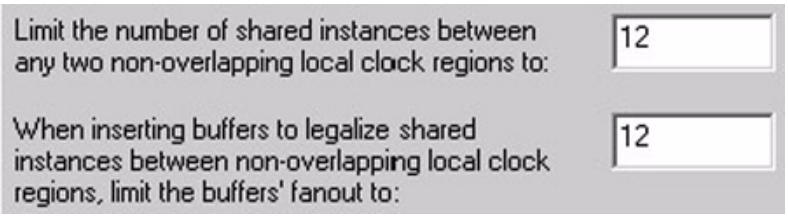


Figure 3-10 **• Shared Instances in the Compile Option Dialog Box**

Designer Flow for Global Assignment

To achieve the desired result, pay special attention to global management during synthesis and place-and-route. The current Synplify tool does not insert more than six global buffers in the netlist by default. Thus, the default flow will not assign any signal to the quadrant global network. However, you can use attributes in Synplify and increase the default global macro assignment in the netlist. Designer v6.2 supports automatic quadrant global assignment, which was not available in Designer v6.1. Layout will make the choice to assign the correct signals to global. However, you can also utilize PDC and perform manual global assignment to overwrite any automatic assignment. The following step-by-step suggestions guide you in the layout of your design and help you improve timing in Designer:

1. Run Compile and check the Compile report. The Compile report has global information in the "Device Utilization" section that describes the number of chip and quadrant signals in the design. A "Net Report" section describes chip global nets, quadrant global nets, local clock nets, a list of nets listed by fanout, and net candidates for local clock assignment. Review this information. Note that YB or YC are counted as global only when they are used in isolation; if you use YB only and not GLB, this net is not shown in the global/quadrant nets report. Instead, it appears in the Global Utilization report.
2. If some signals have a very high fanout and are candidates for global promotion, promote those signals to global using the compile options or PDC commands. Figure 3-11 on page 3-16 shows the Globals Management section of the compile options. Select **Promote regular nets whose fanout is greater than** and enter a reasonable value for fanouts.

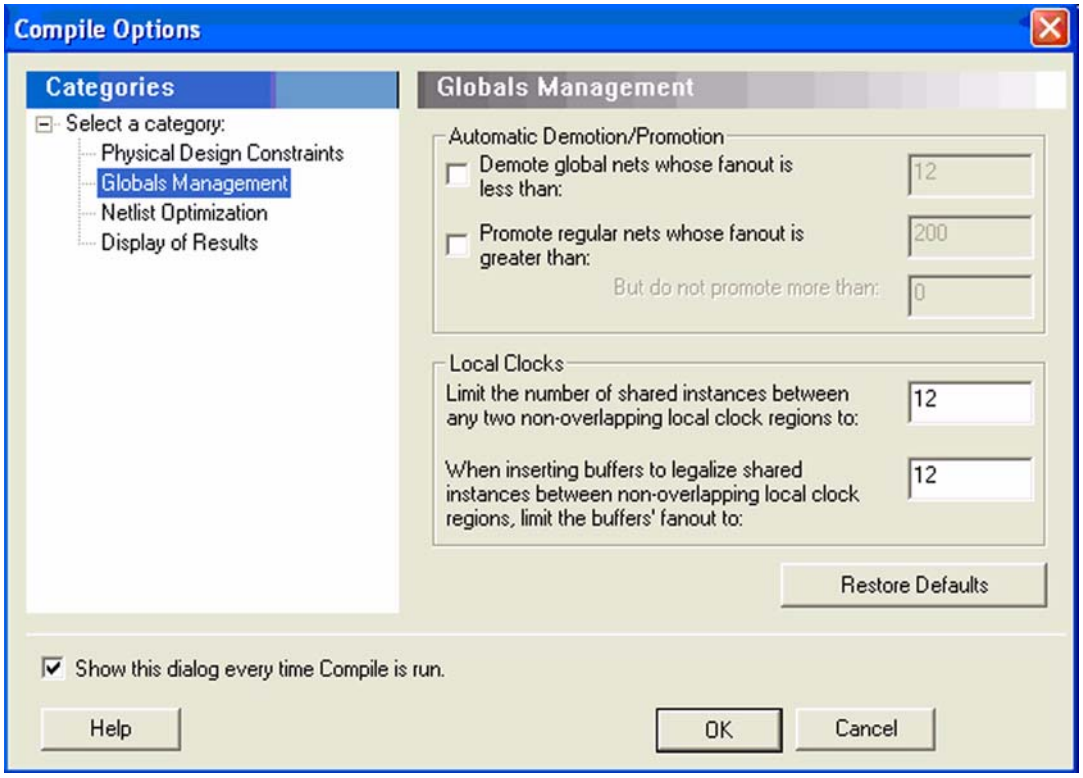


***Figure 3-11* • Globals Management GUI in Designer**

3. Occasionally, the synthesis tool assigns a global macro to clock nets, even though the fanout is significantly less than other asynchronous signals. Select **Demote global nets whose fanout is less than** and enter a reasonable value for fanouts. This frees up some global networks from the signals that have very low fanouts. This can also be done using PDC.
4. Use local clocks for the signals that do not need to go to the whole chip but should have low skew. This local clocks assignment can only be done using PDC.
5. Assign the I/O buffer using MVN if you have fixed I/O assignment. As shown in Figure 3-6 on page 3-8, there are three sets of global pins that have a hardwired connection to each global network. Do not try to put multiple CLKBUF macros in these three sets of global pins. For example, do not assign two CLKBUFs to GAA0x and GAA2x pins.
6. You must click **Commit** at the end of MVN assignment. This runs the pre-layout checker and checks the validity of global assignment.
7. Always run Compile with the **Keep existing physical constraints** option on. This uses the quadrant clock network assignment in the MVN assignment and checks if you have the desired signals on the global networks.
8. Run Layout and check the timing.

Simple Design Example

Consider a design consisting of six building blocks (shift registers) and targeted for an A3PE600-PQ208 (Figure 3-9 on page 3-14). The example design consists of two PLLs (PLL1 has GLA only; PLL2 has both GLA and GLB), a global reset (ACLR), an enable (EN_ALL), and three external clock domains (QCLK1, QCLK2, and QCLK3) driving the different blocks of the design. Note that the PQ208 package only has two PLLs (which access the chip global network). Because of fanout, the global reset and enable signals need to be assigned to the chip global resources. There is only one free chip global for the remaining global (QCLK1, QCLK2, QCLK3). Place two of these signals on the quadrant global resource. The design example demonstrates manually assignment of QCLK1 and QCLK2 to the quadrant global using the PDC command.

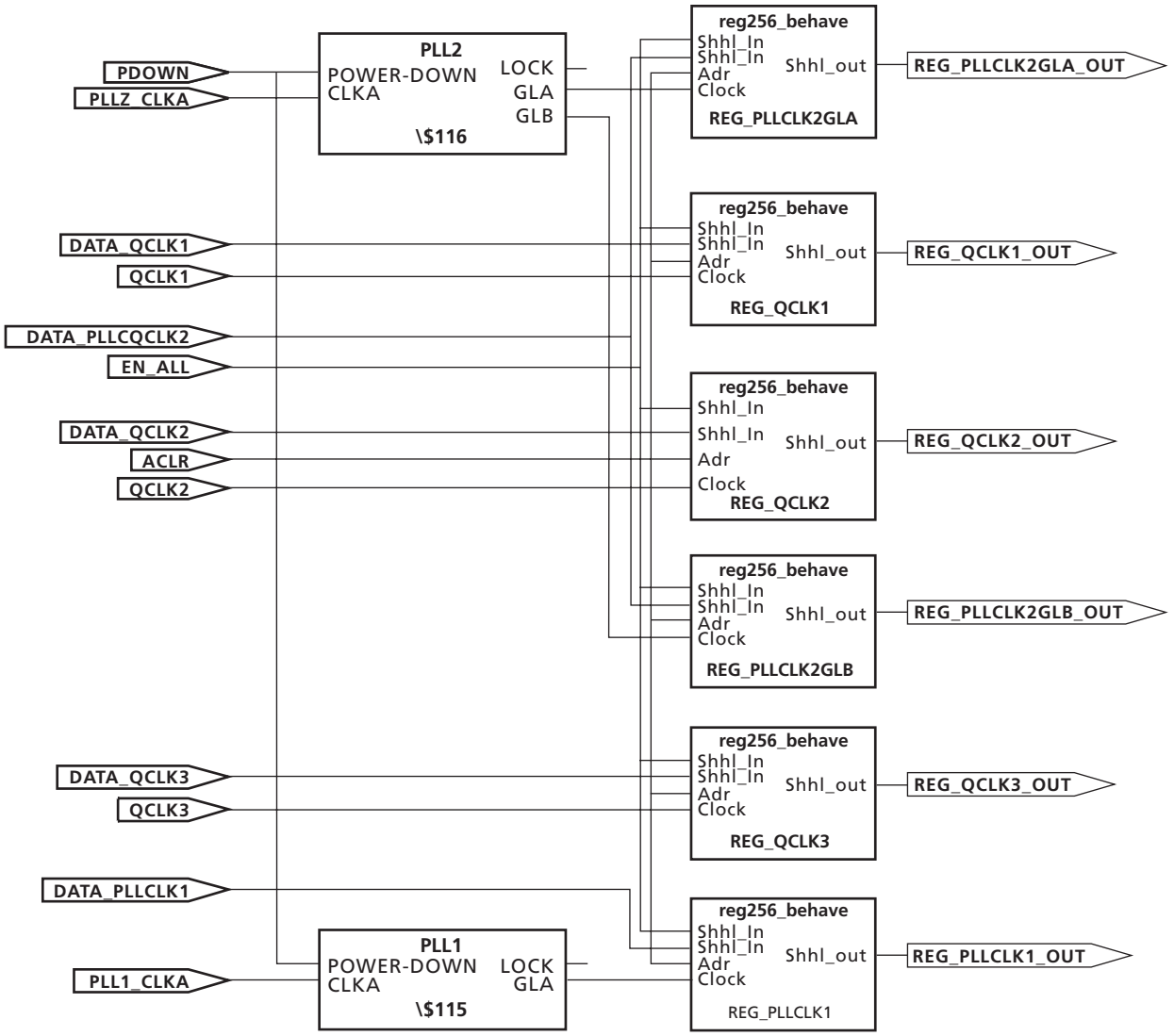


Figure 3-12 • **Block Diagram of the Global Management Example Design**

Step 1

Run Synthesis with default options. The Synplicity log shows the following device utilization:

Cell usage:

	cell count	area	count*area
DFN1E1C1	1536	2.0	3072.0
BUFF	278	1.0	278.0
INBUF	10	0.0	0.0
VCC	9	0.0	0.0
GND	9	0.0	0.0
OUTBUF	6	0.0	0.0
CLKBUF	3	0.0	0.0
PLL	2	0.0	0.0
TOTAL	1853		3350.0

Step 2

Run Compile with the **Promote regular nets whose fanout is greater than** option selected in Designer; you will see the following in the Compile report:

```
Device utilization report:
==========================
CORE               Used:   1536  Total:  13824   (11.11%)
IO (W/ clocks)     Used:     19  Total:    147   (12.93%)
Differential IO    Used:      0  Total:     65    (0.00%)
GLOBAL             Used:      8  Total:     18   (44.44%)
PLL                Used:      2  Total:      2  (100.00%)
RAM/FIFO           Used:      0  Total:     24    (0.00%)
FlashROM           Used:      0  Total:      1    (0.00%)
……................
The following nets have been assigned to a global resource:
Fanout  Type           Name
--------------------------
1536    INT_NET        Net    : EN_ALL_c
                       Driver: EN_ALL_pad_CLKINT
                       Source: AUTO PROMOTED
1536    SET/RESET_NET  Net    : ACLR_c
                       Driver: ACLR_pad_CLKINT
                       Source: AUTO PROMOTED
256     CLK_NET        Net    : QCLK1_c
                       Driver: QCLK1_pad_CLKINT
                       Source: AUTO PROMOTED
256     CLK_NET        Net    : QCLK2_c
                       Driver: QCLK2_pad_CLKINT
                       Source: AUTO PROMOTED
256     CLK_NET        Net    : QCLK3_c
                       Driver: QCLK3_pad_CLKINT
                       Source: AUTO PROMOTED
256     CLK_NET        Net    : $1N14
                       Driver: $1I5/Core
                       Source: ESSENTIAL
256     CLK_NET        Net    : $1N12
                       Driver: $1I6/Core
                       Source: ESSENTIAL
256     CLK_NET        Net    : $1N10
                       Driver: $1I6/Core
                       Source: ESSENTIAL
```

Designer will promote five more signals to global due to high fanout. There are eight signals assigned to global networks.

During Layout, Designer will assign two of the signals to quadrant global locations.

Step 3 (optional)

You can also assign the QCLK1_c and QCLK2_c nets to quadrant regions using the following PDC commands:

```
assign_local_clock –net QCLK1_c  –type quadrant UL
assign_local_clock –net QCLK2_c  –type quadrant LL
```

Step 4

Import this PDC with the netlist and run Compile again. You will see the following in the Compile report:

```
The following nets have been assigned to a global resource:
Fanout  Type          Name
--------------------------
1536    INT_NET       Net    : EN_ALL_c
                      Driver: EN_ALL_pad_CLKINT
                      Source: AUTO PROMOTED
1536    SET/RESET_NET Net    : ACLR_c
                      Driver: ACLR_pad_CLKINT
                      Source: AUTO PROMOTED
256     CLK_NET       Net    : QCLK3_c
                      Driver: QCLK3_pad_CLKINT
                      Source: AUTO PROMOTED
256     CLK_NET       Net    : $1N14
                      Driver: $1I5/Core
                      Source: ESSENTIAL
256     CLK_NET       Net    : $1N12
                      Driver: $1I6/Core
                      Source: ESSENTIAL
256     CLK_NET       Net    : $1N10
                      Driver: $1I6/Core
                      Source: ESSENTIAL
The following nets have been assigned to a quadrant clock resource using PDC:
Fanout  Type          Name
--------------------------
256     CLK_NET       Net    : QCLK1_c
                      Driver: QCLK1_pad_CLKINT
                      Region: quadrant_UL
256     CLK_NET       Net    : QCLK2_c
                      Driver: QCLK2_pad_CLKINT
                      Region: quadrant_LL
```

Step 5

Run Layout.

Global Management in PLL Design

This section describes the legal global network connections to PLLs in the low-power flash devices. For detailed information on using PLLs, refer to *Clock Conditioning Circuits in IGLOO and ProASIC3 Devices*. Actel recommends that you use the dedicated global pins to directly drive the reference clock input of the associated PLL for reduced propagation delays and clock distortion. However, low-power flash devices offer the flexibility to connect other signals to reference clock inputs. Each PLL is associated with three global networks (Figure 3-7 on page 3-9). There are some limitations, such as when trying to use the global and PLL at the same time:

- If you use a PLL with only primary output, you can still use the remaining two free global networks.
- If you use three globals associated with a PLL location, you cannot use the PLL on that location.
- If the YB or YC output is used standalone, it will occupy one global, even though this signal does not go to the global network.

Using Spines of Occupied Global Networks

When a signal is assigned to a global network, the flash switches are programmed to set the MUX select lines (explained in the "Clock Aggregation Architecture" section on page 3-8) to drive the spines of that network with the global net. However, if the global net is restricted from reaching into the scope of a spine, the MUX drivers of that spine are available for other high-fanout or critical signals (Figure 3-13).

For example, if you want to limit the CLK1_c signal to the left half of the chip and want use the right side of the same global network for CLK2_c, you can add the following PDC commands:

```
define_region -name region1 -type inclusive 0 0 34 29
assign_net_macros region1 CLK1_c
assign_local_clock –net CLK2_c –type chip B2
```

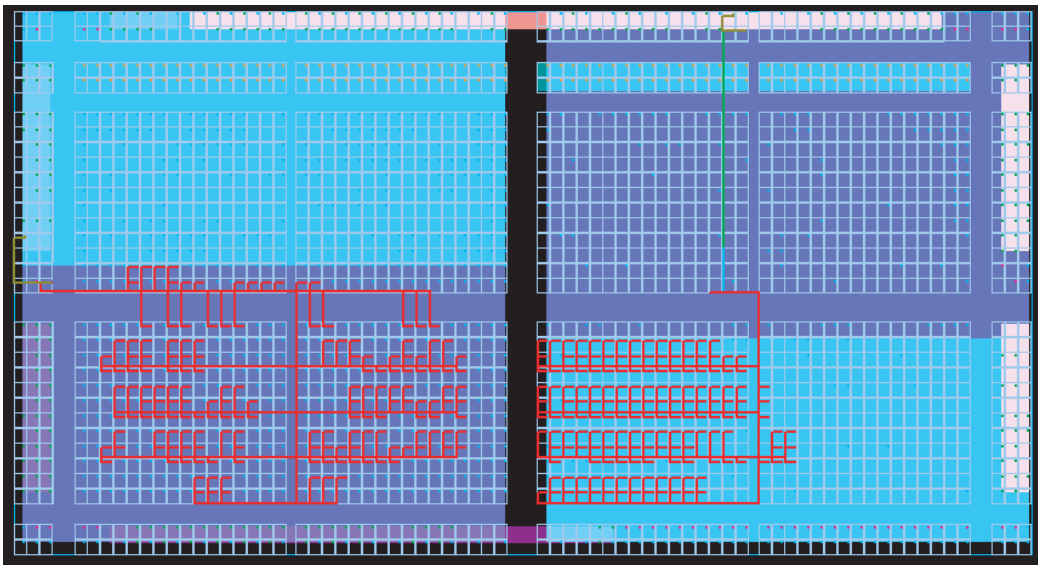


Figure 3-13 **• Design Example Using Spines of Occupied Global Networks**

Conclusion

IGLOO, Fusion, and ProASIC3 devices contain 18 global networks: 6 chip global networks and 12 quadrant global networks. These global networks can be segmented into local low-skew networks called spines. The spines provide low-skew networks for the high-fanout signals of a design. These allow you up to 252 different internal/external clocks in an A3PE3000 device. This document describes the architecture for the global network, plus guidelines and methodologies in assigning signals to globals and spines.

Related Documents

Handbook Documents

Clock Conditioning Circuits in IGLOO and ProASIC3 Devices

http://www.actel.com/LPD_CCC_HBs.pdf

I/O Structures in IGLOO PLUS Devices

http://www.actel.com/documents/IGLOOPLUS_IO_HBs.pdf

I/O Structures in IGLOO and ProASIC3 Devices

http://www.actel.com/documents/IGLOO_PA3_IO_HBs.pdf

I/O Structures in IGLOOe and ProASIC3E Devices

http://www.actel.com/documents/IGLOOe_PA3E_IO_HBs.pdf

User's Guides

IGLOO, Fusion, and ProASIC3 Macro Library Guide

http://www.actel.com/documents/pa3_libguide_ug.pdf

Part Number and Revision Date

This document contains content extracted from the Device Architecture section of the datasheet, combined with content previously published as an application note describing features and functions of the device. To improve usability for customers, the device architecture information has now been combined with usage information, to reduce duplication and possible inconsistencies in published information. No technical changes were made to the datasheet content unless explicitly listed. Changes to the application note content were made only to be consistent with existing datasheet information.

Part Number 51700094-005-2

Revised June 2008

List of Changes

The following table lists critical changes that were made in the current version of the chapter.

Previous Version	Changes in Current Version (v1.2)	Page
v1.1 (March 2008)	The following changes were made to the family descriptions in Table 3-1 · Low-Power Flash Families: • ProASIC3L was updated to include 1.5 V. • The number of PLLs for ProASIC3E was changed from five to six.	3-2
v1.0 (January 2008)	The "Global Architecture" section was updated to include the IGLOO PLUS family. The bullet was revised to include that the west CCC does not contain a PLL core in 15 k and 30 k devices. Instances of "A3P030 and AGL030 devices" were replaced with "15 k and 30 k gate devices."	3-1
	Table 3-1 · Low-Power Flash Families and the accompanying text was updated to include the IGLOO PLUS family. The "IGLOO Terminology" section and "ProASIC3 Terminology" section are new.	3-2
	The "VersaNet Global Network Distribution" section, "Spine Architecture" section, the note in Figure 3-1 · Overview of VersaNet Global Network and Device Architecture, and the note in Figure 3-2 · Simplified VersaNet Global Network were updated to include mention of 15 k gate devices.	3-3, 3-4
	Table 3-2 · Globals/Spines/Rows for IGLOO and ProASIC3 Devices was updated to add the A3P015 device, and to revise the values for clock trees, globals/spines per tree, and globals/spines per device for the A3P030 and AGL030 devices.	3-5
	Table 3-3 · Globals/Spines/Rows for IGLOO PLUS Devices is new.	3-5
	CLKBUF_LVCMOS12 was added to Table 3-7 · I/O Standards within CLKBUF.	3-11
	The "Handbook Documents" section was updated to include the three different I/O Structures chapters for ProASIC3 and IGLOO device families.	3-21
51900087-1/3.05	Figure 3-2 · Simplified VersaNet Global Network was updated.	3-4
	The "Naming of Global I/Os" section was updated.	3-9
	The "Using Global Macros in Synplicity" section was updated.	3-12
	The "Global Promotion and Demotion Using PDC" section was updated.	3-13
	The "Designer Flow for Global Assignment" section was updated.	3-15
	The "Simple Design Example" section was updated.	3-17
51900087-0/1.05	Table 3-2 · Globals/Spines/Rows for IGLOO and ProASIC3 Devices was updated.	3-5

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4 – Clock Conditioning Circuits in IGLOO and ProASIC3 Devices

Introduction

This document outlines the following device information: CCC features, PLL core specifications, functional descriptions, software configuration information, detailed usage information, recommended board-level considerations, and other considerations concerning clock conditioning circuits and global networks in low-power flash devices.

Overview of Clock Conditioning Circuitry

In IGLOO® and ProASIC®3 devices, the CCCs are used to implement frequency division, frequency multiplication, phase shifting, and delay operations. The CCCs are available in six chip locations—each of the four chip corners and the middle of the east and west chip sides. For device-specific variations, refer to the "Device-Specific Layout" section on page 4-13.

The CCC is composed of the following:

- PLL core
- 3 phase selectors
- 6 programmable delays and 1 fixed delay that advances/delays phase
- 5 programmable frequency dividers that provide frequency multiplication/division (not shown in Figure 4-5 on page 4-8 because they are automatically configured based on the user's required frequencies)
- 1 dynamic shift register that provides CCC dynamic reconfiguration capability

Figure 4-1 provides a simplified block diagram of the physical implementation of the building blocks in each of the CCCs.

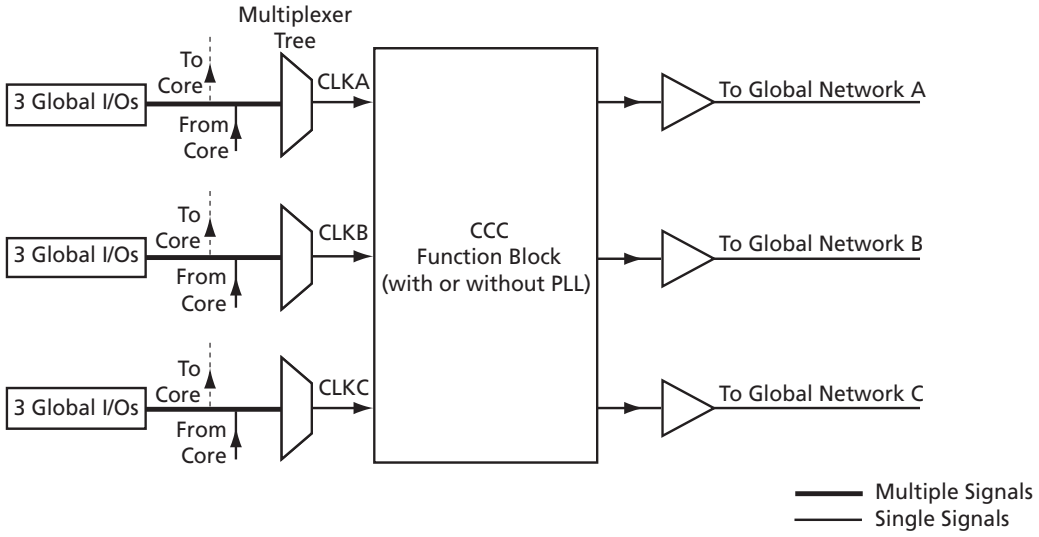


Figure 4-1 • **Overview of the CCCs Offered in IGLOO and ProASIC3**

Each CCC can implement up to three independent global buffers (with or without programmable delay) or a PLL function (programmable frequency division/multiplication, phase shift, and delays)

with up to three global outputs. Unused global outputs of a PLL can be used to implement independent global buffers, up to a maximum of three global outputs for a given CCC.

CCC Programming

The CCC block is fully configurable, either via flash configuration bits set in the programming bitstream or through an asynchronous interface. This asynchronous dedicated shift register interface is dynamically accessible from inside the low-power flash devices to permit parameter changes, such as PLL divide ratios and delays, during device operation.

To increase the versatility and flexibility of the clock conditioning system, the CCC configuration is determined either by the user during the design process, with configuration data being stored in flash memory as part of the device programming procedure, or by writing data into a dedicated shift register during normal device operation.

This latter mode allows the user to dynamically reconfigure the CCC without the need for core programming. The shift register is accessed through a simple serial interface. Refer to *UJTAG Applications in Actel's Low-Power Flash Devices*.

Global Resources

Low-power flash devices provide three global routing networks (GLA, GLB, and GLC) for each of the CCC locations. There are potentially many I/O locations; each global I/O location can be chosen from only one of three possibilities. This is controlled by the multiplexer tree circuitry in each global network. Once the I/O location is selected, the user has the option to utilize the CCCs before the signals are connected to the global networks. The CCC in each location (up to six) has the same structure, so generating the CCC macros is always done with an identical software GUI. The CCCs in the corner locations drive the quadrant global networks, and the CCCs in the middle of the east and west locations drive the chip global networks. The quadrant global networks span only a quarter of the device, while the chip global networks span the entire device. For more details on global resources offered in low-power flash devices, refer to *Global Resources in Actel Low-Power Flash Devices*.

A global buffer can be placed in any of the three global locations (CLKA-GLA, CLKB-GLB, or CLKC-GLC) of a given CCC. A PLL macro uses the CLKA CCC input to drive its reference clock. It uses the GLA and, optionally, the GLB and GLC global outputs to drive the global networks. A PLL macro can also drive the YB and YC regular core outputs. The GLB (or GLC) global output cannot be reused if the YB (or YC) output is used. Refer to the "PLL Macro Signal Descriptions" section on page 4-7 for more information.

Each global buffer, as well as the PLL reference clock, can be driven from one of the following:

- 3 dedicated single-ended I/Os using a hardwired connection
- 2 dedicated differential I/Os using a hardwired connection
- The FPGA core

CCC Support in Low-Power Devices

The low-power flash families listed in Table 4-1 support the CCC feature and the functions described in this document.

Table 4-1 • **Low-Power Flash Families**

Family[1]	Description	Timing Numbers[2]
IGLOO	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*IGLOO DC and Switching Characteristics*
IGLOO PLUS	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology and enhanced I/O capabilities.	*IGLOO PLUS DC and Switching Characteristics*
IGLOOe	IGLOO devices enhanced with higher density, five additional PLLs, and additional I/O standards	*IGLOOe DC and Switching Characteristics*
ProASIC3L	Low-power, high-performance 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*ProASIC3L DC and Switching Characteristics*
ProASIC3	Low-power, high-performance 1.5 V FPGAs	*ProASIC3 DC and Switching Characteristics*
ProASIC3E	ProASIC3 enhanced with higher density, six additional PLLs, and additional I/O standards	*ProASIC3E DC and Switching Characteristics*
ProASIC3 Automotive	Low-power, high-performance FPGAs qualified for automotive applications	*Automotive ProASIC3 DC and Switching Characteristics*

Notes:

1. *The family names are linked to the appropriate product brief.*
2. *The timing number links go to the relevant timing numbers in the datasheet.*

Actel's low-power flash devices (listed in Table 4-1) provide a selection of low-power, secure, live-at-power-up, single-chip solutions. The nonvolatile flash-based devices do not require a boot PROM and incorporate FlashLock® technology, which provides a unique combination of reprogrammability and design security without external overhead. Only low-power flash FPGAs can offer these advantages.

Actel IGLOO PLUS FPGAs are the industry-leading 1.2 V ultra-low-power programmable logic devices (PLDs) and consume 90% less static power and over 50% less dynamic power than PLD alternatives, while ProASIC3L devices offer a balance of low power and higher performance.

Flash*Freeze technology used in IGLOO, IGLOO PLUS, and ProASIC3L devices enables easy entry to and exit from the ultra-low power mode, which consumes as little as 5 µW, while retaining SRAM and register data. IGLOO PLUS also offers the ability to hold I/O state in Flash*Freeze mode. Flash*Freeze technology simplifies power management through I/O and clock management without the need to turn off voltages, I/Os, or clocks at the system level. Entering and exiting Flash*Freeze mode takes less than 1 µs.

IGLOO Terminology

In documentation, the term IGLOO families or IGLOO devices refers to all IGLOO families as listed in Table 4-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

ProASIC3 Terminology

In documentation, the term ProASIC3 families or ProASIC3 devices refers to all ProASIC3 families as listed in Table 4-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

Global Buffers with No Programmable Delays

Access to the global / quadrant global networks can be configured directly from the global I/O buffer, bypassing the CCC functional block (as indicated by the dotted lines in Figure 4-2). Internal signals driven by the FPGA core can use the global / quadrant global networks by connecting via the routed clock input of the multiplexer tree.

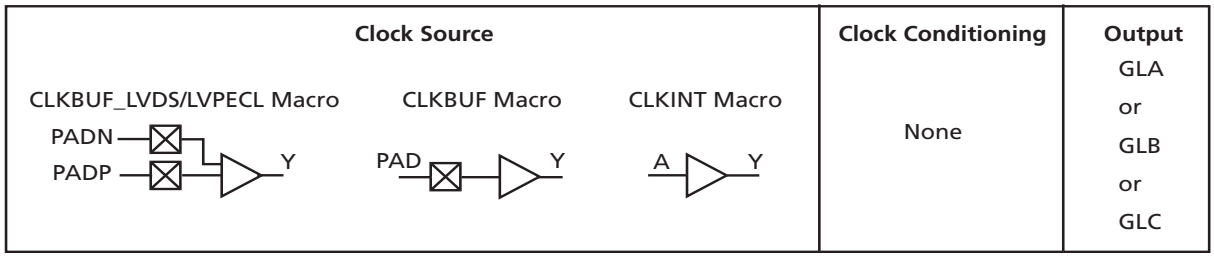
There are many specific CLKBUF macros supporting the wide variety of single-ended I/O inputs (CLKBUF) and differential I/O standards (CLKBUF_LVDS/LVPECL) in the low-power flash families. They are used when connecting global I/Os directly to the global/quadrant networks.

When an internal signal needs to be connected to the global/quadrant network, the CLKINT macro is used to connect the signal to the routed clock input of the network's MUX tree.

To utilize direct connection from global I/Os or from internal signals to the global/quadrant networks, CLKBUF, CLKBUF_LVPECL/LVDS, and CLKINT macros are used.

- The CLKBUF and CLKBUF_LVPECL/LVDS/BLVDS/M-LVDS macros are composite macros that include an I/O macro driving a global buffer, which uses a hardwired connection.
- The CLKBUF, CLKBUF_LVPECL/LVDS/BLVDS/M-LVDS, and CLKINT macros are pass-through clock sources and do not use the PLL or provide any programmable delay functionality.
- The CLKINT macro provides a global buffer function driven internally by the FPGA core.

The available CLKBUF macros are described in the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.



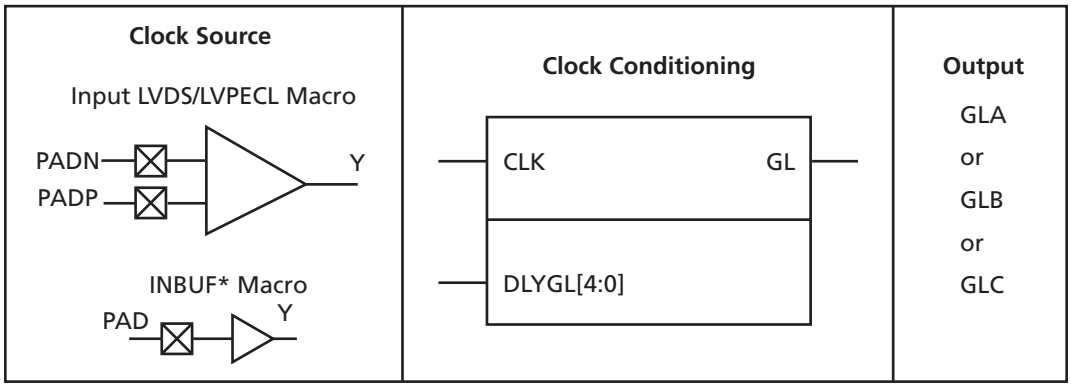
Note: The CLKDLY macro uses programmable delay element type 2.

Figure 4-2 • **CCC Options: Global Buffers with No Programmable Delay**

Global Buffer with Programmable Delay

Clocks requiring clock adjustments can utilize the programmable delay cores before connecting to the global / quadrant global networks. A maximum of 18 CCC global buffers can be instantiated in a device—three per CCC times up to six CCCs per device.

Each CCC functional block contains a programmable delay element for each of the global networks (up to three).



Note: For INBUF driving a PLL macro or CLKDLY macro, the I/O will be hard-routed to the CCC; i.e., will be placed by software to a dedicated Global I/O.*

Figure 4-3 • **CCC Options: Global Buffers with Programmable Delay**

The CLKDLY macro is a pass-through clock source that does not use the PLL, but provides the ability to delay the clock input using a programmable delay. The CLKDLY macro takes the selected clock input and adds a user-defined delay element. This macro generates an output clock phase shift from the input clock.

The CLKDLY macro can be driven by an INBUF* macro to create a composite macro, where the I/O macro drives the global buffer (with programmable delay) using a hardwired connection. In this case, the I/O must be placed in one of the dedicated global I/O locations. Many specific INBUF macros support the wide variety of single-ended and differential I/O standards supported by the low-power flash family. The available INBUF macros are described in the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

The CLKDLY macro can be driven directly from the FPGA core. The CLKDLY macro can also be driven from an I/O that is routed through the FPGA regular routing fabric. In this case, users must instantiate a special macro, PLLINT, to differentiate from the hardwired I/O connection described earlier.

The visual CLKDLY configuration in the SmartGen part of the Actel Libero® Integrated Design Environment (IDE) and Designer tools allows the user to select the desired amount of delay and configures the delay elements appropriately. SmartGen also allows the user to select the input clock source. SmartGen will automatically instantiate the special macro, PLLINT, when needed.

CLKDLY Macro Signal Descriptions

The CLKDLY macro supports one input and one output. Each signal is described in Table 4-2.

Table 4-2 • **Input and Output Description of the CLKDLY Macro**

Signal	Name	I/O	Description
CLK	Reference Clock	Input	Reference clock input for PLL core Input clock for primary output clock, GLA
GL	Global Output	Output	Primary output clock to respective global/quadrant clock networks

CLKDLY Macro Usage

When a CLKDLY macro is used in a CCC location, the programmable delay element is used to allow the clock delays to go to the global network. In addition, the user can bypass the PLL in a CCC location integrated with a PLL, but use the programmable delay that is associated with the global network by instantiating the CLKDLY macro. The same is true when using programmable delay elements in a CCC location with no PLLs (the user needs to instantiate the CLKDLY macro). There is no difference between the programmable delay elements used for the PLL and the CLKDLY macro.

The CCC will be configured to use the programmable delay elements in accordance with the macro instantiated by the user.

As an example, if the PLL is not used in a particular CCC location, the designer is free to specify up to three CLKDLY macros in the CCC, each of which can have its own input frequency and delay adjustment options. If the PLL core is used, assuming output to only one global clock network, the other two global clock networks are free to be used by either connecting directly from the global inputs or connecting from one or two CLKDLY macros for programmable delay.

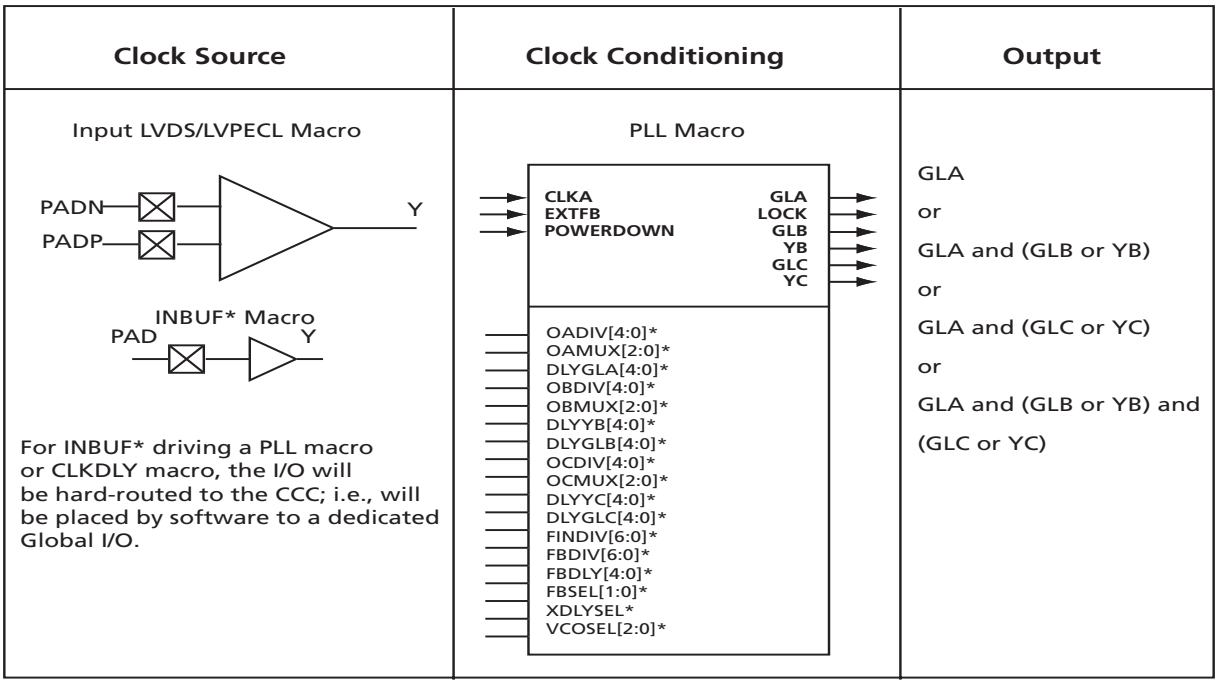
The programmable delay elements are shown in the block diagram of the PLL block shown in Figure 4-5 on page 4-8. Note that any CCC locations with no PLL present contain only the programmable delay blocks going to the global networks (labeled "Programmable Delay Type 2"). Refer to the "Clock Delay Adjustment" section on page 4-19 for a description of the programmable delay types used for the PLL. Also refer to Table 4-13 on page 4-24 for Programmable Delay Type 1 step delay values, and Table 4-14 on page 4-25 for Programmable Delay Type 2 step delay values. CCC locations with a PLL present can be configured to utilize only the programmable delay blocks (Programmable Delay Type 2) going to the global networks A, B, and C.

Global network A can be configured to use only the programmable delay element (bypassing the PLL) if the PLL is not used in the design. Figure 4-5 on page 4-8 shows a block diagram of the PLL, where the programmable delay elements are used for the global networks (Programmable Delay Type 2).

Global Buffers with PLL function

Clocks requiring frequency synthesis or clock adjustments can utilize the PLL core before connecting to the global / quadrant global networks. A maximum of 18 CCC global buffers can be instantiated in a device—three per CCC times up to six CCCs per device. Each PLL core can generate up to three global/quadrant clocks, while a clock delay element provides one.

The PLL functionality of the clock conditioning block is supported by the PLL macro.



Note: Refer to the IGLOO, Fusion, and ProASIC3 Macro Library Guide for more information.

Figure 4-4 • **CCC Options: Global Buffers with PLL**

The PLL macro provides five derived clocks (three independent) from a single reference clock. The PLL macro also provides power-down input and lock output signals. The additional inputs shown

on the macro are configuration settings, which are configured through the use of SmartGen. For manual setting of these bits refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide* for details.

Figure 4-5 on page 4-8 illustrates the various clock output options and delay elements.

PLL Macro Signal Descriptions

The PLL macro supports two inputs and up to six outputs. Table 4-3 gives a description of each signal.

Table 4-3 • **Input and Output Signals of the PLL Block**

Signal	Name	I/O	Description
CLKA	Reference Clock	Input	Reference clock input for PLL core; Input clock for primary output clock, GLA
EXTFB	External Feedback	Input	Allows an external signal to be compared to a reference clock in the PLL core's phase detector
POWERDOWN	Power Down	Input	Active low input that selects power-down mode and disables the PLL. With the POWERDOWN signal asserted, the PLL core sends 0 V signals on all of the outputs.
GLA	Primary Output	Output	Primary output clock to respective global/quadrant clock networks
GLB	Secondary 1 Output	Output	Secondary 1 output clock to respective global/quadrant clock networks
YB	Core 1 Output	Output	Core 1 output clock to local routing network
GLC	Secondary 2 Output	Output	Secondary 2 output clock to respective global/quadrant clock networks
YC	Core 2 Output	Output	Core 2 output clock to local routing network
LOCK	PLL Lock Indicator	Output	Active-high signal indicating that steady-state lock has been achieved between CLKA and the PLL feedback signal

Input Clock

As discussed above, the inputs to the input reference clock (CLKA) of the PLL can come from global input pins, regular I/O pins, or internally from the core.

Global Output Clocks

GLA (Primary), GLB (Secondary 1), and GLC (Secondary 2) are the outputs of Global Multiplexer 1, Global Multiplexer 2, and Global Multiplexer 3, respectively. These signals (GLx) can be used to drive the high-speed global and quadrant networks of the low-power flash devices.

A global multiplexer block consists of the input routing for selecting the input signal for the GLx clock and the output multiplexer, as well as delay elements associated with that clock.

Core Output Clocks

YB and YC are known as Core Outputs and can be used to drive internal logic without using global network resources. This is especially helpful when global network resources must be conserved and utilized for other timing-critical paths.

YB and YC are identical to GLB and GLC, respectively, with the possible exception of a higher selectable final output delay. The SmartGen PLL Wizard will configure these outputs according to user specifications and can enable these signals with or without the enabling of Global Output Clocks.

The above signals can be enabled in the following output groupings in both internal and external feedback configurations of the static PLL:

- One output – GLA only
- Two outputs – GLA + (GLB and/or YB)
- Three outputs – GLA + (GLB and/or YB) + (GLC and/or YC)

PLL Macro Block Diagram

As illustrated, the PLL supports three distinct output frequencies from a given input clock. Two of these (GLB and GLC) can be routed to the B and C global network access, respectively, and/or routed to the device core (YB and YC).

There are five delay elements to support phase control on all five outputs (GLA, GLB, GLC, YB, and YC).

There is also a delay element in the feedback loop that can be used to advance the clock relative to the reference clock.

The PLL macro reference clock can be driven by an INBUF* macro to create a composite macro, where the I/O macro drives the global buffer (with programmable delay) using a hardwired connection. In this case, the I/O must be placed in one of the dedicated global I/O locations.

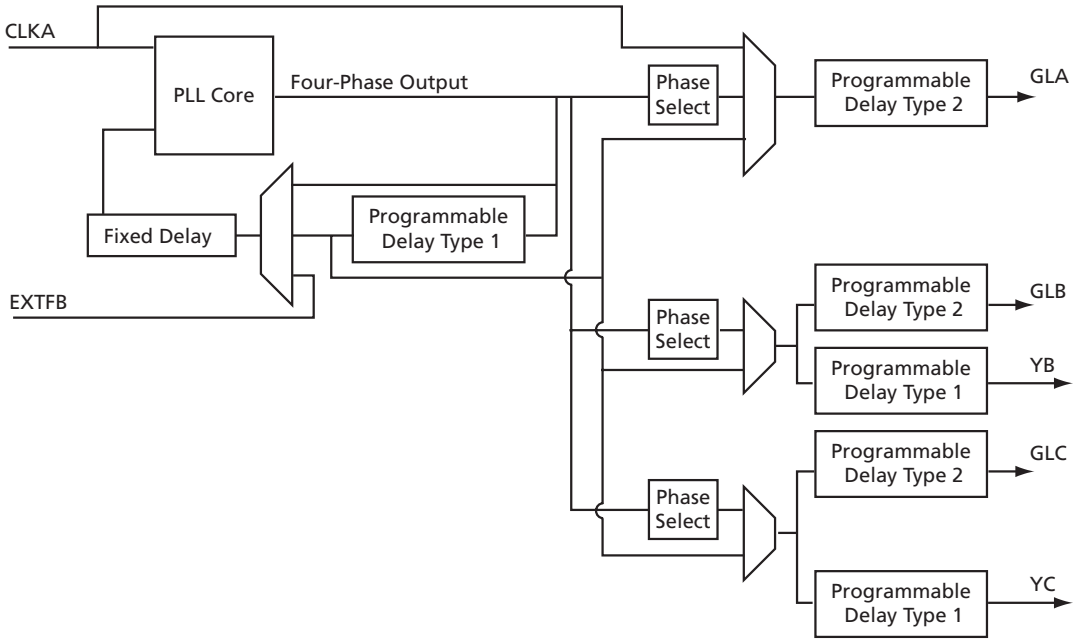
The PLL macro reference clock can be driven directly from the FPGA core.

The PLL macro reference clock can also be driven from an I/O that is routed through the FPGA regular routing fabric. In this case, users must instantiate a special macro, PLLINT, to differentiate from the hardwired I/O connection described earlier.

During power-up, the PLL outputs will toggle around the maximum frequency of the voltage-controlled oscillator (VCO) gear selected. Toggle frequencies can range from 40 MHz to 250 MHz. This will continue as long as the clock input (CLKA) is constant (HIGH or LOW). This can be prevented by LOW assertion of the POWERDOWN signal.

The visual PLL configuration in SmartGen, part of the Libero IDE and Designer tools, will derive the necessary internal divider ratios based on the input frequency and desired output frequencies selected by the user.

SmartGen also allows the user to select the various delays and phase shift values necessary to adjust the phases between the reference clock (CLKA) and the derived clocks (GLA, GLB, GLC, YB, and YC). SmartGen also allows the user to select the input clock source. SmartGen automatically instantiates the special macro, PLLINT, when needed.



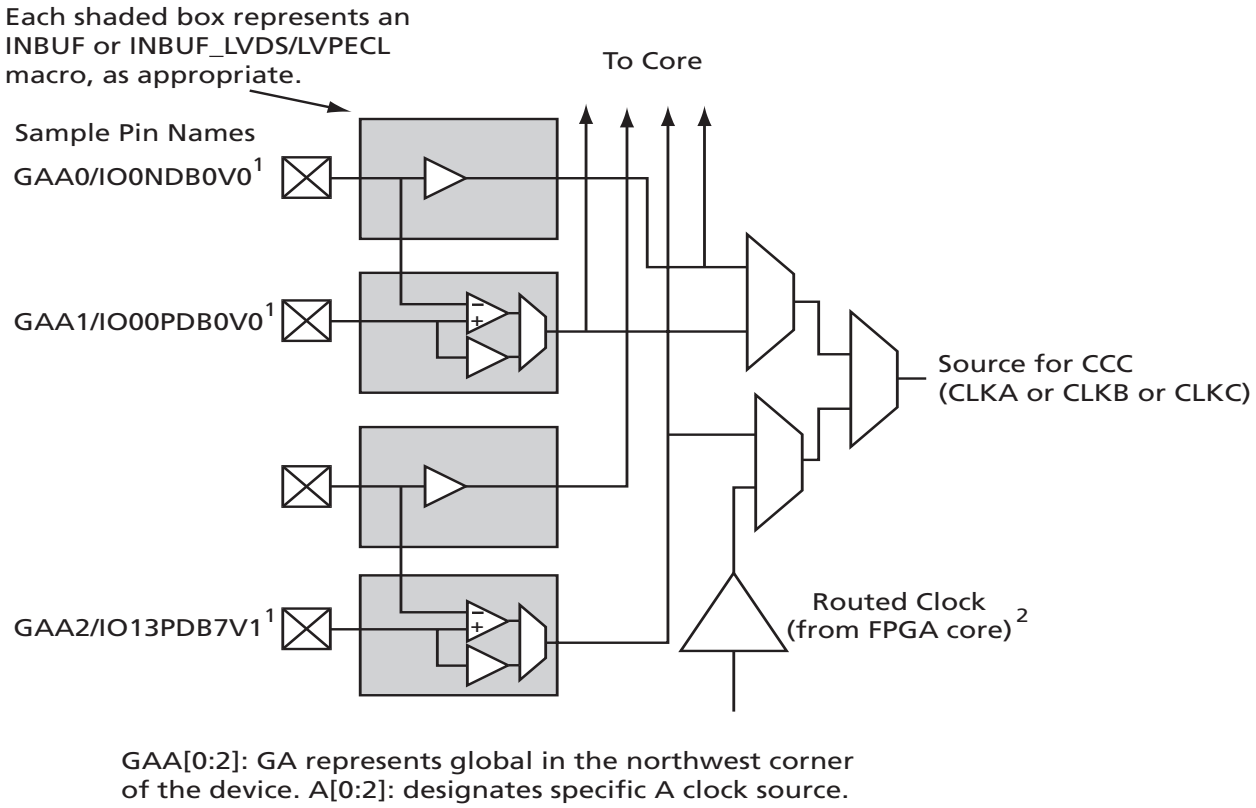
Note: Clock divider and clock multiplier blocks are not shown in this figure or in SmartGen. They are automatically configured based on the user's required frequencies.

Figure 4-5 • **CCC with PLL Block**

Global Input Selections

Low-power flash devices provide the flexibility of choosing one of the three global input pad locations available to connect to a CCC functional block or to a global / quadrant global network. Figure 4-6 shows the detailed architecture of each global input structure. If the single-ended I/O standard is chosen, there is flexibility to choose one of the global input pads (the first, second, and fourth input). Once chosen, the other I/O locations are used as regular I/Os. If the differential I/O standard is chosen, the first and second inputs are considered as paired, and the third input is paired with a regular I/O.

The user then has the choice of selecting one of the two sets to be used as the clock input source to the CCC functional block. There is also the option to allow an internal clock signal to feed the global network or the CCC functional block. A multiplexer tree selects the appropriate global input for routing to the desired location. Note that the global I/O pads do not need to feed the global network; they can also be used as regular I/O pads.



Notes:

1. *Represents the global input pins. Globals have direct access to the clock conditioning block and are not routed via the FPGA fabric. Refer to* User I/O Naming Conventions *in I/O Structures in IGLOO and ProASIC3 Devices.*
2. *Instantiate the routed clock source input as follows:*
   a) Connect the output of a logic element to the clock input of a PLL, CLKDLY, or CLKINT macro.
   b) Do not place a clock source I/O (INBUF or INBUF_LVPECL/LVDS/BLVDS/M-LVDS/DDR) in a relevant global pin location.

Figure 4-6 • **Clock Input Sources Including CLKBUF, CLKBUF_LVDS/LVPECL, and CLKINT**

Each global buffer, as well as the PLL reference clock, can be driven from one of the following:

- 3 dedicated single-ended I/Os using a hardwired connection
- 2 dedicated differential I/Os using a hardwired connection
- The FPGA core

Since the architecture of the devices varies as size increases, the following list details I/O types supported for globals:

- LVDS-, BLVDS-, and M-LVDS–based clock sources are only available on 250 k gate devices and above.
- 65 k and 125 k gate devices support single-ended clock sources only.
- 15 k and 30 k gate devices support these inputs for CCC only and do not contain a PLL.

Clock Sources for PLL and CLKDLY Macros

The input reference clock (CLKA for a PLL macro, CLK for a CLKDLY macro) can be accessed from different sources via the associated clock multiplexer tree. Each CCC has the option of choosing the source of the input clock from one of the following:

- Hardwired I/O
- External I/O
- Core Logic

The SmartGen macro builder tool allows users to easily create the PLL and CLKDLY macros with the desired settings. It is strongly recommended that SmartGen be used to generate the CCC macros.

Hardwired I/O Clock Source

Hardwired I/O refers to global input pins that are hardwired to the multiplexer tree, which directly accesses the CCC global buffers. These global input pins have designated pin locations and are indicated with the I/O naming convention *Gmn* (*m* refers to any one of the positions where the PLL core is available, and *n* refers to any one of the three global input MUXes and the pin number of the associated global location, *m*). Choosing this option provides the benefit of directly connecting to the CCC reference clock input, which provides less delay. See Figure 4-7 for an example illustration of the connections, shown in red. If a CLKDLY macro is initiated to utilize the programmable delay element of the CCC, the clock input can be placed at one of nine dedicated global input pin locations. In other words, if Hardwired I/O is chosen as the input source, the user can decide to place the input pin in one of the GmA0, GmA1, GmA2, GmB0, GmB1, GmB2, GmC0, GmC1, or GmC2 locations of the low-power flash devices. When a PLL macro is used to utilize the PLL core in a CCC location, the clock input of the PLL can only be connected to one of three GmA* global pin locations: GmA0, GmA1, or GmA2.

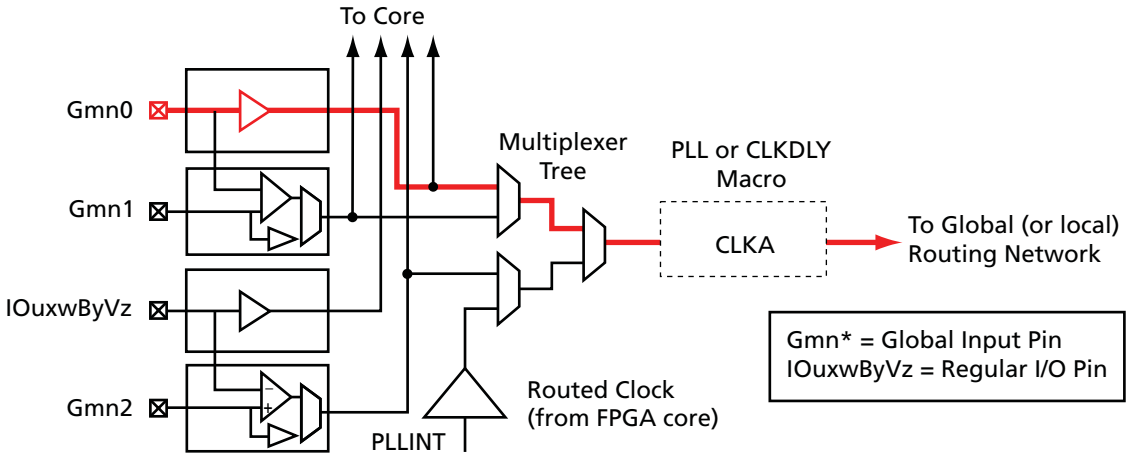


Figure 4-7 • **Illustration of Hardwired I/O (global input pins) Usage**

External I/O Clock Source

External I/O refers to regular I/O pins. The clock source is instantiated with one of the various INBUF options and accesses the CCCs via internal routing. The user has the option of assigning this input to any of the I/Os labeled with the I/O convention *IOuxwByVz*. Refer to *User I/O Naming Conventions* in I/O Structures in IGLOO and ProASIC3 Devices *for more information.* Figure 4-8 gives a brief explanation of external I/O usage. Choosing this option provides the freedom of selecting any user I/O location but introduces additional delay because the signal connects to the routed clock input through internal routing before connecting to the CCC reference clock input.

For the External I/O option, the routed signal would be instantiated with a PLLINT macro before connecting to the CCC reference clock input. This instantiation is conveniently done automatically by SmartGen when this option is selected. Using the SmartGen tool to generate the CCC macro is the recommended approach. The instantiation of the PLLINT macro results in the use of the routed clock input of the I/O to connect to the PLL clock input. If not using SmartGen, manually instantiate a PLLINT macro before the PLL reference clock to indicate that the regular I/O driving the PLL reference clock should be used (see Figure 4-8 for an example illustration of the connections, shown in red).

In the above two options, the clock source must be instantiated with one of the various INBUF macros. The reference clock pins of the CCC functional block core macros must be driven by regular input macros (INBUFs), not clock input macros.

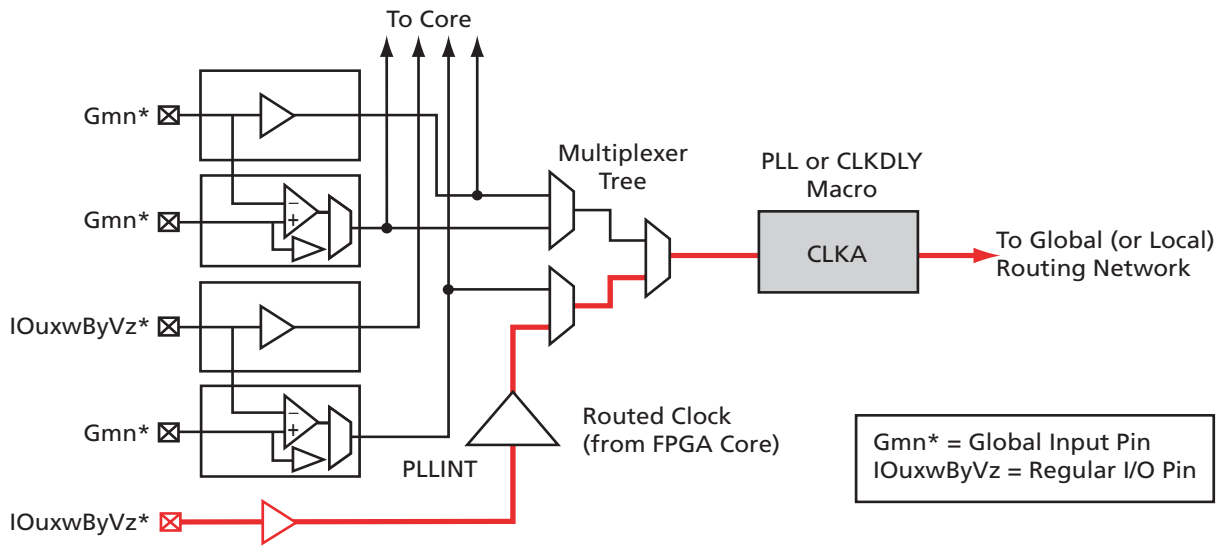


Figure 4-8 • **Illustration of External I/O Usage**

Core Logic Clock Source

Core logic refers to internal routed nets. Internal routed signals access the CCC via the FPGA Core Fabric. Similar to the external I/O option, whenever the clock source comes internally from the core itself, the routed signal is instantiated with a PLLINT macro before connecting to the CCC clock input (see Figure 4-9 for an example illustration of the connections, shown in red).

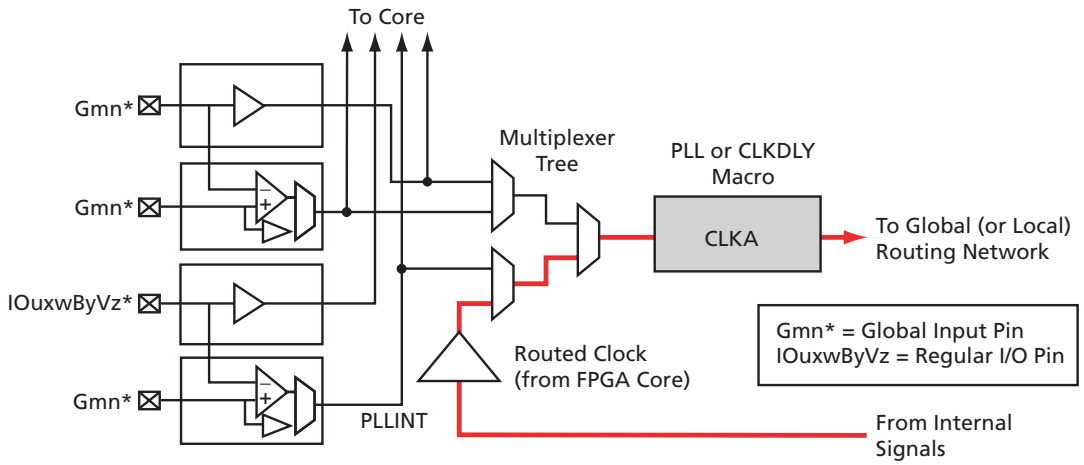


Figure 4-9 • **Illustration of Core Logic Usage**

Available I/O Standards

Table 4-4 • **Available I/O Standards within CLKBUF and CLKBUF_LVDS/LVPECL Macros**

CLKBUF_LVCMOS5
CLKBUF_LVCMOS33 [1]
CLKBUF_LVCMOS25 [2]
CLKBUF_LVCMOS18
CLKBUF_LVCMOS15
CLKBUF_PCI
CLKBUF_PCIX [2]
CLKBUF_GTL25 [2]
CLKBUF_GTL33 [2]
CLKBUF_GTLP25 [2]
CLKBUF_GTLP33 [2]
CLKBUF_HSTL_I [2]
CLKBUF_HSTL_II [2]
CLKBUF_SSTL3_I [2]
CLKBUF_SSTL3_II [2]
CLKBUF_SSTL2_I [2]
CLKBUF_SSTL2_II [2]
CLKBUF_LVDS [3]
CLKBUF_LVPECL

Notes:

1. *By default, the CLKBUF macro uses the 3.3 V LVTTL I/O technology. For more details, refer to the* IGLOO, Fusion, and ProASIC3 Macro Library Guide.
2. *I/O standards only supported in ProASIC3E and IGLOOe families.*
3. *BLVDS and M-LVDS standards are supported by CLKBUF_LVDS.*

Global Synthesis Constraints

The Synplify® synthesis tool, by default, allows six clocks in a design for IGLOO and ProASIC3. When more than six clocks are needed in the design, a user synthesis constraint attribute, syn_global_buffers, can be used to control the maximum number of clocks (up to 18) that can be inferred by the synthesis engine.

High-fanout nets will be inferred with clock buffers and/or internal clock buffers. If the design consists of CCC global buffers, they are included in the count of clocks in the design.

The subsections below discuss the clock input source (global buffers with no programmable delays) and the clock conditioning functional block (global buffers with programmable delays and/or PLL function) in detail.

Device-Specific Layout

Two kinds of CCCs are offered in low-power flash devices: CCCs with integrated PLLs, and CCCs without integrated PLLs (simplified CCCs). Table 4-5 lists the number of CCCs in various devices.

Table 4-5 • **Number of CCCs by Device Size and Package**

Device		Package	CCCs with Integrated PLLs	CCCs without Integrated PLLs (simplified CCC)
ProASIC3/ProASIC3L	IGLOO/IGLOO PLUS			
A3P015	AGL015	All	0	2
A3P030	AGL030/AGLP030	All	0	2
A3P060	AGL060/AGLP060	All	1	5
A3P125	AGL125/AGLP125	All	1	5
A3P250/L	AGL250	All	1	5
A3P400		All	1	5
A3P600/L	AGL600	All	1	5
A3P1000/L	AGL1000	All	1	5
A3PE600	AGLE600	PQ208	2	4
A3PE600		All other packages	6	0
A3PE1500		PQ208	2	4
A3PE1500		All other packages	6	0
A3PE3000/L		PQ208	2	4
A3PE3000/L	AGLE3000	All other packages	6	0

This document outlines the following device information: CCC features, PLL core specifications, functional descriptions, software configuration information, detailed usage information, recommended board-level considerations, and other considerations concerning global networks in low-power flash devices.

Clock Conditioning Circuits with Integrated PLLs

Each of the CCCs with integrated PLLs includes the following:

- 1 PLL core, which consists of a phase detector, a low-pass filter, and a four-phase voltage-controlled oscillator
- 3 global multiplexer blocks that steer signals from the global pads and the PLL core onto the global networks
- 6 programmable delays and 1 fixed delay for time advance/delay adjustments

- 5 programmable frequency divider blocks to provide frequency synthesis (automatically configured by the SmartGen macro builder tool)

Clock Conditioning Circuits without Integrated PLLs

Each of the simplified CCCs without integrated PLLs in the low-power flash families is composed of the following:

- 3 global multiplexer blocks that steer signals from the global pads and the programmable delay elements onto the global networks
- 3 programmable delay elements to provide time delay adjustments

CCC Locations

CCCs located in the middle of the east and west sides of the device access the three VersaNet global networks on each side (six total networks), while the four CCCs located in the four corners access three quadrant global networks (twelve total networks). See Figure 4-10.

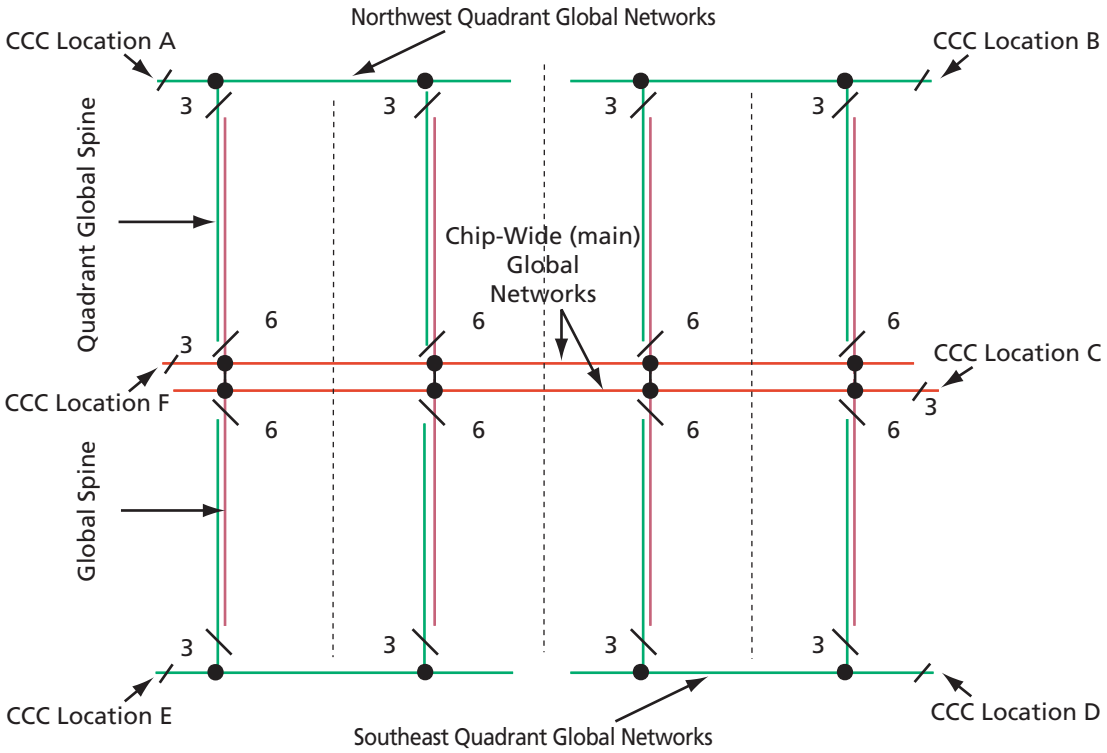


Figure 4-10 **• Global Network Architecture**

The following explains the locations of the CCCs in IGLOO and ProASIC3 devices:

In Figure 4-13 on page 4-16 through Figure 4-14 on page 4-16, CCCs with integrated PLLs are indicated in red, and simplified CCCs are indicated in yellow. There is a letter associated with each location of the CCC, in clockwise order. The upper left corner CCC is named "A," the upper right is named "B," and so on. These names finish up at the middle left with letter "F."

IGLOO and ProASIC3 CCC Locations

In all IGLOO and ProASIC3 devices (except 15 k and 30 k gate devices, which do not contain PLLs), six CCCs are located in the same positions as the IGLOOe and ProASIC3E CCCs. Only one of the CCCs has an integrated PLL and is located in the middle of the west (middle left) side of the device. The

other five CCCs are simplified CCCs and are located in the four corners and the middle of the east side of the device (Figure 4-11).

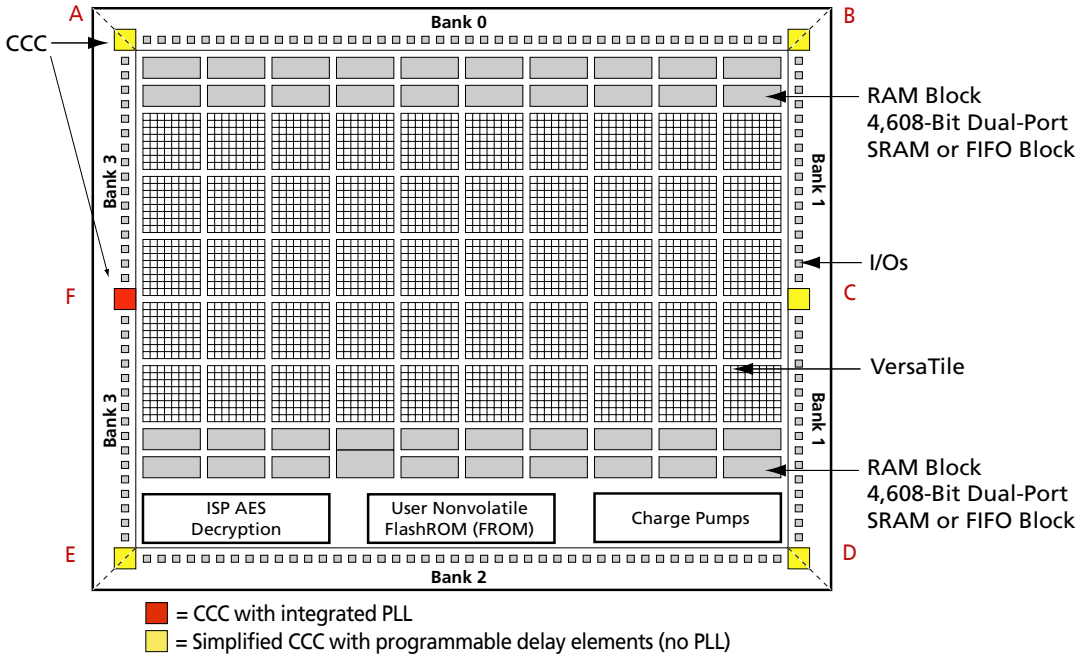


***Figure 4-11* • CCC Locations in IGLOO and ProASIC3 Family Devices (except 15 k and 30 k gate devices)**

Note that the 15 k and 30 k gate devices do not support PLL features. This device has only six global I/O buffers, three each located in the middle of the east and west sides of the device. A CCC functional block is available in each of the two locations, for a total of two CCCs. No quadrant global networks are present in the four corners of this device (Figure 4-12).

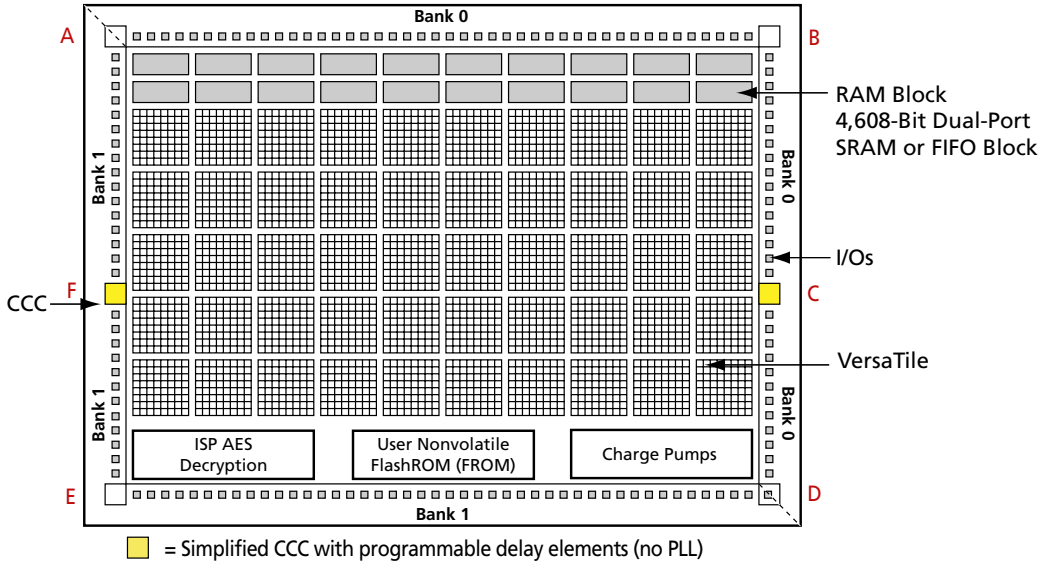


***Figure 4-12* • CCC Locations in the 15 k and 30 k Gate Devices**

IGLOOe and ProASIC3E CCC Locations

IGLOOe and ProASIC3E devices have six CCCs – one in each of the four corners and one each in the middle of the east and west sides of the device (Figure 4-13).

All six CCCs are integrated with PLLs, except in PQFP-208 package devices. PQFP-208 package devices also have six CCCs, of which two include PLLs and four are simplified CCCs. The CCCs with PLLs are implemented in the middle of the east and west (middle right and middle left) sides of the device. The simplified CCCs without PLLs are located in the four corners of the device (Figure 4-14).

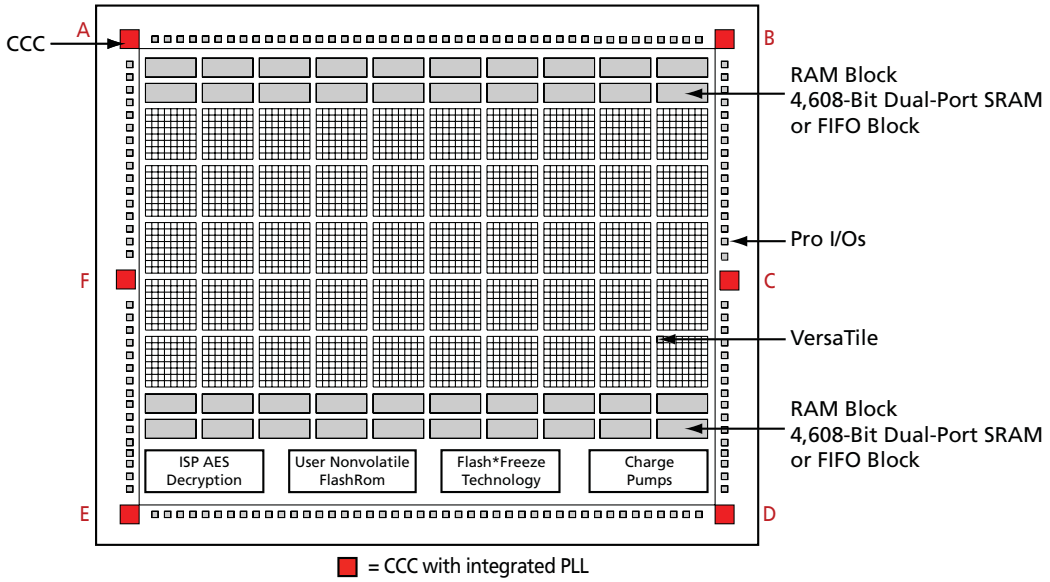


Figure 4-13 • **CCC Locations in IGLOOe and ProASIC3E Family Devices (except PQFP-208 package)**

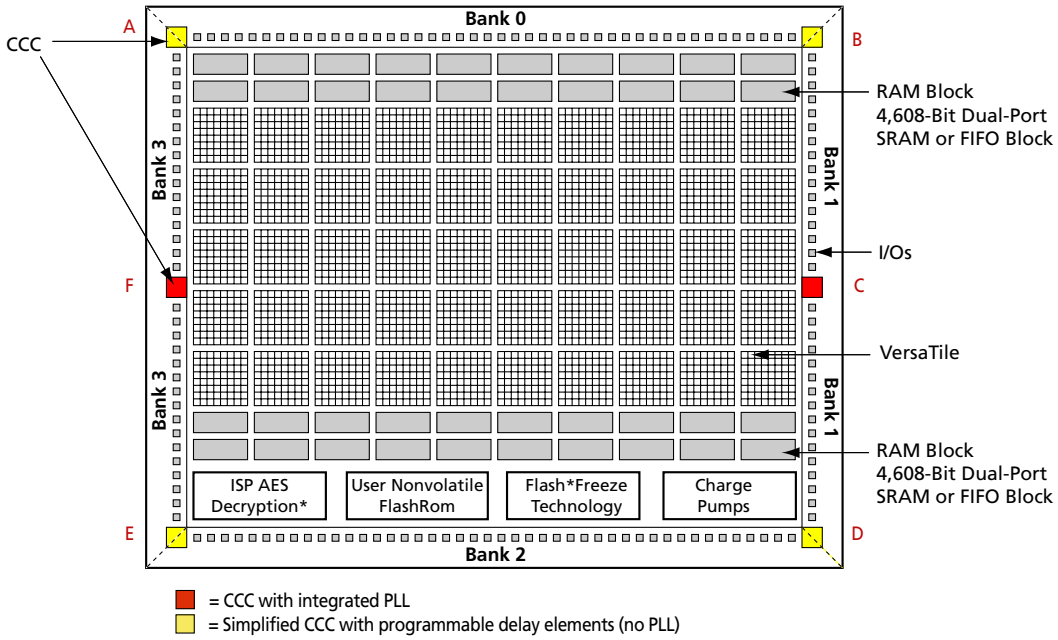


Figure 4-14 • **CCC Locations in ProASIC3E Family Devices (PQFP-208 package)**

PLL Core Specifications

PLL Core Specifications can be found in the DC and Switching Characteristics chapter of the appropriate family datasheet.

Loop Bandwidth

Common design practice for systems with a low-noise input clock is the need to have PLLs with small loop bandwidths to reduce the effects of noise sources at the output. Table 4-6 shows the PLL loop bandwidth, providing a measure of the PLL's ability to track the input clock and jitter.

Table 4-6 • **–3dB Frequency of the PLL**

	Minimum (T_a = +125°C, V_{CCA} = 1.4 V)	Typical (T_a = +25°C, V_{CCA} = 1.5 V)	Maximum (T_a = –55°C, V_{CCA} = 1.6 V)
–3 dB Frequency	15 kHz	25 kHz	45 kHz

PLL Core Operating Principles

This section briefly describes the basic principles of PLL operation. The PLL core is composed of a phase detector (PD), a low-pass filter (LPF), and a four-phase voltage-controlled oscillator (VCO). Figure 4-15 illustrates a basic single-phase PLL core with a divider and delay in the feedback path.

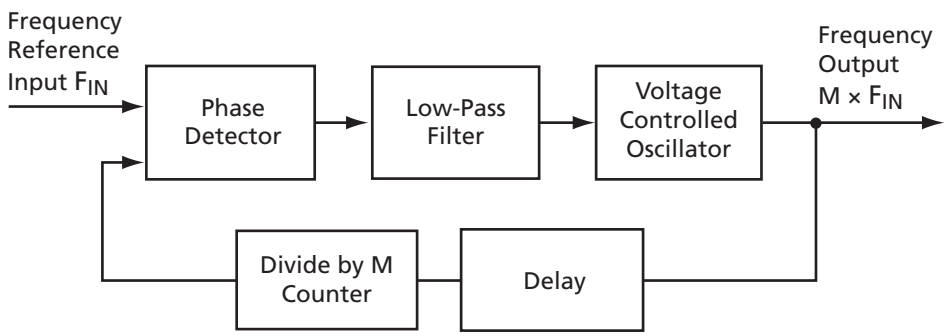


Figure 4-15 • **Simplified PLL Core with Feedback Divider and Delay**

The PLL is an electronic servo loop that phase-aligns the PD feedback signal with the reference input. To achieve this, the PLL dynamically adjusts the VCO output signal according to the average phase difference between the input and feedback signals.

The first element is the PD, which produces a voltage proportional to the phase difference between its inputs. A simple example of a digital phase detector is an Exclusive-OR gate. The second element, the LPF, extracts the average voltage from the phase detector and applies it to the VCO. This applied voltage alters the resonant frequency of the VCO, thus adjusting its output frequency.

Consider Figure 4-15 with the feedback path bypassing the divider and delay elements. If the LPF steadily applies a voltage to the VCO such that the output frequency is identical to the input frequency, this steady-state condition is known as lock. Note that the input and output phases are also identical. The PLL core sets a LOCK output signal HIGH to indicate this condition.

Should the input frequency increase slightly, the PD detects the frequency/phase difference between its reference and feedback input signals. Since the PD output is proportional to the phase difference, the change causes the output from the LPF to increase. This voltage change increases the resonant frequency of the VCO and increases the feedback frequency as a result. The PLL dynamically adjusts in this manner until the PD senses two phase-identical signals and steady-state lock is achieved. The opposite (decreasing PD output signal) occurs when the input frequency decreases.

Now suppose the feedback divider is inserted in the feedback path. As the division factor N is increased, the average phase difference increases. The average phase difference will cause the VCO to increase its frequency until the output signal is phase-identical to the input after undergoing division. In other words, lock in both frequency and phase is achieved when the output frequency is M times the input. Thus, clock division in the feedback path results in multiplication at the output.

A similar argument can be made when the delay element is inserted into the feedback path. To achieve steady-state lock, the VCO output signal will be delayed by the input period *less* the feedback delay. For periodic signals, this is equivalent to time-advancing the output clock by the feedback delay.

Another key parameter of a PLL system is the acquisition time. Acquisition time is the amount of time it takes for the PLL to achieve lock (i.e., phase-align the feedback signal with the input reference clock). For example, suppose there is no voltage applied to the VCO, allowing it to operate at its free-running frequency. Should an input reference clock suddenly appear, a lock would be established within the maximum acquisition time.

Functional Description

This section provides detailed descriptions of PLL block functionality: clock dividers and multipliers, clock delay adjustment, phase adjustment, and dynamic PLL configuration.

Clock Dividers and Multipliers

The PLL block contains five programmable dividers. Figure 4-16 shows a simplified PLL block.

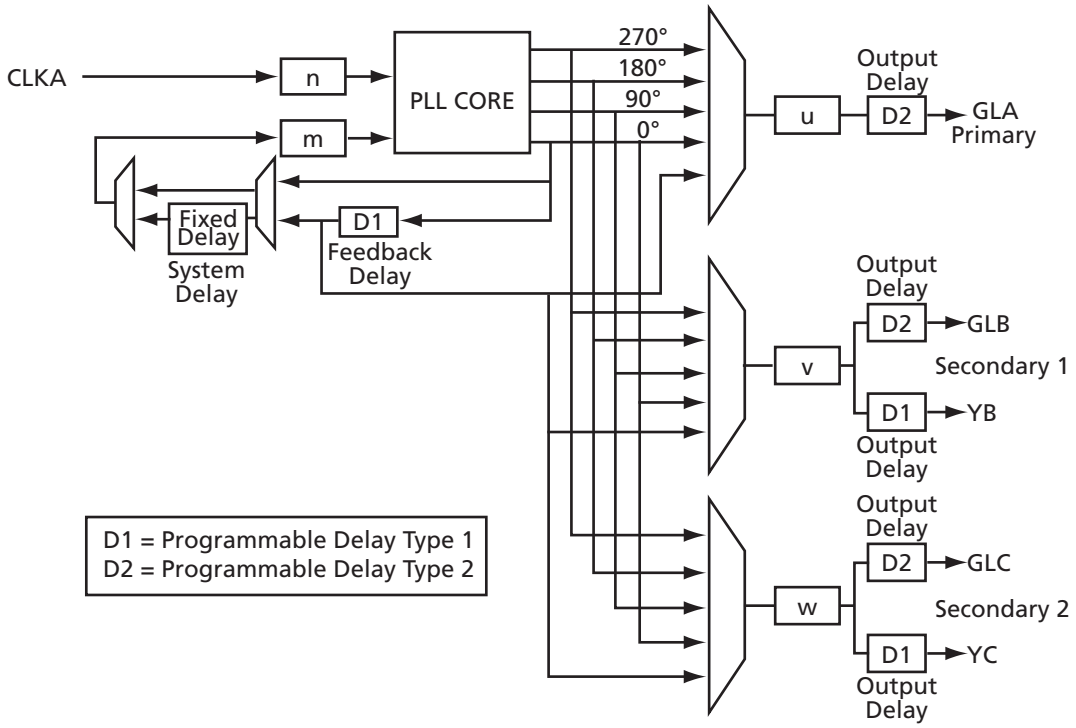


Figure 4-16 • **PLL Block Diagram**

Dividers *n* and *m* (the input divider and feedback divider, respectively) provide integer frequency division factors from 1 to 128. The output dividers *u*, *v*, and *w* provide integer division factors from 1 to 32. Frequency scaling of the reference clock CLKA is performed according to the following formulas:

$$f_{GLA} = f_{CLKA} \times m \ / (n \times u) \text{ – GLA Primary PLL Output Clock}$$

EQ 4-1

$$f_{GLB} = f_{YB} = f_{CLKA} \times m \ / (n \times v) \text{ – GLB Secondary 1 PLL Output Clock(s)}$$

EQ 4-2

$$f_{GLC} = f_{YC} = f_{CLKA} \times m \ / \ (n \times w) \text{ – GLC Secondary 2 PLL Output Clock(s)}$$

EQ 4-3

SmartGen provides a user-friendly method of generating the configured PLL netlist, which includes automatically setting the division factors to achieve the closest possible match to the requested frequencies. Since the five output clocks share the *n* and *m* dividers, the achievable output frequencies are interdependent and related according to the following formula:

$$f_{GLA} = f_{GLB} \times (v / u) = f_{GLC} \times (w / u)$$

EQ 4-4

Clock Delay Adjustment

There are a total of seven configurable delay elements implemented in the PLL architecture.

Two of the delays are located in the feedback path, entitled System Delay and Feedback Delay. System Delay provides a fixed delay of 2 ns (typical), and Feedback Delay provides selectable delay values from 0.6 ns to 5.56 ns in 160 ps increments (typical). For PLLs, delays in the feedback path will effectively advance the output signal from the PLL core with respect to the reference clock. Thus, the System and Feedback delays generate negative delay on the output clock. Additionally, each of these delays can be independently bypassed if necessary.

The remaining five delays perform traditional time delay and are located at each of the outputs of the PLL. Besides the fixed global driver delay of 0.755 ns for each of the global networks, the global multiplexer outputs (GLA, GLB, and GLC) each feature an additional selectable delay value from 0.025 ns to 0.76 ns in the first step, and then to 5.56 ns in 160 ps increments. The additional YB and YC signals have access to a selectable delay from 0.6 ns to 5.56 ns in 160 ps increments (typical). This is the same delay value as the CLKDLY macro. It is similar to CLKDLY, which bypasses the PLL core just to take advantage of the phase adjustment option with the delay value.

The following parameters must be taken into consideration to achieve minimum delay at the outputs (GLA, GLB, GLC, YB, and YC) relative to the reference clock: routing delays from the PLL core to CCC outputs, core outputs and global network output delays, and the feedback path delay. The feedback path delay acts as a time advance of the input clock and will offset any delays introduced beyond the PLL core output. The routing delays are determined from back-annotated simulation and are configuration-dependent.

Phase Adjustment

The output from the PLL core can be phase-adjusted with respect to the reference input clock, CLKA. The user can select a 0°, 90°, 180°, or 270° phase shift independently for each of the outputs YA, GLB/YB, and GLC/YC. Note that each of these phase-adjusted signals may also undergo further frequency division and/or time adjustment via the remaining dividers and delays located at the outputs of the PLL.

Dynamic PLL Configuration

The CCCs can be configured both statically and dynamically.

In addition to the ports available in the Static CCC, the Dynamic CCC has the dynamic shift register signals that enable dynamic reconfiguration of the CCC. With the Dynamic CCC, the ports CLKB and CLKC are also exposed. All three clocks (CLKA, CLKB, and CLKC) can be configured independently.

The CCC block is fully configurable. The following two sources can act as the CCC configuration bits.

Flash Configuration Bits

The flash configuration bits are the configuration bits associated with programmed flash switches. These bits are used when the CCC is in static configuration mode. Once the device is programmed, these bits cannot be modified. They provide the default operating state of the CCC.

Dynamic Shift Register Outputs

This source does not require core reprogramming and allows core-driven dynamic CCC reconfiguration. When the dynamic register drives the configuration bits, the user-defined core circuit takes full control over SDIN, SDOUT, SCLK, SSHIFT, and SUPDATE. The configuration bits can consequently be dynamically changed through shift and update operations in the serial register interface. Access to the logic core is accomplished via the dynamic bits in the specific tiles assigned to the PLLs.

Figure 4-17 illustrates a simplified block diagram of the MUX architecture in the CCCs.

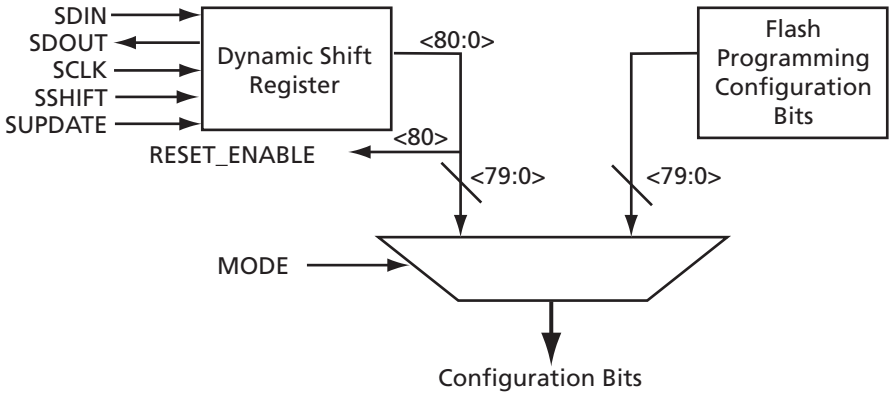


***Figure 4-17* • The CCC Configuration MUX Architecture**

The selection between the flash configuration bits and the bits from the configuration register is made using the MODE signal shown in Figure 4-17. If the MODE signal is logic HIGH, the dynamic shift register configuration bits are selected. There are 81 control bits to configure the different functions of the CCC.

Each group of control bits is assigned a specific location in the configuration shift register. For a list of the 81 configuration bits (C[80:0]) in the CCC and a description of each, refer to "PLL Configuration Bits Description" on page 4-22. The configuration register can be serially loaded with the new configuration data and programmed into the CCC using the following ports:

- SDIN: The configuration bits are serially loaded into a shift register through this port. The LSB of the configuration data bits should be loaded first.
- SDOUT: The shift register contents can be shifted out (LSB first) through this port using the shift operation.
- SCLK: This port should be driven by the shift clock.
- SSHIFT: The active-high shift enable signal should drive this port. The configuration data will be shifted into the shift register if this signal is HIGH. Once SSHIFT goes LOW, the data shifting will be halted.
- SUPDATE: The SUPDATE signal is used to configure the CCC with the new configuration bits when shifting is complete.

To access the configuration ports of the shift register (SDIN, SDOUT, SSHIFT, etc.), the user should instantiate the CCC macro in his design with appropriate ports. Actel recommends that users choose SmartGen to generate the CCC macros with the required ports for dynamic reconfiguration.

Users must familiarize themselves with the architecture of the CCC core and its input, output, and configuration ports to implement the desired delay and output frequency in the CCC structure. Figure 4-18 shows a model of the CCC with configurable blocks and switches.

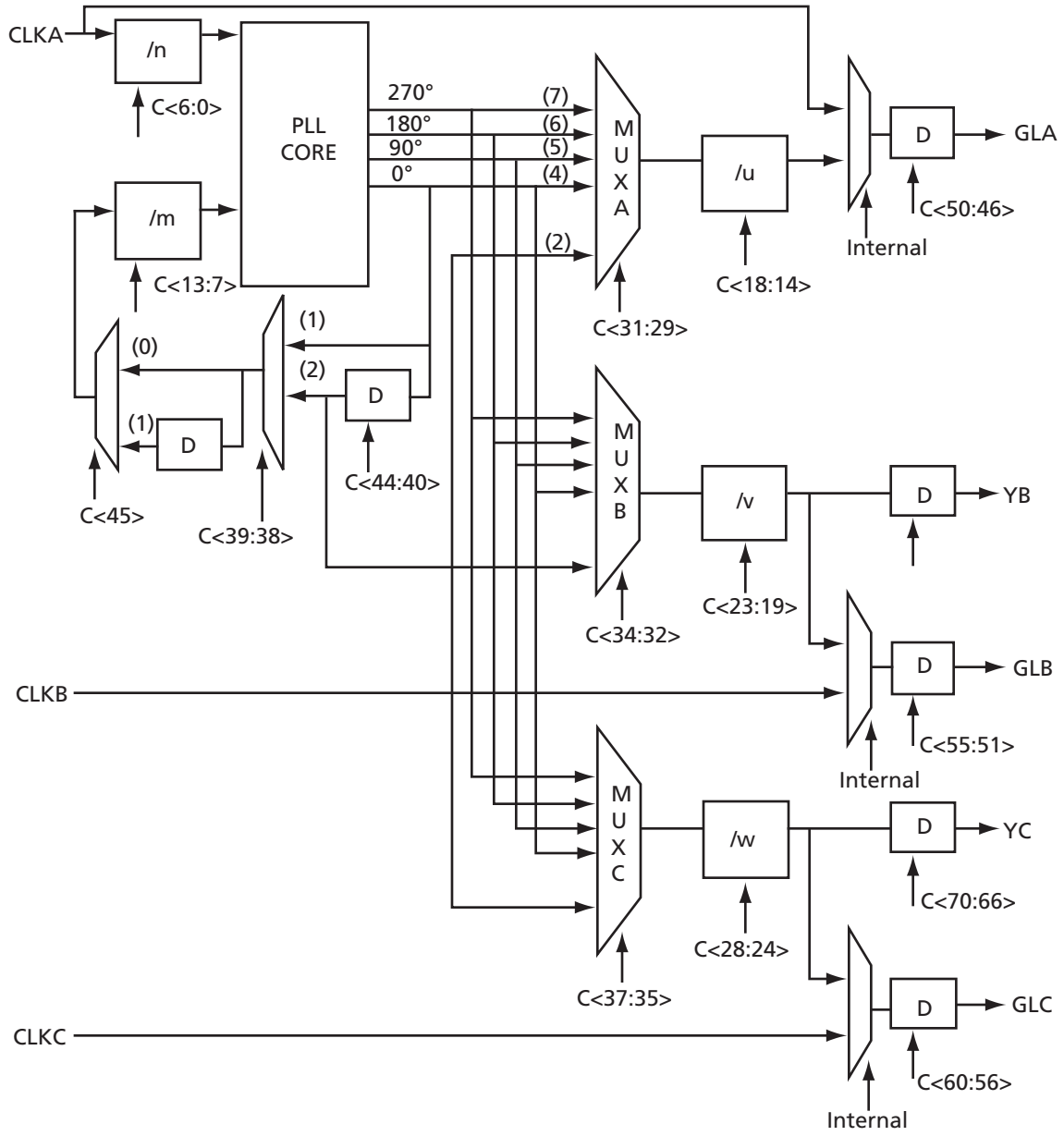


Figure 4-18 • **CCC Block Control Bits – Graphical Representation of Assignments**

Loading the Configuration Register

The most important part of CCC dynamic configuration is to load the shift register properly with the configuration bits. There are different ways to access and load the configuration shift register:

- JTAG Interface
- Logic Core
- Specific I/O Tiles

JTAG Interface

The JTAG interface requires no additional I/O pins. The JTAG TAP controller is used to control the loading of the CCC configuration shift register.

Low-power flash devices provide a user interface macro between the JTAG pins and the device core logic. This macro is called UJTAG. A user should instantiate the UJTAG macro in his design to access the configuration register ports via the JTAG pins.

For more information on CCC dynamic reconfiguration using UJTAG, refer to *UJTAG Applications in Actel's Low-Power Flash Devices.*

Logic Core

If the logic core is employed, the user must design a module to provide the configuration data and control the shifting and updating of the CCC configuration shift register. In effect, this is a user-designed TAP controller, which requires additional chip resources.

Specific I/O Tiles

If specific I/O tiles are used for configuration, the user must provide the external equivalent of a TAP controller. This does not require additional core resources but does use pins.

Shifting the Configuration Data

To enter a new configuration, all 81 bits must shift in via SDIN. After all bits are shifted, SSHIFT must go LOW and SUPDATE HIGH to enable the new configuration. For simulation purposes, bits <71:73> and <77:80> are "don't cares."

The SUPDATE signal must be LOW during any clock cycle where SSHIFT is active. After SUPDATE is asserted, it must go back to the LOW state until a new update is required.

PLL Configuration Bits Description

Table 4-7 • **Configuration Bit Descriptions for the CCC Blocks**

Config. Bits	Signal	Name	Description
80	RESETEN	Reset Enable	Enables (active high) the synchronization of PLL output dividers after dynamic reconfiguration (SUPDATE). The Reset Enable signal is READ-ONLY and should not be modified via dynamic reconfiguration.
79	DYNCSEL	Clock Input C Dynamic Select	Configures clock input C to be sent to GLC for dynamic control.*
78	DYNBSEL	Clock Input B Dynamic Select	Configures clock input B to be sent to GLB for dynamic control.*
77	DYNASEL	Clock Input A Dynamic Select	Configures clock input A for dynamic PLL configuration.*
<76:74>	VCOSEL[2:0]	VCO Gear Control	Three-bit VCO Gear Control for four frequency ranges
73	STATCSEL	MUX Select on Input C	MUX selection for clock input C*
72	STATBSEL	MUX Select on Input B	MUX selection for clock input B*
71	STATASEL	MUX Select on Input A	MUX selection for clock input A*
<70:66>	DLYC[4:0]	YC Output Delay	Sets the output delay value for YC.
<65:61>	DLYB[4:0]	YB Output Delay	Sets the output delay value for YB.
<60:56>	DLYGLC[4:0]	GLC Output Delay	Sets the output delay value for GLC.
<55:51>	DLYGLB[4:0]	GLB Output Delay	Sets the output delay value for GLB.
<50:46>	DLYGLA[4:0]	Primary Output Delay	Primary, GLA Output Delay

* *This value depends on the input clock source, so Layout must complete before these bits can be set. After completing Layout in Designer, generate the "CCC_Configuration" report by choosing* ***Tools*** > ***Report*** > ***CCC_Configuration****. The report contains the appropriate settings for these bits.*

Table 4-7 • **Configuration Bit Descriptions for the CCC Blocks (continued)**

Config. Bits	Signal	Name	Description
45	XDLYSEL	System Delay Select	When selected, inserts System Delay in the feedback path in Figure 4-16 on page 4-18.
<44:40>	FBDLY[4:0]	Feedback Delay	Sets the feedback delay value for the feedback element in Figure 4-16 on page 4-18.
<39:38>	FBSEL[1:0]	Primary Feedback Delay Select	Controls the feedback MUX: no delay, include programmable delay element, or use external feedback.
<37:35>	OCMUX[2:0]	Secondary 2 Output Select	Selects from the VCO's four phase outputs for GLC/YC.
<34:32>	OBMUX[2:0]	Secondary 1 Output Select	Selects from the VCO's four phase outputs for GLB/YB.
<31:29>	OAMUX[2:0]	GLA Output Select	Selects from the VCO's four phase outputs for GLA.
<28:24>	OCDIV[4:0]	Secondary 2 Output Divider	Sets the divider value for the GLC/YC outputs. Also known as divider *w* in Figure 4-16 on page 4-18. The divider value will be OCDIV[4:0] + 1.
<23:19>	OBDIV[4:0]	Secondary 1 Output Divider	Sets the divider value for the GLB/YB outputs. Also known as divider *v* in Figure 4-16 on page 4-18. The divider value will be OBDIV[4:0] + 1.
<18:14>	OADIV[4:0]	Primary Output Divider	Sets the divider value for the GLA output. Also known as divider *u* in Figure 4-16 on page 4-18. The divider value will be OADIV[4:0] + 1.
<13:7>	FBDIV[6:0]	Feedback Divider	Sets the divider value for the PLL core feedback. Also known as divider *m* in Figure 4-16 on page 4-18. The divider value will be FBDIV[6:0] + 1.
<6:0>	FINDIV[6:0]	Input Divider	Input Clock Divider (/n). Sets the divider value for the input delay on CLKA. The divider value will be FINDIV[6:0] + 1.

* *This value depends on the input clock source, so Layout must complete before these bits can be set. After completing Layout in Designer, generate the "CCC_Configuration" report by choosing* ***Tools*** > ***Report*** > ***CCC_Configuration****. The report contains the appropriate settings for these bits.*

Table 4-8 to Table 4-14 on page 4-25 provide descriptions of the configuration data for the configuration bits.

Table 4-8 • **Input Clock (fin) Divider, (/n) (used as frequency divider)**

FINDIV<6:0> State	Divisor	New Frequency Factor
0	1	1.00000
1	2	0.50000
⋮	⋮	⋮
127	128	0.0078125

Table 4-9 • **Feedback Signal (fbin) Divider, (/m) (used as frequency multiplier)**

FBDIV<6:0> State	Divisor	New Frequency Factor
0	1	1
1	2	2
⋮	⋮	⋮
127	128	128

Table 4-10 • **Output Frequency Dividers**
A **Output Divider, OADIV <4:0> (/u);**
B **Output Divider, OBDIV <4:0> (/v);**
C **Output Divider, OCDIV <4:0> (/w)**

OADIV<4:0>; OBDIV<4:0>; CDIV<4:0> State	Divisor	New Frequency Factor
0	1	1.00000
1	2	0.50000
⋮	⋮	⋮
31	32	0.03125

Table 4-11 • **MUXA, MUXB, MUXC**

OAMUX<2:0>; OBMUX<2:0>; OCMUX<2:0> State	MUX Input Selected
0	None. Six-input MUX and PLL are bypassed. Clock passes only through global MUX and goes directly into HC ribs.
1	Not available
2	PLL feedback delay line output
3	Not used
4	PLL VCO 0° phase shift
5	PLL VCO 90° phase shift
6	PLL VCO 180° phase shift
7	PLL VCO 270° phase shift

Table 4-12 • **2-Bit Feedback MUX**

FBSEL<1:0> State	MUX Input Selected
0	Ground. Used for power-down mode in power-down logic block.
1	PLL VCO 0° phase shift
2	PLL delayed VCO 0° phase shift
3	N/A

Table 4-13 • **Programmable Delay Selection for Feedback Delay and Secondary Core Output Delays**

FBDLY<4:0>; DLYYB<4:0>; DLYYC<4:0> State	Delay Value
0	Typical delay = 600 ps
1	Typical delay = 760 ps
2	Typical delay = 920 ps
⋮	⋮
31	Typical delay = 5.56 ns

Table 4-14 • **Programmable Delay Selection for Global Clock Output Delays**

DLYGLA<4:0>; DLYGLB<4:0>; DLYGLC<4:0> State	Delay Value
0	Typical delay = 225 ps
1	Typical delay = 760 ps
2	Typical delay = 920 ps
⋮	⋮
31	Typical delay = 5.56 ns

Software Configuration

SmartGen automatically generates the desired CCC functional block by configuring the control bits, and allows the user to select two CCC modes: Static PLL and Delayed Clock (CLKDLY).

Static PLL Configuration

The newly implemented Visual PLL Configuration Wizard feature provides the user a quick and easy way to configure the PLL with the desired settings (Figure 4-19 on page 4-26). The user can invoke SmartGen to set the parameters and generate the netlist file with the appropriate flash configuration bits set for the CCCs. As mentioned in "PLL Macro Block Diagram" on page 4-8, the input reference clock CLKA can be configured to be driven by Hardwired I/O, External I/O, or Core Logic. The user enters the desired settings for all the parameters (output frequency, output selection, output phase adjustment, clock delay, feedback delay, and system delay). Notice that the actual values (divider values, output frequency, delay values, and phase) are shown to aid the user in reaching the desired design frequency in real time. These values are typical-case data. Best- and worst-case data can be observed through static timing analysis in SmartTime within Designer.

For dynamic configuration, the CCC parameters are defined using either the external JTAG port or an internally defined serial interface via the built-in dynamic shift register. This feature provides the ability to compensate for changes in the external environment.

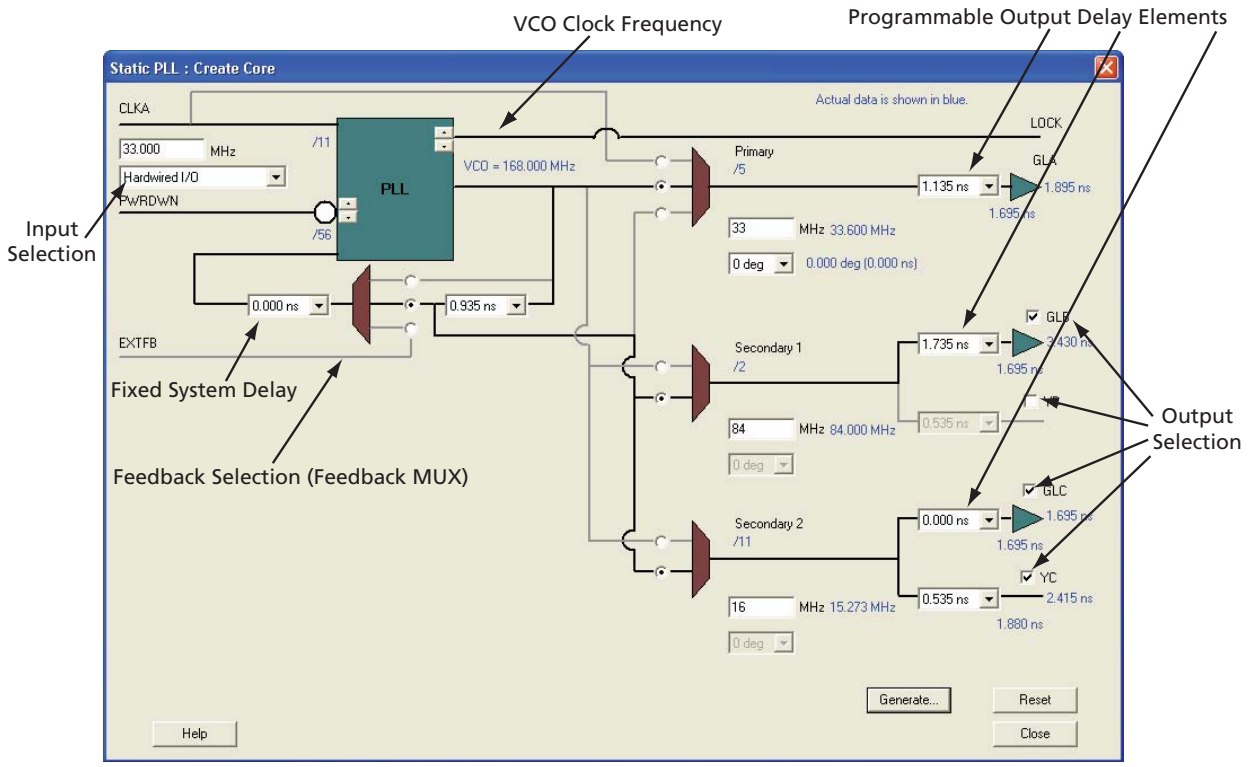


Figure 4-19 • **Visual PLL Configuration Wizard**

Feedback Configuration

The PLL provides both internal and external feedback delays. Depending on the configuration, various combinations of feedback delays can be achieved.

Internal Feedback Configuration

This configuration essentially sets the feedback multiplexer to route the VCO output of the PLL Core as the input to the feedback of the PLL. The feedback signal may be processed with the fixed system and the adjustable feedback delay, as shown in Figure 4-20. The dividers are automatically configured by SmartGen based on the user input.

Indicated below is the System Delay pull-down menu. The System Delay can be bypassed by setting it to 0. When set, it adds a 2 ns delay to the feedback path (which results in delay advancement of the output clock by 2 ns).

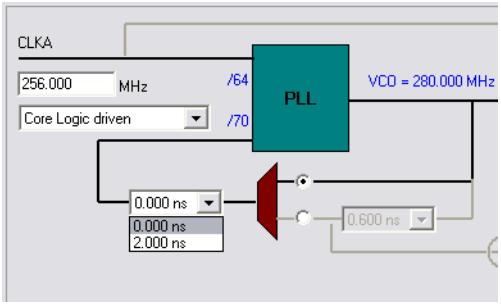


Figure 4-20 • **Internal Feedback with Selectable System Delay**

Figure 4-21 shows the controllable Feedback Delay. If set properly in conjunction with the fixed System Delay, the total output delay can be advanced significantly.

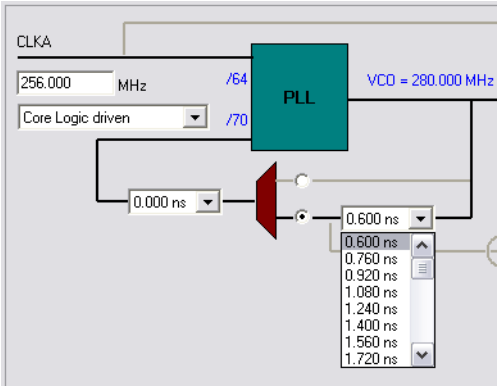


Figure 4-21 **• Internal Feedback with Selectable Feedback Delay**

External Feedback Configuration

For certain applications, such as those requiring generation of PCB clocks that must be matched with existing board delays, it is useful to implement an external feedback EXTFB. The Phase Detector of the PLL core will receive CLKA and EXTFB as inputs. EXTFB may be processed by the fixed System Delay element as well as the *M* divider element. The EXTFB option is currently not supported.

After setting all the required parameters, users can generate one or more PLL configurations with HDL or EDIF descriptions by clicking the **Generate** button. SmartGen enables them to save the session results and messages in a log file:

```
****************
Macro Parameters
****************

Name                            : test_pll
Family                          : ProASIC3E
Output Format                   : VHDL
Type                            : Static PLL
Input Freq(MHz)                 : 10.000
CLKA Source                     : Hardwired I/O
Feedback Delay Value Index      : 1
Feedback Mux Select             : 2
XDLY Mux Select                 : No
Primary Freq(MHz)               : 33.000
Primary PhaseShift              : 0
Primary Delay Value Index       : 1
Primary Mux Select              : 4
Secondary1 Freq(MHz)            : 66.000
Use GLB                         : YES
Use YB                          : YES
GLB Delay Value Index           : 1
YB Delay Value Index            : 1
Secondary1 PhaseShift           : 0
Secondary1 Mux Select           : 4
Secondary2 Freq(MHz)            : 101.000
Use GLC                         : YES
Use YC                          : NO
GLC Delay Value Index           : 1
YC Delay Value Index            : 1
Secondary2 PhaseShift           : 0
Secondary2 Mux Select           : 4
```

```
…
…
…

Primary Clock frequency 33.333
Primary Clock Phase Shift 0.000
Primary Clock Output Delay from CLKA 0.180

Secondary1 Clock frequency 66.667
Secondary1 Clock Phase Shift 0.000
Secondary1 Clock Global Output Delay from CLKA 0.180
Secondary1 Clock Core Output Delay from CLKA 0.625

Secondary2 Clock frequency 100.000
Secondary2 Clock Phase Shift 0.000
Secondary2 Clock Global Output Delay from CLKA 0.180
```

Below is an example Verilog HDL description of a legal PLL core configuration generated by SmartGen:

```
module test_pll(POWERDOWN,CLKA,LOCK,GLA);
input POWERDOWN, CLKA;
output  LOCK, GLA;

    wire VCC, GND;

    VCC VCC_1_net(.Y(VCC));
    GND GND_1_net(.Y(GND));
    PLL Core(.CLKA(CLKA), .EXTFB(GND), .POWERDOWN(POWERDOWN),
        .GLA(GLA), .LOCK(LOCK), .GLB(), .YB(), .GLC(), .YC(),
        .OADIV0(GND), .OADIV1(GND), .OADIV2(GND), .OADIV3(GND),
        .OADIV4(GND), .OAMUX0(GND), .OAMUX1(GND), .OAMUX2(VCC),
        .DLYGLA0(GND), .DLYGLA1(GND), .DLYGLA2(GND), .DLYGLA3(GND)
        , .DLYGLA4(GND), .OBDIV0(GND), .OBDIV1(GND), .OBDIV2(GND),
        .OBDIV3(GND), .OBDIV4(GND), .OBMUX0(GND), .OBMUX1(GND),
        .OBMUX2(GND), .DLYYB0(GND), .DLYYB1(GND), .DLYYB2(GND),
        .DLYYB3(GND), .DLYYB4(GND), .DLYGLB0(GND), .DLYGLB1(GND),
        .DLYGLB2(GND), .DLYGLB3(GND), .DLYGLB4(GND), .OCDIV0(GND),
        .OCDIV1(GND), .OCDIV2(GND), .OCDIV3(GND), .OCDIV4(GND),
        .OCMUX0(GND), .OCMUX1(GND), .OCMUX2(GND), .DLYYC0(GND),
        .DLYYC1(GND), .DLYYC2(GND), .DLYYC3(GND), .DLYYC4(GND),
        .DLYGLC0(GND), .DLYGLC1(GND), .DLYGLC2(GND), .DLYGLC3(GND)
        , .DLYGLC4(GND), .FINDIV0(VCC), .FINDIV1(GND), .FINDIV2(
        VCC), .FINDIV3(GND), .FINDIV4(GND), .FINDIV5(GND),
        .FINDIV6(GND), .FBDIV0(VCC), .FBDIV1(GND), .FBDIV2(VCC),
        .FBDIV3(GND), .FBDIV4(GND), .FBDIV5(GND), .FBDIV6(GND),
        .FBDLY0(GND), .FBDLY1(GND), .FBDLY2(GND), .FBDLY3(GND),
        .FBDLY4(GND), .FBSEL0(VCC), .FBSEL1(GND), .XDLYSEL(GND),
        .VCOSEL0(GND), .VCOSEL1(GND), .VCOSEL2(GND));
    defparam Core.VCOFREQUENCY = 33.000;
endmodule
```

The "PLL Configuration Bits Description" section on page 4-22 provides descriptions of the PLL configuration bits and is provided only for completeness. The configuration bits are shown as busses only for purposes of illustration. They will actually be broken up into individual pins in compilation libraries and all simulation models. For example, the FBSEL[1:0] bus will actually appear as pins FBSEL1 and FBSEL0. The setting of these select lines for the static PLL configuration is performed by the software and is completely transparent to the user.

Dynamic PLL Configuration

To generate a dynamically reconfigurable CCC, the user should select **Dynamic CCC** in the configuration section of the SmartGen GUI (Figure 4-22). This will generate both the CCC core and the configuration shift register / control bit MUX.

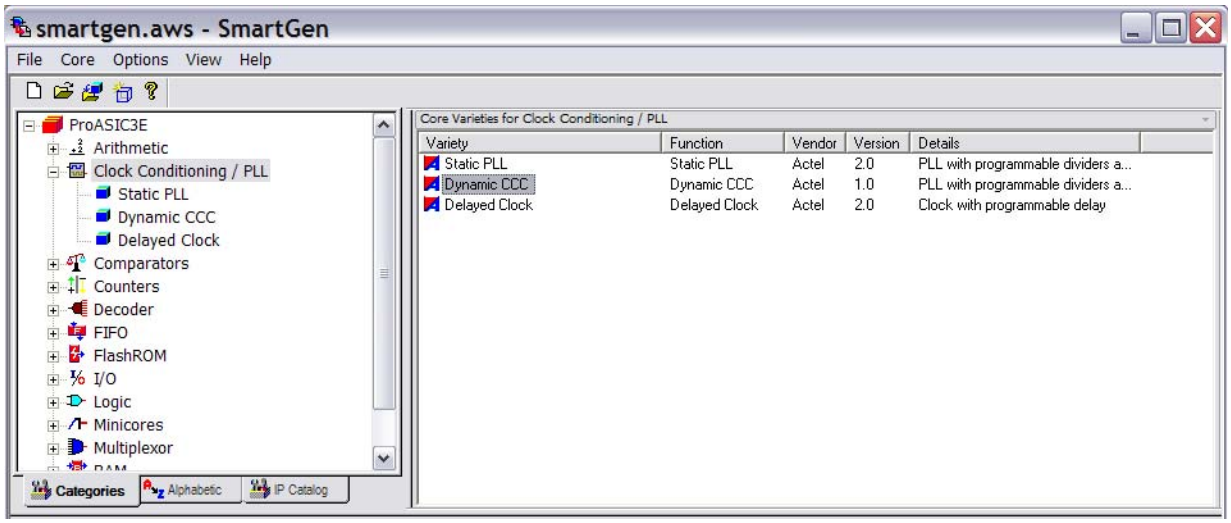


Figure 4-22 • **SmartGen GUI**

Even if dynamic configuration is selected in SmartGen, the user still must specify the static configuration data for the CCC (Figure 4-23). The specified static configuration is used whenever the MODE signal is set to LOW and the CCC is required to function in the static mode. The static configuration data can be used as the default behavior of the CCC where required.

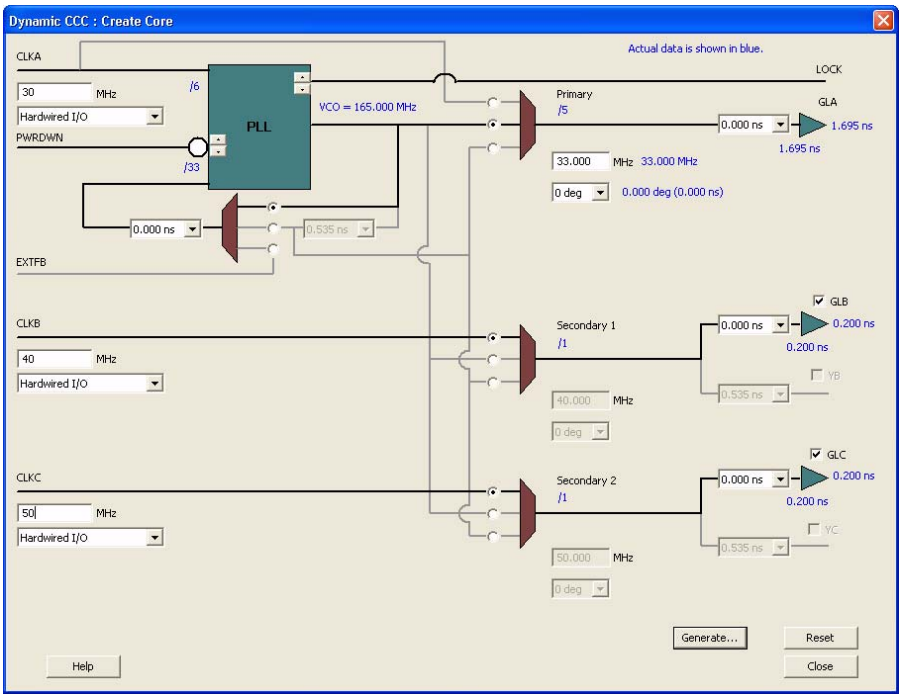


Figure 4-23 • **Dynamic CCC Configuration in SmartGen**

When SmartGen is used to define the configuration that will be shifted in via the serial interface, SmartGen prints out the values of the 81 configuration bits. For ease of use, several configuration bits are automatically inferred by SmartGen when the dynamic PLL core is generated; however, <71:73> (STATASEL, STATBSEL, STATCSEL) and <77:79> (DYNASEL, DYNBSEL, DYNCSEL) depend on the input clock source of the corresponding CCC. Users must first run Layout in Designer to determine the exact setting for these ports. After Layout is complete, generate the "CCC_Configuration" report by choosing **Tools** > **Reports** > **CCC_Configuration** in the Designer software. Refer to "PLL Configuration Bits Description" on page 4-22 for descriptions of the PLL configuration bits. For simulation purposes, bits <71:73> and <78:80> are "don't cares." Therefore, it is strongly suggested that SmartGen be used to generate the correct configuration bit settings for the dynamic PLL core.

After setting all the required parameters, users can generate one or more PLL configurations with HDL or EDIF descriptions by clicking the **Generate** button. SmartGen enables them to save the session results and messages in a log file:

```
****************
Macro Parameters
****************

Name                            : dyn_pll_hardio
Family                          : ProASIC3E
Output Format                   : VERILOG
Type                            : Dynamic CCC
Input Freq(MHz)                 : 30.000
CLKA Source                     : Hardwired I/O
Feedback Delay Value Index      : 1
Feedback Mux Select             : 1
XDLY Mux Select                 : No
Primary Freq(MHz)               : 33.000
Primary PhaseShift              : 0
Primary Delay Value Index       : 1
Primary Mux Select              : 4
Secondary1 Freq(MHz)            : 40.000
Use GLB                         : YES
Use YB                          : NO
GLB Delay Value Index           : 1
YB Delay Value Index            : 1
Secondary1 PhaseShift           : 0
Secondary1 Mux Select           : 0
Secondary1 Input Freq(MHz)      : 40.000
CLKB Source                     : Hardwired I/O
Secondary2 Freq(MHz)            : 50.000
Use GLC                         : YES
Use YC                          : NO
GLC Delay Value Index           : 1
YC Delay Value Index            : 1
Secondary2 PhaseShift           : 0
Secondary2 Mux Select           : 0
Secondary2 Input Freq(MHz)      : 50.000
CLKC Source                     : Hardwired I/O

Configuration Bits:
FINDIV[6:0]     0000101
FBDIV[6:0]      0100000
OADIV[4:0]      00100
OBDIV[4:0]      00000
OCDIV[4:0]      00000
OAMUX[2:0]      100
OBMUX[2:0]      000
OCMUX[2:0]      000
FBSEL[1:0]      01
FBDLY[4:0]      00000
XDLYSEL         0
DLYGLA[4:0]     00000
```

```
DLYGLB[4:0]     00000
DLYGLC[4:0]     00000
DLYYB[4:0]      00000
DLYYC[4:0]      00000
VCOSEL[2:0]     100

Primary Clock Frequency 33.000
Primary Clock Phase Shift 0.000
Primary Clock Output Delay from CLKA 1.695

Secondary1 Clock Frequency 40.000
Secondary1 Clock Phase Shift 0.000
Secondary1 Clock Global Output Delay from CLKB 0.200

Secondary2 Clock Frequency 50.000
Secondary2 Clock Phase Shift 0.000
Secondary2 Clock Global Output Delay from CLKC 0.200

#####################################
# Dynamic Stream Data
#####################################
-------------------------------------
|NAME    |SDIN     |VALUE   |TYPE     |
-------------------------------------
|FINDIV  |[6:0]    |0000101 |EDIT     |
|FBDIV   |[13:7]   |0100000 |EDIT     |
|OADIV   |[18:14]  |00100   |EDIT     |
|OBDIV   |[23:19]  |00000   |EDIT     |
|OCDIV   |[28:24]  |00000   |EDIT     |
|OAMUX   |[31:29]  |100     |EDIT     |
|OBMUX   |[34:32]  |000     |EDIT     |
|OCMUX   |[37:35]  |000     |EDIT     |
|FBSEL   |[39:38]  |01      |EDIT     |
|FBDLY   |[44:40]  |00000   |EDIT     |
|XDLYSEL |[45]     |0       |EDIT     |
|DLYGLA  |[50:46]  |00000   |EDIT     |
|DLYGLB  |[55:51]  |00000   |EDIT     |
|DLYGLC  |[60:56]  |00000   |EDIT     |
|DLYYB   |[65:61]  |00000   |EDIT     |
|DLYYC   |[70:66]  |00000   |EDIT     |
|STATASEL|[71]     |X       |MASKED   |
|STATBSEL|[72]     |X       |MASKED   |
|STATCSEL|[73]     |X       |MASKED   |
|VCOSEL  |[76:74]  |100     |EDIT     |
|DYNASEL |[77]     |X       |MASKED   |
|DYNBSEL |[78]     |X       |MASKED   |
|DYNCSEL |[79]     |X       |MASKED   |
|RESETEN |[80]     |1       |READONLY |
```

The resultant Verilog HDL description of a legal dynamic PLL core configuration generated by SmartGen is as follows:

```
module dyn_pll_macro(POWERDOWN, CLKA, LOCK, GLA, GLB, GLC, SDIN, SCLK, SSHIFT, SUPDATE,
  MODE, SDOUT, CLKB, CLKC);

input POWERDOWN, CLKA;
output  LOCK, GLA, GLB, GLC;
input  SDIN, SCLK, SSHIFT, SUPDATE, MODE;
output  SDOUT;
input  CLKB, CLKC;

  wire VCC, GND;

  VCC VCC_1_net(.Y(VCC));
  GND GND_1_net(.Y(GND));
```

```
  DYNCCC Core(.CLKA(CLKA), .EXTFB(GND), .POWERDOWN(POWERDOWN), .GLA(GLA), .LOCK(LOCK),
    .CLKB(CLKB), .GLB(GLB), .YB(), .CLKC(CLKC), .GLC(GLC), .YC(), .SDIN(SDIN),
    .SCLK(SCLK), .SSHIFT(SSHIFT), .SUPDATE(SUPDATE), .MODE(MODE), .SDOUT(SDOUT),
    .OADIV0(GND), .OADIV1(GND), .OADIV2(VCC), .OADIV3(GND), .OADIV4(GND), .OAMUX0(GND),
    .OAMUX1(GND), .OAMUX2(VCC), .DLYGLA0(GND), .DLYGLA1(GND), .DLYGLA2(GND),
    .DLYGLA3(GND), .DLYGLA4(GND), .OBDIV0(GND), .OBDIV1(GND), .OBDIV2(GND),
    .OBDIV3(GND), .OBDIV4(GND), .OBMUX0(GND), .OBMUX1(GND), .OBMUX2(GND), .DLYYB0(GND),
    .DLYYB1(GND), .DLYYB2(GND), .DLYYB3(GND), .DLYYB4(GND), .DLYGLB0(GND),
    .DLYGLB1(GND), .DLYGLB2(GND), .DLYGLB3(GND), .DLYGLB4(GND), .OCDIV0(GND),
    .OCDIV1(GND), .OCDIV2(GND), .OCDIV3(GND), .OCDIV4(GND), .OCMUX0(GND), .OCMUX1(GND),
    .OCMUX2(GND), .DLYYC0(GND), .DLYYC1(GND), .DLYYC2(GND), .DLYYC3(GND), .DLYYC4(GND),
    .DLYGLC0(GND), .DLYGLC1(GND), .DLYGLC2(GND), .DLYGLC3(GND), .DLYGLC4(GND),
    .FINDIV0(VCC), .FINDIV1(GND), .FINDIV2(VCC), .FINDIV3(GND), .FINDIV4(GND),
    .FINDIV5(GND), .FINDIV6(GND), .FBDIV0(GND), .FBDIV1(GND), .FBDIV2(GND),
    .FBDIV3(GND), .FBDIV4(GND), .FBDIV5(VCC), .FBDIV6(GND), .FBDLY0(GND), .FBDLY1(GND),
    .FBDLY2(GND), .FBDLY3(GND), .FBDLY4(GND), .FBSEL0(VCC), .FBSEL1(GND),
    .XDLYSEL(GND), .VCOSEL0(GND), .VCOSEL1(GND), .VCOSEL2(VCC));
  defparam Core.VCOFREQUENCY = 165.000;

endmodule
```

Delayed Clock Configuration

The CLKDLY macro can be generated with the desired delay and input clock source (Hardwired I/O, External I/O, or Core Logic), as in Figure 4-24.

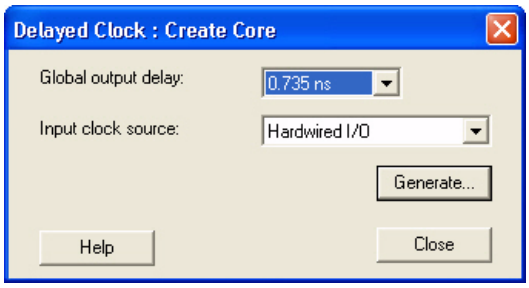


Figure 4-24 **• Delayed Clock Configuration Dialog Box**

After setting all the required parameters, users can generate one or more PLL configurations with HDL or EDIF descriptions by clicking the **Generate** button. SmartGen enables them to save the session results and messages in a log file:

```
****************
Macro Parameters
****************

Name                            : delay_macro
Family                          : ProASIC3
Output Format                   : Verilog
Type                            : Delayed Clock
Delay Index                     : 2
CLKA Source                     : Hardwired I/O

Total Clock Delay = 0.935 ns.

The resultant CLKDLY macro Verilog netlist is as follows:

module delay_macro(GL,CLK);

output GL;
input  CLK;
```

```
  wire VCC, GND;

  VCC VCC_1_net(.Y(VCC));
  GND GND_1_net(.Y(GND));
  CLKDLY Inst1(.CLK(CLK), .GL(GL), .DLYGL0(VCC), .DLYGL1(GND), .DLYGL2(VCC),
    .DLYGL3(GND), .DLYGL4(GND));

endmodule
```

Detailed Usage Information

Clock Frequency Synthesis

Deriving clocks of various frequencies from a single reference clock is known as frequency synthesis. The PLL has an input frequency range from 1.5 to 350 MHz. This frequency is automatically divided down to a range between 1.5 MHz and 5.5 MHz by input dividers (not shown) between PLL macro inputs and PLL phase detector inputs. The VCO output is capable of an output range from 24 to 350 MHz. With dividers before the input to the PLL core and following the VCO outputs, the VCO output frequency can be divided to provide the final frequency range from 0.75 to 350 MHz. Using SmartGen, the dividers are automatically set to achieve the closest possible matches to the specified output frequencies.

Users should be cautious when selecting the desired PLL input and output frequencies and the I/O buffer standard used to connect to the PLL input and output clocks. Depending on the I/O standards used for the PLL input and output clocks, the I/O frequencies have different maximum limits. Refer to the family datasheets for specifications of maximum I/O frequencies for supported I/O standards. Desired PLL input or output frequencies will not be achieved if the selected frequencies are higher than the maximum I/O frequencies allowed by the selected I/O standards. Users should be careful when selecting the I/O standards used for PLL input and output clocks. Performing post-layout simulation can help detect this type of error, which will be identified with pulse width violation errors. Users are strongly encouraged to perform post-layout simulation to ensure the I/O standard used can provide the desired PLL input or output frequencies. Users can also choose to cascade PLLs together to achieve the high frequencies needed for their applications. Details of cascading PLLs are discussed in the "Cascading CCCs" section on page 4-38.

In SmartGen, the actual generated frequency (under typical operating conditions) will be displayed beside the requested output frequency value. This provides the ability to determine the exact frequency that can be generated by SmartGen, in real time. The log file generated by SmartGen is a useful tool in determining how closely the requested clock frequencies match the user specifications. For example, assume a user specifies 101 MHz as one of the secondary output frequencies. If the best output frequency that could be achieved were 100 MHz, the log file generated by SmartGen would indicate the actual generated frequency.

Simulation Verification

The integration of the generated PLL and CLKDLY modules is similar to any VHDL component or Verilog module instantiation in a larger design; i.e., there is no special requirement that users need to take into account to successfully synthesize their designs.

For simulation purposes, users need to refer to the VITAL or Verilog library that includes the functional description and associated timing parameters. Refer to the Software Tools section of the Actel website to obtain the family simulation libraries. If Actel Designer is installed, these libraries are stored in the following locations:

<Designer_Installation_Directory>\lib\vtl\95\proasic3.vhd

<Designer_Installation_Directory>\lib\vtl\95\proasic3e.vhd

<Designer_Installation_Directory>\lib\vlog\ proasic3.v

<Designer_Installation_Directory>\lib\vlog\ proasic3e.v

For Libero IDE users, there is no need to compile the simulation libraries, as they are conveniently pre-compiled in the Model*Sim*® Actel simulation tool.

The following is an example of a PLL configuration utilizing the clock frequency synthesis and clock delay adjustment features. The steps include generating the PLL core with SmartGen, performing simulation for verification with Model*Sim*, and performing static timing analysis with SmartTime in Designer.

Parameters of the example PLL configuration:

Input Frequency – 20 MHz

Primary Output Requirement – 20 MHz with clock advancement of 3.02 ns

Secondary 1 Output Requirement – 40 MHz with clock delay of 2.515 ns

Figure 4-25 shows the SmartGen settings. Notice that the overall delays are calculated automatically, allowing the user to adjust the delay elements appropriately to obtain the desired delays.

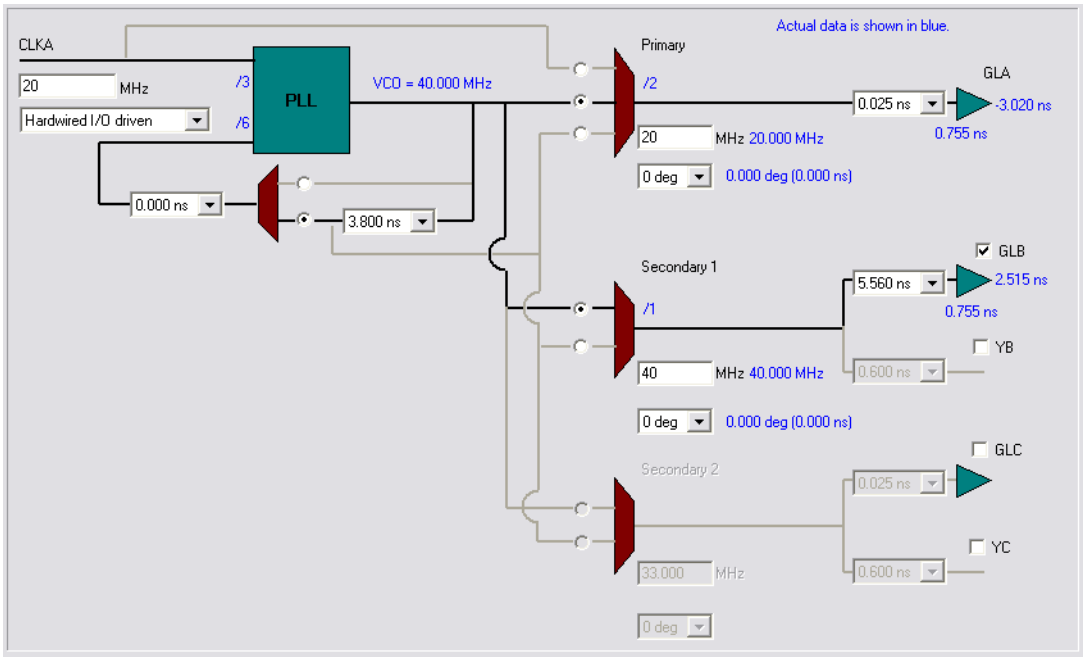


***Figure 4-25* • SmartGen Settings**

After confirming the correct settings, generate a structural netlist of the PLL and verify PLL core settings by checking the log file:

```
Name                          : test_pll_delays
Family                        : ProASIC3E
Output Format                 : VHDL
Type                          : Static PLL
Input Freq(MHz)               : 20.000
CLKA Source                   : Hardwired I/O
Feedback Delay Value Index    : 21
Feedback Mux Select           : 2
XDLY Mux Select               : No
Primary Freq(MHz)             : 20.000
Primary PhaseShift            : 0
Primary Delay Value Index     : 1
Primary Mux Select            : 4
Secondary1 Freq(MHz)          : 40.000
Use GLB                       : YES
Use YB                        : NO
```

```
…
…
…
Primary Clock frequency 20.000
Primary Clock Phase Shift 0.000
Primary Clock Output Delay from CLKA -3.020

Secondary1 Clock frequency 40.000
Secondary1 Clock Phase Shift 0.000
Secondary1 Clock Global Output Delay from CLKA 2.515
```

Next, perform simulation in Model*Sim* to verify the correct delays. Figure 4-26 shows the simulation results. The delay values match those reported in the SmartGen PLL wizard.

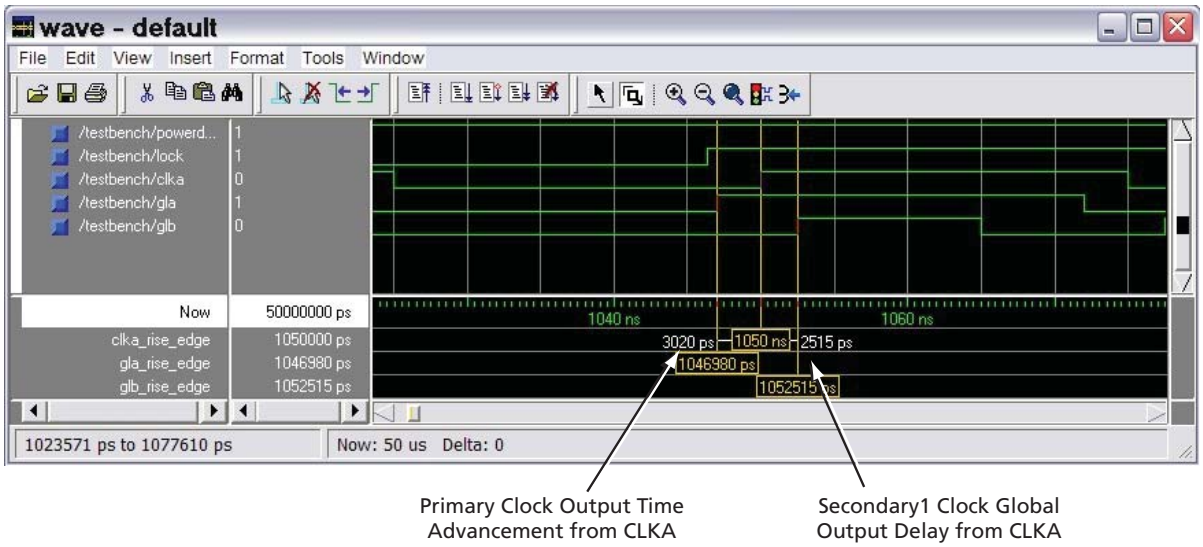
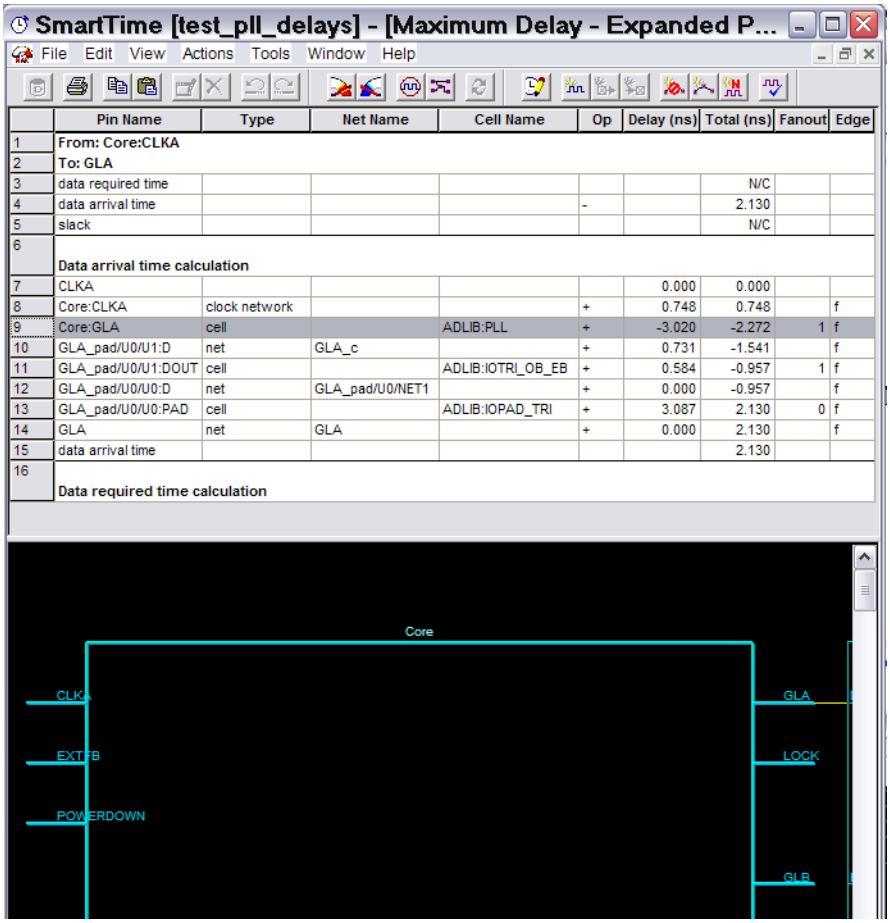


Figure 4-26 **• Model*Sim* Simulation Results**

The timing can also be analyzed using SmartTime in Designer. The user should import the synthesized netlist to Designer, perform Compile and Layout, and then invoke SmartTime. Go to **Tools** > **Options** and change the maximum delay operating conditions to **Typical Case**. Then expand the Clock-to-Out paths of GLA and GLB and the individual components of the path delays are shown. The path of GLA is shown in Figure 4-27 on page 4-36 displaying the same delay value.



	Pin Name	Type	Net Name	Cell Name	Op	Delay (ns)	Total (ns)	Fanout	Edge
1	From: Core:CLKA								
2	To: GLA								
3	data required time						N/C		
4	data arrival time				-		2.130		
5	slack						N/C		
6	Data arrival time calculation								
7	CLKA					0.000	0.000		
8	Core:CLKA	clock network			+	0.748	0.748		f
9	Core:GLA	cell		ADLIB:PLL	+	-3.020	-2.272	1	f
10	GLA_pad/U0/U1:D	net	GLA_c		+	0.731	-1.541		f
11	GLA_pad/U0/U1:DOUT	cell		ADLIB:IOTRI_OB_EB	+	0.584	-0.957	1	f
12	GLA_pad/U0/U0:D	net	GLA_pad/U0/NET1		+	0.000	-0.957		f
13	GLA_pad/U0/U0:PAD	cell		ADLIB:IOPAD_TRI	+	3.087	2.130	0	f
14	GLA	net	GLA		+	0.000	2.130		f
15	data arrival time						2.130		
16	Data required time calculation								

Figure 4-27 **• Static Timing Analysis Using SmartTime**

Place-and-Route Stage Considerations

Several considerations must be noted to properly place the CCC macros for layout.

For CCCs with clock inputs configured with the Hardwired I/O–Driven option:

- PLL macros must have the clock input pad coming from one of the GmA* locations.
- CLKDLY macros must have the clock input pad coming from one of the Global I/Os.

If a PLL with a Hardwired I/O input is used at a CCC location and a Hardwired I/O–Driven CLKDLY macro is used at the same CCC location, the clock input of the CLKDLY macro must be chosen from one of the GmB* or GmC* pin locations. If the PLL is not used or is an External I/O–Driven or Core Logic–Driven PLL, the clock input of the CLKDLY macro can be sourced from the GmA*, GmB*, or GmC* pin locations.

For CCCs with clock inputs configured with the External I/O–Driven option, the clock input pad can be assigned to any regular I/O location (IO******** pins). Note that since global I/O pins can also be used as regular I/Os, regardless of CCC function (CLKDLY or PLL), clock inputs can also be placed in any of these I/O locations.

By default, the Designer layout engine will place global nets in the design at one of the six chip globals. When the number of globals in the design is greater than six, the Designer layout engine will automatically assign additional globals to the quadrant global networks of the low-power flash devices. If the user wishes to decide which global signals should be assigned to chip globals (six available) and which to the quadrant globals (three per quadrant for a total of 12 available), the assignment can be achieved with PinEditor, ChipPlanner, or by importing a placement

constraint file. Layout will fail if the global assignments are not allocated properly. See the "Physical Constraints for Quadrant Clocks" section for information on assigning global signals to the quadrant clock networks.

Promoted global signals will be instantiated with CLKINT macros to drive these signals onto the global network. This is automatically done by Designer when the Auto-Promotion option is selected. If the user wishes to assign the signals to the quadrant globals instead of the default chip globals, this can done by using ChipPlanner, by declaring a physical design constraint (PDC), or by importing a PDC file.

Physical Constraints for Quadrant Clocks

If it is necessary to promote global clocks (CLKBUF, CLKINT, PLL, CLKDLY) to quadrant clocks, the user can define PDCs to execute the promotion. PDCs can be created using PDC commands (pre-compile) or the MVN interface (post-compile). The advantage of using the PDC flow over the MVN flow is that the Compile stage is able to automatically promote any regular net to a global net before assigning it to a quadrant. There are three options to place a quadrant clock using PDC commands:

- Place a clock core (not hardwired to an I/O) into a quadrant clock location.
- Place a clock core (hardwired to an I/O) into an I/O location (set_io) or an I/O module location (set_location) that drives a quadrant clock location.
- Assign a net driven by a regular net or a clock net to a quadrant clock using the following command:

  ```
  assign_local_clock -net <net name> -type quadrant <quadrant clock region>
  ```

  where

  `<net name>` is the name of the net assigned to the local user clock region.

  `<quadrant clock region>` defines which quadrant the net should be assigned to. Quadrant clock regions are defined as UL (upper left), UR (upper right), LL (lower left), and LR (lower right).

Note: If the net is a regular net, the software inserts a CLKINT buffer on the net.

For example:

```
assign_local_clock -net localReset -type quadrant UR
```

Keep in mind the following when placing quadrant clocks using MultiView Navigator:

Hardwired I/O–Driven CCCs

- Find the associated clock input port under the Ports tab, and place the input port at one of the Gmn* locations using PinEditor or I/O Attribute Editor, as shown in Figure 4-28.

Figure 4-28 • **Port Assignment for a CCC with Hardwired I/O Clock Input**

- Use quadrant global region assignments by finding the clock net associated with the CCC macro under the Nets tab and creating a quadrant global region for the net, as shown in Figure 4-29.

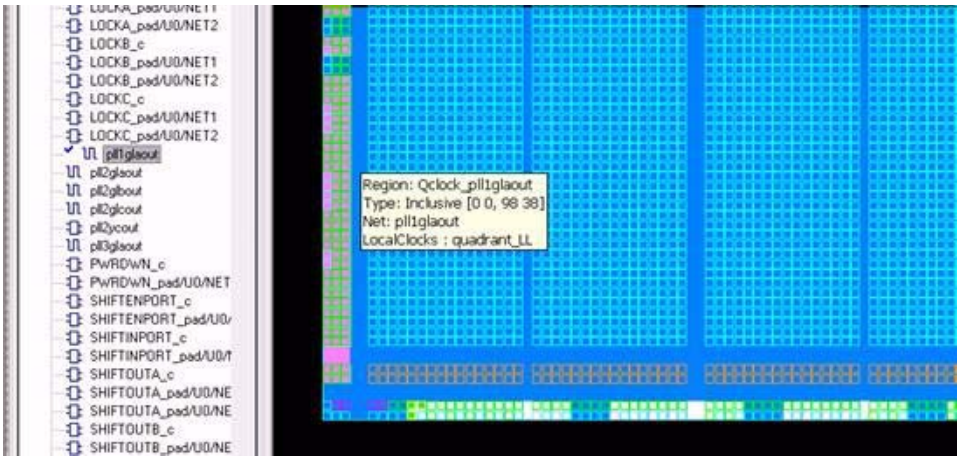


***Figure 4-29* • Quadrant Clock Assignment for a Global Net**

External I/O–Driven CCCs

The above-mentioned recommendation for proper layout techniques will ensure the correct assignment. It is possible that, especially with External I/O–Driven CCC macros, placement of the CCC macro in a desired location may not be achieved. For example, assigning an input port of an External I/O–Driven CCC near a particular CCC location does not guarantee global assignments to the desired location. This is because the clock inputs of External I/O–Driven CCCs can be assigned to any I/O location; therefore, it is possible that the CCC connected to the clock input will be routed to a location other than the one closest to the I/O location, depending on resource availability and placement constraints.

Clock Placer

The clock placer is a placement engine for low-power flash devices that places global signals on the chip global and quadrant global networks. Based on the clock assignment constraints for the chip global and quadrant global clocks, it will try to satisfy all constraints, as well as creating quadrant clock regions when necessary. If the clock placer fails to create the quadrant clock regions for the global signals, it will report an error and stop Layout.

The user must ensure that the constraints set to promote clock signals to quadrant global networks are valid.

Cascading CCCs

The CCCs in low-power flash devices can be cascaded. Cascading CCCs can help achieve more accurate PLL output frequency results than those achievable with a single CCC. In addition, this technique is useful when the user application requires the output clock of the PLL to be a multiple of the reference clock by an integer greater than the maximum feedback divider value of the PLL (divide by 128) to achieve the desired frequency.

For example, the user application may require a 280 MHz output clock using a 2 MHz input reference clock, as shown in Figure 4-30 on page 4-39.

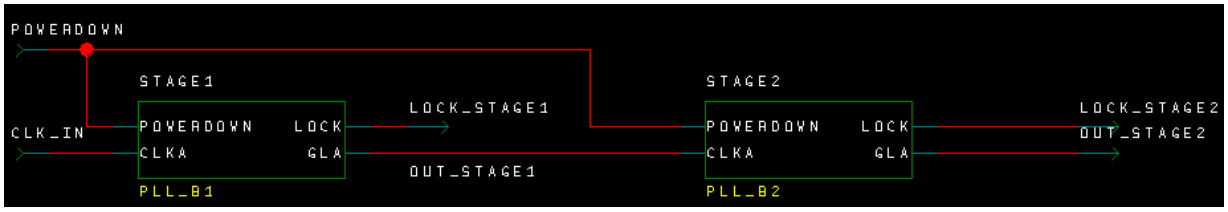


***Figure 4-30* • Cascade PLL Configuration**

Using internal feedback, we know from EQ 4-1 on page 4-19 that the maximum achievable output frequency from the primary output is

$$f_{GLA} = f_{CLKA} \times m \ / (n \times u) = 2 \text{ MHz} \times 128 / (1 \times 1) = 256 \text{ MHz}$$

EQ 4-5

Figure 4-31 shows the settings of the initial PLL. When configuring the initial PLL, specify the input to be either Hardwired I/O–Driven or External I/O–Driven. This generates a netlist with the initial PLL routed from an I/O. Do not specify the input to be Core Logic–Driven, as this prohibits the connection from the I/O pin to the input of the PLL.

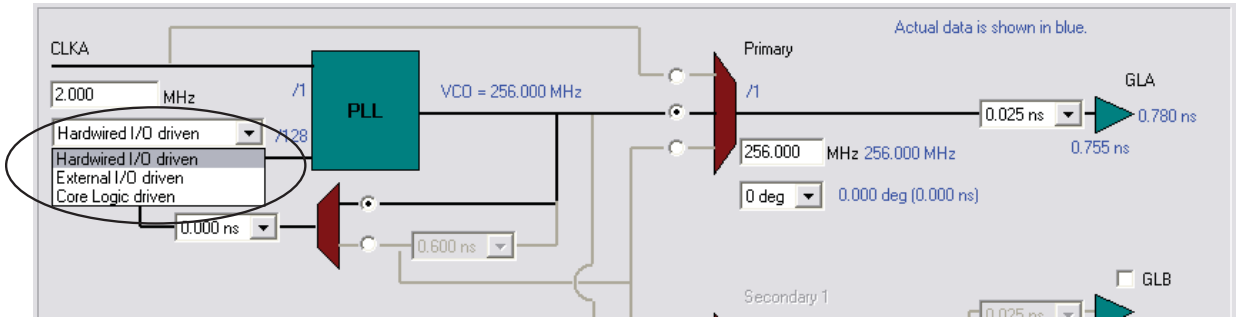


***Figure 4-31* • First-Stage PLL Showing Input of 2 MHz and Output of 256 MHz**

A second PLL can be connected serially to achieve the required frequency. EQ 4-1 on page 4-19 to EQ 4-3 on page 4-19 are extended as follows:

$$f_{GLA2} = f_{GLA} \times m_2 / (n_2 \times u_2) = f_{CLKA1} \times m_1 \times m_2 / (n_1 \times u_1 \times n_2 \times u_2) \text{ – Primary PLL Output Clock}$$

EQ 4-6

$$f_{GLB2} = f_{YB2} = f_{CLKA1} \times m_1 \times m_2 / (n_1 \times n_2 \times v_1 \times v_2) \text{ – Secondary 1 PLL Output Clock(s)}$$

EQ 4-7

$$f_{GLC2} = f_{YC2} = f_{CLKA1} \times m_1 \times m_2 / (n_1 \times n_2 \times w_1 \times w_2) \text{ – Secondary 2 PLL Output Clock(s)}$$

EQ 4-8

In the example, the final output frequency (f_{output}) from the primary output of the second PLL will be as follows (EQ 4-9):

$$f_{output} = f_{GLA2} = f_{GLA} \times m_2 / (n_2 \times u_2) = 256 \text{ MHz} \times 70 / (64 \times 1) = 280 \text{ MHz}$$

EQ 4-9

Figure 4-32 on page 4-40 shows the settings of the second PLL. When configuring the second PLL (or any subsequent-stage PLLs), specify the input to be Core Logic–Driven. This generates a netlist with the second PLL routed internally from the core. Do not specify the input to be Hardwired I/O–Driven or External I/O–Driven, as these options prohibit the connection from the output of the first PLL to the input of the second PLL.

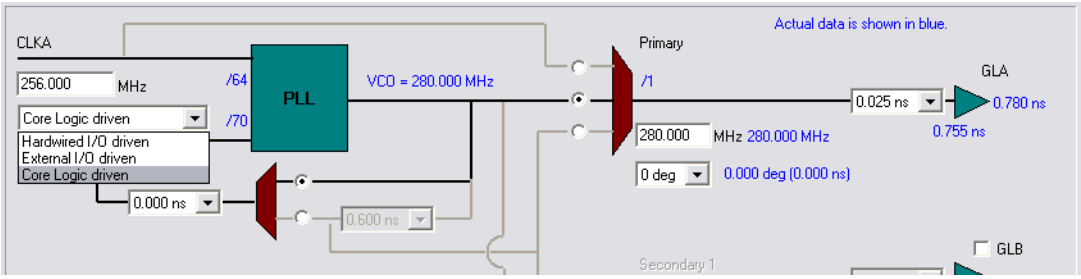


Figure 4-32 • **Second-Stage PLL Showing Input of 256 MHz from First Stage and Final Output of 280 MHz**

Figure 4-33 shows the simulation results, where the first PLL's output period is 3.9 ns (~256 MHz), and the stage 2 (final) output period is 3.56 ns (~280 MHz).

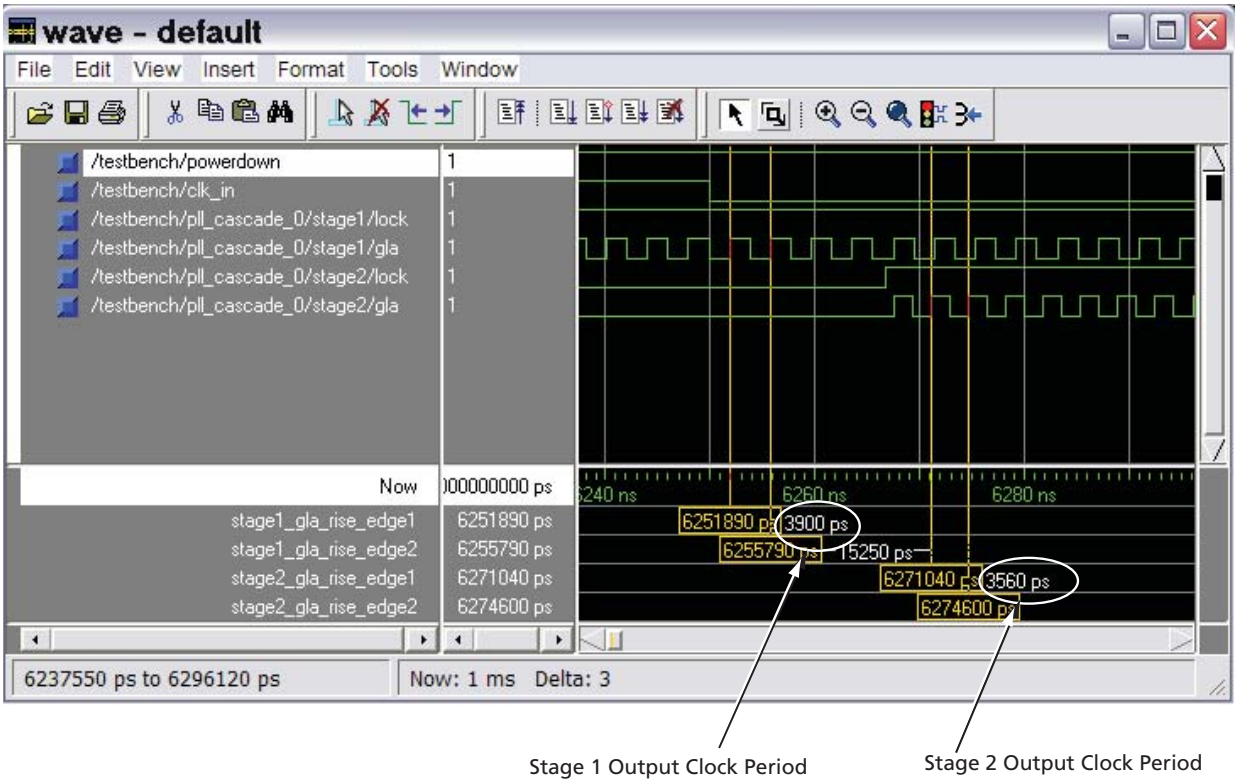


Figure 4-33 • **Model*Sim* Simulation Results**

Recommended Board-Level Considerations

The power to the PLL core is supplied by $V_{CCPLA/B/C/D/E/F}$ (V_{CCPLx}), and the associated ground connections are supplied by $V_{COMPLA/B/C/D/E/F}$ (V_{COMPLx}). When the PLLs are not used, the Actel Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused V_{CCPLx} and V_{COMPLx} pins to ground. Optionally, the PLL can be turned on/off during normal device operation via the POWERDOWN port (see Table 4-3 on page 4-7).

PLL Power Supply Decoupling Scheme

The PLL core is designed to tolerate noise levels on the PLL power supply as specified in the datasheets. When operated within the noise limits, the PLL will meet the output peak-to-peak jitter specifications specified in the datasheets. User applications should always ensure the PLL power supply is powered from a noise-free or low-noise power source.

However, in situations where the PLL power supply noise level is higher than the tolerable limits, various decoupling schemes can be designed to suppress noise to the PLL power supply. An example is provided in Figure 4-34. The V_{CCPLx} and V_{COMPLx} pins correspond to the PLL analog power supply and ground.

Actel strongly recommends that two ceramic capacitors (10 nF in parallel with 100 nF) be placed close to the power pins (less than 1 inch away). A third generic 10 µF electrolytic capacitor is recommended for low-frequency noise and should be placed farther away due to its large physical size. Actel recommends that a 6.8 µH inductor be placed between the supply source and the capacitors to filter out any low-/medium- and high-frequency noise. In addition, the PCB layers should be controlled so the V_{CCPLx} and V_{COMPLx} planes have the minimum separation possible, thus generating a good-quality RF capacitor.

For more recommendations, refer to the *Board-Level Considerations* application note.

Recommended 100 nF capacitor:

- Producer BC Components, type X7R, 100 nF, 16 V
- BC Components part number: 0603B104K160BT
- Digi-Key part number: BC1254CT-ND
- Digi-Key part number: BC1254TR-ND

Recommended 10 nF capacitor:

- Surface-mount ceramic capacitor
- Producer BC Components, type X7R, 10 nF, 50 V
- BC Components part number: 0603B103K500BT
- Digi-Key part number: BC1252CT-ND
- Digi-Key part number: BC1252TR-ND

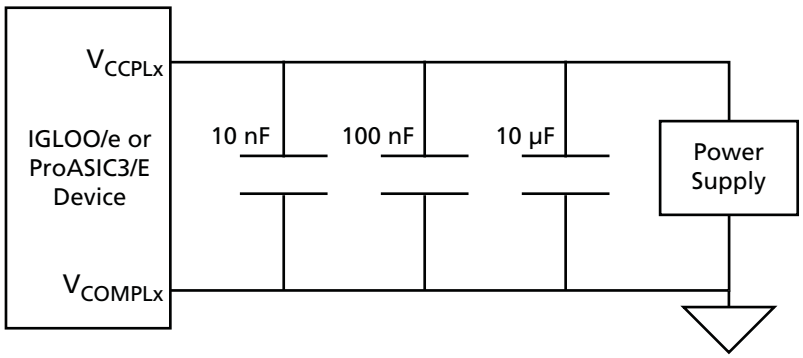


Figure 4-34 **• Decoupling Scheme for One PLL (should be replicated for each PLL used)**

Conclusion

The advanced CCCs of the IGLOO and ProASIC3 families are ideal for applications requiring precise clock management. They integrate easily with the internal low-skew clock networks and provide flexible frequency synthesis, clock de-skewing, and/or time shifting operations.

Related Documents

Application Notes

Board-Level Considerations

http://www.actel.com/documents/BoardLevelCons_AN.pdf

Handbook Documents

UJTAG Applications in Actel's Low-Power Flash Devices

http://www.actel.com/documents/LPD_UJTAG_HBs.pdf

Global Resources in Actel Low-Power Flash Devices

http://www.actel.com/documents/LPD_Global_HBs.pdf

I/O Structures in IGLOO and ProASIC3 Devices

http://www.actel.com/documents/IGLOO_PA3_IO_HBs.pdf

User's Guides

IGLOO, Fusion, and ProASIC3 Macro Library Guide

http://www.actel.com/documents/pa3_libguide_ug.pdf

Part Number and Revision Date

This document contains content extracted from the Device Architecture section of the datasheet, combined with content previously published as an application note describing features and functions of the device. To improve usability for customers, the device architecture information has now been combined with usage information, to reduce duplication and possible inconsistencies in published information. No technical changes were made to the datasheet content unless explicitly listed. Changes to the application note content were made only to be consistent with existing datasheet information.

Part Number 51700094-006-2

Revised June 2008

List of Changes

The following table lists critical changes that were made in the current version of the chapter.

Previous Version	Changes in the Current Version (v1.2)	Page
v1.1 (March 2008)	The following changes were made to the family descriptions in Table 4-1 · Low-Power Flash Families: • ProASIC3L was updated to include 1.5 V. • The number of PLLs for ProASIC3E was changed from five to six.	4-3
v1.0 (January 2008)	Table 4-1 · Low-Power Flash Families and the associated text were updated to include the IGLOO PLUS family. The "IGLOO Terminology" section and "ProASIC3 Terminology" section are new.	4-3
	The "Global Input Selections" section was updated to include 15 k gate devices as supported I/O types for globals, for CCC only.	4-9
	Table 4-5 · Number of CCCs by Device Size and Package was revised to include ProASIC3L, IGLOO PLUS, A3P015, AGL015, AGLP030, AGLP060, and AGLP125.	4-13
	The "IGLOO and ProASIC3 CCC Locations" section was revised to include 15 k gate devices in the exception statements, as they do not contain PLLs.	4-14
51900133-0/5.06	Information about unlocking the PLL was removed from the "Dynamic PLL Configuration" section.	4-19
	In the "Dynamic PLL Configuration" section, information was added about running Layout and determining the exact setting of the ports.	4-29
	In Table 4-7 · Configuration Bit Descriptions for the CCC Blocks, the following bits were updated to delete "transport to the user" and reference the footnote at the bottom of the table: 79 to 71.	4-22

Embedded Memories

Actel®
POWER MATTERS

5 – FlashROM in Actel's Low-Power Flash Devices

Introduction

The IGLOO,® ProASIC®3, and Fusion families of low-power flash-based FPGAs have a dedicated nonvolatile FlashROM memory of 1,024 bits, which provides a unique feature in the FPGA market. The FlashROM can be read, modified, and written using the JTAG (or UJTAG) interface. It can be read but not modified from the FPGA core. Only low-power flash FPGAs contain on-chip user nonvolatile memory (NVM).

Architecture of User Nonvolatile FlashROM

Low-power flash devices have 1 kbit of user-accessible nonvolatile flash memory on-chip that can be read from the FPGA core fabric. The FlashROM is arranged in eight banks of 128 bits (16 bytes) during programming. The 128 bits in each bank are addressable as 16 bytes during the read-back of the FlashROM from the FPGA core. Figure 5-1 shows the FlashROM logical structure.

The FlashROM can only be programmed via the IEEE 1532 JTAG port. It cannot be programmed directly from the FPGA core. When programming, each of the eight 128-bit banks can be selectively reprogrammed. The FlashROM can only be reprogrammed on a bank boundary. Programming involves an automatic, on-chip bank erase prior to reprogramming the bank. The FlashROM supports synchronous read. The address is latched on the rising edge of the clock, and the new output data is stable after the falling edge of the same clock cycle. For more information, refer to the timing diagrams in the appropriate family datasheet DC and Switching Characteristics chapter. The FlashROM can be read on byte boundaries. The upper three bits of the FlashROM address from the FPGA core define the bank being accessed. The lower four bits of the FlashROM address from the FPGA core define which of the 16 bytes in the bank is being accessed.

		Byte Number in Bank								4 LSB of ADDR (READ)							
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bank Number 3 MSB of ADDR (READ)	7																
	6																
	5																
	4																
	3																
	2																
	1																
	0																

Figure 5-1 • **FlashROM Architecture**

FlashROM Support in Low-Power Devices

The low-power flash families listed in Table 5-1 support the FlashROM feature and the functions described in this document.

Table 5-1 • **Low-Power Flash Families**

Family[1]	Description	Timing Numbers[2]
IGLOO	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*IGLOO DC and Switching Characteristics*
IGLOO PLUS	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology and enhanced I/O capabilities.	*IGLOO PLUS DC and Switching Characteristics*
IGLOOe	IGLOO devices enhanced with higher density, five additional PLLs, and additional I/O standards	*IGLOOe DC and Switching Characteristics*
ProASIC3L	Low-power, high-performance 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*ProASIC3L DC and Switching Characteristics*
ProASIC3	Low-power, high-performance 1.5 V FPGAs	*ProASIC3 DC and Switching Characteristics*
ProASIC3E	ProASIC3 enhanced with higher density, six additional PLLs, and additional I/O standards	*ProASIC3E DC and Switching Characteristics*
ProASIC3 Automotive	Low-power, high-performance FPGAs qualified for automotive applications	*Automotive ProASIC3 DC and Switching Characteristics*
Fusion	Low-power mixed-signal Programmable System Chip (PSC)	*Fusion DC and Power Characteristics*

Notes:

1. *The family names are linked to the appropriate product brief.*
2. *The timing number links go to the relevant timing numbers in the datasheet.*

Actel's low-power flash devices (listed in Table 5-1) provide a selection of low-power, secure, live-at-power-up, single-chip solutions. The nonvolatile flash-based devices do not require a boot PROM and incorporate FlashLock® technology, which provides a unique combination of reprogrammability and design security without external overhead. Only low-power flash FPGAs can offer these advantages.

Actel IGLOO PLUS FPGAs are the industry-leading 1.2 V ultra-low-power programmable logic devices (PLDs) and consume 90% less static power and over 50% less dynamic power than PLD alternatives, while ProASIC3L devices offer a balance of low power and higher performance.

Flash*Freeze technology used in IGLOO, IGLOO PLUS, and ProASIC3L devices enables easy entry to and exit from the ultra-low power mode, which consumes as little as 5 µW, while retaining SRAM and register data. IGLOO PLUS also offers the ability to hold I/O state in Flash*Freeze mode. Flash*Freeze technology simplifies power management through I/O and clock management without the need to turn off voltages, I/Os, or clocks at the system level. Entering and exiting Flash*Freeze mode takes less than 1 µs.

The Actel Fusion® family, based on the highly successful ProASIC3 flash FPGA architecture, has been designed as a high-performance, mixed-signal Programmable System Chip. Fusion supports many peripherals, including embedded flash memory, analog-to-digital converter (ADC), high-drive outputs, RC and crystal oscillators, and real-time counter (RTC). The total available on-chip memory, including the flash array blocks, is greater than that found in SRAM FPGAs.

IGLOO Terminology

In documentation, the term IGLOO families or IGLOO devices refers to all IGLOO families as listed in Table 5-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

ProASIC3 Terminology

In documentation, the term ProASIC3 families or ProASIC3 devices refers to all ProASIC3 families as listed in Table 5-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

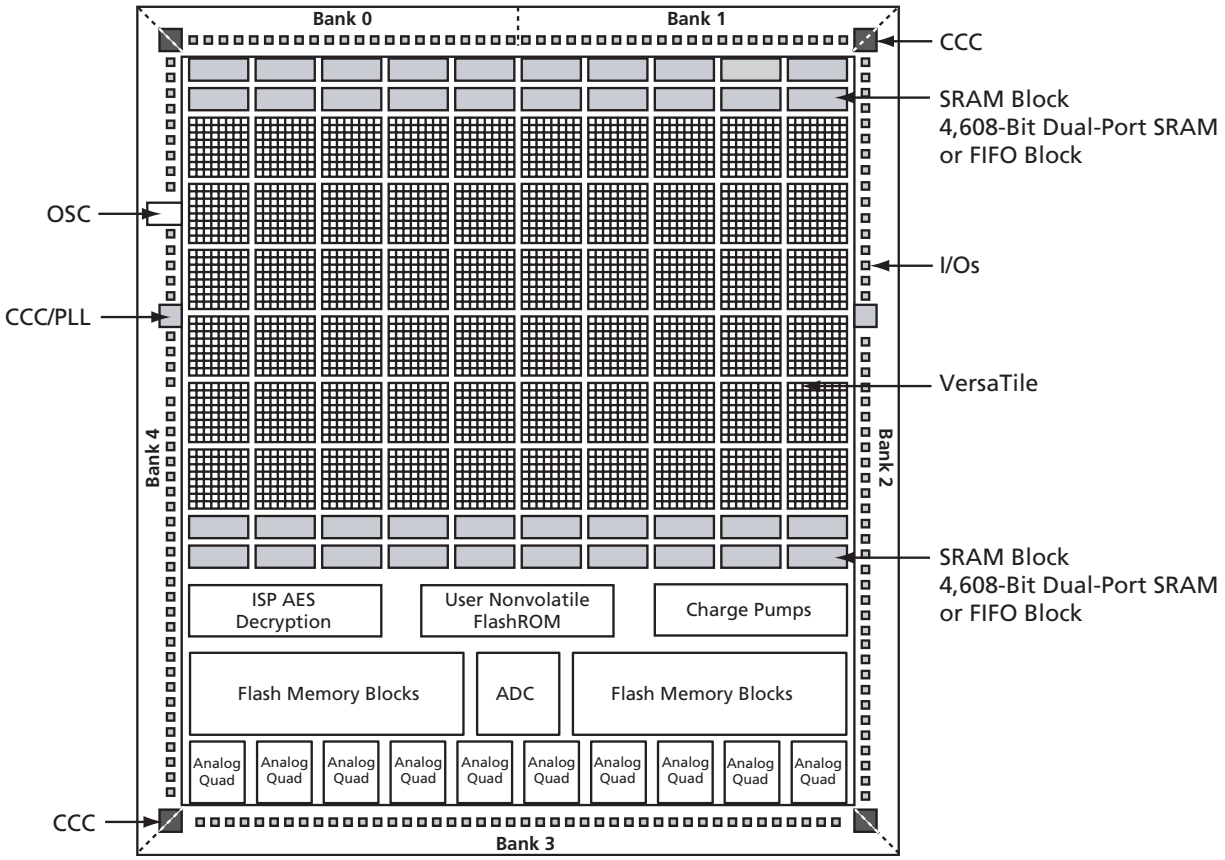


Figure 5-2 • **Fusion Device Architecture Overview (AFS600)**

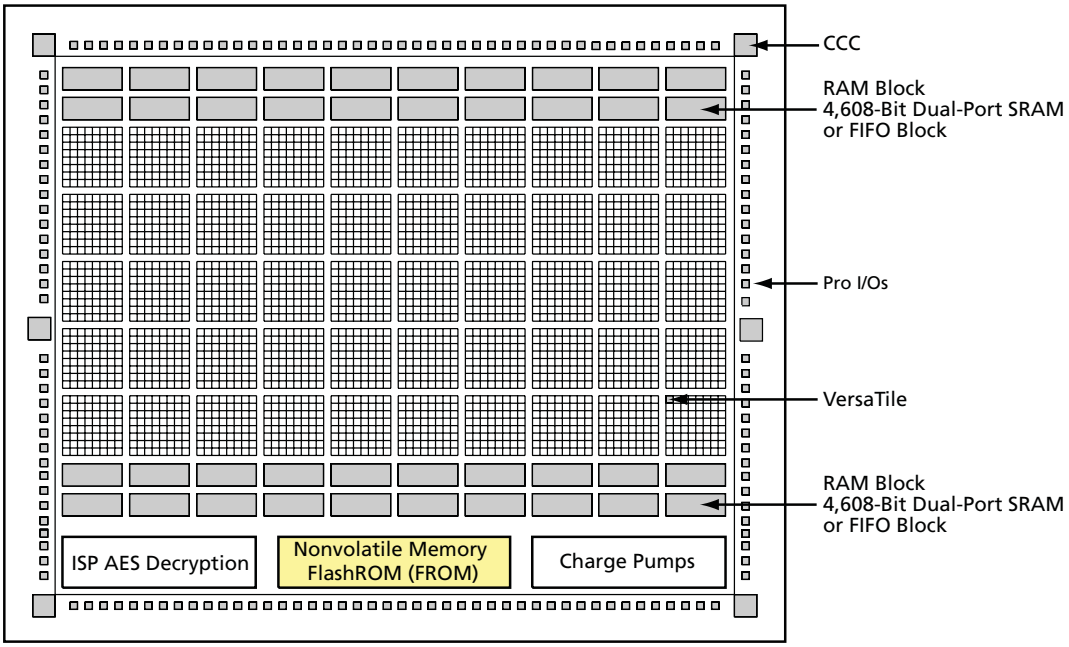


Figure 5-3 • **ProASIC3 and IGLOO Device Architecture**

FlashROM Applications

The SmartGen core generator is used to configure FlashROM content. You can configure each page independently. SmartGen enables you to create and modify regions within a page; these regions can be 1 to 16 bytes long (Figure 5-4).

		Byte Number in Page															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Page Number	7																
	6																
	5																
	4																
	3																
	2																
	1																
	0																

Figure 5-4 • **FlashROM Configuration**

The FlashROM content can be changed independently of the FPGA core content. It can be easily accessed and programmed via JTAG, depending on the security settings of the device. The SmartGen core generator enables each region to be independently updated (described in the "Programming and Accessing FlashROM" section on page 5-6). This enables you to change the FlashROM content on a per-part basis while keeping some regions "constant" for all parts. These features allow the FlashROM to be used in diverse system applications. Consider the following possible uses of FlashROM:

- Internet protocol (IP) addressing (wireless or fixed)
- System calibration settings
- Restoring configuration after unpredictable system power-down
- Device serialization and/or inventory control
- Subscription-based business models (e.g., set-top boxes)
- Secure key storage
- Asset management tracking
- Date stamping
- Version management

FlashROM Security

Low-power flash devices have an on-chip Advanced Encryption Standard (AES) decryption core, combined with an enhanced version of the Actel flash-based lock technology (FlashLock®). Together, they provide unmatched levels of security in a programmable logic device. This security applies to both the FPGA core and FlashROM content. These devices use the 128-bit AES (Rijndael) algorithm to encrypt programming files for secure transmission to the on-chip AES decryption core. The same algorithm is then used to decrypt the programming file. This key size provides approximately 3.4×10^{38} possible 128-bit keys. A computing system that could find a DES key in a second would take approximately 149 trillion years to crack a 128-bit AES key. The 128-bit FlashLock feature in low-power flash devices works via a FlashLock security Pass Key mechanism, where the user locks or unlocks the device with a user-defined key. Refer to *Security in Low-Power Flash Devices*.

If the device is locked with certain security settings, functions such as device read, write, and erase are disabled. This unique feature helps to protect against invasive and noninvasive attacks. Without the correct Pass Key, access to the FPGA is denied. To gain access to the FPGA, the device first must be unlocked using the correct Pass Key. During programming of the FlashROM or the FPGA core, you can generate the security header programming file, which is used to program the AES key and/or FlashLock Pass Key. The security header programming file can also be generated independently of the FlashROM and FPGA core content. The FlashLock Pass Key is not stored in the FlashROM.

Low-power flash devices with AES-based security allow for secure remote field updates over public networks such as the Internet, and ensure that valuable intellectual property (IP) remains out of the hands of IP thieves. Figure 5-5 shows this flow diagram.

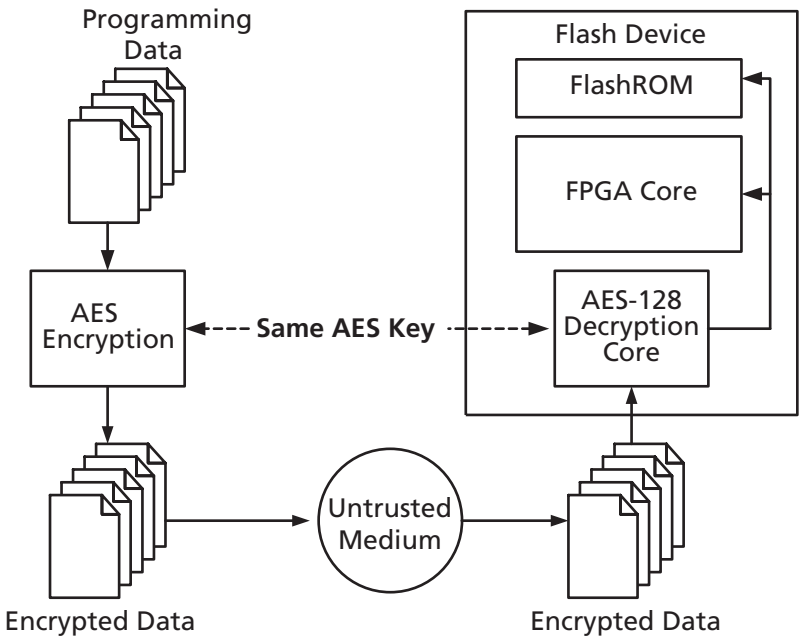


Figure 5-5 • **Programming FlashROM Using AES**

Programming and Accessing FlashROM

The FlashROM content can only be programmed via JTAG, but it can be read back selectively through the JTAG programming interface, the UJTAG interface, or via direct FPGA core addressing. The pages of the FlashROM can be made secure to prevent read-back via JTAG. In that case, read-back on these secured pages is only possible by the FPGA core fabric or via UJTAG.

A 7-bit address from the FPGA core defines which of the eight pages (three MSBs) is being read, and which of the 16 bytes within the selected page (four LSBs) are being read. The FlashROM content can be read on a random basis; the access time is 10 ns for a device supporting commercial specifications. The FPGA core will be powered down during writing of the FlashROM content. FPGA power-down during FlashROM programming is managed on-chip, and FPGA core functionality is not available during programming of the FlashROM. Table 5-2 summarizes various FlashROM access scenarios.

Table 5-2 • **FlashROM Read/Write Capabilities by Access Mode**

Access Mode	FlashROM Read	FlashROM Write
JTAG	Yes	Yes
UJTAG	Yes	No
FPGA core	Yes	No

Figure 5-6 shows the accessing of the FlashROM using the UJTAG macro. This is similar to FPGA core access, where the 7-bit address defines which of the eight pages (three MSBs) is being read and which of the 16 bytes within the selected page (four LSBs) are being read. Refer to *UJTAG Applications in Actel's Low-Power Flash Devices* for details on using the UJTAG macro to read the FlashROM.

Figure 5-7 on page 5-7 and Figure 5-8 on page 5-7 show the FlashROM access from the JTAG port. The FlashROM content can be read on a random basis. The three-bit address defines which page is being read or updated.

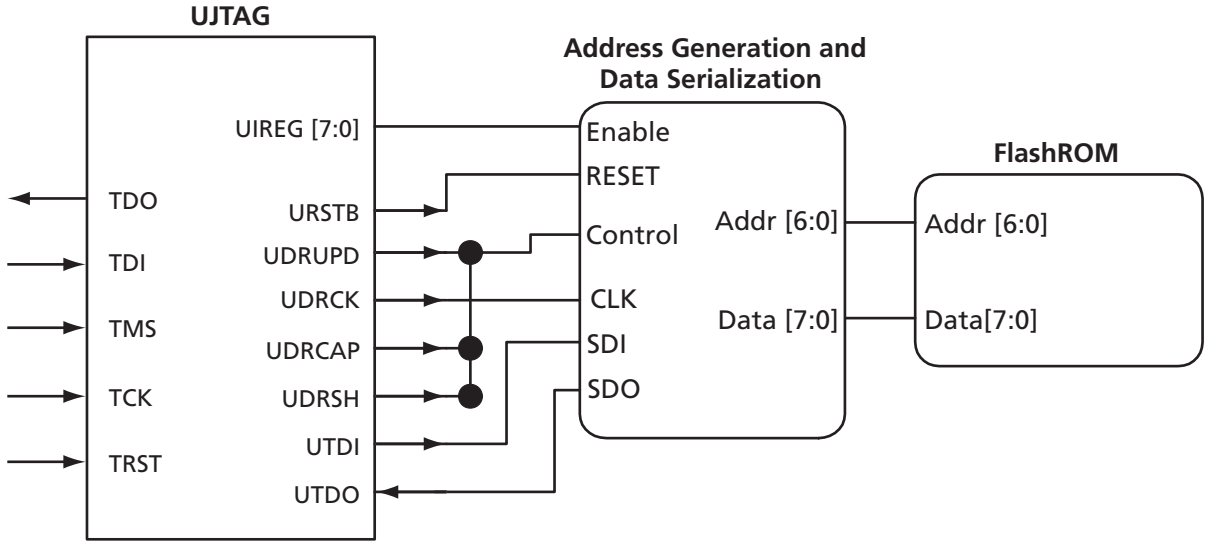


Figure 5-6 • **Block Diagram of Using UJTAG to Read FlashROM Contents**

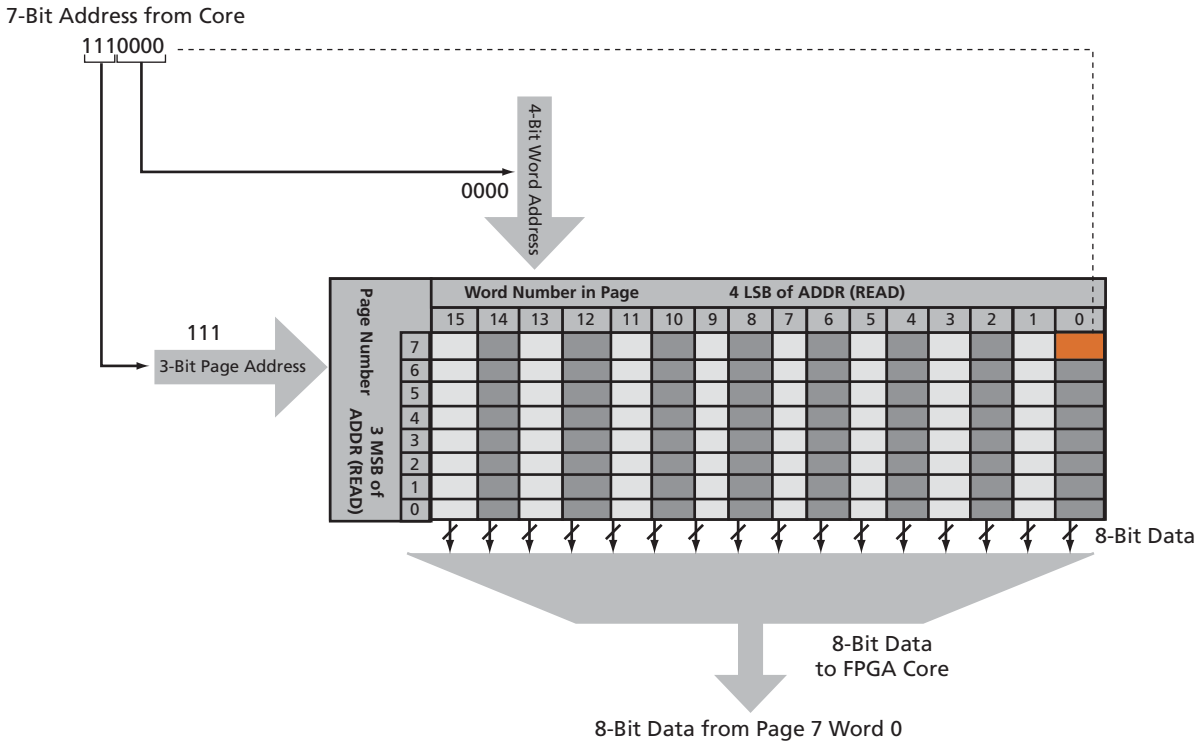


Figure 5-7 • **Accessing FlashROM Using FPGA Core**

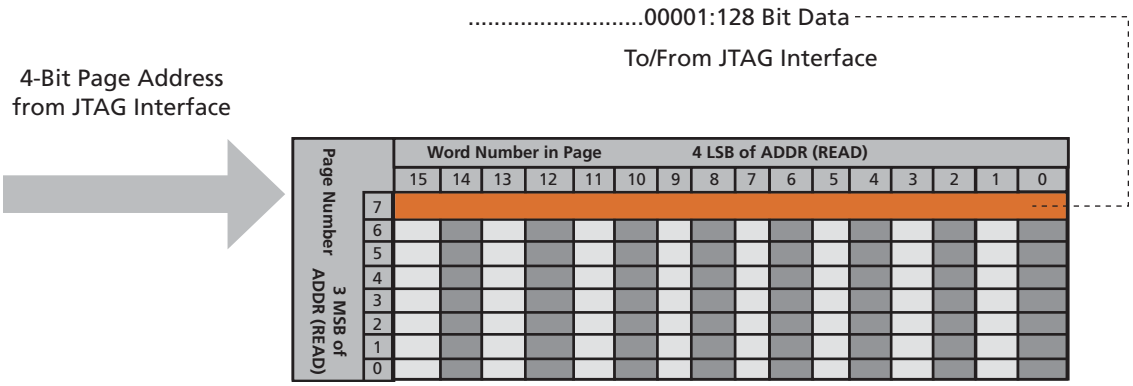


Figure 5-8 • **Accessing FlashROM Using JTAG Port**

FlashROM Design Flow

The Actel Libero® Integrated Design Environment (IDE) software has extensive FlashROM support, including FlashROM generation, instantiation, simulation, and programming. Figure 5-9 shows the user flow diagram. In the design flow, there are three main steps:

1. FlashROM generation and instantiation in the design
2. Simulation of FlashROM design
3. Programming file generation for FlashROM design

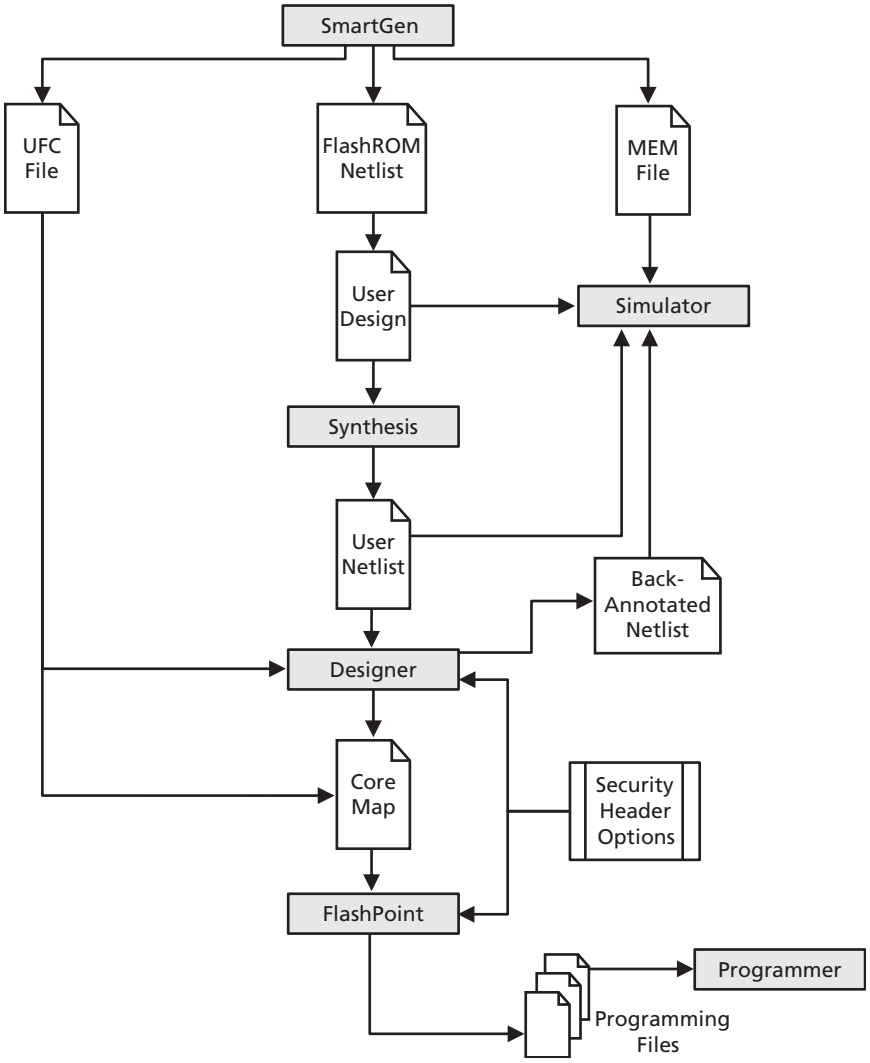


Figure 5-9 • **FlashROM Design Flow**

FlashROM Generation and Instantiation in the Design

The SmartGen core generator, available in Libero IDE and Designer, is the only tool that can be used to generate the FlashROM content. SmartGen has several user-friendly features to help generate the FlashROM contents. Instead of selecting each byte and assigning values, you can create a region within a page, modify the region, and assign properties to that region. The FlashROM user interface, shown in Figure 5-10 on page 5-9, includes the configuration grid, existing regions list, and properties field. The properties field specifies the region-specific information and defines the data used for that region. You can assign values to the following properties:

1. Static Fixed Data—Enables you to fix the data so it cannot be changed during programming time. This option is useful when you have fixed data stored in this region, which is required for the operation of the design in the FPGA. Key storage is one example.
2. Static Modifiable Data—Select this option when the data in a particular region is expected to be static data (such as a version number, which remains the same for a long duration but could conceivably change in the future). This option enables you to avoid changing the value every time you enter new data.
3. Read from File—This provides the full flexibility of FlashROM usage to the customer. If you have a customized algorithm for generating the FlashROM data, you can specify this setting. You can then generate a text file with data for as many devices as you wish to program, and load that into the FlashPoint programming file generation software to get programming files that include all the data. SmartGen will optionally pass the location of the file where the data is stored if the file is specified in SmartGen. Each text file has only one type of data format (binary, decimal, hex, or ASCII text). The length of each data file must be shorter than or equal to the selected region length. If the data is shorter than the selected region length, the most significant bits will be padded with 0s. For multiple text files for multiple regions, the first lines are for the first device. In SmartGen, **Load Sim. Value From File** allows you to load the first device data in the MEM file for simulation.
4. Auto Increment/Decrement—This scenario is useful when you specify the contents of FlashROM for a large number of devices in a series. You can specify the step value for the serial number and a maximum value for inventory control. During programming file generation, the actual number of devices to be programmed is specified and a start value is fed to the software.

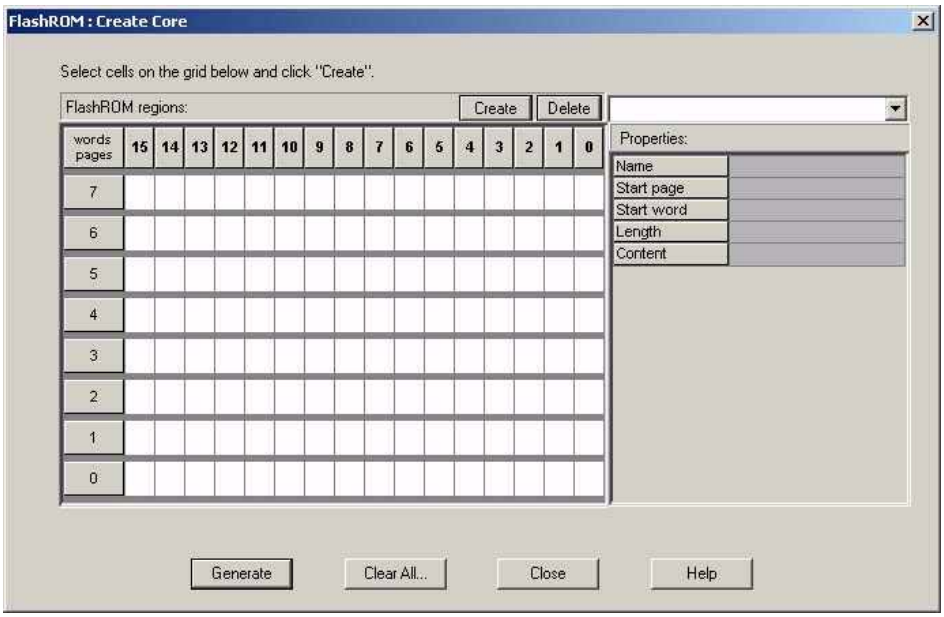


Figure 5-10 • **SmartGen GUI of the FlashROM**

SmartGen allows you to generate the FlashROM netlist in VHDL, Verilog, or EDIF format. After the FlashROM netlist is generated, the core can be instantiated in the main design like other SmartGen cores. Note that the macro library name for FlashROM is UFROM. The following is a sample FlashROM VHDL netlist that can be instantiated in the main design:

```
library ieee;
use ieee.std_logic_1164.all;
library fusion;

entity FROM_a is
  port( ADDR : in std_logic_vector(6 downto 0); DOUT : out std_logic_vector(7 downto 0));
end FROM_a;

architecture DEF_ARCH of  FROM_a is

  component UFROM
    generic (MEMORYFILE:string);
    port(DO0, DO1, DO2, DO3, DO4, DO5, DO6, DO7 : out std_logic;
      ADDR0, ADDR1, ADDR2, ADDR3, ADDR4, ADDR5, ADDR6 : in std_logic := 'U') ;
  end component;

  component GND
    port( Y : out std_logic);
  end component;

signal U_7_PIN2 : std_logic ;

begin

  GND_1_net : GND port map(Y => U_7_PIN2);
  UFROM0 : UFROM
  generic map(MEMORYFILE => "FROM_a.mem")
  port map(DO0 => DOUT(0), DO1 => DOUT(1), DO2 => DOUT(2), DO3 => DOUT(3), DO4 => DOUT(4),
    DO5 => DOUT(5), DO6 => DOUT(6), DO7 => DOUT(7), ADDR0 => ADDR(0), ADDR1 => ADDR(1),
    ADDR2 => ADDR(2), ADDR3 => ADDR(3), ADDR4 => ADDR(4), ADDR5 => ADDR(5),
    ADDR6 => ADDR(6));

end DEF_ARCH;
```

SmartGen generates the following files along with the netlist. These are located in the SmartGen folder for the Libero IDE project.

1. MEM (Memory Initialization) file
2. UFC (User Flash Configuration) file
3. Log file

The MEM file is used for simulation, as explained in the "Simulation of FlashROM Design" section. The UFC file, generated by SmartGen, has the FlashROM configuration for single or multiple devices and is used during STAPL generation. It contains the region properties and simulation values. Note that any changes in the MEM file will not be reflected in the UFC file. Do not modify the UFC to change FlashROM content. Instead, use the SmartGen GUI to modify the FlashROM content. See the "Programming File Generation for FlashROM Design" section on page 5-11 for a description of how the UFC file is used during the programming file generation. The log file has information regarding the file type and file location.

Simulation of FlashROM Design

The MEM file has 128 rows of 8 bits, each representing the contents of the FlashROM used for simulation. For example, the first row represents page 0, byte 0; the next row is page 0, byte 1; and so the pattern continues. Note that the three MSBs of the address define the page number, and the four LSBs define the byte number. So, if you send address 0000100 to FlashROM, this corresponds to the page 0 and byte 4 location, which is the fifth row in the MEM file. SmartGen defaults to 0s for any unspecified location of the FlashROM. Besides using the MEM file generated by SmartGen, you can create a binary file with 128 rows of 8 bits each and use this as a MEM file. Actel recommends that you use different file names if you plan to generate multiple MEM files. During simulation, Libero IDE passes the MEM file used as the generic file in the netlist, along with the design files and testbench. If you want to use different MEM files during simulation, you need to modify the generic file reference in the netlist.

```
……................
UFROM0: UFROM
--generic map(MEMORYFILE => "F:\Appsnotes\FROM\test_designs\testa\smartgen\FROM_a.mem")
--generic map(MEMORYFILE => "F:\Appsnotes\FROM\test_designs\testa\smartgen\FROM_b.mem")
……..................
```

The VITAL and Verilog simulation models accept the generics passed by the netlist, read the MEM file, and perform simulation with the data in the file.

Programming File Generation for FlashROM Design

FlashPoint is the programming software used to generate the programming files for flash devices. Depending on the applications, you can use the FlashPoint software to generate a STAPL file with different FlashROM contents. In each case, optional AES decryption is available. To generate a STAPL file that contains the same FPGA core content and different FlashROM contents, the FlashPoint software needs an Array Map file for the core and UFC file(s) for the FlashROM. This final STAPL file represents the combination of the logic of the FPGA core and FlashROM content.

FlashPoint generates the STAPL files you can use to program the desired FlashROM page and/or FPGA core of the FPGA device contents. FlashPoint supports the encryption of the FlashROM content and/or FPGA Array configuration data. In the case of using the FlashROM for device serialization, a sequence of unique FlashROM contents will be generated. When generating a programming file with multiple unique FlashROM contents, you can specify in FlashPoint whether to include all FlashROM content in a single STAPL file or generate a different STAPL file for each FlashROM (Figure 5-11). The programming software (FlashPro) handles the single STAPL file that contains the FlashROM content from multiple devices. It enables you to program the FlashROM content into a series of devices sequentially (Figure 5-11). See the *FlashPro User's Guide* for information on serial programming.

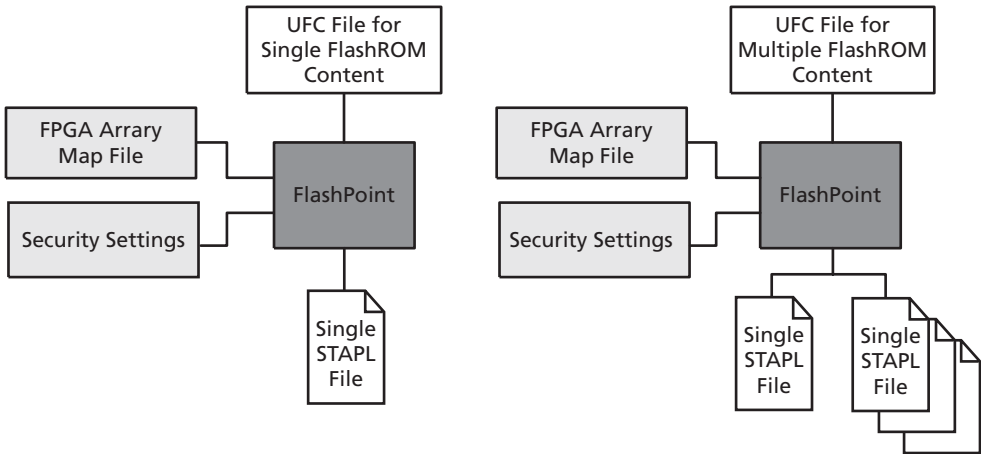


***Figure 5-11* • Single or Multiple Programming File Generation**

Figure 5-12 on page 5-12 shows the programming file generator, which enables different STAPL file generation methods. When you select **Program FlashROM** and choose the UFC file, the FlashROM Settings window appears, as shown in Figure 5-13 on page 5-12. In this window, you can select the FlashROM page you want to program and the data value for the configured regions. This enables you to use a different page for different programming files.

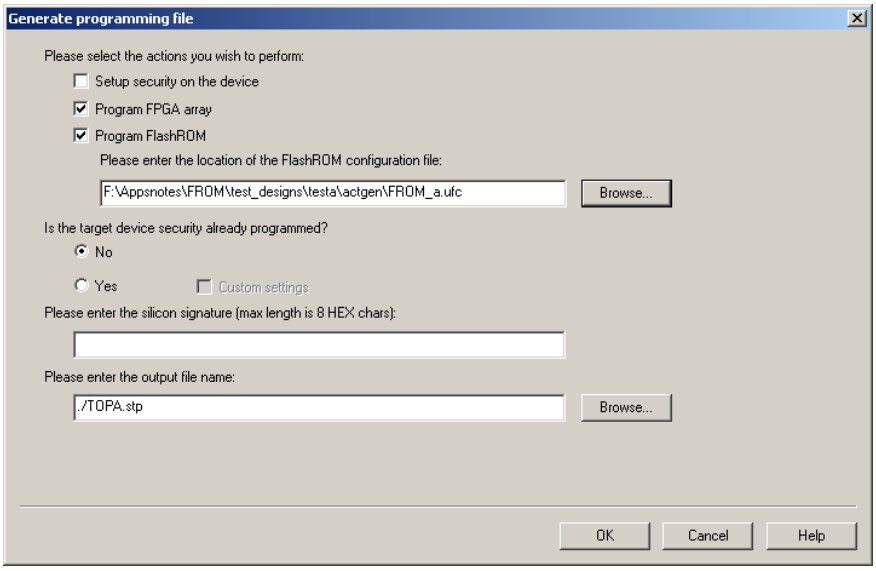


***Figure 5-12* • Programming File Generator**

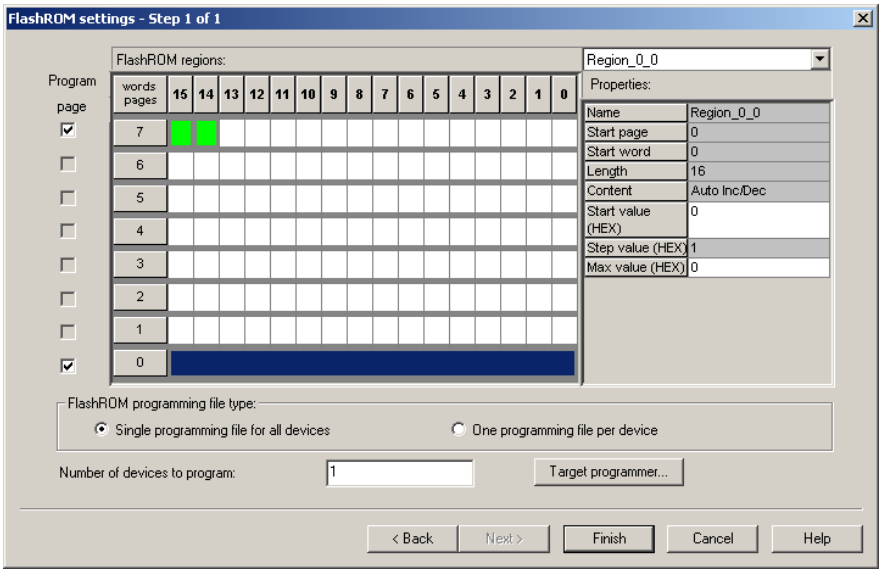


***Figure 5-13* • Setting FlashROM during Programming File Generation**

The programming hardware and software can load the FlashROM with the appropriate STAPL file. Programming software handles the single STAPL file that contains multiple FlashROM contents for multiple devices, and programs the FlashROM in sequential order (e.g., for device serialization).

This feature is supported in the programming software. After programming with the STAPL file, you can run **DEVICE_INFO** to check the FlashROM content.

DEVICE_INFO displays the FlashROM content, serial number, Design Name, and checksum as shown below:

```
EXPORT IDCODE[32] = 123261CF
EXPORT SILSIG[32] = 00000000
User information :
CHECKSUM: 61A0
Design Name:        TOP
Programming Method: STAPL
Algorithm Version: 1
Programmer: UNKNOWN
========================================
FlashROM Information :
EXPORT Region_7_0[128] = FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF
========================================
Security Setting :
Encrypted FlashROM Programming Enabled.
Encrypted FPGA Array Programming Enabled.
========================================
```

The Libero IDE file manager recognizes the UFC and MEM files and displays them in the appropriate view. Libero IDE also recognizes the multiple programming files, if you choose the option to generate multiple files for multiple FlashROM content in Designer. These features enable a user-friendly flow for the FlashROM generation and programming in Libero IDE.

Custom Serialization Using FlashROM

You can use FlashROM for device serialization or inventory control by using the Auto Inc region or Read From File region. FlashPoint will automatically generate the serial number sequence for the Auto Inc region with the **Start Value**, **Max Value**, and **Step Value** provided. If you have a unique serial number generation scheme that you prefer, the Read From File region allows you to import the file with your serial number scheme programmed into the region. See the *FlashPro User's Guide* for custom serialization file format information.

The following steps describe how to perform device serialization or inventory control using FlashROM:

1. Generate FlashROM using SmartGen. From the **Properties** section in the **FlashROM Settings** dialog box, select **Auto Inc** or **Read From File** region. For **Auto Inc** region, specify the desired step value. You will not be able to modify this value in the FlashPoint software.
2. Go through the regular design flow and finish place-and-route.
3. Select **Programming File** in Designer and open **Generate Programming File** (Figure 5-12 on page 5-12).
4. Click **Program FlashROM**, browse to the UFC file, and click **Next**. The FlashROM Settings window appears, as shown in Figure 5-13 on page 5-12.
5. Select the FlashROM page you want to program and the data value for the configured regions. The STAPL file generated will contain only the data that targets the selected FlashROM page.
6. Modify properties for the serialization.
   - For Auto Inc region, specify the **Start** and **Max** values.
   - For Read From File region, select the file name of the custom serialization file.
7. Select the FlashROM programming file type you want to generate from the two options below:
   - Single programming file for all devices: generates one programming file with all FlashROM values.
   - One programming file per device: generates a separate programming file for each FlashROM value.

8. Enter the number of devices you want to program and generate the required programming file.
9. Open the programming software and load the programming file. The programming software, FlashPro3 and Silicon Sculptor II, supports the device serialization feature. If, for some reason, the device fails to program a part during serialization, the software allows you to reuse the serial data or skip the serial data. Refer to the *FlashPro User's Guide* for details.

Conclusion

The IGLOO, Fusion, and ProASIC3 families are the only FPGAs that offer on-chip FlashROM support. This document presents information on the FlashROM architecture, possible applications, programming, access through the JTAG and UJTAG interface, and integration into your design. In addition, the Libero IDE tool set enables easy creation and modification of the FlashROM content.

The nonvolatile FlashROM block in the FPGA can be customized, enabling multiple applications.

Additionally, the security offered by the low-power flash devices keeps both the contents of FlashROM and the FPGA design safe from system over-builders, system cloners, and IP thieves.

Related Documents

Handbook Documents

Security in Low-Power Flash Devices

www.actel.com/documents/LPD_Security_HBs.pdf

UJTAG Applications in Actel's Low-Power Flash Devices

http://www.actel.com/documents/LPD_UJTAG_HBs.pdf

User's Guides

FlashPro User's Guide

http://www.actel.com/documents/FlashPro_UG.pdf

FlashPoint User's Guide

http://www.actel.com/documents/FlashPoint_UG.pdf

Part Number and Revision Date

This document contains content extracted from the Device Architecture section of the datasheet, combined with content previously published as an application note describing features and functions of the device. To improve usability for customers, the device architecture information has now been combined with usage information, to reduce duplication and possible inconsistencies in published information. No technical changes were made to the datasheet content unless explicitly listed. Changes to the application note content were made only to be consistent with existing datasheet information.

Part Number 51700094-007-2

Revised June 2008

List of Changes

The following table lists critical changes that were made in the current version of the chapter.

Previous Version	Changes in Current Version (v1.2)	Page
v1.1 (March 2008)	The following changes were made to the family descriptions in Table 5-1 · Low-Power Flash Families: • ProASIC3L was updated to include 1.5 V. • The number of PLLs for ProASIC3E was changed from five to six.	5-2
v1.0 (January 2008)	The chapter was updated to include the IGLOO PLUS family and information regarding 15 k gate devices. The "IGLOO Terminology" section and "ProASIC3 Terminology" section are new.	N/A

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6 – SRAM and FIFO Memories in Actel's Low-Power Flash Devices

Introduction

As design complexity grows, greater demands are placed upon an FPGA's embedded memory. Actel IGLOO,® Fusion, and ProASIC®3 devices provide the flexibility of true dual-port and two-port SRAM blocks. The embedded memory, along with built-in, dedicated FIFO control logic, can be used to create cascading RAM blocks and FIFOs without using additional logic gates.

IGLOO, IGLOO PLUS, and ProASIC3L FPGAs contain an additional feature that allows the device to be put in a low-power mode called Flash*Freeze. In this mode, the core draws minimal power (on the order of 4 to 127 µW) and still retains values on the embedded SRAM/FIFO and registers. Flash*Freeze technology allows the user to switch to Active mode on demand, thus simplifying power management and the use of SRAM/FIFOs.

Device Architecture

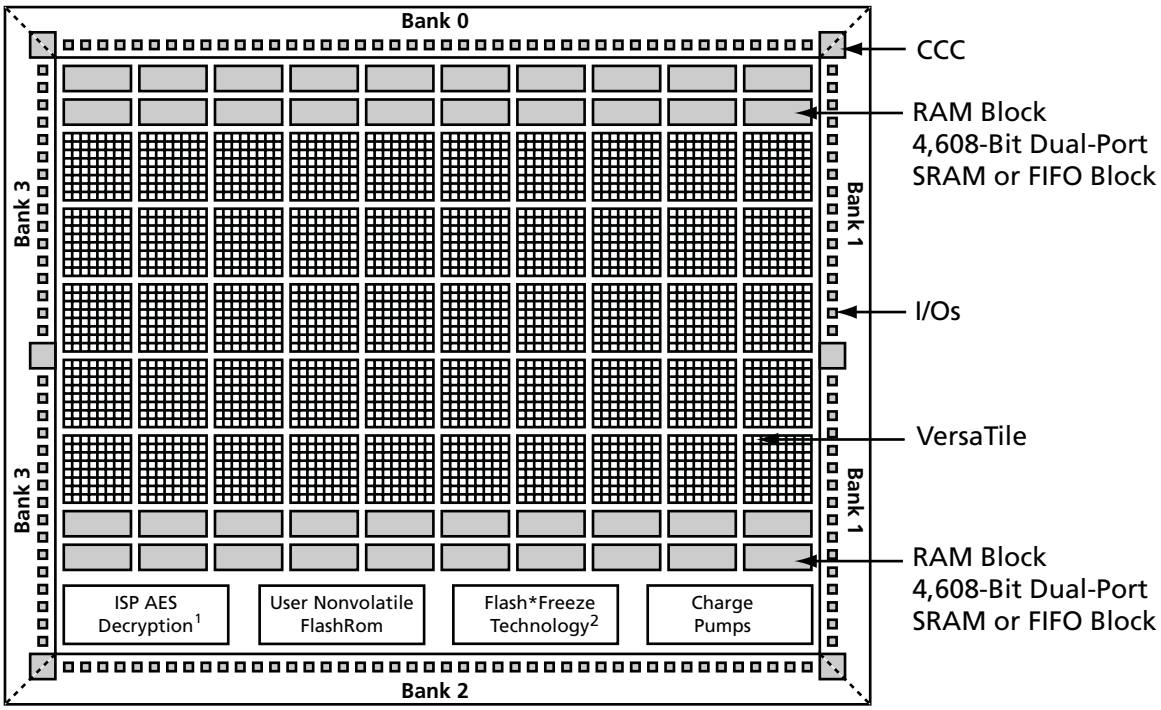
The low-power flash devices feature up to 504 kbits of RAM in 4,608-bit blocks (Figure 6-1 on page 6-2 and Figure 6-2 on page 6-3). The total embedded SRAM for each device can be found in the datasheets. These memory blocks are arranged along the top and bottom of the device to allow better access from the core and I/O (in some devices, they are only available on the north side of the device). Every RAM block has a flexible, hardwired, embedded FIFO controller, enabling the user to implement efficient FIFOs without sacrificing user gates.

In the IGLOO and ProASIC3 families of devices, the following memories are supported:

- 15 k and 30 k gate devices do not support SRAM and FIFO.
- 60 k and 125 k gate devices support memories on the north side of the device only.
- 250 k devices and larger support memories on the north and south sides of the device.

In Fusion devices, the following memories are supported:

- AFS090 and AFS250 support memories on the north side of the device only.
- AFS600 and AFS1500 support memories on the north and south sides of the device.



Notes:

1. *AES decryption not supported in 15 k and 30 k gate devices*
2. *Flash*Freeze is supported only in IGLOO, IGLOO PLUS, and IGLOOe and ProASIC3L devices.*

Figure 6-1 • **IGLOO and ProASIC3 Device Architecture Overview**

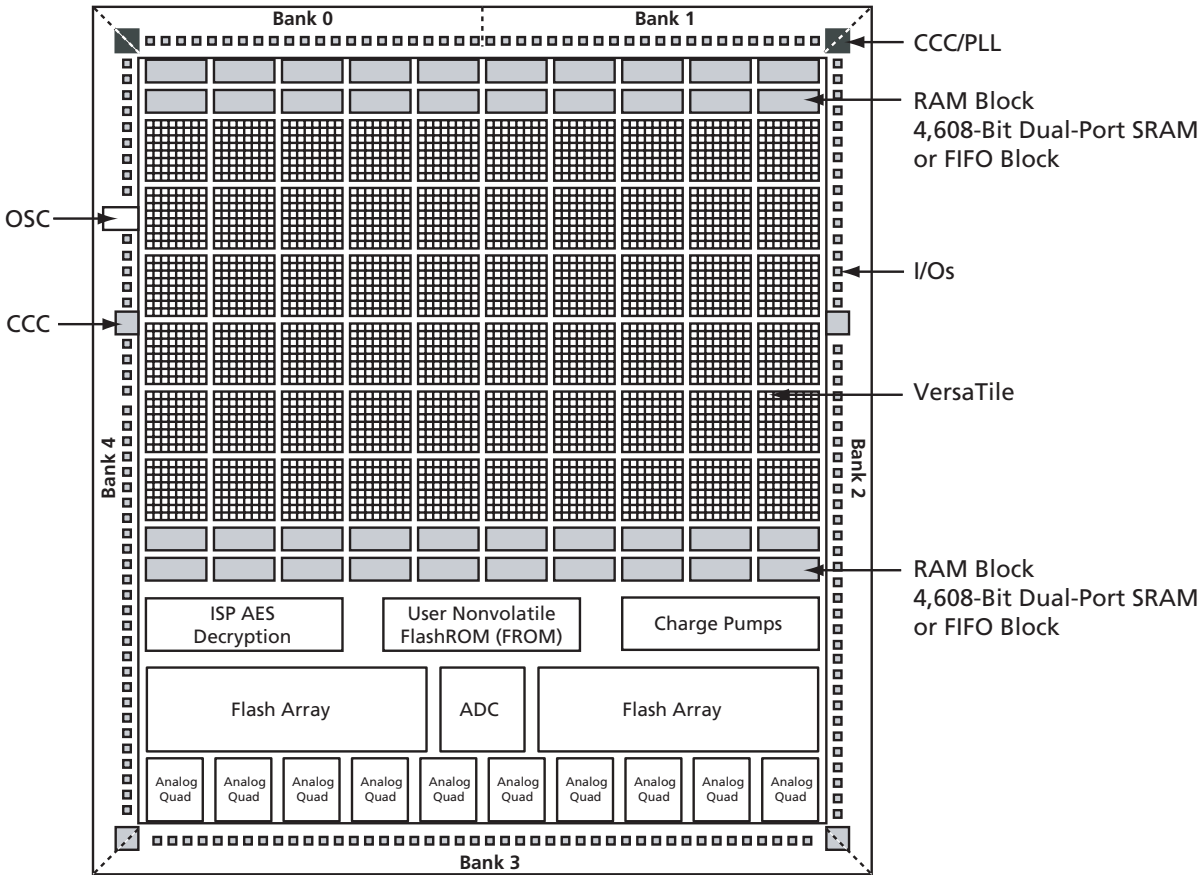


Figure 6-2 • **Fusion Device Architecture Overview (AFS600)**

SRAM/FIFO Support in Low-Power Devices

The low-power flash families listed in Table 6-1 support SRAM and FIFO blocks and the functions described in this document.

Table 6-1 • **Low-Power Flash Families**

Family[1]	Description	Timing Numbers[2]
IGLOO	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*IGLOO DC and Switching Characteristics*
IGLOO PLUS	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology and enhanced I/O capabilities	*IGLOO PLUS DC and Switching Characteristics*
IGLOOe	IGLOO devices enhanced with higher density, five additional PLLs, and additional I/O standards	*IGLOOe DC and Switching Characteristics*
ProASIC3L	Low-power, high-performance 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*ProASIC3L DC and Switching Characteristics*
ProASIC3	Low-power, high-performance 1.5 V FPGAs	*ProASIC3 DC and Switching Characteristics*
ProASIC3E	ProASIC3 enhanced with higher density, six additional PLLs, and additional I/O standards	*ProASIC3E DC and Switching Characteristics*
ProASIC3 Automotive	Low-power, high-performance FPGAs qualified for automotive applications	*Automotive ProASIC3 DC and Switching Characteristics*
Fusion	Low-power mixed-signal Programmable System Chip (PSC)	*Fusion DC and Power Characteristics*

Notes:

1. *The family names are linked to the appropriate product brief.*
2. *The timing number links go to the relevant timing numbers in the datasheet.*

Actel's low-power flash devices (listed in Table 6-1) provide a selection of low-power, secure, live-at-power-up, single-chip solutions. The nonvolatile flash-based devices do not require a boot PROM and incorporate FlashLock® technology, which provides a unique combination of reprogrammability and design security without external overhead. Only low-power flash FPGAs can offer these advantages.

Actel IGLOO PLUS FPGAs are the industry-leading 1.2 V ultra-low-power programmable logic devices (PLDs) and consume 90% less static power and over 50% less dynamic power than PLD alternatives, while ProASIC3L devices offer a balance of low power and higher performance.

Flash*Freeze technology used in IGLOO, IGLOO PLUS, and ProASIC3L devices enables easy entry to and exit from the ultra-low power mode, which consumes as little as 5 µW, while retaining SRAM and register data. IGLOO PLUS also offers the ability to hold I/O state in Flash*Freeze mode. Flash*Freeze technology simplifies power management through I/O and clock management without the need to turn off voltages, I/Os, or clocks at the system level. Entering and exiting Flash*Freeze mode takes less than 1 µs.

The Actel Fusion® family, based on the highly successful ProASIC3 flash FPGA architecture, has been designed as a high-performance, mixed-signal Programmable System Chip. Fusion supports many peripherals, including embedded flash memory, analog-to-digital converter (ADC), high-drive outputs, RC and crystal oscillators, and real-time counter (RTC). The total available on-chip memory, including the flash array blocks, is greater than that found in SRAM FPGAs.

IGLOO Terminology

In documentation, the term IGLOO families or IGLOO devices refers to all IGLOO families as listed in Table 6-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

ProASIC3 Terminology

In documentation, the term ProASIC3 families or ProASIC3 devices refers to all ProASIC3 families as listed in Table 6-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

SRAM and FIFO Architecture

To meet the needs of high-performance designs, the memory blocks operate strictly in synchronous mode for both read and write operations. The read and write clocks are completely independent, and each can operate at any desired frequency up to 250 MHz.

- 4k×1, 2k×2, 1k×4, 512×9 (dual-port RAM—2 read / 2 write or 1 read / 1 write)
- 512×9, 256×18 (2-port RAM—1 read / 1 write)
- Sync write, sync pipelined / nonpipelined read

Automotive ProASIC3 devices support single-port SRAM capabilities or dual-port SRAM only under specific conditions. Dual-port mode is supported if the clocks to the two SRAM ports are the same and 180° out of phase (i.e., the port A clock is the inverse of the port B clock). The Actel Libero® Integrated Design Environment (IDE) software macro libraries support a dual-port macro only. For use of this macro as a single-port SRAM, the inputs and clock of one port should be tied off (grounded) to prevent errors during design compile. For use in dual-port mode, the same clock with an inversion between the two clock pins of the macro should be used in the design to prevent errors during compile.

The IGLOOe and ProASIC3E memory block includes dedicated FIFO control logic to generate internal addresses and external flag logic (FULL, EMPTY, AFULL, AEMPTY).

Simultaneous dual-port read/write and write/write operations at the same address are allowed when certain timing requirements are met.

During RAM operation, addresses are sourced by the user logic, and the FIFO controller is ignored. In FIFO mode, the internal addresses are generated by the FIFO controller and routed to the RAM array by internal MUXes.

The low-power flash device architecture enables the read and write sizes of RAMs to be organized independently, allowing for bus conversion. For example, the write size can be set to 256×18 and the read size to 512×9.

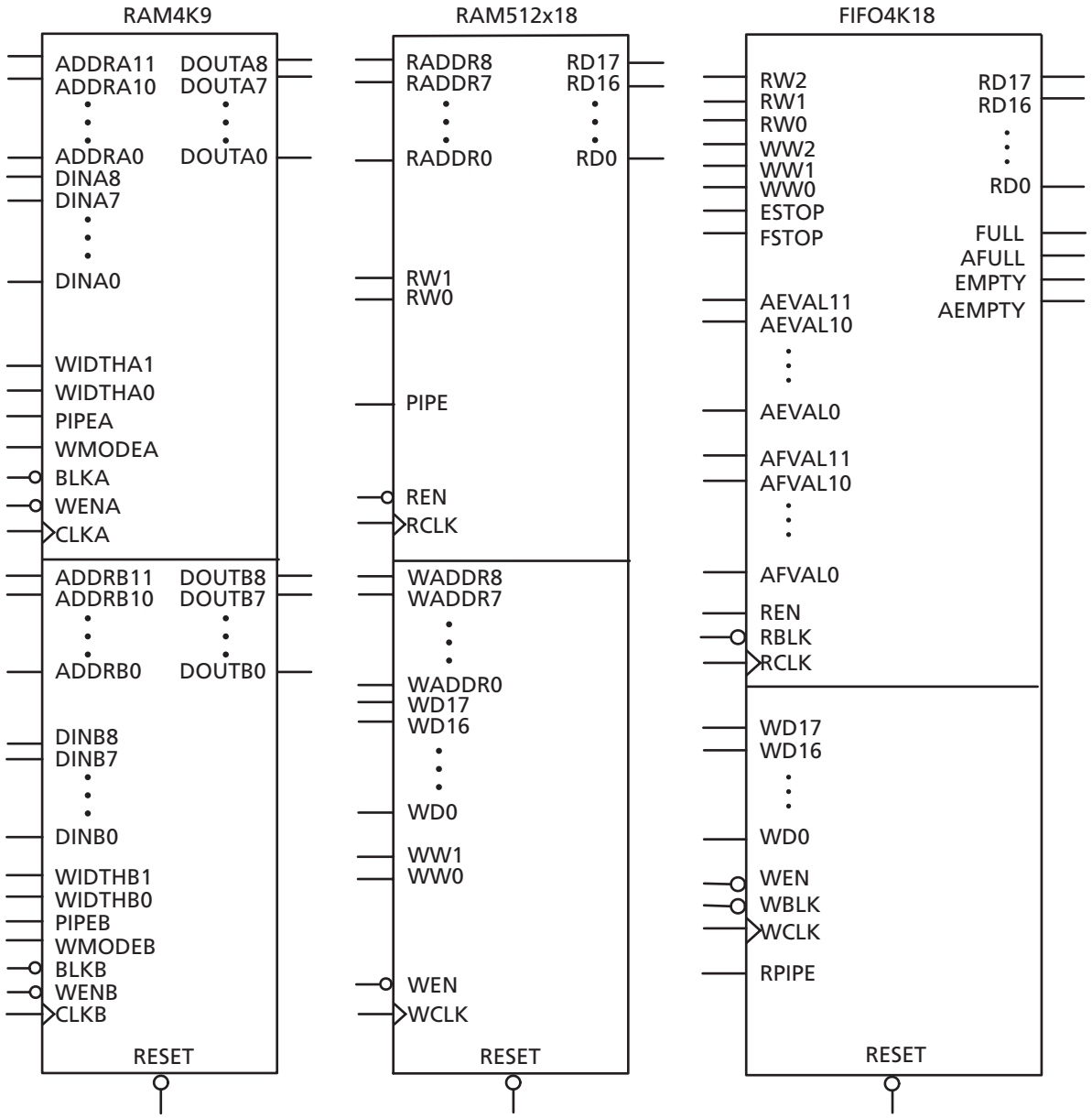
Both the write width and read width for the RAM blocks can be specified independently with the WW (write width) and RW (read width) pins. The different D×W configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1. When widths of one, two, or four are selected, the ninth bit is unused. For example, when writing nine-bit values and reading four-bit values, only the first four bits and the second four bits of each nine-bit value are addressable for read operations. The ninth bit is not accessible.

Conversely, when writing four-bit values and reading nine-bit values, the ninth bit of a read operation will be undefined. The RAM blocks employ little-endian byte order for read and write operations.

Memory Blocks and Macros

Memory blocks can be configured with many different aspect ratios, but are generically supported in the macro libraries as one of two memory elements: RAM4K9 or RAM512X18. The RAM4K9 is configured as a true dual-port memory block, and the RAM512X18 is configured as a two-port memory block. Dual-port memory allows the RAM to both read from and write to either port independently. Two-port memory allows the RAM to read from one port and write to the other using a common clock or independent read and write clocks. If needed, the RAM4K9 blocks can be configured as two-port memory blocks. The memory block can be configured as a FIFO by combining the basic memory block with dedicated FIFO controller logic. The FIFO macro is named FIFO4KX18 (Figure 6-3 on page 6-6).

Clocks for the RAM blocks can be driven by the VersaNet (global resources) or by regular nets. When using local clock segments, the clock segment region that encompasses the RAM blocks can drive the RAMs. In the dual-port configuration (RAM4K9), each memory block port can be driven by either rising-edge or falling-edge clocks. Each port can be driven by clocks with different edges. Though only a rising-edge clock can drive the physical block itself, the Actel Designer software will automatically bubble-push the inversion to properly implement the falling-edge trigger for the RAM block.



Note: Automotive ProASIC3 devices restrict RAM4K9 to a single port or to dual ports with the same clock 180° out of phase (inverted) between clock pins. In single-port mode, inputs to port B should be tied to ground to prevent errors during compile. For FIFO4K18, the same clock 180° out of phase (inverted) between clock pins should be used.

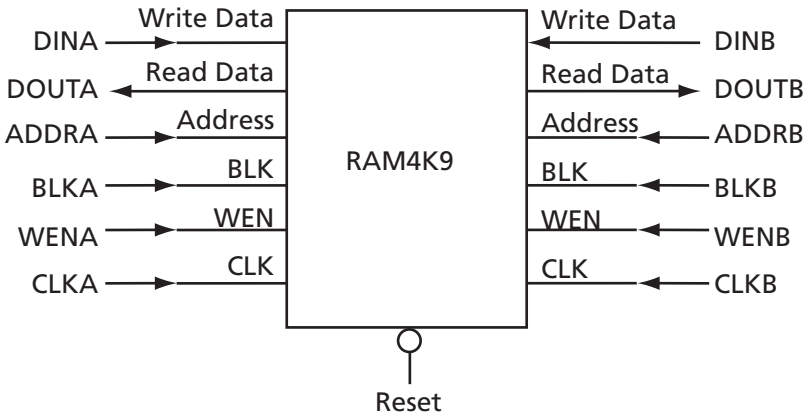
Figure 6-3 • **Supported Basic RAM Macros**

SRAM Features

RAM4K9 Macro

RAM4K9 is the dual-port configuration of the RAM block (Figure 6-4). The RAM4K9 nomenclature refers to both the deepest possible configuration and the widest possible configuration the dual-port RAM block can assume, and does not denote a possible memory aspect ratio. The RAM block can be configured to the following aspect ratios: 4,096x1, 2,048x2, 1,024x4, and 512x9. RAM4K9 is fully synchronous and has the following features:

- Two ports that allow fully independent reads and writes at different frequencies
- Selectable pipelined or nonpipelined read
- Active-low block enables for each port
- Toggle control between read and write mode for each port
- Active-low asynchronous reset
- Pass-through write data or hold existing data on output. In pass-through mode, the data written to the write port will immediately appear on the read port.
- Designer software will automatically facilitate falling-edge clocks by bubble-pushing the inversion to previous stages.



Note: For timing diagrams of the RAM signals, refer to the appropriate family datasheet.

Figure 6-4 • **RAM4K9 Simplified Configuration**

Signal Descriptions for RAM4K9

Note: Automotive ProASIC3 devices support single-port SRAM capabilities, or dual-port SRAM only under specific conditions. Dual-port mode is supported if the clocks to the two SRAM ports are the same and 180° out of phase (i.e., the port A clock is the inverse of the port B clock). Since Actel Libero IDE macro libraries support a dual-port macro only, certain modifications must be made. These are detailed below.

The following signals are used to configure the RAM4K9 memory element:

WIDTHA and WIDTHB

These signals enable the RAM to be configured in one of four allowable aspect ratios (Table 6-2 on page 6-8).

Note: When using the SRAM in single-port mode for Automotive ProASIC3 devices, WIDTHB should be tied to ground.

Table 6-2 • **Allowable Aspect Ratio Settings for WIDTHA[1:0]**

WIDTHA[1:0]	WIDTHB[1:0]	D×W
00	00	4k×1
01	01	2k×2
10	10	1k×4
11	11	512×9

Note: The aspect ratio settings are constant and cannot be changed on the fly.

BLKA and BLKB

These signals are active-low and will enable the respective ports when asserted. When a BLKx signal is deasserted, that port's outputs hold the previous value.

Note: When using the SRAM in single-port mode for Automotive ProASIC3 devices, BLKB should be tied to ground.

WENA and WENB

These signals switch the RAM between read and write modes for the respective ports. A LOW on these signals indicates a write operation, and a HIGH indicates a read.

Note: When using the SRAM in single-port mode for Automotive ProASIC3 devices, WENB should be tied to ground.

CLKA and CLKB

These are the clock signals for the synchronous read and write operations. These can be driven independently or with the same driver.

Note: For Automotive ProASIC3 devices, dual-port mode is supported if the clocks to the two SRAM ports are the same and 180° out of phase (i.e., the port A clock is the inverse of the port B clock). For use of this macro as a single-port SRAM, the inputs and clock of one port should be tied off (grounded) to prevent errors during design compile.

PIPEA and PIPEB

These signals are used to specify pipelined read on the output. A LOW on PIPEA or PIPEB indicates a nonpipelined read, and the data appears on the corresponding output in the same clock cycle. A HIGH indicates a pipelined read, and data appears on the corresponding output in the next clock cycle.

Note: When using the SRAM in single-port mode for Automotive ProASIC3 devices, PIPEB should be tied to ground. For use in dual-port mode, the same clock with an inversion between the two clock pins of the macro should be used in the design to prevent errors during compile.

WMODEA and WMODEB

These signals are used to configure the behavior of the output when the RAM is in write mode. A LOW on these signals makes the output retain data from the previous read. A HIGH indicates pass-through behavior, wherein the data being written will appear immediately on the output. This signal is overridden when the RAM is being read.

Note: When using the SRAM in single-port mode for Automotive ProASIC3 devices, WMODEB should be tied to ground.

RESET

This active-low signal resets the control logic, forces the output hold state registers to zero, disables reads and writes from the SRAM block, and clears the data hold registers when asserted. It does not reset the contents of the memory array.

While the RESET signal is active, read and write operations are disabled. As with any asynchronous reset signal, care must be taken not to assert it too close to the edges of active read and write clocks.

ADDRA and ADDRB

These are used as read or write addresses, and they are 12 bits wide. When a depth of less than 4 k is specified, the unused high-order bits must be grounded (Table 6-3 on page 6-9).

Note: When using the SRAM in single-port mode for Automotive ProASIC3 devices, ADDRB should be tied to ground.

Table 6-3 • **Address Pins Unused/Used for Various Supported Bus Widths**

D×W	ADDRx	
	Unused	Used
4k×1	None	[11:0]
2k×2	[11]	[10:0]
1k×4	[11:10]	[9:0]
512×9	[11:9]	[8:0]

Note: The "x" in ADDRx implies A or B.

DINA and DINB

These are the input data signals, and they are nine bits wide. Not all nine bits are valid in all configurations. When a data width less than nine is specified, unused high-order signals must be grounded (Table 6-4).

Note: When using the SRAM in single-port mode for Automotive ProASIC3 devices, DINB should be tied to ground.

DOUTA and DOUTB

These are the nine-bit output data signals. Not all nine bits are valid in all configurations. As with DINA and DINB, high-order bits may not be used (Table 6-4). The output data on unused pins is undefined.

Table 6-4 • **Unused/Used Input and Output Data Pins for Various Supported Bus Widths**

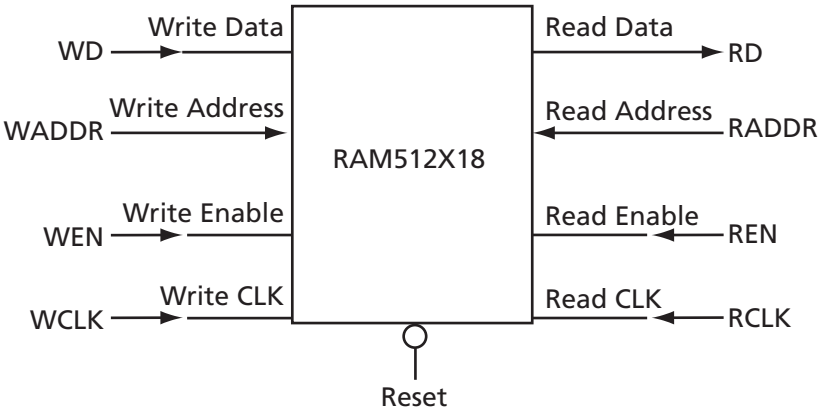
D×W	DINx/DOUTx	
	Unused	Used
4k×1	[8:1]	[0]
2k×2	[8:2]	[1:0]
1k×4	[8:4]	[3:0]
512×9	None	[8:0]

Note: The "x" in DINx or DOUTx implies A or B.

RAM512X18 Macro

RAM512X18 is the two-port configuration of the same RAM block (Figure 6-5 on page 6-10). Like the RAM4K9 nomenclature, the RAM512X18 nomenclature refers to both the deepest possible configuration and the widest possible configuration the two-port RAM block can assume. In two-port mode, the RAM block can be configured to either the 512x9 aspect ratio or the 256x18 aspect ratio. RAM512X18 is also fully synchronous and has the following features:

- Dedicated read and write ports
- Active-low read and write enables
- Selectable pipelined or nonpipelined read
- Active-low asynchronous reset
- Designer software will automatically facilitate falling-edge clocks by bubble-pushing the inversion to previous stages.



Note: For timing diagrams of the RAM signals, refer to the appropriate family datasheet.

Figure 6-5 • **512X18 Two-Port RAM Block Diagram**

Signal Descriptions for RAM512X18

RAM512X18 has slightly different behavior from RAM4K9, as it has dedicated read and write ports.

WW and RW

These signals enable the RAM to be configured in one of the two allowable aspect ratios (Table 6-5).

Table 6-5 • **Aspect Ratio Settings for WW[1:0]**

WW[1:0]	RW[1:0]	D×W
01	01	512×9
10	10	256×18
00, 11	00, 11	Reserved

WD and RD

These are the input and output data signals, and they are 18 bits wide. When a 512×9 aspect ratio is used for write, WD[17:9] are unused and must be grounded. If this aspect ratio is used for read, RD[17:9] are undefined.

WADDR and RADDR

These are read and write addresses, and they are nine bits wide. When the 256×18 aspect ratio is used for write or read, WADDR[8] and RADDR[8] are unused and must be grounded.

WCLK and RCLK

These signals are the write and read clocks, respectively. They can be clocked on the rising or falling edge of WCLK and RCLK.

WEN and REN

These signals are the write and read enables, respectively. They are both active-low by default. These signals can be configured as active-high.

RESET

This active-low signal resets the control logic, forces the output hold state registers to zero, disables reads and writes from the SRAM block, and clears the data hold registers when asserted. It does not reset the contents of the memory array.

While the RESET signal is active, read and write operations are disabled. As with any asynchronous reset signal, care must be taken not to assert it too close to the edges of active read and write clocks.

PIPE

This signal is used to specify pipelined read on the output. A LOW on PIPE indicates a nonpipelined read, and the data appears on the output in the same clock cycle. A HIGH indicates a pipelined read, and data appears on the output in the next clock cycle.

SRAM Usage

The following descriptions refer to the usage of both RAM4K9 and RAM512X18.

Clocking

The dual-port SRAM blocks are only clocked on the rising edge. SmartGen allows falling-edge-triggered clocks by adding inverters to the netlist, hence achieving dual-port SRAM blocks that are clocked on either edge (rising or falling). For dual-port SRAM, each port can be clocked on either edge and by separate clocks by port. Note that for Automotive ProASIC3, the same clock, with an inversion between the two clock pins of the macro, should be used in design to prevent errors during compile.

IGLOO and ProASIC3 devices support inversion (bubble-pushing) throughout the FPGA architecture, including the clock input to the SRAM modules. Inversions added to the SRAM clock pin on the design schematic or in the HDL code will be automatically accounted for during design compile without incurring additional delay in the clock path.

The two-port SRAM can be clocked on the rising or falling edge of WCLK and RCLK.

If negative-edge RAM and FIFO clocking is selected for memory macros, clock edge inversion management (bubble-pushing) is automatically used within the IGLOO and ProASIC3 development tools, without performance penalty.

Modes of Operation

There are two read modes and one write mode:

- Read Nonpipelined (synchronous—1 clock edge): In the standard read mode, new data is driven onto the RD bus in the same clock cycle following RA and REN valid. The read address is registered on the read port clock active edge, and data appears at RD after the RAM access time. Setting PIPE to OFF enables this mode.
- Read Pipelined (synchronous—2 clock edges): The pipelined mode incurs an additional clock delay from address to data but enables operation at a much higher frequency. The read address is registered on the read port active clock edge, and the read data is registered and appears at RD after the second read clock edge. Setting PIPE to ON enables this mode.
- Write (synchronous—1 clock edge): On the write clock active edge, the write data is written into the SRAM at the write address when WEN is HIGH. The setup times of the write address, write enables, and write data are minimal with respect to the write clock.

RAM Initialization

Each SRAM block can be individually initialized on power-up by means of the JTAG port using the UJTAG mechanism. The shift register for a target block can be selected and loaded with the proper bit configuration to enable serial loading. The 4,608 bits of data can be loaded in a single operation.

FIFO Features

The FIFO4KX18 macro is created by merging the RAM block with dedicated FIFO logic (Figure 6-6 on page 6-12). Since the FIFO logic can only be used in conjunction with the memory block, there is no separate FIFO controller macro. As with the RAM blocks, the FIFO4KX18 nomenclature does not refer to a possible aspect ratio, but rather to the deepest possible data depth and the widest possible data width. FIFO4KX18 can be configured into the following aspect ratios: 4,096x1, 2,048x2, 1,024x4, 512x9, and 256x18. In addition to being fully synchronous, the FIFO4KX18 also has the following features:

- Four FIFO flags: Empty, Full, Almost-Empty, and Almost-Full
- EMPTY flag is synchronized to the read clock
- FULL flag is synchronized to the write clock
- Both Almost-Empty and Almost-Full flags have programmable thresholds

- Active-low asynchronous reset
- Active-low block enable
- Active-low write enable
- Active-high read enable
- Ability to configure the FIFO to either stop counting after the empty or full states are reached or to allow the FIFO counters to continue
- Designer software will automatically facilitate falling-edge clocks by bubble-pushing the inversion to previous stages.

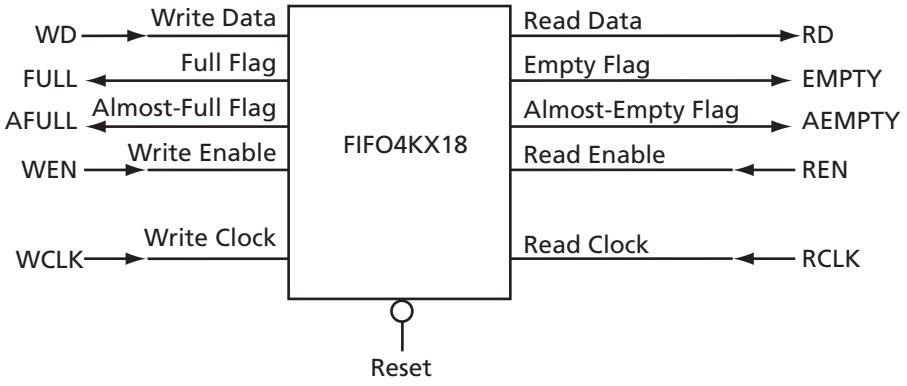


Figure 6-6 • **FIFO4KX18 Block Diagram**

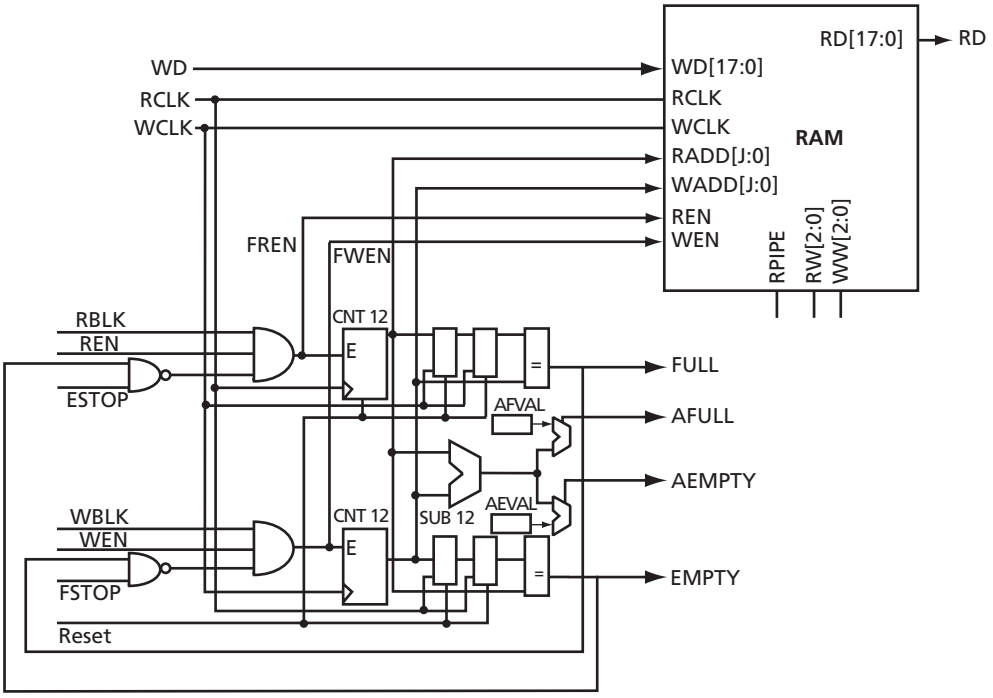


Figure 6-7 • **RAM Block with Embedded FIFO Controller**

The FIFOs maintain a separate read and write address. Whenever the difference between the write address and the read address is greater than or equal to the almost-full value (AFVAL), the Almost-Full flag is asserted. Similarly, the Almost-Empty flag is asserted whenever the difference between the write address and read address is less than or equal to the almost-empty value (AEVAL).

Due to synchronization between the read and write clocks, the Empty flag will deassert after the second read clock edge from the point that the write enable asserts. However, since the Empty flag is synchronized to the read clock, it will assert after the read clock reads the last data in the FIFO. Also, since the Full flag is dependent on the actual hardware configuration, it will assert when the actual physical implementation of the FIFO is full.

For example, when a user configures a 128×18 FIFO, the actual physical implementation will be a 256×18 FIFO element. Since the actual implementation is 256×18, the Full flag will not trigger until the 256×18 FIFO is full, even though a 128×18 FIFO was requested. For this example, the Almost-Full flag can be used instead of the Full flag to signal when the 128th data word is reached.

To accommodate different aspect ratios, the almost-full and almost-empty values are expressed in terms of data bits instead of data words. SmartGen translates the user's input, expressed in data words, into data bits internally. SmartGen allows the user to select the thresholds for the Almost-Empty and Almost-Full flags in terms of either the read data words or the write data words, and makes the appropriate conversions for each flag.

After the empty or full states are reached, the FIFO can be configured so the FIFO counters either stop or continue counting. For timing numbers, refer to the appropriate family datasheet.

Signal Descriptions for FIFO4K18

The following signals are used to configure the FIFO4K18 memory element:

WW and RW

These signals enable the FIFO to be configured in one of the five allowable aspect ratios (Table 6-6).

Table 6-6 • **Aspect Ratio Settings for WW[2:0]**

WW[2:0]	RW[2:0]	D×W
000	000	4k×1
001	001	2k×2
010	010	1k×4
011	011	512×9
100	100	256×18
101, 110, 111	101, 110, 111	Reserved

WBLK and RBLK

These signals are active-low and will enable the respective ports when LOW. When the RBLK signal is HIGH, that port's outputs hold the previous value.

WEN and REN

Read and write enables. WEN is active-low and REN is active-high by default. These signals can be configured as active-high or -low.

WCLK and RCLK

These are the clock signals for the synchronous read and write operations. These can be driven independently or with the same driver.

Note: For the Automotive ProASIC3 FIFO4K18, for the same clock, 180° out of phase (inverted) between clock pins should be used.

RPIPE

This signal is used to specify pipelined read on the output. A LOW on RPIPE indicates a nonpipelined read, and the data appears on the output in the same clock cycle. A HIGH indicates a pipelined read, and data appears on the output in the next clock cycle.

RESET

This active-low signal resets the control logic and forces the output hold state registers to zero when asserted. It does not reset the contents of the memory array (Table 6-7 on page 6-14).

While the RESET signal is active, read and write operations are disabled. As with any asynchronous RESET signal, care must be taken not to assert it too close to the edges of active read and write clocks.

WD

This is the input data bus and is 18 bits wide. Not all 18 bits are valid in all configurations. When a data width less than 18 is specified, unused higher-order signals must be grounded (Table 6-7).

RD

This is the output data bus and is 18 bits wide. Not all 18 bits are valid in all configurations. Like the WD bus, high-order bits become unusable if the data width is less than 18. The output data on unused pins is undefined (Table 6-7).

Table 6-7 • **Input Data Signal Usage for Different Aspect Ratios**

D×W	WD/RD Unused
4k×1	WD[17:1], RD[17:1]
2k×2	WD[17:2], RD[17:2]
1k×4	WD[17:4], RD[17:4]
512×9	WD[17:9], RD[17:9]
256×18	–

ESTOP, FSTOP

ESTOP is used to stop the FIFO read counter from further counting once the FIFO is empty (i.e., the EMPTY flag goes HIGH). A HIGH on this signal inhibits the counting.

FSTOP is used to stop the FIFO write counter from further counting once the FIFO is full (i.e., the FULL flag goes HIGH). A HIGH on this signal inhibits the counting.

For more information on these signals, refer to the "ESTOP and FSTOP Usage" section on page 6-15.

FULL, EMPTY

When the FIFO is full and no more data can be written, the FULL flag asserts HIGH. The FULL flag is synchronous to WCLK to inhibit writing immediately upon detection of a full condition and to prevent overflows. Since the write address is compared to a resynchronized (and thus time-delayed) version of the read address, the FULL flag will remain asserted until two WCLK active edges after a read operation eliminates the full condition.

When the FIFO is empty and no more data can be read, the EMPTY flag asserts HIGH. The EMPTY flag is synchronous to RCLK to inhibit reading immediately upon detection of an empty condition and to prevent underflows. Since the read address is compared to a resynchronized (and thus time-delayed) version of the write address, the EMPTY flag will remain asserted until two RCLK active edges after a write operation removes the empty condition.

For more information on these signals, refer to the "FIFO Flag Usage Considerations" section on page 6-15.

AFULL, AEMPTY

These are programmable flags and will be asserted on the threshold specified by AFVAL and AEVAL, respectively.

When the number of words stored in the FIFO reaches the amount specified by AEVAL while reading, the AEMPTY output will go HIGH. Likewise, when the number of words stored in the FIFO reaches the amount specified by AFVAL while writing, the AFULL output will go HIGH.

AFVAL, AEVAL

The AEVAL and AFVAL pins are used to specify the almost-empty and almost-full threshold values. They are 12-bit signals. For more information on these signals, refer to the "FIFO Flag Usage Considerations" section on page 6-15.

FIFO Usage

ESTOP and FSTOP Usage

The ESTOP pin is used to stop the read counter from counting any further once the FIFO is empty (i.e., the EMPTY flag goes HIGH). Likewise, the FSTOP pin is used to stop the write counter from counting any further once the FIFO is full (i.e., the FULL flag goes HIGH).

The FIFO counters in the IGLOOe and ProASIC3E device start the count at zero, reach the maximum depth for the configuration (e.g., 511 for a 512×9 configuration), and then restart at zero. An example application for ESTOP, where the read counter keeps counting, would be writing to the FIFO once and reading the same content over and over without doing another write.

FIFO Flag Usage Considerations

The AEVAL and AFVAL pins are used to specify the 12-bit AEMPTY and AFULL threshold values. The FIFO contains separate 12-bit write address (WADDR) and read address (RADDR) counters. WADDR is incremented every time a write operation is performed, and RADDR is incremented every time a read operation is performed. Whenever the difference between WADDR and RADDR is greater than or equal to AFVAL, the AFULL output is asserted. Likewise, whenever the difference between WADDR and RADDR is less than or equal to AEVAL, the AEMPTY output is asserted. To handle different read and write aspect ratios, AFVAL and AEVAL are expressed in terms of total data bits instead of total data words. When users specify AFVAL and AEVAL in terms of read or write words, the SmartGen tool translates them into bit addresses and configures these signals automatically. SmartGen configures the AFULL flag to assert when the write address exceeds the read address by at least a predefined value. In a 2k×8 FIFO, for example, a value of 1,500 for AFVAL means that the AFULL flag will be asserted after a write when the difference between the write address and the read address reaches 1,500 (there have been at least 1,500 more writes than reads). It will stay asserted until the difference between the write and read addresses drops below 1,500.

The AEMPTY flag is asserted when the difference between the write address and the read address is less than a predefined value. In the example above, a value of 200 for AEVAL means that the AEMPTY flag will be asserted when a read causes the difference between the write address and the read address to drop to 200. It will stay asserted until that difference rises above 200. Note that the FIFO can be configured with different read and write widths; in this case, the AFVAL setting is based on the number of write data entries, and the AEVAL setting is based on the number of read data entries. For aspect ratios of 512×9 and 256×18, only 4,096 bits can be addressed by the 12 bits of AFVAL and AEVAL. The number of words must be multiplied by 8 and 16 instead of 9 and 18. The SmartGen tool automatically uses the proper values. To avoid halfwords being written or read, which could happen if different read and write aspect ratios were specified, the FIFO will assert FULL or EMPTY as soon as at least one word cannot be written or read. For example, if a two-bit word is written and a four-bit word is being read, the FIFO will remain in the empty state when the first word is written. This occurs even if the FIFO is not completely empty, because in this case, a complete word cannot be read. The same is applicable in the full state. If a four-bit word is written and a two-bit word is read, the FIFO is full and one word is read. The FULL flag will remain asserted because a complete word cannot be written at this point.

Variable Aspect Ratio and Cascading

Variable aspect ratio and cascading allow users to configure the memory in the width and depth required. The memory block can be configured as a FIFO by combining the basic memory block with dedicated FIFO controller logic. The FIFO macro is named FIFO4KX18. Low-power flash device RAM can be configured as 1, 2, 4, 9, or 18 bits wide. By cascading the memory blocks, any multiple of those widths can be created. The RAM blocks can be from 256 to 4,096 bits deep, depending on the aspect ratio, and the blocks can also be cascaded to create deeper areas. Refer to the aspect ratios available for each macro cell in the "SRAM Features" section on page 6-7. The largest continuous configurable memory area is equal to half the total memory available on the device, because the RAM is separated into two groups, one on each side of the device.

The Actel SmartGen core generator will automatically configure and cascade both RAM and FIFO blocks. Cascading is accomplished using dedicated memory logic and does not consume user gates for depths up to 4,096 bits deep and widths up to 18, depending on the configuration. Deeper memory will utilize some user gates to multiplex the outputs.

Generated RAM and FIFO macros can be created as either structural VHDL or Verilog for easy instantiation into the design. Users of Actel Libero IDE can create a symbol for the macro and incorporate it into a design schematic.

Table 6-10 on page 6-17 shows the number of memory blocks required for each of the supported depth and width memory configurations, and for each depth and width combination. For example, a 256-bit deep by 32-bit wide two-port RAM would consist of two 256×18 RAM blocks. The first 18 bits would be stored in the first RAM block, and the remaining 14 bits would be implemented in the other 256×18 RAM block. This second RAM block would have four bits of unused storage. Similarly, a dual-port memory block that is 8,192 bits deep and 8 bits wide would be implemented using 16 memory blocks. The dual-port memory would be configured in a 4,096×1 aspect ratio. These blocks would then be cascaded two deep to achieve 8,192 bits of depth, and eight wide to achieve the eight bits of width.

Table 6-8 and Table 6-9 show the maximum potential width and depth configuration for each device. Note that 15 k and 30 k gate devices do not support RAM or FIFO.

Table 6-8 • **Memory Availability per IGLOO and ProASIC3 Devices**

Device		RAM Blocks	Maximum Potential Width[1]		Maximum Potential Depth[2]	
IGLOO/ IGLOO PLUS	ProASIC3/ ProASIC3L		Depth	Width	Depth	Width
AGL060 / AGLP060	A3P060	4	256	72 (4×18)	16,384 (4,096×4)	1
AGL125 AGLP125	A3P125	8	256	144 (8×18)	32,768 (4,094×8)	1
AGL250	A3P250/L	8	256	144 (8×18)	32,768 (4,096×8)	1
	A3P400	12	256	216 (12×18)	49,152 (4,096×12)	1
AGL600	A3P600/L	24	256	432 (24×18)	98,304 (4,096×24)	1
AGL1000	A3P1000/L	32	256	576 (32×18)	131,072 (4,096×32)	1
AGLE600	A3PE600	24	256	432 (24×18)	98,304 (4,096×24)	1
	A3PE1500	60	256	1,080 (60×18)	245,760 (4,096×60)	1
AGLE3000	A3PE3000/L	112	256	2,016 (112×18)	458,752 (4,096×112)	1

Notes:

1. *Maximum potential width uses the two-port configuration.*
2. *Maximum potential depth uses the dual-port configuration.*

Table 6-9 • **Memory Availability per Fusion Device**

Device	RAM Blocks	Maximum Potential Width[1]		Maximum Potential Depth[2]	
		Depth	Width	Depth	Width
AFS090	6	256	108 (6×18)	24,576 (4,094×6)	1
AFS250	8	256	144 (8×18)	32,768 (4,094×8)	1
AFS600	24	256	432 (24×18)	98,304 (4,096×24)	1
AFS1500	60	256	1,080 (60×18)	245,760 (4,096×60)	1

Notes:

1. *Maximum potential width uses the two-port configuration.*
2. *Maximum potential depth uses the dual-port configuration.*

Table 6-10 • **RAM and FIFO Memory Block Consumption**

			Depth									
			256		512	1,024	2,048	4,096	8,192	16,384	32,768	65,536
			Two-Port	Dual-Port	Dual-Port	Dual-Port	Dual-Port	Dual-Port	Dual-Port	Dual-Port	Dual-Port	Dual-Port
Width	1	Number Block	1	1	1	1	1	1	2	4	8	16 × 1
		Configuration	Any	Any	Any	1,024 × 4	2,048 × 2	4,096 × 1	2 × (4,096 × 1) Cascade Deep	4 × (4,096 × 1) Cascade Deep	8 × (4,096 × 1) Cascade Deep	16 × (4,096 × 1) Cascade Deep
	2	Number Block	1	1	1	1	1	2	4	8	16	32
		Configuration	Any	Any	Any	1,024×4	2,048 × 2	2 × (4,096 × 1) Cascaded Wide	4 × (4,096 × 1) Cascaded 2 Deep and 2 Wide	8 × (4,096 × 1) Cascaded 4 Deep and 2 Wide	16 × (4,096 × 1) Cascaded 8 Deep and 2 Wide	32 × (4,096 × 1) Cascaded 16 Deep and 2 Wide
	4	Number Block	1	1	1	1	2	4	8	16	32	64
		Configuration	Any	Any	Any	1,024 × 4	2 × (2,048 × 2) Cascaded Wide	4 × (4,096 × 1) Cascaded Wide	4 × (4,096 × 1) Cascaded 2 Deep and 4 Wide	16 × (4,096 × 1) Cascaded 4 Deep and 4 Wide	32 × (4,096 × 1) Cascaded 8 Deep and 4 Wide	64 × (4,096 × 1) Cascaded 16 Deep and 4 Wide
	8	Number Block	1	1	1	2	4	8	16	32	64	
		Configuration	Any	Any	Any	2 × (1,024 × 4) Cascaded Wide	4 × (2,048 × 2) Cascaded Wide	8 × (4,096 × 1) Cascaded Wide	16 × (4,096 × 1) Cascaded 2 Deep and 8 Wide	32 × (4,096 × 1) Cascaded 4 Deep and 8 Wide	64 × (4,096 × 1) Cascaded 8 Deep and 8 Wide	
	9	Number Block	1	1	1	2	4	8	16	32		
		Configuration	Any	Any	Any	2 × (512 × 9) Cascaded Deep	4 × (512 × 9) Cascaded Deep	8 × (512 × 9) Cascaded Deep	16 × (512 × 9) Cascaded Deep	32 × (512 × 9) Cascaded Deep		
	16	Number Block	1	1	1	4	8	16	32	64		
		Configuration	256 × 18	256 × 18	256 × 18	4 × (1,024 × 4) Cascaded Wide	8 × (2,048 × 2) Cascaded Wide	16 × (4,096 × 1) Cascaded Wide	32 × (4,096 × 1) Cascaded 2 Deep and 16 Wide	32 × (4,096 × 1) Cascaded 4 Deep and 16 Wide		
	18	Number Block	1	2	2	4	8	18	32			
		Configuration	256 × 8	2 × (512 × 9) Cascaded Wide	2 × (512 × 9) Cascaded Wide	4 × (512 × 9) Cascaded 2 Deep and 2 Wide	8 × (512 × 9) Cascaded 4 Deep and 2 Wide	16 × (512 × 9) Cascaded 8 Deep and 2 Wide	16 × (512 × 9) Cascaded 16 Deep and 2 Wide			
	32	Number Block	2	4	4	8	16	32	64			
		Configuration	2 × (256 × 18) Cascaded Wide	4 × (512 × 9) Cascaded Wide	4 × (512 × 9) Cascaded Wide	8 × (1,024 × 4) Cascaded Wide	16 × (2,048 × 2) Cascaded Wide	32 × (4,096 × 1) Cascaded Wide	64 × (4,096 × 1) Cascaded 2 Deep and 32 Wide			
	36	Number Block	2	4	4	8	16	32				
		Configuration	2 × (256 × 18) Cascaded Wide	4 × (512 × 9) Cascaded Wide	4 × (512 × 9) Cascaded Wide	4 × (512 × 9) Cascaded 2 Deep and 4 Wide	16 × (512 × 9) Cascaded 4 Deep and 4 Wide	16 × (512 × 9) Cascaded 8 Deep and 4 Wide				
	64	Number Block	4	8	8	16	32	64				
		Configuration	4 × (256 × 18) Cascaded Wide	8 × (512 × 9) Cascaded Wide	8 × (512 × 9) Cascaded Wide	16 × (1,024 × 4) Cascaded Wide	32 × (2,048 × 2) Cascaded Wide	64 × (4,096 × 1) Cascaded Wide				
	72	Number Block	4	8	8	16	32					
		Configuration	4 × (256 × 18) Cascaded Wide	8 × (512 × 9) Cascaded Wide	8 × (512 × 9) Cascaded Wide	16 × (512 × 9) Cascaded Wide	16 × (512 × 9) Cascaded 4 Deep and 8 Wide					

Note: Memory configurations represented by grayed cells are not supported.

Initializing the RAM/FIFO

The SRAM blocks can be initialized with data to use as a lookup table (LUT). Data initialization can be accomplished either by loading the data through the design logic or through the UJTAG interface. The UJTAG macro is used to allow access from the JTAG port to the internal logic in the device. By sending the appropriate initialization string to the JTAG Test Access Port (TAP) Controller, the designer can put the JTAG circuitry into a mode that allows the user to shift data into the array logic through the JTAG port using the UJTAG macro. For a more detailed explanation of the UJTAG macro, refer to *UJTAG Applications in Actel's Low-Power Flash Devices*.

A user interface is required to receive the user command, initialization data, and clock from the UJTAG macro. The interface must synchronize and load the data into the correct RAM block of the design. The main outputs of the user interface block are the following:

- Memory block chip select: Selects a memory block for initialization. The chip selects signals for each memory block that can be generated from different user-defined pockets or simple logic, such as a ring counter (see below).
- Memory block write address: Identifies the address of the memory cell that needs to be initialized.
- Memory block write data: The interface block receives the data serially from the UTDI port of the UJTAG macro and loads it in parallel into the write data ports of the memory blocks.
- Memory block write clock: Drives the WCLK of the memory block and synchronizes the write data, write address, and chip select signals.

Figure 6-8 shows the user interface between UJTAG and the memory blocks.

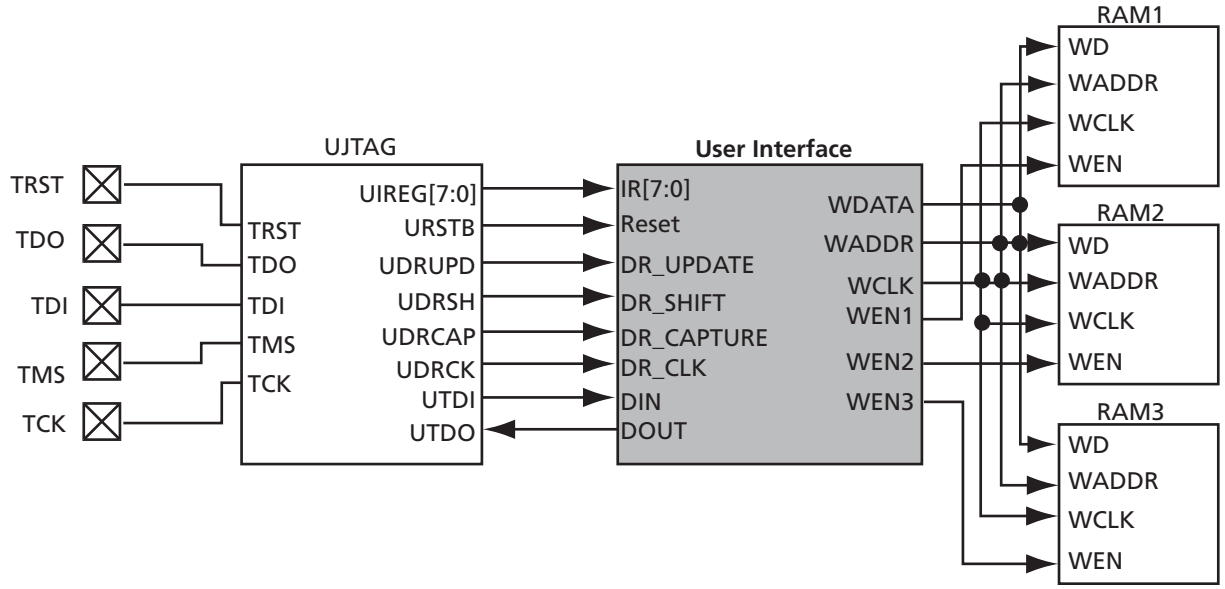


Figure 6-8 • **Interfacing TAP Ports and SRAM Blocks**

An important component of the interface between the UJTAG macro and the RAM blocks is a serial-in/parallel-out shift register. The width of the shift register should equal the data width of the RAM blocks. The RAM data arrives serially from the UTDI output of the UJTAG macro. The data must be shifted into a shift register clocked by the JTAG clock (provided at the UDRCK output of the UJTAG macro).

Then, after the shift register is fully loaded, the data must be transferred to the write data port of the RAM block. To synchronize the loading of the write data with the write address and write clock, the output of the shift register can be pipelined before driving the RAM block.

The write address can be generated in different ways. It can be imported through the TAP using a different instruction opcode and another shift register, or generated internally using a simple

counter. Using a counter to generate the address bits and sweep through the address range of the RAM blocks is recommended, since it reduces the complexity of the user interface block and the board-level JTAG driver.

Moreover, using an internal counter for address generation speeds up the initialization procedure, since the user only needs to import the data through the JTAG port.

The designer may use different methods to select among the multiple RAM blocks. Using counters along with demultiplexers is one approach to set the write enable signals. Basically, the number of RAM blocks needing initialization determines the most efficient approach. For example, if all the blocks are initialized with the same data, one enable signal is enough to activate the write procedure for all of them at the same time. Another alternative is to use different opcodes to initialize each memory block. For a small number of RAM blocks, using counters is an optimal choice. For example, a ring counter can be used to select from multiple RAM blocks. The clock driver of this counter needs to be controlled by the address generation process.

Once the addressing of one block is finished, a clock pulse is sent to the (ring) counter to select the next memory block.

Figure 6-9 illustrates a simple block diagram of an interface block between UJTAG and RAM blocks.

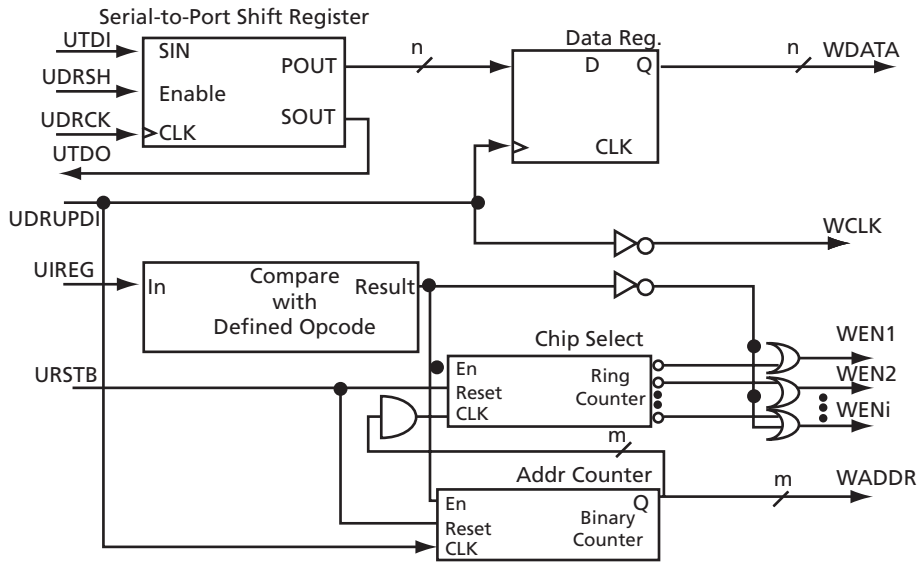


Figure 6-9 • **Block Diagram of a Sample User Interface**

In the circuit shown in Figure 6-9, the shift register is enabled by the UDRSH output of the UJTAG macro. The counters and chip select outputs are controlled by the value of the TAP Instruction Register. The comparison block compares the UIREG value with the "start initialization" opcode value (defined by the user). If the result is true, the counters start to generate addresses and activate the WEN inputs of appropriate RAM blocks.

The UDRUPD output of the UJTAG macro, also shown in Figure 6-9, is used for generating the write clock (WCLK) and synchronizing the data register and address counter with WCLK. UDRUPD is HIGH when the TAP Controller is in the Data Register Update state, which is an indication of completing the loading of one data word. Once the TAP Controller goes into the Data Register Update state, the UDRUPD output of the UJTAG macro goes HIGH. Therefore, the pipeline register and the address counter place the proper data and address on the outputs of the interface block. Meanwhile, WCLK is defined as the inverted UDRUPD. This will provide enough time (equal to the UDRUPD HIGH time) for the data and address to be placed at the proper ports of the RAM block before the rising edge of WCLK. The inverter is not required if the RAM blocks are clocked at the falling edge of the write clock. An example of this is described in the "Example of RAM Initialization" section on page 6-20.

Example of RAM Initialization

This section of the document presents a sample design in which a 4×4 RAM block is being initialized through the JTAG port. A test feature has been implemented in the design to read back the contents of the RAM after initialization to verify the procedure.

The interface block of this example performs two major functions: initialization of the RAM block and running a test procedure to read back the contents. The clock output of the interface is either the write clock (for initialization) or the read clock (for reading back the contents). The Verilog code for the interface block is included in the "Sample Verilog Code" section on page 6-21.

For simulation purposes, users can declare the input ports of the UJTAG macro for easier assignment in the testbench. However, the UJTAG input ports should not be declared on the top level during synthesis. If the input ports of the UJTAG are declared during synthesis, the synthesis tool will instantiate input buffers on these ports. The input buffers on the ports will cause Compile to fail in Designer.

Figure 6-10 shows the simulation results for the initialization step of the example design.

The CLK_OUT signal, which is the clock output of the interface block, is the inverted DR_UPDATE output of the UJTAG macro. It is clear that it gives sufficient time (while the TAP Controller is in the Data Register Update state) for the write address and data to become stable before loading them into the RAM block.

Figure 6-11 presents the test procedure of the example. The data read back from the memory block matches the written data, thus verifying the design functionality.

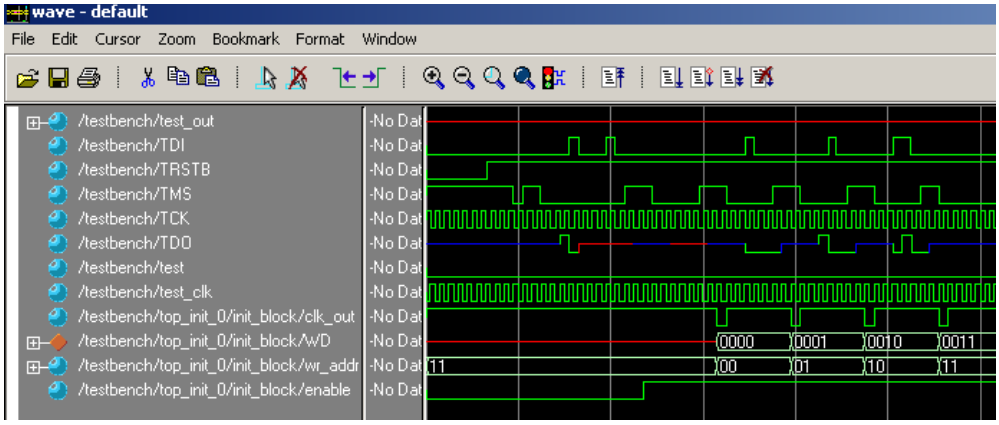


Figure 6-10 • **Simulation of Initialization Step**

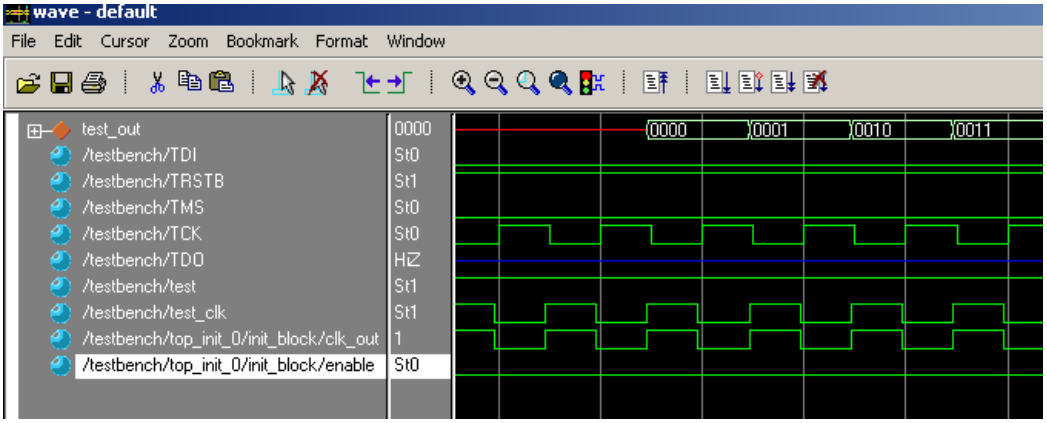


Figure 6-11 • **Simulation of the Test Procedure of the Example**

The ROM emulation application is based on RAM block initialization. If the user's main design has access only to the read ports of the RAM block (RADDR, RD, RCLK, and REN), and the contents of the RAM are already initialized through the TAP, then the memory blocks will emulate ROM functionality for the core design. In this case, the write ports of the RAM blocks are accessed only by the user interface block, and the interface is activated only by the TAP Instruction Register contents.

Users should note that the contents of the RAM blocks are lost in the absence of applied power. However, the 1 kbit of flash memory, FlashROM, in low-power flash devices can be used to retain data after power is removed from the device. Refer to *FlashROM in Actel's Low-Power Flash Devices* for more information.

Sample Verilog Code

Interface Block

```
`define Initialize_start 8'h22 //INITIALIZATION START COMMAND VALUE
`define Initialize_stop 8'h23 //INITIALIZATION START COMMAND VALUE

module interface(IR, rst_n, data_shift, clk_in, data_update, din_ser, dout_ser, test,
  test_out,test_clk,clk_out,wr_en,rd_en,write_word,read_word,rd_addr, wr_addr);

input [7:0] IR;
input [3:0] read_word; //RAM DATA READ BACK
input rst_n, data_shift, clk_in, data_update, din_ser; //INITIALIZATION SIGNALS
input test, test_clk; //TEST PROCEDURE CLOCK AND COMMAND INPUT
output [3:0] test_out; //READ DATA
output [3:0] write_word; //WRITE DATA
output [1:0] rd_addr; //READ ADDRESS
output [1:0] wr_addr; //WRITE ADDRESS
output dout_ser; //TDO DRIVER
output clk_out, wr_en, rd_en;

wire [3:0] write_word;
wire [1:0] rd_addr;
wire [1:0] wr_addr;
wire [3:0] Q_out;
wire enable, test_active;

reg clk_out;

//SELECT CLOCK FOR INITIALIZATION OR READBACK TEST
always @(enable or test_clk or data_update)
begin
  case ({test_active})
    1 : clk_out = test_clk ;
    0 : clk_out = !data_update;
    default : clk_out = 1'b1;
  endcase
end

assign test_active = test && (IR == 8'h23);
assign enable = (IR == 8'h22);
assign wr_en = !enable;
assign rd_en = !test_active;
assign test_out = read_word;
assign dout_ser = Q_out[3];

//4-bit SIN/POUT SHIFT REGISTER
shift_reg data_shift_reg (.Shiften(data_shift), .Shiftin(din_ser), .Clock(clk_in),
  .Q(Q_out));

//4-bit PIPELINE REGISTER
D_pipeline pipeline_reg (.Data(Q_out), .Clock(data_update), .Q(write_word));
```

```
//
addr_counter counter_1 (.Clock(data_update), .Q(wr_addr), .Aset(rst_n),
  .Enable(enable));
addr_counter counter_2 (.Clock(test_clk), .Q(rd_addr), .Aset(rst_n),
  .Enable( test_active));

endmodule
```

Interface Block / UJTAG Wrapper

This example is a sample wrapper, which connects the interface block to the UJTAG and the memory blocks.

```
// WRAPPER
module top_init (TDI, TRSTB, TMS, TCK, TDO, test, test_clk, test_ out);

input TDI, TRSTB, TMS, TCK;
output TDO;
input test, test_clk;
output [3:0] test_out;

wire [7:0] IR;
wire reset, DR_shift, DR_cap, init_clk, DR_update, data_in, data_out;
wire clk_out, wen, ren;
wire [3:0] word_in, word_out;
wire [1:0] write_addr, read_addr;

UJTAG UJTAG_U1 (.UIREG0(IR[0]), .UIREG1(IR[1]), .UIREG2(IR[2]), .UIREG3(IR[3]),
  .UIREG4(IR[4]), .UIREG5(IR[5]), .UIREG6(IR[6]), .UIREG7(IR[7]), .URSTB(reset),
  .UDRSH(DR_shift), .UDRCAP(DR_cap), .UDRCK(init_clk), .UDRUPD(DR_update),
  .UT-DI(data_in), .TDI(TDI), .TMS(TMS), .TCK(TCK), .TRSTB(TRSTB), .TDO(TDO),
  .UT-DO(data_out));
mem_block RAM_block (.DO(word_out), .RCLOCK(clk_out), .WCLOCK(clk_out), .DI(word_in),
  .WRB(wen), .RDB(ren), .WAD-DR(write_addr), .RADDR(read_addr));
interface init_block (.IR(IR), .rst_n(reset), .data_shift(DR_shift), .clk_in(init_clk),
  .data_update(DR_update), .din_ser(data_in), .dout_ser(data_out), .test(test),
  .test_out(test_out), .test_clk(test_clk), .clk_out(clk_out), .wr_en(wen),
  .rd_en(ren), .write_word(word_in), .read_word(word_out), .rd_addr(read_addr),
  .wr_addr(write_addr));

endmodule
```

Address Counter

```
module addr_counter (Clock, Q, Aset, Enable);

input Clock;
output [1:0] Q;
input Aset;
input Enable;

reg [1:0] Qaux;

always @(posedge Clock or negedge Aset)
begin
  if (!Aset) Qaux <= 2'b11;
  else if (Enable) Qaux <= Qaux + 1;
end

assign Q = Qaux;

endmodule
```

Pipeline Register

```
module D_pipeline (Data, Clock, Q);

input [3:0] Data;
input Clock;
output [3:0] Q;

reg [3:0] Q;

always @ (posedge Clock) Q <= Data;

endmodule
```

4x4 RAM Block (created by SmartGen Core Generator)

```
module mem_block(DI,DO,WADDR,RADDR,WRB,RDB,WCLOCK,RCLOCK);

input [3:0] DI;
output [3:0] DO;
input [1:0] WADDR, RADDR;
input WRB, RDB, WCLOCK, RCLOCK;

wire WEBP, WEAP, VCC, GND;

VCC VCC_1_net(.Y(VCC));
GND GND_1_net(.Y(GND));
INV WEBUBBLEB(.A(WRB), .Y(WEBP));
RAM4K9 RAMBLOCK0(.ADDRA11(GND), .ADDRA10(GND), .ADDRA9(GND), .ADDRA8(GND),
  .ADDRA7(GND), .ADDRA6(GND), .ADDRA5(GND), .ADDRA4(GND), .ADDRA3(GND), .ADDRA2(GND),
  .ADDRA1(RADDR[1]), .ADDRA0(RADDR[0]), .ADDRB11(GND), .ADDRB10(GND), .ADDRB9(GND),
  .ADDRB8(GND), .ADDRB7(GND), .ADDRB6(GND), .ADDRB5(GND), .ADDRB4(GND), .ADDRB3(GND),
  .ADDRB2(GND), .ADDRB1(WADDR[1]), .ADDRB0(WADDR[0]), .DINA8(GND), .DINA7(GND),
  .DINA6(GND), .DINA5(GND), .DINA4(GND), .DINA3(GND), .DINA2(GND), .DINA1(GND),
  .DINA0(GND), .DINB8(GND), .DINB7(GND), .DINB6(GND), .DINB5(GND), .DINB4(GND),
  .DINB3(DI[3]), .DINB2(DI[2]), .DINB1(DI[1]), .DINB0(DI[0]), .WIDTHA0(GND),
  .WIDTHA1(VCC), .WIDTHB0(GND), .WIDTHB1(VCC), .PIPEA(GND), .PIPEB(GND),
  .WMODEA(GND), .WMODEB(GND), .BLKA(WEAP), .BLKB(WEBP), .WENA(VCC), .WENB(GND),
  .CLKA(RCLOCK), .CLKB(WCLOCK), .RESET(VCC), .DOUTA8(), .DOUTA7(), .DOUTA6(),
  .DOUTA5(), .DOUTA4(), .DOUTA3(DO[3]), .DOUTA2(DO[2]), .DOUTA1(DO[1]),
  .DOUTA0(DO[0]), .DOUTB8(), .DOUTB7(), .DOUTB6(), .DOUTB5(), .DOUTB4(), .DOUTB3(),
  .DOUTB2(), .DOUTB1(), .DOUTB0());
INV WEBUBBLEA(.A(RDB), .Y(WEAP));

endmodule
```

Software Support

The SmartGen core generator is the easiest way to select and configure the memory blocks (Figure 6-12). SmartGen automatically selects the proper memory block type and aspect ratio, and cascades the memory blocks based on the user's selection. SmartGen also configures any additional signals that may require tie-off.

SmartGen will attempt to use the minimum number of blocks required to implement the desired memory. When cascading, SmartGen will configure the memory for width before configuring for depth. For example, if the user requests a 256×8 FIFO, SmartGen will use a 512×9 FIFO configuration, not 256×18.

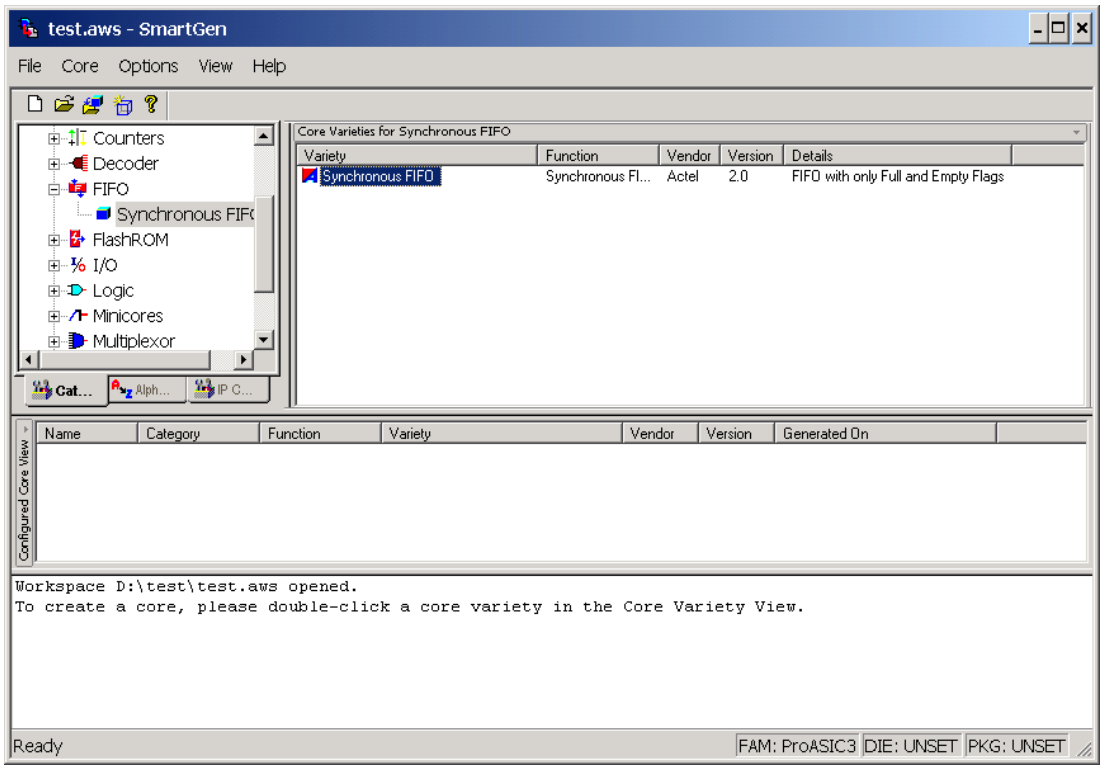


***Figure 6-12* • SmartGen Core Generator Interface**

SmartGen enables the user to configure the desired RAM element to use either a single clock for read and write, or two independent clocks for read and write. The user can select the type of RAM as well as the width/depth and several other parameters (Figure 6-13).

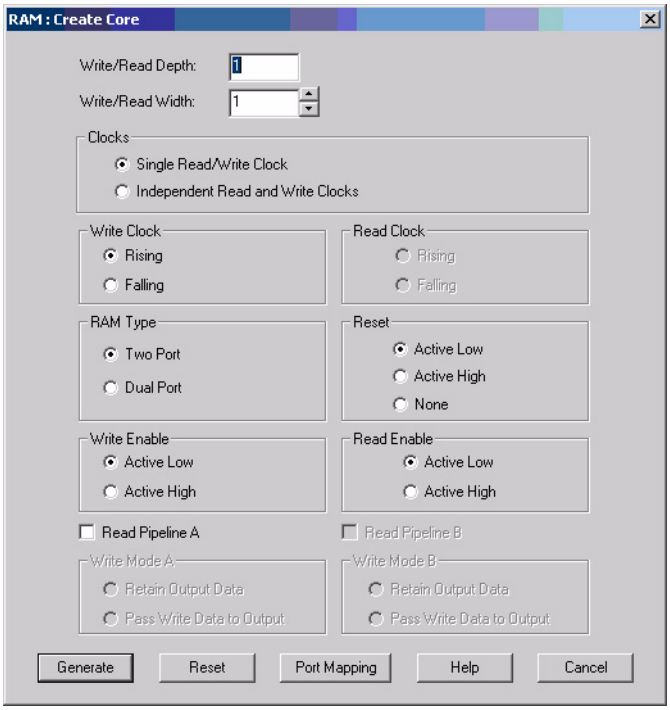


***Figure 6-13* • SmartGen Memory Configuration Interface**

SmartGen also has a Port Mapping option that allows the user to specify the names of the ports generated in the memory block (Figure 6-14).

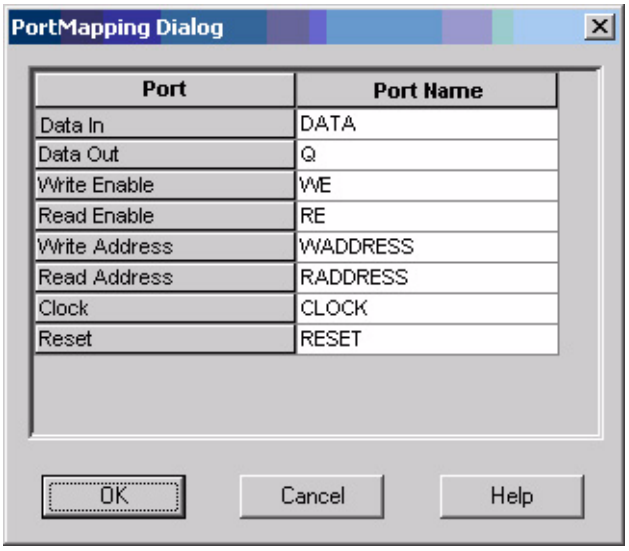


***Figure 6-14* • Port Mapping Interface for SmartGen-Generated Memory**

SmartGen also configures the FIFO according to user specifications. Users can select no flags, static flags, or dynamic flags. Static flag settings are configured using configuration flash and cannot be altered without reprogramming the device. Dynamic flag settings are determined by register values and can be altered without reprogramming the device by reloading the register values either from the design or through the UJTAG interface described in the "Initializing the RAM/FIFO" section on page 6-18.

SmartGen can also configure the FIFO to continue counting after the FIFO is full. In this configuration, the FIFO write counter will wrap after the counter is full and continue to write data. With the FIFO configured to continue to read after the FIFO is empty, the read counter will also wrap and re-read data that was previously read. This mode can be used to continually read back repeating data patterns stored in the FIFO (Figure 6-15).

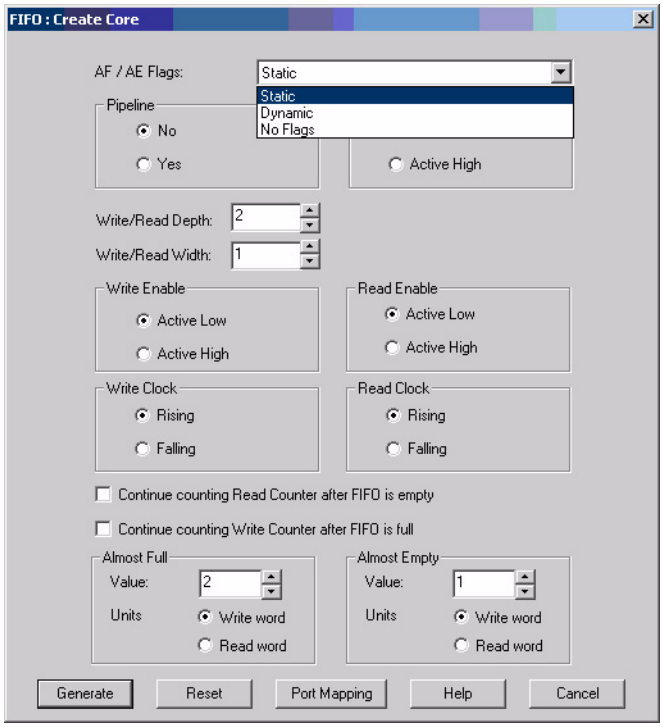


***Figure 6-15* • SmartGen FIFO Configuration Interface**

FIFOs configured using SmartGen can also make use of the port mapping feature to configure the names of the ports.

Limitations

Users should be aware of the following limitations when configuring SRAM blocks for low-power flash devices:

- SmartGen does not track the target device in a family, so it cannot determine if a configured memory block will fit in the target device.
- Dual-port RAMs with different read and write aspect ratios are not supported.
- Cascaded memory blocks can only use a maximum of 64 blocks of RAM.
- The Full flag of the FIFO is sensitive to the maximum depth of the actual physical FIFO block, not the depth requested in the SmartGen interface.

Conclusion

IGLOO, Fusion, and ProASIC3 devices provide users with extremely flexible SRAM blocks for most design needs, with the ability to choose between an easy-to-use dual-port memory or a wide-word two-port memory. Used with the built-in FIFO controllers, these memory blocks also serve as highly efficient FIFOs that do not consume user gates when implemented. The Actel SmartGen core generator provides a fast and easy way to configure these memory elements for use in designs.

Related Documents

Handbook Documents

UJTAG Applications in Actel's Low-Power Flash Devices

www.actel.com/documents/LPD_UJTAG_HBs.pdf

FlashROM in Actel's Low-Power Flash Devices

http://www.actel.com/documents/LPD_FlashROM_HBs.pdf

Part Number and Revision Date

This document contains content extracted from the Device Architecture section of the datasheet, combined with content previously published as an application note describing features and functions of the device. To improve usability for customers, the device architecture information has now been combined with usage information, to reduce duplication and possible inconsistencies in published information. No technical changes were made to the datasheet content unless explicitly listed. Changes to the application note content were made only to be consistent with existing datasheet information.

Part Number 51700094-008-3

Revised August 2008

List of Changes

The following table lists critical changes that were made in the current version of the chapter.

Previous Version	Changes in the Current Version (v1.3)	Page
v1.2 (June 2008)	The note was removed from Figure 6-7 · RAM Block with Embedded FIFO Controller and placed in the "WCLK and RCLK" description.	6-12, 6-13
	The "WCLK and RCLK" description was revised.	6-13
v1.1 (March 2008)	The following changes were made to the family descriptions in Table 6-1 · Low-Power Flash Families: • ProASIC3L was updated to include 1.5 V. • The number of PLLs for ProASIC3E was changed from five to six.	6-4
v1.0 (January 2008)	The "Introduction" section was updated to include the IGLOO PLUS family.	6-1
	The "Device Architecture" section was updated to state that 15 k gate devices do not support SRAM and FIFO.	6-1
	The first note in Figure 6-1 · IGLOO and ProASIC3 Device Architecture Overview was updated to include mention of 15 k gate devices, and IGLOO PLUS was added to the second note.	6-3
	The Table 6-1 · Low-Power Flash Families table and associated text were updated to include the IGLOO PLUS family. The "IGLOO Terminology" section and "ProASIC3 Terminology" section are new.	6-4
	The text introducing Table 6-8 · Memory Availability per IGLOO and ProASIC3 Devices was updated to replace "A3P030 and AGL030" with "15 k and 30 k gate devices. Table 6-8 · Memory Availability per IGLOO and ProASIC3 Devices was updated to remove AGL400 and AGLE1500 and include IGLOO PLUS and ProASIC3L devices.	6-16

I/O Descriptions and Usage

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7 – I/O Structures in IGLOO and ProASIC3 Devices

Introduction

Low-power flash devices feature a flexible I/O structure, supporting a range of mixed voltages (1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V) through bank-selectable voltages. IGLOO,® ProASIC3®L, and ProASIC3 families support Standard, Standard Plus, and Advanced I/Os.

Users designing I/O solutions are faced with a number of implementation decisions and configuration choices that can directly impact the efficiency and effectiveness of their final design. The flexible I/O structure, supporting a wide variety of voltages and I/O standards, enables users to meet the growing challenges of their many diverse applications. The Actel Libero® Integrated Design Environment (IDE) provides an easy way to implement I/Os that will result in robust I/O design.

This document first describes the two different I/O types in terms of the standards and features they support. It then explains the individual features and how to implement them in Actel's Libero IDE.

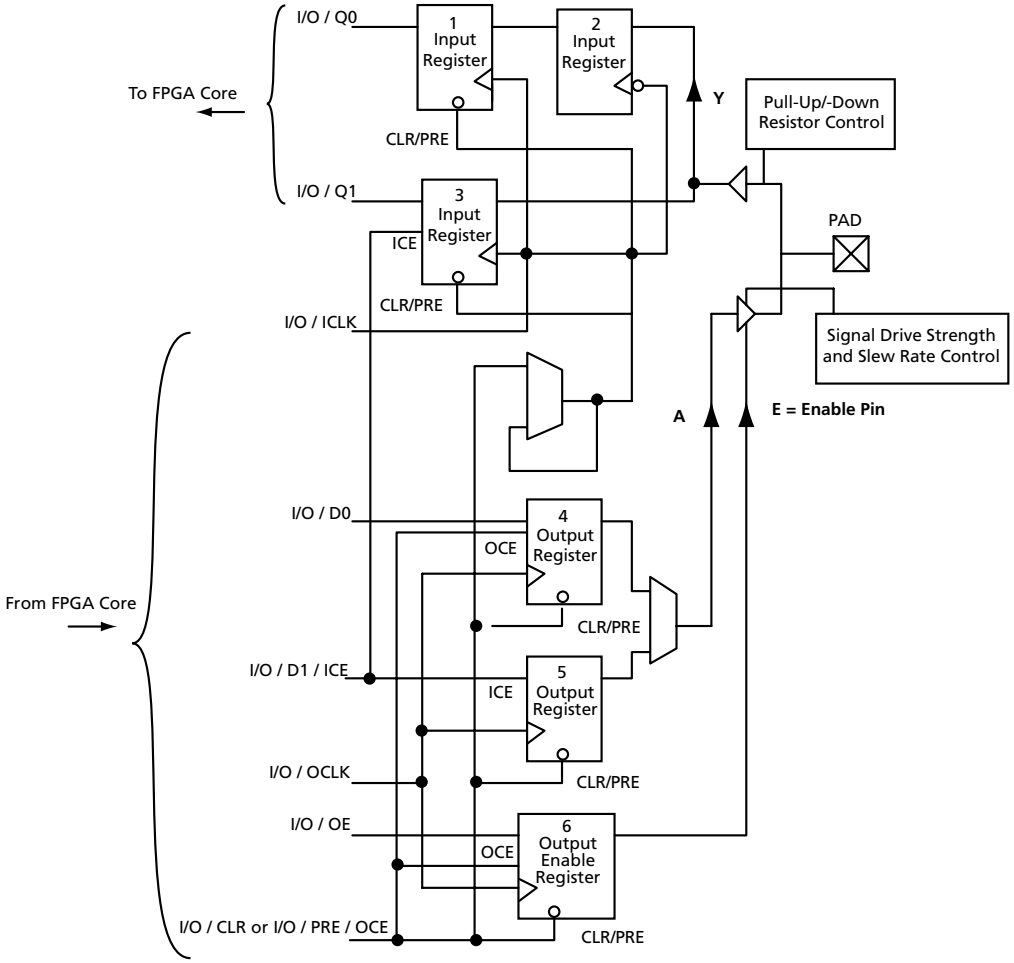


Figure 7-1 • **I/O Block Logical Representation**

Low-Power Flash Device I/O Support

The low-power flash families listed in Table 7-1 support I/Os and the functions described in this document.

Table 7-1 • **Low-Power Flash Families**

Family[1]	Description	Timing Numbers[2]
IGLOO	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*IGLOO DC and Switching Characteristics*
IGLOO PLUS	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology and enhanced I/O capabilities	*IGLOO PLUS DC and Switching Characteristics*
IGLOOe	IGLOO devices enhanced with higher density, five additional PLLs, and additional I/O standards	*IGLOOe DC and Switching Characteristics*
ProASIC3L	Low-power, high-performance 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*ProASIC3L DC and Switching Characteristics*
ProASIC3	Low-power, high-performance 1.5 V FPGAs	*ProASIC3 DC and Switching Characteristics*
ProASIC3E	ProASIC3 enhanced with higher density, six additional PLLs, and additional I/O standards	*ProASIC3E DC and Switching Characteristics*
ProASIC3 Automotive	Low-power, high-performance FPGAs qualified for automotive applications	*Automotive ProASIC3 DC and Switching Characteristics*

Notes:

1. *The family names are linked to the appropriate product brief.*
2. *The timing number links go to the relevant timing numbers in the datasheet.*

Actel's low-power flash devices (listed in Table 7-1) provide a selection of low-power, secure, live-at-power-up, single-chip solutions. The nonvolatile flash-based devices do not require a boot PROM and incorporate FlashLock® technology, which provides a unique combination of reprogrammability and design security without external overhead. Only low-power flash FPGAs can offer these advantages.

Actel IGLOO PLUS FPGAs are the industry-leading 1.2 V ultra-low-power programmable logic devices (PLDs) and consume 90% less static power and over 50% less dynamic power than PLD alternatives, while ProASIC3L devices offer a balance of low power and higher performance.

Flash*Freeze technology used in IGLOO, IGLOO PLUS, and ProASIC3L devices enables easy entry to and exit from the ultra-low power mode, which consumes as little as 5 µW, while retaining SRAM and register data. IGLOO PLUS also offers the ability to hold I/O state in Flash*Freeze mode. Flash*Freeze technology simplifies power management through I/O and clock management without the need to turn off voltages, I/Os, or clocks at the system level. Entering and exiting Flash*Freeze mode takes less than 1 µs.

IGLOO Terminology

In documentation, the term IGLOO families or IGLOO devices refers to all IGLOO families as listed in Table 7-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

ProASIC3 Terminology

In documentation, the term ProASIC3 families or ProASIC3 devices refers to all ProASIC3 families as listed in Table 7-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

Advanced I/Os—IGLOO, ProASIC3L, and ProASIC3

Table 7-2 and Table 7-3 show the voltages and compatible I/O standards for IGLOO, ProASIC3L, and ProASIC3 families.

I/Os provide programmable slew rates (except 30 k gate devices), drive strengths, and weak pull-up and pull-down circuits. 3.3 V PCI and 3.3 V PCI-X are 5 V–tolerant. See the "5 V Input Tolerance" section on page 7-20 for possible implementations of 5 V tolerance.

All I/Os are in a known state during power-up, and any power-up sequence is allowed without current impact. Refer to the "I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)" section in the datasheet for more information. During power-up, before reaching activation levels, the I/O input and output buffers are disabled while the weak pull-up is enabled. Activation levels are described in the datasheet.

Table 7-2 • **Supported I/O Standards**

IGLOO	**AGL030**	**AGL060**	**AGL125**	**AGL250**		**AGL600**	**AGL1000**
ProASIC3	**A3P030**	**A3P060**	**A3P125**	**A3P250/ A3P250L**	**A3P400**	**A3P600/ A3P600L**	**A3P1000/ A3P1000L**
Single-Ended							
LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V / 1.8 V / 1.5 V, LVCMOS 2.5/5.0 V	✓	✓	✓	✓	✓	✓	✓
3.3 V PCI/PCI-X	–	✓	✓	✓	✓	✓	✓
Differential							
LVPECL, LVDS, BLVDS, M-LVDS	–	–	–	✓	✓	✓	✓

I/O Banks and I/O Standards Compatibility

I/Os are grouped into I/O voltage banks.

Each I/O voltage bank has dedicated I/O supply and ground voltages (VMV/GNDQ for input buffers and V_{CCI}/GND for output buffers). This isolation is necessary to minimize simultaneous switching noise from the input and output (SSI and SSO). The switching noise (ground bounce and power bounce) is generated by the output buffers and transferred into input buffer circuits, and vice versa. Because of these dedicated supplies, only I/Os with compatible standards can be assigned to the same I/O voltage bank. Table 7-3 shows the required voltage compatibility values for each of these voltages.

There are four I/O banks on the 250 k gate through 1 M gate devices.

There are two I/O banks on the 30 k, 60 k, and 125 k gate devices.

I/O standards are compatible if their V_{CCI} and VMV values are identical. VMV and GNDQ are "quiet" input power supply pins and are not used on 30 k gate devices (Table 7-3).

Table 7-3 • **V_{CCI} Voltages and Compatible IGLOO and ProASIC3 Standards**

V_{CCI} and VMV (typical)	**Compatible Standards**
3.3 V	LVTTL/LVCMOS 3.3, PCI 3.3, PCI-X 3.3 LVPECL
2.5 V	LVCMOS 2.5, LVCMOS 2.5/5.0, LVDS, BLVDS, M-LVDS
1.8 V	LVCMOS 1.8
1.5 V	LVCMOS 1.5

I/O Banks

Advanced I/Os are divided into multiple technology banks. Each device has two to four banks, and the number of banks is device-dependent as described above. The bank types have different characteristics, such as drive strength, the I/O standards supported, and timing and power differences.

There are three types of banks: Advanced I/O banks, Standard Plus I/O banks, and Standard I/O banks.

Advanced I/O banks offer single-ended and differential capabilities. These banks are available on the east and west sides of 250 k, 400 k, 600 k and 1 M gate devices.

Standard Plus I/O banks offer LVTTL/LVCMOS and PCI single-ended I/O standards. These banks are available on the north and south sides of 250 k, 400 k, 600 k, and 1 M gate devices as well as all sides of 125 k and 60 k devices.

Standard I/O banks offer LVTTL/LVCMOS single-ended I/O standards. These banks are available on all sides of 30 k gate devices.

Table 7-5 shows the I/O bank types, devices and bank locations supported, drive strength, slew rate control, and supported standards.

Orphan—All inputs and disabled outputs are voltage-tolerant up to 3.3 V.

For more information about I/O and global assignments to I/O banks in a device, refer to the specific pin table for the device in the packaging section of the datasheet and the "User I/O Naming Convention" section on page 7-32.

Table 7-4 • **IGLOO and ProASIC3 Bank Type Definitions and Differences**

I/O Bank Type	Device and Bank Location	Drive Strength	I/O Standards Supported		
			LVTTL/ LVCMOS	PCI/PCI-X	LVPECL, LVDS, BLVDS, M-LVDS
Standard	30 k gate devices (all banks)	Refer to Table 7-14 on page 7-29	✓	Not Supported	Not Supported
Standard Plus	60 k and 125 k gate devices (all banks)	Refer to Table 7-15 on page 7-29	✓	✓	Not Supported
	North and south banks of 250 k and 1 M gate devices	Refer to Table 7-15 on page 7-29	✓	✓	Not Supported
Advanced	East and west banks of 250 k and 1 M gate devices	Refer to Table 7-16 on page 7-30	✓	✓	✓

Features Supported on Every I/O

Table 7-5 lists all features supported by transmitter/receiver for single-ended and differential I/Os. Table 7-6 on page 7-6 lists the performance of each IO technology.

Table 7-5 • **I/O Features**

Feature	Description
All I/O	• High performance (Table 7-6 on page 7-6) • Electrostatic discharge (ESD) protection • I/O register combining option
Single-Ended Transmitter Features	• Hot-swap: – 30 k gate devices: hot-swap in every mode – All other IGLOO and ProASIC3 devices: no hot-swap • Output slew rate: 2 slew rates (except 30 k gate devices) • Weak pull-up and pull-down resistors • Output drive: 3 drive strengths • Programmable output loading • Skew between output buffer enable/disable time: 2 ns delay on rising edge and 0 ns delay on falling edge (see the "Selectable Skew between Output Buffer Enable and Disable Times" section on page 7-25 for more information) • LVTTL/LVCMOS 3.3 V outputs compatible with 5 V TTL inputs
Single-Ended Receiver Features	• 5 V–input–tolerant receiver (Table 7-12 on page 7-19) • Separate ground plane for GNDQ pin and power plane for VMV pin are used for input buffer to reduce output-induced noise.
Differential Receiver Features—250 k through 1 M Gate Devices	• Separate ground plane for GNDQ pin and power plane for VMV pin are used for input buffer to reduce output-induced noise.
CMOS-Style LVDS, BLVDS, M-LVDS, or LVPECL Transmitter	• Two I/Os and external resistors are used to provide a CMOS-style LVDS, DDR LVDS, BLVDS, and M-LVDS/LVPECL transmitter solution. • High slew rate • Weak pull-up and pull-down resistors • Programmable output loading

Table 7-6 • **Maximum I/O Frequency for Single-Ended and Differential I/Os in All Banks in IGLOO and ProASIC Devices (maximum drive strength and high slew selected)**

Specification	Maximum Performance		
	ProASIC3	IGLOO V2 or V5 Devices, 1.5 V DC Core Supply Voltage	IGLOO V2, 1.2 V DC Core Supply Voltage
LVTTL/LVCMOS 3.3 V	200 MHz	180 MHz	TBD
LVCMOS 2.5 V	250 MHz	230 MHz	TBD
LVCMOS 1.8 V	200 MHz	180 MHz	TBD
LVCMOS 1.5 V	130 MHz	120 MHz	TBD
PCI	200 MHz	180 MHz	TBD
PCI-X	200 MHz	180 MHz	TBD
LVDS	350 MHz	300 MHz	TBD
LVPECL	350 MHz	300 MHz	TBD

I/O Architecture

I/O Tile

The I/O tile provides a flexible, programmable structure for implementing a large number of I/O standards. In addition, the registers available in the I/O tile can be used to support high-performance register inputs and outputs, with register enable if desired (Figure 7-2). The registers can also be used to support the JESD-79C Double Data Rate (DDR) standard within the I/O structure (see *DDR for Actel's Low-Power Flash Devices* for more information). In addition, the registers available in the I/O tile can be used to support high-performance register inputs and outputs, with register enable if desired (Figure 7-2).

As depicted in Figure 7-2, all I/O registers share one CLR port. The output register and output enable register share one CLK port.

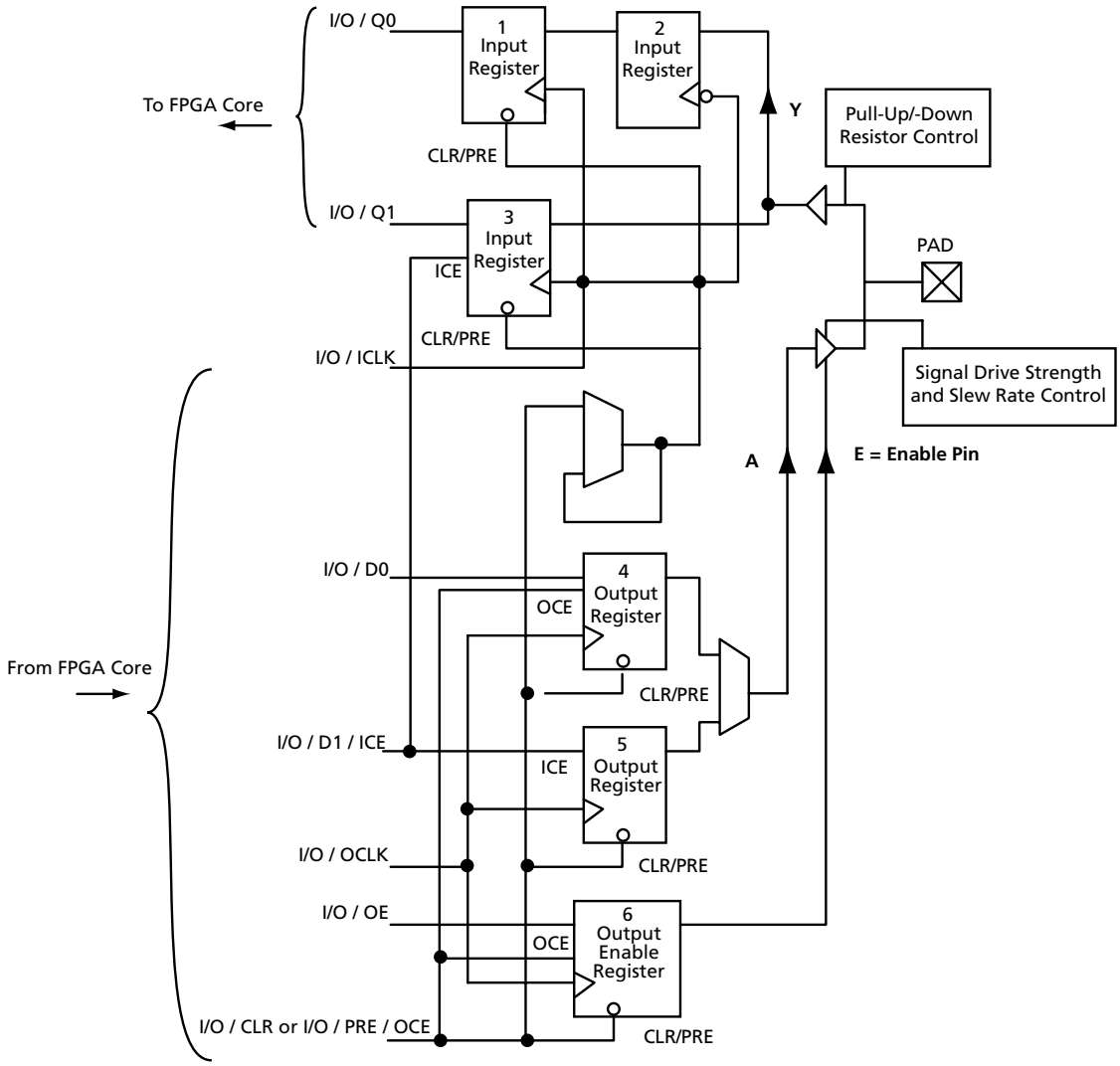


Figure 7-2 • **I/O Block Logical Representation**

I/O Bank Structure

Low-power flash device I/Os are divided into multiple technology banks. The number of banks is device-dependent. The IGLOOe, ProASIC3EL, and ProASIC3E devices have eight banks (two per side); and IGLOO, ProASIC3L, and ProASIC3 devices have two to four banks. Each bank has its own V_{CCI} power supply pin. Multiple I/O standards can co-exist within a single I/O bank.

In IGLOOe, ProASIC3EL, and ProASIC3E devices, each I/O bank is subdivided into V_{REF} minibanks. These are used by voltage-referenced I/Os. V_{REF} minibanks contain 8 to 18 I/Os. All I/Os in a given minibank share a common V_{REF} line (only one V_{REF} pin is needed per V_{REF} minibank). Therefore, if an I/O in a V_{REF} minibank is configured as a V_{REF} pin, the remaining I/Os in that minibank will be able to use the voltage assigned to that pin. If the location of the V_{REF} pin is selected manually in the software, the user must satisfy V_{REF} rules (refer to the *I/O Software Control in Low-Power Flash Devices*). If the user does not pick the V_{REF} pin manually, the software automatically assigns the V_{REF} pin.

Figure 7-3 is a snapshot of a section of the I/O ring, showing the basic elements of an I/O tile, as viewed from the Designer place-and-route tool's MultiView Navigator (MVN).

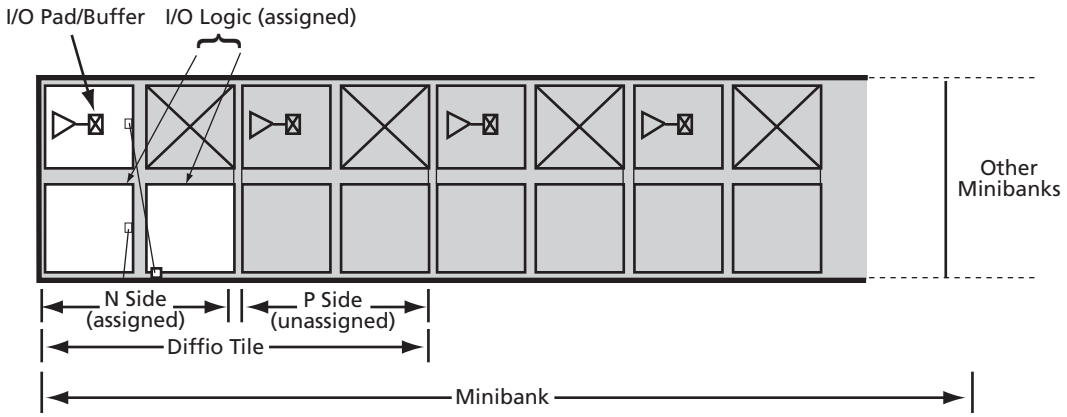


Figure 7-3 • **Snapshot of an I/O Tile**

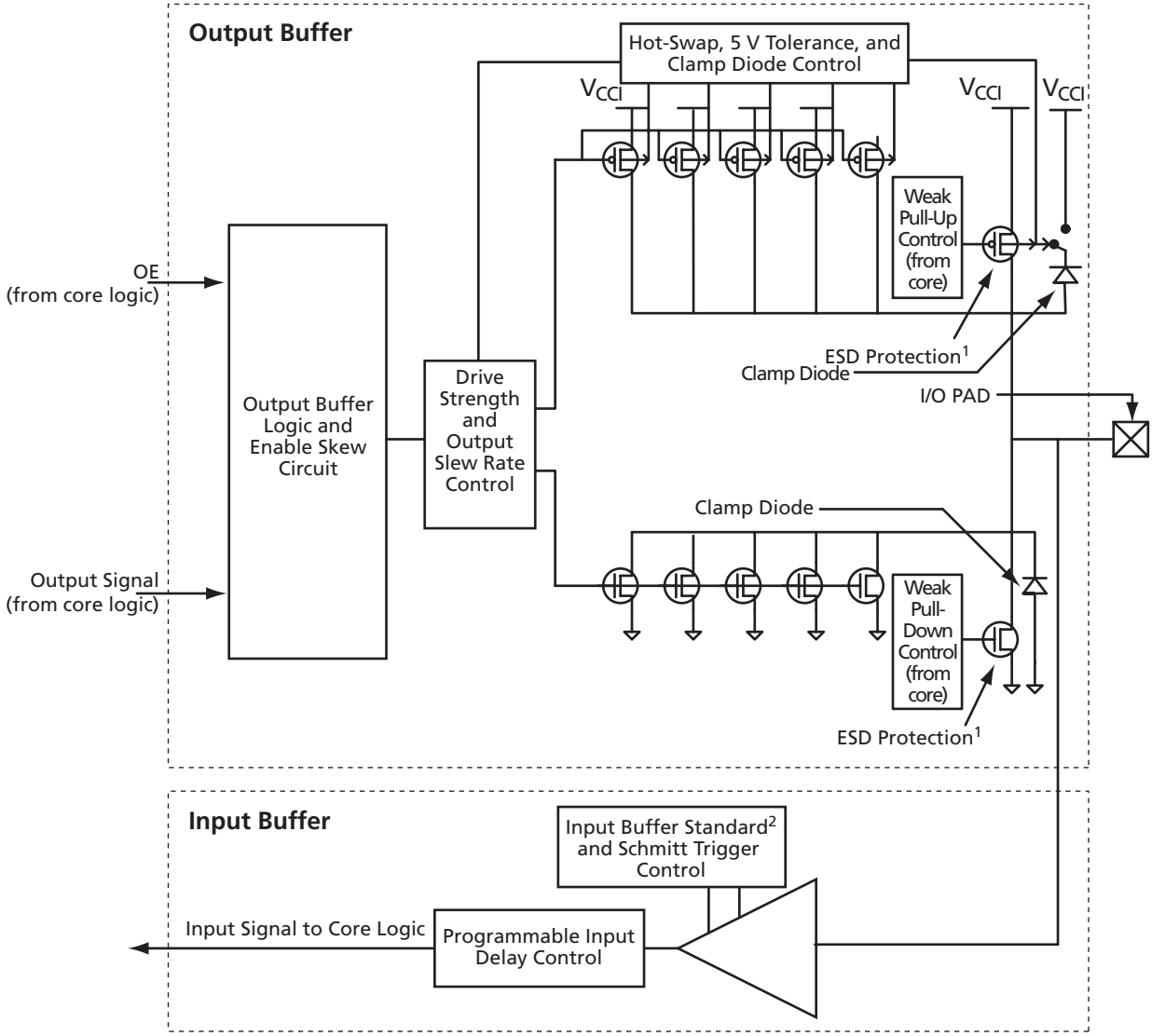
Low-power flash device I/Os are implemented using two tile types: I/O and differential I/O (diffio).

The diffio tile is built up using two I/O tiles, which form an I/O pair (P side and N side). These I/O pairs are used according to differential I/O standards. Both the P and N sides of the diffio tile include an I/O buffer and two I/O logic blocks (auxiliary and main logic).

Every minibank (E devices only) is built up from multiple diffio tiles. The number of the minibank depends on the different-size dies. Refer to the "I/O Architecture" section on page 7-7 for an illustration of the minibank structure.

Figure 7-4 on page 7-9 shows a simplified diagram of the I/O buffer circuitry. The Output Enable signal (OE) enables the output buffer to pass the signal from the core logic to the pin. The output buffer contains ESD protection circuitry, an n-channel transistor that shunts all ESD surges (up to the limit of the device ESD specification) to GND. This transistor also serves as an output pull-down resistor.

Each output buffer also contains programmable slew rate, drive strength, programmable power-up state (pull-up/-down resistor), hot-swap, 5 V tolerance, and clamp diode control circuitry. Multiple flash switches (not shown in Figure 7-4 on page 7-9) are programmed by user selections in the software to activate different I/O features.



Notes:

1. *All NMOS transistors connected to the I/O pad serve as ESD protection.*
2. *See Table 7-2 on page 7-3 for available I/O standards.*

Figure 7-4 • **Simplified I/O Buffer Circuitry**

I/O Registers

Each I/O module contains several input, output, and enable registers. Refer to Figure 7-4 for a simplified representation of the I/O block. The number of input registers is selected by a set of switches (not shown in Figure 7-2 on page 7-7) between registers to implement single-ended or differential data transmission to and from the FPGA core. The Designer software sets these switches for the user. A common CLR/PRE signal is employed by all I/O registers when I/O register combining is used. Input Register 2 does not have a CLR/PRE pin, as this register is used for DDR implementation. The I/O register combining must satisfy certain rules.

I/O Standards

Single-Ended Standards

These I/O standards use a push-pull CMOS output stage with a voltage referenced to system ground to designate logical states. The input buffer configuration, output drive, and I/O supply voltage (V_{CCI}) vary among the I/O standards (Figure 7-5).

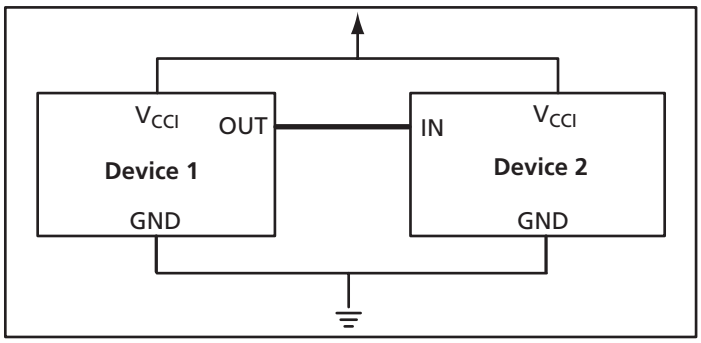


Figure 7-5 • **Single-Ended I/O Standard Topology**

The advantage of these standards is that a common ground can be used for multiple I/Os. This simplifies board layout and reduces system cost. Their low-edge-rate (*dv*/*dt*) data transmission causes less electromagnetic interference (EMI) on the board. However, they are not suitable for high-frequency (>200 MHz) switching due to noise impact and higher power consumption.

LVTTL (Low-Voltage TTL)

This is a general-purpose standard (EIA/JESD8-B) for 3.3 V applications. It uses an LVTTL input buffer and a push-pull output buffer. The LVTTL output buffer can have up to six different programmable drive strengths. The default drive strength is 12 mA. V_{CCI} is 3.3 V. Refer to "I/O Programmable Features" on page 7-14 for details.

LVCMOS (Low-Voltage CMOS)

The low-power flash devices provide four different kinds of LVCMOS: LVCMOS 3.3 V, LVCMOS 2.5 V, LVCMOS 1.8 V, and LVCMOS 1.5 V. LVCMOS 3.3 V is an extension of the LVCMOS standard (JESD8-B–compliant) used for general-purpose 3.3 V applications. LVCMOS 2.5 V is an extension of the LVCMOS standard (JESD8-5–compliant) used for general-purpose 2.5 V applications. LVCMOS 2.5 V for the 30 k gate devices has a clamp diode to V_{CCI}, but for all other devices there is no clamp diode.

There is yet another standard supported by IGLOO and ProASIC3 devices (except A3P030): LVCMOS 2.5/5.0 V. This standard is similar to LVCMOS 2.5 V, with the exception that it can support up to 3.3 V on the input side (2.5 V output drive). LVCMOS 1.8 V is an extension of the LVCMOS standard (JESD8-7–compliant) used for general-purpose 1.8 V applications. LVCMOS 1.5 V is an extension of the LVCMOS standard (JESD8-11–compliant) used for general-purpose 1.5 V applications. The V_{CCI} values for these standards are 3.3 V, 2.5 V, 1.8 V, and 1.5 V, respectively. All these versions use a 3.3 V–tolerant CMOS input buffer and a push-pull output buffer. Like LVTTL, the output buffer has up to seven different programmable drive strengths (2, 4, 6, 8, 12, 16, and 24 mA). Refer to "I/O Programmable Features" on page 7-14 for details.

3.3 V PCI (Peripheral Component Interface)

This standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses an LVTTL input buffer and a push-pull output buffer. With the aid of an external resistor, this I/O standard can be 5 V–compliant for low-power flash devices. It does not have programmable drive strength.

3.3 V PCI-X (Peripheral Component Interface Extended)

An enhanced version of the PCI specification, 3.3 V PCI-X can support higher average bandwidths; it increases the speed that data can move within a computer from 66 MHz to 133 MHz. It is backward-compatible, which means devices can operate at conventional PCI frequencies (33 MHz and 66 MHz). PCI-X is more fault-tolerant than PCI. It also does not have programmable drive strength.

Voltage-Referenced Standards

I/Os using these standards are referenced to an external reference voltage (V_{REF}) and are supported on E devices only.

HSTL Class I and II (High-Speed Transceiver Logic)

These are general-purpose, high-speed 1.5 V bus standards (EIA/JESD 8-6) for signaling between integrated circuits. The signaling range is 0 V to 1.5 V, and signals can be either single-ended or differential. HSTL requires a differential amplifier input buffer and a push-pull output buffer. The reference voltage (V_{REF}) is 0.75 V. These standards are used in the memory bus interface with data switching capability of up to 400 MHz. The other advantages of these standards are low power and fewer EMI concerns.

HSTL has four classes, of which low-power flash devices support Class I and II. These classes are defined by standard EIA/JESD 8-6 from the Electronic Industries Alliance (EIA):

- Class I – Unterminated or symmetrically parallel-terminated
- Class II – Series-terminated
- Class III – Asymmetrically parallel-terminated
- Class IV – Asymmetrically double-parallel-terminated

SSTL2 Class I and II (Stub Series Terminated Logic 2.5 V)

These are general-purpose 2.5 V memory bus standards (JESD 8-9) for driving transmission lines, designed specifically for driving the DDR SDRAM modules used in computer memory. SSTL2 requires a differential amplifier input buffer and a push-pull output buffer. The reference voltage (V_{REF}) is 1.25 V.

SSTL3 Class I and II (Stub Series Terminated Logic 3.3 V)

These are general-purpose 3.3 V memory bus standards (JESD 8-8) for driving transmission lines. SSTL3 requires a differential amplifier input buffer and a push-pull output buffer. The reference voltage (V_{REF}) is 1.5 V.

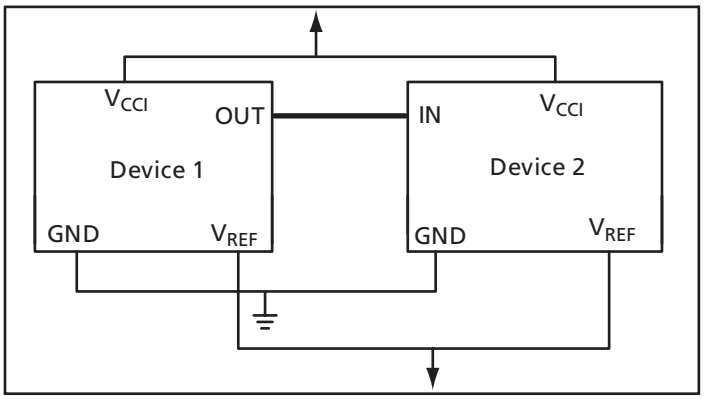


Figure 7-6 • **SSTL and HSTL Topology**

GTL 2.5 V (Gunning Transceiver Logic 2.5 V)

This is a low-power standard (JESD 8.3) for electrical signals used in CMOS circuits that allows for low electromagnetic interference at high transfer speeds. It has a voltage swing between 0.4 V and 1.2 V and typically operates at speeds of between 20 and 40 MHz. V_{CCI} must be connected to 2.5 V. The reference voltage (V_{REF}) is 0.8 V.

GTL 3.3 V (Gunning Transceiver Logic 3.3 V)

This is the same as GTL 2.5 V above, except V_{CCI} must be connected to 3.3 V.

GTL+ (Gunning Transceiver Logic Plus)

This is an enhanced version of GTL that has defined slew rates and higher voltage levels. It requires a differential amplifier input buffer and an open-drain output buffer. Even though the output is open-drain, V_{CCI} must be connected to either 2.5 V or 3.3 V. The reference voltage (V_{REF}) is 1 V.

Differential Standards

These standards require two I/Os per signal (called a “signal pair”). Logic values are determined by the potential difference between the lines, not with respect to ground. This is why differential drivers and receivers have much better noise immunity than single-ended standards. The differential interface standards offer higher performance and lower power consumption than their single-ended counterparts. Two I/O pins are used for each data transfer channel. Both differential standards require resistor termination.

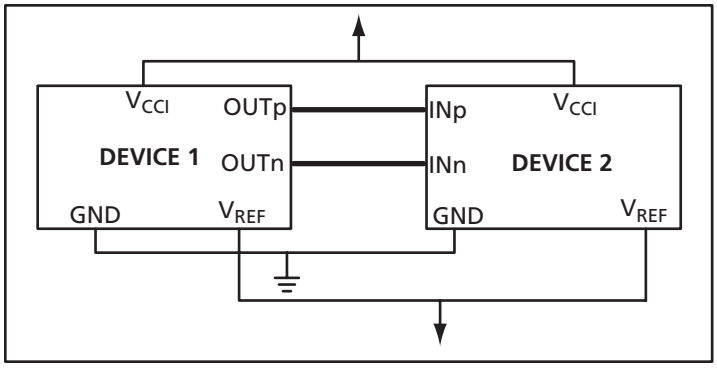


Figure 7-7 • **Differential Topology**

LVPECL (Low-Voltage Positive Emitter Coupled Logic)

LVPECL requires that one data bit be carried through two signal lines; therefore, two pins are needed per input or output. It also requires external resistor termination. The voltage swing between the two signal lines is approximately 850 mV. When the power supply is +3.3 V, it is commonly referred to as Low-Voltage PECL (LVPECL). Refer to the device datasheet for the full implementation of the LVPECL transmitter and receiver.

LVDS (Low-Voltage Differential Signal)

LVDS is a moderate-speed differential signaling system, in which the transmitter generates two different voltages that are compared at the receiver. LVDS uses a differential driver connected to a terminated receiver through a constant-impedance transmission line. It requires that one data bit be carried through two signal lines; therefore, the user will need two pins per input or output. It also requires external resistor termination. The voltage swing between the two signal lines is approximately 350 mV. V_{CCI} is 2.5 V. Low-power flash devices contain dedicated circuitry supporting a high-speed LVDS standard that has its own user specification. Refer to the device datasheet for the full implementation of the LVDS transmitter and receiver.

BLVDS/M-LVDS

Bus LVDS (BLVDS) refers to bus interface circuits based on LVDS technology. Multipoint LVDS (M-LVDS) specifications extend the LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Actel LVDS drivers provide the higher drive current required by BLVDS and M-LVDS to accommodate the loading. The driver requires series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus, since the driver can be located anywhere on the bus. These configurations can be implemented using TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Actel LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 7-8 on page 7-13. The input and output buffer delays are available in the LVDS sections in the datasheet.

Example: For a bus consisting of 20 equidistant loads, the terminations given in EQ 7-1 provide the required differential voltage, in worst-case industrial operating conditions, at the farthest receiver:

$R_S = 60\ \Omega$, $R_T = 70\ \Omega$, given $Z_O = 50\ \Omega$ (2") and a $Z_{stub} = 50\ \Omega$ (~1.5").

EQ 7-1

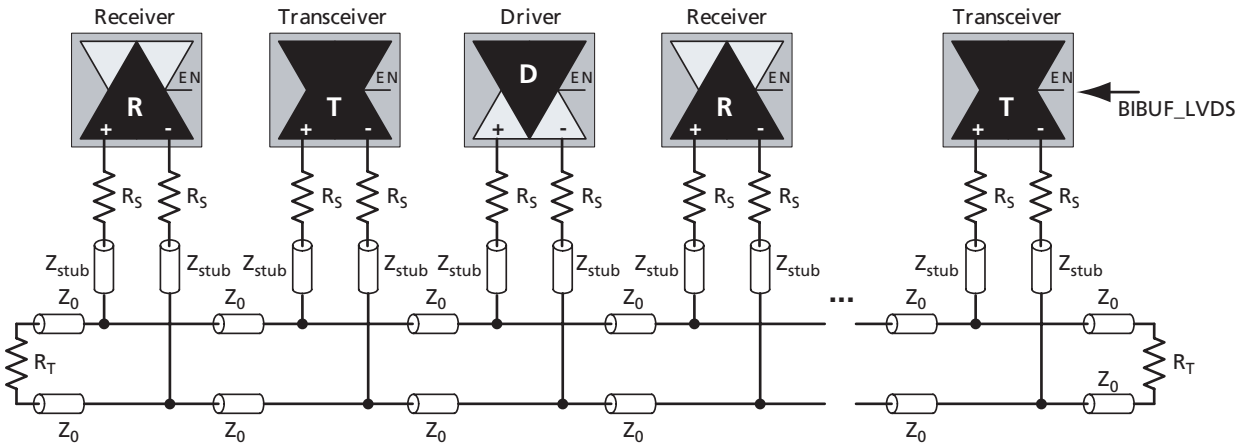


Figure 7-8 • **A BLVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers**

I/O Features

Low-power flash devices support multiple I/O features that make board design easier. For example, an I/O feature like Schmitt Trigger in the ProASIC3E input buffer saves the board space that would be used by an external Schmitt trigger for a slow or noisy input signal. These features are also programmable for each I/O, which in turn gives flexibility in interfacing with other components. The following is a detailed description of all available features in low-power flash devices.

I/O Programmable Features

Low-power flash devices offer many flexible I/O features to support a wide variety of board designs. Some of the features are programmable, with a range for selection. Table 7-7 lists programmable I/O features and their ranges.

Table 7-7 • **Programmable I/O Features (user control via I/O Attribute Editor)**

Feature	Description	Range
Slew Control	Output slew rate	HIGH, LOW
Output Drive (mA)	Output drive strength	2, 4, 6, 8, 12, 16, 24
Skew Control	Output tristate enable Delay option	ON, OFF
Resistor Pull	Resistor pull circuit	Up, Down, None
Input Delay	Input delay	OFF, 0–7
Schmitt Trigger	Schmitt trigger for input only	ON, OFF

Note: Limitations of these features with respect to different devices are discussed in later sections.

Hot-Swap Support

A pull-up clamp diode must not be present in the I/O circuitry if the hot-swap feature is used. The 3.3 V PCI standard requires a pull-up clamp diode on the I/O, so it cannot be selected if hot-swap capability is required. The A3P030 device does not support 3.3 V PCI, so it is the only device in the ProASIC3 family that supports the hot-swap feature. All devices in the ProASIC3E family are hot-swappable. All standards except LVCMOS 2.5/5.0 V and 3.3 V PCI/PCI-X support the hot-swap feature.

The hot-swap feature appears as a read-only check box in the I/O Attribute Editor that shows whether an I/O is hot-swappable or not. Refer to *Power-Up/-Down Behavior of Low-Power Flash Devices* for details on hot-swapping.

Hot-swapping (also called hot-plugging) is the operation of hot insertion or hot removal of a card in a powered-up system. The levels of hot-swap support and examples of related applications are described in Table 7-8 on page 7-15 to Table 7-11 on page 7-16. The I/Os also need to be configured in hot-insertion mode if hot-plugging compliance is required. The AGL030 and A3P030 devices have an I/O structure that allows the support of Level 3 and Level 4 hot-swap with only two levels of staging.

Table 7-8 • **Hot-Swap Level 1**

Description	Cold-swap
Power Applied to Device	No
Bus State	–
Card Ground Connection	–
Device Circuitry Connected to Bus Pins	–
Example Application	System and card with Actel FPGA chip are powered down, and the card is plugged into the system. Then the power supplies are turned on for the system but not for the FPGA on the card.
Compliance of IGLOO and ProASIC3 Devices	30 k gate devices: Compliant Other IGLOO/ProASIC3 devices: Compliant if bus switch used to isolate FPGA I/Os from rest of system IGLOOe/ProASIC3E devices: Compliant I/Os can but do not have to be set to hot-insertion mode.

Table 7-9 • **Hot-Swap Level 2**

Description	Hot-swap while reset
Power Applied to Device	Yes
Bus State	Held in reset state
Card Ground Connection	Reset must be maintained for 1 ms before, during, and after insertion/removal.
Device Circuitry Connected to Bus Pins	–
Example Application	In the PCI hot-plug specification, reset control circuitry isolates the card busses until the card supplies are at their nominal operating levels and stable.
Compliance of IGLOO and ProASIC3 Devices	30 k gate devices, all IGLOOe/ProASIC3E devices: Compliant I/Os can but do not have to be set to hot-insertion mode. Other IGLOO/ProASIC3 devices: Compliant

Table 7-10 • **Hot-Swap Level 3**

Description	Hot-swap while bus idle
Power Applied to Device	Yes
Bus State	Held idle (no ongoing I/O processes during insertion/removal)
Card Ground Connection	Reset must be maintained for 1 ms before, during, and after insertion/removal.
Device Circuitry Connected to Bus Pins	Must remain glitch-free during power-up or power-down
Example Application	Board bus shared with card bus is "frozen," and there is no toggling activity on the bus. It is critical that the logic states set on the bus signal not be disturbed during card insertion/removal.
Compliance of IGLOO and ProASIC3 Devices	30 k gate devices, all IGLOOe/ProASIC3E devices: Compliant with two levels of staging (first: GND; second: all other pins) Other IGLOO/ProASIC3 devices: Compliant: Option A – Two levels of staging (first: GND; second: all other pins) together with bus switch on the I/Os Option B – Three levels of staging (first: GND; second: supplies; third: all other pins)

Table 7-11 • **Hot-Swap Level 4**

Description	Hot-swap on an active bus
Power Applied to Device	Yes
Bus State	Bus may have active I/O processes ongoing, but device being inserted or removed must be idle.
Card Ground Connection	Reset must be maintained for 1 ms before, during, and after insertion/removal.
Device Circuitry Connected to Bus Pins	Must remain glitch-free during power-up or power-down
Example Application	There is activity on the system bus, and it is critical that the logic states set on the bus signal not be disturbed during card insertion/removal.
Compliance of IGLOO and ProASIC3 Devices	30 k gate devices, all IGLOOe/ProASIC3E devices: Compliant with two levels of staging (first: GND; second: all other pins) Other IGLOO/ProASIC3 devices: Compliant: Option A – Two levels of staging (first: GND; second: all other pins) together with bus switch on the I/Os Option B – Three levels of staging (first: GND; second: supplies; third: all other pins)

IGLOO and ProASIC3

For boards and cards with three levels of staging, card power supplies must have time to reach their final values before the I/Os are connected. Pay attention to the sizing of power supply decoupling capacitors on the card to ensure that the power supplies are not overloaded with capacitance.

Cards with three levels of staging should have the following sequence:

- Grounds
- Powers
- I/Os and other pins

For Level 3 and Level 4 compliance with the 30 k gate device, cards with two levels of staging should have the following sequence:

- Grounds
- Powers, I/Os, and other pins

Cold-Sparing Support

Cold-sparing refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

The resistor value is calculated based on the decoupling capacitance on a given power supply. The RC constant should be greater than 3 µs.

To remove resistor current during operation, it is suggested that the resistor be disconnected (e.g., with an NMOS switch) from the power supply after the supply has reached its final value. Refer to the *Power-Upl-Down Behavior of Low-Power Flash Devices* chapter of the *ProASIC3* and *ProASIC3E* handbooks for details on cold-sparing.

Cold-sparing means that a subsystem with no power applied (usually a circuit board) is electrically connected to the system that is in operation. This means that all input buffers of the subsystem must present very high input impedance with no power applied so as not to disturb the operating portion of the system.

The 30 k gate devices fully support cold-sparing, since the I/O clamp diode is always off (see Table 7-12 on page 7-19). If the 30 k gate device is used in applications requiring cold-sparing, a discharge path from the power supply to ground should be provided. This can be done with a discharge resistor or a switched resistor. This is necessary because the 30 k gate devices do not have built-in I/O clamp diodes.

For other IGLOO and ProASIC3 devices, since the I/O clamp diode is always active, cold-sparing can be accomplished either by employing a bus switch to isolate the device I/Os from the rest of the system or by driving each I/O pin to 0 V. If the resistor is chosen, the resistor value must be calculated based on decoupling capacitance on a given power supply on the board (this decoupling capacitance is in parallel with the resistor). The RC time constant should ensure full discharge of supplies before cold-sparing functionality is required. The resistor is necessary to ensure that the power pins are discharged to ground every time there is an interruption of power to the device.

IGLOOe and ProASIC3E devices support cold-sparing for all I/O configurations. Standards, such as PCI, that require I/O clamp diodes can also achieve cold-sparing compliance, since clamp diodes get disconnected internally when the supplies are at 0 V.

When targeting low-power applications, I/O cold-sparing may add additional current if a pin is configured with either a pull-up or pull-down resistor and driven in the opposite direction. A small static current is induced on each I/O pin when the pin is driven to a voltage opposite to the weak pull resistor. The current is equal to the voltage drop across the input pin divided by the pull resistor. Refer to the "Detailed I/O DC Characteristics" section of the appropriate family datasheet for the specific pull resistor value for the corresponding I/O standard.

For example, assuming an LVTTL 3.3 V input pin is configured with a weak pull-up resistor, a current will flow through the pull-up resistor if the input pin is driven LOW. For LVTTL 3.3 V, the pull-up resistor is ~45 kΩ, and the resulting current is equal to 3.3 V / 45 kΩ = 73 µA for the I/O pin. This is true also when a weak pull-down is chosen and the input pin is driven HIGH. This current can

be avoided by driving the input LOW when a weak pull-down resistor is used and driving it HIGH when a weak pull-up resistor is used.

This current draw can occur in the following cases:

- In Active and Static modes:
  - Input buffers with pull-up, driven LOW
  - Input buffers with pull-down, driven HIGH
  - Bidirectional buffers with pull-up, driven LOW
  - Bidirectional buffers with pull-down, driven HIGH
  - Output buffers with pull-up, driven LOW
  - Output buffers with pull-down, driven HIGH
  - Tristate buffers with pull-up, driven LOW
  - Tristate buffers with pull-down, driven HIGH
- In Flash*Freeze mode:
  - Input buffers with pull-up, driven LOW
  - Input buffers with pull-down, driven HIGH
  - Bidirectional buffers with pull-up, driven LOW
  - Bidirectional buffers with pull-down, driven HIGH

Electrostatic Discharge Protection

Low-power flash devices are tested per JEDEC Standard JESD22-A114-B.

These devices contain clamp diodes at every I/O, global, and power pad. Clamp diodes protect all device pads against damage from ESD as well as from excessive voltage transients.

All IGLOO and ProASIC3 devices are tested to the following models: the Human Body Model (HBM) with a tolerance of 2,000 V, the Machine Model (MM) with a tolerance of 250 V, and the Charged Device Model (CDM) with a tolerance of 200 V.

Each I/O has two clamp diodes. One diode has its positive (P) side connected to the pad and its negative (N) side connected to V_{CCI}. The second diode has its P side connected to GND and its N side connected to the pad. During operation, these diodes are normally biased in the off state, except when transient voltage is significantly above V_{CCI} or below GND levels.

In 30 k gate devices, the first diode is always off. In other devices, the clamp diode is always on and cannot be switched off.

By selecting the appropriate I/O configuration, the diode is turned on or off. Refer to Table 7-12 on page 7-19 for more information about the I/O standards and the clamp diode.

The second diode is always connected to the pad, regardless of the I/O configuration selected.

Table 7-12 • **I/O Hot-Swap and 5 V Input Tolerance Capabilities in IGLOO and ProASIC3 Devices**

I/O Assignment	Clamp Diode[1]		Hot Insertion		5 V Input Tolerance[2]		Input and Output Buffer
	AGL030 and A3P030	Other IGLOO and ProASIC3 Devices	AGL030 and A3P030	Other IGLOO and ProASIC3 Devices	AGL030 and A3P030	Other IGLOO and ProASIC3 Devices	
3.3 V LVTTL/LVCMOS	No	Yes	Yes	Yes	Yes[2]	Yes[2]	Enabled/Disabled
3.3 V PCI, 3.3 V PCI-X	N/A	Yes	N/A	Yes	N/A	Yes[2]	Enabled/Disabled
LVCMOS 2.5 V [5]	No	Yes	Yes	Yes	Yes[2]	Yes[4]	Enabled/Disabled
LVCMOS 2.5 V / 5.0 V [6]	N/A	Yes	N/A	Yes	N/A	Yes[4]	Enabled/Disabled
LVCMOS 1.8 V	No	Yes	Yes	Yes	No	No	Enabled/Disabled
LVCMOS 1.5 V	No	Yes	Yes	Yes	No	No	Enabled/Disabled
Differential, LVDS/ BLVDS/M-LVDS/ LVPECL	N/A	Yes	N/A	Yes	N/A	No	Enabled/Disabled

Notes:

1. *The clamp diode is always off for the AGL030 and A3P030 device and always active for other IGLOO and ProASIC3 devices.*
2. *Can be implemented with an external IDT bus switch, resistor divider, or Zener with resistor.*
3. *Refer to Table 7-8 on page 7-15 to Table 7-11 on page 7-16 for device-compliant information.*
4. *Can be implemented with an external resistor and an internal clamp diode.*
5. *The LVCMOS 2.5 V I/O standard is supported by the 30 k gate devices only; select the LVCMOS25 macro.*
6. *The LVCMOS 2.5 V / 5.0 V I/O standard is supported by all IGLOO and ProASIC3 devices except 30 k gate devices; select the LVCMOS5 macro.*

5 V Input and Output Tolerance

IGLOO and ProASIC3 devices are both 5 V-input– and 5 V–output–tolerant if certain I/O standards are selected. Table 7-5 on page 7-5 shows the I/O standards that support 5 V input tolerance. Only 3.3 V LVTTL/LVCMOS standards support 5 V output tolerance. Refer to the appropriate family datasheet for the detailed description and configuration information.

This feature is not shown in the I/O Attribute Editor.

5 V Input Tolerance

I/Os can support 5 V input tolerance when LVTTL 3.3 V, LVCMOS 3.3 V, LVCMOS 2.5 V, and LVCMOS 2.5 V / 5.0 V configurations are used (see Table 7-12 on page 7-19). There are four recommended solutions for achieving 5 V receiver tolerance (see Figure 7-9 on page 7-21 to Figure 7-12 on page 7-23 for details of board and macro setups). All the solutions meet a common requirement of limiting the voltage at the input to 3.6 V or less. In fact, the I/O absolute maximum voltage rating is 3.6 V, and any voltage above 3.6 V may cause long-term gate oxide failures.

Solution 1

The board-level design must ensure that the reflected waveform at the pad does not exceed the limits provided in the recommended operating conditions in the datasheet. This is a requirement to ensure long-term reliability.

This scheme will also work for a 3.3 V PCI/PCI-X configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the two external resistors as explained below. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.

This solution requires two board resistors, as demonstrated in Figure 7-9 on page 7-21. Here are some examples of possible resistor values (based on a simplified simulation model with no line effects and 10 Ω transmitter output resistance, where Rtx_out_high = $(V_{CCI} - V_{OH}) / I_{OH}$ and Rtx_out_low = V_{OL} / I_{OL}).

Example 1 (high speed, high current):

Rtx_out_high = Rtx_out_low = 10 Ω

R1 = 36 Ω (±5%), P(r1)min = 0.069 Ω

R2 = 82 Ω (±5%), P(r2)min = 0.158 Ω

Imax_tx = 5.5 V / (82 × 0.95 + 36 × 0.95 + 10) = 45.04 mA

$t_{RISE} = t_{FALL}$ = 0.85 ns at C_pad_load = 10 pF (includes up to 25% safety margin)

$t_{RISE} = t_{FALL}$ = 4 ns at C_pad_load = 50 pF (includes up to 25% safety margin)

Example 2 (low–medium speed, medium current):

Rtx_out_high = Rtx_out_low = 10 Ω

R1 = 220 Ω (±5%), P(r1)min = 0.018 Ω

R2 = 390 Ω (±5%), P(r2)min = 0.032 Ω

Imax_tx = 5.5 V / (220 × 0.95 + 390 × 0.95 + 10) = 9.17 mA

$t_{RISE} = t_{FALL}$ = 4 ns at C_pad_load = 10 pF (includes up to 25% safety margin)

$t_{RISE} = t_{FALL}$ = 20 ns at C_pad_load = 50 pF (includes up to 25% safety margin)

Other values of resistors are also allowed as long as the resistors are sized appropriately to limit the voltage at the receiving end to 2.5 V < Vin (rx) < 3.6 V when the transmitter sends a logic 1. This range of Vin_dc(rx) must be assured for any combination of transmitter supply (5 V ± 0.5 V), transmitter output resistance, and board resistor tolerances.

Temporary overshoots are allowed according to the overshoot and undershoot table in the datasheet.

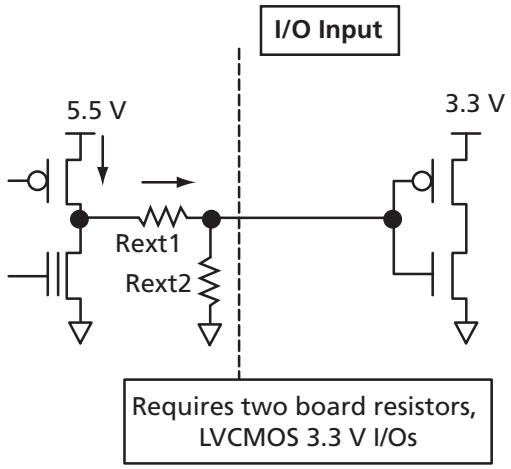


Figure 7-9 • **Solution 1**

Solution 2

The board-level design must ensure that the reflected waveform at the pad does not exceed the voltage overshoot/undershoot limits provided in the datasheet. This is a requirement to ensure long-term reliability.

This scheme will also work for a 3.3 V PCI/PCI-X configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the external resistors and Zener, as shown in Figure 7-10. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.

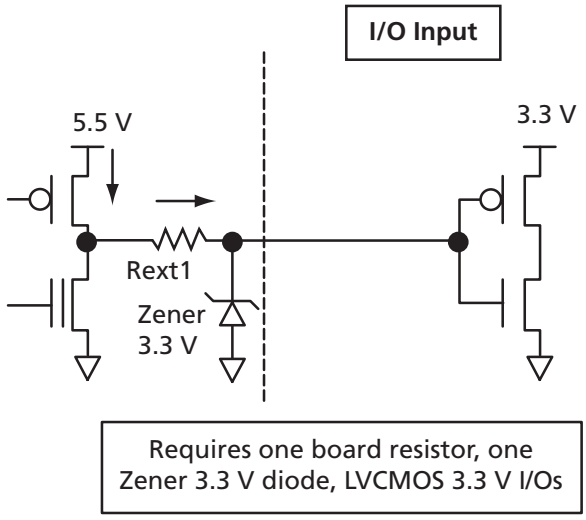


Figure 7-10 • **Solution 2**

Solution 3

The board-level design must ensure that the reflected waveform at the pad does not exceed the voltage overshoot/undershoot limits provided in the datasheet. This is a requirement to ensure long-term reliability.

This scheme will also work for a 3.3 V PCI/PCI-X configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the bus switch, as shown in Figure 7-11. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.

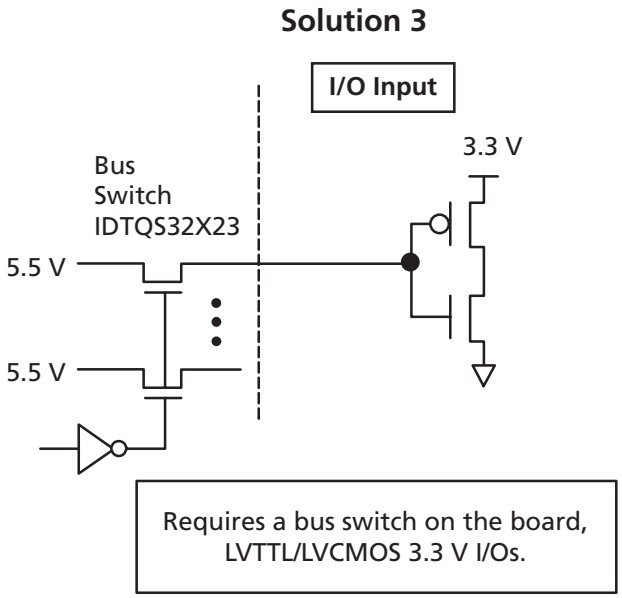


Figure 7-11 • **Solution 3**

Solution 4

The board-level design must ensure that the reflected waveform at the pad does not exceed the voltage overshoot/undershoot limits provided in the DS. This is a requirement to ensure long-term reliability.

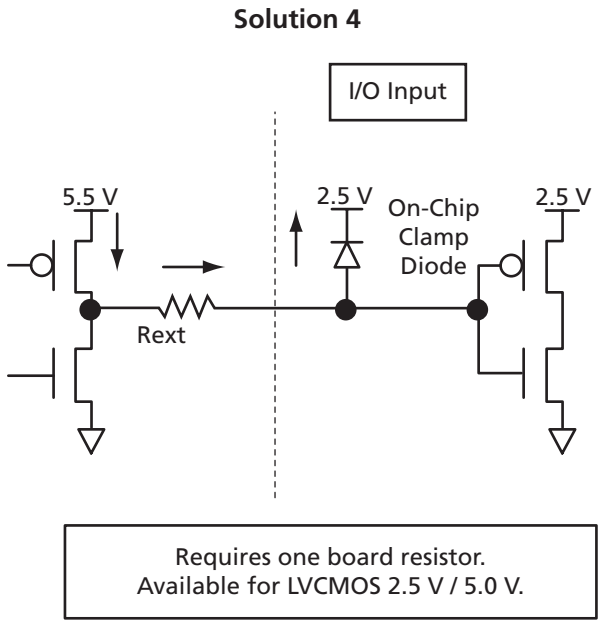


Figure 7-12 • **Solution 4**

Table 7-13 • **Comparison Table for 5 V–Compliant Receiver Solutions**

Solution	Board Components	Speed	Current Limitations
1	Two resistors	Low to High[1]	Limited by transmitter's drive strength
2	Resistor and Zener 3.3 V	Medium	Limited by transmitter's drive strength
3	Bus switch	High	N/A
4	Minimum resistor value[2,3,4,5] R = 47 Ω at T_J = 70°C R = 150 Ω at T_J = 85°C R = 420 Ω at T_J = 100°C	Medium	Maximum diode current at 100% duty cycle, signal constantly at 1 52.7 mA at T_J = 70°C / 10-year lifetime 16.5 mA at T_J = 85°C / 10-year lifetime 5.9 mA at T_J = 100°C / 10-year lifetime For duty cycles other than 100%, the currents can be increased by a factor of 1 / (duty cycle). Example: 20% duty cycle at 70°C Maximum current = (1 / 0.2) × 52.7 mA = 5 × 52.7 mA = 263.5 mA

Notes:

1. *Speed and current consumption increase as the board resistance values decrease.*
2. *Resistor values ensure I/O diode long-term reliability.*
3. *At 70°C, customers could still use 420 Ω on every I/O.*
4. *At 85°C, a 5 V solution on every other I/O is permitted, since the resistance is lower (150 Ω) and the current is higher. Also, the designer can still use 420 Ω and use the solution on every I/O.*
5. *At 100°C, the 5 V solution on every I/O is permitted, since 420 Ω are used to limit the current to 5.9 mA.*

5 V Output Tolerance

IGLOO and ProASIC3 I/Os must be set to 3.3 V LVTTL or 3.3 V LVCMOS mode to reliably drive 5 V TTL receivers. It is also critical that there be NO external I/O pull-up resistor to 5 V, since this resistor would pull the I/O pad voltage beyond the 3.6 V absolute maximum value and consequently cause damage to the I/O.

When set to 3.3 V LVTTL or 3.3 V LVCMOS mode, the I/Os can directly drive signals into 5 V TTL receivers. In fact, V_{OL} = 0.4 V and V_{OH} = 2.4 V in both 3.3 V LVTTL and 3.3 V LVCMOS modes exceeds the V_{IL} = 0.8 V and V_{IH} = 2 V level requirements of 5 V TTL receivers. Therefore, level 1 and level 0 will be recognized correctly by 5 V TTL receivers.

Schmitt Trigger

A Schmitt trigger is a buffer used to convert a slow or noisy input signal into a clean one before passing it to the FPGA. Using Schmitt trigger buffers guarantees a fast, noise-free input signal to the FPGA.

The Schmitt trigger is available for the LVTTL, LVCMOS, and 3.3 V PCI I/O standards.

This feature can be implemented by using a Physical Design Constraints (PDC) command (Table 7-5 on page 7-5) or by selecting a check box in the I/O Attribute Editor in Designer. The check box is cleared by default.

Selectable Skew between Output Buffer Enable and Disable Times

Low-power flash devices have a configurable skew block in the output buffer circuitry that can be enabled to delay output buffer assertion without affecting deassertion time. Since this skew block is only available for the OE signal, the feature can be used in tristate and bidirectional buffers. A typical 1.2 ns delay is added to the OE signal to prevent potential bus contention. Refer to the appropriate family datasheet for detailed timing diagrams and descriptions.

The skew feature is available for all I/O standards.

This feature can be implemented by using a PDC command (Table 7-5 on page 7-5) or by selecting a check box in the I/O Attribute Editor in Designer. The check box is cleared by default.

The configurable skew block is used to delay output buffer assertion (enable) without affecting deassertion (disable) time.

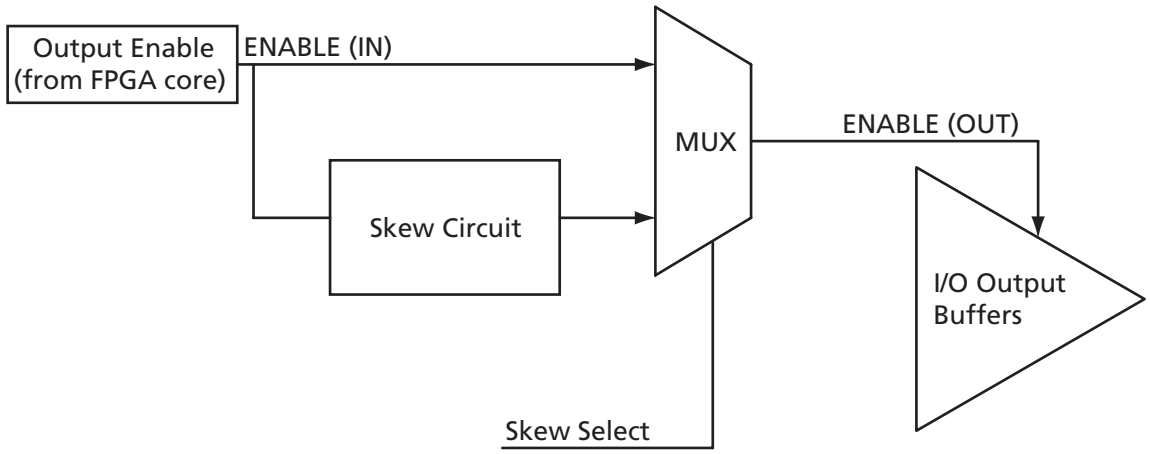


Figure 7-13 • **Block Diagram of Output Enable Path**

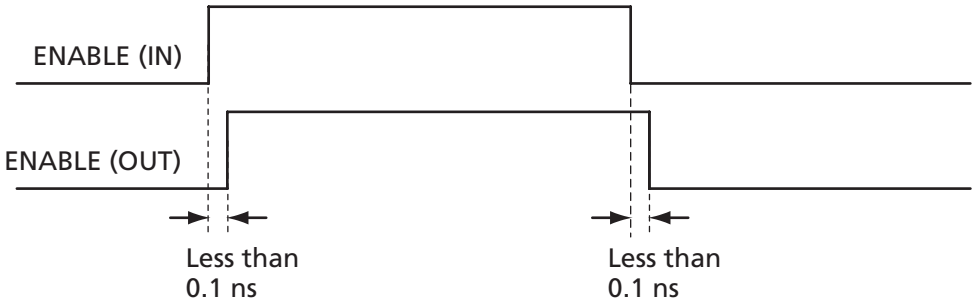


Figure 7-14 • **Timing Diagram (option 1: bypasses skew circuit)**

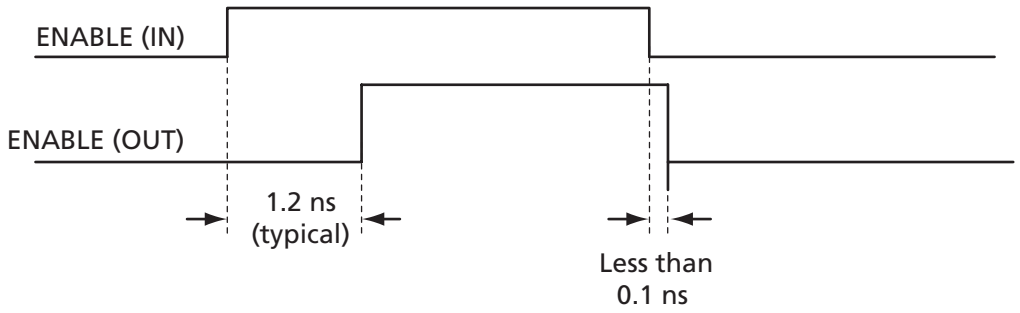


***Figure 7-15* • Timing Diagram (option 2: enables skew circuit)**

At the system level, the skew circuit can be used in applications where transmission activities on bidirectional data lines need to be coordinated. This circuit, when selected, provides a timing margin that can prevent bus contention and subsequent data loss and/or transmitter over-stress due to transmitter-to-transmitter current shorts. Figure 7-16 presents an example of the skew circuit implementation in a bidirectional communication system. Figure 7-17 on page 7-27 shows how bus contention is created, and Figure 7-18 on page 7-27 shows how it can be avoided with the skew circuit.

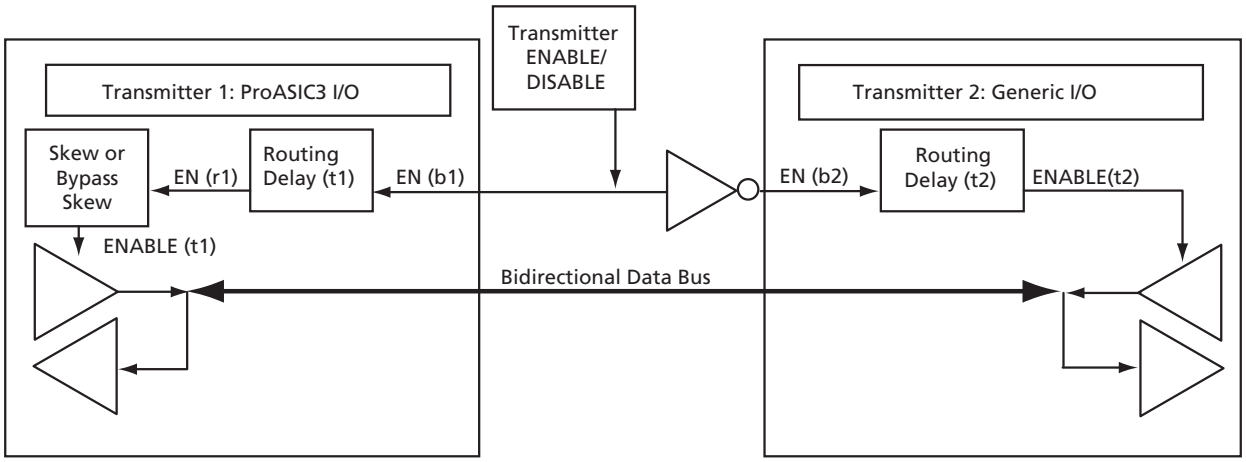


***Figure 7-16* • Example of Implementation of Skew Circuits in Bidirectional Transmission Systems Using IGLOO or ProASIC3 Devices**

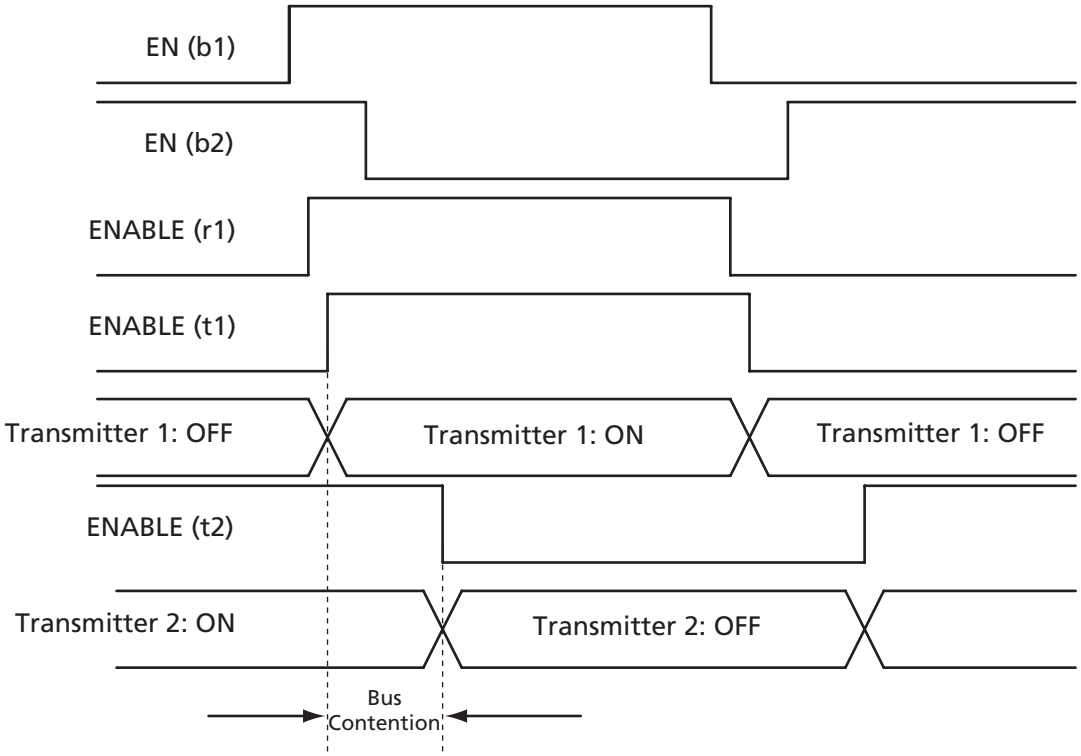


Figure 7-17 **• Timing Diagram (bypasses skew circuit)**

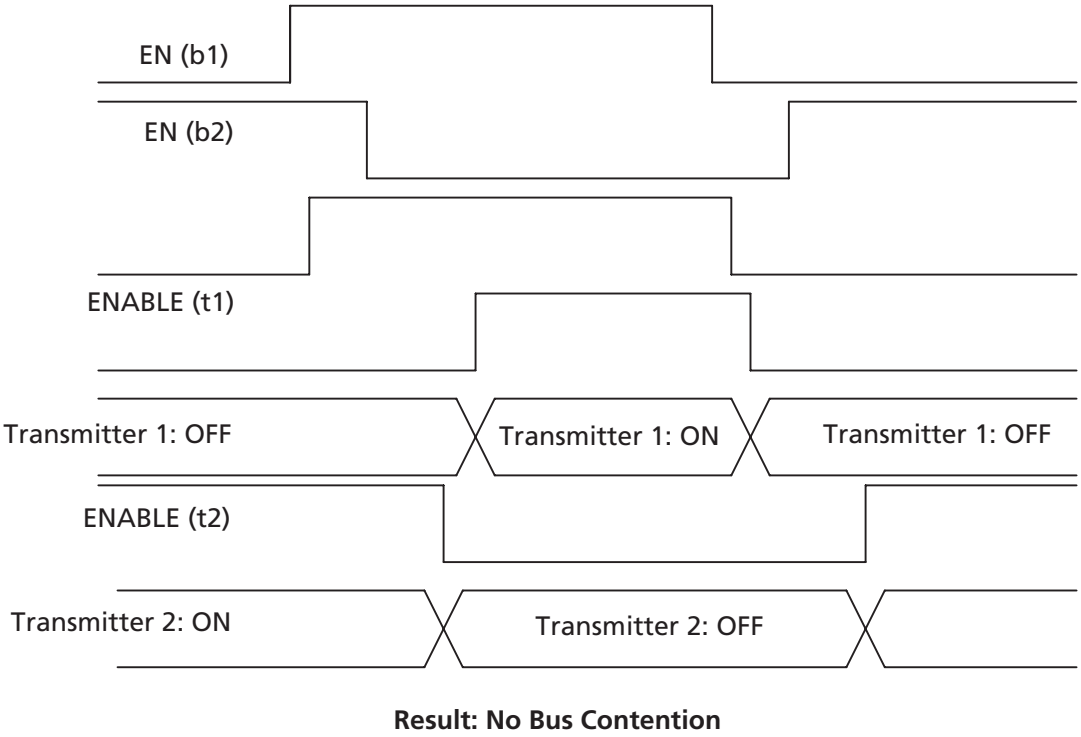


Figure 7-18 **• Timing Diagram (with skew circuit selected)**

I/O Register Combining

Every I/O has several embedded registers in the I/O tile that are close to the I/O pads. Rather than using the internal register from the core, the user has the option of using these registers for faster clock-to-out timing, and external hold and setup. When combining these registers at the I/O buffer, some architectural rules must be met. Provided these rules are met, the user can enable register combining globally during Compile (as shown in the "Compiling the Design" section in the *I/O Software Control in Low-Power Flash Devices* section of the handbook).

This feature is supported by all I/O standards.

Rules for Registered I/O Function:

1. The fanout between an I/O pin (D, Y, or E) and a register must be equal to one for combining to be considered on that pin.
2. All registers (Input, Output, and Output Enable) connected to an I/O must share the same clear or preset function:
   - If one of the registers has a CLR pin, all the other registers that are candidates for combining in the I/O must have a CLR pin.
   - If one of the registers has a PRE pin, all the other registers that are candidates for combining in the I/O must have a PRE pin.
   - If one of the registers has neither a CLR nor a PRE pin, all the other registers that are candidates for combining must have neither a CLR nor a PRE pin.
   - If the clear or preset pins are present, they must have the same polarity.
   - If the clear or preset pins are present, they must be driven by the same signal (net).
3. Registers connected to an I/O on the Output and Output Enable pins must have the same clock and enable function:
   - Both the Output and Output Enable registers must have an E pin (clock enable), or none at all.
   - If the E pins are present, they must have the same polarity. The CLK pins must also have the same polarity.

In some cases, the user may want registers to be combined with the input of a bibuf while maintaining the output as-is. This can be achieved by using PDC commands as follows:

```
set_io <signal name> -REGISTER yes ------register will combine
set_preserve <signal name> ----register will not combine
```

Weak Pull-Up and Weak Pull-Down Resistors

IGLOO and ProASIC3 devices support optional weak pull-up and pull-down resistors on each I/O pin. When the I/O is pulled up, it is connected to the V_{CCI} of its corresponding I/O bank. When it is pulled down, it is connected to GND. Refer to the datasheet for more information.

For low-power applications, configuration of the pull-up or pull-down of the I/O can be used to set the I/O to a known state while the device is in Flash*Freeze mode. Refer to *Flash*Freeze Technology and Low-Power Modes in IGLOO and ProASIC3L Devices* for more information.

The Flash*Freeze (FF) pin cannot be configured with a weak pull-down or pull-up I/O attribute, as the signal needs to be driven at all times.

Output Slew Rate Control

The slew rate is the amount of time an input signal takes to get from logic LOW to logic HIGH or vice versa.

It is commonly defined as the propagation delay between 10% and 90% of the signal's voltage swing. Slew rate control is available for the output buffers of low-power flash devices. The output buffer has a programmable slew rate for both HIGH-to-LOW and LOW-to-HIGH transitions. Slew rate control is available for LVTTL, LVCMOS, and PCI-X I/O standards. The other I/O standards have a preset slew value.

The slew rate can be implemented by using a PDC command (Table 7-5 on page 7-5), setting "High" or "Low" in the I/O Attribute Editor in Designer, or instantiating a special I/O macro. The default slew rate value is "High."

IGLOO and ProASIC3 devices support output slew rate control: high and low. Actel recommends the high slew rate option to minimize the propagation delay. This high-speed option may introduce noise into the system if appropriate signal integrity measures are not adopted. Selecting a low slew rate reduces this kind of noise but adds some delays in the system. Low slew rate is recommended when bus transients are expected.

Output Drive

The output buffers of IGLOO and ProASIC3 devices can provide multiple drive strengths to meet signal integrity requirements. The LVTTL and LVCMOS (except 1.2 V LVCMOS) standards have selectable drive strengths. Other standards have a preset value.

Drive strength should also be selected according to the design requirements and noise immunity of the system.

The output slew rate and multiple drive strength controls are available in LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V, LVCMOS 2.5 V / 5.0 V input, LVCMOS 1.8 V, and LVCMOS 1.5 V. All other I/O standards have a high output slew rate by default.

For 30 k gate devices, refer to Table 7-14. For other ProASIC3 and IGLOO devices, refer to Table 7-15 through Table 7-16 on page 7-30 for more information about the slew rate and drive strength specification. Refer to Table 7-4 on page 7-4 for I/O bank type definitions.

There will be a difference in timing between the Standard Plus I/O banks and the Advanced I/O banks. Refer to the I/O timing tables in the datasheet for the standards supported by each device.

Table 7-14 • **IGLOO and ProASIC3 Output Drive and Slew for Standard I/O Bank Type (for 30 k gate devices)**

I/O Standards	2 mA	4 mA	6 mA	8 mA	Slew	
LVTTL/LVCMOS 3.3 V	✓	✓	✓	✓	High	Low
LVCMOS 2.5 V	✓	✓	✓	✓	High	Low
LVCMOS 1.8 V	✓	✓	–	–	High	Low
LVCMOS 1.5 V	✓	–	–	–	High	Low

Table 7-15 • **IGLOO and ProASIC3 Output Drive and Slew for Standard Plus I/O Bank Type**

I/O Standards	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	Slew	
LVTTL	✓	✓	✓	✓	✓	✓	High	Low
LVCMOS 3.3 V	✓	✓	✓	✓	✓	✓	High	Low
LVCMOS 2.5 V	✓	✓ *	✓	✓ *	✓	–	High	Low
LVCMOS 1.8 V	✓	✓	✓	✓	–	–	High	Low
LVCMOS 1.5 V	✓	✓	–	–	–	–	High	Low

*Note: *Not available in Automotive devices.*

Table 7-16 • **IGLOO and ProASIC3 Output Drive and Slew for Advanced I/O Bank Type**

I/O Standards	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA	Slew	
LVTTL	✓	✓	✓	✓	✓	✓	✓	High	Low
LVCMOS 3.3 V	✓	✓	✓	✓	✓	✓	✓	High	Low
LVCMOS 2.5 V	✓	✓ *	✓	✓ *	✓	✓	✓	High	Low
LVCMOS 2.5/5.0 V	✓	✓ *	✓	✓ *	✓	✓	✓	High	Low
LVCMOS 1.8 V	✓	✓	✓	✓	✓	✓	–	High	Low
LVCMOS 1.5 V	✓	✓	✓	✓	✓	–	–	High	Low

Note: Not available in Automotive devices.

Simultaneously Switching Outputs (SSOs) and Printed Circuit Board Layout

Each I/O voltage bank has a separate ground and power plane for input and output circuits (VMV/GNDQ for input buffers and V_{CCI}/GND for output buffers). This isolation is necessary to minimize simultaneous switching noise from the input and output (SSI and SSO). The switching noise (ground bounce and power bounce) is generated by the output buffers and transferred into input buffer circuits, and vice versa.

Since voltage bounce originates on the package inductance, the VMV and V_{CCI} supplies have separate package pin assignments. For the same reason, GND and GNDQ also have separate pin assignments.

The VMV and V_{CCI} pins must be shorted to each other on the board. Also, the GND and GNDQ pins must be shorted to each other on the board. This will prevent unwanted current draw from the power supply.

SSOs can cause signal integrity problems on adjacent signals that are not part of the SSO bus. Both inductive and capacitive coupling parasitics of bond wires inside packages and of traces on PCBs will transfer noise from SSO busses onto signals adjacent to those busses. Additionally, SSOs can produce ground bounce noise and V_{CCI} dip noise. These two noise types are caused by rapidly changing currents through GND and V_{CCI} package pin inductances during switching activities (EQ 7-2 and EQ 7-3).

$$\text{Ground bounce noise voltage} = L(GND) \times di/dt \qquad \textit{EQ 7-2}$$

$$V_{CCI} \text{ dip noise voltage} = L(V_{CCI}) \times di/dt \qquad \textit{EQ 7-3}$$

Any group of four or more input pins switching on the same clock edge is considered an SSO bus. The shielding should be done both on the board and inside the package unless otherwise described.

In-package shielding can be achieved in several ways; the required shielding will vary depending on whether pins next to the SSO bus are LVTTL/LVCMOS inputs, LVTTL/LVCMOS outputs, or GTL/SSTL/HSTL/LVDS/LVPECL inputs and outputs. Board traces in the vicinity of the SSO bus have to be adequately shielded from mutual coupling and inductive noise that can be generated by the SSO bus. Also, noise generated by the SSO bus needs to be reduced inside the package.

PCBs perform an important function in feeding stable supply voltages to the IC and, at the same time, maintaining signal integrity between devices.

Key issues that need to be considered are as follows:

- Power and ground plane design and decoupling network design
- Transmission line reflections and terminations

For extensive data per package on the SSO and PCB issues, refer to *ProASIC3/E SSO and Pin Placement and Guidelines* chapter of the handbook.

I/O Software Support

In Actel's Libero IDE software, default settings have been defined for the various I/O standards supported. Changes can be made to the default settings via the use of attributes; however, not all I/O attributes are applicable for all I/O standards. Table 7-17 list the valid I/O attributes that can be manipulated by the user for each I/O standard.

Single-ended I/O standards in low-power flash devices support up to five different drive strengths.

Table 7-17 • **IGLOO and ProASIC3 I/O Attributes vs. I/O Standard Applications**

I/O Standard	SLEW (output only)	OUT_DRIVE (output only)	SKEW (all macros with OE)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER
LVTTL/LVCMOS 3.3 V	✓	✓	✓	✓	✓	✓
LVCMOS 2.5 V	✓	✓	✓	✓	✓	✓
LVCMOS 2.5/5.0 V	✓	✓	✓	✓	✓	✓
LVCMOS 1.8 V	✓	✓	✓	✓	✓	✓
LVCMOS 1.5 V	✓	✓	✓	✓	✓	✓
PCI (3.3 V)			✓		✓	✓
PCI-X (3.3 V)	✓		✓		✓	✓
LVDS, BLVDS, M-LVDS			✓			✓
LVPECL						✓

Note: Applies to all 30 k gate devices.

Table 7-18 lists the default values for the above selectable I/O attributes as well as those that are preset for that I/O standard. See Table 7-14 on page 7-29 to Table 7-16 on page 7-30 for SLEW and OUT_DRIVE settings.

Table 7-18 • **IGLOO and ProASIC3 I/O Default Attributes**

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (tribuf and bibuf only)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER
LVTTL/LVCMOS 3.3 V	See Table 7-14 on page 7-29 to Table 7-16 on page 7-30.	See Table 7-14 on page 7-29 to Table 7-16 on page 7-30.	Off	None	35 pF	–
LVCMOS 2.5 V			Off	None	35 pF	–
LVCMOS 2.5/5.0 V			Off	None	35 pF	–
LVCMOS 1.8 V			Off	None	35 pF	–
LVCMOS 1.5 V			Off	None	35 pF	–
PCI (3.3 V)			Off	None	10 pF	–
PCI-X (3.3 V)			Off	None	10 pF	–
LVDS, BLVDS, M-LVDS			Off	None	0 pF	–
LVPECL			Off	None	0 pF	–

User I/O Naming Convention

IGLOO and ProASIC3

Due to the comprehensive and flexible nature of IGLOO and ProASIC3 device user I/Os, a naming scheme is used to show the details of each I/O (Figure 7-19 on page 7-33 and Figure 7-20 on page 7-33). The name identifies to which I/O bank it belongs, as well as pairing and pin polarity for differential I/Os.

I/O Nomenclature = FF/Gmn/IOuxwBy

Gmn is only used for I/Os that also have CCC access—i.e., global pins.

FF = Indicates the I/O dedicated for the Flash*Freeze mode activation pin in IGLOO and ProASIC3L devices only

G = Global

m = Global pin location associated with each CCC on the device: A (northwest corner), B (northeast corner), C (east middle), D (southeast corner), E (southwest corner), and F (west middle)

n = Global input MUX and pin number of the associated Global location m—either A0, A1, A2, B0, B1, B2, C0, C1, or C2. Refer to *Global Resources in Actel Low-Power Flash Devices* for information about the three input pins per clock source MUX at CCC location m.

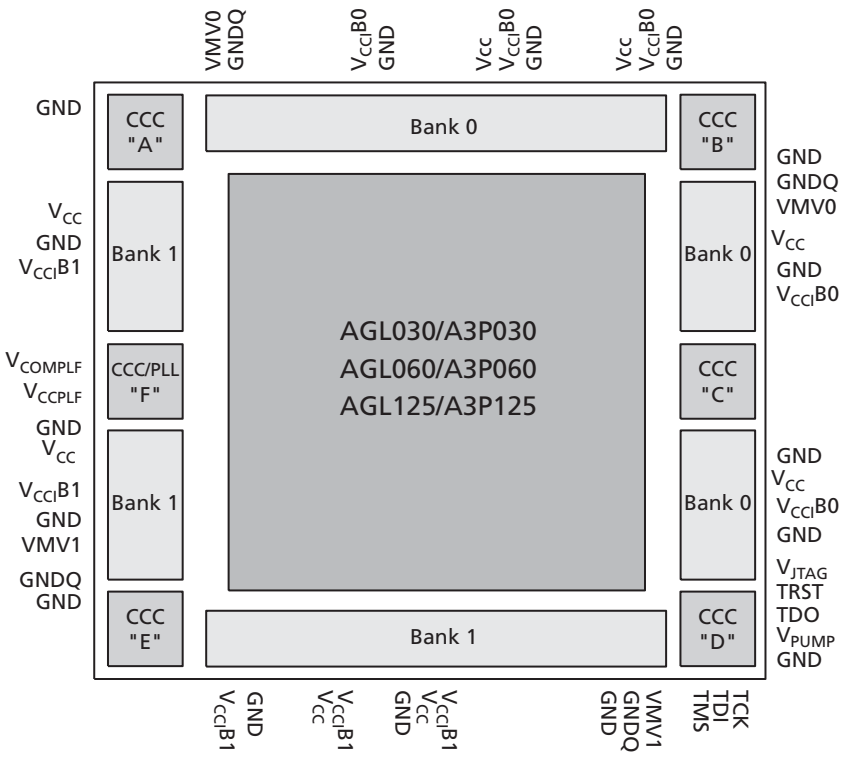
u = I/O pair number in the bank, starting at 00 from the northwest I/O bank and proceeding in a clockwise direction

x = P or U (Positive), N or V (Negative) for differential pairs, or R (Regular—single-ended) for the I/Os that support single-ended and voltage-referenced I/O standards only. U (Positive) or V (Negative)—for LVDS, DDR LVDS, BLVDS, and M-LVDS only—restricts the I/O differential pair from being selected as an LVPECL pair.

w = D (Differential Pair), P (Pair), or S (Single-Ended). D (Differential Pair) if both members of the pair are bonded out to adjacent pins or are separated only by one GND or NC pin; P (Pair) if both members of the pair are bonded out but do not meet the adjacency requirement; or S (Single-Ended) if the I/O pair is not bonded out. For Differential Pairs (D), adjacency for ball grid packages means only vertical or horizontal. Diagonal adjacency does not meet the requirements for a true differential pair.

B = Bank

y = Bank number (0–3). The Bank number starts at 0 from the northwest I/O bank and proceeds in a clockwise direction.



Note: The 30 k gate devices do not support a PLL (V_{COMPLF} and V_{CCPLF} pins).

***Figure 7-19* • Naming Conventions of IGLOO and ProASIC3 Devices with Two I/O Banks – Top View**

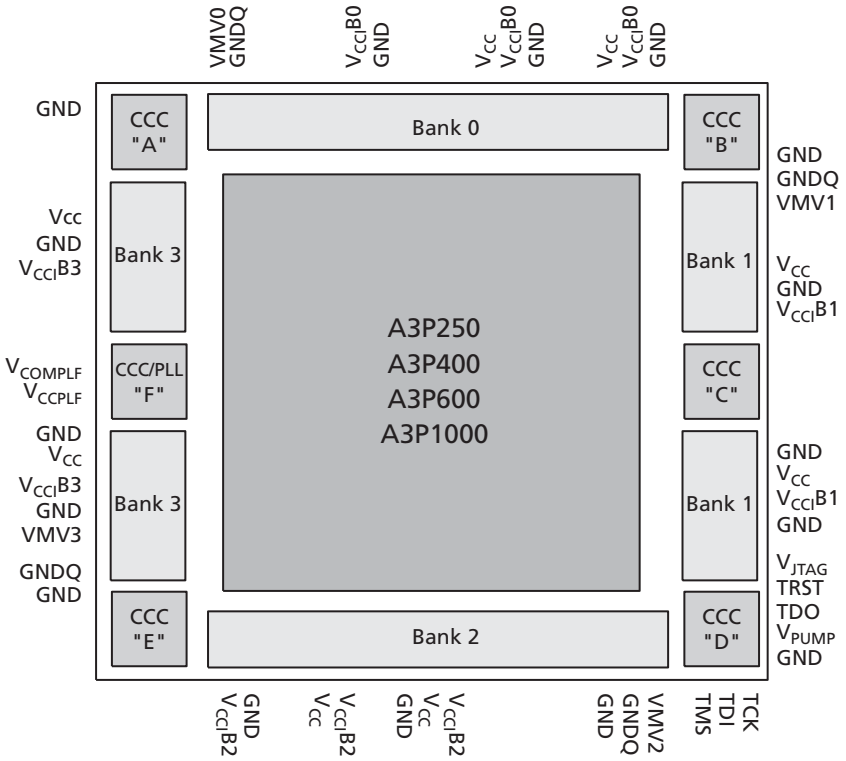


***Figure 7-20* • Naming Conventions of IGLOO and ProASIC3 Devices with Four I/O Banks – Top View**

Board-Level Considerations

Low-power flash devices have robust I/O features that can help in reducing board-level components. The devices offer single-chip solutions, which makes the board layout simpler and more immune to signal integrity issues. Although, in many cases, these devices resolve board-level issues, special attention should always be given to overall signal integrity. This section covers important board-level considerations to facilitate optimum device performance.

Termination

Proper termination of all signals is essential for good signal quality. Nonterminated signals, especially clock signals, can cause malfunctioning of the device.

For general termination guidelines, refer to the *Board-Level Considerations* application note for Actel FPGAs. Also refer to *Pin Descriptions* for termination requirements for specific pins.

Low-power flash I/Os are equipped with on-chip pull-up/-down resistors. The user can enable these resistors by instantiating them either in the top level of the design (refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide* for the available I/O macros with pull-up/-down) or in the I/O Attribute Editor in Designer if generic input or output buffers are instantiated in the top level. Unused I/O pins are configured as inputs with pull-up resistors.

As mentioned earlier, low-power flash devices have multiple programmable drive strengths, and the user can eliminate unwanted overshoot and undershoot by adjusting the drive strengths.

Power-Up Behavior

Low-power flash devices are power-up/-down friendly; i.e., no particular sequencing is required for power-up and power-down. This eliminates extra board components for power-up sequencing, such as a power-up sequencer.

During power-up, all I/Os are tristated, irrespective of I/O macro type (input buffers, output buffers, I/O buffers with weak pull-ups or weak pull-downs, etc.). Once I/Os become activated, they are set to the user-selected I/O macros. Refer to the *Power-Up/-Down Behavior of Low-Power Flash Devices* chapter of the *ProASIC3* and *ProASIC3E* handbooks for details.

Drive Strength

Low-power flash devices have up to seven programmable output drive strengths. The user can select the drive strength of a particular output in the I/O Attribute Editor or can instantiate a specialized I/O macro, such as OUTBUF_S_12 (slew = low, out_drive = 12 mA).

The maximum available drive strength is 24 mA per I/O. Though no I/O should be forced to source or sink more than 24 mA indefinitely, I/Os may handle a higher amount of current (refer to the device IBIS model for maximum source/sink current) during signal transition (AC current). Every device package has its own power dissipation limit; hence, power calculation must be performed accurately to determine how much current can be tolerated per I/O within that limit.

I/O Interfacing

Low-power flash devices are 5 V–input– and 5 V–output–tolerant without adding any extra circuitry. Along with other low-voltage I/O macros, this 5 V tolerance makes these devices suitable for many types of board component interfacing.

Table 7-19 shows some high-level interfacing examples using low-power flash devices.

Table 7-19 • **High-Level Interface Examples**

Interface	Clock		I/O			
	Type	Frequency	Type	Signals In	Signals Out	Data I/O
GM	Src Sync	125 MHz	LVTTL	8	8	125 Mbps
TBI	Src Sync	125 MHz	LVTTL	10	10	125 Mbps
XSBI	Src Sync	644 MHz	LVDS	16	16	644 Mbps
XGMI	Src Sync DDR	156 MHz	HSTL1	32	32	312 Mbps
FlexBus 3	Sys Sync	104 MHz	LVTTL	≤32	≤32	≤104
Pos-PHY3/SPI-3	Sys Sync	104	LVTTL	8,16,32	8,16,32	≤104 Mbps
FlexBus 4/SPI-4.1	Src Sync	200 MHz	HSTL1	16,64	16,64	200 Mbps
Pos-PHY4/SPI-4.2	Src Sync DDR	≥311 MHz	LVDS	16	16	≥622 Mbps
SFI-4.1	Src Sync	622 MHz	LVDS	16	16	622 Mbps
CSIX L1	Sys Sync	≤250 MHz	HSTL1	32,64,96,128	32,64,96,128	≤250 Mbps
Hyper Transport	Sys Sync DDR	≤800 MHz	LVDS	2,4,8,16	2,4,8,16	≤1.6 Gbps
Rapid I/O Parallel	Sys Sync DDR	250 MHz – 1 GHz	LVDS	8,16	8,16	≤2 Gbps
Star Fabric	CDR		LVDS	4	4	622 Mbps

Note: Sys Sync = System Synchronous Clocking, Src Sync = Source Synchronous Clocking, and CDR = Clock and Data Recovery.

Conclusion

IGLOO and ProASIC3 support for multiple I/O standards minimizes board-level components and makes possible a wide variety of applications. The Actel Designer software, integrated with Actel Libero IDE, presents a clear visual display of I/O assignments, allowing users to verify I/O and board-level design requirements before programming the device. The IGLOO and ProASIC3 device I/O features and functionalities ensure board designers can produce low-cost and low-power FPGA applications fulfilling the complexities of contemporary design needs.

Related Documents

Handbook Documents

Board-Level Considerations
http://www.actel.com/documents/BoardLevelCons_AN.pdf
DDR for Actel's Low-Power Flash Devices
http://www.actel.com/documents/LPD_DDR_HBs.pdf
*Flash*Freeze Technology and Low-Power Modes in IGLOO and ProASIC3L Devices*
http://www.actel.com/documents/LPD_FlashFreeze_HBs.pdf
Global Resources in Actel Low-Power Flash Devices
http://www.actel.com/documents/LPD_Global_HBs.pdf
Pin Descriptions
http://www.actel.com/documents/LPD_PinDescriptions_HBs.pdf
Power-Up/-Down Behavior of Low-Power Flash Devices
http://www.actel.com/documents/LPD_PowerUp_HBs.pdf
ProASIC3/E SSO and Pin Placement and Guidelines
http://www.actel.com/documents/PA3_E_SSO_HBs.pdf

User's Guides

Actel Libero IDE User's Guide
http://www.actel.com/documents/libero_ug.pdf
IGLOO, Fusion, and ProASIC3 Macro Library Guide
http://www.actel.com/documents/pa3_libguide_ug.pdf
SmartGen Core Reference Guide
http://www.actel.com/documents/genguide_ug.pdf

Part Number and Revision Date

This document contains content extracted from the Device Architecture section of the datasheet, combined with content previously published as an application note describing features and functions of the device. To improve usability for customers, the device architecture information has now been combined with usage information, to reduce duplication and possible inconsistencies in published information. No technical changes were made to the datasheet content unless explicitly listed. Changes to the application note content were made only to be consistent with existing datasheet information.

Part Number 51700094-009-2

Revised June 2008

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v1.2)	Page
v1.1 (March 2008)	The following changes were made to the family descriptions in Table 7-1 · Low-Power Flash Families: • ProASIC3L was updated to include 1.5 V. • The number of PLLs for ProASIC3E was changed from five to six.	7-2
v1.0 (January 2008)	Originally, this document contained information on all IGLOO and ProASIC3 families. With the addition of new families and to highlight the differences between the features, the document has been separated into 3 documents: This document contains information specific to IGLOO, ProASIC3, and ProASIC3L. *I/O Structures in IGLOOe and ProASIC3E Devices* contains information specific to IGLOOe, ProASIC3E, and ProASIC3EL I/O features. *I/O Structures in IGLOO PLUS Devices* contains information specific to IGLOO PLUS I/O features.	N/A

8 – I/O Software Control in Low-Power Flash Devices

Actel Fusion,® IGLOO,® and ProASIC®3 I/Os provide more design flexibility, allowing the user to control specific features by enabling certain I/O standards. Some features are selectable only for certain I/O standards, whereas others are available for all I/O standards. For example, slew control is not supported by differential I/O standards. Conversely, I/O register combining is supported by all I/O standards. For detailed information about which I/O standards and features are available on each device and each I/O type, refer to the I/O Structures section of the handbook for the device you are using.

Figure 8-1 shows the various points in the software design flow where a user can provide input or control of the I/O selection and parameters. A detailed description is provided throughout this document.

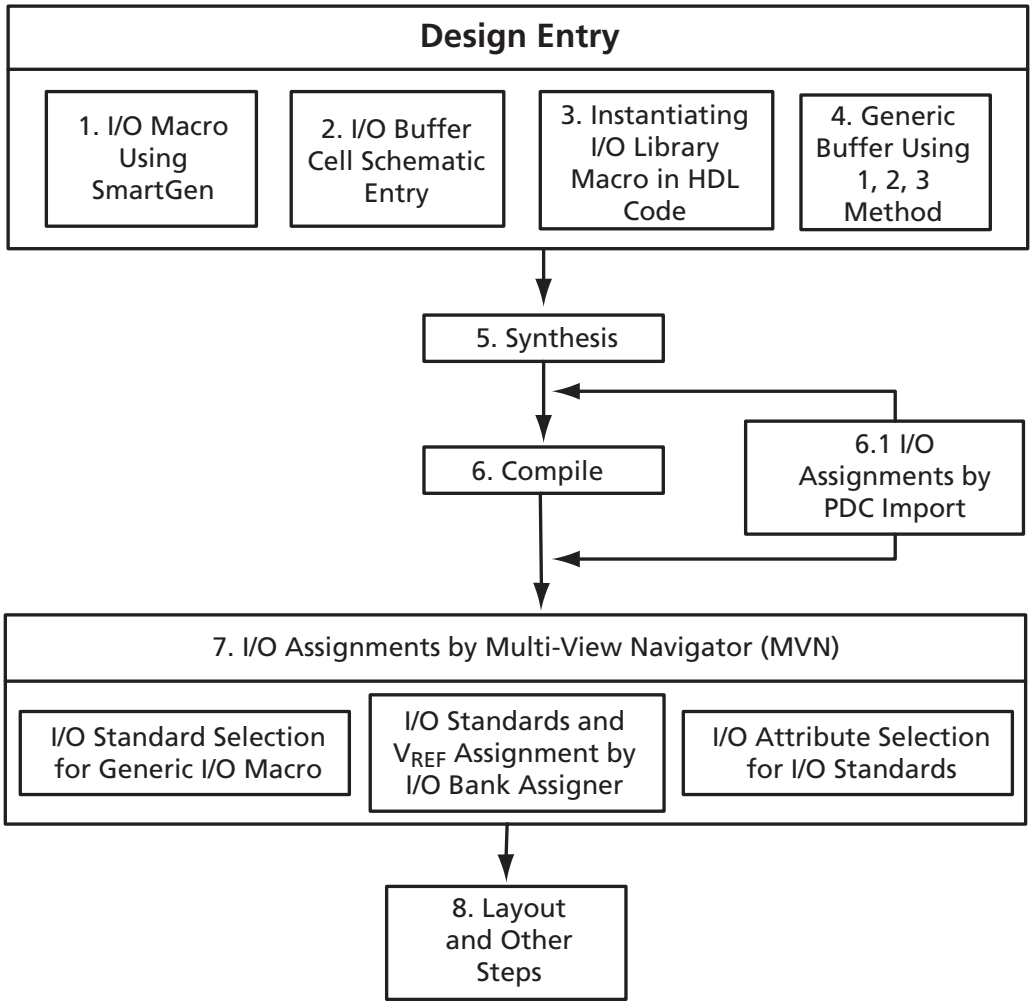


Figure 8-1 • **User I/O Assignment Flow Chart**

IGLOO and ProASIC3 I/O Support

The low-power flash families listed in Table 8-1 support I/Os and the functions described in this document.

Table 8-1 • **Low-Power Flash Families**

Family[1]	Description	Timing Numbers[2]
IGLOO	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*IGLOO DC and Switching Characteristics*
IGLOO PLUS	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology and enhanced I/O capabilities	*IGLOO PLUS DC and Switching Characteristics*
IGLOOe	IGLOO devices enhanced with higher density, five additional PLLs, and additional I/O standards	*IGLOOe DC and Switching Characteristics*
ProASIC3L	Low-power, high-performance 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*ProASIC3L DC and Switching Characteristics*
ProASIC3	Low-power, high-performance 1.5 V FPGAs	*ProASIC3 DC and Switching Characteristics*
ProASIC3E	ProASIC3 enhanced with higher density, six additional PLLs, and additional I/O standards	*ProASIC3E DC and Switching Characteristics*
ProASIC3 Automotive	Low-power, high-performance FPGAs qualified for Automotive applications	*Automotive ProASIC3 DC and Switching Characteristics*

Notes:

1. *The family names are linked to the appropriate product brief.*
2. *The timing number links go to the relevant timing numbers in the datasheet.*

Actel's low-power flash devices (listed in Table 8-1) provide a selection of low-power, secure, live-at-power-up, single-chip solutions. The nonvolatile flash-based devices do not require a boot PROM and incorporate FlashLock® technology, which provides a unique combination of reprogrammability and design security without external overhead. Only low-power flash FPGAs can offer these advantages.

Actel IGLOO PLUS FPGAs are the industry-leading 1.2 V ultra-low-power programmable logic devices (PLDs) and consume 90% less static power and over 50% less dynamic power than PLD alternatives, while ProASIC3L devices offer a balance of low power and higher performance.

Flash*Freeze technology used in IGLOO, IGLOO PLUS, and ProASIC3L devices enables easy entry to and exit from the ultra-low power mode, which consumes as little as 5 µW, while retaining SRAM and register data. IGLOO PLUS also offers the ability to hold I/O state in Flash*Freeze Mode. Flash*Freeze technology simplifies power management through I/O and clock management without the need to turn off voltages, I/Os, or clocks at the system level. Entering and exiting Flash*Freeze mode takes less than 1 µs.

The Actel Fusion family, based on the highly successful ProASIC3 flash FPGA architecture, has been designed as a high-performance, mixed-signal Programmable System Chip. Fusion supports many peripherals, including embedded flash memory, analog-to-digital converter (ADC), high-drive outputs, RC and crystal oscillators, and real-time counter (RTC). The total available on-chip memory, including the flash array blocks, is greater than that found in SRAM FPGAs.

IGLOO Terminology

In documentation, the term IGLOO families or IGLOO devices refers to all IGLOO families as listed in Table 8-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

ProASIC3 Terminology

In documentation, the term ProASIC3 families or ProASIC3 devices refers to all ProASIC3 families as listed in Table 8-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

Software-Controlled I/O Attributes

Users may modify these programmable I/O attributes using the I/O Attribute Editor. Modifying an I/O attribute may result in a change of state in Designer. Table 8-2 details which steps have to be re-run as a function of modified I/O attribute.

Table 8-2 • **Designer State (resulting from I/O attribute modification)**

	Designer States				
I/O Attribute	**Compile**	**Layout**	**Fuse**	**Timing**	**Power**
Slew Control	No	No	Yes	Yes	Yes
Output Drive (mA)	No	No	Yes	Yes	Yes
Skew Control	No	No	Yes	Yes	Yes
Resistor Pull	No	No	Yes	Yes	Yes
Input Delay	No	No	Yes	Yes	Yes
Schmitt Trigger	No	No	Yes	Yes	Yes
OUT_LOAD	No	No	No	Yes	Yes
COMBINE_REGISTER	Yes	Yes	N/A	N/A	N/A

Notes:

1. *No = Remains the same, Yes = Re-run the step, N/A = Not applicable*
2. *Skew control and input delay do not apply to IGLOO PLUS.*

Implementing I/Os in Actel Software

Actel Libero® Integrated Design Environment (IDE) is integrated with design entry tools such as the SmartGen macro builder, the ViewDraw schematic entry tool, and an HDL editor. It is also integrated with the synthesis and Designer tools. In this section, all necessary steps to implement the I/Os are discussed.

Design Entry

There are three ways to implement I/Os in a design:

1. Use the SmartGen macro builder to configure I/Os by generating specific I/O library macros and then instantiating them in top-level code. This is especially useful when creating I/O bus structures.
2. Use an I/O buffer cell in a schematic design.
3. Manually instantiate specific I/O macros in the top-level code.

If technology-specific macros, such as INBUF_LVCMOS33 and OUTBUF_PCI, are used in the HDL code or schematic, the user will not be able to change the I/O standard later on in Designer. If generic I/O macros are used, such as INBUF, OUTBUF, TRIBUF, CLKBUF, and BIBUF, the user can change the I/O standard using the Designer I/O Attribute Editor tool.

Using SmartGen for I/O Configuration

The SmartGen tool in Libero IDE provides a GUI-based method of configuring the I/O attributes. The user can select certain I/O attributes while configuring the I/O macro in SmartGen. The steps to configure an I/O macro with specific I/O attributes are as follows:

1. Open Libero IDE.
2. On the left hand side of the Catalog View, select **I/O**, as shown in Figure 8-2.

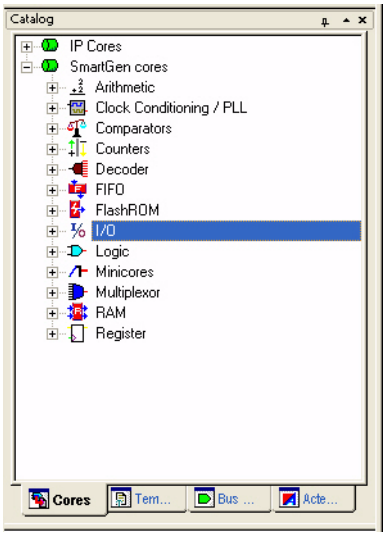


Figure 8-2 • **SmartGen Catalog**

3. Expand the I/O section and double-click one of the options (Figure 8-3).

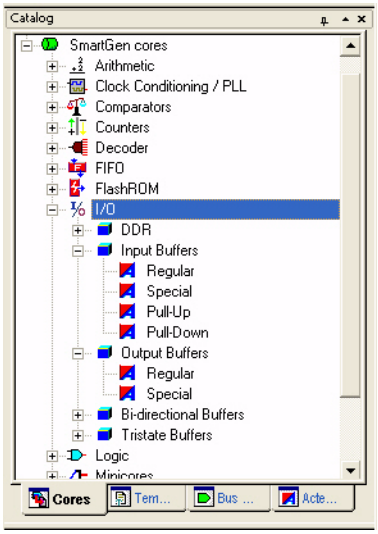


Figure 8-3 • **Expanded I/O Section**

4. Double-click any of the varieties. The I/O Create Core window opens (Figure 8-4).

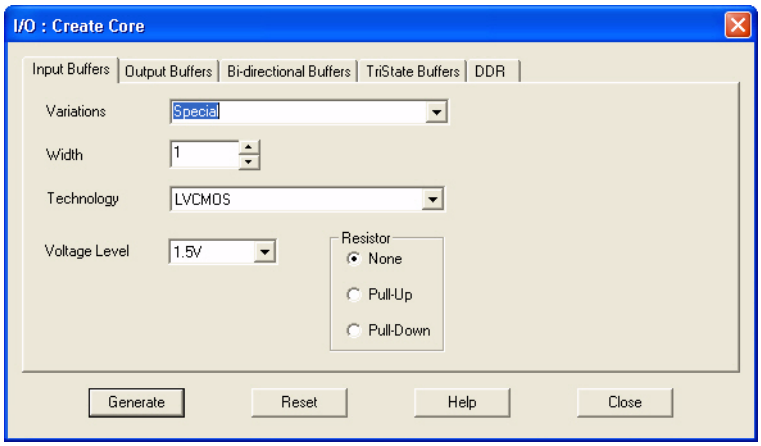


Figure 8-4 • **I/O Create Core Window**

As seen in Figure 8-4, there are five tabs to configure the I/O macro: Input Buffers, Output Buffers, Bidirectional Buffers, Tristate Buffers, and DDR.

Input Buffers

There are two variations: Regular and Special.

If the **Regular** variation is selected, only the Width (1 to 128) needs to be entered. The default value for Width is 1.

The **Special** variation has Width, Technology, Voltage Level, and Resistor Pull-Up/-Down options (see Figure 8-4). All the I/O standards and supply voltages (V_{CCI}) supported for the device family are available for selection.

Output Buffers

There are two variations: Regular and Special.

If the **Regular** variation is selected, only the Width (1 to 128) needs to be entered. The default value for Width is 1.

The **Special** variation has Width, Technology, Output Drive, and Slew Rate options.

Bidirectional Buffers

There are two variations: Regular and Special.

The **Regular** variation has Enable Polarity (Active High, Active Low) in addition to the Width option.

The **Special** variation has Width, Technology, Output Drive, Slew Rate, and Resistor Pull-Up/-Down options.

Tristate Buffers

Same as Bidirectional Buffers.

DDR

There are eight variations: DDR with Regular Input Buffers, Special Input Buffers, Regular Output Buffers, Special Output Buffers, Regular Tristate Buffers, Special Tristate Buffers, Regular Bidirectional Buffers, and Special Bidirectional Buffers.

These variations resemble the options of the previous I/O macro. For example, the Special Input Buffers variation has Width, Technology, Voltage Level, and Resistor Pull-Up/-Down options. DDR is not available on IGLOO PLUS devices.

5. Once the desired configuration is selected, click the **Generate** button. The Generate Core window opens (Figure 8-5).
6. Enter a name for the macro. Click **OK**. The core will be generated and saved to the appropriate location within the project files (Figure 8-6 on page 8-7).

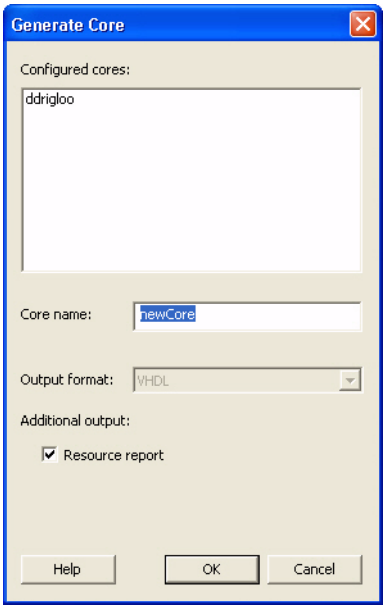


Figure 8-5 • **Generate Core Window**

7. Instantiate the I/O macro in the top-level code.

   The user must instantiate the DDR_REG or DDR_OUT macro in the design. Use SmartGen to generate both these macros and then instantiate them in your top level. To combine the DDR macros with the I/O, the following rules must be met:

Rules for the DDR I/O Function

- The fanout between an I/O pin (D or Y) and a DDR (DDR_REG or DDR_OUT) macro must be equal to one for the combining to happen on that pin.
- If a DDR_REG macro and a DDR_OUT macro are combined on the same bidirectional I/O, they must share the same clear signal.
- Registers will not be combined in an I/O in the presence of DDR combining on the same I/O.

Using the I/O Buffer Schematic Cell

Libero IDE includes the ViewDraw schematic entry tool. Using ViewDraw, the user can insert any supported I/O buffer cell in the top-level schematic. Figure 8-6 shows a top-level schematic with different I/O buffer cells. When synthesized, the netlist will contain the same I/O macro.

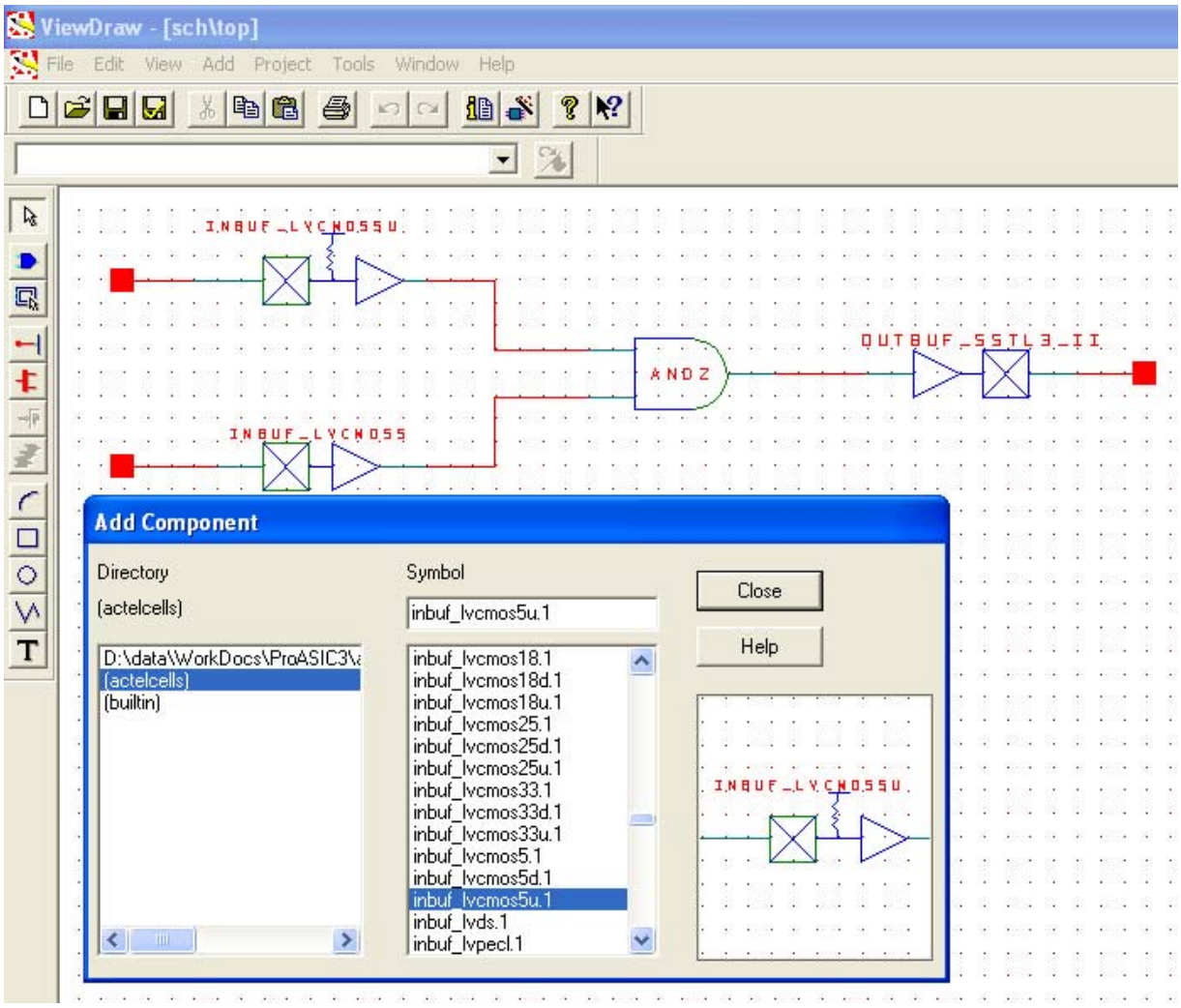


Figure 8-6 • **I/O Buffer Schematic Cell Usage**

Instantiating in HDL code

All the supported I/O macros can be instantiated in the top-level HDL code (refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide* for a detailed list of all I/O macros). The following is an example:

```
library ieee;
use ieee.std_logic_1164.all;
library proasic3e;

entity TOP is
  port(IN2, IN1 : in std_logic; OUT1 : out std_logic);
end TOP;

architecture DEF_ARCH of TOP is

  component INBUF_LVCMOS5U
    port(PAD : in std_logic := 'U'; Y : out std_logic);
  end component;

  component INBUF_LVCMOS5
    port(PAD : in std_logic := 'U'; Y : out std_logic);
  end component;

  component OUTBUF_SSTL3_II
    port(D : in std_logic := 'U'; PAD : out std_logic);
  end component;

  Other component …..

signal x, y, z…….other signals : std_logic;

begin

  I1 : INBUF_LVCMOS5U
    port map(PAD => IN1, Y =>x);
  I2 : INBUF_LVCMOS5
    port map(PAD => IN2, Y => y);
  I3 : OUTBUF_SSTL3_II
    port map(D => z, PAD => OUT1);

  other port mapping…

end DEF_ARCH;
```

Synthesizing the Design

Libero IDE integrates with the Synplify® synthesis tool. Other synthesis tools can also be used with Libero IDE. Refer to the *Actel Libero IDE User's Guide* or Libero IDE online help for details on how to set up the Libero IDE tool profile with synthesis tools from other vendors.

During synthesis, the following rules apply:

- Generic macros:
  - Users can instantiate generic INBUF, OUTBUF, TRIBUF, and BIBUF macros.
  - Synthesis will automatically infer generic I/O macros.
  - The default I/O technology for these macros is LVTTL.
  - Users will need to use the I/O Attribute Editor in Designer to change the default I/O standard if needed (see Figure 8-7 on page 8-9).
- Technology-specific I/O macros:
  - Technology-specific I/O macros, such as INBUF_LVCMO25 and OUTBUF_GTL25, can be instantiated in the design. Synthesis will infer these I/O macros in the netlist.

- The I/O standard of technology-specific I/O macros cannot be changed in the I/O Attribute Editor (see Figure 8-7).
- The user MUST instantiate differential I/O macros (LVDS/LVPECL) in the design. This is the only way to use these standards in the design.
- To implement the DDR I/O function, the user must instantiate a DDR_REG or DDR_OUT macro. This is the only way to use a DDR macro in the design.

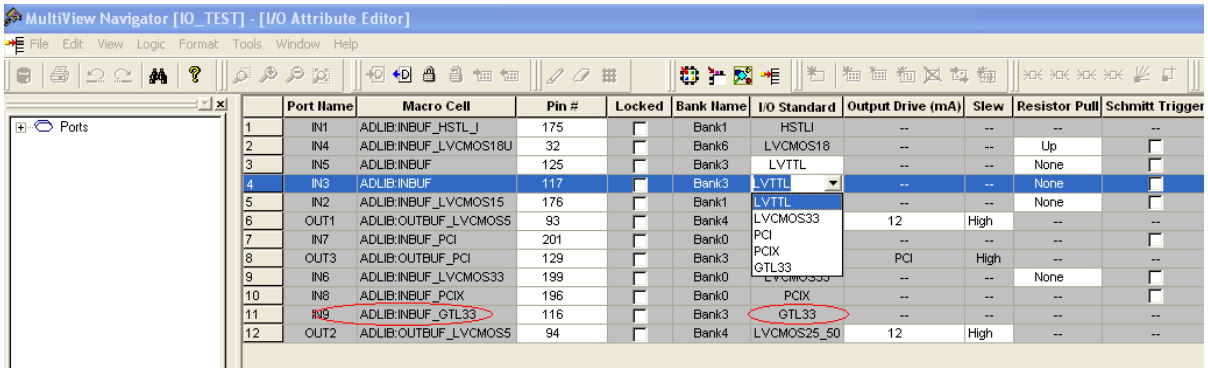


Figure 8-7 • **Assigning a Different I/O Standard to the Generic I/O Macro**

Performing Place-and-Route on the Design

The netlist created by the synthesis tool should now be imported into Designer and compiled. During Compile, the user can specify the I/O placement and attributes by importing the PDC file. The user can also specify the I/O placement and attributes using ChipPlanner and the I/O Attribute Editor, under MVN.

Defining I/O Assignments in the PDC File

A PDC file is a Tcl script file specifying physical constraints. This file can be imported to and exported from Designer.

Table 8-3 shows I/O assignment constraints supported in the PDC file.

Table 8-3 • **PDC I/O Constraints**

Command	Action	Example	Comment
I/O Banks Setting Constraints			

set_iobank	Sets the I/O supply voltage, V_{CCI}, and the input reference voltage, V_{REF}, for the specified I/O bank.	`set_iobank bankname [-vcci vcci_voltage] [-vref vref_voltage]`
		
		`set_iobank Bank7 -vcci 1.50 -vref 0.75`
			Must use in case of mixed I/O voltage (V_{CCI}) design

set_vref	Assigns a V_{REF} pin to a bank.	`set_vref -bank [bankname] [pinnum]`
		
		`set_vref -bank Bank0 685 704 723 742 761`
			Must use if voltage-referenced I/Os are used

Note: Refer to the Actel Libero IDE User's Guide for detailed rules on PDC naming and syntax conventions.

Table 8-3 • **PDC I/O Constraints (continued)**

Command	Action	Example	Comment

set_vref_defaults	Sets the default V_{REF} pins for the specified bank. This command is ignored if the bank does not need a V_{REF} pin.	`set_vref_defaults bankname`
		
		`set_vref_defaults bank2`	

I/O Attribute Constraint			

set_io	Sets the attributes of an I/O	`set_io portname`
		`[-pinname value]`
		`[-fixed value]`
		`[-iostd value]`
		`[-out_drive value]`
		`[-slew value]`
		`[-res_pull value]`
		`[-schmitt_trigger value]`
		`[-in_delay value]`
		`[-skew value]`
		`[-out_load value]`
		`[-register value]`
		
		`set_io IN2 -pinname 28`
		`-fixed yes -iostd LVCMOS15`
		`-out_drive 12 -slew high`
		`-RES_PULL None`
		`-SCHMITT_TRIGGER Off`
		`-IN_DELAY Off –skew off`
		`-REGISTER No`
			If the I/O macro is generic (e.g., INBUF) or technology-specific (INBUF_LVCMOS25), then all I/O attributes can be assigned using this constraint.
			If netlist has an I/O macro that specifies one of its attributes, that attribute cannot be changed using this constraint, though other attributes can be changed.
			Example: OUTBUF_S_24 (low slew, output drive 24 mA)
			Slew and output drive cannot be changed.

I/O Region Placement Constraints			

define_region	Defines either a rectangular region or a rectilinear region	`define_region`
		`-name [region_name]`
		`-type [region_type] x1 y1 x2 y2`
		
		`define_region -name test`
		`-type inclusive 0 15 2 29`
			If any number of I/Os must be assigned to a particular I/O region, such a region can be created with this constraint.

assign_region	Assigns a set of macros to a specified region	`assign_region [region name]`
		`[macro_name...]`
		
		`assign_region test U12`
			This constraint assigns I/O macros to the I/O regions. When assigning an I/O macro, PDC naming conventions must be followed if the macro name contains special characters; e.g., if the macro name is \\$1I19\\, the correct use of escape characters is \\\\\$1I19\\\\.

Note: Refer to the Actel Libero IDE User's Guide *for detailed rules on PDC naming and syntax conventions.*

Compiling the Design

During Compile, a PDC I/O constraint file can be imported along with the netlist file. If only the netlist file is compiled, certain I/O assignments need to be completed before proceeding to Layout. All constraints that can be entered in PDC can also be entered using ChipPlanner, I/O Attribute Editor, and PinEditor.

There are certain rules that must be followed in implementing I/O register combining and the I/O DDR macro (refer to the I/O Registers section of the handbook for the device that you are using and the "DDR" section on page 8-6 for details). Provided these rules are met, the user can enable or disable I/O register combining by using the PDC command `set_io portname -register yes|no` in the I/O Attribute Editor or selecting a check box in the Compile Options dialog box (see Figure 8-8). The Compile Options dialog box appears when the design is compiled for the first time. It can also be accessed by choosing **Options** > **Compile** during successive runs. I/O register combining is off by default. The PDC command overrides the setting in the Compile Options dialog box.

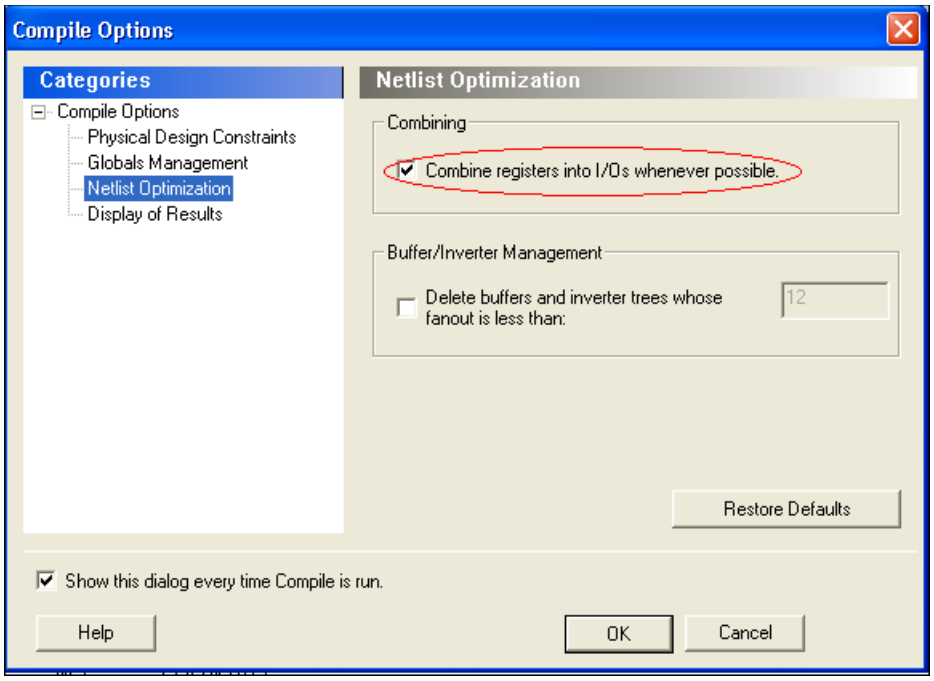


Figure 8-8 • **Setting Register Combining During Compile**

Understanding the Compile Report

The I/O bank report is generated during Compile and displayed in the log window. This report lists the I/O assignments necessary before Layout can proceed.

When Designer is started, the I/O Bank Assigner tool is run automatically if the Layout command is executed. The I/O Bank Assigner takes care of the necessary I/O assignments. However, these assignments can also be made manually with MVN or by importing the PDC file. Refer to the "Assigning Technologies and V_{REF} to I/O Banks" section on page 8-14 for further description.

The I/O bank report can also be extracted from Designer by choosing **Tools** > **Report** and setting the Report Type to **IOBank**.

This report has the following tables: I/O Function, I/O Technology, I/O Bank Resource Usage, and I/O Voltage Usage. This report is useful if the user wants to do I/O assignments manually.

I/O Function

Figure 8-9 shows an example of the I/O Function table included in the I/O bank report:

```
I/O Function:

    Type                            | w/o register  | w/ register   | w/ DDR register
    --------------------------------|---------------|---------------|----------------
    Input I/O                       | 7             | 0             | 1
    Output I/O                      | 1             | 1             | 0
    Bidirectional I/O               | 0             | 0             | 0
    Differential Input I/O Pairs    | 0             | 0             | 0
    Differential Output I/O Pairs   | 0             | 0             | 1
```

Figure 8-9 • **I/O Function Table**

This table lists the number of input I/Os, output I/Os, bidirectional I/Os, and differential input and output I/O pairs that use I/O and DDR registers.

Certain rules must be met to implement registered and DDR I/O functions (refer to the I/O Structures section of the handbook for the device you are using and the "DDR" section on page 8-6).

I/O Technology

The I/O Technology table (shown in Figure 8-10) gives the values of V_{CCI} and V_{REF} (reference voltage) for all the I/O standards used in the design. The user should assign these voltages appropriately.

```
I/O Technology:

                                    |   Voltages    |              I/Os
    --------------------------------|-------|-------|-------|--------|--------------
    I/O Standard(s)                 | Vcci  | Vref  | Input | Output | Bidirectional
    --------------------------------|-------|-------|-------|--------|--------------
    LVTTL                           | 3.30v | N/A   | 1     | 1      | 0
    LVCMOS33                        | 3.30v | N/A   | 1     | 0      | 0
    LVCMOS25_50                     | 2.50v | N/A   | 1     | 1      | 0
    LVCMOS18                        | 1.80v | N/A   | 1     | 0      | 0
    LVCMOS15                        | 1.50v | N/A   | 1     | 0      | 0
    PCIX                            | 3.30v | N/A   | 1     | 0      | 0
    LVDS                            | 2.50v | N/A   | 0     | 2      | 0
    SSTL3I (Input/Bidirectional)    | 3.30v | 1.50v | 1     | 0      | 0
    GTLP33 (Input/Bidirectional)    | 3.30v | 1.00v | 1     | 0      | 0
```

Figure 8-10 • **I/O Technology Table**

I/O Bank Resource Usage

This is an important portion of the report. The user must meet the requirements stated in this table. Figure 8-11 shows the I/O Bank Resource Usage table included in the I/O bank report:

```
I/O Bank Resource Usage:

          |   Voltages    | Single I/Os  | Diff I/O Pairs |        Vref I/Os
          |-------|-------|------|-------|-------|--------|------|-------|----------
          | Vcci  | Vref  | Used | Total | Used  | Total  | Used | Total | Vref Pins
    ------|-------|-------|------|-------|-------|--------|------|-------|----------
    Bank0 | N/A   | N/A   | 0    | 25    | 0     | 12     | N/A  | N/A   | N/A
    Bank1 | N/A   | N/A   | 0    | 15    | 0     | 7      | N/A  | N/A   | N/A
    Bank2 | N/A   | N/A   | 0    | 17    | 0     | 6      | N/A  | N/A   | N/A
    Bank3 | N/A   | N/A   | 0    | 16    | 0     | 7      | N/A  | N/A   | N/A
    Bank4 | N/A   | N/A   | 0    | 15    | 0     | 7      | N/A  | N/A   | N/A
    Bank5 | N/A   | N/A   | 0    | 22    | 0     | 10     | N/A  | N/A   | N/A
    Bank6 | N/A   | N/A   | 0    | 19    | 0     | 9      | N/A  | N/A   | N/A
    Bank7 | N/A   | N/A   | 0    | 18    | 0     | 7      | N/A  | N/A   | N/A

Warning: IOPRL1: 8 I/O Bank(s) have not been assigned any voltages.
         The I/O modules located in these banks cannot be assigned any I/O macro.
```

***Figure 8-11* • I/O Bank Resource Usage Table**

The example in Figure 8-11 shows that none of the I/O macros is assigned to the bank because more than one V_{CCI} is detected.

I/O Voltage Usage

The I/O Voltage Usage table provides the number of V_{REF} (E devices only) and V_{CCI} assignments required in the design. If the user decides to make I/O assignments manually (PDC or MVN), the issues listed in this table must be resolved before proceeding to Layout. As stated earlier, V_{REF} assignments must be made if there are any voltage-referenced I/Os.

Figure 8-12 shows the I/O Voltage Usage table included in the I/O bank report.

```
I/O Voltage Usage:

       Voltages    |      I/Os
    -------|-------|------|-------
     Vcci  | Vref  | Used | Total
    -------|-------|------|-------
     1.50v | N/A   | 1*   | 0
     1.80v | N/A   | 1*   | 0
     2.50v | N/A   | 4*   | 0
     3.30v | N/A   | 6*   | 0
     3.30v | 1.00v | 1*   | 0
     3.30v | 1.50v | 1*   | 0

Warning: IOPRL3: This design has infeasible I/O voltage requirement(s),
         which are indicated with a '*' in the I/O Voltage Usage table.
         Please consider importing a Physical Design Constraint (PDC) file or
         use the MultiView Navigator (MVN) to resolve the design's voltage requirements
         before running Layout.
```

***Figure 8-12* • I/O Voltage Usage Table**

The table in Figure 8-12 indicates that there are two voltage-referenced I/Os used in the design. Even though both of the voltage-referenced I/O technologies have the same V_{CCI} voltage, their V_{REF} voltages are different. As a result, two I/O banks are needed to assign the V_{CCI} and V_{REF} voltages.

In addition, there are six single-ended I/Os used that have the same V_{CCI} voltage. Since two banks are already assigned with the same V_{CCI} voltage and there are enough unused bonded I/Os in those banks, the user does not need to assign the same V_{CCI} voltage to another bank. The user needs to assign the other three V_{CCI} voltages to three more banks.

Assigning Technologies and V_{REF} to I/O Banks

Low-power flash devices offer a wide variety of I/O standards, including voltage-referenced standards. Before proceeding to Layout, each bank must have the required V_{CCI} voltage assigned for the corresponding I/O technologies used for that bank. The voltage-referenced standards require the use of a reference voltage (V_{REF}). This assignment can be done manually or automatically. The following sections describe this in detail.

Manually Assigning Technologies to I/O Banks

The user can import the PDC at this point and resolve this requirement. The PDC command is

```
set_iobank [bank name] –vcci [vcci value]
```

Another method is to use the I/O Bank Settings dialog box (**MVN** > **Edit** > **I/O Bank Settings**) to set up the V_{CCI} voltage for the bank (Figure 8-13).

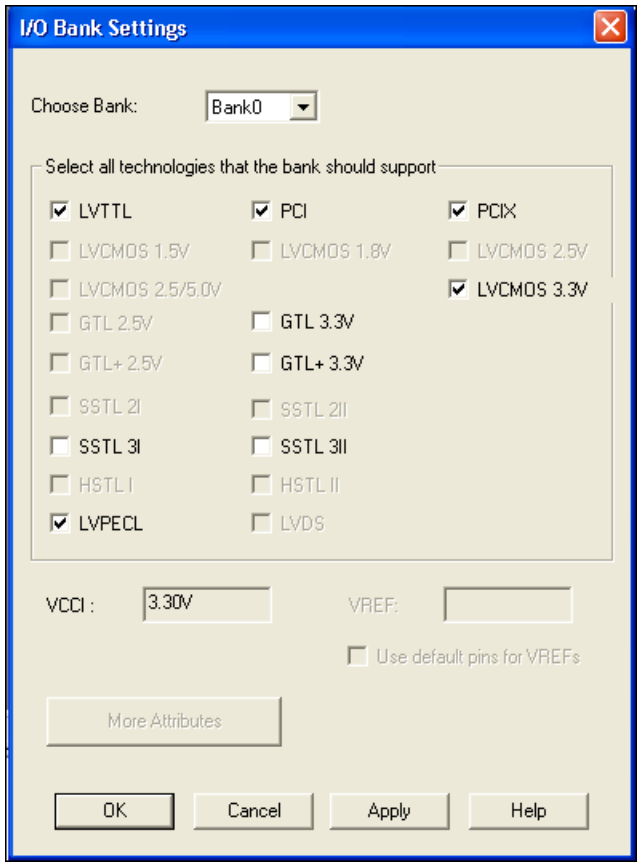


Figure 8-13 • **Setting V_{CCI} for a Bank**

The procedure is as follows:

1. Select the bank to which you want V_{CCI} to be assigned from the **Choose Bank** list.
2. Select the I/O standards for that bank. If you select any standard, the tool will automatically show all compatible standards that have a common V_{CCI} voltage requirement.
3. Click **Apply**.
4. Repeat steps 1–3 to assign V_{CCI} voltages to other banks. Refer to Figure 8-12 on page 8-13 to find out how many I/O banks are needed for V_{CCI} bank assignment.

Manually Assigning V_{REF} Pins

Voltage-referenced inputs require an input reference voltage (V_{REF}). The user must assign V_{REF} pins before running Layout. Before assigning a V_{REF} pin, the user must set a V_{REF} technology for the bank to which the pin belongs.

V_{REF} Rules for the Implementation of Voltage-Referenced I/O Standards

The V_{REF} rules are as follows:

1. Any I/O (except JTAG I/Os) can be used as a V_{REF} pin.
2. One V_{REF} pin can support up to 15 I/Os. It is recommended, but not required, that eight of them be on one side and seven on the other side (in other words, all 15 can still be on one side of V_{REF}).
3. SSTL3 (I) and (II): Up to 40 I/Os per north or south bank in any position
4. LVPECL / GTL+ 3.3 V / GTL 3.3 V: Up to 48 I/Os per north or south bank in any position
5. SSTL2 (I) and (II) / GTL+ 2.5 V / GTL 2.5 V: Up to 72 I/Os per north or south bank in any position.
6. V_{REF} minibanks partition rule: Each I/O bank is physically partitioned into V_{REF} minibanks. The V_{REF} pins within a V_{REF} minibank are interconnected internally, and consequently, only one V_{REF} voltage can be used within each V_{REF} minibank. If a bank does not require a V_{REF} signal, the V_{REF} pins of that bank are available as user I/Os.
7. The first V_{REF} minibank includes all I/Os starting from one end of the bank to the first power triple and eight more I/Os after the power triple. Therefore, the first V_{REF} minibank may contain (0 + 8), (2 + 8), (4 + 8), (6 + 8), or (8 + 8) I/Os.

   The second V_{REF} minibank is adjacent to the first V_{REF} minibank and contains eight I/Os, a power triple, and eight more I/Os after the triple. An analogous rule applies to all other V_{REF} minibanks but the last.

   The last V_{REF} minibank is adjacent to the previous one but contains eight I/Os, a power triple, and all I/Os left at the end of the bank. This bank may also contain (8 + 0), (8 + 2), (8 + 4), (8 + 6), or (8 + 8) available I/Os.

Example:

4 I/Os → Triple → 8 I/Os, 8 I/Os → Triple → 8 I/Os, 8 I/Os → Triple → 2 I/Os

i.e., minibank A = (4 + 8) I/Os, minibank B = (8 + 8) I/Os, minibank C = (8 + 2) I/Os

Assigning the V_{REF} Voltage to a Bank

When importing the PDC file, the V_{REF} voltage can be assigned to the I/O bank. The PDC command is as follows:

```
set_iobank -vref [value]
```

Another method for assigning V_{REF} is by using **MVN** > **Edit** > **I/O Bank Settings** (Figure 8-14 on page 8-16).

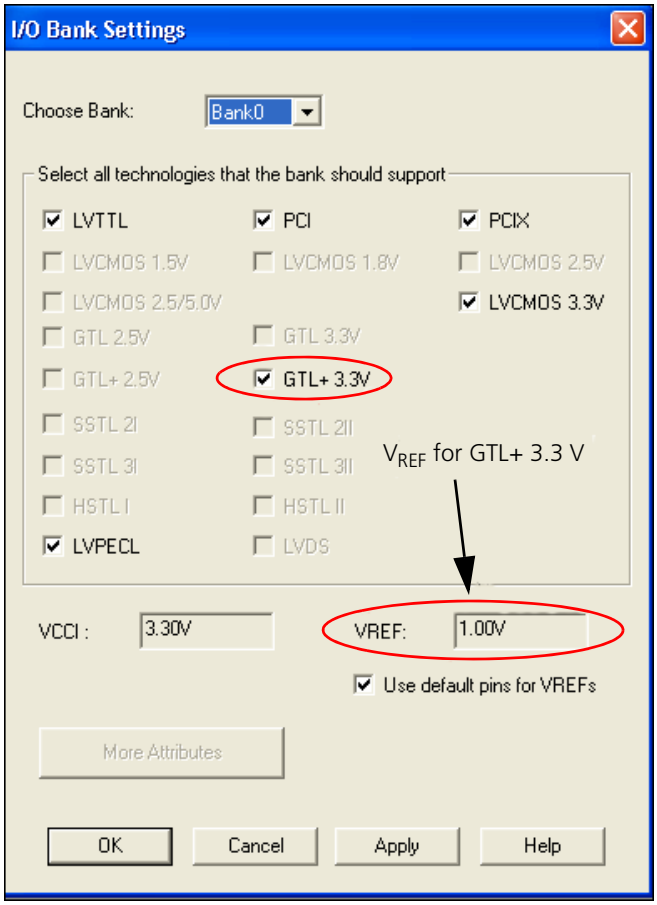


Figure 8-14 **• Selecting V_{REF} Voltage for the I/O Bank**

Assigning V_{REF} Pins for a Bank

The user can use default pins for V_{REF}. In this case, select the **Use default pins for V_{REF}s** check box (Figure 8-14). This option guarantees full V_{REF} coverage of the bank. The equivalent PDC command is as follows:

```
set_vref_default [bank name]
```

To be able to choose V_{REF} pins, adequate V_{REF} pins must be created to allow legal placement of the compatible voltage-referenced I/Os.

To assign V_{REF} pins manually, the PDC command is as follows:

```
set_vref –bank [bank name] [package pin numbers]
```

For ChipPlanner/PinEditor to show the range of a V_{REF} pin, perform the following steps:

1. Assign V_{CCI} to a bank using **MVN** > **Edit** > **I/O Bank Settings**.
2. Open **ChipPlanner**. Zoom in on an I/O package pin in that bank.
3. Highlight the pin and then right-click. Choose **Use Pin for V_{REF}**.

4. Right-click and then choose **Show V_{REF} range**. All the pins covered by that V_{REF} pin will be highlighted (Figure 8-15).

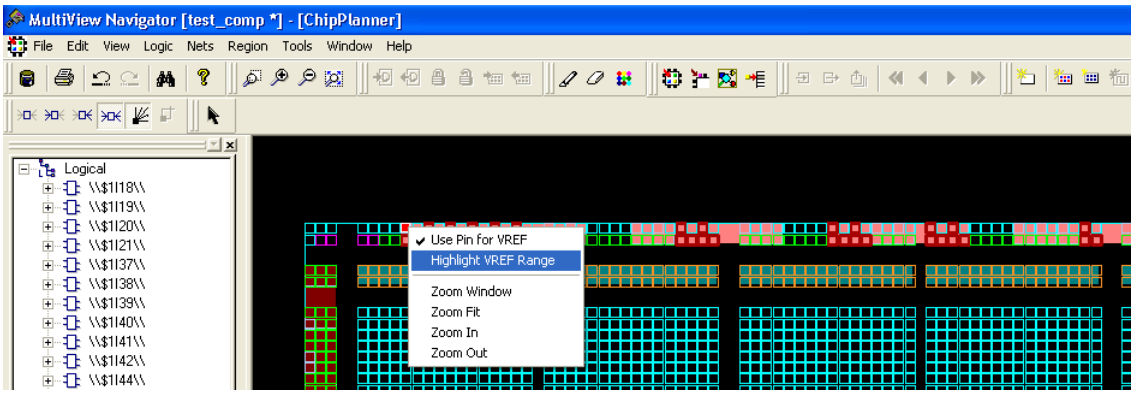


***Figure 8-15* • V_{REF} Range**

Using PinEditor or ChipPlanner, V_{REF} pins can also be assigned (Figure 8-16).

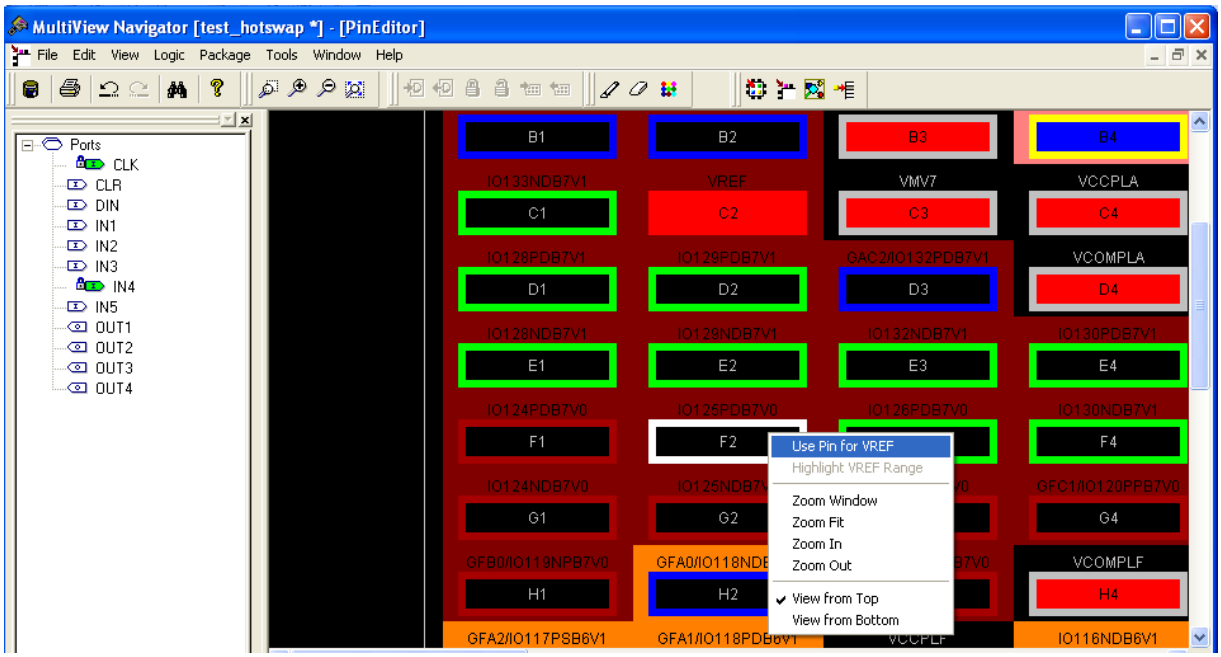


***Figure 8-16* • Assigning V_{REF} from PinEditor**

To unassign a V_{REF} pin:

1. Select the pin to unassign.
2. Right-click and choose **Use Pin for V_{REF}**. The check mark next to the command disappears. The V_{REF} pin is now a regular pin.

Resetting the pin may result in unassigning I/O cores, even if they are locked. In this case, a warning message appears so you can cancel the operation.

After you assign the V_{REF} pins, right-click a V_{REF} pin and choose **Highlight VREF Range** to see how many I/Os are covered by this pin. To unhighlight the range, choose **Unhighlight All** from the **Edit** menu.

Automatically Assigning Technologies to I/O Banks

The I/O Bank Assigner (IOBA) tool runs automatically when you run Layout. You can also use this tool from within the MultiView Navigator (Figure 8-18). The IOBA tool automatically assigns technologies and V_{REF} pins (if required) to every I/O bank that does not currently have any technologies assigned to it. This tool is available when at least one I/O bank is unassigned.

To automatically assign technologies to I/O banks, choose **I/O Bank Assigner** from the **Tools** menu (or click the I/O Bank Assigner's toolbar button, shown in Figure 8-17).

Figure 8-17 **• I/O Bank Assigner's Toolbar Button**

Messages will appear in the Output window informing you when the automatic I/O bank assignment begins and ends. If the assignment is successful, the message "I/O Bank Assigner completed successfully" appears in the Output window, as shown in Figure 8-18.

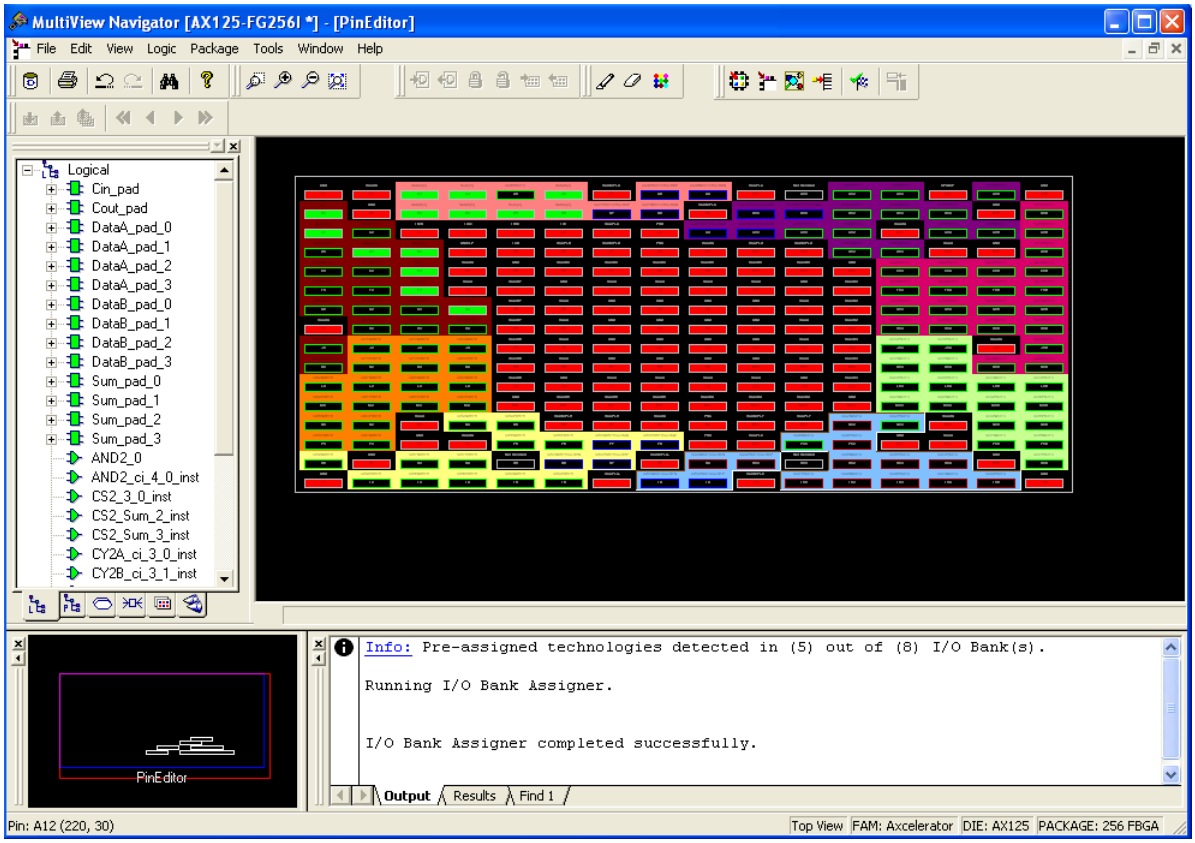


Figure 8-18 **• I/O Bank Assigner Displays Messages in Output Window**

If the assignment is not successful, an error message appears in the Output window.

To undo the I/O bank assignments, choose **Undo** from the **Edit** menu. Undo removes the I/O technologies assigned by the IOBA. It does not remove the I/O technologies previously assigned.

To redo the changes undone by the Undo command, choose **Redo** from the **Edit** menu.

To clear I/O bank assignments made before using the Undo command, manually unassign or reassign I/O technologies to banks. To do so, choose **I/O Bank Settings** from the **Edit** menu to display the I/O Bank Settings dialog box.

Conclusion

IGLOO and ProASIC3 support for multiple I/O standards minimizes board-level components and makes possible a wide variety of applications. The Actel Designer software, integrated with Actel Libero IDE, presents a clear visual display of I/O assignments, allowing users to verify I/O and board-level design requirements before programming the device. The device I/O features and functionalities ensure board designers can produce low-cost and low-power FPGA applications fulfilling the complexities of contemporary design needs.

Related Documents

Handbook Documents

DDR for Actel's Low-Power Flash Devices

http://www.actel.com/documents/LPD_DDR_HBs.pdf

*Flash*Freeze Technology and Low-Power Modes in IGLOO and ProASIC3L Devices*

http://www.actel.com/documents/LPD_FlashFreeze_HBs.pdf

Global Resources in Actel Low-Power Flash Devices

http://www.actel.com/documents/LPD_Global_HBs.pdf

I/O Structures in IGLOO and ProASIC3 Devices

http://www.actel.com/documents/IGLOO_PA3_IO_HBs.pdf

I/O Structures in IGLOO PLUS Devices

http://www.actel.com/documents/IGLOOPLUS_IO_HBs.pdf

I/O Structures in IGLOOe and ProASIC3E Devices

http://www.actel.com/documents/IGLOOe_PA3E_IO_HBs.pdf

Pin Descriptions

http://www.actel.com/documents/LPD_PinDescriptions_HBs.pdf

Power-Up/-Down Behavior of Low-Power Flash Devices

http://www.actel.com/documents/LPD_PowerUp_HBs.pdf

ProASIC3/E SSO and Pin Placement and Guidelines

http://www.actel.com/documents/PA3_E_SSO_HBs.pdf

User's Guides

Actel Libero IDE User's Guide

http://www.actel.com/documents/libero_ug.pdf

IGLOO, Fusion, and ProASIC3 Macro Library Guide

http://www.actel.com/documents/pa3_libguide_ug.pdf

SmartGen Core Reference Guide

http://www.actel.com/documents/genguide_ug.pdf

Part Number and Revision Date

This document contains content extracted from the Device Architecture section of the datasheet, combined with content previously published as an application note describing features and functions of the device. To improve usability for customers, the device architecture information has now been combined with usage information, to reduce duplication and possible inconsistencies in published information. No technical changes were made to the datasheet content unless explicitly listed. Changes to the application note content were made only to be consistent with existing datasheet information.

Part Number 51700094-026-1

Revised June 2008

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v1.2)	Page
v1.1 (March 2008)	The following changes were made to the family descriptions in Table 8-1 · Low-Power Flash Families: • ProASIC3L was updated to include 1.5 V. • The number of PLLs for ProASIC3E was changed from five to six.	8-2
v1.0 (January 2008)	This document was previously part of the I/O Structures in IGLOO and ProASIC3 Devices document. The content was separated and made into a new document.	N/A
	Table 8-2 · Designer State (resulting from I/O attribute modification) was updated to include note 2 for IGLOO PLUS.	8-3

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9 – DDR for Actel's Low-Power Flash Devices

Introduction

The I/Os in IGLOO,® Fusion, and ProASIC®3 devices support Double Data Rate (DDR) mode. In this mode, new data is present on every transition (or clock edge) of the clock signal. This mode doubles the data transfer rate compared with Single Data Rate (SDR) mode, where new data is present on one transition (or clock edge) of the clock signal. Low-power flash devices have DDR circuitry built into the I/O tiles. I/Os are configured to be DDR receivers or transmitters by instantiating the appropriate special macros (examples shown in Figure 9-4 on page 9-6 and Figure 9-5 on page 9-7) and buffers (DDR_OUT or DDR_REG) in the RTL design. This document discusses the options the user can choose to configure the I/Os in this mode and how to instantiate them in the design.

Double Data Rate (DDR) Architecture

Low-power flash devices support 350 MHz DDR inputs and outputs. In DDR mode, new data is present on every transition of the clock signal. Clock and data lines have identical bandwidths and signal integrity requirements, making them very efficient for implementing very high-speed systems. High-speed DDR interfaces can be implemented using LVDS. In IGLOOe and ProASIC3E devices, DDR interfaces can also be implemented using the HSTL, SSTL, and LVPECL I/O standards. The DDR feature is primarily implemented in the FPGA core periphery and is not tied to a specific I/O technology or limited to any I/O standard.

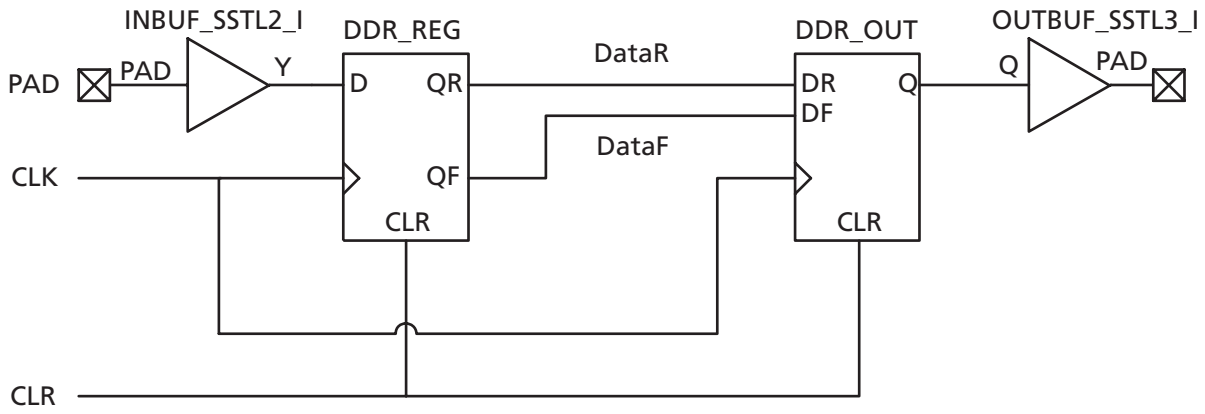

Figure 9-1 • **DDR Support in Low-Power Flash Devices**

DDR Support in Low-Power Devices

The low-power flash families listed in Table 9-1 support the DDR feature and the functions described in this document.

Table 9-1 • **Low-Power Flash Families**

Family[1]	Description	Timing Numbers[2]
IGLOO	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*IGLOO DC and Switching Characteristics*
IGLOOe	IGLOO devices enhanced with higher density, five additional PLLs, and additional I/O standards	*IGLOOe DC and Switching Characteristics*
ProASIC3L	Low-power, high-performance 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*ProASIC3L DC and Switching Characteristics*
ProASIC3	Low-power, high-performance 1.5 V FPGAs	*ProASIC3 DC and Switching Characteristics*
ProASIC3E	ProASIC3 enhanced with higher density, six additional PLLs, and additional I/O standards	*ProASIC3E DC and Switching Characteristics*
ProASIC3 Automotive	Low-power, high-performance FPGAs qualified for Automotive applications	*Automotive ProASIC3 DC and Switching Characteristics*
Fusion	Low-power mixed-signal Programmable System Chip (PSC)	*Fusion DC and Power Characteristics*

Notes:

1. *The family names are linked to the appropriate product brief.*
2. *The timing number links go to the relevant timing numbers in the datasheet.*

Actel's low-power flash devices (listed in Table 9-1) provide a selection of secure, low-power, live-at-power-up, single-chip solutions. The nonvolatile flash-based devices do not require a boot PROM and incorporate FlashLock® technology, which provides a unique combination of reprogrammability and design security without external overhead. Only low-power flash FPGAs can offer these advantages.

Actel IGLOO FPGAs are the only 1.2 V ultra-low-power programmable logic devices (PLDs) and consume 30% less static power and over 50% less dynamic power than PLD alternatives.

Flash*Freeze technology used in IGLOO and ProASIC3L devices enables easy entry to and exit from the ultra-low power mode, which consumes as little as 5 µW, while retaining SRAM and register data. Flash*Freeze technology simplifies power management through I/O and clock management without the need to turn off voltages, I/Os, or clocks at the system level. Entering and exiting Flash*Freeze mode takes less than 1 µs.

The Actel Fusion® family, based on the highly successful ProASIC3 flash FPGA architecture, has been designed as a high-performance, mixed-signal Programmable System Chip. Fusion supports many peripherals, including embedded flash memory, analog-to-digital Converter (ADC), high-drive outputs, RC and crystal oscillators, and real-time counter (RTC). The total available on-chip memory, including the flash array blocks, is greater than that found in SRAM FPGAs.

IGLOO Terminology

In documentation, the term IGLOO families or IGLOO devices refers to all IGLOO families as listed in Table 9-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

ProASIC3 Terminology

In documentation, the term ProASIC3 families or ProASIC3 devices refers to all ProASIC3 families as listed in Table 9-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

I/O Cell Architecture

Low-power flash devices support DDR in the I/O cells in four different modes: Input, Output, Tristate, and Bidirectional pins. For each mode, different I/O standards are supported, with most I/O standards having special sub-options. Refer to Table 9-2 for a sample of the available I/O options. Additional I/O options can be found in the relevant family datasheet.

Table 9-2 • **DDR I/O Options**

DDR Register Type	I/O Type	I/O Standard	Sub-Options	Comments
Receive Register	Input	Normal	None	3.3 V TTL (default)
		LVCMOS	Voltage	1.5 V, 1.8 V, 2.5 V, 5 V (1.5 V default)
			Pull-Up	None (default)
		PCI/PCI-X	None	
		GTL/GTL+	Voltage	2.5 V, 3.3 V (3.3 V default)
		HSTL	Class	I / II (I default)
		SSTL2/SSTL3	Class	I / II (I default)
		LVPECL	None	
		LVDS	None	
Transmit Register	Output	Normal	None	3.3 V TTL (default)
		LVTTL	Output Drive	2, 4, 6, 8, 12, 16, 24, 36 mA (8 mA default)
			Slew Rate	Low/high (high default)
		LVCMOS	Voltage	1.5 V, 1.8 V, 2.5 V, 5 V (1.5 V default)
		PCI/PCI-X	None	
		GTL/GTL+	Voltage	1.8 V, 2.5 V, 3.3 V (3.3 V default)
		HSTL	Class	I / II (I default)
		SSTL2/SSTL3	Class	I / II (I default)
		LVPECL	None	
		LVDS	None	

Table 9-2 • **DDR I/O Options (continued)**

DDR Register Type	I/O Type	I/O Standard	Sub-Options	Comments
Transmit Register (continued)	Tristate Buffer	Normal	Enable Polarity	Low/high (low default)
		LVTTL	Output Drive	2, 4, 6, 8, 12,16, 24, 36 mA (8 mA default)
			Slew Rate	Low/high (high default)
			Enable Polarity	Low/high (low default)
			Pull-Up/-Down	None (default)
		LVCMOS	Voltage	1.5 V, 1.8 V, 2.5 V, 5 V (1.5 V default)
			Output Drive	2, 4, 6, 8, 12, 16, 24, 36 mA (8 mA default)
			Slew Rate	Low/high (high default)
			Enable Polarity	Low/high (low default)
			Pull-Up/-Down	None (default)
		PCI/PCI-X	Enable Polarity	Low/high (low default)
		GTL/GTL+	Voltage	1.8 V, 2.5 V, 3.3 V (3.3 V default)
			Enable Polarity	Low/high (low default)
		HSTL	Class	I / II (I default)
			Enable Polarity	Low/high (low default)
		SSTL2/SSTL3	Class	I / II (I default)
			Enable Polarity	Low/high (low default)
	Bidirectional Buffer	Normal	Enable Polarity	Low/high (low default)
		LVTTL	Output Drive	2, 4, 6, 8, 12, 16, 24, 36 mA (8 mA default)
			Slew Rate	Low/high (high default)
			Enable Polarity	Low/high (low default)
			Pull-Up/-Down	None (default)
		LVCMOS	Voltage	1.5 V, 1.8 V, 2.5 V, 5 V (1.5 V default)
			Enable Polarity	Low/high (low default)
			Pull-Up	None (default)
		PCI/PCI-X	None	
			Enable Polarity	Low/high (low default)
		GTL/GTL+	Voltage	1.8 V, 2.5 V, 3.3 V (3.3 V default)
			Enable Polarity	Low/high (low default)
		HSTL	Class	I / II (I default)
			Enable Polarity	Low/high (low default)
		SSTL2/SSTL3	Class	I / II (I default)
			Enable Polarity	Low/high (low default)

Input Support for DDR

The basic structure to support a DDR input is shown in Figure 9-2. Three input registers are used to capture incoming data, which is presented to the core on each rising edge of the I/O register clock. Each I/O tile supports DDR inputs.

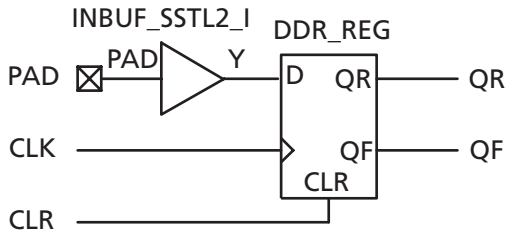

Figure 9-2 • **DDR Input Register Support in Low-Power Flash Devices**

Output Support for DDR

The basic DDR output structure is shown in Figure 9-1 on page 9-1. New data is presented to the output every half clock cycle.

Note: DDR macros and I/O registers do not require additional routing. The combiner automatically recognizes the DDR macro and pushes its registers to the I/O register area at the edge of the chip. The routing delay from the I/O registers to the I/O buffers is already taken into account in the DDR macro.

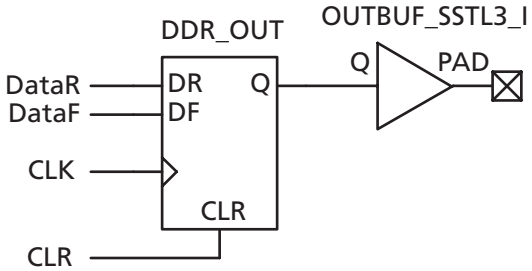

Figure 9-3 • **DDR Output Register (SSTL3 Class I)**

Instantiating DDR Registers

Using SmartGen is the simplest way to generate the appropriate RTL files for use in the design. Figure 9-4 shows an example of using SmartGen to generate a DDR SSTL2 Class I input register. SmartGen provides the capability to generate all of the DDR I/O cells as described. The user, through the graphical user interface, can select from among the many supported I/O standards. The output formats supported are Verilog, VHDL, and EDIF.

Figure 9-5 on page 9-7 through Figure 9-8 on page 9-10 show the I/O cell configured for DDR using SSTL2 Class I technology. For each I/O standard, the I/O pad is buffered by a special primitive that indicates the I/O standard type.

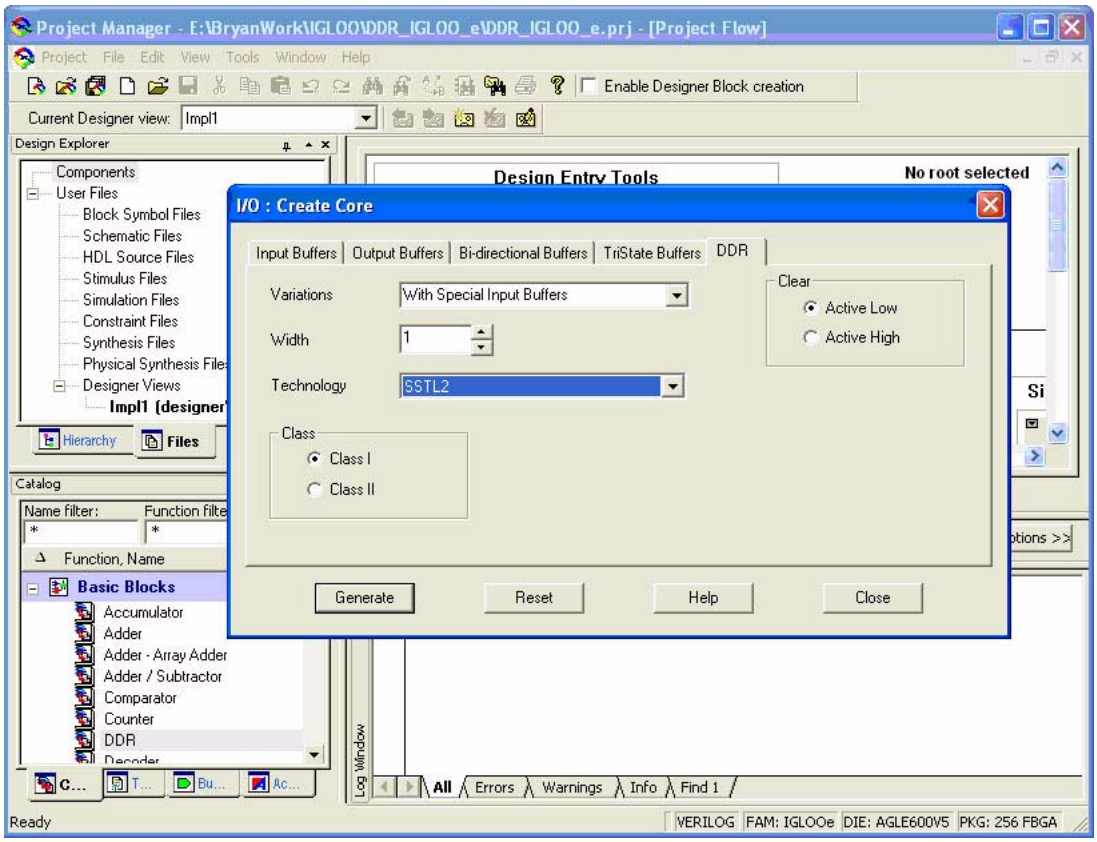

Figure 9-4 • **Example of Using SmartGen to Generate a DDR SSTL2 Class I Input Register**

DDR Input Register

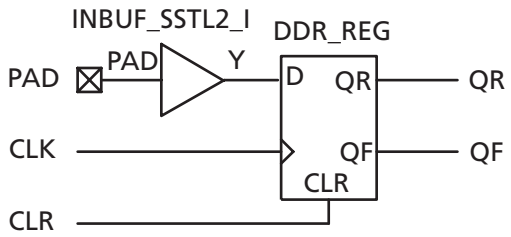

Figure 9-5 • **DDR Input Register (SSTL2 Class I)**

The corresponding structural representations, as generated by SmartGen, are shown below:

Verilog

```
module DDR_InBuf_SSTL2_I(PAD,CLR,CLK,QR,QF);

input   PAD, CLR, CLK;
output  QR, QF;

wire Y;

  INBUF_SSTL2_I INBUF_SSTL2_I_0_inst(.PAD(PAD),.Y(Y));
  DDR_REG DDR_REG_0_inst(.D(Y),.CLK(CLK),.CLR(CLR),.QR(QR),.QF(QF));

endmodule
```

VHDL

```
library ieee;
use ieee.std_logic_1164.all;
--The correct library will be inserted automatically by SmartGen
library proasic3; use proasic3.all;
--library fusion; use fusion.all;
--library igloo; use igloo.all;

entity DDR_InBuf_SSTL2_I is
  port(PAD, CLR, CLK : in std_logic;  QR, QF : out std_logic) ;
end DDR_InBuf_SSTL2_I;

architecture DEF_ARCH of  DDR_InBuf_SSTL2_I is

  component INBUF_SSTL2_I
    port(PAD : in std_logic := 'U'; Y : out std_logic) ;
  end component;

  component DDR_REG
    port(D, CLK, CLR : in std_logic := 'U'; QR, QF : out std_logic) ;
  end component;

signal Y : std_logic ;

begin

  INBUF_SSTL2_I_0_inst : INBUF_SSTL2_I
  port map(PAD => PAD, Y => Y);
  DDR_REG_0_inst : DDR_REG
  port map(D => Y, CLK => CLK, CLR => CLR, QR => QR, QF => QF);

end DEF_ARCH;
```

DDR Output Register

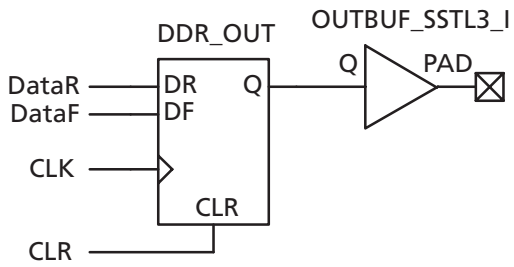

Figure 9-6 • **DDR Output Register (SSTL3 Class I)**

Verilog

```
module DDR_OutBuf_SSTL3_I(DataR,DataF,CLR,CLK,PAD);

input   DataR, DataF, CLR, CLK;
output  PAD;

wire Q, VCC;

  VCC VCC_1_net(.Y(VCC));
  DDR_OUT DDR_OUT_0_inst(.DR(DataR),.DF(DataF),.CLK(CLK),.CLR(CLR),.Q(Q));
  OUTBUF_SSTL3_I OUTBUF_SSTL3_I_0_inst(.D(Q),.PAD(PAD));

endmodule
```

VHDL

```
library ieee;
use ieee.std_logic_1164.all;
library proasic3; use proasic3.all;

entity DDR_OutBuf_SSTL3_I is
  port(DataR, DataF, CLR, CLK : in std_logic;  PAD : out std_logic) ;
end DDR_OutBuf_SSTL3_I;

architecture DEF_ARCH of  DDR_OutBuf_SSTL3_I is

  component DDR_OUT
    port(DR, DF, CLK, CLR : in std_logic := 'U'; Q : out std_logic) ;
  end component;

  component OUTBUF_SSTL3_I
    port(D : in std_logic := 'U'; PAD : out std_logic) ;
  end component;

  component VCC
    port( Y : out std_logic);
  end component;

signal Q, VCC_1_net : std_logic ;

begin

  VCC_2_net : VCC port map(Y => VCC_1_net);
  DDR_OUT_0_inst : DDR_OUT
  port map(DR => DataR, DF => DataF, CLK => CLK, CLR => CLR, Q => Q);
  OUTBUF_SSTL3_I_0_inst : OUTBUF_SSTL3_I
  port map(D => Q, PAD => PAD);

end DEF_ARCH;
```

DDR Tristate Output Register

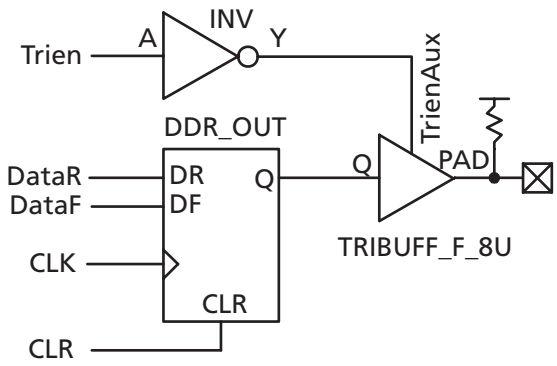

Figure 9-7 • **DDR Tristate Output Register, LOW Enable, 8 mA, Pull-Up (LVTTL)**

Verilog

```
module DDR_TriStateBuf_LVTTL_8mA_HighSlew_LowEnb_PullUp(DataR, DataF, CLR, CLK, Trien,
  PAD);

input   DataR, DataF, CLR, CLK, Trien;
output  PAD;

wire TrienAux, Q;

  INV Inv_Tri(.A(Trien),.Y(TrienAux));
  DDR_OUT DDR_OUT_0_inst(.DR(DataR),.DF(DataF),.CLK(CLK),.CLR(CLR),.Q(Q));
  TRIBUFF_F_8U TRIBUFF_F_8U_0_inst(.D(Q),.E(TrienAux),.PAD(PAD));

endmodule
```

VHDL

```
library ieee;
use ieee.std_logic_1164.all;
library proasic3; use proasic3.all;

entity DDR_TriStateBuf_LVTTL_8mA_HighSlew_LowEnb_PullUp is
  port(DataR, DataF, CLR, CLK, Trien : in std_logic;  PAD : out std_logic) ;
end DDR_TriStateBuf_LVTTL_8mA_HighSlew_LowEnb_PullUp;

architecture DEF_ARCH of DDR_TriStateBuf_LVTTL_8mA_HighSlew_LowEnb_PullUp is

  component INV
    port(A : in std_logic := 'U'; Y : out std_logic) ;
  end component;

  component DDR_OUT
    port(DR, DF, CLK, CLR : in std_logic := 'U'; Q : out std_logic) ;
  end component;

  component TRIBUFF_F_8U
    port(D, E : in std_logic := 'U'; PAD : out std_logic) ;
  end component;

signal TrienAux, Q : std_logic ;

begin

  Inv_Tri : INV
```

```
  port map(A => Trien, Y => TrienAux);
  DDR_OUT_0_inst : DDR_OUT
  port map(DR => DataR, DF => DataF, CLK => CLK, CLR => CLR, Q => Q);
  TRIBUFF_F_8U_0_inst : TRIBUFF_F_8U
  port map(D => Q, E => TrienAux, PAD => PAD);

end DEF_ARCH;
```

DDR Bidirectional Buffer

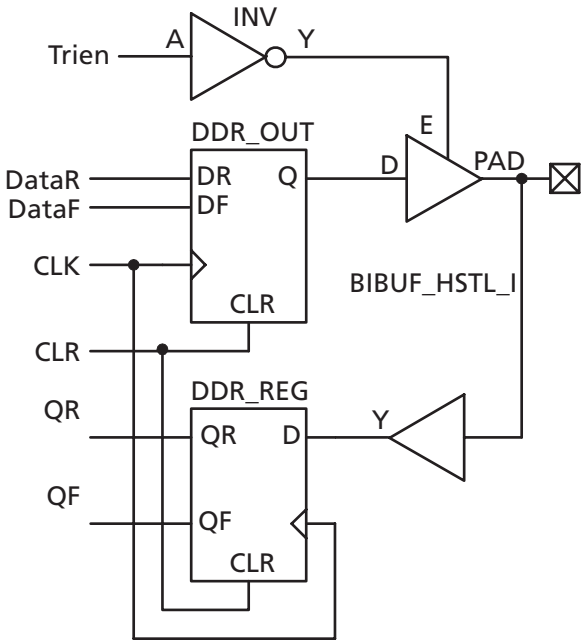

Figure 9-8 • **DDR Bidirectional Buffer, LOW Output Enable (HSTL Class II)**

Verilog

```
module DDR_BiDir_HSTL_I_LowEnb(DataR,DataF,CLR,CLK,Trien,QR,QF,PAD);

input   DataR, DataF, CLR, CLK, Trien;
output  QR, QF;
inout   PAD;

wire TrienAux, D, Q;

  INV Inv_Tri(.A(Trien), .Y(TrienAux));
  DDR_OUT DDR_OUT_0_inst(.DR(DataR),.DF(DataF),.CLK(CLK),.CLR(CLR),.Q(Q));
  DDR_REG DDR_REG_0_inst(.D(D),.CLK(CLK),.CLR(CLR),.QR(QR),.QF(QF));
  BIBUF_HSTL_I BIBUF_HSTL_I_0_inst(.PAD(PAD),.D(Q),.E(TrienAux),.Y(D));

endmodule
```

VHDL

```
library ieee;
use ieee.std_logic_1164.all;
library proasic3; use proasic3.all;

entity DDR_BiDir_HSTL_I_LowEnb is
  port(DataR, DataF, CLR, CLK, Trien : in std_logic; QR, QF : out std_logic;
    PAD : inout std_logic) ;
end DDR_BiDir_HSTL_I_LowEnb;

architecture DEF_ARCH of  DDR_BiDir_HSTL_I_LowEnb is

  component INV
    port(A : in std_logic := 'U'; Y : out std_logic) ;
  end component;

  component DDR_OUT
    port(DR, DF, CLK, CLR : in std_logic := 'U'; Q : out std_logic) ;
  end component;

  component DDR_REG
    port(D, CLK, CLR : in std_logic := 'U'; QR, QF : out std_logic) ;
  end component;

  component BIBUF_HSTL_I
    port(PAD : inout std_logic := 'U'; D, E : in std_logic := 'U'; Y : out std_logic) ;
  end component;

signal TrienAux, D, Q : std_logic ;

begin

  Inv_Tri : INV
  port map(A => Trien, Y => TrienAux);
  DDR_OUT_0_inst : DDR_OUT
  port map(DR => DataR, DF => DataF, CLK => CLK, CLR => CLR, Q => Q);
  DDR_REG_0_inst : DDR_REG
  port map(D => D, CLK => CLK, CLR => CLR, QR => QR, QF => QF);
  BIBUF_HSTL_I_0_inst : BIBUF_HSTL_I
  port map(PAD => PAD, D => Q, E => TrienAux, Y => D);

end DEF_ARCH;
```

Design Example

Figure 9-9 shows a simple example of a design using both DDR input and DDR output registers. The user can copy the HDL code in Actel Libero® Integrated Design Environment (IDE) and go thorough the design flow. Figure 9-10 and Figure 9-11 on page 9-13 show the netlist and ChipPlanner views of the ddr_test design. Diagrams may vary slightly for different families.

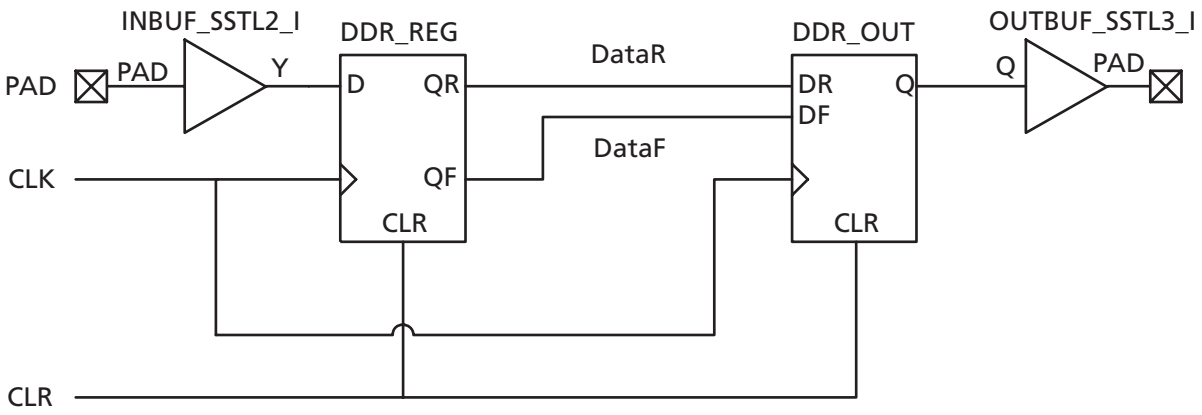

Figure 9-9 • **Design Example**

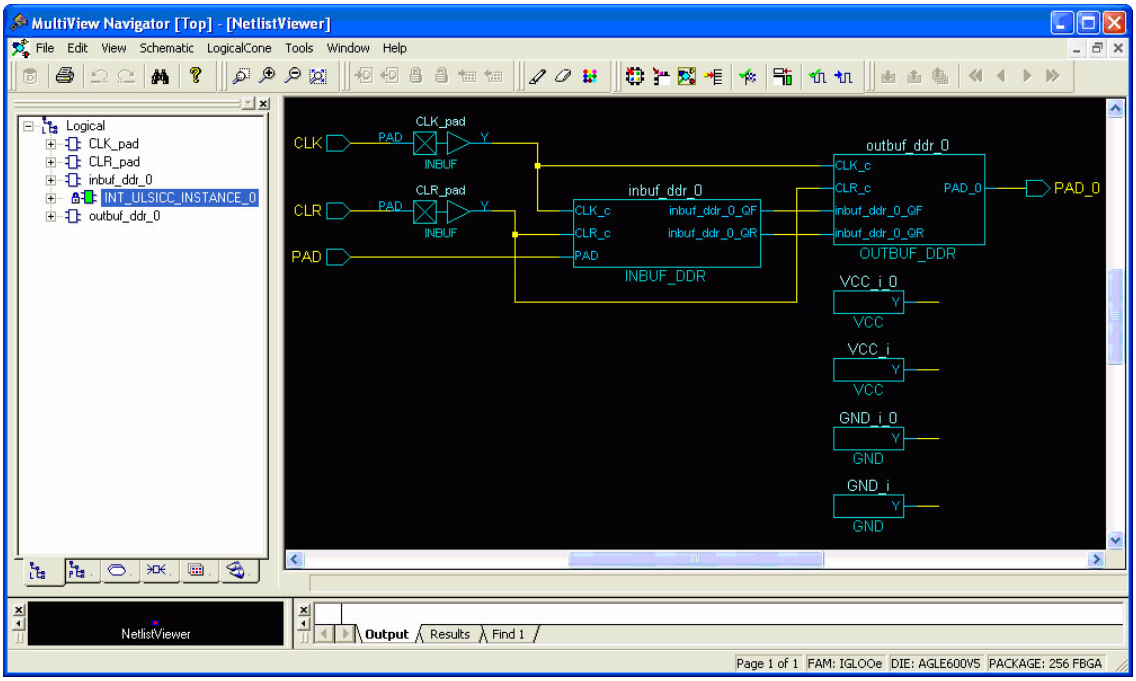

Figure 9-10 • **DDR Test Design as Seen by NetlistViewer for IGLOO/e Devices**

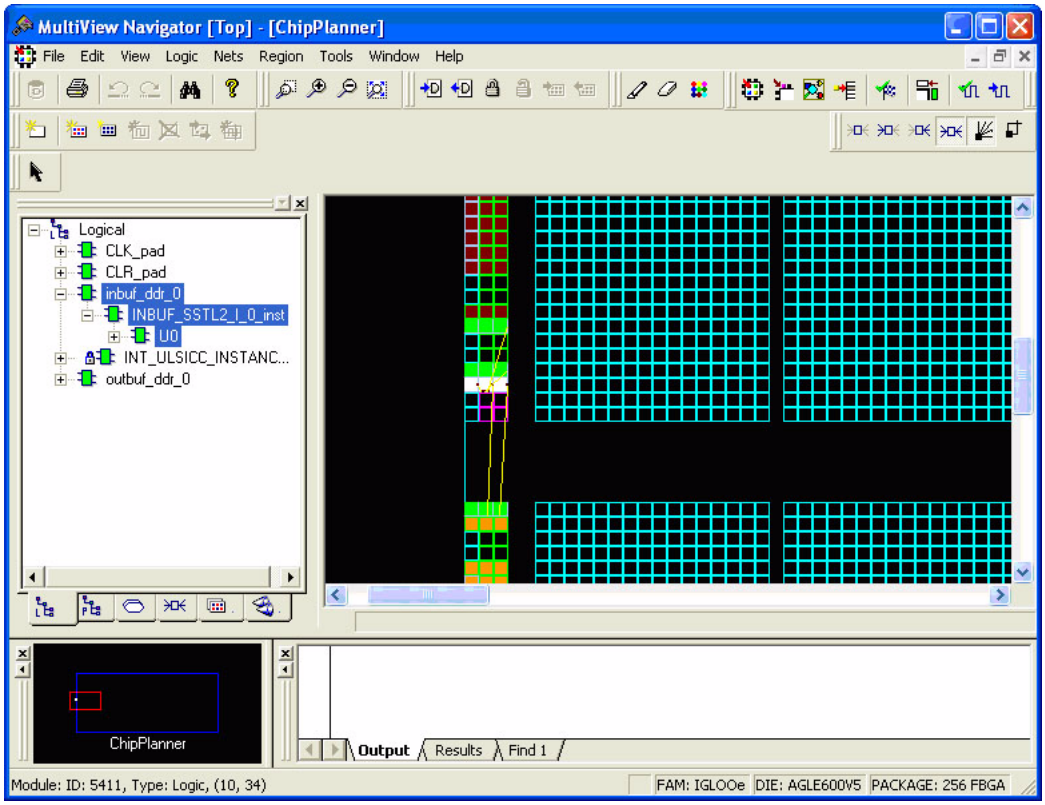

Figure 9-11 **• DDR Input/Output Cells as Seen by ChipPlanner for IGLOO/e Devices**

Verilog

```
module Inbuf_ddr(PAD,CLR,CLK,QR,QF);

input PAD, CLR, CLK;
output  QR, QF;

wire Y;

  DDR_REG DDR_REG_0_inst(.D(Y), .CLK(CLK), .CLR(CLR), .QR(QR), .QF(QF));
  INBUF INBUF_0_inst(.PAD(PAD), .Y(Y));

endmodule

module Outbuf_ddr(DataR,DataF,CLR,CLK,PAD);

input DataR, DataF, CLR, CLK;
output  PAD;

wire Q, VCC;

  VCC VCC_1_net(.Y(VCC));
  DDR_OUT DDR_OUT_0_inst(.DR(DataR), .DF(DataF), .CLK(CLK), .CLR(CLR), .Q(Q));
  OUTBUF OUTBUF_0_inst(.D(Q), .PAD(PAD));

endmodule
```

```
module ddr_test(DIN, CLK, CLR, DOUT);

input  DIN, CLK, CLR;
output DOUT;

  Inbuf_ddr Inbuf_ddr (.PAD(DIN), .CLR(clr), .CLK(clk), .QR(qr), .QF(qf));
  Outbuf_ddr Outbuf_ddr (.DataR(qr),.DataF(qf), .CLR(clr), .CLK(clk),.PAD(DOUT));

  INBUF INBUF_CLR (.PAD(CLR), .Y(clr));
  INBUF INBUF_CLK (.PAD(CLK), .Y(clk));

endmodule
```

Simulation Consideration

Actel DDR simulation models use inertial delay modeling by default (versus transport delay modeling). As such, pulses that are shorter than the actual gate delays should be avoided, as they will not be seen by the simulator and may be an issue in post-routed simulations. The user must be aware of the default delay modeling and must set the correct delay model in the simulator as needed.

Conclusion

IGLOO, Fusion, and ProASIC3 devices support a wide range of DDR applications with different I/O standards and include built-in DDR macros. The powerful capabilities provided by SmartGen and its GUI can simplify the process of including DDR macros in designs and minimize design errors. Additional considerations should be taken into account by the designer in design floorplanning and placement of I/O flip-flops to minimize datapath skew and to help improve system timing margins. Other system-related issues to consider include PLL and clock partitioning.

Part Number and Revision Date

This document contains content extracted from the Device Architecture section of the datasheet, combined with content previously published as an application note describing features and functions of the device. To improve usability for customers, the device architecture information has now been combined with usage information, to reduce duplication and possible inconsistencies in published information. No technical changes were made to the datasheet content unless explicitly listed. Changes to the application note content were made only to be consistent with existing datasheet information.

Part Number 51700094-010-2

Revised June 2008

List of Changes

The following table lists critical changes that were made in the current version of the chapter.

Previous Version	Changes in the Current Version (v1.2)	Page
v1.1 (March 2008)	The following changes were made to the family descriptions in Table 9-1 · Low-Power Flash Families: • ProASIC3L was updated to include 1.5 V. • The number of PLLs for ProASIC3E was changed from five to six.	9-2
v1.0 (January 2008)	The "IGLOO Terminology" section and "ProASIC3 Terminology" section are new.	9-2

Packaging and Pin Descriptions

10 – Pin Descriptions

Supply Pins

GND **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

V_{CC} **Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V for ProASIC®3/E devices, 1.5 V for IGLOO®/e V5 devices, and 1.2 V or 1.5 V for IGLOO/e V2 and ProASIC3L devices. V_{CC} is required for powering the JTAG state machine in addition to V_{JTAG}. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both V_{CC} and V_{JTAG} must remain powered to allow JTAG signals to pass through the device.

For IGLOO/e V2 and ProASIC3L devices, V_{CC} can be switched dynamically from 1.2 V to 1.5 V or vice versa. This allows in-system programming (ISP) when V_{CC} is at 1.5 V and the benefit of low-power operation when V_{CC} is at 1.2 V.

V_{CCI}Bx **I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on low-power flash devices plus a dedicated V_{JTAG} bank. Each bank can have a separate V_{CCI} connection. All I/Os in a bank will run off the same V_{CCI}Bx supply. V_{CCI} can be 1.2 V (not supported on ProASIC3/E devices), 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding V_{CCI} pins tied to GND.

VMVx **I/O Supply Voltage (quiet)**

Quiet supply voltage to the input buffers of each I/O bank. *x* is the bank number. Within the package, the VMV plane is decoupled from the simultaneous switching noise originated from the output buffer V_{CCI} domain. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.2 V (ProASIC3L and IGLOO/e devices only), 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and V_{CCI} should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding V_{CCI} pins of the same bank (i.e., VMV0 to V_{CCI}B0, VMV1 to V_{CCI}B1, etc.).

$V_{CCPLA/B/C/D/E/F}$ **PLL Supply Voltage**

Supply voltage to analog PLL, nominally 1.5 V or 1.2 V, depending on the device family.

- 1.5 V for IGLOO V5, IGLOOe V5, ProASIC3, and ProASIC3E devices
- 1.2 V or 1.5 V for IGLOO V2, IGLOOe V2, ProASIC3L, and ProASIC3EL devices

When the PLLs are not used, the Actel Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused V_{CCPLx} and V_{COMPLx} pins to ground. Actel recommends tying V_{CCPLx} to V_{CC} and using proper filtering circuits to decouple V_{CC} noise from PLL. Refer to the PLL Power Supply Decoupling section of *Clock Conditioning Circuits in IGLOO and ProASIC3 Devices* for a complete board solution for the PLL analog power supply and ground.

- There is one V_{CCPLF} pin on IGLOO, IGLOO PLUS, ProASIC3L, and ProASIC3 devices.
- There are six V_{CCPLX} pins on IGLOOe, ProASIC3EL, and ProASIC3E devices.

$V_{COMPLA/B/C/D/E/F}$ PLL Ground

Ground to analog PLL power supplies. When the PLLs are not used, the Actel Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused V_{CCPLx} and V_{COMPLx} pins to ground.

- There is one V_{COMPLF} pin on IGLOO, ProASIC3L, and ProASIC3 devices.
- There are six V_{COMPL} pins (PLL ground) on IGLOOe, ProASIC3EL, and ProASIC3E devices.

V_{JTAG} JTAG Supply Voltage

Low-power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the V_{JTAG} pin together with the TRST pin could be tied to GND. It should be noted that V_{CC} is required to be powered for JTAG operation; V_{JTAG} alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both V_{JTAG} and V_{CC} to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Actel recommends that V_{PUMP} and V_{JTAG} power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

V_{PUMP} Programming Supply Voltage

IGLOO, ProASIC3L, and ProASIC3 devices support single-voltage ISP of the configuration flash and FlashROM. For programming, V_{PUMP} should be 3.3 V nominal. During normal device operation, V_{PUMP} can be left floating or can be tied (pulled up) to any voltage between 0 V and the V_{PUMP} maximum. Programming power supply voltage (V_{PUMP}) range is listed in the datasheet.

When the V_{PUMP} pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 µF and 0.33 µF capacitors (both rated at 16 V) are to be connected in parallel across V_{PUMP} and GND, and positioned as close to the FPGA pins as possible.

Actel recommends that V_{PUMP} and V_{JTAG} power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

User-Defined Supply Pins

V_{REF} I/O Voltage Reference

Reference voltage for I/O minibanks in IGLOOe, ProASIC3EL, and ProASIC3E devices. V_{REF} pins are configured by the user from regular I/Os, and any I/O in a bank, except JTAG I/Os, can be designated the voltage reference I/O. Only certain I/O standards require a voltage reference—HSTL (I) and (II), SSTL2 (I) and (II), SSTL3 (I) and (II), and GTL/GTL+. One V_{REF} pin can support the number of I/Os available in its minibank.

User Pins

I/O User Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to V_{CCI}. With V_{CCI}, VMV, and V_{CC} supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

GL Globals

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in *Clock Conditioning Circuits in IGLOO and ProASIC3 Devices*. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

Refer to the I/O Structure section of the handbook for the device you are using for an explanation of the naming of global pins.

FF Flash*Freeze Mode Activation Pin

Flash*Freeze is available on IGLOO and ProASIC3L devices. It is not supported on ProASIC3/E devices. The FF pin is a dedicated input pin used to enter and exit Flash*Freeze mode. The FF pin is active-low, has the same characteristics as a single-ended I/O, and must meet the maximum rise and fall times. When Flash*Freeze mode is not used in the design, the FF pin is available as a regular I/O. For IGLOOe and ProASIC3EL only, the FF pin can be configured as a Schmitt trigger input.

When Flash*Freeze mode is used, the FF pin must not be left floating to avoid accidentally entering Flash*Freeze mode. While in Flash*Freeze mode, the Flash*Freeze pin should be constantly asserted.

The Flash*Freeze pin can be used with any single-ended I/O standard supported by the I/O bank in which the pin is located, and input signal levels compatible with the I/O standard selected. The FF pin should be treated as a sensitive asynchronous signal. When defining pin placement and board layout, simultaneously switching outputs (SSOs) and their effects on sensitive asynchronous pins must be considered.

Unused FF or I/O pins are tristated with weak pull-up. This default configuration applies to both Flash*Freeze mode and normal operation mode. No user intervention is required.

Table 10-1 shows the Flash*Freeze pin location on the available packages for IGLOO and ProASIC3L devices. The Flash*Freeze pin location is independent of device (except for a PQ208 package), allowing migration to larger or smaller IGLOO devices while maintaining the same pin location on the board. Refer to *Flash*Freeze Technology and Low-Power Modes in IGLOO and ProASIC3L Devices* for more information on I/O states during Flash*Freeze mode.

Table 10-1 • **Flash*Freeze Pin Location in IGLOO and ProASIC3L Family Packages (device-independent)**

IGLOO and ProASIC3L Packages	Flash*Freeze Pin
CS81/UC81	H2
CS121	J5
CS196	P3
QN68	18
QN132	B12
CS281	W2
CS201 (package only available for IGLOO PLUS devices)	R4
CS289 (package only available for IGLOO PLUS devices)	TBD
VQ100	27
FG144	L3
FG256	T3
FG484	W6
FG896	AH4
PQ208 (package only available for ProASIC3L devices)	
PQ208-A3P250 PQ208-A3P600L PQ2097-A3P1000L PQ208-A3PE3000L	56 55 55 58

JTAG Pins

Low-power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). V_{CC} must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; V_{JTAG} alone is insufficient. Both V_{JTAG} and V_{CC} to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the V_{JTAG} pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Actel recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all V_{JTAG} voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 10-2 for more information.

Table 10-2 • **Recommended Tie-Off Values for the TCK and TRST Pins**

V_{JTAG}	Tie-Off Resistance
V_{JTAG} at 3.3 V	200 Ω to 1 kΩ
V_{JTAG} at 2.5 V	200 Ω to 1 kΩ
V_{JTAG} at 1.8 V	500 Ω to 1 kΩ
V_{JTAG} at 1.5 V	500 Ω to 1 kΩ

Notes:

1. *Equivalent parallel resistance if more than one device is on the JTAG chain*
2. *The TCK pin can be pulled up/down.*
3. *The TRST pin is pulled down.*

TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST Boundary Scan Reset Pin

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 10-2 and must satisfy the parallel resistance value requirement. The values in Table 10-2 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Actel recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all V_{JTAG} voltages, 500 Ω to 1 kΩ will satisfy the requirements.

Special Function Pins

NC No Connect

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

DC Do Not Connect

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

Related Documents

Handbook Documents

Clock Conditioning Circuits in IGLOO and ProASIC3 Devices

http://www.actel.com/documents/LPD_CCC_HBs.pdf

I/O Structures in IGLOO PLUS Devices

http://www.actel.com/documents/IGLOOPLUS_IO_HBs.pdf

I/O Structures in IGLOO and ProASIC3 Devices

http://www.actel.com/documents/IGLOO_PA3_IO_HBs.pdf

I/O Structures in IGLOOe and ProASIC3E Devices

http://www.actel.com/documents/IGLOOe_PA3E_IO_HBs.pdf

*Flash*Freeze Technology and Low-Power Modes in IGLOO and ProASIC3L Devices*

http://www.actel.com/documents/LPD_FlashFreeze_HBs.pdf

Part Number and Revision Date

This document contains content extracted from the Device Architecture section of the datasheet. To improve usability for customers, the device architecture information has now been split into handbook sections, which also include usage information. No technical changes were made to the content unless explicitly listed.

Part Number 51700094-011-1

Revised March 2008

List of Changes

The following table lists critical changes that were made in the current version of the chapter.

Previous Version	Changes in Current Version (v1.1)	Page
v1.0 (January 2008)	The "VCCIBx I/O Supply Voltage" section was revised to note that 1.2 V is not supported for ProASIC3/E devices. The "VMVx I/O Supply Voltage (quiet)" section was updated to state that VMVx can also be 1.2 V nominal voltage on ProASIC3L and IGLOO/e devices.	10-1
	The "Handbook Documents" section was revised to include the three different I/O Structures chapters for IGLOO and ProASIC3 device families.	10-6
	The "$V_{CCPLA/B/C/D/E/F}$ PLL Supply Voltage" section and "$V_{COMPLA/B/C/D/E/F}$ PLL Ground" section were revised. The "V_{CCPLF} PLL Supply Voltage" section and "V_{COMPLF} PLL Ground" section were removed.	10-1 to 10-2
	The following packages were added to Table 10-1 · Flash*Freeze Pin Location in IGLOO and ProASIC3L Family Packages (device-independent): UC81, QN68, CS201, and CS289. Flash*Freeze pin W2 was specified for the CS281 package. The PG208 package was changed to the correct designation of PQ208.	10-4

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11 – Packaging

Semiconductor technology is constantly shrinking in size while growing in capability and functional integration. To enable next-generation silicon technologies, semiconductor packages have also evolved to provide improved performance and flexibility.

Actel consistently delivers packages that provide the necessary mechanical and environmental protection to ensure consistent reliability and performance. Actel IC packaging technology efficiently supports high-density FPGAs with large-pin-count Ball Grid Arrays (BGAs), but is also flexible enough to accommodate stringent form factor requirements for Chip Scale Packaging (CSP). In addition, Actel offers a variety of packages designed to meet your most demanding application and economic requirements for today's embedded and mobile systems.

The following documents provide packaging information and device selection for low-power flash devices.

Package Selector Guide

http://www.actel.com/documents/selguide.pdf

Lists devices currently recommended for new designs and the packages available for each member of the family. Use this document or the datasheet tables to determine the best package for your design, and which package drawing to use.

Package Mechanical Drawings

http://www.actel.com/documents/PckgMechDrwngs.pdf

This document contains the package mechanical drawings for all packages currently or previously supplied by Actel. Use the bookmarks to navigate to the package mechanical drawings.

Related Documents

Additional packaging materials are available at
http://www.actel.com/products/solutions/package/docs.aspx.

Part Number and Revision Date

This document contains content extracted from the Device Architecture section of the datasheet, combined with content previously published as an application note describing features and functions of the device. To improve usability for customers, the device architecture information has now been combined with usage information, to reduce duplication and possible inconsistencies in published information. No technical changes were made to the datasheet content unless explicitly listed. Changes to the application note content were made only to be consistent with existing datasheet information.

Part Number 5170009-012-0

Revised January 2008

Programming and Security

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POWER MATTERS

12 – Programming Flash Devices

Introduction

This document provides an overview of the various programming options available for the Actel flash families. The electronic version of this document includes active links to all programming resources, which are available at http://www.actel.com/products/hardware/default.aspx. For Actel antifuse devices, refer to the *Programming Antifuse Devices* document.

Summary of Programming Support

FlashPro3 is a high-performance in-system programming (ISP) tool targeted at the latest generation of low-power flash devices offered by Actel: IGLOO,® Fusion, and ProASIC®3, including ARM®-enabled devices. FlashPro3 offers extremely high performance through the use of USB 2.0 and is high-speed compliant for full use of the 480 Mbps bandwidth. This newest programmer can program ProASIC3E devices in under 30 seconds; even the largest ProASIC3E devices take under two minutes to program. Powered exclusively via USB, FlashPro3 provides a V_{PUMP} voltage of 3.3 V for programming these devices.

Silicon Sculptor 3 is an easy-to-use, single-site programming tool for Actel FPGAs that delivers high data throughput and promotes ease of use while lowering the overall cost of ownership. Silicon Sculptor 3 includes a high-speed USB 2.0 interface that allows a customer to connect as many as 12 programmers to a single PC. Furthermore, Silicon Sculptor 3 is compatible with adapter modules from Silicon Sculptor II, thereby preserving a customer's investment and enabling a seamless upgrade to this latest generation of the tool.

For details of programmer support for each device, refer to Table 12-5 on page 12-8.

General Flash Programming Information

Programming Basics

When choosing a programming solution, there are a number of options available. This section provides a brief overview of those options. The next sections provide more detail on those options as they apply to Actel FPGAs.

Reprogrammable or One-Time-Programmable (OTP)

Depending on the technology chosen, devices may be reprogrammable or one-time-programmable. As the name implies, a reprogrammable device can be programmed many times. Generally, the contents of such a device will be completely overwritten when it is reprogrammed. All Actel flash devices are reprogrammable.

An OTP device is programmable one time only. Once programmed, no more changes can be made to the contents. Actel flash devices provide the option of disabling the reprogrammability for security purposes. This combines the convenience of reprogrammability during design verification with the security of an OTP technology for highly sensitive designs.

Device Programmer or In-System Programming

There are two fundamental ways to program an FPGA: using a device programmer or, if the technology permits, using in-system programming. A device programmer is a piece of equipment in a lab or on the production floor that is used for programming devices. The devices are placed into a socket mounted in a programming adapter module, and the appropriate electrical interface is applied. The device can then be placed on the board. A typical programmer, used during

development, programs a single device at a time and is referred to as a single-site engineering programmer.

With ISP, the device is already mounted onto the board when programming occurs, most typically via the JTAG pins. The JTAG pins can be controlled either by an on-board resource, such as a microprocessor, or by an off-board programmer through a header connection. Once mounted, it can be programmed repeatedly. If the application requires it, the system can be designed to reprogram itself using a microprocessor, without the use of any external programmer.

For production, high-volume multi-site production programmers handle designs that require device programmers. In addition, Actel can preprogram devices for production, negating the need for further programming. This service is referred to as in-house programming (IHP).

Live at Power-Up (LAPU) or Boot PROM

Utilizing the technology of the FPGA significantly impacts board-level power-up considerations. Some technologies are nonvolatile and are considered functional, or "live," as soon as power reaches the operational level. All Actel FPGA technologies are live at power-up. By contrast, SRAM technology is volatile, and devices built using SRAM cells lose their contents when power cycling occurs. These devices must be reprogrammed every time power is applied. Such a design must include nonvolatile storage for the contents as well as the means to reprogram. There is a delay before SRAM devices are functional; other parts of the board must come alive first to reprogram these types of FPGAs. Therefore, such devices can never be part of critical boot circuits.

Design Security

Design security is a growing concern for systems designers. The choice of programming methodology and technology affects system security. Use of Actel programming technology is the most secure option available, providing much better protection than SRAM-based devices and ASICs. Actel provides a number of ways to ensure designs are protected. General information on design security can be found on the Actel website:

http://www.actel.com/products/solutions/security/default.aspx

Programming Features for Actel Devices

Actel provides two types of FPGAs: flash and antifuse (Table 12-1). Some programming methods are common to both and some are exclusive to flash. This document describes only the programming solutions supported for flash devices.

Table 12-1 • **Programming Features for Actel Devices**

Feature	Flash	Antifuse
Reprogrammable	Yes	No
In-system programmable	Yes	No
One-time programmable	Yes (option)	Yes
Live at power-up	Yes	Yes
Secure	Yes	Yes
Single-site programmer support	Yes	Yes
Multi-site programmer support	Yes	Yes
In-house programming support	Yes	Yes

Flash Devices

The flash devices supplied by Actel are reprogrammable by either a generic device programmer or ISP. Actel supports ISP using JTAG, which is supported by the FlashPro3, FlashPro, FlashPro Lite, and Sculptor programmers.

Levels of ISP support vary depending on the device chosen:

- Fusion, ProASIC3, and ProASIC3E devices support ISP.
- ProASIC3L devices operate using a 1.2 V core voltage and support ISP at 1.5 V only. Voltage switching is required in-system to switch from a 1.2 V core to 1.5 V core for programming.

- IGLOO, IGLOO PLUS, and IGLOOe V5 devices can be programmed in-system when the device is using a 1.5 V supply voltage to the FPGA core.
- IGLOO, IGLOO PLUS, and IGLOOe V2 devices can operate using either 1.2 V core voltage or 1.5 V core voltage. Although the device can operate at 1.2 V core voltage, the device can only be reprogrammed when the core voltage is 1.5 V. Voltage switching is required in-system to switch from a 1.2 V supply (V_{CC}, V_{CCI}, and V_{JTAG}) to 1.5 V for programming.

Since flash devices are nonvolatile, they are live at power-up. This is different from an SRAM-based device, which loads its programming information when it is powered up. SRAM devices require a time on the order of hundreds of milliseconds before the system is active.

There are multiple levels of security available in flash devices. Use of a security key will lock the device. The device can then only be reprogrammed by first unlocking the device with the appropriate security key. It can also be locked permanently, which means there is no key that can access the device. The command to secure the device is embedded within the programming file, optionally enabled by the programming software. This is also referred to as the OTP version of flash, allowing for only a single programming instance. This is discussed in more detail in the *Implementation of Security in Actel's ProASIC and ProASIC^PLUS Flash-Based FPGAs* application note. For ProASIC3/E devices, refer to *Security in Low-Power Flash Devices*

Flash devices can also be programmed using single-site or multi-site programmers as well as volume-programming services from Actel or other vendors.

Types of Programming for Flash Devices

The number of devices to be programmed will influence the optimal programming methodology. Those available are listed below:

- In-system programming
  - Using a programmer
  - Using a microprocessor or microcontroller
- Device programmers
  - Single-site programmers
  - Multi-site programmers, batch programmers, or gang programmers
  - Automated production (robotic) programmers
- Volume programming services
  - Actel in-house programming
  - Programming centers

In-System Programming

Device Type Supported: Flash

ISP refers to programming the FPGA after it has been mounted on the system board. The FPGA may be preprogrammed and later reprogrammed using ISP.

The advantage of using ISP is the ability to update the FPGA design many times without any changes to the board. This eliminates the requirement of using a socket for the FPGA, saving cost and improving reliability. It also reduces programming hardware expenses, as the ISP methodology is die-/package-independent.

There are two methods of in-system programming: external and internal.

- Programmer ISP—Refer to *In-System Programming (ISP) of Actel's Low-Power Flash Devices Using FlashPro3* for more information.

  Using an external programmer and a cable, the device can be programmed through a header on the system board. In Actel documentation, this is referred to as external ISP. Actel provides FlashPro3, FlashPro Lite, FlashPro, or Silicon Sculptor 3 to perform external ISP. Note that Silicon Sculptor 3 can only provide ISP for ProASIC and ProASIC^PLUS® families, not for ProASIC3 or ProASIC3E.

- Advantages: Allows local control of programming and data files for maximum security. The programming algorithms and hardware are available from Actel. The only hardware required on the board is a programming header.
- Limitations: A negligible board space requirement for the programming header and JTAG signal routing

- Microprocessor ISP—Refer to *MicroProcessor Programming of Actel's Low-Power Flash Devices* for more information.

  Using a microprocessor and an external or internal memory, you can store the program in memory and use the microprocessor to perform the programming. In Actel documentation, this is referred to as internal ISP. Both the code for the programming algorithm and the FPGA programming file must be stored in memory on the board. Programming voltages must also be generated on the board.

  - Advantages: The programming code is stored in the system memory. An external programmer is not required during programming.
  - Limitations: This is the approach that requires the most design work, since some way of getting and/or storing the data is needed; a system interface to the device must be designed; and the low-level API to the programming firmware must be written and linked into the code provided by Actel. While there are benefits to this methodology, serious thought and planning should go into the decision.

Device Programmers

Device Type Supported: Flash and Antifuse

Device programmers are used to program a device before it is mounted on the system board.

The advantage of using device programmers is that no programming hardware is required on the system board. Therefore, no additional components or board space are required.

If devices are to be reprogrammed multiple times, or if the quantity of devices to be programmed is relatively low, a single-site device programmer is the simplest solution. For applications in which design security is paramount (often the case in military or space designs), the use of on-site programing maintains design security at all times.

Adapter modules are purchased with the programmers to support the FPGA packages used. The FPGA is placed in the adapter module and the programming software is run from a PC. Actel supplies the programming software for all of the Actel programmers. The software allows for the selection of the correct die/package and programming files. It will then program and verify the device.

- Single-site programmers

  A single-site programmer programs one device at a time. Actel offers Silicon Sculptor 3 as a single-site programmer.

  - Advantages: Lower cost than multi-site programmers. No additional overhead for programming on the system board. Allows local control of programming and data files for maximum security. Allows on-demand programming on-site.
  - Limitations: Only programs one device at a time.

- Multi-site programmers

  Often referred to as batch or gang programmers, multi-site programmers can program multiple devices at the same time using the same programming file. This is often used for large volume programming and by programming houses. The sites often have independent processors and memory enabling the sites to operate concurrently, meaning each site may start programming the same file independently. This enables the operator to change one device while the other sites continue programming, which increases throughput. Multiple adapter modules for the same package are required when using a multi-site programmer. Silicon Sculptor I, II, and 3 programmers can be cascaded to program multiple devices in a chain. Multi-site programmers can also be purchased from BP Microsystems.

  - Advantages: Provides the capability of programming multiple devices at the same time. No additional overhead for programming on the system board. Allows local control of programming and data files for maximum security.

– Limitations: More expensive than a single-site programmer

- Automated production (robotic) programmers

  Automated production programmers are based on multi-site programmers. They consist of a large input tray holding multiple parts and a robotic arm to select and place parts into appropriate programming sockets automatically. When the programming of the parts is complete, the parts are removed and placed in a finished tray. The automated programmers are often used in volume programming houses to program parts for which the programming time is small.

Volume Programming Services

Device Type Supported: Flash and Antifuse

Once the design is stable for applications with large production volumes, preprogrammed devices can be purchased. Table 12-2 describes the volume programming services.

Table 12-2 • **Volume Programming Services**

Programmer	Vendor	Availability
In-House Programming	Actel	Contact Actel Sales
Distributor Programming Centers	Memec Unique	Contact Distribution
Independent Programming Centers	Various	Contact Vendor

Advantages: As programming is outsourced, this solution is easier to implement than creating a substantial in-house programming capability. As programming houses specialize in large-volume programming, this is often the most cost-effective solution.

Limitations: There are some logistical issues with the use of a programming service provider, such as the transfer of programming files and the approval of first articles. By definition, the programming file must be released to a third-party programming house. Nondisclosure agreements (NDAs) can be signed to help ensure data protection; however, for extremely security-conscious designs, this may not be an option.

- Actel In-House Programming

  When purchasing Actel devices in volume, IHP can be requested as part of the purchase. If this option is chosen, there is a small cost adder for each device programmed. Each device is marked with a special mark to distinguish it from blank parts. Programming files for the design will be sent to Actel. Sample parts with the design programmed, First Articles, will be returned for customer approval. Once approval of First Articles has been received, Actel will proceed with programming the remainder of the order. To request Actel IHP, contact your local Actel representative.

- Distributor Programming Centers

  If purchases are made through a distributor, many distributors will provide programming for their customers. Consult with your preferred distributor about this option.

- Independent Programming Centers

  There are many programming centers that specialize only in programming but are not directly affiliated with Actel or our distributors. These programming centers must follow the guidelines for programming Actel devices and use certified programmers to program Actel devices. Actel does not have recommendations for external programming centers.

Programming Solutions

Details for the available programmers can be found in the programmer user's guides listed in the "Related Documents" section on page 12-12. Refer to Table 12-3 on page 12-6 for more information concerning programming solutions.

All of the programmers except the FlashPro3, FlashPro Lite, and FlashPro require adapter modules, which are designed to support device packages. The modules are all listed on the Actel website at http://www.actel.com/products/hardware/program_debug/ss/modules.aspx. They are not listed in this document, since this list is updated frequently with new package options and any upgrades required to improve programming yield or support new families.

Table 12-3 • **Programming Solutions**

Programmer	Vendor	ISP	Single Device	Multi-Device	Availability
FlashPro3	Actel	Only	Yes	Yes[1]	Available
FlashPro Lite	Actel	Only	Yes	Yes[1]	Available
FlashPro	Actel	Only	Yes	Yes[1]	Available
Silicon Sculptor 3	Actel	Yes	Yes	Cascade option (up to two)	Available
Silicon Sculptor II	Actel	Yes	Yes[2]	Cascade option (up to two)	Available
Silicon Sculptor	Actel	Yes	Yes	Cascade option (up to four)	Discontinued
Sculptor 6X	Actel	No	Yes	Yes	Discontinued
BP MicroProgrammers	BP Microsystems	No	Yes	Yes	Contact BP Microsystems at www.bpmicro.com

Notes:

1. *Multiple devices can be connected in the same JTAG chain for programming.*
2. *Silicon Sculptor II can only provide ISP for ProASIC and ProASIC^{PLUS} families, not for ProASIC3/E.*

Programmer Ordering Codes

The products shown in Table 12-4 can be ordered through Actel sales and will be shipped directly from Actel. Products can also be ordered from Actel distributors, but will still be shipped directly from Actel. Table 12-4 includes ordering codes for the full kit, as well as codes for replacement items and any related hardware. Some additional products can be purchased from external suppliers for use with the programmers. Ordering codes for adapter modules used with Silicon Sculptor are available on the Actel website at http://www.actel.com/products/hardware/program_debug/ss/modules.aspx.

Table 12-4 • **Programming Ordering Codes**

Description	Vendor	Ordering Code	Comment
FlashPro3 ISP programmer	Actel	FLASHPRO 3	Uses a 2x5, RA male header connector
FlashPro Lite ISP programmer	Actel	FLASHPRO LITE	Supports small programming header or large header through header converter (not included)
FlashPro ISP programmer	Actel	FLASH PRO	Supports small programming header or large header through header converter (not included)
Silicon Sculptor 3	Actel	SILICON-SCULPTOR 3	USB 2.0 high-speed production programmer
Silicon Sculptor II	Actel	SILICON-SCULPTOR II	Requires add-on adapter modules to support devices
Silicon Sculptor ISP module	Actel	SMPA-ISP-ACTEL-3-KIT	Ships with both large and small header support

** A maximum of two Silicon Sculptor II programmers can be chained together using a standard IEEE 1284 parallel port cable.*

Table 12-4 • **Programming Ordering Codes (continued)**

Description	Vendor	Ordering Code	Comment
Concurrent programming cable	Actel	SS-EXPANDER	Used to cascade Silicon Sculptor I programmers together*
Software for Silicon Sculptor	Actel	SCULPTOR-SOFTWARE-CD	http://www.actel.com/download/program_debug/ss/
ISP cable for small header	Actel	ISP-CABLE-S	Supplied with SMPA-ISP-ACTEL-3-KIT
ISP cable for large header	Actel	PA-ISP-CABLE	Supplied with SMPA-ISP-ACTEL-3-KIT
Header converter	Actel	Header-Converter	Converts from small to large header
Small programming header	Samtec	FTSH-113-01-L-D-K	Supported by FlashPro, FlashPro Lite, and Silicon Sculptor In migrating to ProASIC3/E devices, an FP3-26PIN-ADAPTER is required.
10-pin 0.1" pitch cable header (right-angle PCB mount angle)	AMP	103310-1	Supported by FlashPro3
10-pin 0.1" pitch cable header (straight PCB mount angle)	3M	2510-6002UB	Supported by FlashPro3
Compact programming header (10-pin 0.05" pitch, 2 rows of 5 pins)	Samtec	FTSH-105-01-L-D-K	Supported by FlashPro3, FP3-26PIN-ADAPTER required. Used for boards where space is at a premium.
Migration and compact header adapter	Actel	FP3-26PIN-ADAPTER	Required with the use of FTSH-105-01-L-D-K
Large programming header 0.062" board thickness	3M	3429-6502	Supported by Silicon Sculptor by default, FlashPro, and FlashPro Lite, with header converter
Large programming header 0.094" to 0.125" board thickness	3M	3429-6503	Supported by Silicon Sculptor by default, FlashPro, and FlashPro Lite, with header converter
Plug-in header small	Actel	SMPA-ISP-HEADER-S	Required for small header for ProASIC only; not used for ProASIC^{PLUS}
Plug-in header	Actel	SMPA-ISP-HEADER	Required for large header for ProASIC only; not used for ProASIC^{PLUS}
Vacuum pens for PQ, TQ, VQ; <208 pins	Actel	PENVAC	
Vacuum pens for PQ, TQ, VQ; ≥208 pins	Actel	PENVAC-HD	Heavy-duty, provides stronger vacuum

* *A maximum of two Silicon Sculptor II programmers can be chained together using a standard IEEE 1284 parallel port cable.*

Programmer Device Support

Refer to Table 12-5 to determine which general-purpose flash devices have programmer device support. To learn more about the different Actel families, refer to the Actel website: http://www.actel.com/products/devices.aspx.

Data in Table 12-5 also applies to ARM-enabled M7 device versions of Fusion, IGLOO, and ProASIC3 devices. Refer to the appropriate family datasheets for information on die/package combinations available as ARM-enabled versions.

Table 12-5 • **Programmer Device Support**

Actel Family	Device	ARM-Enabled	Silicon Sculptor	Silicon Sculptor 6X	Silicon Sculptor II	Silicon Sculptor 3	FlashPro	FlashPro Lite	FlashPro3
Fusion	AFS090		No	No	Yes. No ISP support.	Yes. No ISP support.	No	No	Yes. ISP support
	AFS250								
	AFS600	✓							
	AFS1500	✓							
IGLOO	AGL015		No	No	Yes. No ISP support.	Yes. No ISP support.	No	No	Yes. ISP support.
	AGL030								
	AGL060								
	AGL125								
	AGL250	✓							
	AGL600	✓							
	AGL1000	✓							
IGLOO PLUS	AGLP030		No	No	Yes. No ISP support	Yes. No ISP support.	No	No	Yes. ISP support
	AGLP060								
	AGLP125								
IGLOOe	AGLE600	✓	No	No	Yes. No ISP support.	Yes. No ISP support.	No	No	Yes. ISP support
	AGLE3000	✓							
ProASIC3L	A3P250L	✓	No	No	Yes. No ISP support.	Yes. No ISP support.	No	No	Yes. ISP support.
	A3P600L	✓							
	A3P1000L	✓							
	A3PE3000L	✓							
ProASIC3	A3P015		No	No	Yes. No ISP support.	Yes. No ISP support.	No	No	Yes. ISP support.
	A3P030								
	A3P060								
	A3P125								
	A3P250	✓							
	A3P400	✓							
	A3P600	✓							
	A3P1000	✓							
ProASIC3E	A3PE600	✓	No	No	Yes. No ISP support.	Yes. No ISP support.	No	No	Yes. ISP support.
	A3PE1500	✓							
	A3PE3000	✓							

** Refer to the "Certified Programming Solutions" section on page 12-9 for more information on programmer support.*

Table 12-5 • **Programmer Device Support (continued)**

Actel Family	Device	ARM-Enabled	Silicon Sculptor	Silicon Sculptor 6X	Silicon Sculptor II	Silicon Sculptor 3	FlashPro	FlashPro Lite	FlashPro3
ProASIC[PLUS]	APA075		Yes. ISP support.	Yes. ISP support.	Yes. ISP support.	Yes. ISP support.	Yes. ISP support.	Yes. ISP support.	No
	APA150								
	APA300								
	APA450								
	APA600								
	APA750								
	APA1000								
ProASIC	A500K50		Yes	Yes	Yes	Yes	Yes	No	No
	A500K130								
	A500K180								
	A500K270								

* *Refer to the "Certified Programming Solutions" section on page 12-9 for more information on programmer support.*

Certified Programming Solutions

The Actel-certified programmers for flash devices are FlashPro3, FlashPro Lite, FlashPro, Silicon Sculptor I and II, and any programmer that is built by BP Microsystems. All other programmers are considered noncertified programmers.

- **FlashPro3, FlashPro Lite, FlashPro**

  The Actel family of FlashPro device programmers provides in-system programming in an easy-to-use, compact system that supports all ProASIC families. Whether programming a board containing a single device or multiple devices connected in a chain, the Actel line of FlashPro programmers enables fast programming and reprogramming. Programming with the FlashPro series of programmers saves board space and money as it eliminates the need for sockets on the board. There are no built-in algorithms, so there is no delay between product release and programming support.

- **Silicon Sculptor II**

  Silicon Sculptor II is a robust, compact, single-device programmer with standalone software for the PC. It is designed to enable concurrent programming of multiple units from the same PC with speeds equivalent to or faster than previous Actel programmers. It replaces Silicon Sculptor I as the Actel programmer of choice.

- **Silicon Sculptor I and Silicon Sculptor 6X**

  Actel no longer offers Silicon Sculptor I or Silicon Sculptor 6X for sale. Both items have been discontinued. Actel does support Silicon Sculptor I and Silicon Sculptor 6X by continuing to release new software that enables improved programming of previously covered Actel devices; new Actel devices are only supported on Silicon Sculptor II. All software support for Silicon Sculptor I and Silicon Sculptor 6X programmers will be disconnected by the end of 2005; no support for these older programmers will be offered in 2006. Actel recommends that all customers upgrade to Silicon Sculptor II or a BP multi-site programmer.

- **Noncertified Programmers**

  Actel does not test programming solutions from other vendors, and CANNOT guarantee programming yield. Also, Actel will not perform any failure analysis on devices programmed by hardware from other vendors.

- **Programming Centers**

  Actel programming hardware policy also applies to programming centers. Actel expects all programming centers to use certified programmers to program Actel devices. If a programming center uses noncertified programmers to program Actel devices, the "Noncertified Programmers" policy applies.

Flash Programming Guidelines

Preprogramming Setup

Before programming, several steps are required to ensure an optimal programming yield.

Use Proper Handling and Electrostatic Discharge (ESD) Precautions

Actel FPGAs are sensitive electronic devices that are susceptible to damage from ESD and other types of mishandling. For more information about ESD, refer to the *Actel Quality and Reliability Guide,* beginning with page 41.

Use the Latest Version of the Designer Software to Generate Your Programming File (recommended)

The files used to program Actel flash devices (*.bit, *.stp) contain important information about the switches that will be programmed in the FPGA. Find the latest version and corresponding release notes at http://www.actel.com/download/software/designer/. Also, programming files must always be zipped during file transfer to avoid the possibility of file corruption.

Use the Latest Version of the Programming Software

The programming software is frequently updated to accommodate yield enhancements in FPGA manufacturing. These updates ensure maximum programming yield and minimum programming times. Before programming, always check the version of software being used to ensure it is the most recent. Depending on the programming software, refer to one of the following:

- FlashPro: http://www.actel.com/download/program_debug/flashpro/
- Silicon Sculptor: http://www.actel.com/download/program_debug/ss/

Use the Most Recent Adapter Module with Silicon Sculptor

Occasionally, Actel makes modifications to the adapter modules to improve programming yields and programming times. To identify the latest version of each module before programming, visit http://www.actel.com/products/hardware/program_debug/ss/modules.aspx.

Perform Routine Hardware Self-Diagnostic Test

- FlashPro

  The self-test is only applicable when programming with FlashPro and FlashPro3 programmers. It is not supported with FlashPro Lite. To run the self-diagnostic test, follow the instructions given in the "Performing a Self-Test" section of http://www.actel.com/documents/FlashPro_UG.pdf.

- Silicon Sculptor

  The self-diagnostic test verifies correct operation of the pin drivers, power supply, CPU, memory, and adapter module. This test should be performed before every programming session. At minimum, the test must be executed every week. To perform self-diagnostic testing using the Silicon Sculptor software, perform the following steps, depending on the operating system:

  – DOS: From anywhere in the software, type **ALT + D**.

  – Windows: Click **Device** > choose **Actel Diagnostic** > select the **Test** tab > click **OK**.

Programming Flash FPGAs

Programming a flash device is a one-step process, whether programming is conducted with a socket adapter module or via ISP. The Execute function will automatically erase the device, program the flash cells, and verify that it is programmed correctly. Actel recommends confirming the security status is correct before programming.

The following steps are required to program Actel flash FPGAs.

Programming with FlashPro

Setup

Properly connect the FlashPro ribbon cable with the programming header and turn on the switch. Actel recommends running the self-test before programming any devices; see the "Perform Routine Hardware Self-Diagnostic Test" section on page 12-10.

In the programming software, from the File menu, choose **Connect**. In the FlashPro Connect to Programmer dialog box that appears, select the port to which the FlashPro programmer is connected, and select the device family. Disable voltages from the programmer if they are available on the board.

Click **Connect**. A successful connect or any errors appear in the Log window.

Analyze Chain and Device Selection

From the File menu, choose **Analyze Chain**. Chain details appear in the Log window. If any failures appear, refer to the error and troubleshooting section of the *FlashPro User's Guide*. Select the device to be programmed from the **Device** list. If only one device is present in the chain, performing Analyze Chain selects that device automatically from the Device list.

Loading the STAPL file

FlashPro3, FlashPro Lite, and FlashPro programmers use a STAPL (*.stp) file to program the device. To load the STAPL file, from the File menu, choose **Open STAPL file**, or click the **Open File** button in the toolbar.

Selecting an Action

After loading the STAPL file, select an action from the Action list. See the "Programming File Actions" section in the *FlashPro User's Guide* for a definition of each action.

Programming the Device

To program the device, in the Action list, select **Program**. Make the required selections and click **Execute** to start programming. The progress of the programming action displays in the Log window. The message "Exit 0" indicates that the device has successfully been programmed.

Note: Do not interrupt the programming sequence; it may damage the device or programmer.

Verify Correct Programming

To verify the device is programmed with the correct STAPL file, load the STAPL file and in the Action list and click **Verify**. Click **Execute** to start the verification process. A successful verification results in "Exit 0."

Note: Verification is also performed in the previous "Programming the Device" step; clicking **Verify** is an additional standalone option.

Programming Failure Allowances

Flash FPGAs are reprogrammable, so Actel tests the programmability for 100% of the devices shipped.

Return Material Authorization (RMA) Policies

Actel consistently strives to exceed customer expectations by continuing to improve the quality of our products and our quality management system. Actel has RMA procedures in place to address programming fallout. Customers should be mindful of the following RMA policies.

All devices submitted for an RMA, must be within the Actel warranty period of one year from date of shipment. Actel will reject RMAs for devices that are no longer under warranty.

RMAs will only be authorized for current Actel devices. Devices that have been discontinued will not receive RMAs. All functional failure analysis requests must be initiated by opening a case with Actel Technical Support. Devices returned for failure analysis against an RMA should be in their original packaging and must have an RMA number issued by Actel.

Contacting the Customer Support Group

Highly skilled engineers staff the Customer Applications Center from 7:00 A.M. to 6:00 P.M., Pacific time, Monday through Friday. You can contact the center by one of the following methods:

Electronic Mail

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. Actel monitors the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and contact information for efficient processing of your request. The technical support email address is tech@actel.com.

Telephone

Our Technical Support Hotline answers all calls. The center retrieves information, such as your name, company name, telephone number, and question. Once this is done, a case number is assigned. Then the center forwards the information to a queue where the first available applications engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific time, Monday through Friday.

The Customer Applications Center number is (800) 262-1060.

European customers can call +44 (0) 1256 305 600.

Related Documents

Below is a list of related documents, their location on the Actel website, and a brief summary of each document.

Application Notes

Programming Antifuse Devices

http://www.actel.com/documents/AntifuseProgram_AN.pdf

Implementation of Security in Actel's ProASIC and ProASIC^{PLUS} Flash-Based FPGAs

http://www.actel.com/documents/Flash_Security_AN.pdf

Handbook Documents

Security in Low-Power Flash Devices

http://www.actel.com/documents/LPD_Security_HBs.pdf

In-System Programming (ISP) of Actel's Low-Power Flash Devices Using FlashPro3

http://www.actel.com/documents/LPD_ISP_HBs.pdf

MicroProcessor Programming of Actel's Low-Power Flash Devices

http://www.actel.com/documents/LPD_Microprocessor_HBs.pdf

User's Guides

FlashPro Programmers

FlashPro3, FlashPro Lite, and FlashPro

http://www.actel.com/products/hardware/program_debug/flashpro/default.aspx

FlashPro User's Guide

http://www.actel.com/documents/FlashPro_UG.pdf

The FlashPro User's Guide includes hardware and software setup, self-test instructions, use instructions, and a troubleshooting / error message guide.

Silicon Sculptor 3 and Silicon Sculptor II

http://www.actel.com/products/hardware/program_debug/ss/default.aspx

Other Documents

http://www.actel.com/products/solutions/security/default.aspx#flashlock

The security resource center describes security in Actel Flash FPGAs.

Actel Quality and Reliability Guide

http://www.actel.com/documents/RelGuide.pdf

Part Number and Revision Date

This document was previously published as an application note describing features and functions of the device, and as such has now been incorporated into the device handbook format. No technical changes have been made to the content.

Part Number 51700094-013-1

Revised March 2008

List of Changes

The following table lists critical changes that were made in the current version of the chapter.

Previous Version	Changes in Current Version (v1.1)	Page
v1.0 (January 2008)	The "Flash Devices" section was updated to include the IGLOO PLUS family. The text, "Voltage switching is required in-system to switch from a 1.2 V core to 1.5 V core for programming" was revised to state, "Although the device can operate at 1.2 V core voltage, the device can only be reprogrammed when the core voltage is 1.5 V. Voltage switching is required in-system to switch from a 1.2 V supply (V_{CC}, V_{CCI}, and V_{JTAG}) to 1.5 V for programming."	12-2
	The ProASIC3L family was added to Table 12-5 · Programmer Device Support as a separate set of rows rather than combined with ProASIC3 and ProASIC3E devices. The IGLOO PLUS family was included, and AGL015 and A3P015 were added.	12-8

Rate This Document

13 – Security in Low-Power Flash Devices

Security in Programmable Logic

The need for security on FPGA programmable logic devices (PLDs) has never been greater than today. If the contents of the FPGA can be read by an external source, the intellectual property (IP) of the system is vulnerable to unauthorized copying. Actel IGLOO,® Fusion, and ProASIC®3 devices contain state-of-the-art circuitry to make the flash-based devices secure during and after programming. Low-power flash devices have a built-in 128-bit Advanced Encryption Standard (AES) decryption core (except for 15 k and 30 k gate devices). The decryption core facilitates secure in-system programming (ISP) of the FPGA core array fabric, the FlashROM, and the Flash Memory Blocks (FBs) in Fusion devices. The FlashROM, Flash Blocks, and FPGA core fabric can be programmed independently of each other, allowing the FlashROM or Flash Blocks to be updated without the need for change to the FPGA core fabric.

Actel has incorporated the AES decryption core into the low-power flash devices and has also included the Actel flash-based lock technology, FlashLock.® Together, they provide leading-edge security in a programmable logic device. Configuration data loaded into a device can be decrypted prior to being written to the FPGA core using the AES 128-bit block cipher standard. The AES encryption key is stored in on-chip, nonvolatile flash memory.

This document outlines the security features offered in low-power flash devices, some applications and uses, as well as the different software settings for each application.

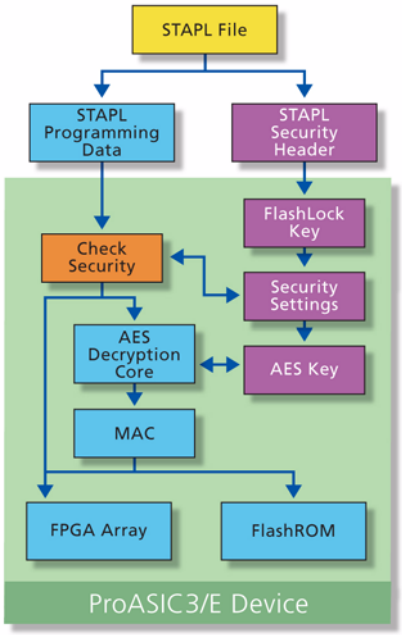


Figure 13-1 • **Overview on Security**

Security Support in Low-Power Devices

The low-power flash families listed in Table 13-1 support the security feature and the functions described in this document. The family name links to the datasheet for each family. Any required timing details are linked from the Timing Numbers column to the relevant datasheet sections.

Table 13-1 • **Low-Power Flash Families**

Family[1]	Description	Timing Numbers[2]
IGLOO	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*IGLOO DC and Switching Characteristics*
IGLOO PLUS	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology and enhanced I/O capabilities	*IGLOO PLUS DC and Switching Characteristics*
IGLOOe	IGLOO devices enhanced with higher density, five additional PLLs, and additional I/O standards	*IGLOOe DC and Switching Characteristics*
ProASIC3L	Low-power, high-performance 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*ProASIC3L DC and Switching Characteristics*
ProASIC3	Low-power, high-performance 1.5 V FPGAs	*ProASIC3 DC and Switching Characteristics*
ProASIC3E	ProASIC3 enhanced with higher density, six additional PLLs, and additional I/O standards	*ProASIC3E DC and Switching Characteristics*
ProASIC3 Automotive	Low-power, high-performance FPGAs qualified for automotive applications	*Automotive ProASIC3 DC and Switching Characteristics*
Fusion	Low-power mixed-signal Programmable System Chip (PSC)	*Fusion DC and Power Characteristics*

Notes:

1. *The family names are linked to the appropriate product brief.*
2. *The timing number links go to the relevant timing numbers in the datasheet.*

Actel's low-power flash devices (listed in Table 13-1) provide a selection of low-power, secure, live-at-power-up, single-chip solutions. The nonvolatile flash-based devices do not require a boot PROM and incorporate FlashLock® technology, which provides a unique combination of reprogrammability and design security without external overhead. Only low-power flash FPGAs can offer these advantages.

Actel IGLOO PLUS FPGAs are the industry-leading 1.2 V ultra-low-power programmable logic devices (PLDs) and consume 90% less static power and over 50% less dynamic power than PLD alternatives, while ProASIC3L devices offer a balance of low power and higher performance.

Flash*Freeze technology used in IGLOO, IGLOO PLUS, and ProASIC3L devices enables easy entry to and exit from the ultra-low power mode, which consumes as little as 5 µW, while retaining SRAM and register data. IGLOO PLUS also offers the ability to hold I/O state in Flash*Freeze mode. Flash*Freeze technology simplifies power management through I/O and clock management without the need to turn off voltages, I/Os, or clocks at the system level. Entering and exiting Flash*Freeze mode takes less than 1 µs.

The Actel Fusion® family, based on the highly successful ProASIC3 flash FPGA architecture, has been designed as a high-performance, mixed-signal Programmable System Chip. Fusion supports many peripherals, including embedded flash memory, analog-to-digital converter (ADC), high-drive outputs, RC and crystal oscillators, and real-time counter (RTC). The total available on-chip memory, including the flash array blocks, is greater than that found in SRAM FPGAs.

IGLOO Terminology

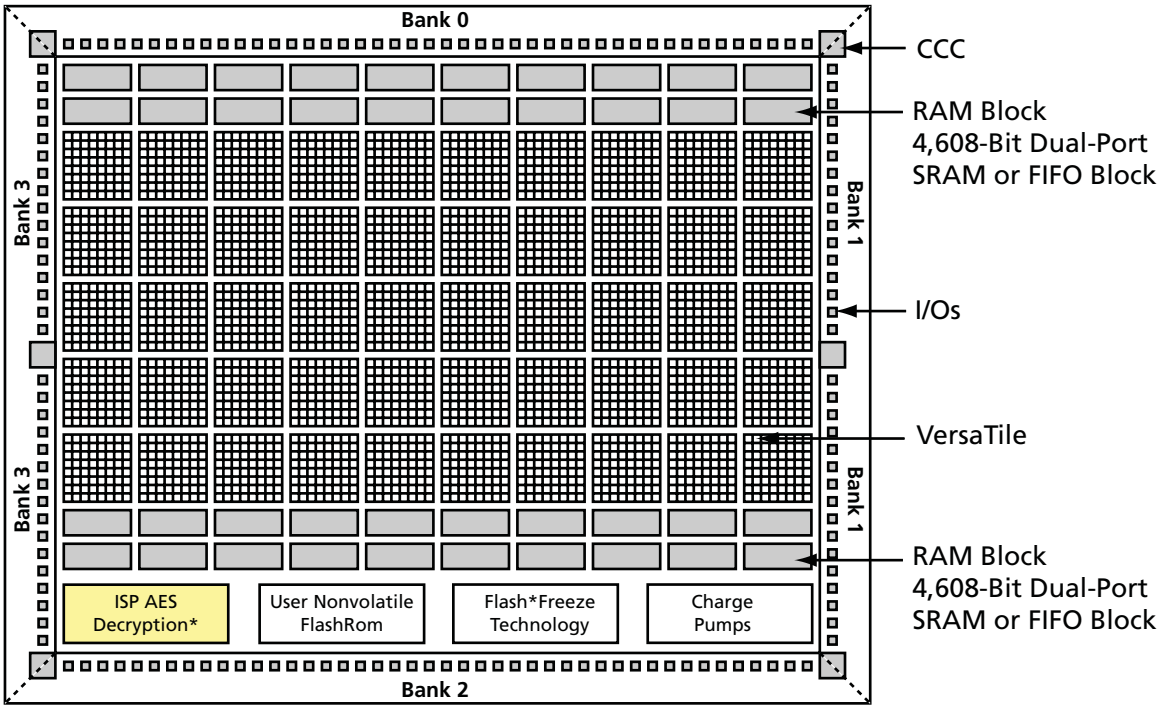
In documentation, the term IGLOO families or IGLOO devices refers to all IGLOO families as listed in Table 13-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

ProASIC3 Terminology

In documentation, the term ProASIC3 families or ProASIC3 devices refers to all ProASIC3 families as listed in Table 13-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

Security Architecture

IGLOO, Fusion, and ProASIC3 devices have been designed with the most comprehensive programming logic design security in the industry. In the architecture of these devices, security has been designed into the very fabric. The flash cells are located beneath seven metal layers, and the use of many device design and layout techniques makes invasive attacks difficult. Since device layers cannot be removed without disturbing the charge on the programmed (or erased) flash gates, devices cannot be easily deconstructed to decode the design. Low-power flash devices are unique in being reprogrammable and having inherent resistance to both invasive and noninvasive attacks on valuable IP. Secure, remote ISP is now possible with AES encryption capability for the programming file during electronic transfer. Figure 13-2 shows a view of the AES decryption core inside an IGLOO device; Figure 13-3 on page 13-4 shows the AES decryption core inside a Fusion device. The AES core is used to decrypt the encrypted programming file when programming.



Note: ISP AES Decryption is not supported by 15 k and 30 k gate devices. For details of other architecture features by device, refer to the appropriate family datasheet.

***Figure 13-2* • Block Representation of the AES Decryption Core in IGLOO and ProASIC3 Devices**

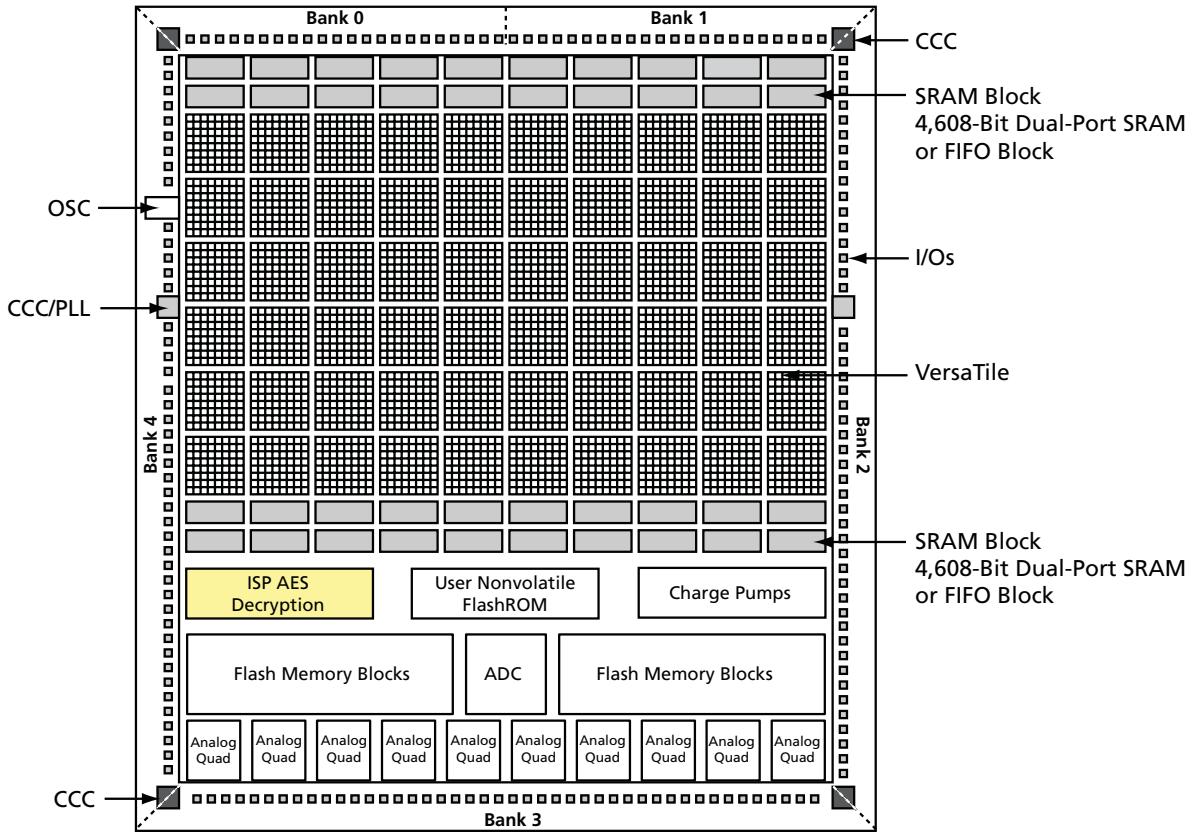


***Figure 13-3* • Block Representation of the AES Decryption Core in a Fusion AFS600 FPGA**

Security Features

IGLOO and ProASIC3 devices have two entities inside: FlashROM and the FPGA core fabric. Fusion devices contain three entities: FlashROM, FBs, and the FPGA core fabric. The parts can be programmed or updated independently with a STAPL programming file. The programming files can be AES-encrypted or plaintext. This allows maximum flexibility in providing security to the entire device. Refer to *FlashROM in Actel's Low-Power Flash Devices* for information on the FlashROM structure.

Unlike SRAM-based FPGA devices, which require a separate boot PROM to store programming data, low-power flash devices are nonvolatile, and the secured configuration data is stored in on-chip flash cells that are part of the FPGA fabric. Once programmed, this data is an inherent part of the FPGA array and does not need to be loaded at system power-up. SRAM-based FPGAs load the configuration bitstream upon power-up; therefore, the configuration is exposed and can be read easily.

The built-in FPGA core, FB, and FlashROM support programming files encrypted with the 128-bit AES (FIPS-192) block ciphers. The AES key is stored in dedicated, on-chip flash memory and can be programmed before the device is shipped to other parties (allowing secure remote field updates).

Security in ARM-Enabled Low-Power Flash Devices

There are slight differences between the regular flash devices and the ARM®-enabled flash devices, which have the M1 and M7 prefix.

The AES key is used by Actel and preprogrammed into the device to protect the ARM IP. As a result, the design is encrypted along with the ARM IP, according to the details below.

CoreMP7 Device Security

ARM7 (M7-enabled) devices are shipped with the following security features:

- FPGA array enabled for AES-encrypted programming and verification
- FlashROM enabled for plaintext Read and Write

Cortex-M1 Device Security

Cortex-M1–enabled devices are shipped with the following security features:

- FPGA array enabled for AES-encrypted programming and verification
- FlashROM enabled for AES-encrypted Write and Verify
- Fusion Embedded Flash Memory enabled for AES-encrypted Write

AES Encryption of Programming Files

Low-power flash devices employ AES as part of the security mechanism that prevents invasive and noninvasive attacks. The mechanism entails encrypting the programming file with AES encryption and then passing the programming file through the AES decryption core, which is embedded in the device. The file is decrypted there, and the device is successfully programmed. The AES master key is stored in on-chip nonvolatile memory (flash). The AES master key can be preloaded into parts in a secure programming environment (such as the Actel In-House Programming center), and then "blank" parts can be shipped to an untrusted programming or manufacturing center for final personalization with an AES-encrypted bitstream. Late-stage product changes or personalization can be implemented easily and securely by simply sending a STAPL file with AES-encrypted data. Secure remote field updates over public networks (such as the Internet) are possible by sending and programming a STAPL file with AES-encrypted data.

The AES key protects the programming data for file transfer into the device, with 128-bit AES encryption. If AES encryption is used, the AES key is stored or preprogrammed into the device. To program, you must use an AES-encrypted file, and the encryption used on the file must match the encryption key already in the device.

The AES key is protected by a FlashLock security Pass Key that is also implemented in each device. The AES key is always protected by the FlashLock Key, and the AES-encrypted file does NOT contain the FlashLock Key. This FlashLock Pass Key technology is exclusive to the Actel flash-based device families. FlashLock Pass Key technology can also be implemented without the AES encryption option, providing a choice of different security levels.

In essence, security features can be categorized into the following three options:

- AES encryption with FlashLock Pass Key protection
- FlashLock protection only (no AES encryption)
- No protection

Each of the above options is explained in more detail in the following sections with application examples and software implementation options.

Advanced Encryption Standard

The 128-bit AES standard (FIPS-192) block cipher is the NIST (National Institute of Standards and Technology) replacement for DES (Data Encryption Standard FIPS46-2). AES has been designed to protect sensitive government information well into the 21st century. It replaces the aging DES, which NIST adopted in 1977 as a Federal Information Processing Standard used by federal agencies to protect sensitive, unclassified information. The 128-bit AES standard has 3.4×10^{38} possible 128-bit key variants, and it has been estimated that it would take 1,000 trillion years to crack 128-bit AES cipher text using exhaustive techniques. Keys are stored (securely) in low-power flash devices in nonvolatile flash memory. All programming files sent to the device can be authenticated by the part prior to programming to ensure that bad programming data is not loaded into the part that may possibly damage it. All programming verification is performed on-chip, ensuring that the contents of low-power flash devices remain secure.

Actel has implemented the 128-bit AES (Rijndael) algorithm in low-power flash devices. With this key size, there are approximately 3.4×10^{38} possible 128-bit keys. DES has a 56-bit key size, which provides approximately 7.2×10^{16} possible keys. In their AES fact sheet, the National Institute of

Standards and Technology uses the following hypothetical example to illustrate the theoretical security provided by AES. If one were to assume that a computing system existed that could recover a DES key in a second, it would take that same machine approximately 149 trillion years to crack a 128-bit AES key. NIST continues to make their point by stating the universe is believed to be less than 20 billion years old.[1]

The AES key is securely stored on-chip in dedicated low-power flash device flash memory and cannot be read out. In the first step, the AES key is generated and programmed into the device (for example, at a secure or trusted programming site). The Actel Designer software tool provides AES key generation capability. After the key has been programmed into the device, the device will only correctly decrypt programming files that have been encrypted with the same key. If the individual programming file content is incorrect, a Message Authentication Control (MAC) mechanism inside the device will fail in authenticating the programming file. In other words, when an encrypted programming file is being loaded into a device that has a different programmed AES key, the MAC will prevent this incorrect data from being loaded, preventing possible device damage. See Figure 13-3 on page 13-4 and Figure 13-4 on page 13-7 for graphical representations of this process.

It is important to note that the user decides what level of protection will be implemented for the device. When AES protection is desired, the FlashLock Pass Key must be set. The AES key is a content protection mechanism, whereas the FlashLock Pass Key is a device protection mechanism. When the AES key is programmed into the device, the device still needs the Pass Key to protect the FPGA and FlashROM contents and the security settings, including the AES key. Using the FlashLock Pass Key prevents modification of the design contents by means of simply programming the device with a different AES key.

AES Decryption and MAC Authentication

Low-power flash devices have a built-in 128-bit AES decryption core, which decrypts the encrypted programming file and performs a MAC check that authenticates the file prior to programming.

MAC authenticates the entire programming data stream. After AES decryption, the MAC checks the data to make sure it is valid programming data for the device. This can be done while the device is still operating. If the MAC validates the file, the device will be erased and programmed. If the MAC fails to validate, then the device will continue to operate uninterrupted.

This will ensure the following:

- Correct decryption of the encrypted programming file
- Prevention of erroneous or corrupted data being programmed during the programming file transfer
- Correct bitstream passed to the device for decryption

1. *National Institute of Standards and Technology, "ADVANCED ENCRYPTION STANDARD (AES) Questions and Answers," 28 January 2002 (10 January 2005). See http://csrc.nist.gov/archive/aes/index1.html for more information.*

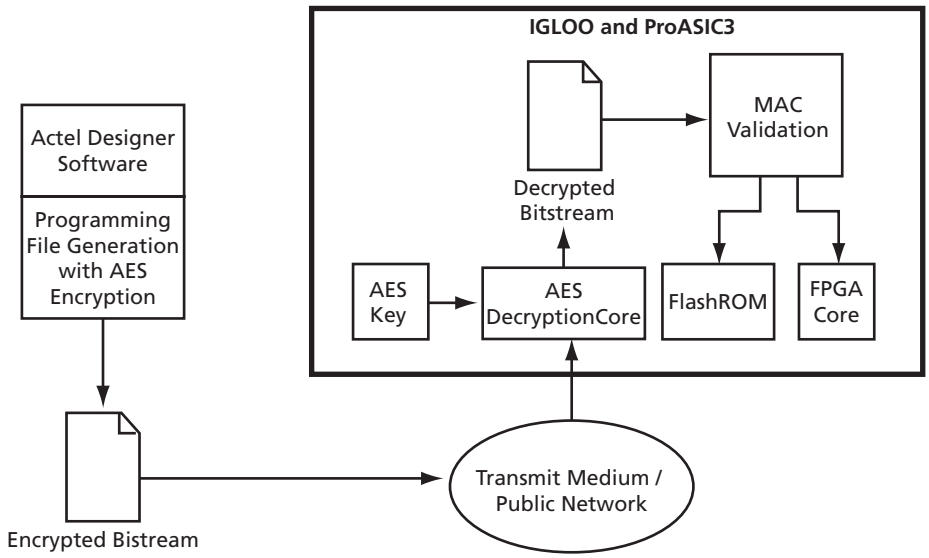


Figure 13-4 **• Example Application Scenario Using AES in IGLOO and ProASIC3 Devices**

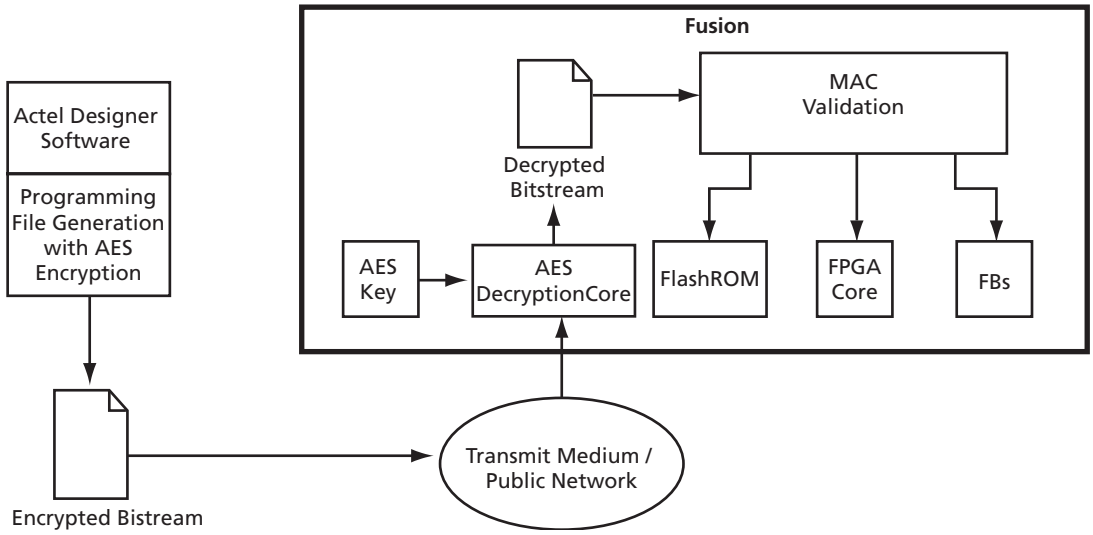


Figure 13-5 **• Example Application Scenario Using AES in Fusion Devices**

FlashLock

Additional Options for IGLOO and ProASIC3 Devices

The user also has the option of prohibiting Write operations to the FPGA array but allowing Verify operations on the FPGA array and/or Read operations on the FlashROM without the use of the FlashLock Pass Key. This option provides the user the freedom of verifying the FPGA array and/or reading the FlashROM contents after the device is programmed, without having to provide the FlashLock Pass Key. The user can incorporate AES encryption on the programming files to better enhance the level of security used.

Permanent Security Setting Options

In applications where a permanent lock is not desired, yet the security settings should not be modifiable, IGLOO and ProASIC3 devices can accommodate this requirement.

This application is particularly useful in cases where a device is located at a remote location and must be reprogrammed with a design or data update. Refer to the "Application 3: Nontrusted Environment—Field Updates/Upgrades" section on page 13-10 for further discussion and examples of how this can be achieved.

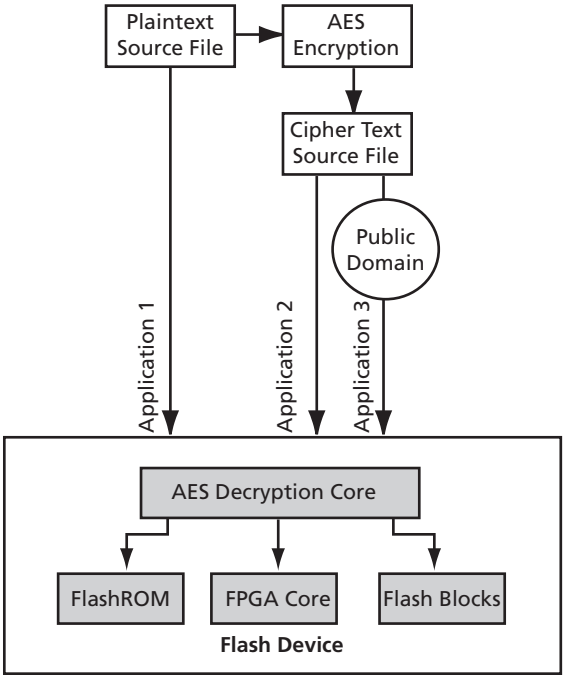
The user must be careful when considering the Permanent FlashLock or Permanent Security Settings option. Once the design is programmed with the permanent settings, it is not possible to reconfigure the security settings already employed on the device. Therefore, exercise careful consideration before programming permanent settings.

Permanent FlashLock

The purpose of the permanent lock feature is to provide the benefits of the highest level of security to IGLOO and ProASIC3 devices. If selected, the permanent FlashLock feature will create a permanent barrier, preventing any access to the contents of the device. This is achieved by permanently disabling Write and Verify access to the array, and Write and Read access to the FlashROM. After permanently locking the device, it has been effectively rendered one-time-programmable. This feature is useful if the intended applications do not require design or system updates to the device.

Security in Action

This section illustrates some applications of the security advantages of Actel's devices (Figure 13-6).



Note: Flash blocks are only used in Fusion devices.

***Figure 13-6* • Security Options**

Application 1: Trusted Environment

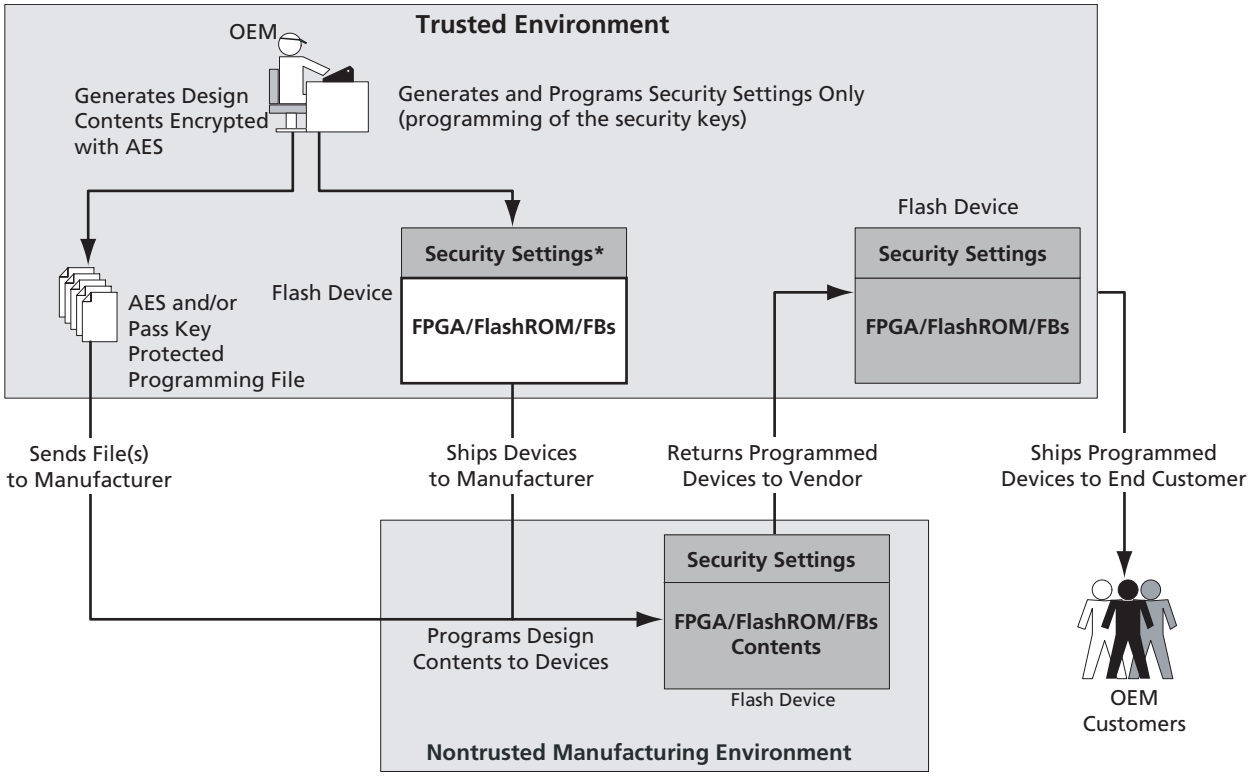
As illustrated in Figure 13-7 on page 13-10, this application allows the programming of devices at design locations where research and development take place. Therefore, encryption is not necessary and is optional to the user. This is often a secure way to protect the design, since the design program files are not sent elsewhere. In situations where production programming is not available at the design location, programming centers (such as Actel In-House Programming) provide a way of programming designs at an alternative, secure, and trusted location. In this scenario, the user generates a STAPL programming file from the Designer software in plaintext format, containing information on the entire design or the portion of the design to be programmed. The user can choose to employ the FlashLock Pass Key feature with the design. Once the design is programmed to unprogrammed devices, the design is protected by this FlashLock Pass Key. If no future programming is needed, the user can consider permanently securing the IGLOO and ProASIC3 device, as discussed in the "Permanent FlashLock" section on page 13-8.

Application 2: Nontrusted Environment—Unsecured Location

Often, programming of devices is not performed in the same location as actual design implementation, to reduce manufacturing cost. Overseas programming centers and contract manufacturers are examples of this scenario.

To achieve security in this case, the AES key and the FlashLock Pass Key can be initially programmed in-house (trusted environment). This is done by generating a programming file with only the security settings and no design contents. The design FPGA core, FlashROM, and (for Fusion) FB contents are generated in a separate programming file. This programming file must be set with the same AES key that was used to program to the device previously so the device will correctly decrypt this encrypted programming file. As a result, the encrypted design content programming file can

be safely sent off-site to nontrusted programming locations for design programming. Figure 13-7 shows a more detailed flow for this application.



Notes:

1. *Programmed portion indicated with dark gray.*
2. *Programming of FBs applies to Fusion only*

Figure 13-7 **• Application 2: Device Programming in a Nontrusted Environment**

Application 3: Nontrusted Environment—Field Updates/Upgrades

Programming or reprogramming of devices may occur at remote locations. Reconfiguration of devices in consumer products/equipment through public networks is one example. Typically, the remote system is already programmed with particular design contents. When design update (FPGA array contents update) and/or data upgrade (FlashROM and/or FB contents upgrade) is necessary, an updated programming file with AES encryption can be generated, sent across public networks, and transmitted to the remote system. Reprogramming can then be done using this AES-encrypted programming file, providing easy and secure field upgrades. Low-power flash devices support this secure ISP using AES. The detailed flow for this application is shown in Figure 13-8 on page 13-11. Refer to *Microprocessor Programming of Actel's Low-Power Flash Devices* for more information.

To prepare devices for this scenario, the user can initially generate a programming file with the available security setting options. This programming file is programmed into the devices before shipment. During the programming file generation step, the user has the option of making the security settings permanent or not. In situations where no changes to the security settings are necessary, the user can select this feature in the software to generate the programming file with permanent security settings. Actel recommends that the programming file use encryption with an AES key, especially when ISP is done via public domain.

For example, if the designer wants to use an AES key for the FPGA array and the FlashROM, **Permanent** needs to be chosen for this setting. At first, the user would do this by choosing the options to use an AES key for the FPGA array and the FlashROM, and then choosing **Permanently lock the security settings**. A unique AES key would be chosen. Once this programming file is

generated and programmed to the devices, the AES key is permanently stored in the on-chip memory, where it is secured safely. The devices would be sent to distant locations for the intended application. When an update is needed, a new programming file must be generated. The programming file must use the same AES key for encryption; otherwise, the authentication will fail and the file will not get programmed in the device.

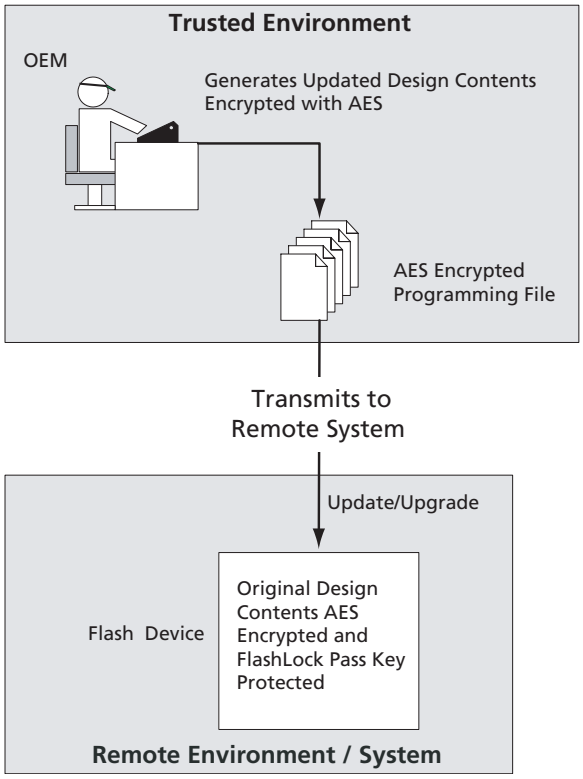


***Figure 13-8* • Application 3: Nontrusted Environment—Field Updates/Upgrades**

FlashROM Security Use Models

Each of the subsequent sections describes in detail the available selections in Actel Designer as an aid to understanding security applications and generating appropriate programming files for those applications. Before proceeding, it is helpful to review Figure 13-7 on page 13-10, which gives a general overview of the programming file generation flow within the Designer software as well as what occurs during the device programming stage. Specific settings are discussed in the following sections.

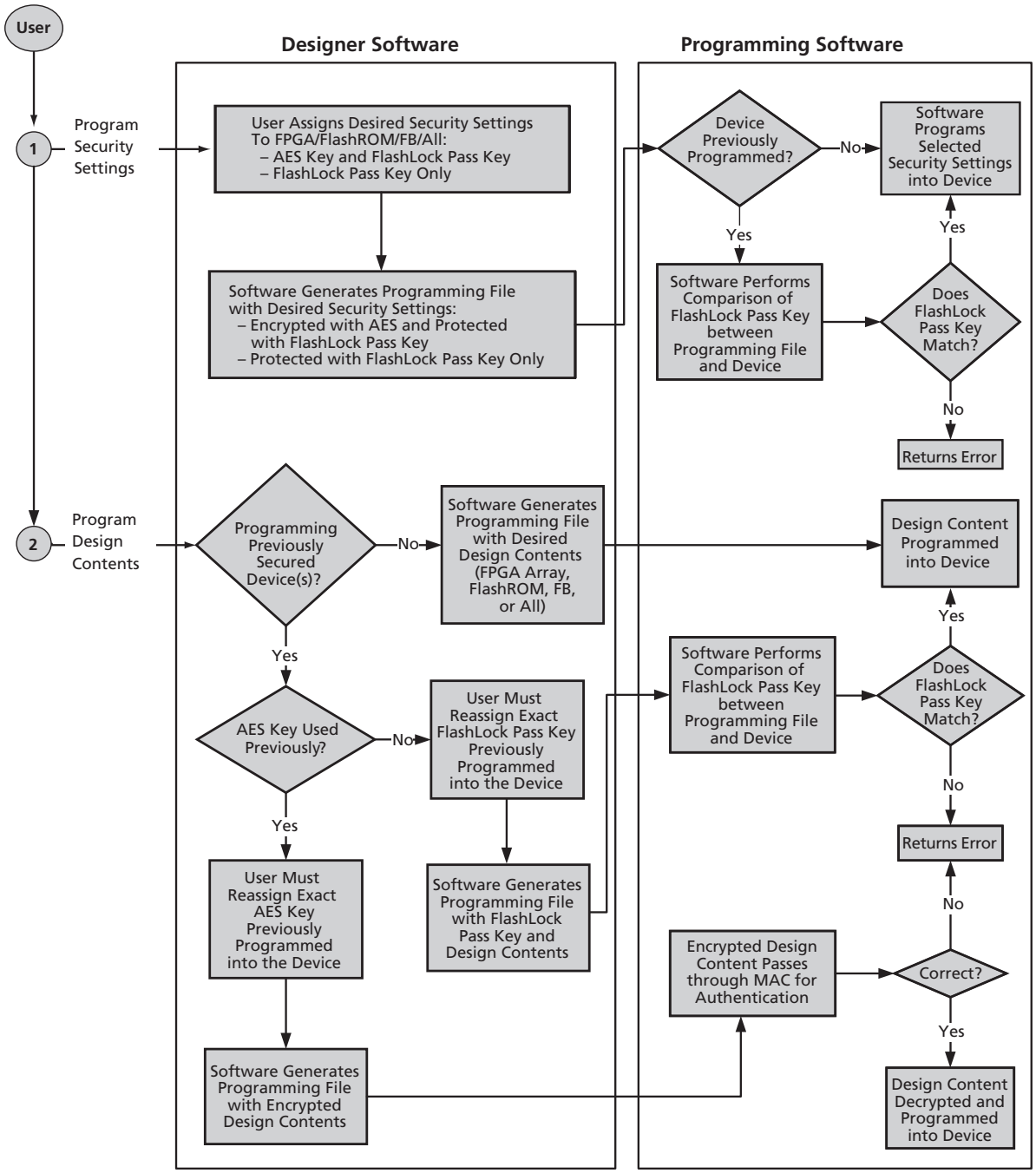
In Figure 13-7 on page 13-10, the flow consists of two sub-flows. Sub-flow 1 describes programming security settings to the device only, and sub-flow 2 describes programming the design contents only.

In Application 1, described in the "Application 1: Trusted Environment" section on page 13-9, the user does not need to generate separate files but can generate one programming file containing both security settings and design contents. Then programming of the security settings and design contents is done in one step. Both sub-flow 1 and sub-flow 2 are used.

In Application 2, described in the "Application 2: Nontrusted Environment—Unsecured Location" section on page 13-9, the trusted site should follow sub-flows 1 and 2 separately to generate two separate programming files. The programming file from sub-flow 1 will be used at the trusted site to program the device(s) first. The programming file from sub-flow 2 will be sent off-site for production programming.

In Application 3, described in the "Application 3: Nontrusted Environment—Field Updates/Upgrades" section on page 13-10, typically only sub-flow 2 will be used because only updates to the design content portion are needed and no security settings need to be changed.

In the event that update of the security settings is necessary, see the "Reprogramming Devices" section on page 13-21 for details. For more information on programming low-power flash devices, refer to *In-System Programming (ISP) of Actel's Low-Power Flash Devices Using FlashPro3*



Note: If programming the Security Header only, just perform sub-flow 1.
If programming design content only, just perform sub-flow 2.

***Figure 13-9* • Security Programming Flows**

Generating Programming Files

Generation of the Programming File in a Trusted Environment—Application 1

As discussed in the "Application 1: Trusted Environment" section on page 13-9, in a trusted environment, the user can choose to program the device with plaintext bitstream content. It is possible to use plaintext for programming even when the FlashLock Pass Key option has been selected. In this application, it is not necessary to employ AES encryption protection. For AES encryption settings, refer to the next sections.

The generated programming file will include the security setting (if selected) and the plaintext programming file content for the FPGA array, FlashROM, and/or FB. These options are indicated in Table 13-2 and Table 13-3.

Table 13-2 • **IGLOO and ProASIC3 Plaintext Security Options, No AES**

Security Protection	FlashROM Only	FPGA Core Only	Both FlashROM and FPGA
No AES / No FlashLock	✓	✓	✓
FlashLock only	✓	✓	✓
AES and FlashLock	–	–	–

Table 13-3 • **Fusion Plaintext Security Options**

Security Protection	FlashROM Only	FPGA Core Only	FB Core Only	All
No AES / No FlashLock	✓	✓	✓	✓
FlashLock	✓	✓	✓	✓
AES and FlashLock	–	–	–	–

Note: For all instructions, the programming of Flash Blocks refers to Fusion only.

For this scenario, generate the programming file as follows:

1. Select the **Silicon features to be programmed** (Security Settings, FPGA Array, FlashROM, Flash Memory Block), as shown in Figure 13-10 on page 13-14 and Figure 13-11 on page 13-14. Click **Next**.

   If **Security Settings** is selected (i.e., the FlashLock security Pass Key feature), an additional dialog will be displayed to prompt you to select the security level setting. If no security setting is selected, you will be directed to Step 3.

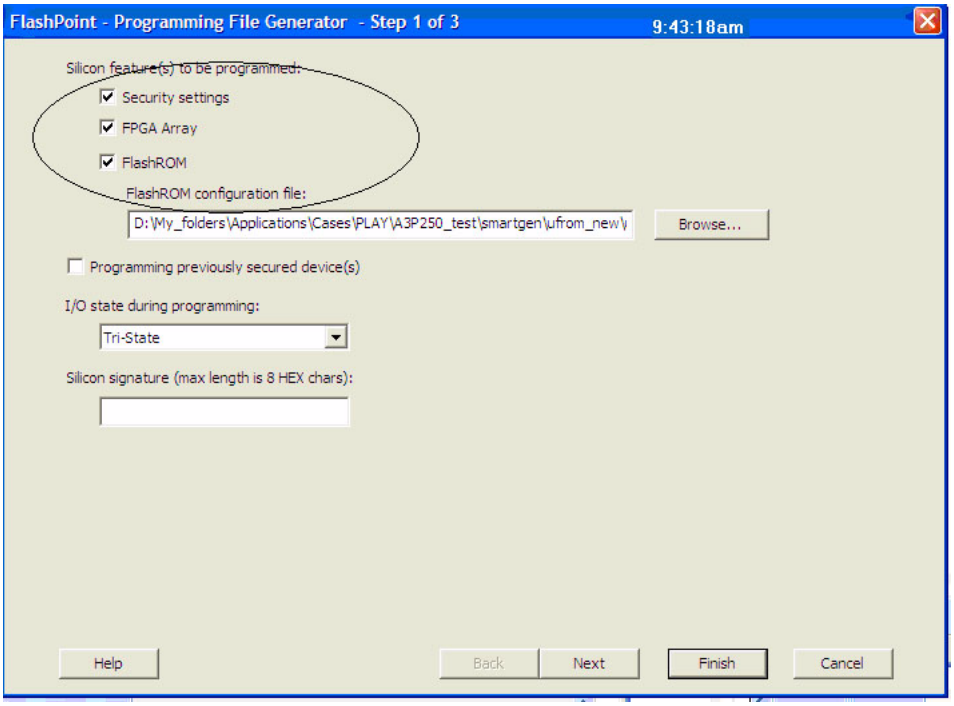


Figure 13-10 • **All Silicon Features Checked for IGLOO and ProASIC3 Devices**

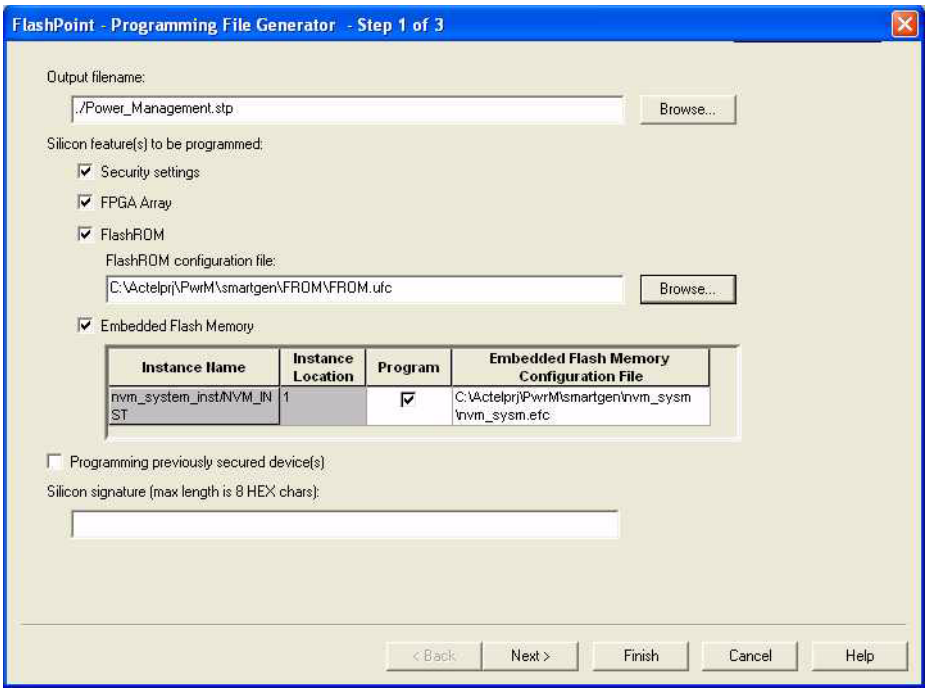


Figure 13-11 • **All Silicon Features Checked for Fusion**

2. Choose the appropriate security level setting and enter a FlashLock Pass Key. The default is the **Medium** security level (Figure 13-12). Click **Next**.

   If you want to select different options for the FPGA and/or FlashROM, this can be set by clicking **Custom Level**. Refer to the "Advanced Options" section on page 13-22 for different custom security level options and descriptions of each.

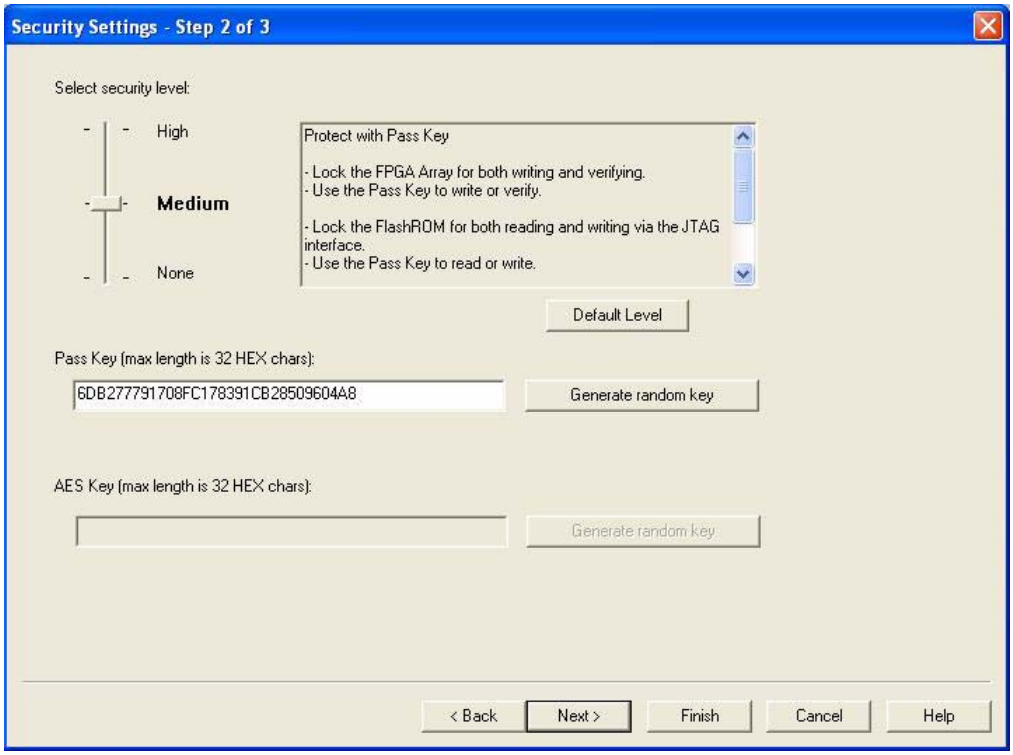


Figure 13-12 • **Medium Security Level Selected for Low-Power Flash Devices**

3. Choose the desired settings for the FlashROM configurations to be programmed (Figure 13-13). Click **Finish** to generate the STAPL programming file for the design.

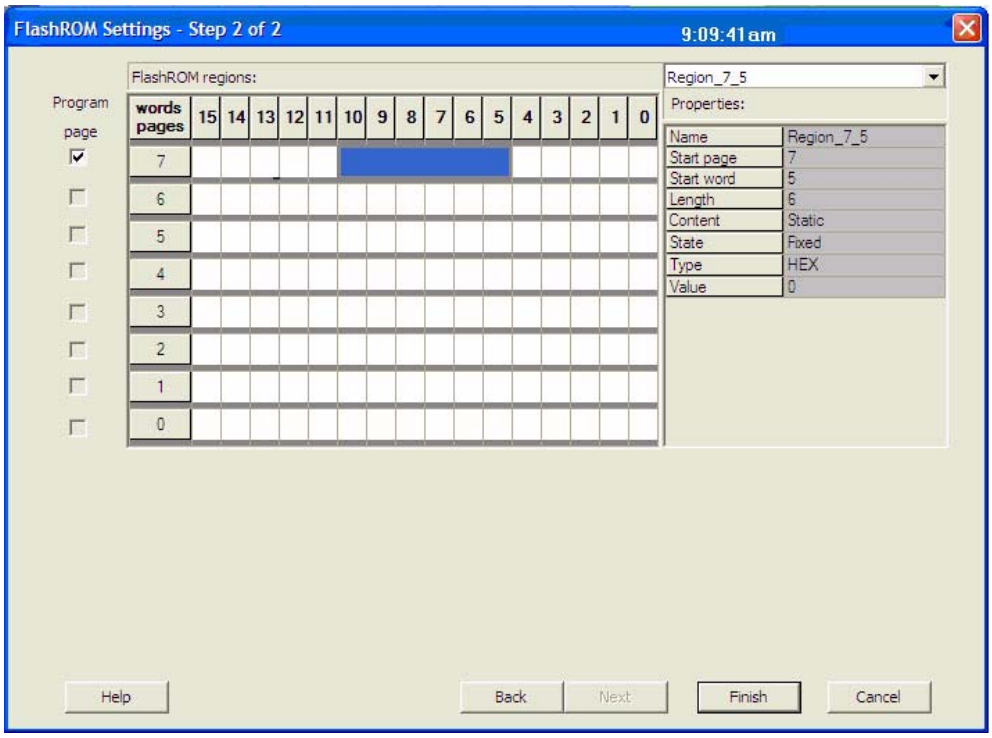


Figure 13-13 **• FlashROM Configuration Settings for Low-Power Flash Devices**

Generation of Security Header Programming File Only—Application 2

As mentioned in the "Application 2: Nontrusted Environment—Unsecured Location" section on page 13-9, the designer may employ FlashLock Pass Key protection or FlashLock Pass Key with AES encryption on the device before sending it to a nontrusted or unsecured location for device programming. To achieve this, the user needs to generate a programming file containing only the security settings desired (Security Header programming file).

Note: If AES encryption is configured, FlashLock Pass Key protection must also be configured.

The available security options are indicated in Table 13-4 and Table 13-5 on page 13-17.

Table 13-4 **• FlashLock Security Options for IGLOO and ProASIC3**

Security Option	FlashROM Only	FPGA Core Only	Both FlashROM and FPGA
No AES / No FlashLock	–	–	–
FlashLock only	✓	✓	✓
AES and FlashLock	✓	✓	✓

Table 13-5 • **FlashLock Security Options for Fusion**

Security Option	FlashROM Only	FPGA Core Only	FB Core Only	All
No AES / No FlashLock	–	–	–	–
FlashLock	✓	✓	✓	✓
AES and FlashLock	✓	✓	✓	✓

For this scenario, generate the programming file as follows:

1. Select only the **Security settings** option, as indicated in Figure 13-14 and Figure 13-15 on page 13-18. Click **Next**.

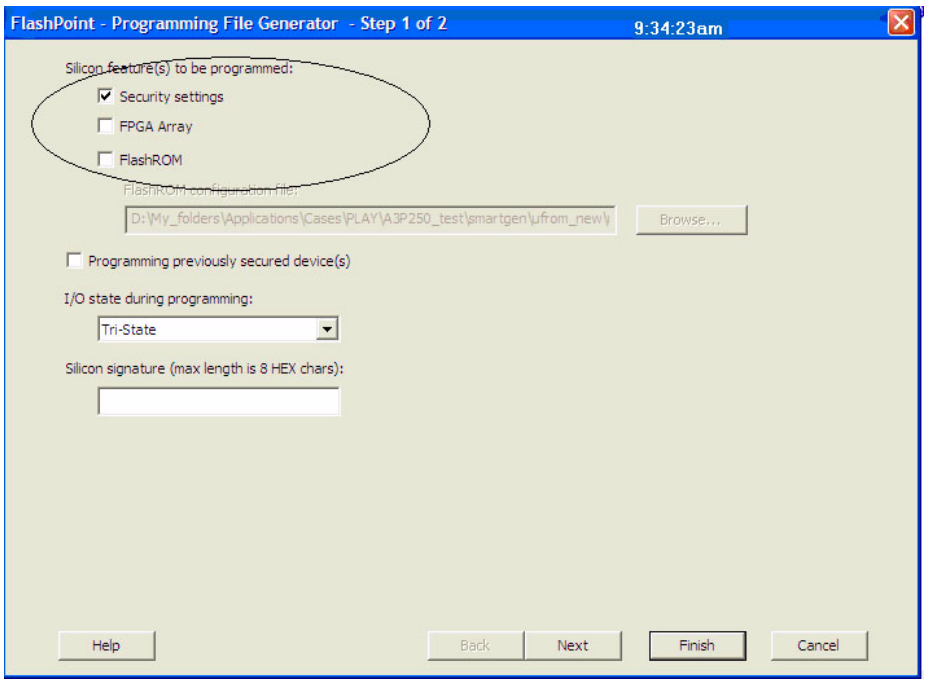


Figure 13-14 • **Programming IGLOO and ProASIC3 Security Settings Only**

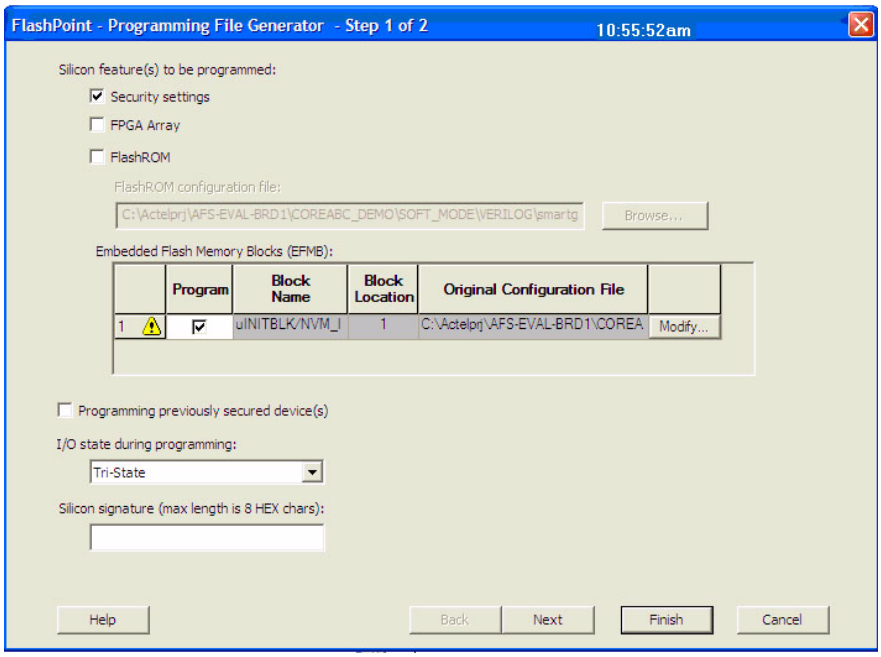


Figure 13-15 • **Programming Fusion Security Settings Only**

2. Choose the desired security level setting and enter the key(s).
   - The **High** security level employs FlashLock Pass Key with AES Key protection.
   - The **Medium** security level employs FlashLock Pass Key protection only.

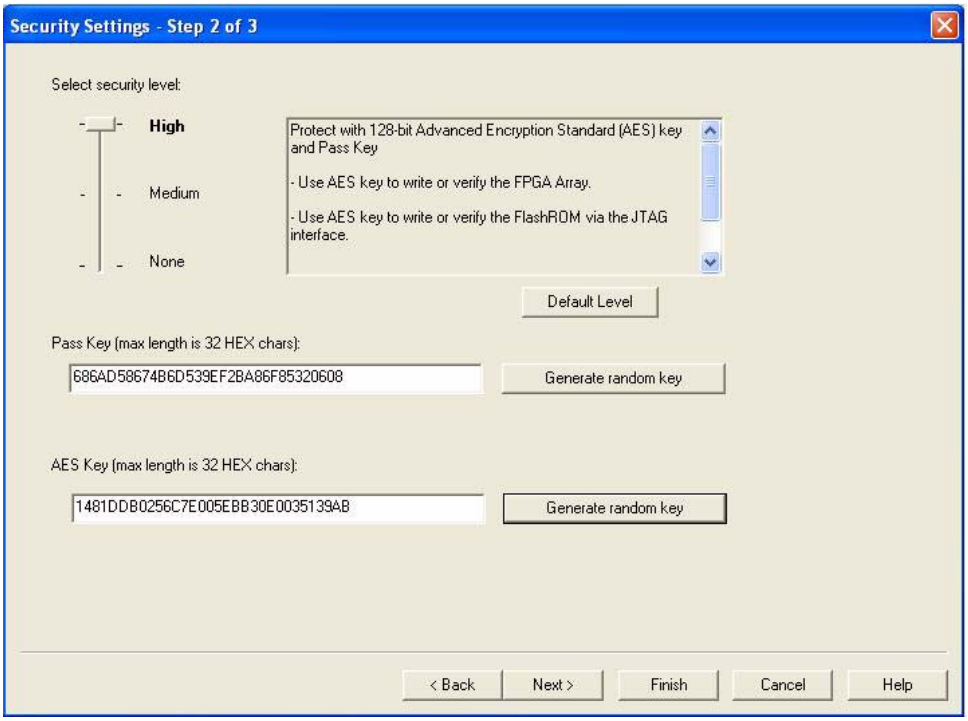


Figure 13-16 • **High Security Level to Implement FlashLock Pass Key and AES Key Protection**

Table 13-6 and Table 13-7 show all available options. If you want to implement custom levels, refer to the "Advanced Options" section on page 13-22 for information on each option and how to set it.

3. When done, click **Finish** to generate the Security Header programming file.

Table 13-6 • **All IGLOO and ProASIC3 Header File Security Options**

Security Option	FlashROM Only	FPGA Core Only	Both FlashROM and FPGA
No AES / No FlashLock	✓	✓	✓
FlashLock only	✓	✓	✓
AES and FlashLock	✓	✓	✓

Note: ✓ = options that may be used

Table 13-7 • **All Fusion Header File Security Options**

Security Option	FlashROM Only	FPGA Core Only	FB Core Only	All
No AES / No FlashLock	✓	✓	✓	✓
FlashLock	✓	✓	✓	✓
AES and FlashLock	✓	✓	✓	✓

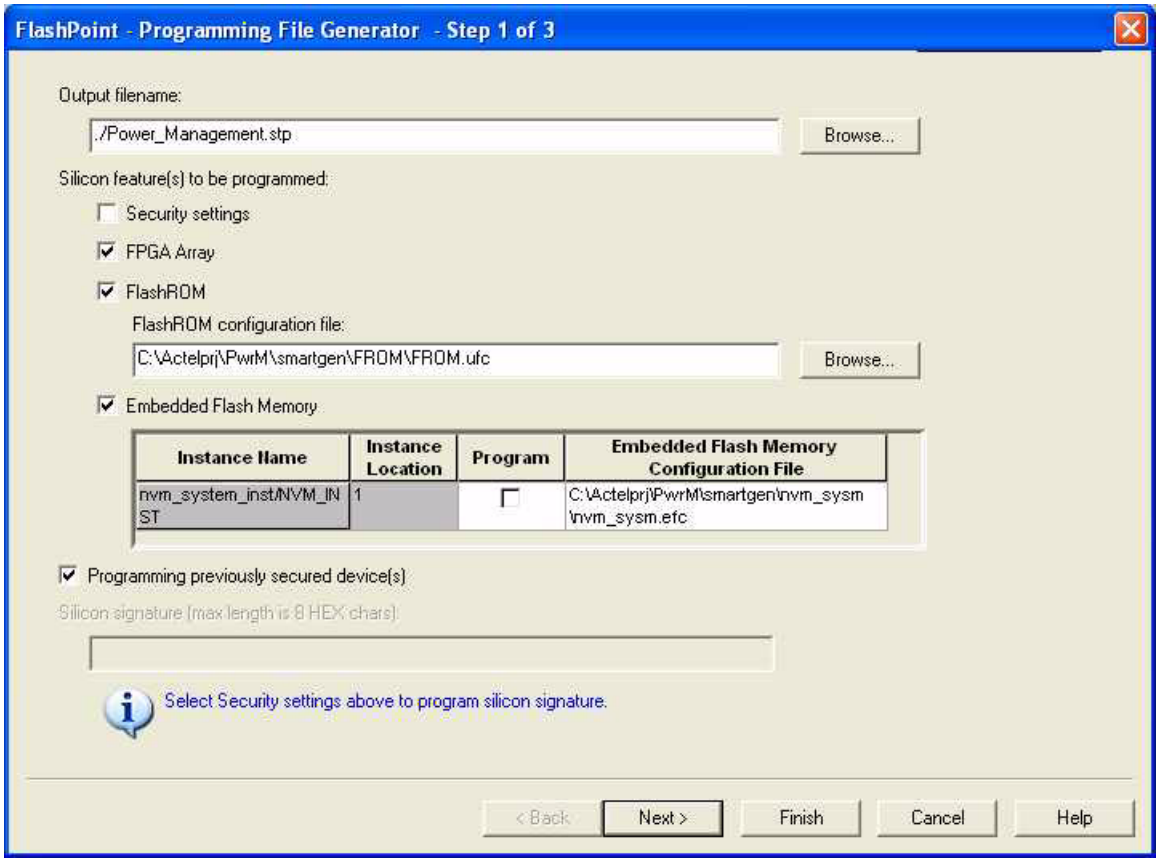
Generation of Programming Files with AES Encryption—Application 3

This section discusses how to generate design content programming files needed specifically at unsecured or remote locations to program devices with a security header (FlashLock Pass Key and AES key) already programmed ("Application 2: Nontrusted Environment—Unsecured Location" section on page 13-9 and "Application 3: Nontrusted Environment—Field Updates/Upgrades" section on page 13-10). In this case, the encrypted programming file must correspond to the AES key already programmed into the device. If AES encryption was previously selected to encrypt the FlashROM, FB, and FPGA array, AES encryption must be set when generating the programming file for them. AES encryption can be applied to the FlashROM only, the FB only, the FPGA array only, or all. The user must ensure both the FlashLock Pass Key and the AES key match those already programmed to the device(s), and all security settings must match what was previously programmed. Otherwise, the encryption and/or device unlocking will not be recognized when attempting to program the device with the programming file.

The generated programming file will be AES-encrypted.

In this scenario, generate the programming file as follows:

1. Deselect the **Security settings** and select the portion of the device to be programmed (Figure 13-17 on page 13-20). Select **Programming previously secured device(s)**. Click **Next**.



Note: The settings in this figure are used to show the generation of an AES-encrypted programming file for the FPGA array, FlashROM, and FB contents. One or all locations may be selected for encryption.

***Figure 13-17* • Settings to Program a Device Secured with FlashLock and using AES Encryption**

Choose the **High** security level to reprogram devices using both the FlashLock Pass Key and AES key protection (Figure 13-18 on page 13-21). Enter the AES key and click **Next**.

A device that has already been secured with FlashLock and has an AES key loaded must recognize the AES key to program the device and generate a valid bitstream in authentication. The FlashLock Key is only required to unlock the device and change the security settings.

This is what makes it possible to program in an untrusted environment. The AES key is protected inside the device by the FlashLock Key, so you can only program if you have the correct AES key. In fact, the AES key is not in the programming file either. It is the key used to encrypt the data in the file. The same key previously programmed with the FlashLock Key matches to decrypt the file.

If you had an AES-encrypted file programmed to a device without FlashLock, this would not be secure, since without FlashLock to protect the AES key, you could simply reprogram the AES key first, then program with any AES key you wanted or no AES key at all. This option is therefore not available in the software.

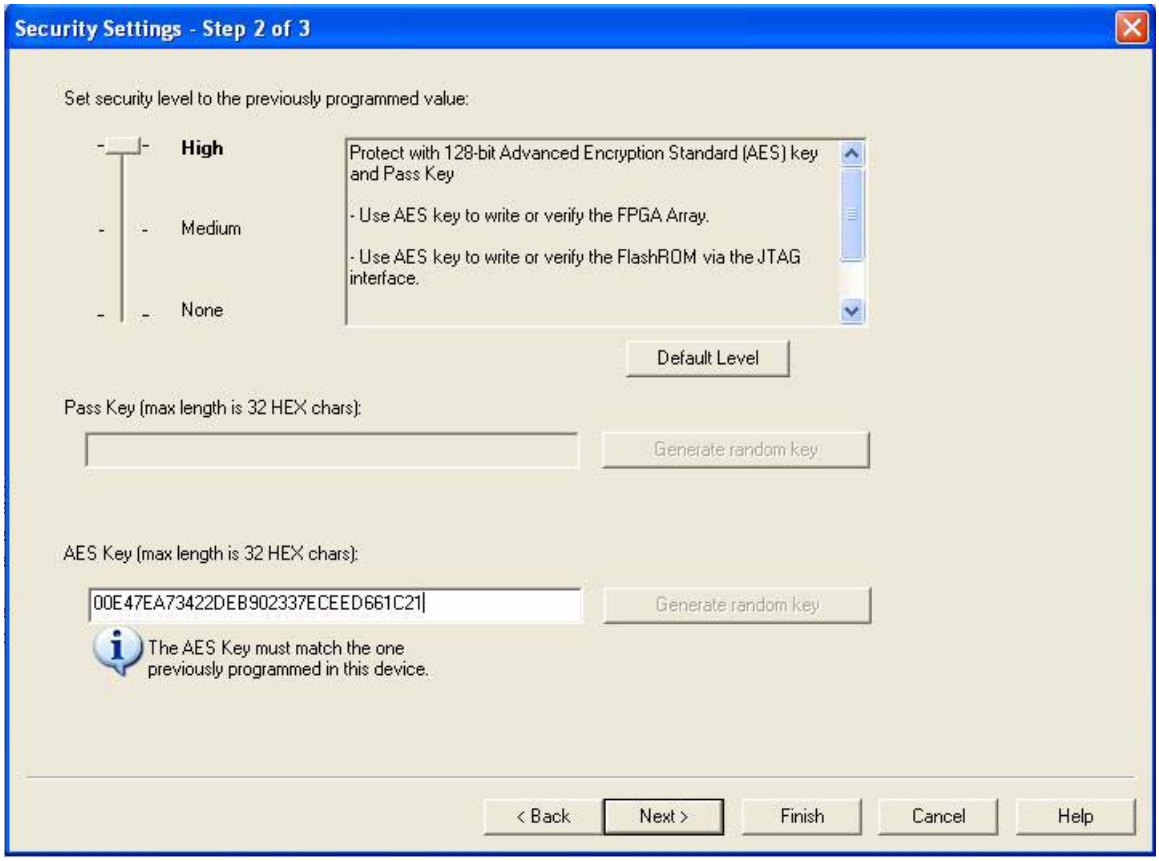


Figure 13-18 **• Security Level Set High to Reprogram Device with AES Key**

Programming with this file is intended for an unsecured environment. The AES key encrypts the programming file with the same AES key already used in the device and utilizes it to program the device.

Reprogramming Devices

Previously programmed devices can be reprogrammed using the steps in the "Generation of the Programming File in a Trusted Environment—Application 1" section on page 13-13 and "Generation of Security Header Programming File Only—Application 2" section on page 13-16. In the case where a FlashLock Pass Key has been programmed previously, the user must generate the new programming file with a FlashLock Pass Key that matches the one previously programmed into the device. The software will check the FlashLock Pass Key in the programming file against the FlashLock Pass Key in the device. The keys must match before the device can be unlocked to perform further programming with the new programming file.

Figure 13-10 on page 13-14 and Figure 13-11 on page 13-14 show the option **Programming previously secured device(s)**, which the user should select before proceeding. Upon going to the next step, the user will be notified that the same FlashLock Pass Key needs to be entered, as shown in Figure 13-19 on page 13-22.

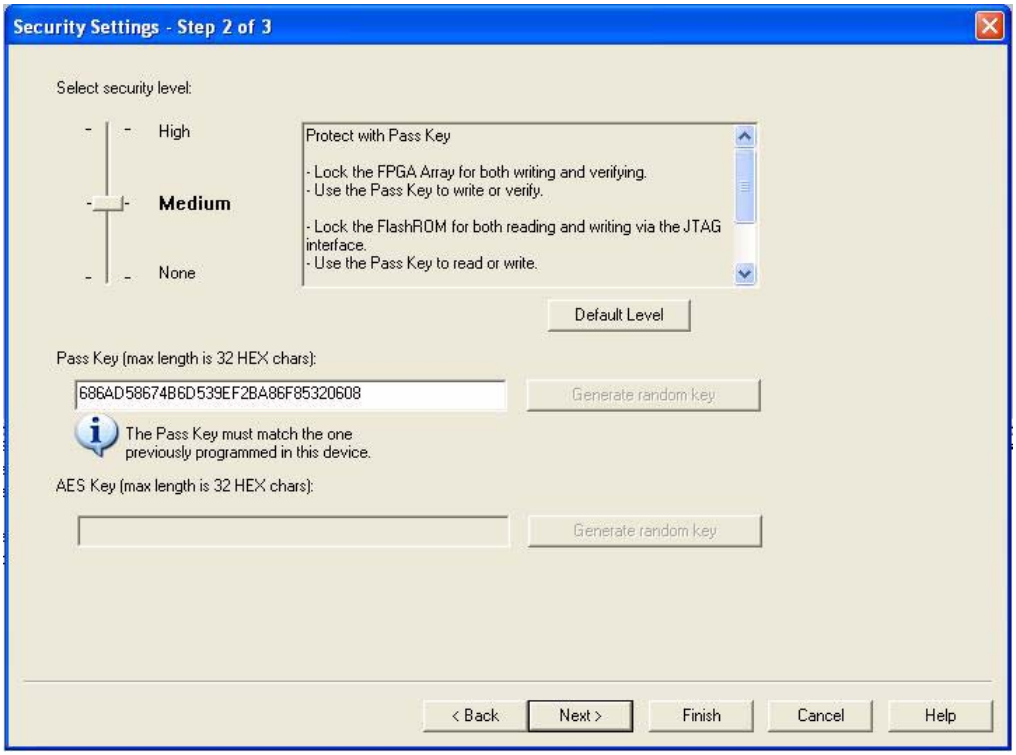


Figure 13-19 **• FlashLock Pass Key, Previously Programmed Devices**

It is important to note that when the security settings need to be updated, the user also needs to select the **Security settings** check box in Step 1, as shown in Figure 13-10 on page 13-14 and Figure 13-11 on page 13-14, to modify the security settings. The user must consider the following:

- If only a new AES key is necessary, the user must re-enter the same Pass Key previously programmed into the device in Designer and then generate a programming file with the same Pass Key and a different AES key. This ensures the programming file can be used to access and program the device and the new AES key.
- If a new Pass Key is necessary, the user can generate a new programming file with a new Pass Key (with the same or a new AES key if desired). However, for programming, the user must first load the original programming file with the Pass Key that was previously used to unlock the device. Then the new programming file can be used to program the new security settings.

Advanced Options

As mentioned, there may be applications where more complicated security settings are required. The "Custom Security Levels" section in the *FlashPoint User's Guide* describes different advanced options available to aid the user in obtaining the best available security settings.

Programming File Header Definition

In each STAPL programming file generated, there will be information about how the AES key and FlashLock Pass Key are configured. Table 13-8 shows the header definitions in STAPL programming files for different security levels.

Table 13-8 • **STAPL Programming File Header Definitions by Security Level**

Security Level	STAPL File Header Definition
No security (no FlashLock Pass Key or AES key)	`NOTE "SECURITY" "Disable";`
FlashLock Pass Key with no AES key	`NOTE "SECURITY" "KEYED ";`
FlashLock Pass Key with AES key	`NOTE "SECURITY" "KEYED ENCRYPT ";`
Permanent Security Settings option enabled	`NOTE "SECURITY" "PERMLOCK ENCRYPT ";`
AES-encrypted FPGA array (for programming updates)	`NOTE "SECURITY" "ENCRYPT CORE ";`
AES-encrypted FlashROM (for programming updates)	`NOTE "SECURITY" "ENCRYPT FROM ";`
AES-encrypted FPGA array and FlashROM (for programming updates)	`NOTE "SECURITY" "ENCRYPT FROM CORE ";`

Example File Headers

STAPL Files Generated with FlashLock Key and AES Key Contain Key Information

- FlashLock Key / AES key indicated in STAPL file header definition
- Intended ONLY for secured/trusted environment programming applications

```
=============================================
NOTE "CREATOR" "Designer Version: 6.1.1.108";
NOTE "DEVICE" "A3PE600";
NOTE "PACKAGE" "208 PQFP";
NOTE "DATE" "2005/04/08";
NOTE "STAPL_VERSION" "JESD71";
NOTE "IDCODE" "$123261CF";
NOTE "DESIGN" "counter32";
NOTE "CHECKSUM" "$EDB9";
NOTE "SAVE_DATA" "FRomStream";
NOTE "SECURITY" "KEYED ENCRYPT ";
NOTE "ALG_VERSION" "1";
NOTE "MAX_FREQ" "20000000";
NOTE "SILSIG" "$00000000";
NOTE "PASS_KEY" "$00123456789012345678901234567890";
NOTE "AES_KEY" "$ABCDEFABCDEFABCDEFABCDEFABCDEFAB";
=============================================
```

STAPL File with AES Encryption

- Does not contain AES key / FlashLock Key information
- Intended for transmission through web or service to unsecured locations for programming

```
=============================================
NOTE "CREATOR" "Designer Version: 6.1.1.108";
NOTE "DEVICE" "A3PE600";
NOTE "PACKAGE" "208 PQFP";
NOTE "DATE" "2005/04/08";
NOTE "STAPL_VERSION" "JESD71";
NOTE "IDCODE" "$123261CF";
NOTE "DESIGN" "counter32";
NOTE "CHECKSUM" "$EF57";
NOTE "SAVE_DATA" "FRomStream";
NOTE "SECURITY" "ENCRYPT FROM CORE ";
NOTE "ALG_VERSION" "1";
NOTE "MAX_FREQ" "20000000";
NOTE "SILSIG" "$00000000";
```

Conclusion

The new and enhanced security features offered in Actel IGLOO, Fusion, and ProASIC3 devices provide state-of-the-art security to designs programmed into these flash-based devices. Actel low-power flash devices employ the encryption standard used by NIST and the U.S. government—AES using the 128-bit Rijndael algorithm.

The combination of an on-chip AES decryption engine and Actel FlashLock technology provides the highest level of security against invasive attacks and design theft, implementing the most robust and secure ISP solution. These security features protect IP within the FPGA and protect the system from cloning, wholesale “black box” copying of a design, invasive attacks, and explicit IP or data theft.

Glossary

Term	Explanation
Security Header programming file	Programming file used to program the FlashLock Pass Key and/or AES key into the device to secure the FPGA, FlashROM, and/or FBs.
AES (encryption) key	128-bit key defined by the user when the AES encryption option is set in the Actel Designer software when generating the programming file.
FlashLock Pass Key	128-bit key defined by the user when the FlashLock option is set in the Actel Designer software when generating the programming file. The FlashLock Key protects the security settings programmed to the device. Once a device is programmed with FlashLock, whatever settings were chosen at that time are secure.
FlashLock	The combined security features that protect the device content from attacks. These features are the following: • Flash technology that does not require an external bitstream to program the device • FlashLock Pass Key that secures device content by locking the security settings and preventing access to the device as defined by the user • AES key that allows secure, encrypted device reprogrammability

References

National Institute of Standards and Technology. "ADVANCED ENCRYPTION STANDARD (AES) Questions and Answers." 28 January 2002 (10 January 2005).
See http://csrc.nist.gov/archive/aes/index1.html for more information.

Related Documents

Handbook Documents

FlashROM in Actel's Low-Power Flash Devices

http://www.actel.com/documents/LPD_FlashROM_HBs.pdf

Programming ProASIC3/E Using a Microprocessor

http://www.actel.com/documents/LPD_Microprocessor_HBs.pdf

In-System Programming (ISP) of Actel's Low-Power Flash Devices Using FlashPro3

http://www.actel.com/documents/LPD_ISP_HBs.pdf

User's Guides

FlashPoint User's Guide

http://www.actel.com/documents/flashpoint_ug.pdf

Part Number and Revision Date

This document contains content extracted from the Device Architecture section of the datasheet, combined with content previously published as an application note describing features and functions of the device. To improve usability for customers, the device architecture information has now been combined with usage information, to reduce duplication and possible inconsistencies in published information. No technical changes were made to the datasheet content unless explicitly listed. Changes to the application note content were made only to be consistent with existing datasheet information.

Part Number 51700094-014-2

Revised June 2008

List of Changes

The following table lists critical changes that were made in the current version of the chapter.

Previous Version	Changes in Current Version (v1.2)	Page
v1.1 (March 2008)	The following changes were made to the family descriptions in Table 13-1 · Low-Power Flash Families: • ProASIC3L was updated to include 1.5 V. • The number of PLLs for ProASIC3E was changed from five to six.	13-2
v1.0 (January 2008)	The chapter was updated to include the IGLOO PLUS family and information regarding 15 k gate devices.	N/A
	The "IGLOO Terminology" section and "ProASIC3 Terminology" section are new.	13-2

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14 – In-System Programming (ISP) of Actel's Low-Power Flash Devices Using FlashPro3

Introduction

Actel's low-power flash devices are all in-system programmable. This document describes the general requirements for programming a device and specific requirements for the FlashPro3 programmer.

IGLOO,® Fusion, and ProASIC®3 devices offer a low-power, single-chip, live-at-power-up solution with the ASIC advantages of security and low unit cost through nonvolatile flash technology. Each device contains 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications such as Internet Protocol (IP) addressing, user system preference storage, device serialization, or subscription-based business models. Fusion, IGLOO, and ProASIC3 devices offer the best in-system programming (ISP) solution, FlashLock® security features, and AES-decryption-based ISP.

ISP Architecture

Low-power flash devices support ISP via JTAG and require a single V_{PUMP} voltage of 3.3 V during programming. In addition, programming via a microcontroller in a target system is also supported.

Refer to *Microprocessor Programming of Actel's Low-Power Flash Devices*.

Family-specific support:

- Fusion, ProASIC3, and ProASIC3E devices support ISP.
- ProASIC3L devices operate using a 1.2 V core voltage and support ISP at 1.5 V only. Voltage switching is required in-system to switch from a 1.2 V core to 1.5 V core for programming.
- IGLOO and IGLOOe V5 devices can be programmed in-system when the device is using a 1.5 V supply voltage to the FPGA core.

IGLOO, IGLOO PLUS, and IGLOOe V2 devices can operate using either a 1.2 V core voltage or a 1.5 V core voltage. Although the device can operate at 1.2 V core voltage, the device can only be reprogrammed when all supplies (V_{CC}, V_{CCI}, and V_{JTAG}) are at 1.5 V. Voltage switching is required in-system to switch from a 1.2 V core to 1.5 V core for programming.

IGLOO devices cannot be programmed in-system when the device is in Flash*Freeze mode. The device should exit Flash*Freeze mode and be in normal operation for programming to start. Programming operations in IGLOO devices can be achieved when the device is in normal operating mode and a 1.5 V core voltage is used.

JTAG 1532

IGLOO and ProASIC3 devices support the JTAG-based IEEE 1532 standard for ISP. To start JTAG operations, the IGLOO device should exit Flash*Freeze mode and be in normal operation before starting to send JTAG commands to the device. As part of this support, when a device is in an unprogrammed state, all user I/O pins are disabled. This is achieved by keeping the global IO_EN signal deactivated, which also has the effect of disabling the input buffers. The SAMPLE/PRELOAD instruction captures the status of pads in parallel and shifts them out as new data is shifted in for loading into the Boundary Scan Register (BSR). When the device is in an unprogrammed state, the SAMPLE/PRELOAD instruction has no effect on I/O status; however, it will continue to shift in new data to be loaded into the BSR. Therefore, when SAMPLE/PRELOAD is used on an unprogrammed device, the BSR will be loaded with undefined data. For JTAG timing information on setup, hold, and fall times, refer to the *FlashPro User's Guide*.

ISP Support in Low-Power Devices

The low-power flash families listed in Table 14-1 support the ISP feature and the functions described in this document.

Table 14-1 • **Low-Power Flash Families**

Family[1]	Description	Timing Numbers[2]
IGLOO	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*IGLOO DC and Switching Characteristics*
IGLOO PLUS	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology and enhanced I/O capabilities	*IGLOO PLUS DC and Switching Characteristics*
IGLOOe	IGLOO devices enhanced with higher density, five additional PLLs, and additional I/O standards	*IGLOOe DC and Switching Characteristics*
ProASIC3L	Low-power, high-performance 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*ProASIC3L DC and Switching Characteristics*
ProASIC3	Low-power, high-performance 1.5 V FPGAs	*ProASIC3 DC and Switching Characteristics*
ProASIC3E	ProASIC3 enhanced with higher density, six additional PLLs, and additional I/O standards	*ProASIC3E DC and Switching Characteristics*
ProASIC3 Automotive	Low-power, high-performance FPGAs qualified for automotive applications	*Automotive ProASIC3 DC and Switching Characteristics*
Fusion	Low-power mixed-signal Programmable System Chip (PSC)	*Fusion DC and Power Characteristics*

Notes:

1. *The family names are linked to the appropriate product brief.*
2. *The timing number links go to the relevant timing numbers in the datasheet.*

Actel's low-power flash devices (listed in Table 14-1) provide a selection of low-power, secure, live-at-power-up, single-chip solutions. The nonvolatile flash-based devices do not require a boot PROM and incorporate FlashLock® technology, which provides a unique combination of reprogrammability and design security without external overhead. Only low-power flash FPGAs can offer these advantages.

Actel IGLOO PLUS FPGAs are the industry-leading 1.2 V ultra-low-power programmable logic devices (PLDs) and consume 90% less static power and over 50% less dynamic power than PLD alternatives, while ProASIC3L devices offer a balance of low power and higher performance.

Flash*Freeze technology used in IGLOO, IGLOO PLUS, and ProASIC3L devices enables easy entry to and exit from the ultra-low power mode, which consumes as little as 5 µW, while retaining SRAM and register data. IGLOO PLUS also offers the ability to hold I/O state in Flash*Freeze mode. Flash*Freeze technology simplifies power management through I/O and clock management without the need to turn off voltages, I/Os, or clocks at the system level. Entering and exiting Flash*Freeze mode takes less than 1 µs.

The Actel Fusion® family, based on the highly successful ProASIC3 flash FPGA architecture, has been designed as a high-performance, mixed-signal Programmable System Chip. Fusion supports many peripherals, including embedded flash memory, analog-to-digital converter (ADC), high-drive outputs, RC and crystal oscillators, and real-time counter (RTC). The total available on-chip memory, including the flash array blocks, is greater than that found in SRAM FPGAs.

IGLOO Terminology

In documentation, the term IGLOO families or IGLOO devices refers to all IGLOO families as listed in Table 14-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

ProASIC3 Terminology

In documentation, the term ProASIC3 families or ProASIC3 devices refers to all ProASIC3 families as listed in Table 14-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

Programming Voltage (V_{PUMP}) and V_{JTAG}

Low-power flash devices support on-chip charge pumps, and therefore require only a single 3.3 V programming voltage for the V_{PUMP} pin during programming. When the device is not being programmed, the V_{PUMP} pin can be left floating or can be tied (pulled up) to any voltage between 0 V and 3.6 V. During programming, the target board or the FlashPro3 programmer can provide V_{PUMP}. FlashPro3 is capable of supplying V_{PUMP} to a single device. If more than one device is to be programmed using FlashPro3 on a given board, FlashPro3 should not be relied on to supply the V_{PUMP} voltage.

Low-power flash device I/Os support a bank-based, voltage-supply architecture that simultaneously supports multiple I/O voltage standards (Table 14-2 on page 14-3). By isolating the JTAG power supply in a separate bank from the user I/Os, low-power flash devices provide greater flexibility with supply selection and simplify power supply and printed circuit board (PCB) design. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Actel recommends that TCK be tied to GND or V_{JTAG} when not used. This prevents a possible totempole current on the input buffer stage. For TDI, TMS, and TRST pins, the devices provide an internal nominal 10 kΩ pull-up resistor. During programming, all I/O pins, except for JTAG interface pins, are tristated and weakly pulled up to V_{CCI}. This isolates the part and prevents the signals from floating. The JTAG interface pins are driven by the FlashPro3 during programming, including the TRST pin, which is driven HIGH.

Table 14-2 • **Power Supplies**

Power Supply	Programming Mode	Current during Programming
V_{CC}	1.5 V	< 70 mA
V_{CCI}	1.5 V / 1.8 V / 2.5 V / 3.3 V (bank-selectable)	I/Os are weakly pulled up.
V_{JTAG}	1.5 V / 1.8 V / 2.5 V / 3.3 V	< 20 mA
V_{PUMP}	3.0 V to 3.6 V	< 80 mA

Note: All supply voltages should be at 1.5 V or higher, regardless of the setting during normal operation.

IEEE 1532 (JTAG) Interface

The supported industry-standard IEEE 1532 programming interface builds on the IEEE 1149.1 (JTAG) standard. IEEE 1532 defines the standardized process and methodology for ISP. Both silicon and software issues are addressed in IEEE 1532 to create a simplified ISP environment. Any IEEE 1532–compliant programmer can be used to program low-power flash devices. However, only limited security and FlashROM features are supported when using the IEEE 1532 standard. The Actel FlashPro3 programmer was developed exclusively for these devices and will support all the security and device serialization features. Refer to the standard for detailed information about IEEE 1532.

Security

Unlike SRAM-based FPGAs that require loading at power-up from an external source such as a microcontroller or boot PROM, Actel nonvolatile devices are live at power-up, and there is no bitstream required to load the device when power is applied. The unique flash-based architecture prevents reverse engineering of the programmed code on the device, because the programmed data is stored in nonvolatile memory cells. Each nonvolatile memory cell is made up of small capacitors and any physical deconstruction of the device will disrupt stored electrical charges.

Each low-power flash device has a built-in 128-bit Advanced Encryption Standard (AES) decryption core, except for the 15 k and 30 k gate devices. Any FPGA core or FlashROM content loaded into the device can optionally be sent as encrypted bitstream and decrypted as it is loaded. This is

particularly suitable for applications where device updates must be transmitted over an unsecured network such as the Internet. The embedded AES decryption core can prevent sensitive data from being intercepted (Figure 14-1 on page 14-4). A single 128-bit AES Key (32 hex characters) is used to encrypt FPGA core programming data and/or FlashROM programming data in the Actel tools. The low-power flash devices also decrypt with a single 128-bit AES Key. In addition, low-power flash devices support a Message Authentication Code (MAC) for authentication of the encrypted bitstream on-chip. This allows the encrypted bitstream to be authenticated and prevents erroneous data from being programmed into the device. The FPGA core, FlashROM, and Flash Memory Blocks (FBs), in Fusion only, can be updated independently using a programming file that is AES-encrypted (cipher text) or uses plain text.

Security in ARM-Enabled Low-Power Flash Devices

There are slight differences between the regular flash device and the ARM®-enabled flash devices, which have the M1 and M7 prefix.

The AES key is used by Actel and pre-programmed into the device to protect the ARM IP. As a result, the design will be encrypted along with the ARM IP, according to the details below.

CoreMP7 Device Security

ARM7™ (M7-enabled) devices are shipped with the following security features:

- FPGA Array enabled for AES encrypted programming and verification
- FlashROM enabled for plaintext read and write

Cortex-M1 Device Security

Cortex-M1–enabled devices are shipped with the following security features:

- FPGA Array enabled for AES-encrypted programming and verification
- FlashROM enabled for AES-encrypted write and verify

Fusion Embedded Flash Memory enabled for AES encrypted write.

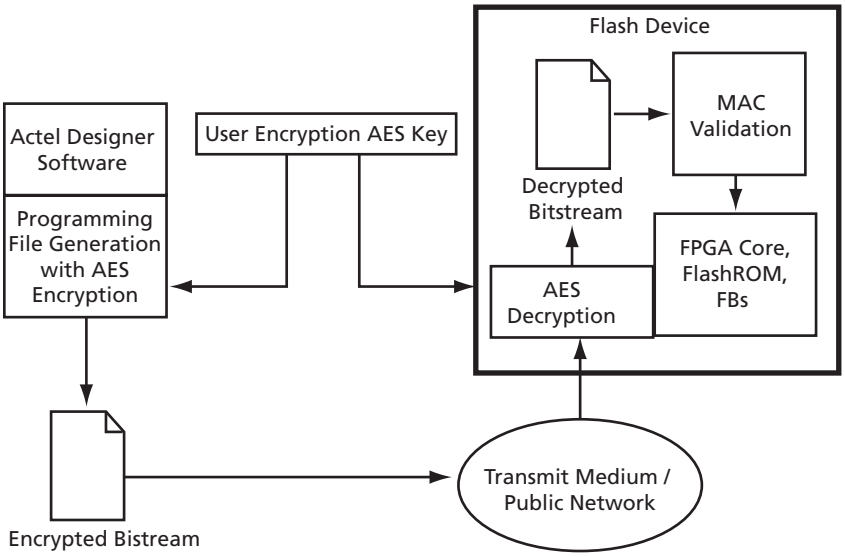

***Figure 14-1* • AES-128 Security Features**

Figure 14-2 on page 14-5 shows different applications for ISP programming.

1. In a trusted programming environment, you can program the device using the unencrypted (plaintext) programming file.
2. You can program the AES Key in a trusted programming environment and finish the final programming in an untrusted environment using the AES-encrypted (cipher text) programming file.
3. For the remote ISP updating/reprogramming, the AES Key stored in the device enables the encrypted programming bitstream to be transmitted through the untrusted network connection.

Actel low-power flash devices also provide the unique Actel FlashLock feature, which protects the Pass Key and AES Key. Unless the original FlashLock Pass Key is used to unlock the device, security settings cannot be modified. Low-power flash devices do not support read-back of FPGA core-programmed data; however, the FlashROM contents can selectively be read back (or disabled) via the JTAG port based on the security settings established by the Actel Designer software. Refer to *Security in Low-Power Flash Devices* for more information.

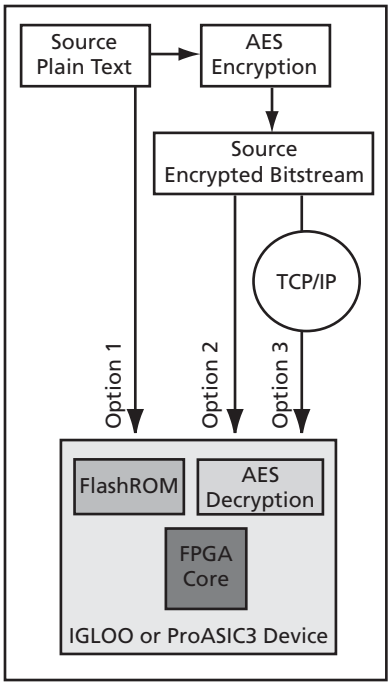

***Figure 14-2* • Different ISP Use Models**

FlashROM and Programming Files

Each low-power flash device has 1 kbit of on-chip, nonvolatile flash memory that can be accessed from the FPGA core. This nonvolatile FlashROM is arranged in eight pages of 128 bits (Figure 14-3). Each page can be programmed independently, with or without the 128-bit AES encryption. The FlashROM can only be programmed via the IEEE 1532 JTAG port and cannot be programmed from the FPGA core. In addition, during programming of the FlashROM, the FPGA core is powered down automatically by the on-chip programming control logic.

Using FlashROM combined with AES, many subscription-based applications or device serialization applications are possible. SmartGen supports easy management of the FlashROM contents even over large numbers of devices. SmartGen can support FlashROM contents that contain the following:

- Static values

		Byte Number in Page															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Page Number	7																
	6																
	5																
	4																
	3																
	2																
	1																
	0																

***Figure 14-3* • FlashROM Architecture**

- Random numbers
- Values read from a file
- Independent updates of each page

In addition, auto-incrementing of fields is possible. In applications where the FlashROM content is different for each device, you have the option to generate a single STAPL file for all the devices or individual serialization files for each device. For more information on how to generate the FlashROM content for device serialization, refer to *FlashROM in Actel's Low-Power Flash Devices*.

Actel Libero® Integrated Designed Environment (IDE) includes a unique tool to support the generation and management of FlashROM and FPGA programming files. This tool is called FlashPoint.

Depending on the applications, designers can use the FlashPoint software to generate a STAPL file with different contents. In each case, optional AES encryption and/or different security settings can be set.

In Designer, when you click the Programming File icon, FlashPoint launches, and you can generate STAPL file(s) with four different cases (Figure 14-4 on page 14-7). When the serialization feature is used during the configuration of FlashROM in SmartGen, you can generate a single STAPL file that will program all the devices or an individual STAPL file for each device.

The following cases present the FPGA core and FlashROM programming file combinations that can be used for different applications. In each case, you can set the optional security settings (FlashLock Pass Key and/or AES Key) depending on the application.

1. A single STAPL file or multiple STAPL files with multiple FlashROM contents and the FPGA core content. A single STAPL file will be generated if the device serialization feature is not used. You can program the whole FlashROM or selectively program individual pages.
2. A single STAPL file for the FPGA core content
3. A single STAPL file or multiple STAPL files with multiple FlashROM contents. A single STAPL file will be generated if the device serialization feature is not used. You can program the whole FlashROM or selectively program individual pages.
4. A single STAPL file to configure the security settings for the device, such as the AES Key and/or Pass Key.

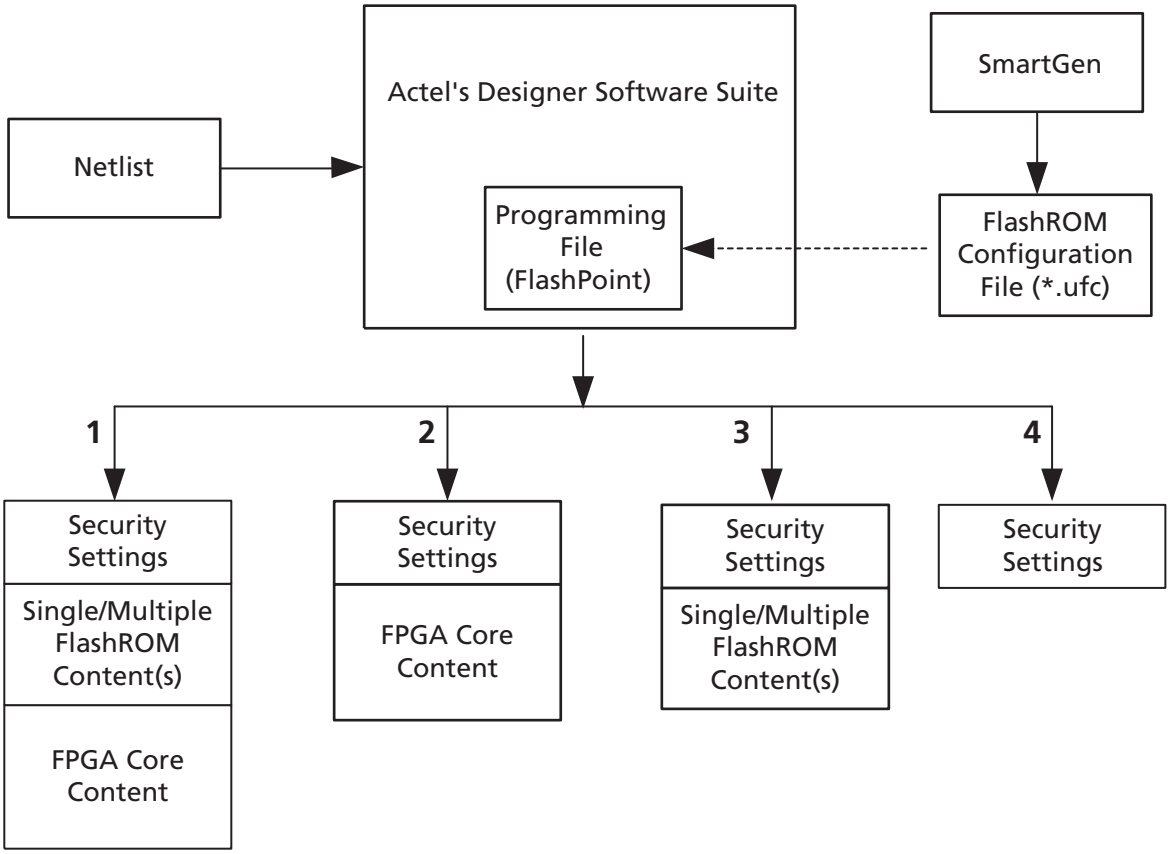

Figure 14-4 **• Flexible Programming File Generation for Different Applications**

Programming Solution

For device programming, any IEEE 1532–compliant programmer can be used; however, the FlashPro3 programmer must be used to control the low-power flash device's rich security features and FlashROM programming options. The FlashPro3 programmer is a low-cost portable programmer for the Actel flash families. It can also be used with a powered USB hub for parallel programming. General specifications for the FlashPro3 programmer are as follows:

- Programming clock – TCK is used with a maximum frequency of 20 MHz, and the default frequency is 4 MHz.
- Programming file – STAPL
- Daisy chain – Supported. You can use the ChainBuilder software to build the programming file for the chain.
- Parallel programming – Supported. Multiple FlashPro3 programmers can be connected together using a powered USB hub or through the multiple USB ports on the PC.
- Power supply – The target board must provide V_{CC}, V_{CCI}, V_{PUMP}, and V_{JTAG} during programming. However, if there is only one device on the target board, the FlashPro3 programmer can generate the required V_{PUMP} voltage from the USB port.

ISP Programming Header Information

The FlashPro3 programming cable connector can be connected with a 10-pin, 0.1"-pitch programming header. The recommended programming headers are manufactured by AMP (103310-1) and 3M (2510-6002UB). If you have limited board space, you can use a compact programming header manufactured by Samtec (FTSH-105-01-L-D-K). Using this compact programming header, you are required to order an additional header adapter manufactured by Actel (FP3-26PIN-ADAPTER).

Existing ProASIC^PLUS family customers who are using the Samtec Small Programming Header (FTSH-113-01-L-D-K) and are planning to migrate to IGLOO or ProASIC3 devices can order a separate adapter kit from Actel (FP3-10PIN-ADAPTER-KIT), which contains a compact 10-pin adapter kit as well as 26-pin migration capability.

Table 14-3 • **Programming Header Ordering Code**

Manufacturer	Part Number	Description
AMP	103310-1	10-pin, 0.1"-pitch cable header (right-angle PCB mount angle)
3M	2510-6002UB	10-pin, 0.1"-pitch cable header (straight PCB mount angle)
Samtec	FTSH-113-01-L-D-K	Small programming header supported by FlashPro and Silicon Sculptor
Samtec	FTSH-105-01-L-D-K	Compact programming header
Samtec	FFSD-05-D-06.00-01-N	10-pin cable with 50 mil pitch sockets; included in FP3-10PIN-ADAPTER-KIT.
Actel	FP3-10PIN-ADAPTER-KIT	Compact header and migration kit

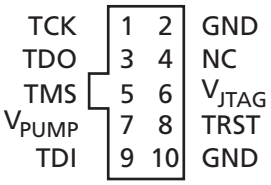

Figure 14-5 • **Programming Header (top view)**

Table 14-4 • **Programming Header Pin Numbers and Description**

Pin	Signal	Source	Description
1	TCK	Programmer	JTAG Clock
2	GND[1]	–	Signal Reference
3	TDO	Target Board	Test Data Output
4	NC	–	No Connect
5	TMS	Programmer	Test Mode Select
6	V_{JTAG}	Target Board	JTAG Supply Voltage
7	V_{PUMP}[2]	Programmer/Target Board	Programming Supply Voltage
8	nTRST	Programmer	JTAG Test Reset (Hi-Z with 10 kΩ pull-down, HIGH, LOW, or toggling)
9	TDI	Programmer	Test Data Input
10	GND[1]	–	Signal Reference

Notes:

1. *Both GND pins must be connected.*
2. *FlashPro3 can provide V_{PUMP} if there is only one device on the target board.*

Board-Level Considerations

A bypass capacitor is required from V_{PUMP} to GND for all low-power flash devices during programming. This bypass capacitor protects the devices from voltage spikes that may occur on the V_{PUMP} supplies during the erase and programming cycles. Refer to *Pin Descriptions* for specific recommendations. For proper programming, 0.01 µF and 0.33 µF capacitors (both rated at 16 V) are to be connected in parallel across V_{PUMP} and GND, and positioned as close to the FPGA pins as possible. The bypass capacitor must be placed within 2.5 cm of the device pins.

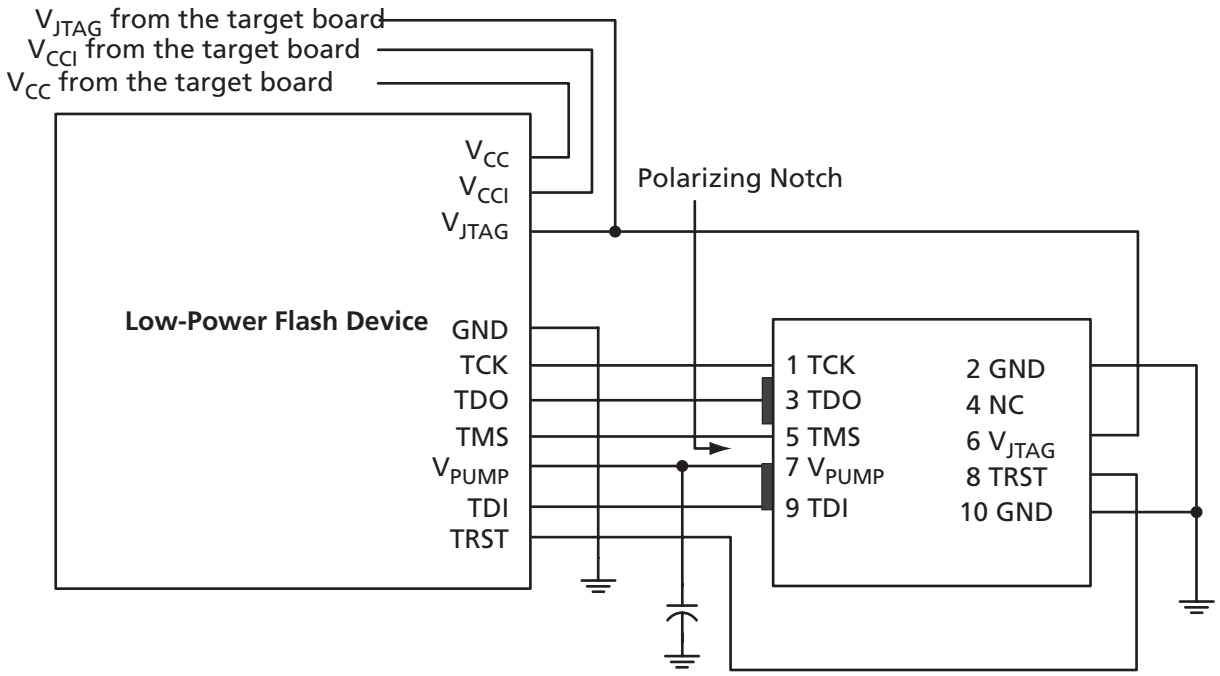

***Figure 14-6* • Board Layout and Programming Header Top View**

Troubleshooting Signal Integrity

Symptoms of a Signal Integrity Problem

A signal integrity problem can manifest itself in many ways. The problem may show up as extra or dropped bits during serial communication, changing the meaning of the communication. There is a normal variation of threshold voltage and frequency response between parts even from the same lot. Because of this, the effects of signal integrity may not always affect different devices on the same board in the same way. Sometimes, replacing a device appears to make signal integrity problems go away, but this is just masking the problem. Different parts on identical boards will exhibit the same problem sooner or later. It is important to fix signal integrity problems early. Unless the signal integrity problems are severe enough to completely block all communication between the device and the programmer, they may show up as subtle problems. Some of the FlashPro3 exit codes that are caused by signal integrity problems are listed below. Signal integrity problems are not the only possible cause of these errors, but this list is intended to show where problems can occur. FlashPro3 allows TCK to be lowered from 24 MHz down to 1 MHz to allow you to address some signal integrity problems that may occur with impedance mismatching at higher frequencies.

Chain Integrity Test Error or Analyze Chain Failure

Normally, the FlashPro3 Analyze Chain command expects to see 0x2 on the TDO pin. If the command reports reading 0x0 or 0x3, it is seeing the TDO pin stuck at 0 or 1. The only time the TDO pin comes out of tristate is when the JTAG TAP state machine is in the Shift-IR or Shift-DR state. If

noise or reflections on the TCK or TMS lines have disrupted the correct state transitions, the device's TAP state controller might not be in one of these two states when the programmer tries to read the device. When this happens, the output is floating when it is read and does not match the expected data value. This can also be caused by a broken TDO net. Only a small amount of data is read from the device during the Analyze Chain command, so marginal problems may not always show up during this command.

Exit 11

This error occurs during the verify stage of programming a device. After programming the design into the ProASIC3/E device, the device is verified to ensure it is programmed correctly. The verification is done by shifting the programming data into the device. An internal comparison is performed within the device to verify that all switches are programmed correctly. Noise induced by poor signal integrity can disrupt the writes and reads or the verification process and produce a verification error. While technically a verification error, the root cause is often related to signal integrity.

Refer to the *FlashPro User's Guide* for other error messages and solutions. For the most up-to-date known issues and solutions, refer to http://www.actel.com/support.

Conclusion

IGLOO, Fusion, and ProASIC3 devices offer a low-cost, single-chip solution that is live at power-up through nonvolatile flash technology. The FlashLock Pass Key and 128-bit AES Key security features enable secure ISP in an untrusted environment. On-chip FlashROM enables a host of new applications, including device serialization, subscription-based applications, and IP addressing. Additionally, as the FlashROM is nonvolatile, all of these services can be provided without battery backup.

Related Documents

Handbook Documents

Microprocessor Programming of Actel's Low-Power Flash Devices

http://www.actel.com/documents/LPD_Microprocessor_HBs.pdf

Security in Low-Power Flash Devices

http://www.actel.com/LPD_Security_HBs.pdf

FlashROM in Actel's Low-Power Flash Devices

http://www.actel.com/documents/LPD_FlashROM_HBs.pdf

Pin Descriptions

http://www.actel.com/documents/LPD_PinDescriptions_HBs.pdf

User's Guides

FlashPro User's Guide

http://www.actel.com/documents/flashpro_ug.pdf

Part Number and Revision Date

This document was previously published as an application note describing features and functions of the device, and as such has now been incorporated into the device handbook format. No technical changes have been made to the content.

Part Number 51700094-015-2

Revised June 2008

List of Changes

The following table lists critical changes that were made in the current version of the chapter.

Previous Version	Changes in Current Version (v1.2)	Page
v1.1 (March 2008)	The following changes were made to the family descriptions in Table 14-1 · Low-Power Flash Families: • ProASIC3L was updated to include 1.5 V. • The number of PLLs for ProASIC3E was changed from five to six.	14-2
v1.0 (January 2008)	The "ISP Architecture" section was updated to included the IGLOO PLUS family in the discussion of family-specific support. The text, "When 1.2 V is used, the device can be reprogrammed in-system at 1.5 V only" was revised to state, "Although the device can operate at 1.2 V core voltage, the device can only be reprogrammed when all supplies (V_{CC}, V_{CCI}, and V_{JTAG}) are at 1.5 V."	14-1
	The "ISP Support in Low-Power Devices" section and Table 14-1 · Low-Power Flash Families were updated to include the IGLOO PLUS family. The "IGLOO Terminology" section and "ProASIC3 Terminology" section are new.	14-2
	The "Security" section was updated to mention that 15 k gate devices do not have a built-in 128-bit decryption core.	14-3
	Table 14-2 · Power Supplies was revised to remove the Normal Operation column and add a table note stating, "All supply voltages should be at 1.5 V or higher, regardless of the setting during normal operation."	14-3
	The "ISP Programming Header Information" section was revised to change FP3-26PIN-ADAPTER to FP3-10PIN-ADAPTER-KIT. Table 14-3 · Programming Header Ordering Code was updated with the same change, as well as adding the part number FFSD-05-D-06.00-01-N, a 10-pin cable with 50-mil-pitch sockets.	14-8
	The "Board-Level Considerations" section was updated to describe connecting two capacitors in parallel across V_{PUMP} and GND for proper programming.	14-9
51900055-2/7.06	Information was added to the "Programming Voltage (VPUMP) and VJTAG" section about the JTAG interface pin.	14-3
51900055-1/1.05	ACTgen was changed to SmartGen.	N/A
	In Figure 14-6 · Board Layout and Programming Header Top View, the order of the text was changed to: V_{JTAG} from the target board V_{CCI} from the target board V_{CC} from the target board	14-9

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15 – Core Voltage Switching Circuit for IGLOO and ProASIC3L In-System Programming

Introduction

The IGLOO® and ProASIC®3L families offer devices that can be powered by either 1.5 V or 1.2 V core voltage.

Since IGLOO and ProASIC3L devices are flash-based, they can be programmed and reprogrammed multiple times in-system using Actel FlashPro3. Actel FlashPro3 uses the JTAG standard interface (IEEE 1532) and STAPL file (IEEE 1149) to program a device. Programming can also be executed by other methods, such as an embedded microcontroller that follows the same standards above.

All IGLOO and ProASIC3L devices must be programmed with the V_{CC} core voltage at 1.5 V. Therefore, applications using IGLOO or ProASIC3L devices powered by a 1.2 V supply must switch the core supply to 1.5 V for in-system programming.

The purpose of this document is to describe an easy-to-use and cost-effective solution for switching the core supply voltage from 1.2 V to 1.5 V during in-system programming for IGLOO and ProASIC3L devices.

Actel's Flash Families Support Voltage Switching Circuit

The low-power flash families listed in Table 15-1 support the voltage switching circuit feature and the functions described in this document.

Table 15-1 • **Low-Power Flash Families**

Family[1]	Description	Timing Numbers[2]
IGLOO	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*IGLOO DC and Switching Characteristics*
IGLOO PLUS	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology and enhanced I/O capabilities	*IGLOO PLUS DC and Switching Characteristics*
IGLOOe	IGLOO devices enhanced with higher density, five additional PLLs, and additional I/O standards	*IGLOOe DC and Switching Characteristics*
ProASIC3L	Low-power high-performance 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*ProASIC3L DC and Switching Characteristics*

Notes:

1. *The family names are linked to the appropriate product brief.*
2. *The timing number links go to the relevant timing numbers in the datasheet.*

Actel's low-power flash devices (listed in Table 15-1) provide a selection of low-power, secure, live-at-power-up, single-chip solutions. The nonvolatile flash-based devices do not require a boot PROM and incorporate FlashLock® technology, which provides a unique combination of reprogrammability and design security without external overhead. Only low-power flash FPGAs can offer these advantages.

Actel IGLOO FPGAs are the industry-leading 1.2 V ultra-low-power programmable logic devices (PLDs) and consume 90% less static power and over 50% less dynamic power than PLD alternatives, while ProASIC3L devices offer a balance of low power and higher performance.

Flash*Freeze technology used in IGLOO, IGLOO PLUS, and ProASIC3L devices enables easy entry to and exit from the ultra-low power mode, which consumes as little as 5 µW, while retaining SRAM and register data. IGLOO PLUS also offers the ability to hold I/O state in Flash*Freeze mode. Flash*Freeze technology simplifies power management through I/O and clock management without the need to turn off voltages, I/Os, or clocks at the system level. Entering and exiting Flash*Freeze mode takes less than 1 µs.

IGLOO Terminology

In documentation, the term IGLOO families or IGLOO devices refers to all IGLOO families as listed in Table 15-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

Circuit Description

Applications that use IGLOO or ProASIC3L devices powered by a 1.2 V core supply must have a mechanism that switches the core voltage from 1.2 V to 1.5 V during in-system programming (ISP). There are several possible techniques to meet this requirement. Actel recommends utilizing a linear voltage regulator, a resistor voltage divider, and an N-Channel Digital FET to set the appropriate V_{CC} voltage, as shown in Figure 15-1.

The main component of Actel's recommended circuit is the LTC3025 linear voltage regulator from LinearTech. The output voltage of the LTC3025 on the OUT pin is set by the ratio of two external resistors, R37 and R38, in a voltage divider. The linear voltage regulator adjusts the voltage on the OUT pin to maintain the ADJ pin voltage at 0.4 V (referenced to ground). By using an R38 value of 40.2 kΩ and an R37 value of 80.6 kΩ, the output voltage on the OUT pin is 1.2 V. To achieve 1.5 V on the OUT pin, R44 can be used in parallel with R38. The OUT pin can now be used as a switchable source for the V_{CC} supply. Refer to the *LTC3025 Linear Voltage Regulator datasheet* for more information.

In Figure 15-1, the N-Channel Digital FET is used to enable and disable R44. This FET is controlled by the JTAG TRST signal driven by the FlashPro3 programmer. During programming of the device, the TRST signal is driven HIGH by the FlashPro3, and turns the N-Channel Digital FET ON. When the FET is ON, R44 becomes enabled as a parallel resistance to R38, which forces the regulator to set OUT to 1.5 V.

When the FlashPro3 is connected and not in programming mode or when it is not connected, the pull-down resistor, R10, will pull the TRST signal LOW. When this signal is LOW, the N-Channel Digital FET is "open" and R44 is not part of the resistance seen by the LTC3025. The new resistance momentarily changes the voltage value on the ADJ pin, which in turn causes the output of the LTC3025 to compensate by setting OUT to 1.2 V. Now the device will run in regular active mode at the regular 1.2 V core voltage.

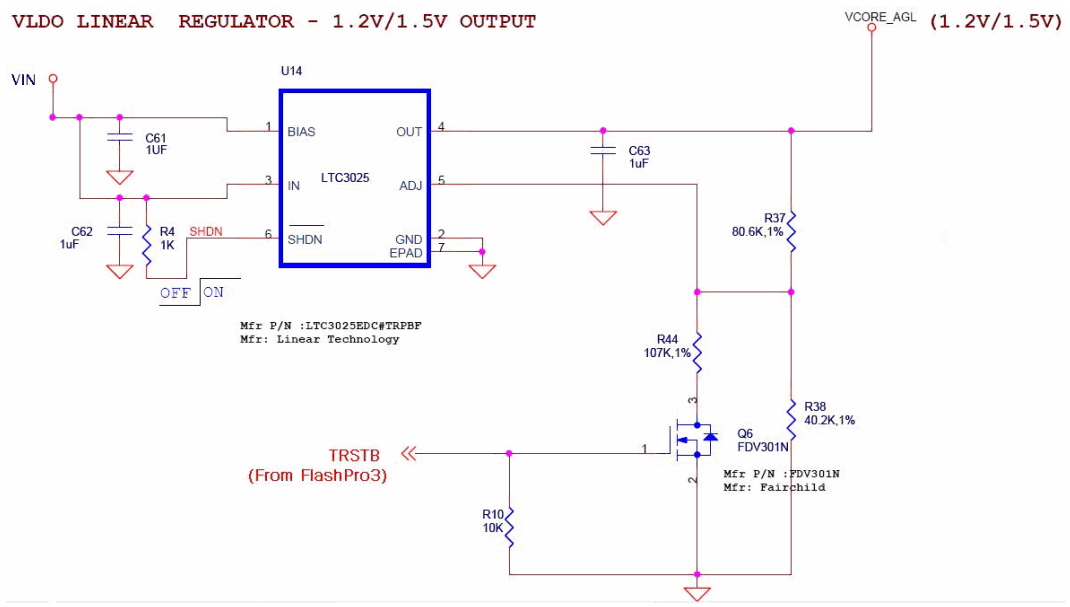

Figure 15-1 • **Circuit Diagram**

Circuit Verification

The power switching circuit recommended above is implemented on Actel's Icicle board (Figure 15-2). On the Icicle board, VJTAGENB is used to control the N-Channel Digital FET; however, this circuit was modified to use TRST instead of VJTAGENB in this application. There are three important aspects of this circuit that were verified:

1. The rise on V_{CC} from 1.2 V to 1.5 V when TRST is HIGH
2. V_{CC} rises to 1.5 V before programming begins.
3. V_{CC} switches from 1.5 V to 1.2 V when TRST is LOW.

Verification Steps

1. The rise on V_{CC} from 1.2 V to 1.5 V when TRST is HIGH.

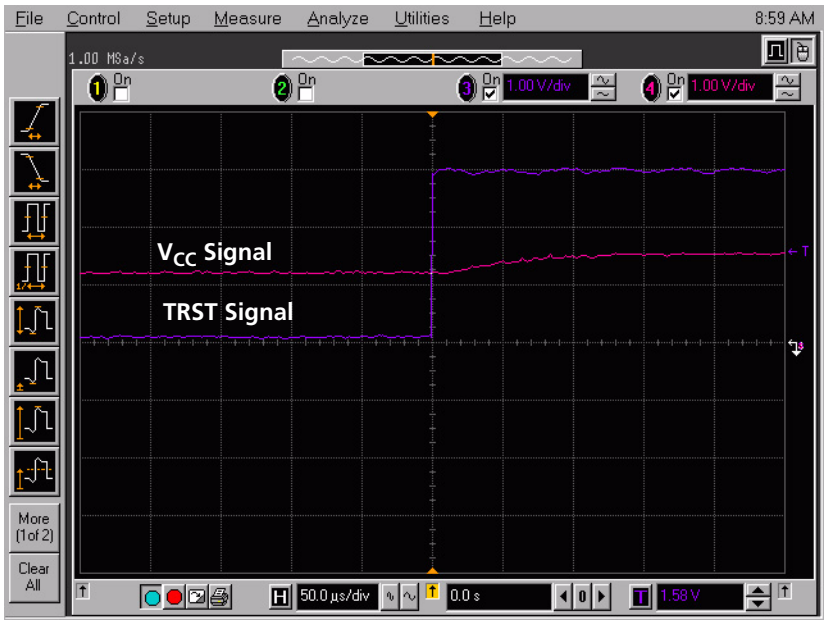

***Figure 15-2* • Core Voltage on the IGLOO AGL125-QNG132 Device**

In the oscilloscope plots (Figure 15-2), the TRST from FlashPro3 and the V_{CC} core voltage of the IGLOO device are labeled. This plot shows the rise characteristic of the TRST signal from FlashPro3. Once the TRST signal is asserted HIGH, the LTC3025 shown in Figure 15-1 on page 15-3 senses the increase in voltage and changes the output from 1.2 V to 1.5 V. It takes the circuit approximately 100 µs to respond to TRST and change the voltage to 1.5 V on the V_{CC} core.

2. V_{CC} rises to 1.5 V before programming begins.

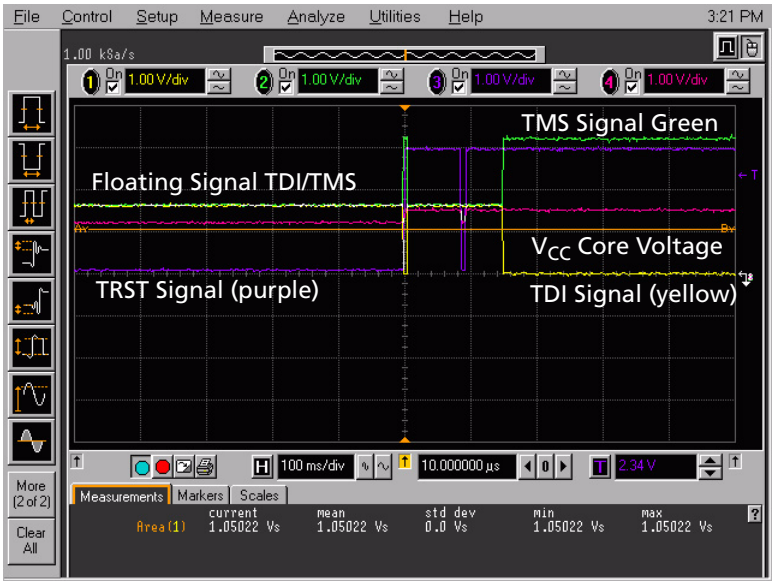

***Figure 15-3* • Programming Algorithm**

The oscilloscope plot in Figure 15-3 shows a wider time interval for the programming algorithm and includes the TDI and TMS signals from the FlashPro3. These signals carry the programming information that is programmed into the device and should only start toggling after the V_{CC} core voltage reaches 1.5 V. Again, the TRST from FlashPro3 and the V_{CC} voltage core of the IGLOO device are labeled. As shown in Figure 15-3, TDI and TMS are floating initially, and the core voltage is 1.2 V. When a programming command on the FlashPro3 is executed, the TRST is driven HIGH and the TDI is momentarily driven to ground. In response to the HIGH TRST signal, the circuit responds and pulls the core voltage to 1.5 V. After 100 ms, TRST is briefly driven LOW by the FlashPro software. This is expected behavior that ensures the device JTAG state machine is in Reset prior to programming. The TRST remains HIGH for the duration of the programming. It can be seen in Figure 15-3 that the V_{CC} core voltage signal remains at 1.5 V for approximately 50 ms before information starts passing through on TDI and TMS. This confirms that the voltage switching circuit drives the V_{CC} core supply voltage to 1.5 V prior to programming.

3. V_{CC} switches from 1.5 V to 1.2 V when TRST is LOW.

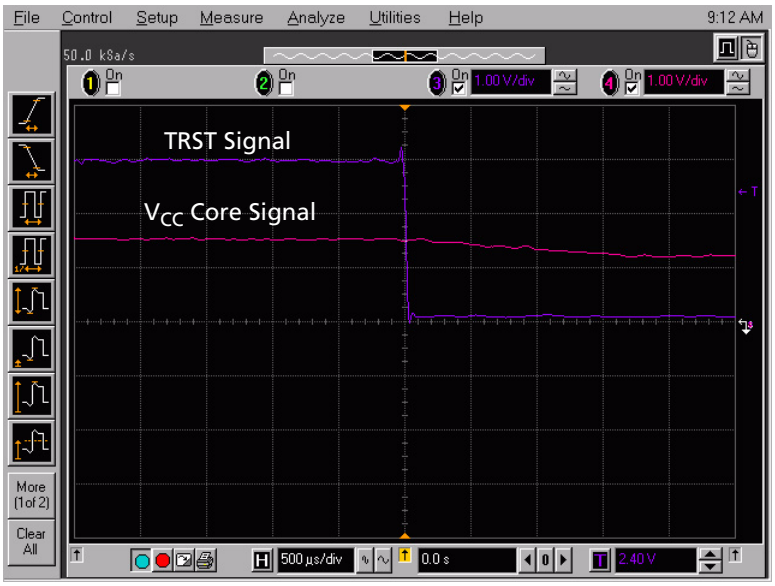

***Figure 15-4* • TRST Toggled LOW**

In Figure 15-4, the TRST signal and the V_{CC} core voltage signal are labeled. As the TRST is pulled to ground, the core voltage is observed to switch from 1.5 V to 1.2 V. The observed fall time is approximately 2 ms.

DirectC

The above analysis is based on FlashPro3 but there are other solutions to ISP, such as DirectC. DirectC is a microprocessor program that can be run in-system to program Actel flash devices. For FlashPro3, TRST is the most convenient control signal to use for the recommended circuit. However, for DirectC, users may use any signal to control the FET. For example, the DirectC code can be edited so that a separate non-JTAG signal can be asserted from the microcontroller that signals the board that it is about to start programming the device. After asserting the N-Channel Digital FET control signal, the programming algorithm must allow sufficient time for the supply to rise to 1.5 V before initiating DirectC programming. As seen in Figure 15-3 on page 15-5, 50 ms is adequate time. Depending on the size of the PCB and the capacitance on the V_{CC} supply, results may vary from system to system. Actel recommends using a conservative value for the wait time to make sure that the V_{CC} core voltage is at the right level.

Conclusion

Actel's IGLOO and ProASIC3L low-power FPGAs offer 1.2 V core operation; however, they must be programmed with a core voltage of 1.5 V. Since the device can have either a 1.2 V or a 1.5 V normal operation, there must be a way for the core voltage to switch from 1.2 V to 1.5 V, which is required during in-system programming. The circuit explained in this document illustrates one simple, cost-effective way of handling this requirement. A JTAG signal from the FlashPro3 programmer allows the circuit to sense when programming is in progress, enabling it to switch to the correct core voltage.

Part Number and Revision Date

This document was previously published as an application note describing features and functions of the device, and as such has now been incorporated into the device handbook format. No technical changes have been made to the content.

Part Number 51700094-028-0

Revised August 2008

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16 – Microprocessor Programming of Actel's Low-Power Flash Devices

Introduction

The IGLOO,® Fusion, and ProASIC®3 families of flash FPGAs support in-system programming (ISP) with the use of a microprocessor. Flash-based FPGAs store their configuration information in the actual cells within the FPGA fabric. SRAM-based devices need an external configuration memory, and hybrid nonvolatile devices store the configuration in a flash memory inside the same package as the SRAM FPGA. Since the programming of a true flash FPGA is simpler, requiring only one stage, it makes sense that programming with a microprocessor in-system should be simpler than with other SRAM FPGAs. This reduces bill-of-materials costs and printed circuit board (PCB) area, and increases system reliability.

Nonvolatile flash technology also gives the low-power flash devices the advantage of a secure, low-power, live-at-power-up, and single-chip solution. Low-power flash devices are reprogrammable and offer time-to-market benefits at an ASIC-level unit cost. These features enable engineers to create high-density systems using existing ASIC or FPGA design flows and tools.

This document is an introduction to microprocessor programming only. To explain the difference between the options available, user's guides for DirectC and STAPL provide more detail on implementing each style.

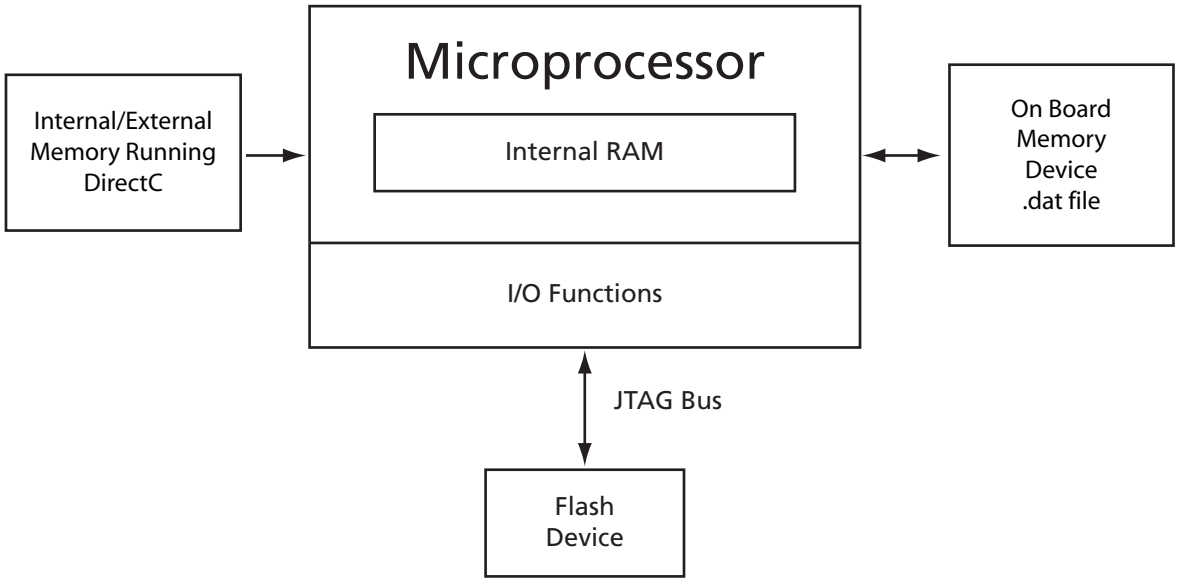

Figure 16-1 • **ISP Using Microprocessor**

Microprocessor Programming Support in Low-Power Devices

The low-power flash families listed in Table 16-1 support programming with a microprocessor and the functions described in this document.

Table 16-1 • **Low-Power Flash Families**

Family[1]	Description	Timing Numbers[2]
IGLOO	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*IGLOO DC and Switching Characteristics*
IGLOOe	IGLOO devices enhanced with higher density, five additional PLLs, and additional I/O standards	*IGLOOe DC and Switching Characteristics*
ProASIC3L	Low-power, high-performance 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*ProASIC3L DC and Switching Characteristics*
ProASIC3	Low-power, high-performance 1.5 V FPGAs	*ProASIC3 DC and Switching Characteristics*
ProASIC3E	ProASIC3 enhanced with higher density, six additional PLLs, and additional I/O standards	*ProASIC3E DC and Switching Characteristics*
ProASIC3 Automotive	Low-power, high-performance FPGAs qualified for Automotive applications	*Automotive ProASIC3 DC and Switching Characteristics*
Fusion	Low-power mixed-signal Programmable System Chip (PSC)	*Fusion DC and Power Characteristics*

Notes:

1. *The family names are linked to the appropriate product brief.*
2. *The timing number links go to the relevant timing numbers in the datasheet.*

Actel's low-power flash devices (listed in Table 16-1) provide a selection of low-power, secure, live-at-power-up, single-chip solutions. The nonvolatile flash-based devices do not require a boot PROM and incorporate FlashLock® technology, which provides a unique combination of reprogrammability and design security without external overhead. Only low-power flash FPGAs can offer these advantages.

Actel IGLOO PLUS FPGAs are the industry-leading 1.2 V ultra-low-power programmable logic devices (PLDs) and consume 90% less static power and over 50% less dynamic power than PLD alternatives, while ProASIC3L devices offer a balance of low power and higher performance.

Flash*Freeze technology used in IGLOO, IGLOO PLUS, and ProASIC3L devices enables easy entry to and exit from the ultra-low power mode, which consumes as little as 5 µW, while retaining SRAM and register data. IGLOO PLUS also offers the ability to hold I/O state in Flash*Freeze mode. Flash*Freeze technology simplifies power management through I/O and clock management without the need to turn off voltages, I/Os, or clocks at the system level. Entering and exiting Flash*Freeze mode takes less than 1 µs.

The Actel Fusion® family, based on the highly successful ProASIC3 flash FPGA architecture, has been designed as a high-performance, mixed-signal Programmable System Chip. Fusion supports many peripherals, including embedded flash memory, analog-to-digital converter (ADC), high-drive outputs, RC and crystal oscillators, and real-time counter (RTC). The total available on-chip memory, including the flash array blocks, is greater than that found in SRAM FPGAs.

IGLOO Terminology

In documentation, the term IGLOO families or IGLOO devices refers to all IGLOO families as listed in Table 16-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

ProASIC3 Terminology

In documentation, the term ProASIC3 families or ProASIC3 devices refers to all ProASIC3 families as listed in Table 16-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

Programming Algorithm

JTAG Interface

The low-power flash families are fully compliant with the IEEE 1149.1 (JTAG) standard. They support all the mandatory boundary scan instructions (EXTEST, SAMPLE/PRELOAD, and BYPASS) as well as six optional public instructions (USERCODE, IDCODE, HIGHZ, and CLAMP).

IEEE 1532

The low-power flash families are also fully compliant with the IEEE 1532 programming standard. The IEEE 1532 standard adds programming instructions and associated data registers to devices that comply with the IEEE 1149.1 standard (JTAG). These instructions and registers extend the capabilities of the IEEE 1149.1 standard such that the Test Access Port (TAP) can be used for configuration activities. The IEEE 1532 standard greatly simplifies the programming algorithm, reducing the amount of time needed to implement microprocessor ISP.

Implementation Overview

To implement device programming with a microprocessor, the user should first download the C-based STAPL player or DirectC code from the Actel website. (See the Actel website for future updates regarding the STAPL player and DirectC code). Using the easy-to-follow Actel user's guide, create the low-level application programming interface (API) to provide the necessary basic functions. These API functions act as the interface between the programming software and the actual hardware (Figure 16-2).

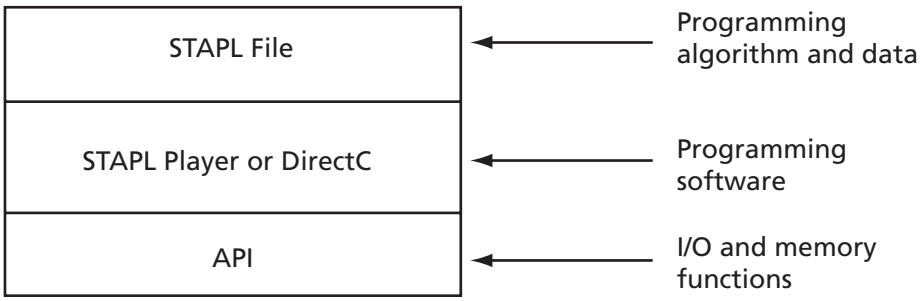

***Figure 16-2* • Device Programming Code Relationship**

The API is then linked with the STAPL player or DirectC and compiled using the microprocessor's compiler. Once the entire code is compiled, the user must download the resulting binary into the MCU system's program memory (such as ROM, EEPROM, or flash). The system is now ready for programming.

To program a design into the FPGA, the user creates a bitstream or STAPL file using the Actel Designer software, downloads it into the MCU system's volatile memory, and activates the stored programming binary file (Figure 16-3 on page 16-4). Once the programming is completed, the bitstream or STAPL file can be removed from the system, as the configuration profile is stored in the flash FPGA fabric and does not need to be reloaded at every system power-on.

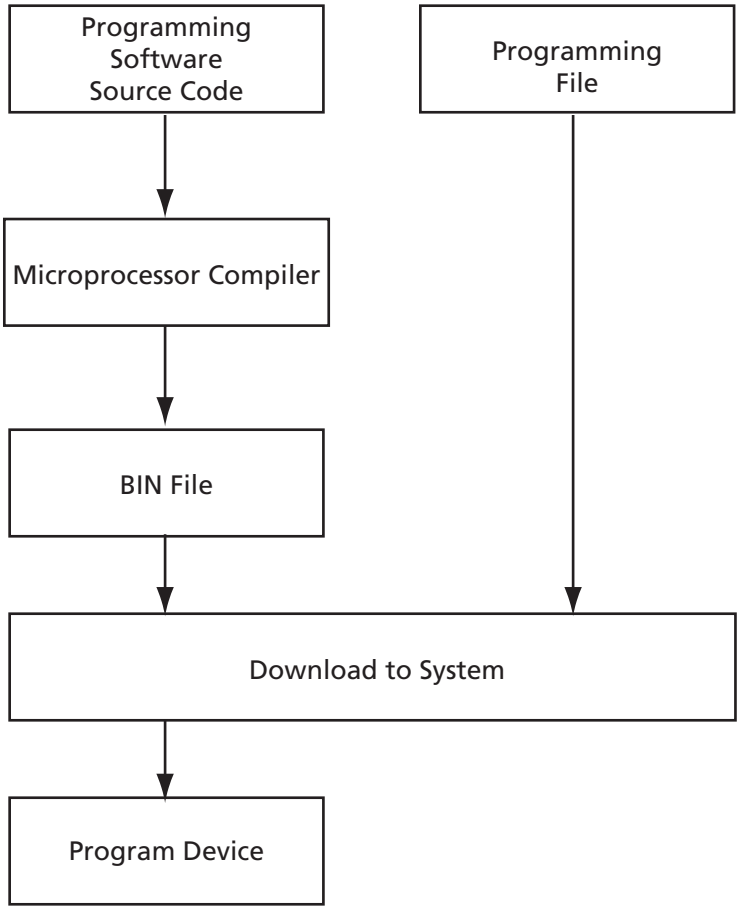

Figure 16-3 **• MCU FPGA Programming Model**

FlashROM

Actel low-power flash devices have 1 kbit of user-accessible, nonvolatile, FlashROM on-chip. This nonvolatile FlashROM can be programmed along with the core or on its own using the standard IEEE 1532 JTAG programming interface.

The FlashROM is architected as eight pages of 128 bits. Each page can be individually programmed (erased and written). Additionally, on-chip AES security decryption can be used selectively to load data securely into the FlashROM (e.g., over public or private networks, such as the Internet). Refer to *FlashROM in Actel's Low-Power Flash Devices*.

STAPL vs. DirectC

Programming the low-power flash devices is performed using DirectC or the STAPL player. Both tools use the STAPL file as an input. DirectC is a compiled language, whereas STAPL is an interpreted language. Microprocessors will be able to load the FPGA using DirectC much more quickly than STAPL. This speed advantage becomes more apparent when lower clock speeds of 8- or 16-bit microprocessors are used. DirectC also requires less memory than STAPL, since the programming algorithm is directly implemented. STAPL does have one advantage over DirectC—the ability to upgrade. When a new programming algorithm is required, the STAPL user simply needs to regenerate a STAPL file using the latest version of the Designer software and download it to the system. The DirectC user must download the latest version of DirectC from Actel, compile everything, and download the result into the system (Figure 16-4 on page 16-5).

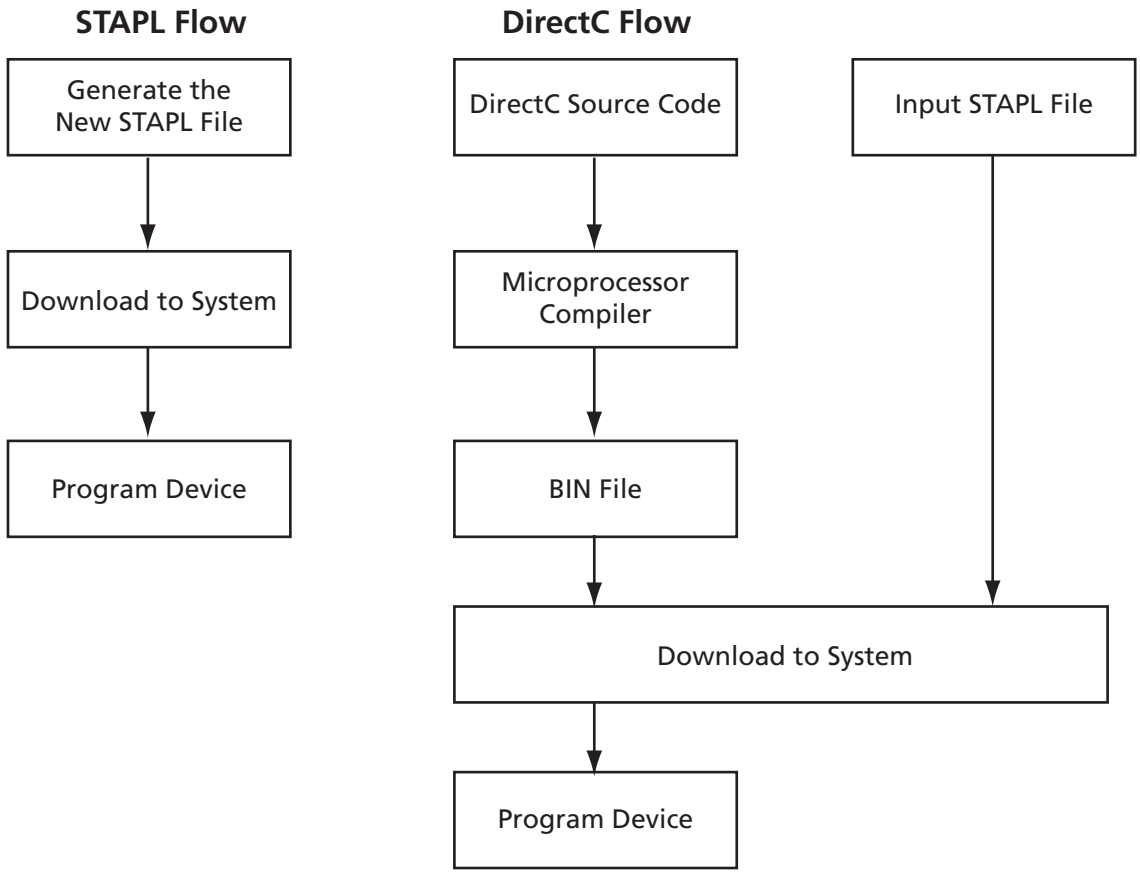

***Figure 16-4* • STAPL vs. DirectC**

Remote Upgrade via TCP/IP

Transmission Control Protocol (TCP) provides a reliable bitstream transfer service between two endpoints on a network. TCP depends on Internet Protocol (IP) to move packets around the network on its behalf. TCP protects against data loss, data corruption, packet reordering, and data duplication by adding checksums and sequence numbers to transmitted data and, on the receiving side, sending back packets and acknowledging the receipt of data.

The system containing the low-power flash device can be assigned an IP address when deployed in the field. When the device requires an update (core or FlashROM), the programming instructions along with the new programming data (AES-encrypted cipher text) can be sent over the Internet to the target system via the TCP/IP protocol. Once the MCU receives the instruction and data, it can proceed with the FPGA update. Low-power flash devices support Message Authentication Code (MAC), which can be used to validate data for the target device. More details are given in the "Message Authentication Code (MAC) Validation/Authentication" section on page 16-6.

Hardware Requirement

To facilitate the programming of the low-power flash families, the system must have a microprocessor (with access to the device JTAG pins) to process the programming algorithm, memory to store the programming algorithm, programming data, and the necessary programming voltage. Refer to the relevant datasheet for programming voltages.

Security

Read-Back Prevention

The low-power flash devices are designed with security in mind. Even without any security measures (such as FlashLock with AES), it is not possible to read back the programming data from a programmed device. Upon programming completion, the programming algorithm will reload the programming data into the device. The device will then use built-in circuitry to determine if it was programmed correctly.

As an additional security measure, the devices are equipped with AES decryption. AES works in two steps. The first step is to program a key into the devices in a secure or trusted programming center (such as Actel In-House Programming (IHP) center). The second step is to encrypt any programming files with the same encryption key. The encrypted programming file will only work with the devices that have the same key. The AES used in the low-power flash families is the 128-bit AES decryption engine (Rijndael algorithm).

Message Authentication Code (MAC) Validation/Authentication

As part of the AES decryption flow, the devices are equipped with a MAC validation/authentication system. MAC is an authentication tag, also called a checksum, derived by applying an on-chip authentication scheme to a STAPL file as it is loaded into the FPGA. MACs are computed and verified with the same key so they can only be verified by the intended recipient. When the MCU system receives the AES-encrypted programming data (cipher text), it can validate the data by loading it into the FPGA and performing a MAC verification prior to loading the data, via a second programming pass, into the FPGA core cells. This prevents erroneous or corrupt data from getting into the FPGA.

Low-power flash devices with AES and MAC are superior to devices with only DES or 3DES encryption. Because the MAC verifies the correctness of the data, the FPGA is protected from erroneous loading of invalid programming data that could damage a device (Figure 16-5 on page 16-7).

The AES with MAC enables field updates over public networks without fear of having the design stolen. An encrypted programming file can only work on devices with the correct key, rendering

any stolen files useless to the thief. To learn more about the low-power flash devices' security features, refer to *Security in Low-Power Flash Devices*.

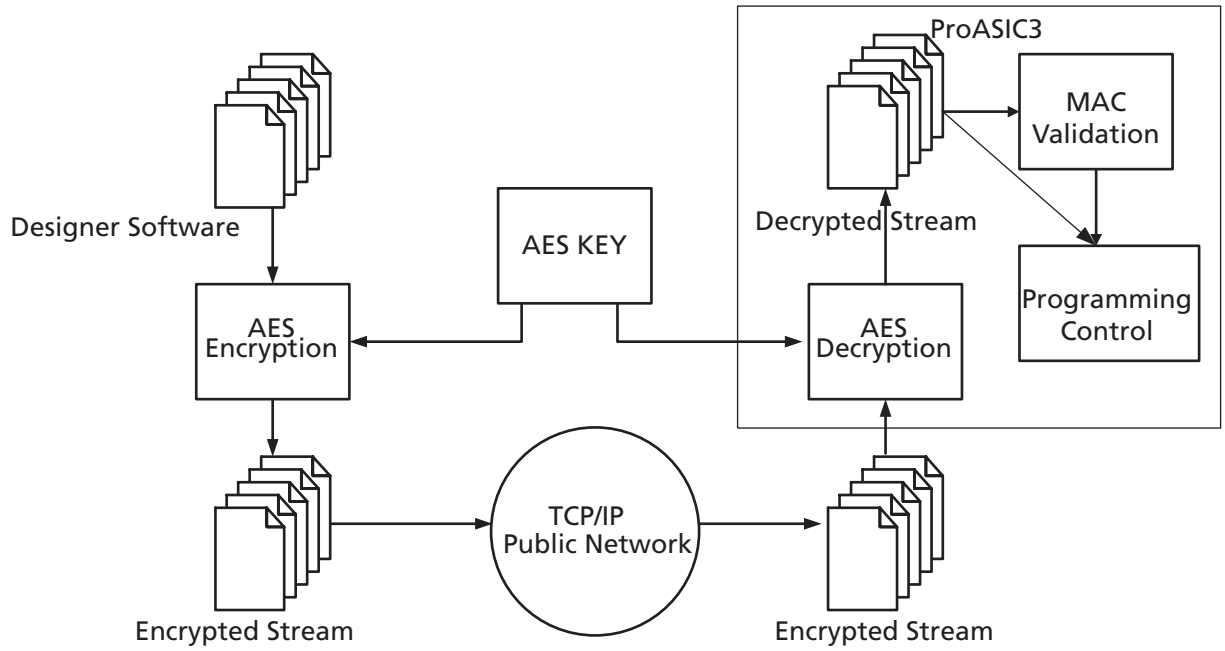

***Figure 16-5* • ProASIC3 Device Encryption Flow**

Conclusion

The Actel IGLOO, Fusion, and ProASIC3 FPGAs are ideal for applications that require field upgrades. The single-chip devices save board space by eliminating the need for EEPROM. The built-in AES with MAC enables transmission of programming data over any network without fear of design theft. IGLOO, Fusion, and ProASIC3 FPGAs are IEEE 1532–compliant and support STAPL, making the target programming software easy to implement.

Related Documents

Handbook Documents

FlashROM in Actel's Low-Power Flash Devices

http://www.actel.com/documents/LPD_FlashROM_HBs.pdf

Security in Low-Power Flash Devices

http://www.actel.com/documents/LPD_Security_HBs.pdf

Part Number and Revision Date

This document was previously published as an application note describing features and functions of the device, and as such has now been incorporated into the device handbook format. No technical changes have been made to the content.

Part Number 51700094-016-2

Revised June 2008

List of Changes

The following table lists critical changes that were made in the current version of the chapter.

Previous Version	Changes in the Current Version (v1.2)	Page
v1.1 (March 2008)	The following changes were made to the family descriptions in Table 16-1 · Low-Power Flash Families: • ProASIC3L was updated to include 1.5 V. • The number of PLLs for ProASIC3E was changed from five to six.	16-2
v1.0 (January 2008)	The "Microprocessor Programming Support in Low-Power Devices" section was updated to include information on the IGLOO PLUS family. The "IGLOO Terminology" section and "ProASIC3 Terminology" section are new.	16-2

Boundary Scan and UJTAG

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17 – Boundary Scan in Low-Power Flash Devices

Boundary Scan

Low-power flash devices are compatible with IEEE Standard 1149.1, which defines a hardware architecture and the set of mechanisms for boundary scan testing. JTAG operations are used during boundary scan testing.

The basic boundary scan logic circuit is composed of the TAP controller, test data registers, and instruction register (Figure 17-2 on page 17-4).

Low-power flash devices support three types of test data registers: bypass, device identification, and boundary scan. The bypass register is selected when no other register needs to be accessed in a device. This speeds up test data transfer to other devices in a test data path. The 32-bit device identification register is a shift register with four fields (LSB, ID number, part number, and version). The boundary scan register observes and controls the state of each I/O pin. Each I/O cell has three boundary scan register cells, each with serial-in, serial-out, parallel-in, and parallel-out pins.

TAP Controller State Machine

The TAP controller is a 4-bit state machine (16 states) that operates as shown in Figure 17-1.

The 1s and 0s represent the values that must be present on TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power-up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain HIGH for five TCK cycles. The TRST pin can also be used to asynchronously place the TAP controller in the Test-Logic-Reset state.

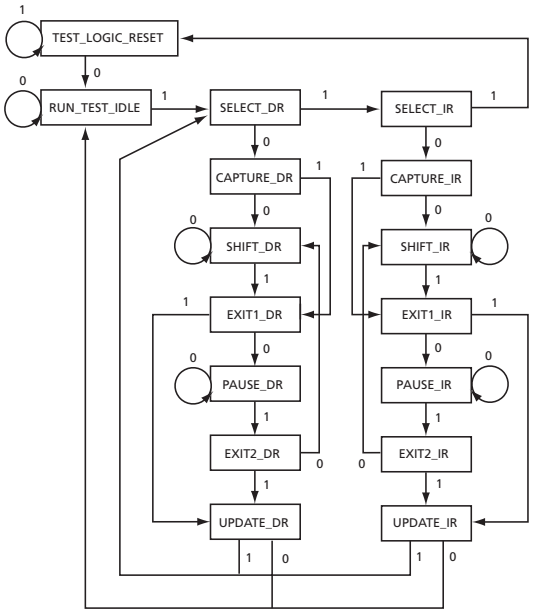


Figure 17-1 • **TAP Controller State Machine**

Actel's Flash Families Support the JTAG Feature

The low-power flash families listed in Table 17-1 support the JTAG feature and the functions described in this document.

Table 17-1 • **Low-Power Flash Families**

Family[1]	Description	Timing Numbers[2]
IGLOO®	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*IGLOO DC and Switching Characteristics*
IGLOO PLUS	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology and enhanced I/O capabilities	*IGLOO PLUS DC and Switching Characteristics*
IGLOOe	IGLOO devices enhanced with higher density, five additional PLLs, and additional I/O standards	*IGLOOe DC and Switching Characteristics*
ProASIC®3L	Low-power high-performance 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*ProASIC3L DC and Switching Characteristics*
ProASIC3	Low-power, high-performance 1.5 V FPGAs	*ProASIC3 DC and Switching Characteristics*
ProASIC3E	ProASIC3 enhanced with higher density, six additional PLLs, and additional I/O standards	*ProASIC3E DC and Switching Characteristics*
ProASIC3 Automotive	Low-power, high-performance FPGAs qualified for automotive applications	*Automotive ProASIC3 DC and Switching Characteristics*
Fusion	Low-power mixed-signal Programmable System Chip (PSC)	*Fusion DC and Power Characteristics*

Notes:

1. *The family names are linked to the appropriate product brief.*
2. *The timing number links go to the relevant timing numbers in the datasheet.*

Actel's low-power flash devices (listed in Table 17-1) provide a selection of low-power, secure, live-at-power-up, single-chip solutions. The nonvolatile flash-based devices do not require a boot PROM and incorporate FlashLock® technology, which provides a unique combination of reprogrammability and design security without external overhead. Only low-power flash FPGAs can offer these advantages.

Actel IGLOO PLUS FPGAs are the industry-leading 1.2 V ultra-low-power programmable logic devices (PLDs) and consume 90% less static power and over 50% less dynamic power than PLD alternatives, while ProASIC3L devices offer a balance of low power and higher performance.

Flash*Freeze technology used in IGLOO, IGLOO PLUS, and ProASIC3L devices enables easy entry to and exit from the ultra-low power mode, which consumes as little as 5 µW, while retaining SRAM and register data. IGLOO PLUS also offers the ability to hold I/O state in Flash*Freeze mode. Flash*Freeze technology simplifies power management through I/O and clock management without the need to turn off voltages, I/Os, or clocks at the system level. Entering and exiting Flash*Freeze mode takes less than 1 µs.

The Actel Fusion® family, based on the highly successful ProASIC3 flash FPGA architecture, has been designed as a high-performance, mixed-signal Programmable System Chip. Fusion supports many peripherals, including embedded flash memory, analog-to-digital converter (ADC), high-drive outputs, RC and crystal oscillators, and real-time counter (RTC). The total available on-chip memory, including the flash array blocks, is greater than that found in SRAM FPGAs.

IGLOO Terminology

In documentation, the term IGLOO families or IGLOO devices refers to all IGLOO families as listed in Table 17-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

ProASIC3 Terminology

In documentation, the term ProASIC3 families or ProASIC3 devices refers to all ProASIC3 families as listed in Table 17-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

Boundary Scan Support in Low-Power Devices

The information in this document applies to all IGLOO, Fusion, and ProASIC3 devices. For IGLOO, IGLOO PLUS, and ProASIC3L devices, the Flash*Freeze pin must be deasserted for successful boundary scan operations. Devices cannot enter JTAG mode directly from Flash*Freeze mode.

Boundary Scan Opcodes

Low-power flash devices support all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD, and BYPASS) and the optional IDCODE instruction (Table 17-2).

Table 17-2 • **Boundary Scan Opcodes**

	Hex Opcode
EXTEST	00
HIGHZ	07
USERCODE	0E
SAMPLE/PRELOAD	01
IDCODE	0F
CLAMP	05
BYPASS	FF

Boundary Scan Chain

The serial pins are used to serially connect all the boundary scan register cells in a device into a boundary scan register chain (Figure 17-2 on page 17-4), which starts at the TDI pin and ends at the TDO pin. The parallel ports are connected to the internal core logic I/O tile and the input, output, and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.

Each test section is accessed through the TAP, which has five associated pins: TCK (test clock input), TDI, TDO (test data input and output), TMS (test mode selector), and TRST (test reset input). TMS, TDI, and TRST are equipped with pull-up resistors to ensure proper operation when no input data is supplied to them. These pins are dedicated for boundary scan test usage. Refer to the "JTAG Pins" description in *Pin Descriptions* for pull-up/-down recommendations for TDO and TCK pins.

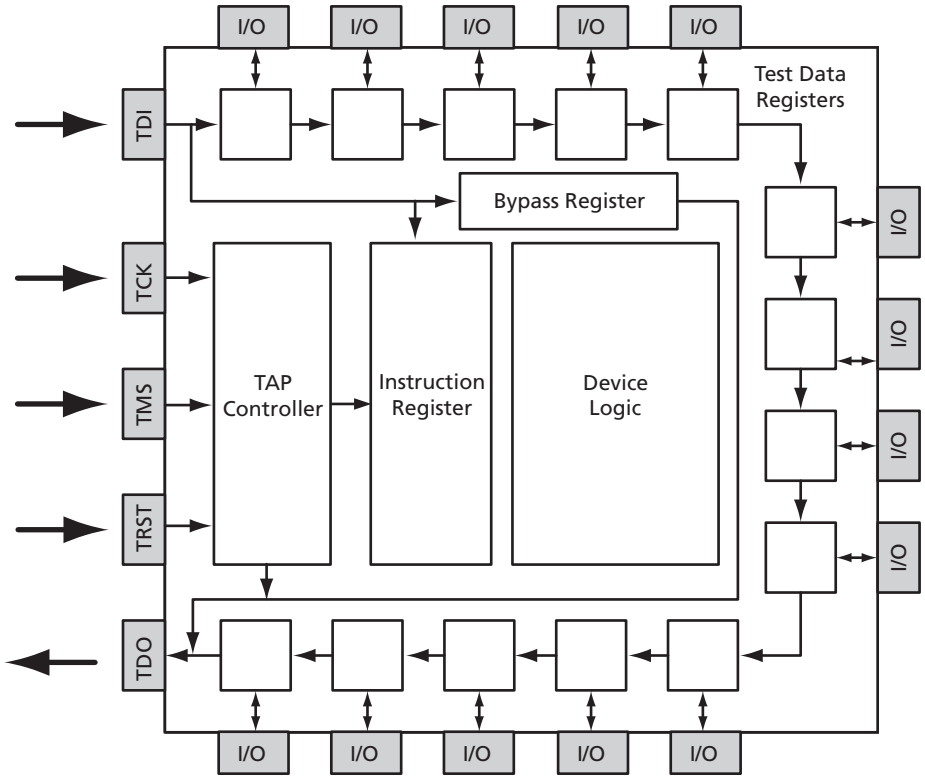


Figure 17-2 **• Boundary Scan Chain**

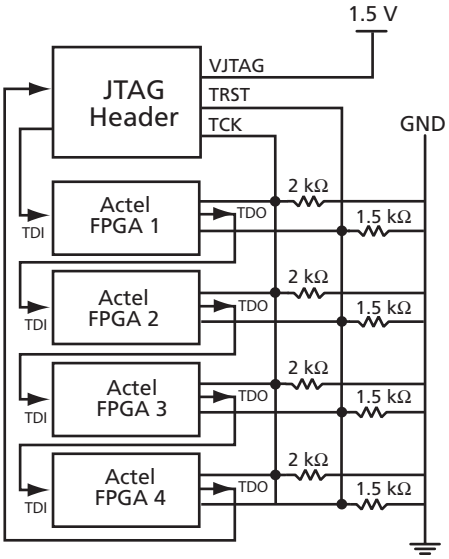
Board Level Recommendations

Table 17-3 gives pull-down recommendations for the TRST and TCK pins.

Table 17-3 **• TRST and TCK Pull-Down Recommendations**

V_{JTAG}	Tie-Off Resistance*
V_{JTAG} at 3.3 V	200 Ω to 1 kΩ
V_{JTAG} at 2.5 V	200 Ω to 1 kΩ
V_{JTAG} at 1.8 V	500 Ω to 1 kΩ
V_{JTAG} at 1.5 V	500 Ω to 1 kΩ

* *Equivalent parallel resistance if more than one device is on JTAG chain (Figure 17-3)*



Note: TCK is correctly wired with an equivalent tie-off resistance of 500 Ω, which satisfies the table for V_{JTAG} of 1.5 V. The resistor values for TRST are not appropriate in this case, as the tie-off resistance of 375 Ω is below the recommended minimum for V_{JTAG} = 1.5 V, but would be appropriate for a V_{JTAG} setting of 2.5 V or 3.3 V.

***Figure 17-3* • Parallel Resistance on JTAG Chain of Devices**

Related Documents

Handbook Documents

Pin Descriptions

http://www.actel.com/documents/LPD_PinDescriptions_HBs.pdf

Part Number and Revision Date

This document contains content extracted from the Device Architecture section of the datasheet. To improve usability for customers, the device architecture information has now been split into handbook sections, which also include usage information. No technical changes were made to the content unless explicitly listed.

Part Number 51700094-019-2

Revised June 2008

List of Changes

The following table lists critical changes that were made in the current version of the chapter.

Previous Version	Changes in Current Version (v1.2)	Page
v1.1 (March 2008)	The following changes were made to the family descriptions in Table 17-1 · Low-Power Flash Families: • ProASIC3L was updated to include 1.5 V. • The number of PLLs for ProASIC3E was changed from five to six.	17-2
v1.0 (January 2008)	The chapter was updated to include the IGLOO PLUS family and information regarding 15 k gate devices.	N/A
	The "IGLOO Terminology" section and "ProASIC3 Terminology" section are new.	17-2

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18 – UJTAG Applications in Actel's Low-Power Flash Devices

Introduction

In IGLOO,® Fusion, and ProASIC®3 devices, there is bidirectional access from the JTAG port to the core VersaTiles during normal operation of the device (Figure 18-1). User JTAG (UJTAG) is the ability for the design to use the JTAG ports for access to the device for updates, etc. While regular JTAG is used, the UJTAG tiles, located at the southeast area of the die, are directly connected to the JTAG Test Access Port (TAP) Controller in normal operating mode. As a result, all the functional blocks of the device, such as Clock Conditioning Circuits (CCC) with PLLs, SRAM blocks, embedded FlashROM, flash memory blocks, and I/O tiles, can be reached via the JTAG ports. The UJTAG functionality is available by instantiating the UJTAG macro directly in the source code of a design. Access to the FPGA core VersaTiles from the JTAG ports enables users to implement different applications using the TAP Controller (JTAG port). This document introduces the UJTAG tile functionality and discusses a few application examples. However, the possible applications are not limited to what is presented in this document. UJTAG can serve different purposes in many designs as an elementary or auxiliary part of the design. For detailed usage information, refer to *Boundary Scan in Low-Power Flash Devices*.

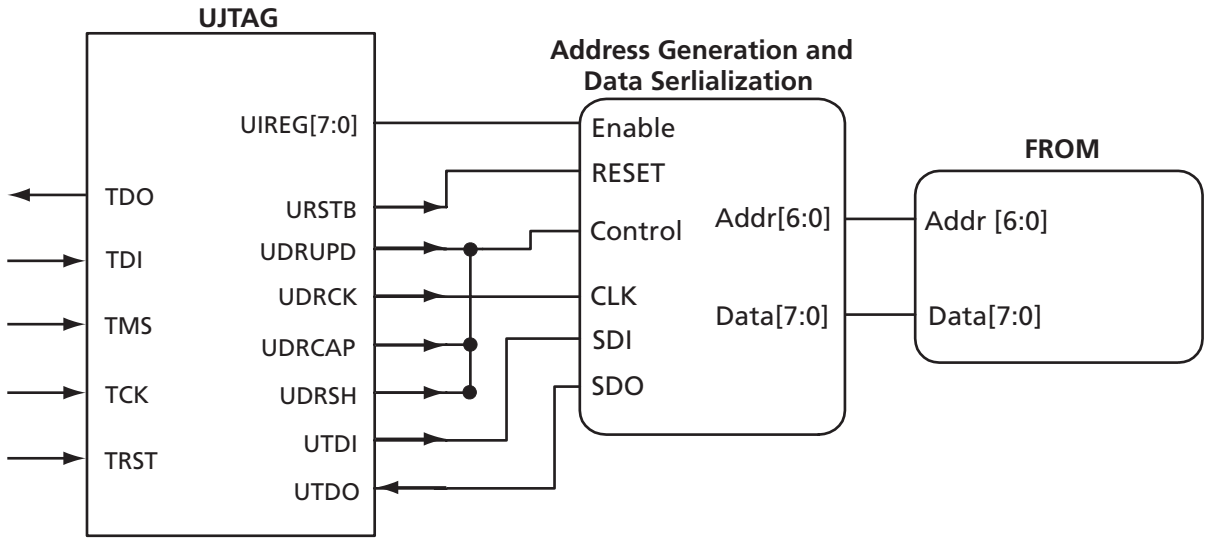


Figure 18-1 • **Block Diagram of Using UJTAG to Read FlashROM Contents**

UJTAG Support in Low-Power Devices

The low-power flash families listed in Table 18-1 support the UJTAG feature and the functions described in this document. The family name links to the datasheet for each family. Any required timing details are linked from the Timing Numbers column to the relevant datasheet sections.

Table 18-1 • **Low-Power Flash Families**

Family[1]	Description	Timing Numbers[2]
IGLOO	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*IGLOO DC and Switching Characteristics*
IGLOO PLUS	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology and enhanced I/O capabilities	*IGLOO PLUS DC and Switching Characteristics*
IGLOOe	IGLOO devices enhanced with higher density, five additional PLLs, and additional I/O standards	*IGLOOe DC and Switching Characteristics*
ProASIC3L	Low-power, high-performance 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*ProASIC3L DC and Switching Characteristics*
ProASIC3	Low-power, high-performance 1.5 V FPGAs	*ProASIC3 DC and Switching Characteristics*
ProASIC3E	ProASIC3 enhanced with higher density, six additional PLLs, and additional I/O standards	*ProASIC3E DC and Switching Characteristics*
ProASIC3 Automotive	Low-power, high-performance FPGAs qualified for Automotive applications	*Automotive ProASIC3 DC and Switching Characteristics*
Fusion	Low-power mixed-signal Programmable System Chip (PSC)	*Fusion DC and Power Characteristics*

Notes:

1. *The family names are linked to the appropriate product brief.*
2. *The timing number links go to the relevant timing numbers in the datasheet.*

Actel's low-power flash devices (listed in Table 18-1) provide a selection of low-power, secure, live-at-power-up, single-chip solutions. The nonvolatile flash-based devices do not require a boot PROM and incorporate FlashLock® technology, which provides a unique combination of reprogrammability and design security without external overhead. Only low-power flash FPGAs can offer these advantages.

Actel IGLOO PLUS FPGAs are the industry-leading 1.2 V ultra-low-power programmable logic devices (PLDs) and consume 90% less static power and over 50% less dynamic power than PLD alternatives, while ProASIC3L devices offer a balance of low power and higher performance.

Flash*Freeze technology used in IGLOO, IGLOO PLUS, and ProASIC3L devices enables easy entry to and exit from the ultra-low power mode, which consumes as little as 5 µW, while retaining SRAM and register data. IGLOO PLUS also offers the ability to hold I/O state in Flash*Freeze mode. Flash*Freeze technology simplifies power management through I/O and clock management without the need to turn off voltages, I/Os, or clocks at the system level. Entering and exiting Flash*Freeze mode takes less than 1 µs.

The Actel Fusion® family, based on the highly successful ProASIC3 flash FPGA architecture, has been designed as a high-performance, mixed-signal Programmable System Chip. Fusion supports many peripherals, including embedded flash memory, analog-to-digital converter (ADC), high-drive outputs, RC and crystal oscillators, and real-time counter (RTC). The total available on-chip memory, including the flash array blocks, is greater than that found in SRAM FPGAs.

IGLOO Terminology

In documentation, the term IGLOO families or IGLOO devices refers to all IGLOO families as listed in Table 18-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

ProASIC3 Terminology

In documentation, the term ProASIC3 families or ProASIC3 devices refers to all ProASIC3 families as listed in Table 18-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

UJTAG Macro

The UJTAG tiles can be instantiated in a design using the UJTAG macro from the IGLOO, Fusion, or ProASIC3 macro library. Note that "UJTAG" is a reserved name and cannot be used for any other user-defined blocks. A block symbol of the UJTAG tile macro is presented in Figure 18-2. In this figure, the ports on the left side of the block are connected to the JTAG TAP Controller, and the right-side ports are accessible by the FPGA core VersaTiles. The TDI, TMS, TDO, TCK, and TRST ports of UJTAG are only provided for design simulation purposes and should be treated as external signals in the design netlist. However, these ports must NOT be connected to any I/O buffer in the netlist. Figure 18-3 on page 18-4 illustrates the correct connection of the UJTAG macro to the user design netlist. Actel Designer software will automatically connect these ports to the TAP during place-and-route. Table 18-2 gives the port descriptions for the rest of the UJTAG ports:

Table 18-2 • **UJTAG Port Descriptions**

Port	Description
UIREG [7:0]	This 8-bit bus carries the contents of the JTAG Instruction Register of each device. Instruction Register values 16 to 127 are not reserved and can be employed as user-defined instructions.
URSTB	URSTB is an active-low signal and will be asserted when the TAP Controller is in Test-Logic-Reset mode. URSTB is asserted at power-up, and a power-on reset signal resets the TAP Controller. URSTB will stay asserted until an external TAP access changes the TAP Controller state.
UTDI	This port is directly connected to the TAP's TDI signal.
UTDO	This port is the user TDO output. Inputs to the UTDO port are sent to the TAP TDO output MUX when the IR address is in user range.
UDRSH	Active-high signal enabled in the ShiftDR TAP state
UDRCAP	Active-high signal enabled in the CaptureDR TAP state
UDRCK	This port is directly connected to the TAP's TCK signal.
UDRUPD	Active-high signal enabled in the UpdateDR TAP state

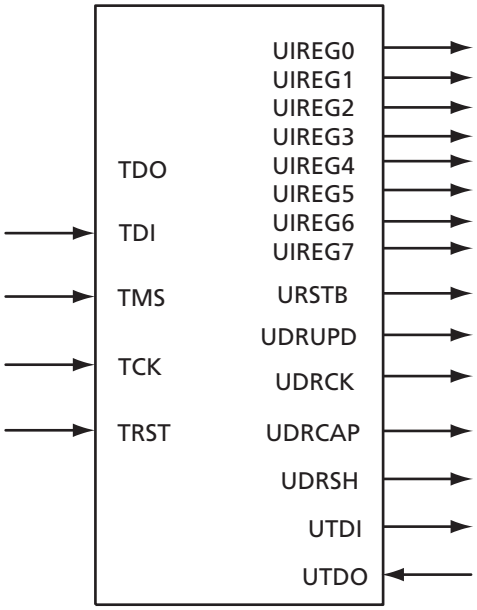
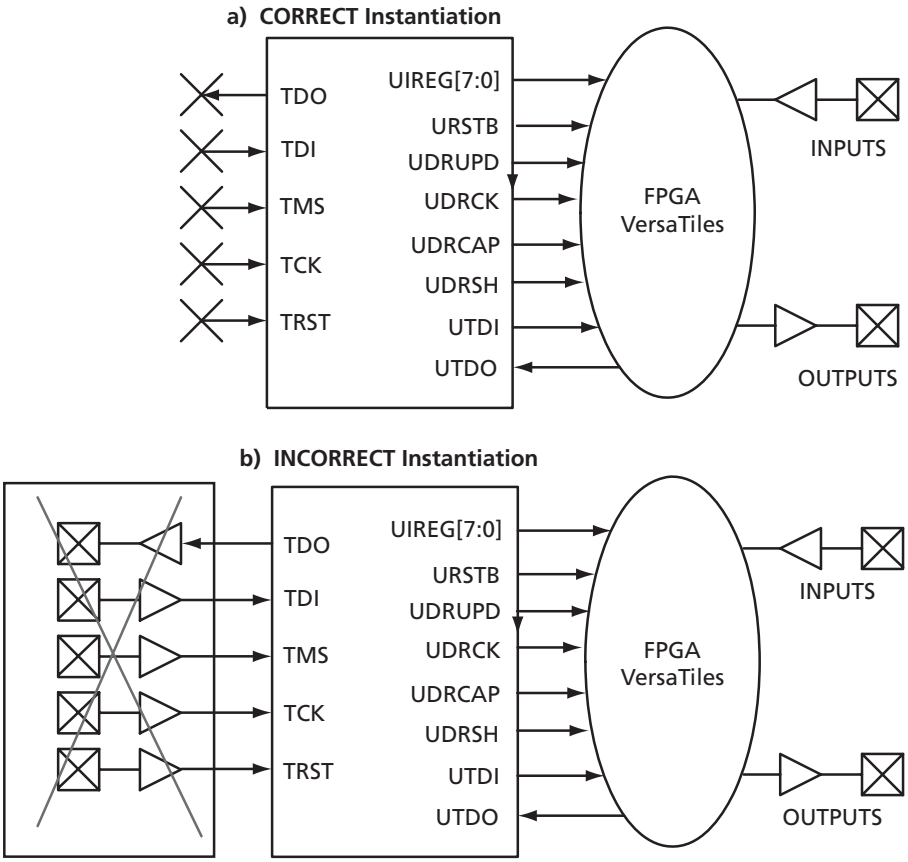


Figure 18-2 • **UJTAG Tile Block Symbol**



Note: Do not connect JTAG pins (TDO, TDI, TMS, TCK, or TRST) to I/Os in the design.

***Figure 18-3* • Connectivity Method of UJTAG Macro**

UJTAG Operation

There are a few basic functions of the UJTAG macro that users must understand before designing with it. The most important fundamental concept of the UJTAG design is its connection with the TAP Controller state machine.

TAP Controller State Machine

The 16 states of the Tap Controller state machine are shown in Figure 18-4 on page 18-5. The 1s and 0s, shown adjacent to the state transitions, represent the TMS values that must be present at the time of a rising TCK edge for a state transition to occur. In the states that include the letters "IR," the instruction register operates; in the states that contain the letters "DR," the test data register operates. The TAP Controller receives two control inputs, TMS and TCK, and generates control and clock signals for the rest of the test logic.

On power-up (or the assertion of TRST), the TAP Controller enters the Test-Logic-Reset state. To reset the controller from any other state, TMS must be held HIGH for at least five TCK cycles. After reset, the TAP state changes at the rising edge of TCK, based on the value of TMS.

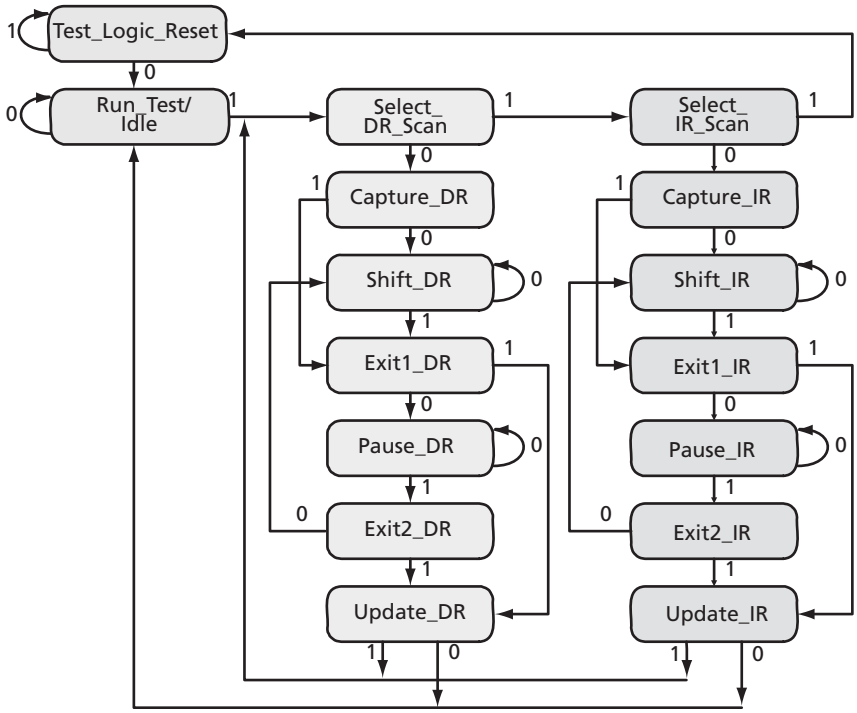


Figure 18-4 **• TAP Controller State Diagram**

UJTAG Port Usage

UIREG[7:0] hold the contents of the JTAG instruction register. The UIREG vector value is updated when the TAP Controller state machine enters the Update_IR state. Instructions 16 to 127 are user-defined and can be employed to encode multiple applications and commands within an application. Loading new instructions into the UIREG vector requires users to send appropriate logic to TMS to put the TAP Controller in a full IR cycle starting from the Select IR_Scan state and ending with the Update_IR state.

UTDI, UTDO, and UDRCK are directly connected to the JTAG TDI, TDO, and TCK ports, respectively. The TDI input can be used to provide either data (TAP Controller in the Shift_DR state) or the new contents of the instruction register (TAP Controller in the Shift_IR state).

UDRSH, UDRUPD, and UDRCAP are HIGH when the TAP Controller state machine is in the Shift_DR, Update_DR, and Capture_DR states, respectively. Therefore, they act as flags to indicate the stages of the data shift process. These flags are useful for applications in which blocks of data are shifted into the design from JTAG pins. For example, an active UDRSH can indicate that UTDI contains the data bitstream, and UDRUPD is a candidate for the end-of-data-stream flag.

As mentioned earlier, users should not connect the TDI, TDO, TCK, TMS, and TRST ports of the UJTAG macro to any port or net of the design netlist. The Designer software will automatically handle the port connection.

Typical UJTAG Applications

Bidirectional access to the JTAG port from VersaTiles—without putting the device into test mode—creates flexibility to implement many different applications. This section describes a few of these. All are based on importing/exporting data through the UJTAG tiles.

Clock Conditioning Circuitry—Dynamic Reconfiguration

In low-power flash devices, CCCs, which include PLLs, can be configured dynamically through either an 81-bit embedded shift register or static flash programming switches. These 81 bits control all the characteristics of the CCC: routing MUX architectures, delay values, divider values, etc. Table 18-3 lists the 81 configuration bits in the CCC.

Table 18-3 • **Configuration Bits of IGLOO and ProASIC3 CCC Blocks**

Bit Number	Control Function
80	RESET ENABLE
79	DYNCSEL
78	DYNBSEL
77	DYNASEL
<76:74>	VCOSEL [2:0]
73	STATCSEL
72	STATBSEL
71	STATASEL
<70:66>	DLYC [4:0]
<65:61>	DLYB {4:0]
<60:56>	DLYGLC [4:0]
<55:51>	DLYGLB [4:0]
<50:46>	DLYGLA [4:0]
45	XDLYSEL
<44:40>	FBDLY [4:0]
<39:38>	FBSEL
<37:35>	OCMUX [2:0]
<34:32>	OBMUX [2:0]
<31:29>	OAMUX [2:0]
<28:24>	OCDIV [4:0]
<23:19>	OBDIV [4:0]
<18:14>	OADIV [4:0]
<13:7>	FBDIV [6:0]
<6:0>	FINDIV [6:0]

The embedded 81-bit shift register (for the dynamic configuration of the CCC) is accessible to the VersaTiles, which, in turn, have access to the UJTAG tiles. Therefore, the CCC configuration shift register can receive and load the new configuration data stream from JTAG.

Dynamic reconfiguration eliminates the need to reprogram the device when reconfiguration of the CCC functional blocks is needed. The CCC configuration can be modified while the device continues to operate. Employing the UJTAG core requires the user to design a module to provide the configuration data and control the CCC configuration shift register. In essence, this is a user-designed TAP Controller requiring chip resources.

Similar reconfiguration capability exists in the Actel ProASIC^PLUS® family. The only difference is the number of shift register bits controlling the CCC (27 in ProASIC^PLUS and 81 in IGLOO, ProASIC3, and Fusion).

Fine Tuning

In some applications, design constants or parameters need to be modified after programming the original design. The tuning process can be done using the UJTAG tile without reprogramming the device with new values. If the parameters or constants of a design are stored in distributed registers or embedded SRAM blocks, the new values can be shifted onto the JTAG TAP Controller pins, replacing the old values. The UJTAG tile is used as the "bridge" for data transfer between the JTAG pins and the FPGA VersaTiles or SRAM logic. Figure 18-5 shows a flow chart example for fine-tuning application steps using the UJTAG tile.

In Figure 18-5, the TMS signal sets the TAP Controller state machine to the appropriate states. The flow mainly consists of two steps: a) shifting the defined instruction and b) shifting the new data. If the target parameter is constantly used in the design, the new data can be shifted into a temporary shift register from UTDI. The UDRSH output of UJTAG can be used as a shift-enable signal, and UDRCK is the shift clock to the shift register. Once the shift process is completed and the TAP Controller state is moved to the Update_DR state, the UDRUPD output of the UJTAG can latch the new parameter value from the temporary register into a permanent location. This avoids any interruption or malfunctioning during the serial shift of the new value.

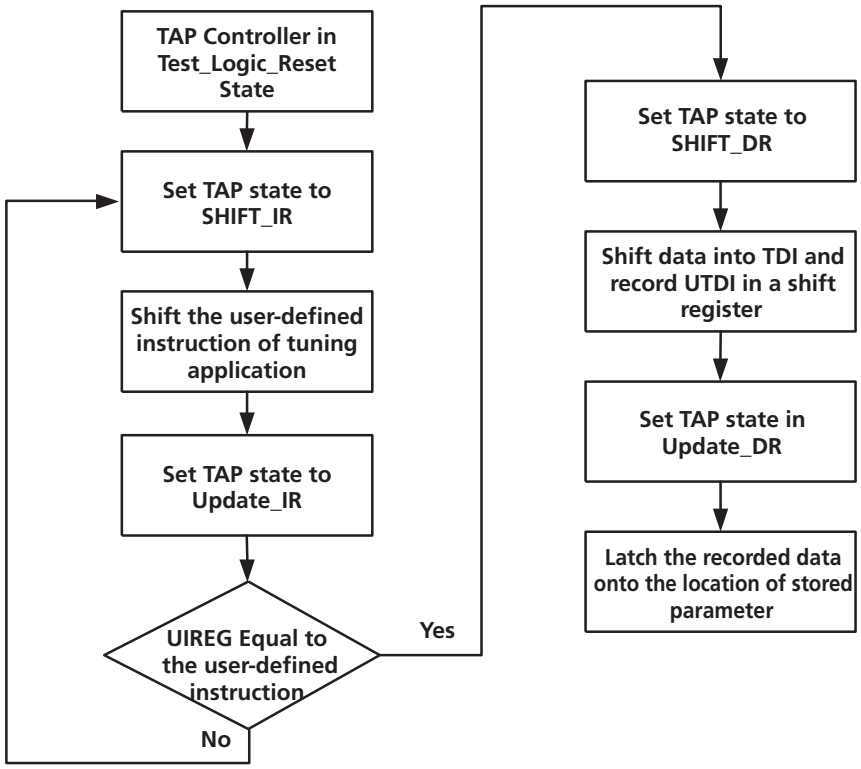


Figure 18-5 • **Flow Chart Example of Fine-Tuning an Application Using UJTAG**

Silicon Testing and Debugging

In many applications, the design needs to be tested, debugged, and verified on real silicon or in the final embedded application. To debug and test the functionality of designs, users may need to monitor some internal logic (or nets) during device operation. The approach of adding design test pins to monitor the critical internal signals has many disadvantages, such as limiting the number of user I/Os. Furthermore, adding external I/Os for test purposes may require additional or dedicated board area for testing and debugging.

The UJTAG tiles of low-power flash devices offer a flexible and cost-effective solution for silicon test and debug applications. In this solution, the signals under test are shifted out to the TDO pin of the TAP Controller. The main advantage is that all the test signals are monitored from the TDO pin; no pins or additional board-level resources are required. Figure 18-6 illustrates this technique. Multiple test nets are brought into an internal MUX architecture. The selection of the MUX is done using the contents of the TAP Controller instruction register, where individual instructions (values from 16 to 127) correspond to different signals under test. The selected test signal can be synchronized with the rising or falling edge of TCK (optional) and sent out to UTDO to drive the TDO output of JTAG.

The test and debug procedure is not limited to the example in Figure 18-5 on page 18-7. Users can customize the debug and test interface to make it appropriate for their applications. For example, multiple test signals can be registered and then sent out through UTDO, each at a different edge of TCK. In other words, *n* signals are sampled with an F_{TCK} / *n* sampling rate. The bandwidth of the information sent out to TDO is always proportional to the frequency of TCK.

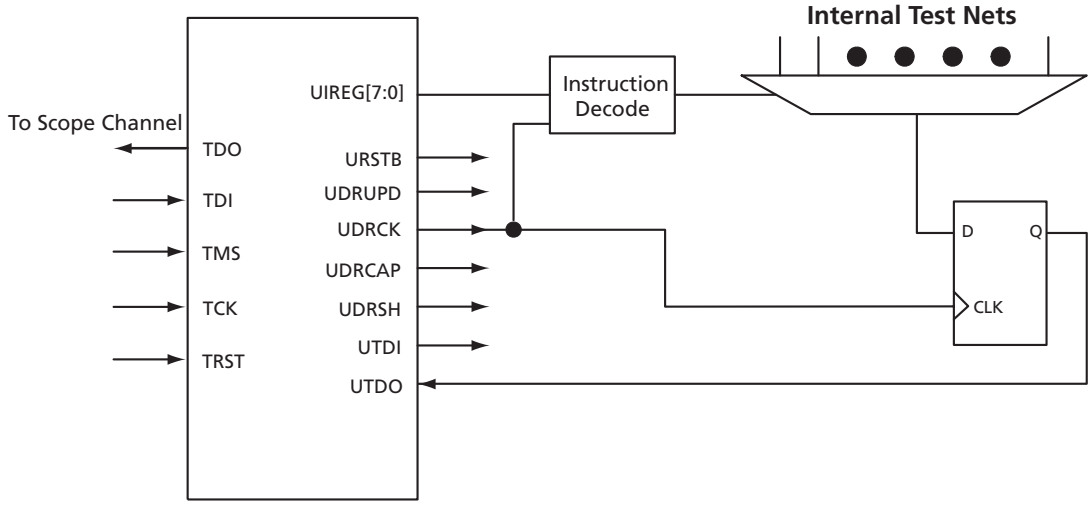


***Figure 18-6* • UJTAG Usage Example in Test and Debug Applications**

SRAM Initialization

Users can also initialize embedded SRAMs of the low-power flash devices. The initialization of the embedded SRAM blocks of the design can be done using UJTAG tiles, where the initialization data is imported using the TAP Controller. Similar functionality is available in ProASIC^{PLUS} devices using JTAG. The guidelines for implementation and design examples are given in the *RAM Initialization and ROM Emulation in ProASIC^{PLUS} Devices* application note.

SRAMs are volatile by nature; data is lost in the absence of power. Therefore, the initialization process should be done at each power-up if necessary.

FlashROM Read-Back Using JTAG

The low-power flash architecture contains a dedicated nonvolatile FlashROM block, which is formatted into eight 128-bit pages. For more information on FlashROM, refer to *FlashROM in Actel's Low-Power Flash Devices*. The contents of FlashROM are available to the VersaTiles during normal operation through a read operation. As a result, the UJTAG macro can be used to provide the FlashROM contents to the JTAG port during normal operation. Figure 18-7 illustrates a simple block diagram of using UJTAG to read the contents of FlashROM during normal operation.

The FlashROM read address can be provided from outside the FPGA through the TDI input or can be generated internally using the core logic. In either case, data serialization logic is required (Figure 18-7) and should be designed using the VersaTile core logic. FlashROM contents are read asynchronously in parallel from the flash memory and shifted out in a synchronous serial format to TDO. Shifting the serial data out of the serialization block should be performed while the TAP is in UDRSH mode. The coordination between TCK and the data shift procedure can be done using the TAP state machine by monitoring UDRSH, UDRCAP, and UDRUPD.

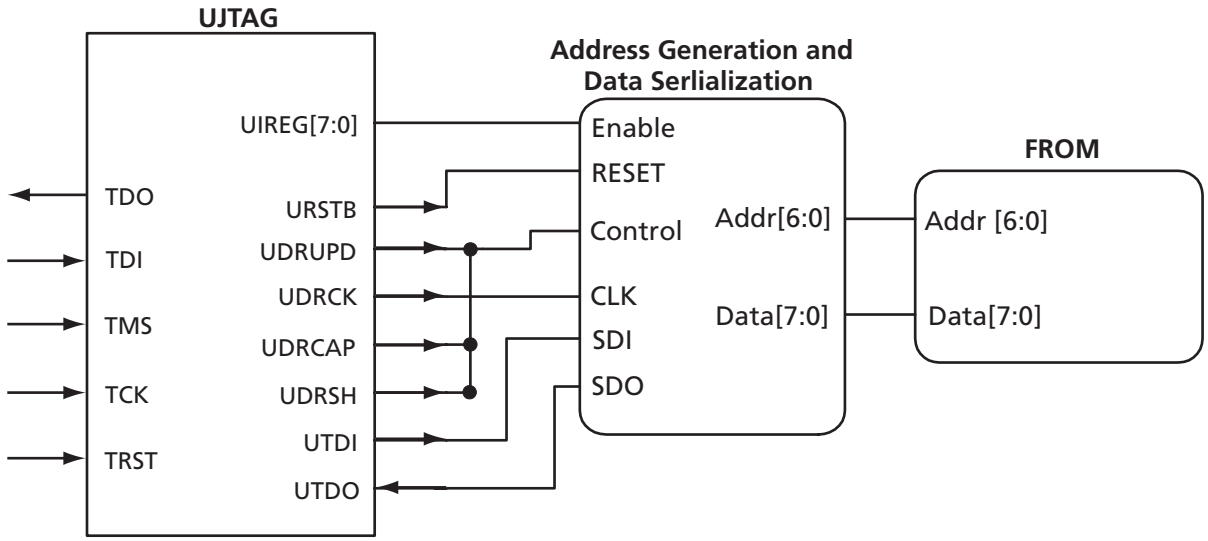


***Figure 18-7* • Block Diagram of Using UJTAG to Read FlashROM Contents**

Conclusion

Actel low-power flash FPGAs offer many unique advantages, such as security, nonvolatility, reprogrammablity, and low power—all in a single chip. In addition, IGLOO, Fusion, and ProASIC3 devices provide access to the JTAG port from core VersaTiles while the device is in normal operating mode. A wide range of available user-defined JTAG opcodes allows users to implement various types of applications, exploiting this feature of these devices. The connection between the JTAG port and core tiles is implemented through an embedded and hardwired UJTAG tile. A UJTAG tile can be instantiated in designs using the UJTAG library cell. This document presents multiple examples of UJTAG applications, such as dynamic reconfiguration, silicon test and debug, fine-tuning of the design, and RAM initialization. Each of these applications offers many useful advantages.

Related Documents

Application Notes

RAM Initialization and ROM Emulation in ProASIC^{PLUS} Devices

http://www.actel.com/documents/APA_RAM_Initd_AN.pdf

Handbook Documents

Boundary Scan in Low-Power Flash Devices

http://www.actel.com/documents/LPD_BoundaryScan_HBs.pdf

FlashROM in Actel's Low-Power Flash Devices

http://www.actel.com/documents/LPD_FlashROM_HBs.pdf

Part Number and Revision Date

This document contains content extracted from the Device Architecture section of the datasheet, combined with content previously published as an application note describing features and functions of the device. To improve usability for customers, the device architecture information has now been combined with usage information, to reduce duplication and possible inconsistencies in published information. No technical changes were made to the datasheet content unless explicitly listed. Changes to the application note content were made only to be consistent with existing datasheet information

Part Number 51700094-020-2

Revised June 2008

List of Changes

The following table lists critical changes that were made in the current version of the chapter.

Previous Version	Changes in Current Version (v1.2)	Page
v1.1 (March 2008)	The following changes were made to the family descriptions in Table 18-1 · Low-Power Flash Families: • ProASIC3L was updated to include 1.5 V. • The number of PLLs for ProASIC3E was changed from five to six.	18-2
v1.0 (January 2008)	The chapter was updated to include the IGLOO PLUS family and information regarding 15 k gate devices.	N/A
	The "IGLOO Terminology" section and "ProASIC3 Terminology" section are new.	18-2

Board-Level Requirements

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19 – Power-Up/-Down Behavior of Low-Power Flash Devices

Introduction

Actel's low-power flash devices are flash-based FPGAs manufactured on a 0.13 µm process node. These devices offer a single-chip, reprogrammable solution and support Level 0 live at power-up (LAPU) due to their nonvolatile architecture.

Actel's four low-power flash FPGA families are optimized for logic area, I/O features, and performance. IGLOO® devices are optimized for power, making them the industry's lowest power programmable solution. IGLOO PLUS FPGAs offer enhanced I/O features beyond those of the IGLOO ultra-low power solution for I/O-intensive low-power applications. ProASIC3®L FPGAs balance low power with high performance. The ProASIC3 family is Actel's high-performance flash FPGA solution.

Actel's low-power flash devices exhibit very low transient current on each power supply during power-up. The peak value of the transient current depends on the device size, temperature, voltage levels, and power-up sequence.

The following devices can have inputs driven in while the device is not powered:

- IGLOO (AGL015 and AGL030)
- IGLOO PLUS (AGLP030, AGLP060, AGLP125)
- IGLOOe (AGLE600, AGLE3000)
- ProASIC3L (A3PE3000L)
- ProASIC3 (A3P015 and A3P030)
- ProASIC3E (A3PE600, A3PE1500, A3PE3000)

The driven I/Os do not pull up power planes, and the current draw is limited to very small leakage current, making them suitable for applications that require cold-sparing. These devices are hot-swappable, meaning they can be inserted in a live power system.[1]

1. *For more details on the levels of hot-swap compatibility in Actel's low-power flash devices, refer to the "Hot-Swap Support" section in the I/O Structures chapter of the handbook for the device you are using.*

Actel's Flash Families Support Power-Up Behavior

The low-power flash families listed in Table 19-1 support power-up behavior and the functions described in this document.

Table 19-1 • **Low-Power Flash Families**

Family[1]	Description	Timing Numbers[2]
IGLOO	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*IGLOO DC and Switching Characteristics*
IGLOO PLUS	Ultra-low-power 1.2 V and 1.5 V FPGAs with Flash*Freeze technology and enhanced I/O capabilities	*IGLOO PLUS DC and Switching Characteristics*
IGLOOe	IGLOO devices enhanced with higher density, five additional PLLs, and additional I/O standards	*IGLOOe DC and Switching Characteristics*
ProASIC3L	Low-power high-performance 1.2 V and 1.5 V FPGAs with Flash*Freeze technology	*ProASIC3L DC and Switching Characteristics*
ProASIC3	Low-power, high-performance 1.5 V FPGAs	*ProASIC3 DC and Switching Characteristics*
ProASIC3E	ProASIC3 enhanced with higher density, six additional PLLs, and additional I/O standards	*ProASIC3E DC and Switching Characteristics*
ProASIC3 Automotive	Low-power, high-performance FPGAs qualified for automotive applications	*Automotive ProASIC3 DC and Switching Characteristics*

Notes:

1. *The family names are linked to the appropriate product brief.*
2. *The timing number links go to the relevant timing numbers in the datasheet.*

Actel's low-power flash devices (listed in Table 19-1) provide a selection of low-power, secure, live-at-power-up, single-chip solutions. The nonvolatile flash-based devices do not require a boot PROM and incorporate FlashLock® technology, which provides a unique combination of reprogrammability and design security without external overhead. Only low-power flash FPGAs can offer these advantages.

Actel IGLOO PLUS FPGAs are the industry-leading 1.2 V ultra-low-power programmable logic devices (PLDs) and consume 90% less static power and over 50% less dynamic power than PLD alternatives, while ProASIC3L devices offer a balance of low power and higher performance.

Flash*Freeze technology used in IGLOO, IGLOO PLUS, and ProASIC3L devices enables easy entry to and exit from the ultra-low power mode, which consumes as little as 5 µW, while retaining SRAM and register data. IGLOO PLUS also offers the ability to hold I/O state in Flash*Freeze mode. Flash*Freeze technology simplifies power management through I/O and clock management without the need to turn off voltages, I/Os, or clocks at the system level. Entering and exiting Flash*Freeze mode takes less than 1 µs.

IGLOO Terminology

In documentation, the term IGLOO families or IGLOO devices refers to all IGLOO families as listed in Table 19-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

ProASIC3 Terminology

In documentation, the term ProASIC3 families or ProASIC3 devices refers to all ProASIC3 families as listed in Table 19-1. Where the information applies to only one family or limited devices, these exclusions will be explicitly stated.

Power-Up/Down Sequence and Transient Current

Actel's low-power flash devices use the following main voltage pins during normal operation:[2]

- V_{CCPLX}
- V_{JTAG}
- V_{CC}: Voltage supply to the FPGA core
  - V_{CC} is 1.5 V ± 0.075 V for IGLOO, IGLOO PLUS, and ProASIC3 devices operating at 1.5 V.
  - V_{CC} is 1.2 V ± 0.06 V for IGLOO, IGLOO PLUS, and ProASIC3L devices operating at 1.2 V.
  - V5 devices will require a 1.5V V_{CC} supply, where as V2 devices can utilize either 1.2 V or 1.5 V V_{CC}.
- V_{CCI}Bx: Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number.
- VMVx: Quiet supply voltage to the input buffers of each I/O bank. x is the bank number. (Note: IGLOO PLUS devices do not have VMVx supply pins.)

The I/O bank VMV pin must be tied to the V_{CCI} pin within the same bank. Therefore, the supplies that need to be powered up/down during normal operation are V_{CC} and V_{CCI}. These power supplies can be powered up/down in any sequence during normal operation of IGLOO, IGLOO PLUS, ProASIC3L, and ProASIC3 FPGAs. During power-up, I/Os in each bank will remain tristated until the last supply (either V_{CCI}Bx or V_{CC}) reaches its functional activation voltage. Similarly, during power-down, I/Os of each bank are tristated once the first supply reaches its brownout deactivation voltage.

Although Actel's low-power flash devices have no power-up or power-down sequencing requirements, Actel identifies the following power conditions that will result in higher than normal transient current. Use this information to help maximize power savings:

Actel recommends tying V_{CCPLX} to V_{CC} and using proper filtering circuits to decouple V_{CC} noise from the PLL.

a. If V_{CCPLX} is powered up before V_{CC}, a static current of up to 5 mA (typical) per PLL may be measured on V_{CCPLX}.
   i. The current vanishes as soon as V_{CC} reaches V_{CCPLX} voltage level.
   ii. The same current is observed at power-down (V_{CC} before V_{CCPLX}).
b. If V_{CCPLX} is powered up simultaneously or after V_{CC}:
   i. Actel's low-power flash devices exhibit very low transient current on V_{CC}. For ProASIC3 devices, the maximum transient current on V_{CC} does not exceed the maximum standby current specified in the device datasheet.

The source of transient current, also known as inrush current, varies depending on the FPGA technology. Due to their volatile technology, the internal registers in SRAM FPGAs must be initialized before configuration can start. This initialization is the source of significant inrush current in SRAM FPGAs during power-up. Due to the nonvolatile nature of flash technology, low-power flash devices do not require any initialization at power-up, and there is very little or no crossbar current through PMOS and NMOS devices. Therefore, the transient current at power-up is significantly less than for SRAM FPGAs. Figure 19-1 on page 19-4 illustrates the types of power consumption by SRAM FPGAs compared to Actel's antifuse and flash FPGAs.

2. *For more information on Actel FPGA voltage supplies, refer to the appropriate datasheet located at http://www.actel.com/techdocs/ds.*

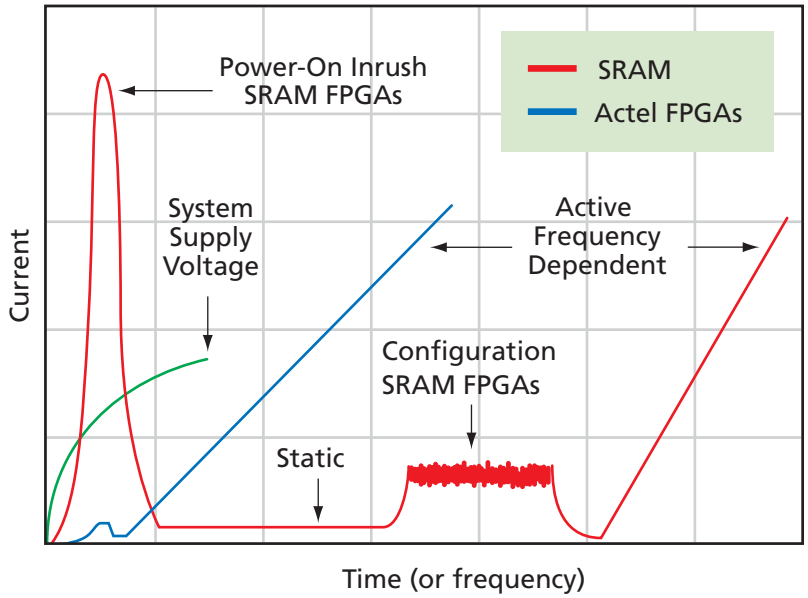

Figure 19-1 **• Types of Power Consumption in SRAM FPGAs and Actel Nonvolatile FPGAs**

Transient Current on V_{CC}

The characterization of the transient current on V_{CC} is performed on nearly all devices within the IGLOO, ProASIC3L, and ProASIC3 families. A sample size of five units is used from each device family member. All the device I/Os are internally pulled down while the transient current measurements are performed. For ProASIC3 devices, the measurements at typical conditions show that the maximum transient current on V_{CC}, when the power supply is powered at ramp-rates ranging from 15 V/ms to 0.15 V/ms, does not exceed the maximum standby current specified in the device datasheets. Refer to *ProASIC3 DC and Switching Characteristics* and *ProASIC3E DC and Switching Characteristics* for more information.

Similarly, IGLOO, IGLOO PLUS, and ProASIC3L devices exhibit very low transient current on V_{CC}. The transient current does not exceed the typical operating current of the device while in active mode. The characterization of AGL600-FG256 V2 and V5 devices has shown that the transient current on V_{CC} is typically in the range of 1–5 mA.

Transient Current on V_{CCI}

The characterization of the transient current on V_{CCI} is performed on nearly all devices within the IGLOO, IGLOO PLUS, ProASIC3L, and ProASIC3 families, similar to V_{CC} transient current measurements. For ProASIC3 devices, the measurements at typical conditions show that the maximum transient current on V_{CCI}, when the power supply is powered at ramp-rates ranging from 33 V/ms to 0.33 V/ms, does not exceed the maximum standby current specified in the device datasheet. Refer to *ProASIC3 DC and Switching Characteristics* and *ProASIC3E DC and Switching Characteristics* for more information.

Similarly, IGLOO, IGLOO PLUS, and ProASIC3L devices exhibit very low transient current on V_{CCI}. The transient current does not exceed the typical operating current of the device while in active mode. The characterization of AGL600-FG256 V2 and V5 devices has shown that the transient current on V_{CCI} is typically in the range of 1–2 mA.

I/O Behavior at Power-Up/-Down

This section discusses the behavior of device I/Os, used and unused, during power-up/-down of V_{CC} and V_{CCI}. As mentioned earlier, VMVx and V_{CCI}Bx are tied together, and therefore, inputs and outputs are powered up/down at the same time.

I/O State during Power-Up/-Down

This section discusses the characteristics of I/O behavior during device power-up and power-down. Before the start of power-up, all I/Os are in tristate mode. The I/Os will remain tristated during power-up until the last voltage supply (V_{CC} or V_{CCI}) is powered to its functional level (power supply functional levels are discussed in the "Power-Up to Functional Time" section on page 19-6). After the last supply reaches the functional level, the outputs will exit the tristate mode and drive the logic at the input of the output buffer. Similarly, the input buffers will pass the external logic into the FPGA fabric once the last supply reaches the functional level. The behavior of user I/Os is independent of the V_{CC} and V_{CCI} sequence or the state of other voltage supplies of the FPGA (V_{PUMP} and V_{JTAG}). Figure 19-2 shows the output buffer driving high and its behavior during power-up with 10 kΩ external pull-down. In Figure 19-2, V_{CC} is powered first, and V_{CCI} is powered 5 ms after V_{CC}. Figure 19-3 on page 19-6 shows the state of the I/O when V_{CCI} is powered about 5 ms before V_{CC}. In the circuitry shown in Figure 19-3 on page 19-6, the output is externally pulled down.

During power-down, device I/Os become tristated once the first power supply (V_{CC} or V_{CCI}) drops below its brownout voltage level. The I/O behavior during power-down is also independent of voltage supply sequencing.

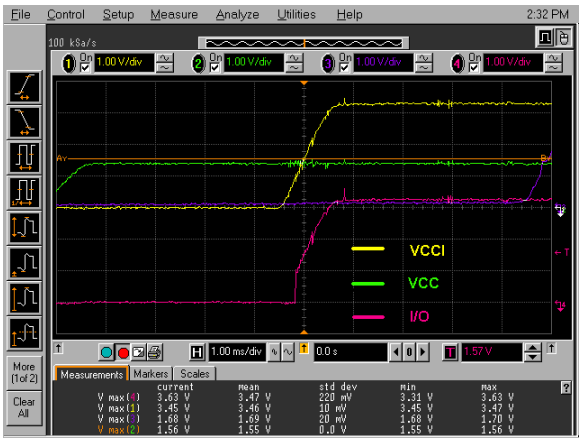

Figure 19-2 **• I/O State when V_{CC} Is Powered before V_{CCI}**

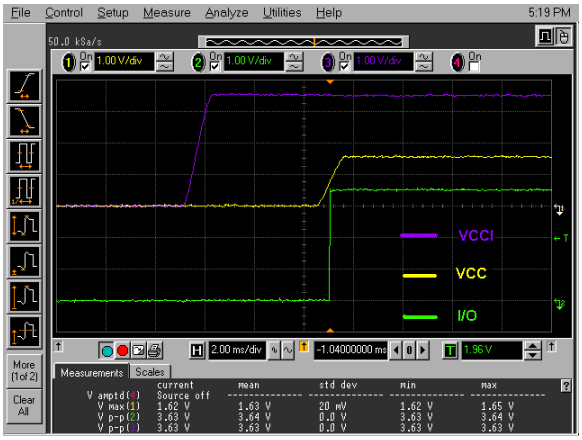

***Figure 19-3* • I/O State when V_{CCI} Is Powered before V_{CC}**

Power-Up to Functional Time

At power-up, device I/Os exit the tristate mode and become functional once the last voltage supply in the power-up sequence (V_{CCI} or V_{CC}) reaches its functional activation level. The power-up–to–functional time is the time it takes for the last supply to power up from zero to its functional level. Note, the functional level of the power supply during power-up may vary slightly within the specification in different ramp-rates. Refer to Table 19-2 for the functional level of the voltage supplies at power-up.

Typical I/O behavior during power-up to functional time is illustrated in Figure 19-2 on page 19-5 and Figure 19-3.

***Table 19-2* • Power-Up Functional Activation Levels for V_{CC} and V_{CCI}**

Device	V_{CC} Functional Activation Level (V)	V_{CCI} Functional Activation Level (V)
ProASIC3, IGLOO, IGLOO PLUS, and ProASIC3L families running at V_{CC} = 1.5 V*	0.85 V ± 0.25 V	0.9 V ± 0.3 V
IGLOO, IGLOO PLUS, and ProASIC3L families running at V_{CC} = 1.2 V*	0.85 V ± 0.2 V	0.9 V ± 0.15 V

Note: V5 devices will require a 1.5 V V_{CC} supply, where as V2 devices can utilize either 1.2 V or 1.5 V V_{CC}.

Actel's low-power flash devices meet Level 0 LAPU; that is, they can be functional prior to V_{CC} reaching the regulated voltage required. This important advantage distinguishes low-power flash devices from their SRAM-based counterparts. SRAM-based FPGAs, due to their volatile technology, require hundreds of milliseconds after power-up to configure the design bitstream before they become functional. Refer to Figure 19-4 on page 19-7 and Figure 19-5 on page 19-8 for more information.

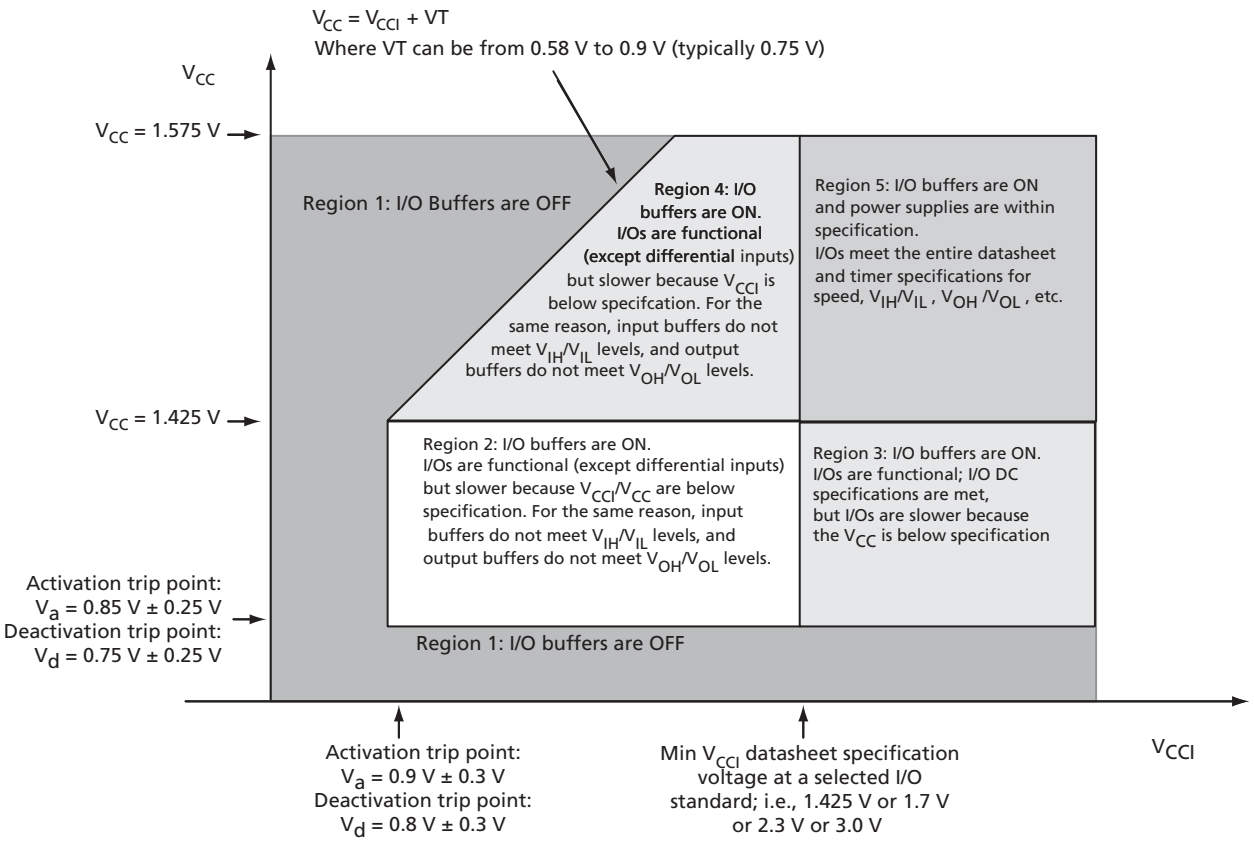

Figure 19-4 **• I/O State as a Function of V_{CCI} and V_{CC} Voltage Levels for IGLOO V5, IGLOO PLUS V5, ProASIC3L, and ProASIC3 Devices, Running at V_{CC} = 1.5 V ± 0.075 V**

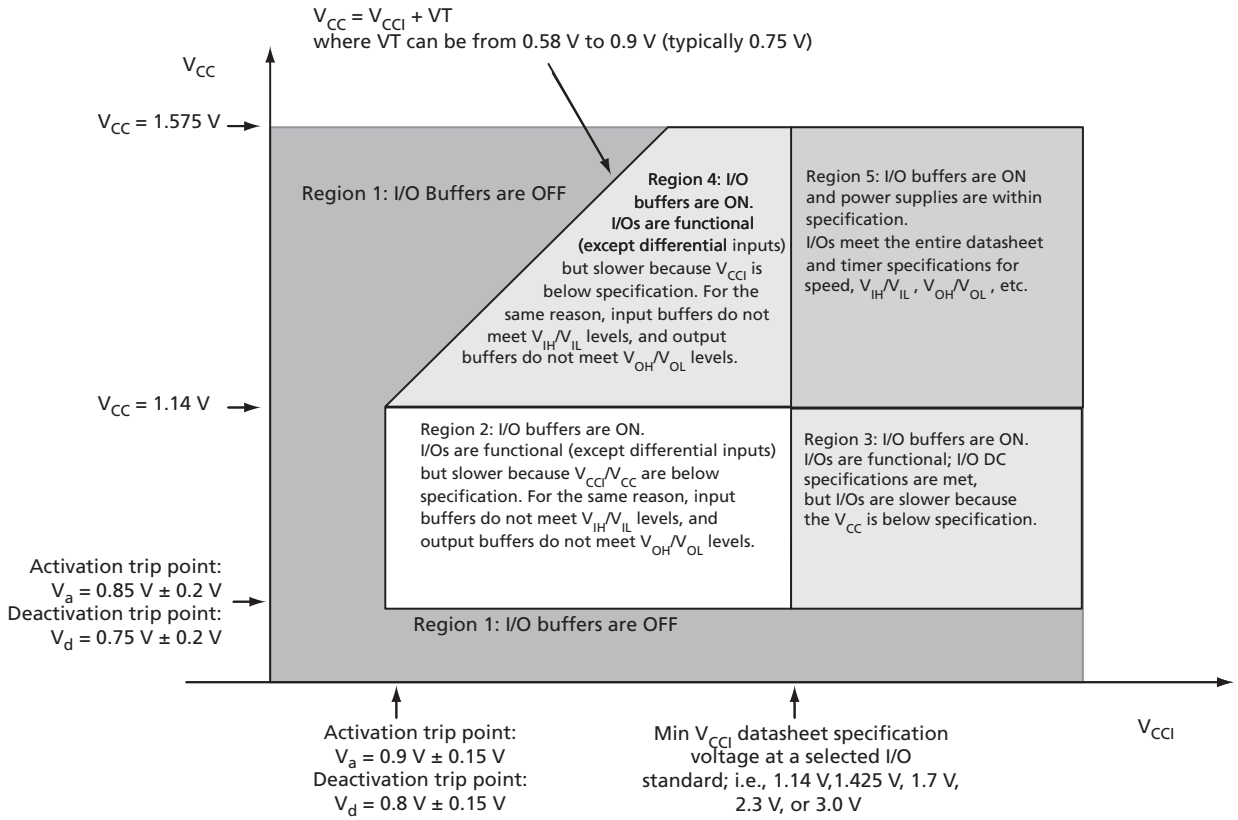

Figure 19-5 **• I/O State as a Function of V_{CCI} and V_{CC} Voltage Levels for IGLOO V2, IGLOO PLUS V2, and ProASIC3L Devices, Running at V_{CC} = 1.2 V ± 0.06 V**

Brownout Voltage

Brownout is a condition in which the voltage supplies are lower than normal, causing the device to malfunction as a result of insufficient power. In general, Actel does not guarantee the functionality of the design inside the flash FPGA if voltage supplies are below their minimum recommended operating condition. Actel has performed measurements to characterize the brownout levels of FPGA power supplies. Refer to Table 19-3 for device-specific brownout deactivation levels. For the purpose of characterization, a direct path from the device input to output is monitored while voltage supplies are lowered gradually. The brownout point is defined as the voltage level at which the output stops following the input. Characterization tests performed on several IGLOO, ProASIC3L, and ProASIC3 devices in typical operating conditions showed the brownout voltage levels to be within the specification.

During device power-down, the device I/Os become tristated once the first supply in the power-down sequence drops below its brownout deactivation voltage.

Table 19-3 • **Brownout Deactivation Levels for V_{CC} and V_{CCI}**

Devices	V_{CC} Brownout Deactivation Level (V)	V_{CCI} Brownout Deactivation Level (V)
ProASIC3, IGLOO, IGLOO PLUS and ProASIC3L families running at V_{CC} = 1.5 V	0.75 V ± 0.25 V	0.8 V ± 0.3 V
IGLOO, IGLOO PLUS, and ProASIC3L families running at V_{CC} = 1.2 V	0.75 V ± 0.2 V	0.8 V ± 0.15 V

PLL Behavior at Brownout Condition

When PLL power supply voltage and/or V_{CC} levels drop below the V_{CC} brownout levels mentioned above for 1.5 V and 1.2 V devices, the PLL output lock signal goes low and/or the output clock is lost. The following sections explain PLL behavior during and after the brownout condition.

V_{CCPLL} and V_{CC} Tied Together

In this condition, both V_{CC} and V_{CCPLL} drop below the 0.75 V (± 0.25 V or ± 0.2 V) brownout level. During the brownout recovery, once V_{CCPLL} and V_{CC} reach the activation point (0.85 ± 0.25 V or ± 0.2 V) again, the PLL output lock signal may still remain low with the PLL output clock signal toggling. If this condition occurs, there are two ways to recover the PLL output lock signal:

1. Cycle the power supplies of the PLL (power off and on) by using the PLL POWERDOWN signal.
2. Turn off the input reference clock to the PLL and then turn it back on.

Only V_{CCPLL} is at Brownout

In this case, only V_{CCPLL} drops below the 0.75 V (± 0.25 V or ± 0.2 V) brownout level and the V_{CC} supply remains at nominal recommended operating voltage (1.5 V ± 0.075 V for 1.5 V devices and 1.2 V ± 0.06 V for 1.2 V devices). In this condition, the PLL behavior after brownout recovery is similar to initial power-up condition, and the PLL will regain lock automatically after V_{CCPLL} is ramped up above the activation level (0.85 ± 0.25 V or ± 0.2 V). No intervention is necessary in this case.

Only V_{CC} Is at Brownout

In this condition, V_{CC} drops below the 0.75 V (± 0.25 V or ± 0.2 V) brownout level and V_{CCPLL} remains at nominal recommended operating voltage (1.5 V ± 0.075 V for 1.5 V devices and 1.2 V ± 0.06 V for 1.2 V devices). During the brownout recovery, once V_{CC} reaches the activation point again (0.85 ± 0.25 V or ± 0.2 V), the PLL output lock signal may still remain low with the PLL output clock signal toggling. If this condition occurs, there are two ways to recover the PLL output lock signal:

1. Cycle the power supplies of the PLL (power off and on) by using the PLL POWERDOWN signal.
2. Turn off the input reference clock to the PLL and then turn it back on.

It is important to note that Actel recommends using a monotonic power supply or voltage regulator to ensure proper power-up behavior.

Internal Pull-Up and Pull-Down

Low-power flash device I/Os are equipped with internal weak pull-up/-down resistors that can be used by designers. If used, these internal pull-up/-down resistors will be activated during power-up, once both V_{CC} and V_{CCI} are above their functional activation level. Similarly, during power-down, these internal pull-up/-down resistors will turn off once the first supply voltage falls below its brownout deactivation level.

Cold-Sparing

In cold-sparing applications, voltage can be applied to device I/Os before and during power-up. Cold-sparing applications rely on three important characteristics of the device:

1. I/Os must be tristated before and during power-up.
2. Voltage applied to the I/Os must not power up any part of the device.
3. V_{CCI} should not exceed 3.6 V, per datasheet specifications.

As described in the "Power-Up to Functional Time" section on page 19-6, Actel's low-power flash I/Os are tristated before and during power-up until the last voltage supply (V_{CC} or V_{CCI}) is powered up past its functional level. Furthermore, applying voltage to the FPGA I/Os does not pull up V_{CC} or V_{CCI} and, therefore, does not partially power up the device. Table 19-4 includes the cold-sparing test results on A3PE600-PQ208 devices. In this test, leakage current on the device I/O and residual voltage on the power supply rails were measured while voltage was applied to the I/O before power-up.

Table 19-4 • **Cold-Sparing Test Results for A3PE600 Devices**

Device I/O	Residual Voltage (V)		Leakage Current
	V_{CC}	V_{CCI}	
Input	0	0.003	<1 µA
Output	0	0.003	<1 µA

V_{CCI} must not exceed 3.6 V, as stated in the datasheet specification. Therefore, ProASIC3E devices meet all three requirements stated earlier in this section and are suitable for cold-sparing applications.

The following devices and families support cold-sparing:

- IGLOO: AGL015 and AGL030
- All IGLOO PLUS
- All IGLOOe
- ProASIC3L: A3PE3000L
- ProASIC3: A3P015 and A3P030
- All ProASIC3E

The following devices and families do not support cold-sparing:

- IGLOO: AGL060, AGL125, AGL250, AGL600, AGL1000
- ProASIC3: A3P060, A3P125, A3P250, A3P400, A3P600, A3P1000
- ProASIC3L: A3P250L, A3P600L, A3P1000L

Hot-Swap

Hot-swapping is the operation of hot insertion or hot removal of a card in a powered-up system. The I/Os need to be configured in hot-insertion mode if hot-swapping compliance is required. For more details on the levels of hot-swap compatibility in low-power flash devices, refer to the "Hot-Swap Support" section in the I/O Structures chapter of the handbook for the device you are using.

The following devices and families support hot-swapping:

- IGLOO: AGL015 and AGL030
- All IGLOO PLUS
- All IGLOOe
- ProASIC3L: A3PE3000L
- ProASIC3: A3P015 and A3P030
- All ProASIC3E

The following devices and families do not support hot-swapping:

- IGLOO: AGL060, AGL125, AGL250, AGL600, AGL1000
- ProASIC3: A3P060, A3P125, A3P250, A3P400, A3P600, A3P1000
- ProASIC3L: A3P250L, A3P600L, A3P1000L

Conclusion

Actel's low-power flash FPGAs provide an excellent programmable logic solution for a broad range of applications. In addition to high performance, low cost, security, nonvolatility, and single chip, they are live at power-up (meet Level 0 of the LAPU classification) and offer clear and easy-to-use power-up/-down characteristics. Unlike SRAM FPGAs, low-power flash devices do not require any specific power-up/-down sequencing and have extremely low power-up inrush current in any power-up sequence. Actel low-power flash FPGAs also support both cold-sparing and hot-swapping for applications requiring these capabilities.

Related Documents

Datasheets

ProASIC3 DC and Switching Characteristics

http://www.actel.com/documents/PA3GenSpecs_DS.pdf

ProASIC3E DC and Switching Characteristics

http://www.actel.com/documents/PA3EGenSpecs_DS.pdf

Handbook Documents

I/O Structures in IGLOO PLUS Devices

http://www.actel.com/documents/IGLOOPLUS_IO_HBs.pdf

I/O Structures in IGLOO and ProASIC3 Devices

http://www.actel.com/documents/IGLOO_PA3_IO_HBs.pdf

I/O Structures in IGLOOe and ProASIC3E Devices

http://www.actel.com/documents/IGLOOe_PA3E_IO_HBs.pdf

Part Number and Revision Date

This document was a previously published handbook chapter that only discussed ProASIC3/E (Power-Up Behavior of ProASIC3/E Devices, part number: 51700094-021), and has now been updated to include data for IGLOO and ProASIC3L families.

Part Number 51700094-027-0

Revised August 2008

List of Changes

The following table lists critical changes that were made in Power-Up Behavior of ProASIC3/E Devices, part number: 51700094-021.

Previous Version	Changes in Current Version (v1.0)	Page
v1.3 (March 2008)	This document was revised, renamed, and assigned a new part number. It now includes data for the IGLOO and ProASIC3L families.	N/A
v1.2 (January 2008) 51700094-021-2	The "Handbook Documents" section was updated to include the three different I/O Structure handbook chapters.	19-12
v1.1 (January 2008) 51700094-021-1	The first sentence of the "PLL Behavior at Brownout Condition" section was updated to read, "When PLL power supply voltage and/or V_{CC} levels drop below the V_{CC} brownout levels (0.75 V ± 0.25 V), the PLL output lock signal goes low and/or the output clock is lost."	19-9
v1.0 (January 2008) 51700094-021-0	The "PLL Behavior at Brownout Condition" section was added.	19-9

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www.actel.com

Actel Corporation
2061 Stierlin Court
Mountain View, CA
94043-4655 USA
Phone 650.318.4200
Fax 650.318.4600

Actel Europe Ltd.
River Court,Meadows Business Park
Station Approach, Blackwater
Camberley Surrey GU17 9AB
United Kingdom
Phone +44 (0) 1276 609 300
Fax +44 (0) 1276 607 540

Actel Japan
EXOS Ebisu Buillding 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan
Phone +81.03.3445.7671
Fax +81.03.3445.7668
http://jp.actel.com

Actel Hong Kong
Room 2107, China Resources Building
26 Harbour Road
Wanchai, Hong Kong
Phone +852 2185 6460
Fax +852 2185 6488
www.actel.com.cn

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