Programmable Logic Device
Course Embedded Systems (SEm)
PLD

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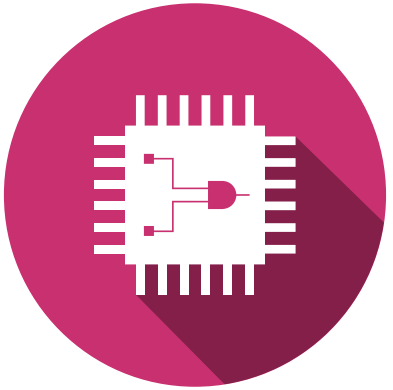
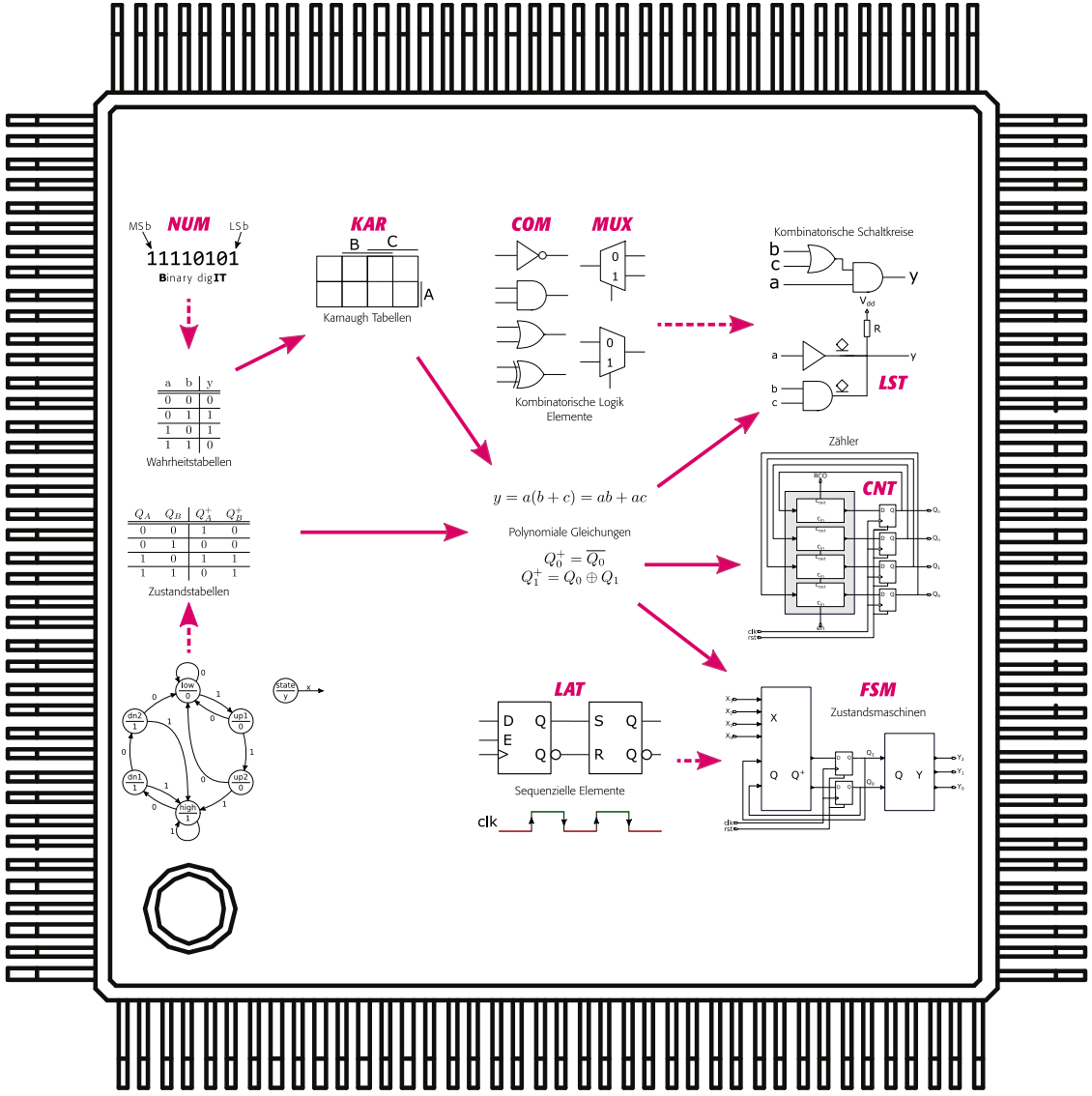


Degree program Systems Engineering
Specialization Infotronics – Embedded Systems

Current content of the topic in the course

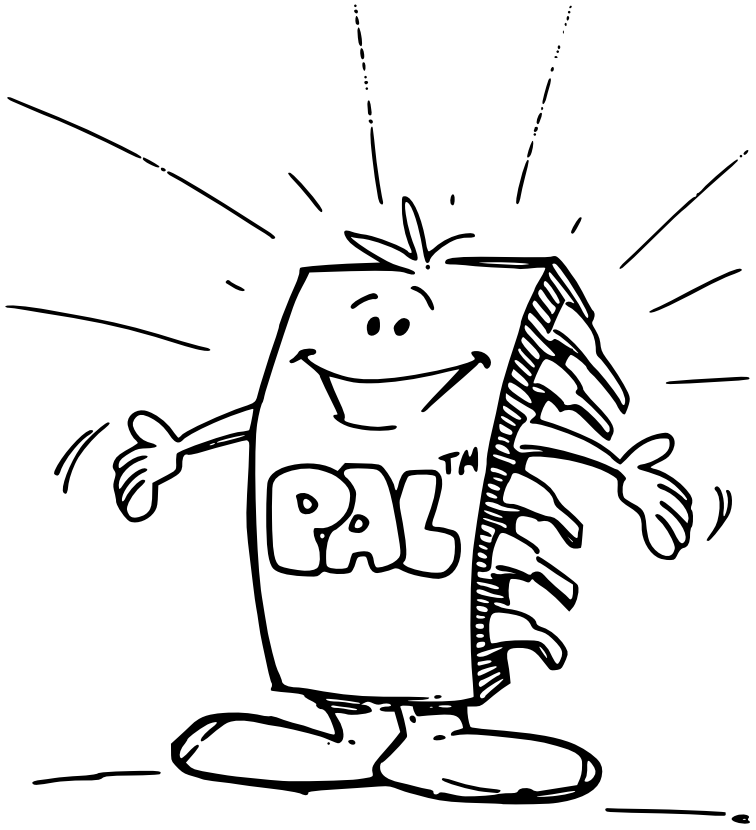


Programmable Logic Devices (PLC)

- **Programmable Array Logic (PAL)**
- Complex Programmable Logic Device (CPLD)
- Field-Programmable Gate Array (FPGA)
- Application-Specific Integrated Circuit (ASIC)
- Synthesis

PAL

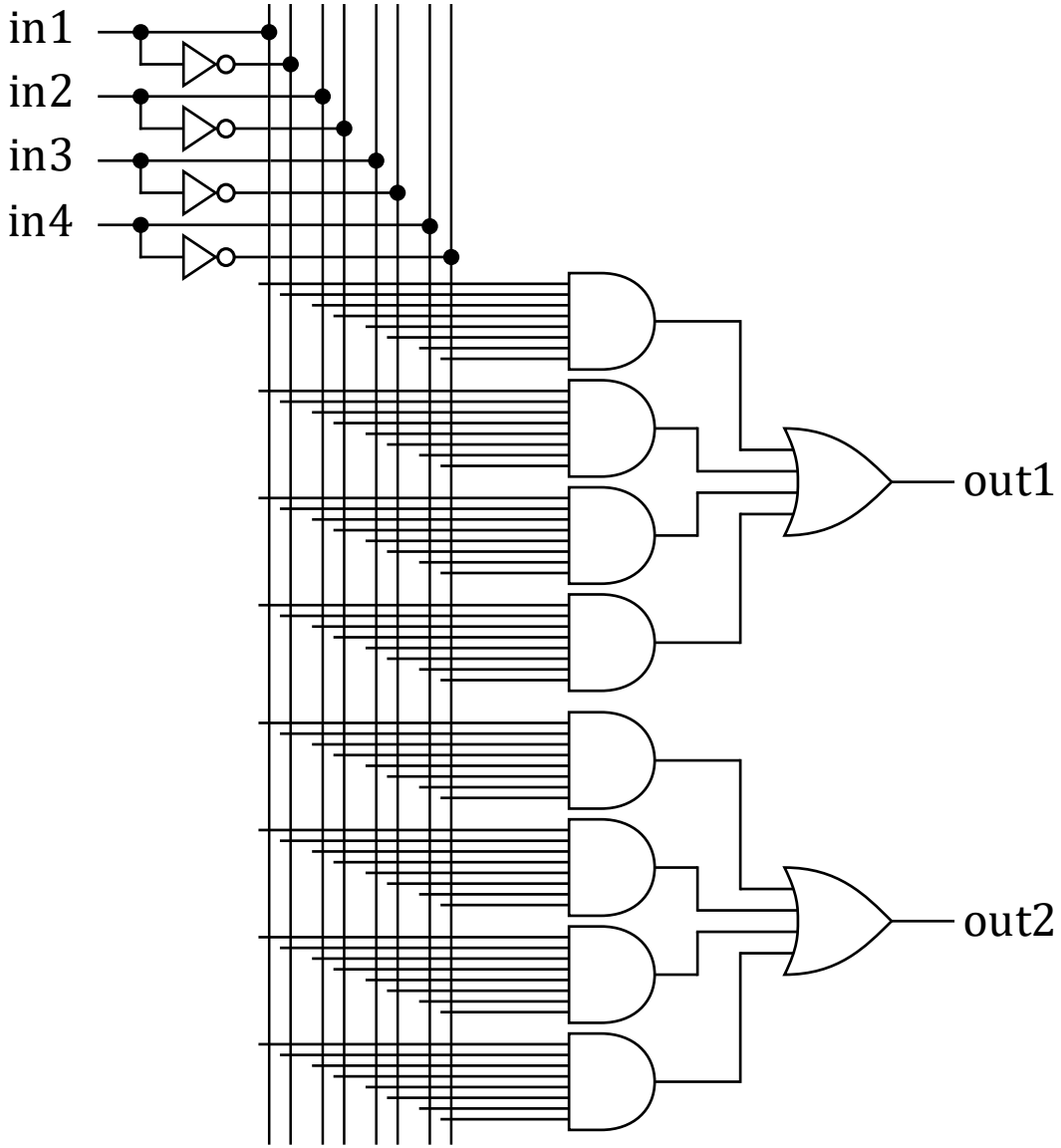
By Monolithic Memories, Inc. (MMI) 1980



PAL

Architecture

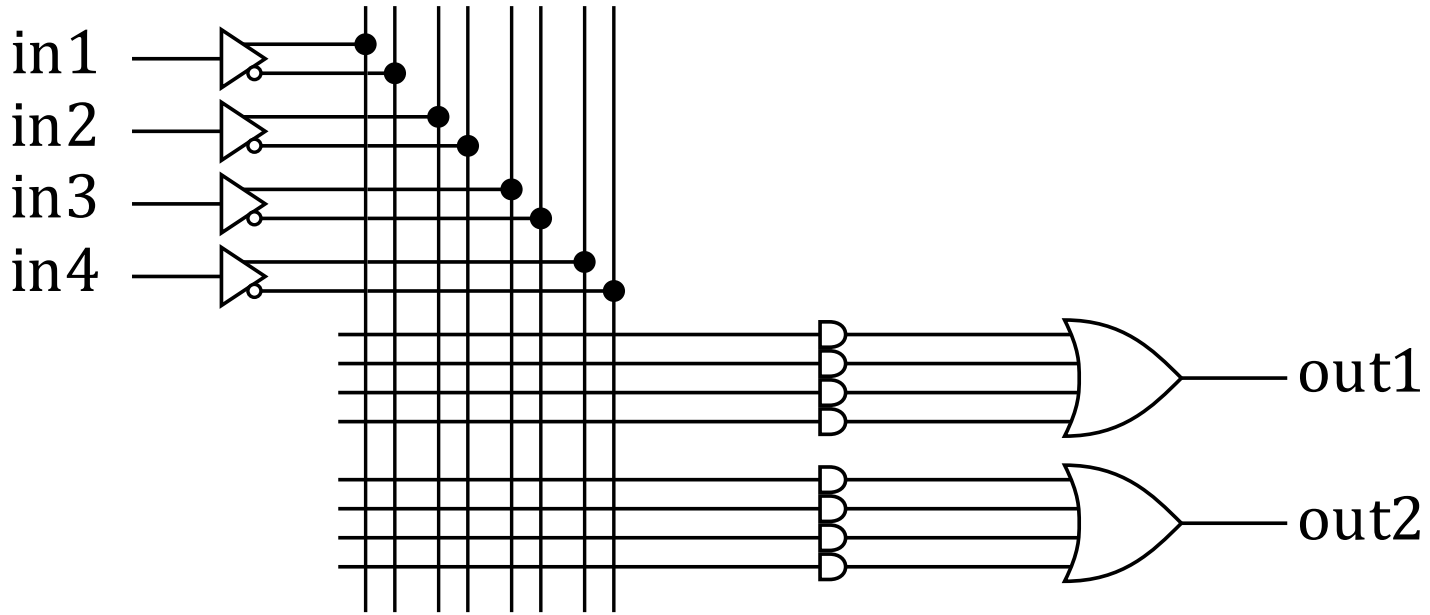
- Inverters
- Programmable AND gates
- Large OR gates



PAL

Drawing

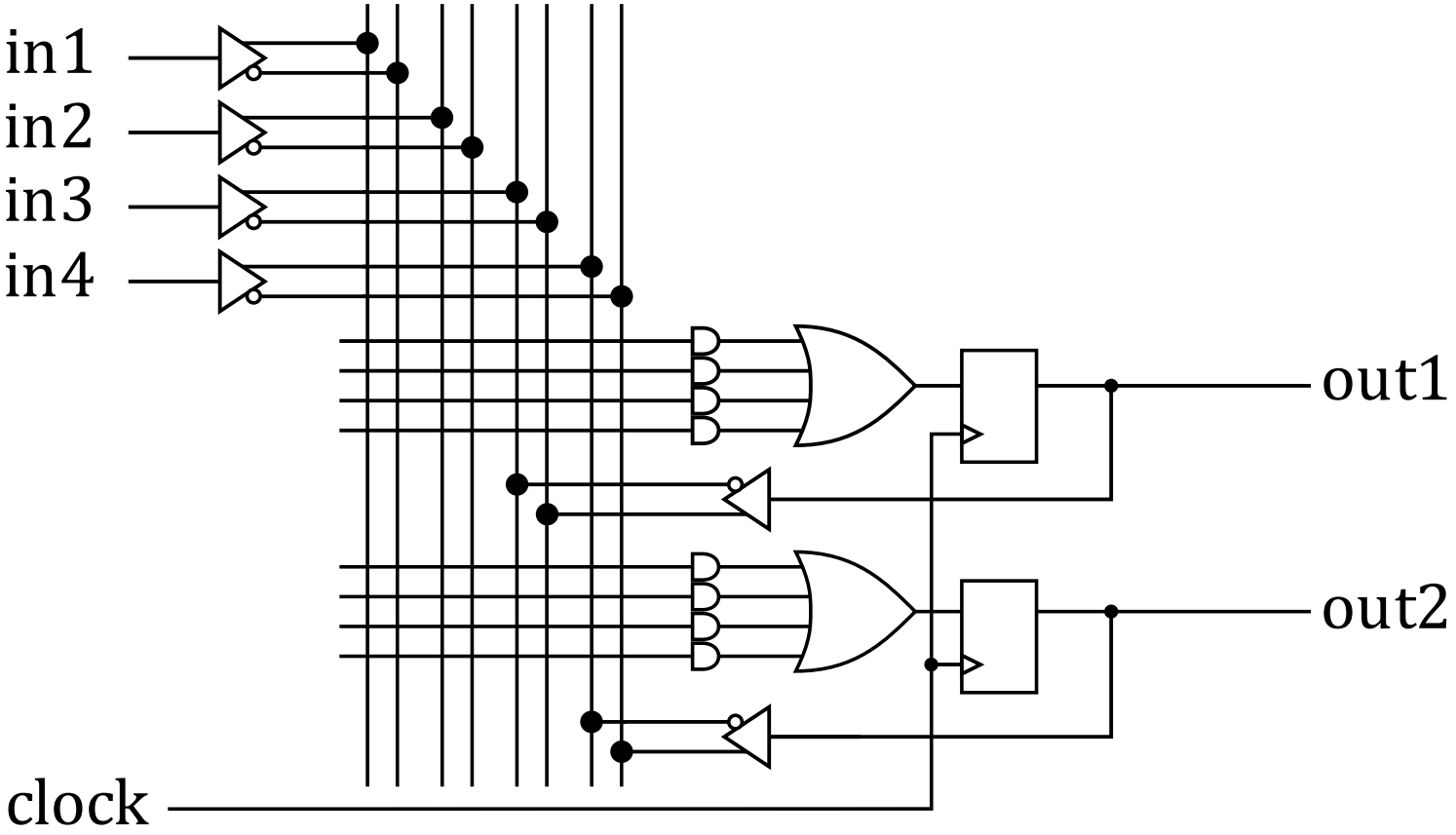
Drawing of circuit with large gates requires a more compact scheme



PAL

Architecture

Different output types: Low, Registered, …



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CPLD

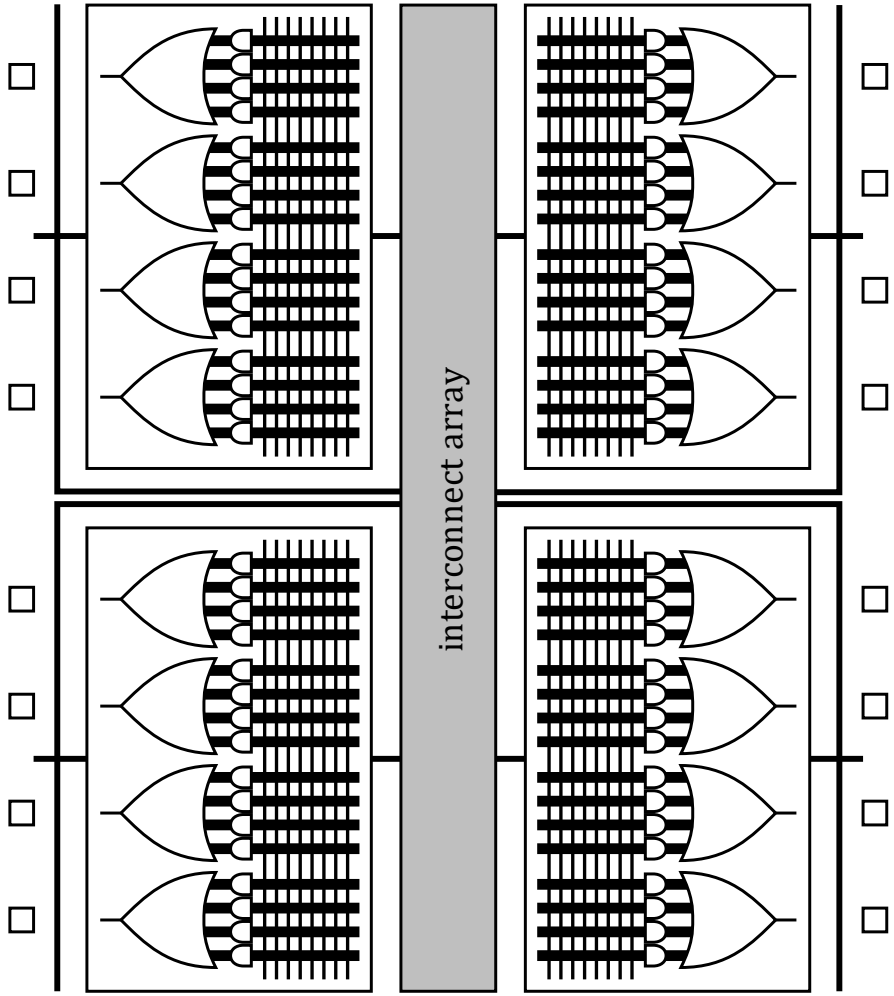
Usage

- Glue logic
- HDL (VHDL, Verilog)

CPLD

Architecture

- Several PALs on one chip
- Interconnect array
- Flipflops linked to I/O pins



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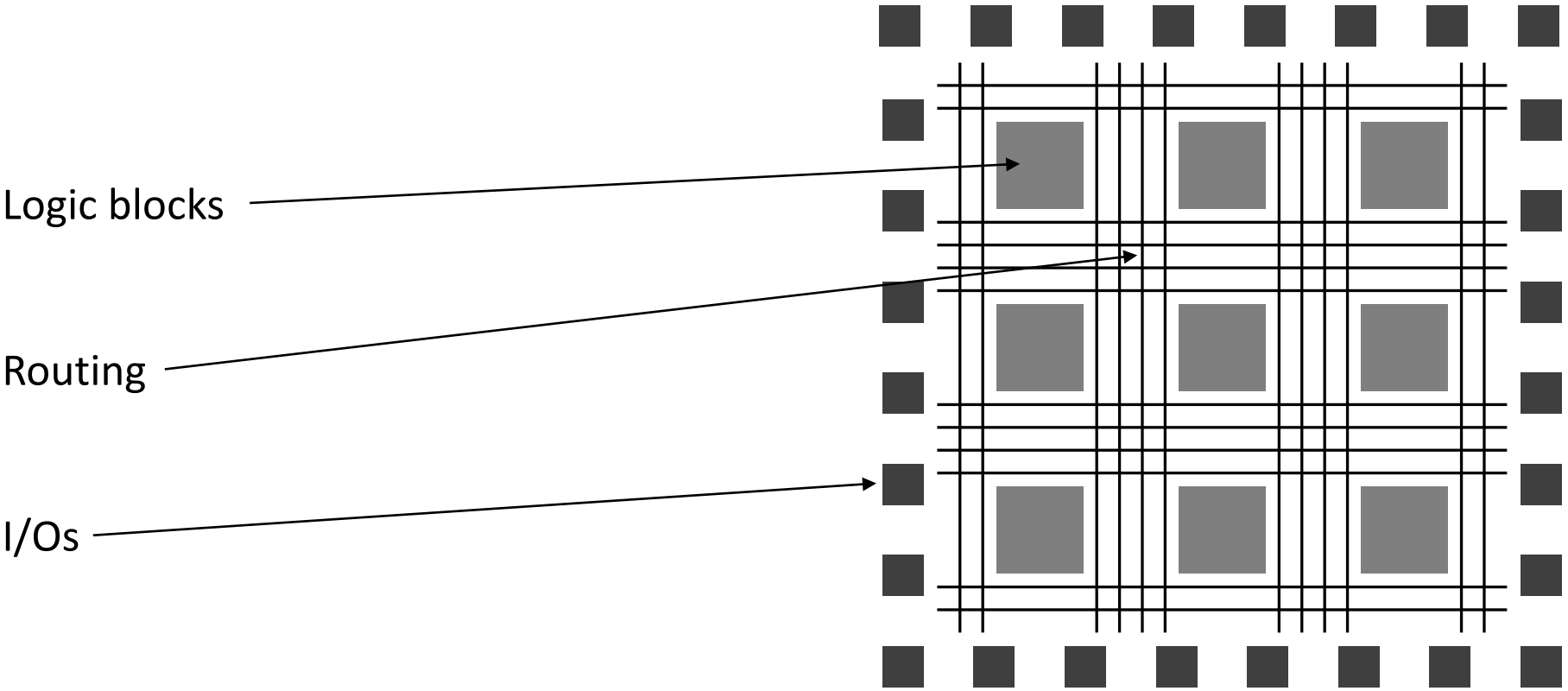
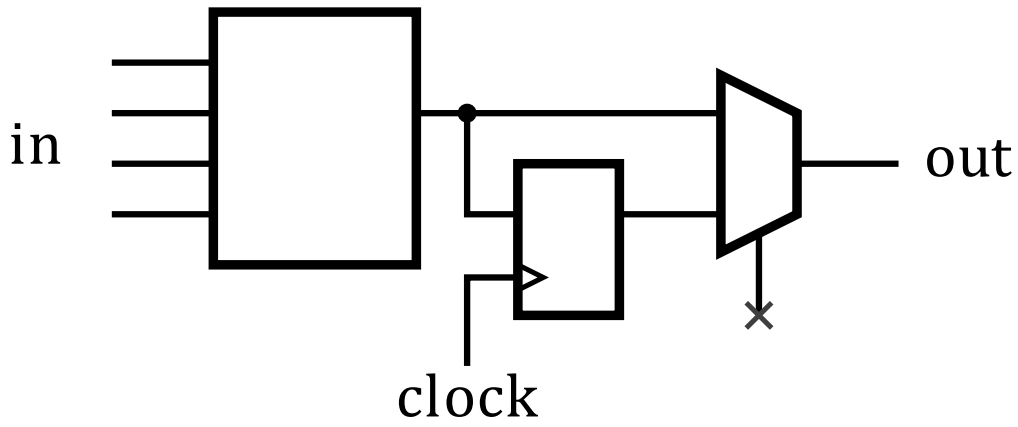
FPGA
Architecture



FPGA

Logic blocks

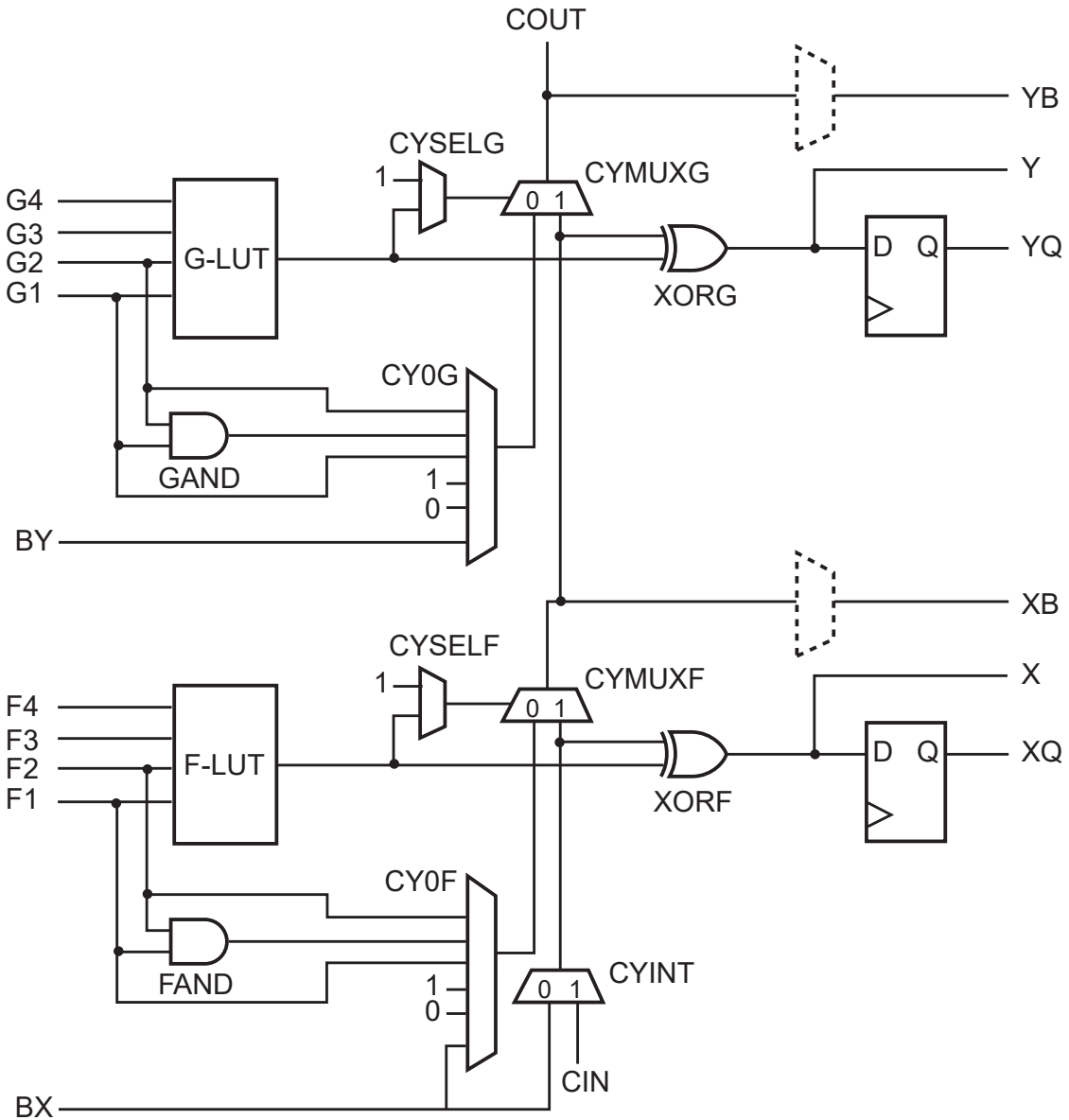
- Logic functions of typically 4 inputs
- Flipflop
- Configuration
- Plus special logic (carry, …)



FPGA

Logic blocks

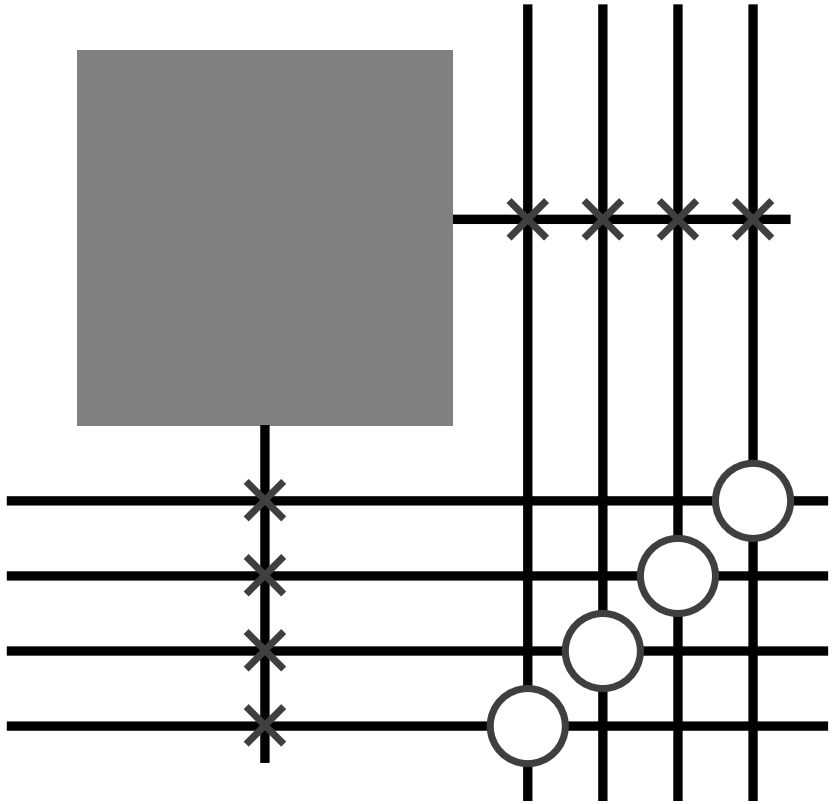
Xilinx Slice



FPGA

Routing

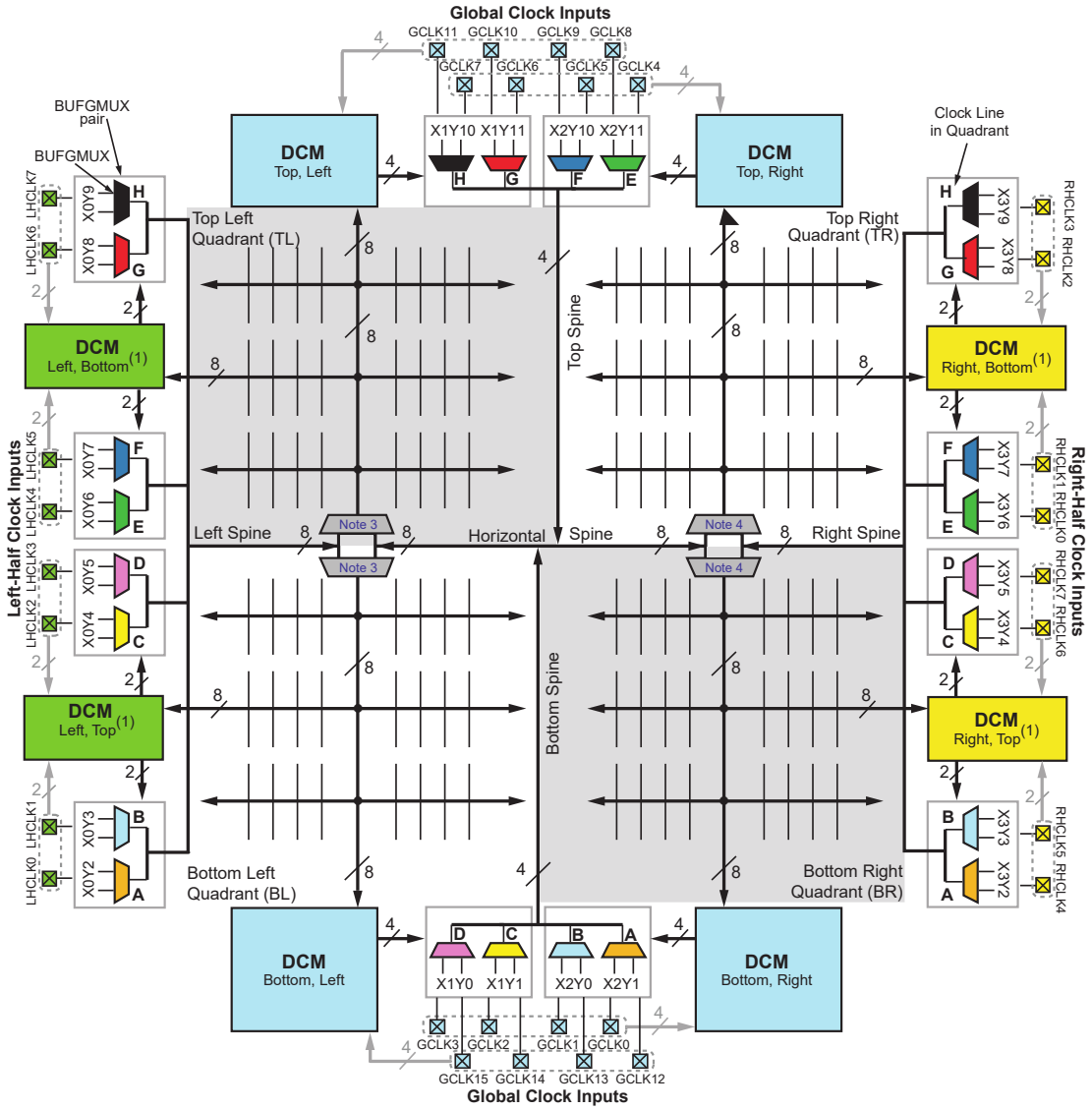
- Routing lines
- Short / long / tristate
- Logic block connect
- Cross-bar connections



FPGA

Clock tree

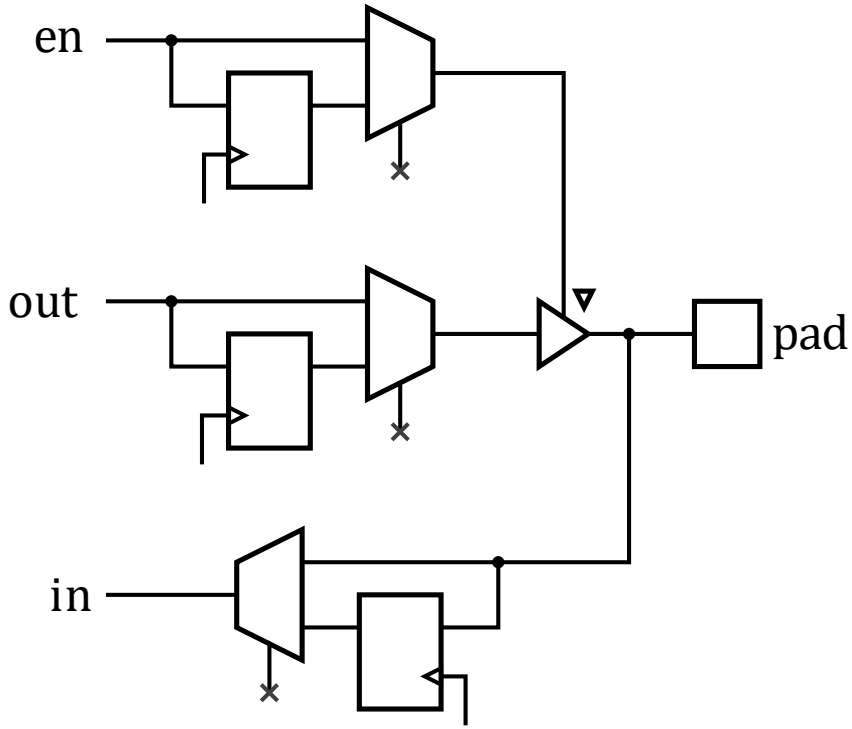
- Specific routing lines
- Full FPGA coverage / quartes
- Phase-Lockes Loops (PLLs)



FPGA

Input / Output block

- Input
- Output with tri-state
- Registers at I/O level
- Pull-up / down
- Bank-wise power supply

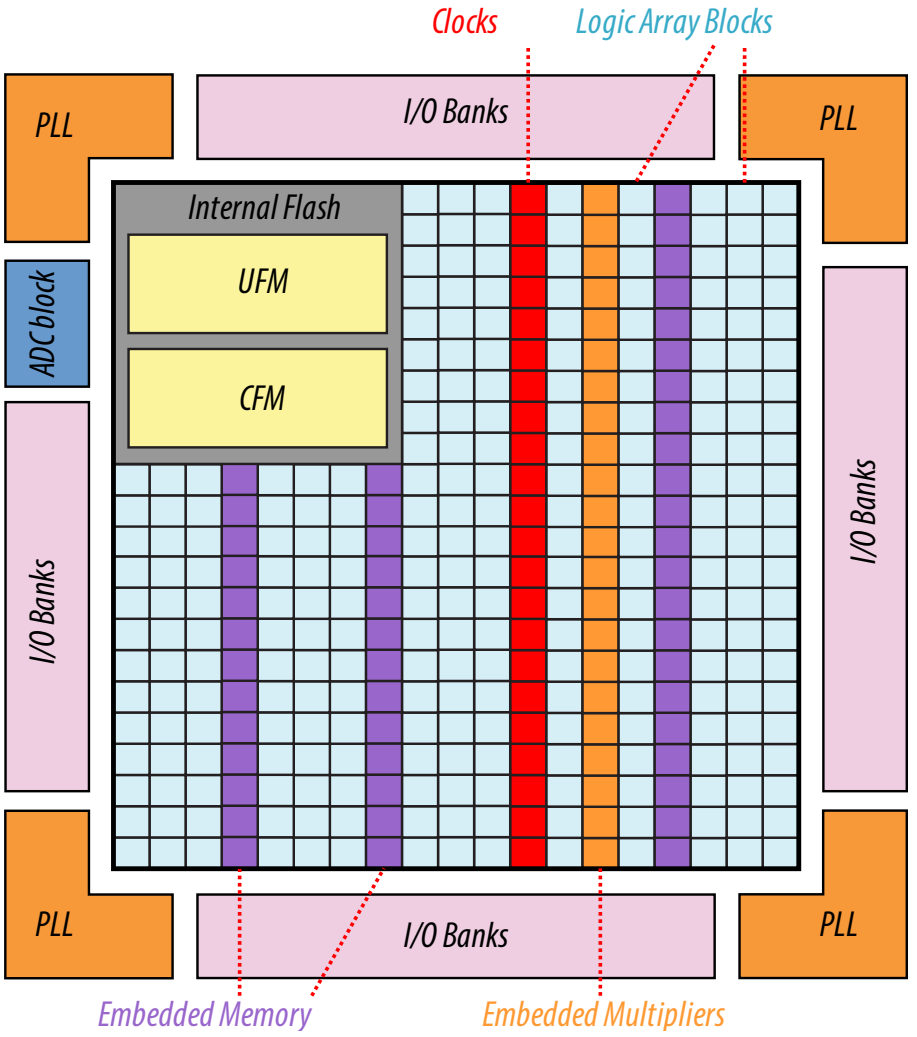


FPGA

Special functions

- RAM blocks
- Multipliers
- Microprocessors

Communication (USB, Ethernet)



FPGA

Usage

- Large circuits, up to microprocessor systems
- HDL (VHDL, Verilog)

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- Synthesis

Application-Specific Integrated Circuit (ASIC)

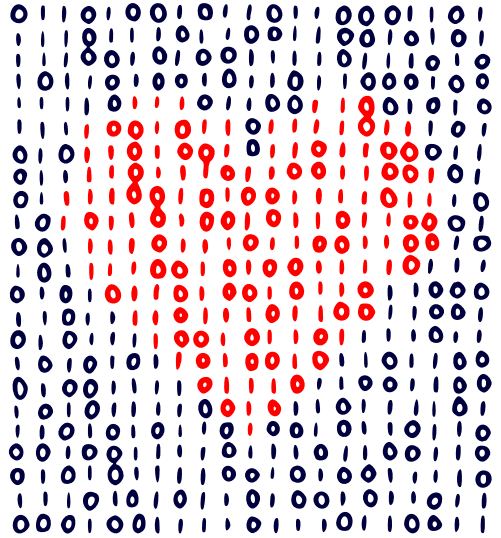
- Designed for a specific function
  - Ethernet bridge, USB hub, …
- Longer development cycle (layout, masks, …)
  - Requires very large quantities
- More compact circuit
  - Higher performance
  - Lower power consumption
- Can mix analog and digital

Synthesis

- VHDL (or Verilog) code generation from graphic views
- Constraints file (pin mapping, logic levels, speed, ...)
- Vendor-specific tool
  - Synthesis, place and route
  - Download

FPGA

- We now know everything about:
  - PAL's
  - CPLD's
  - FPGA's
  - ASIC's
  - Synthesis



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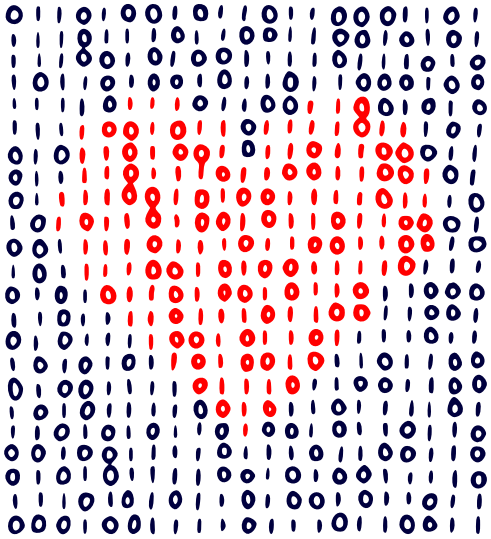


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