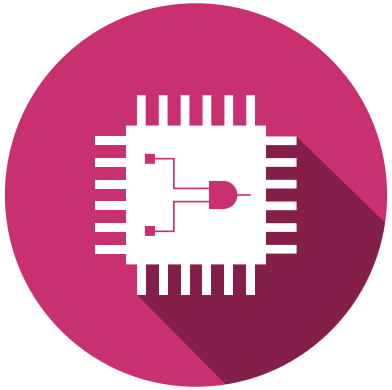
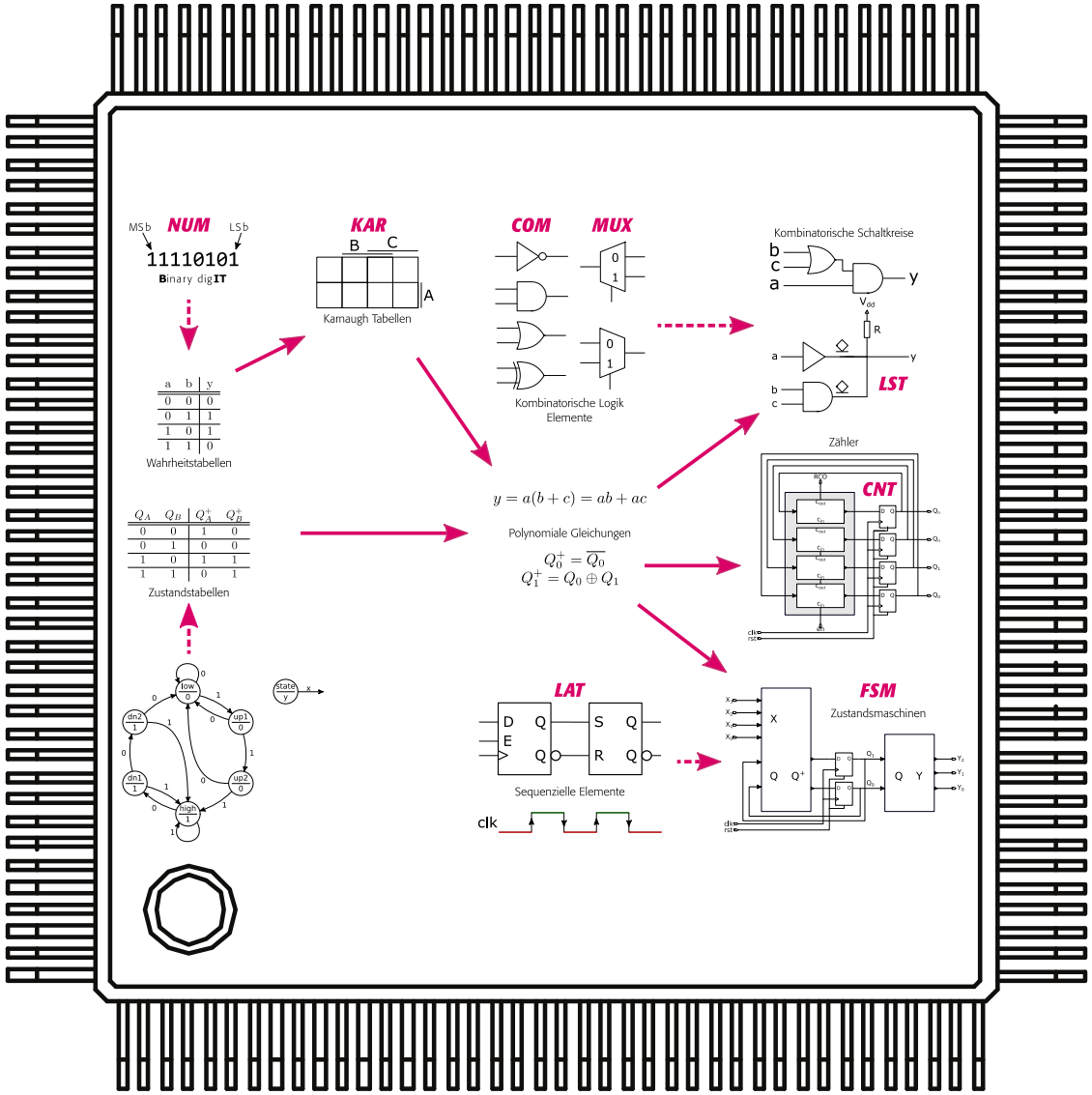
Field Programmable Gate Array
Course Embedded Systems (SEm)
FPGA

Silvan Zahno / François Corthay



Degree program Systems Engineering
Specialization Infotronics – Embedded Systems

Current content of the topic in the course



FPGA Introduction

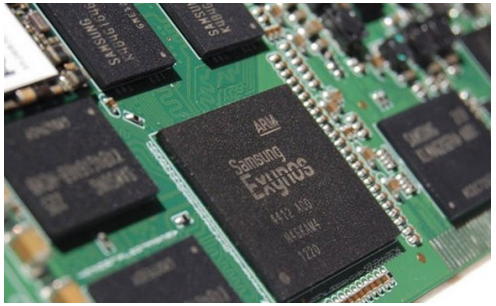
- **ASIC vs FPGA**

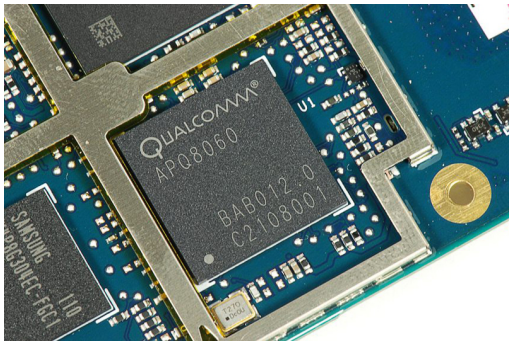
- FPGA
  - Packaging
  - Architecture
  - I/O Elements
  - Slice Elements
  - Logic Elements
  - Networks

- Design flow
  - Implementation
  - Generation
  - Synthesis
  - Place & Route
  - Programming

ASIC vs FPGA Differences

- ASIC – **A**pplication **S**pecific **I**ntegrated **C**ircuit





- FPGA – **F**ield **P**rogrammable **G**ate **A**rray

Actel®

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intel FPGA Design Solutions Network

ASIC vs FPGA Differences

- ASIC – **A**pplication **S**pecific **I**ntegrated **C**ircuit
  - From the behavior description to the physical layout
  - Designs must be sent to a semiconductor factory for costly and time-consuming production

- FPGA – **F**ield **P**rogrammable **G**ate **A**rray
  - A physical layout ends with a bitstream that is used to configure a device.
  - Purchased on the market and reconfigured by the designers themselves.

ASIC vs FPGA Advantages

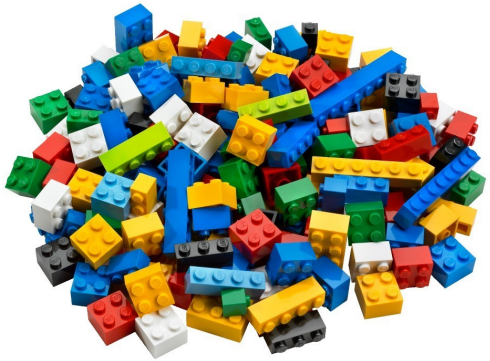
- ASIC – **A**pplication **S**pecific **I**ntegrated **C**ircuit
  - High efficiency
  - Low power consumption
  - Low cost with high volume

- FPGA – **F**ield **P**rogrammable **G**ate **A**rray
  - Commercial standard product
  - Low development costs
  - Short time to market
  - Reconfigurability

ASIC vs FPGA Advantages

- ASIC – **A**pplication **S**pecific **I**ntegrated **C**ircuit

- FPGA – **F**ield **P**rogrammable **G**ate **A**rray



FPGA Introduction

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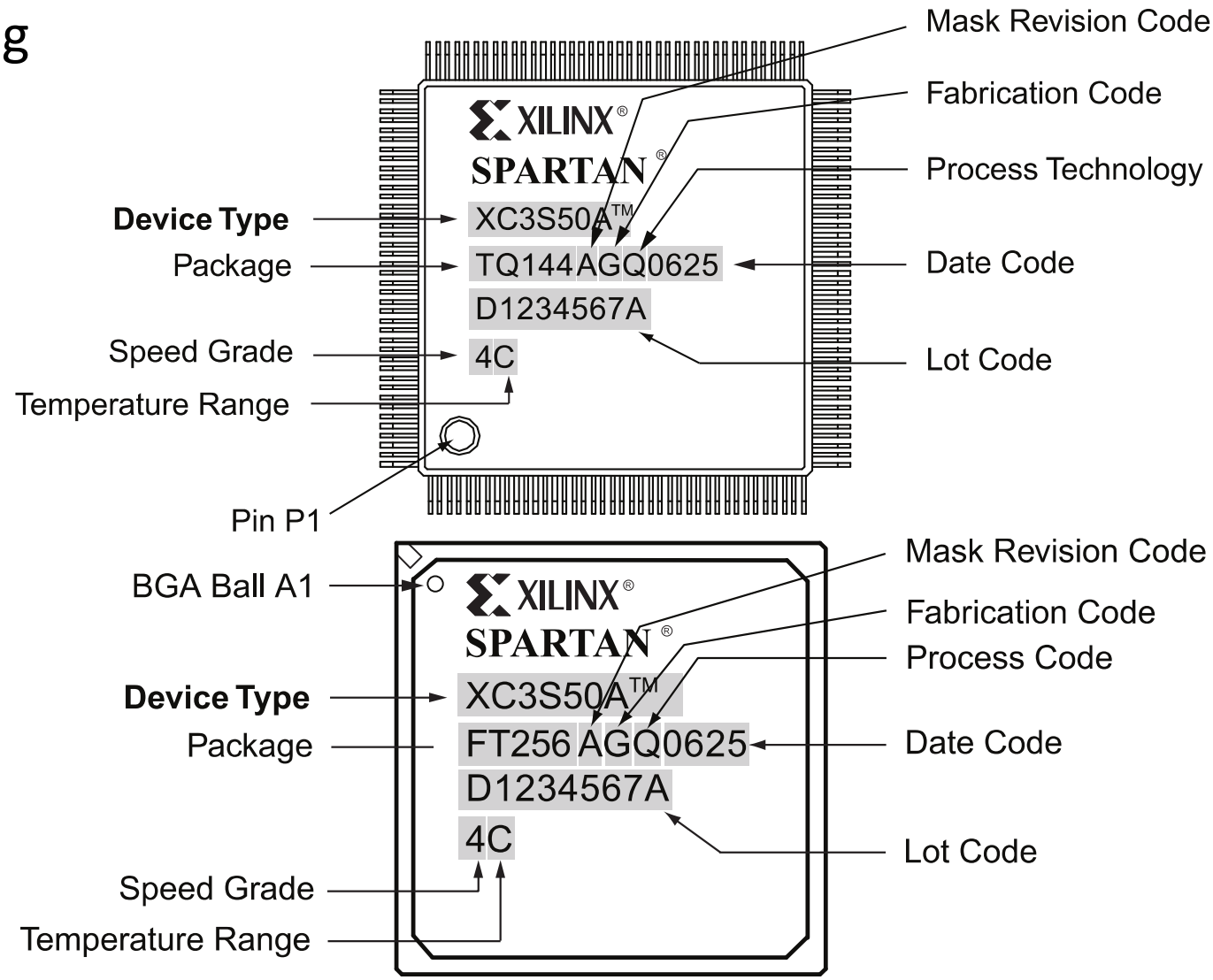
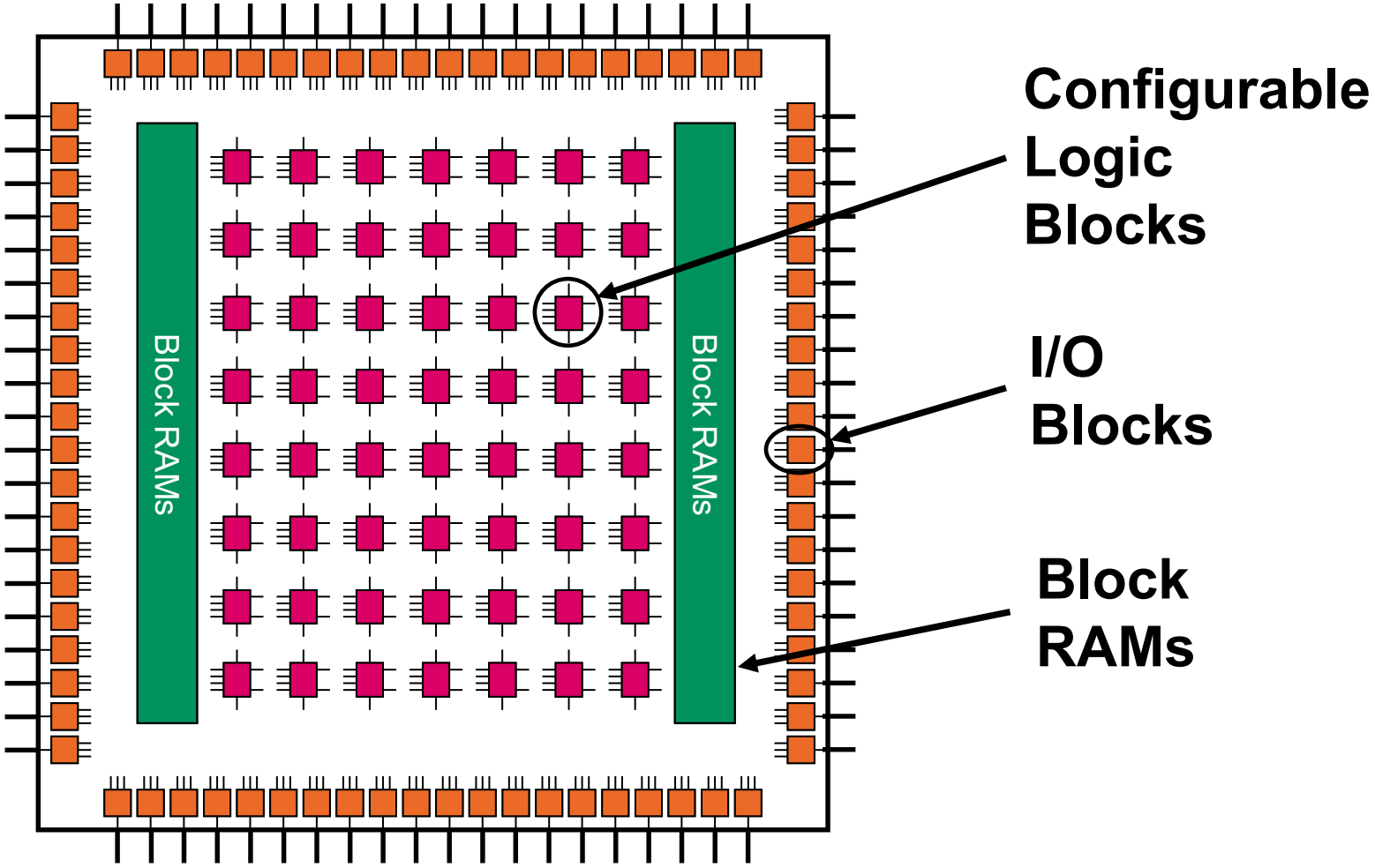
FPGA

Packaging



FPGA

Architecture



FPGA

Architecture

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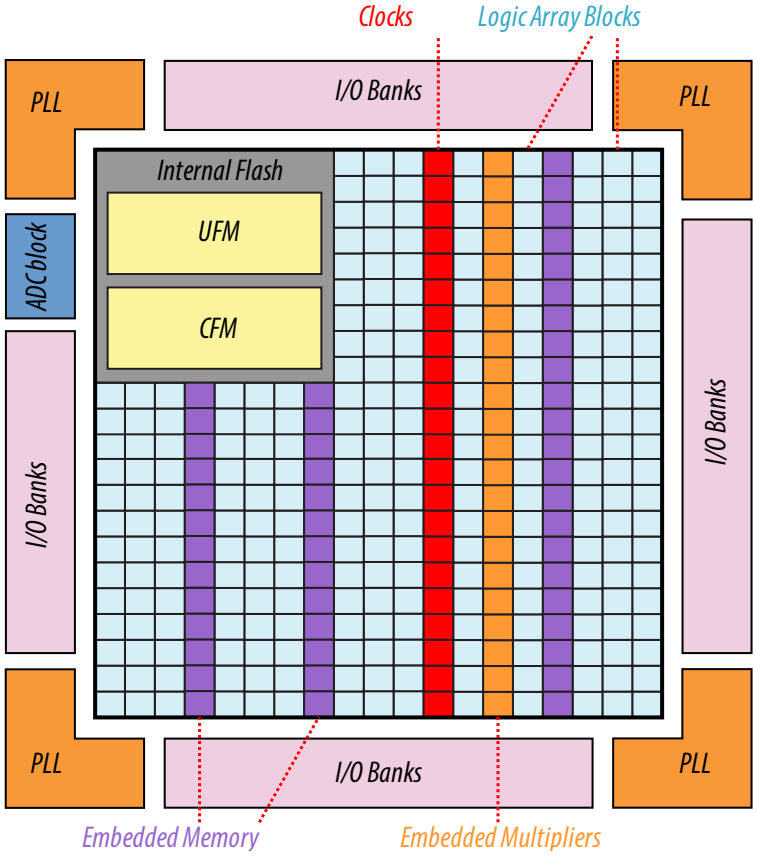
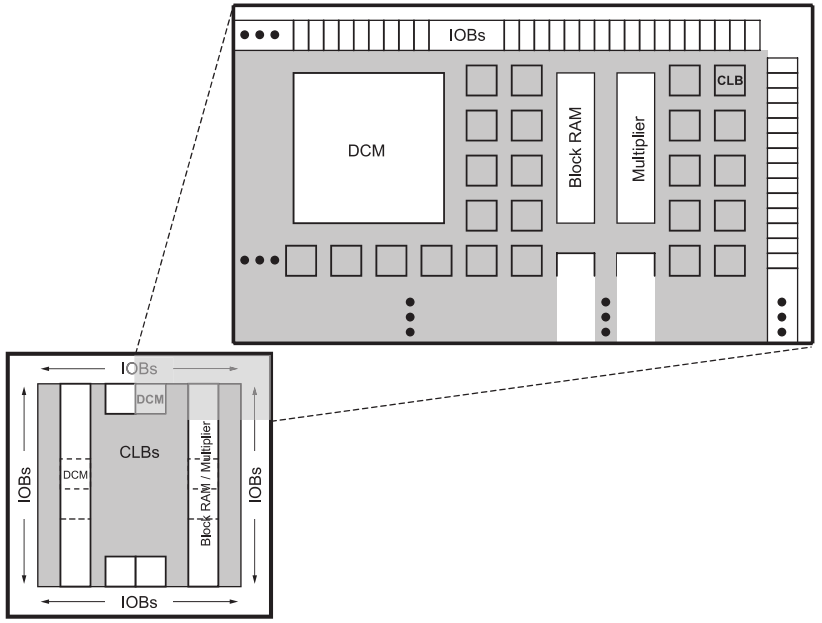
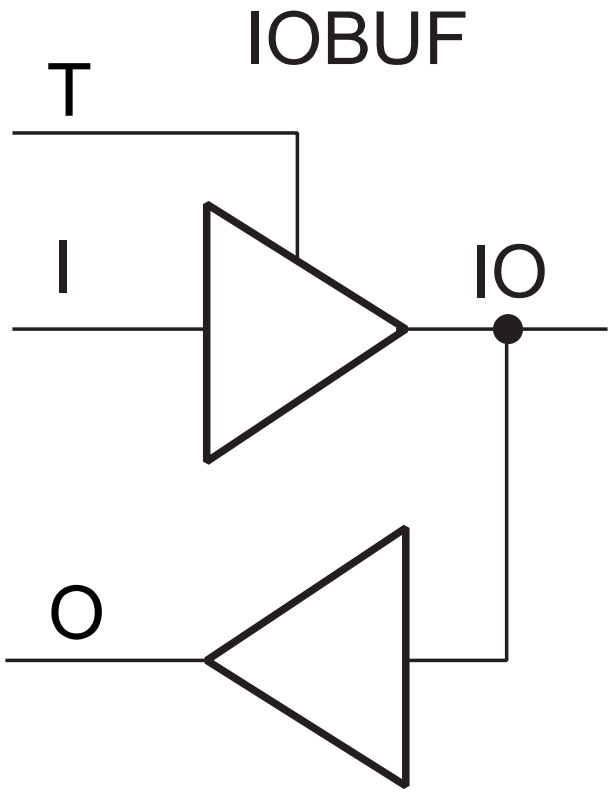
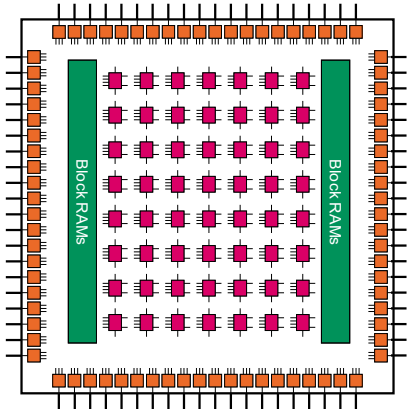


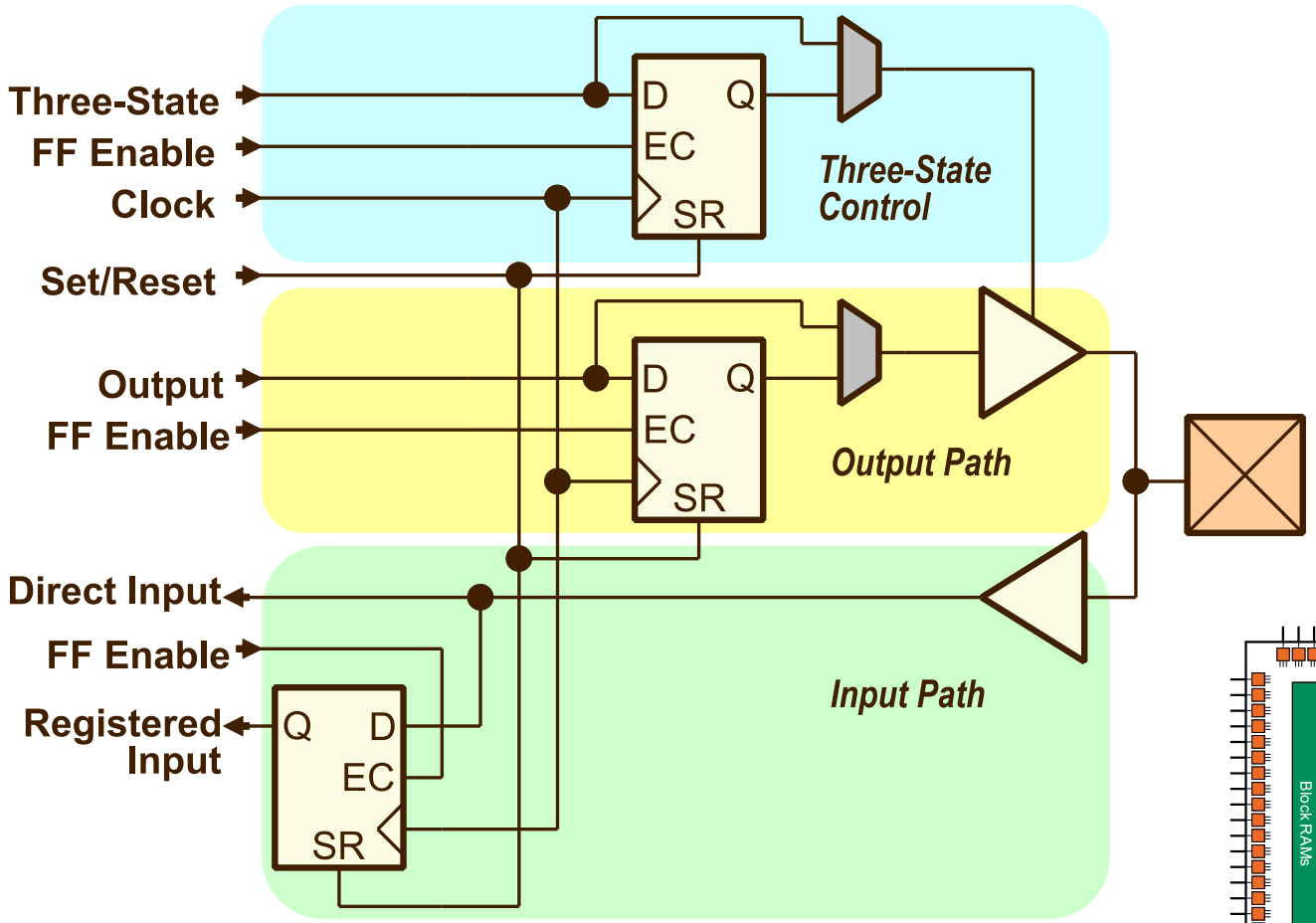


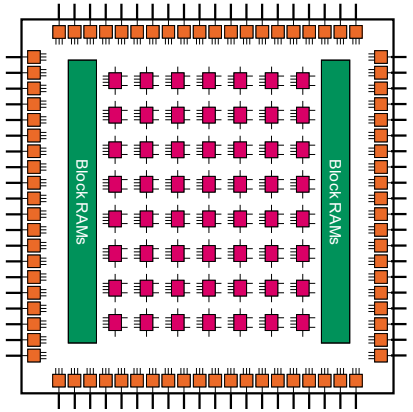
FPGA
I/O Elements





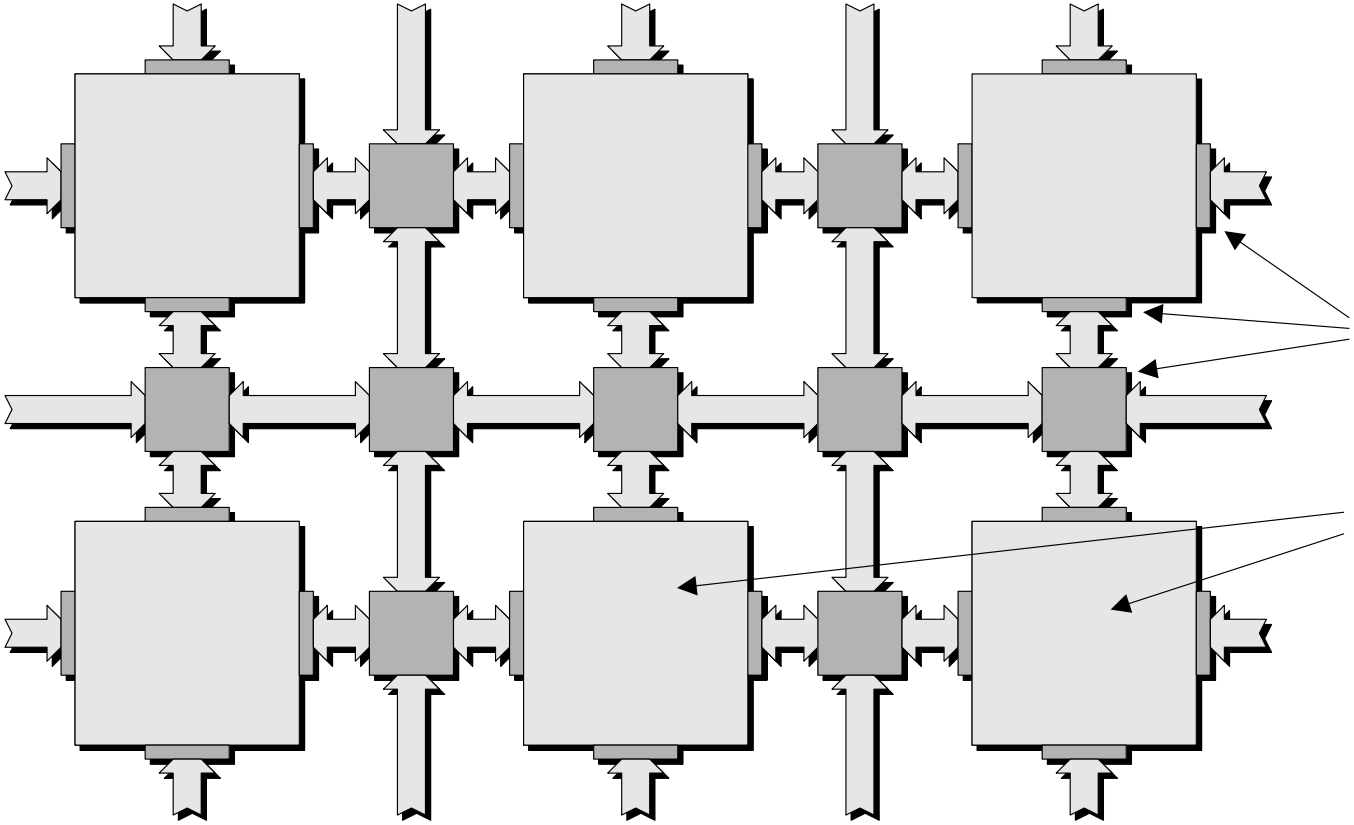
FPGA
I/O Elements





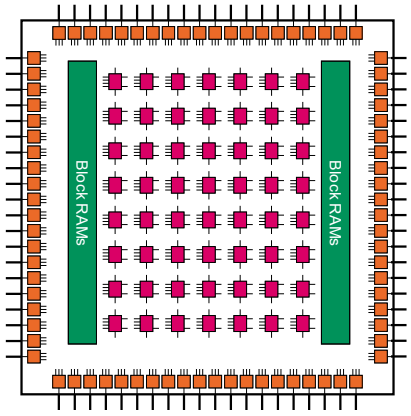
FPGA

Slice Elements



Programmable interconnect

Programmable logic blocks



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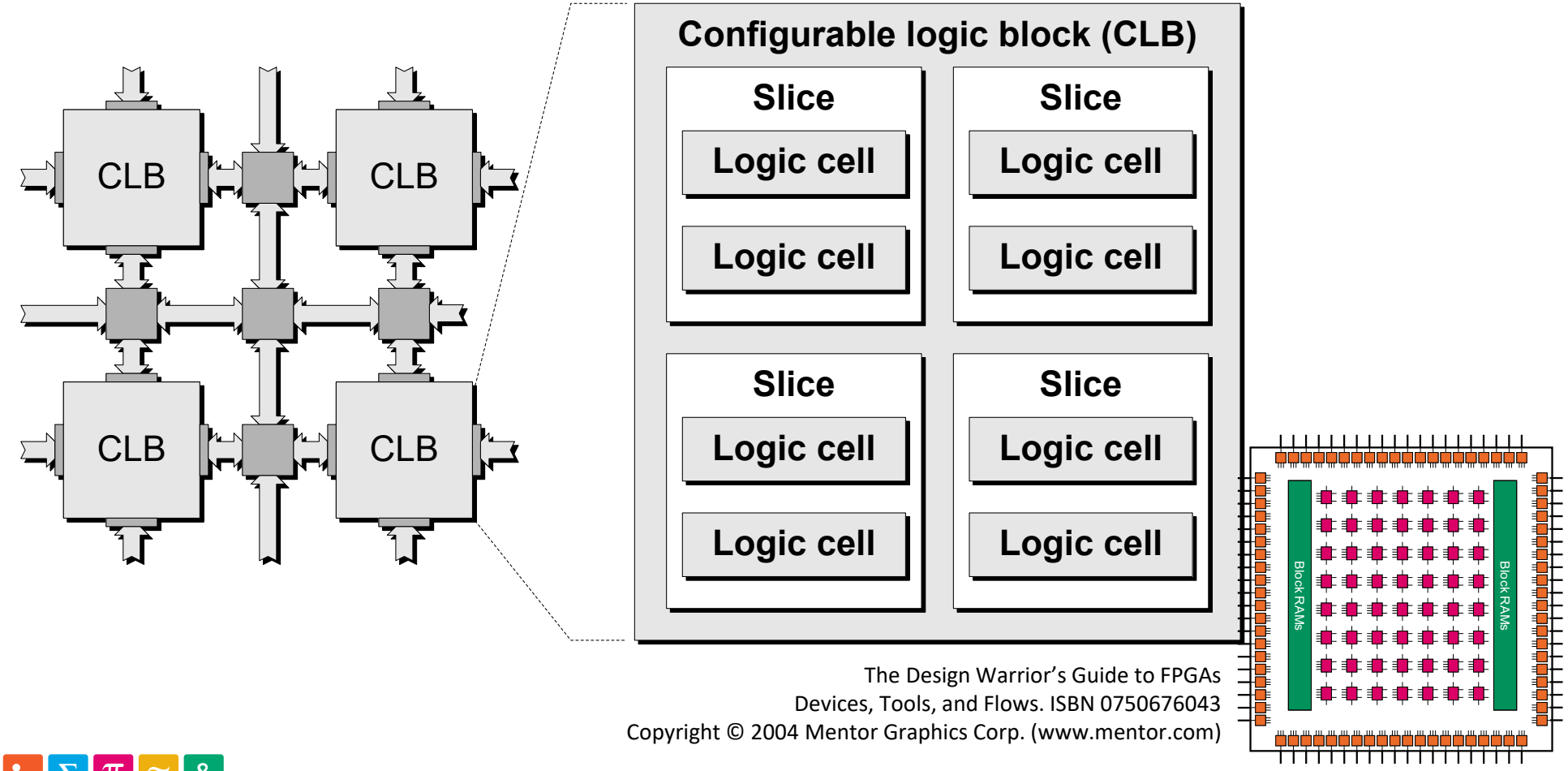
FPGA

Slice Elements



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FPGA

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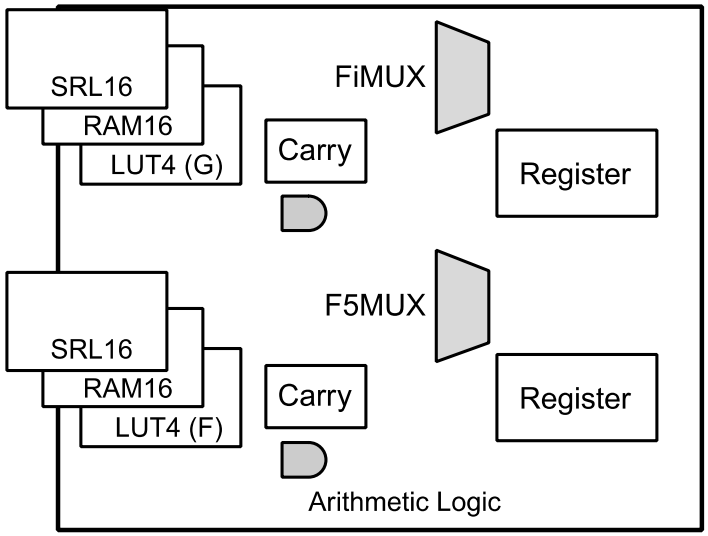

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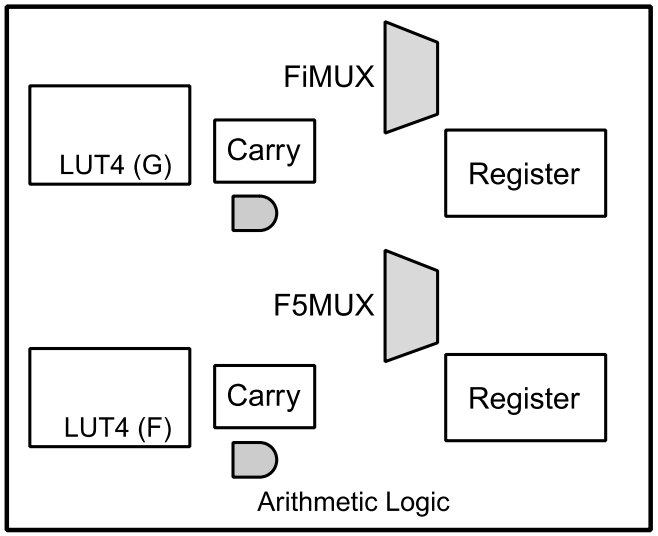

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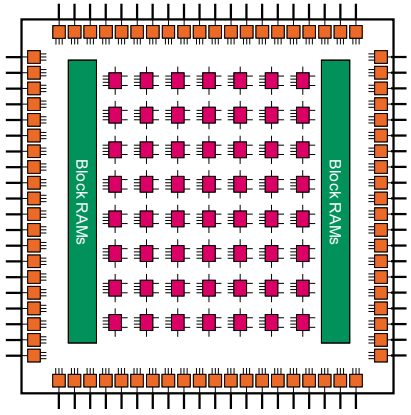

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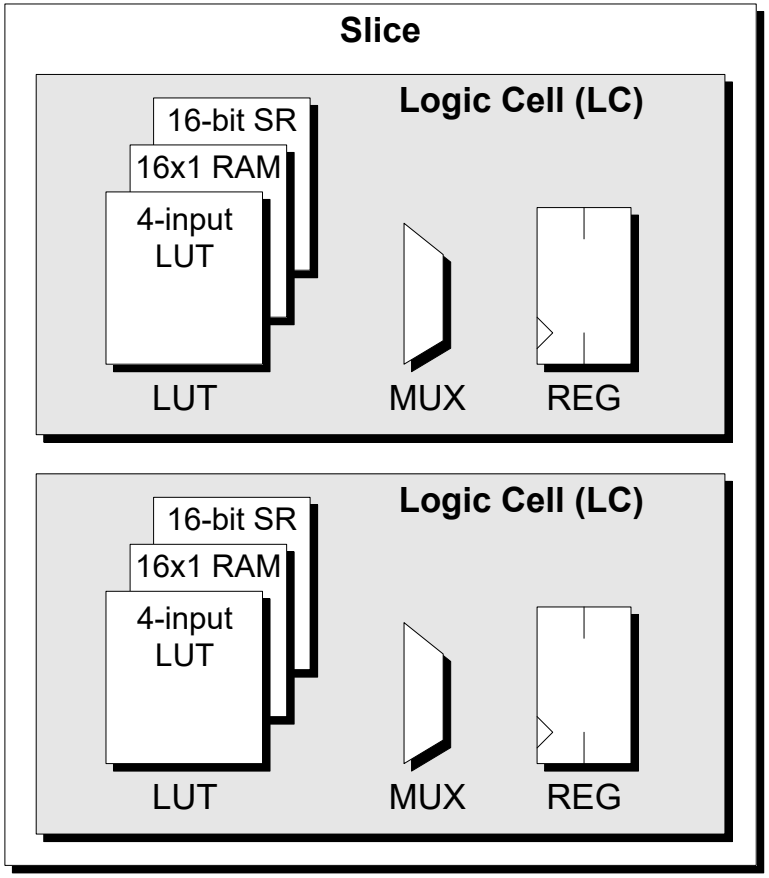
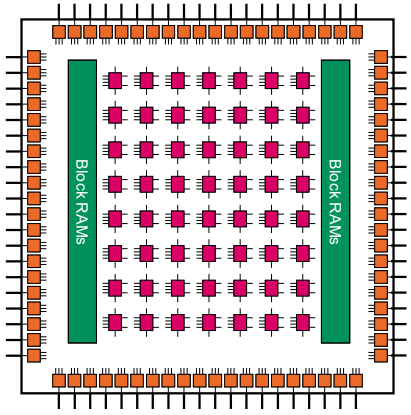
FPGA
Slice Elements





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FPGA

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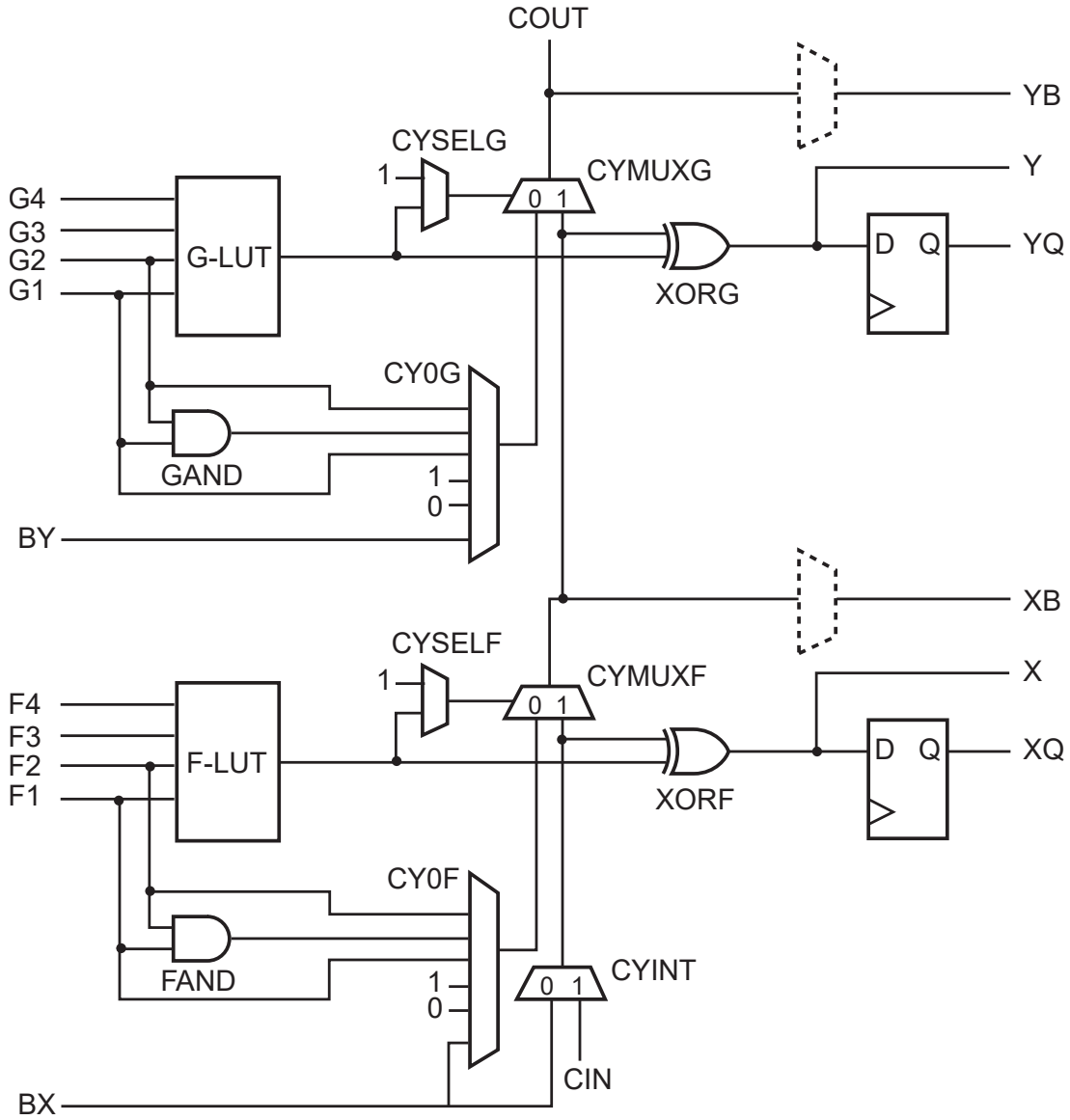
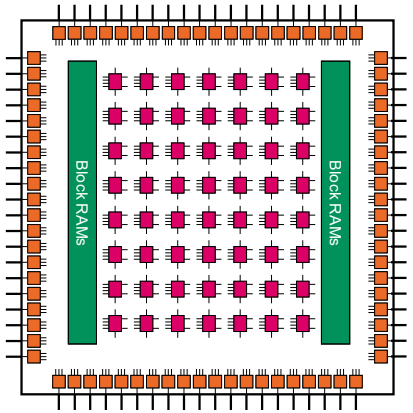
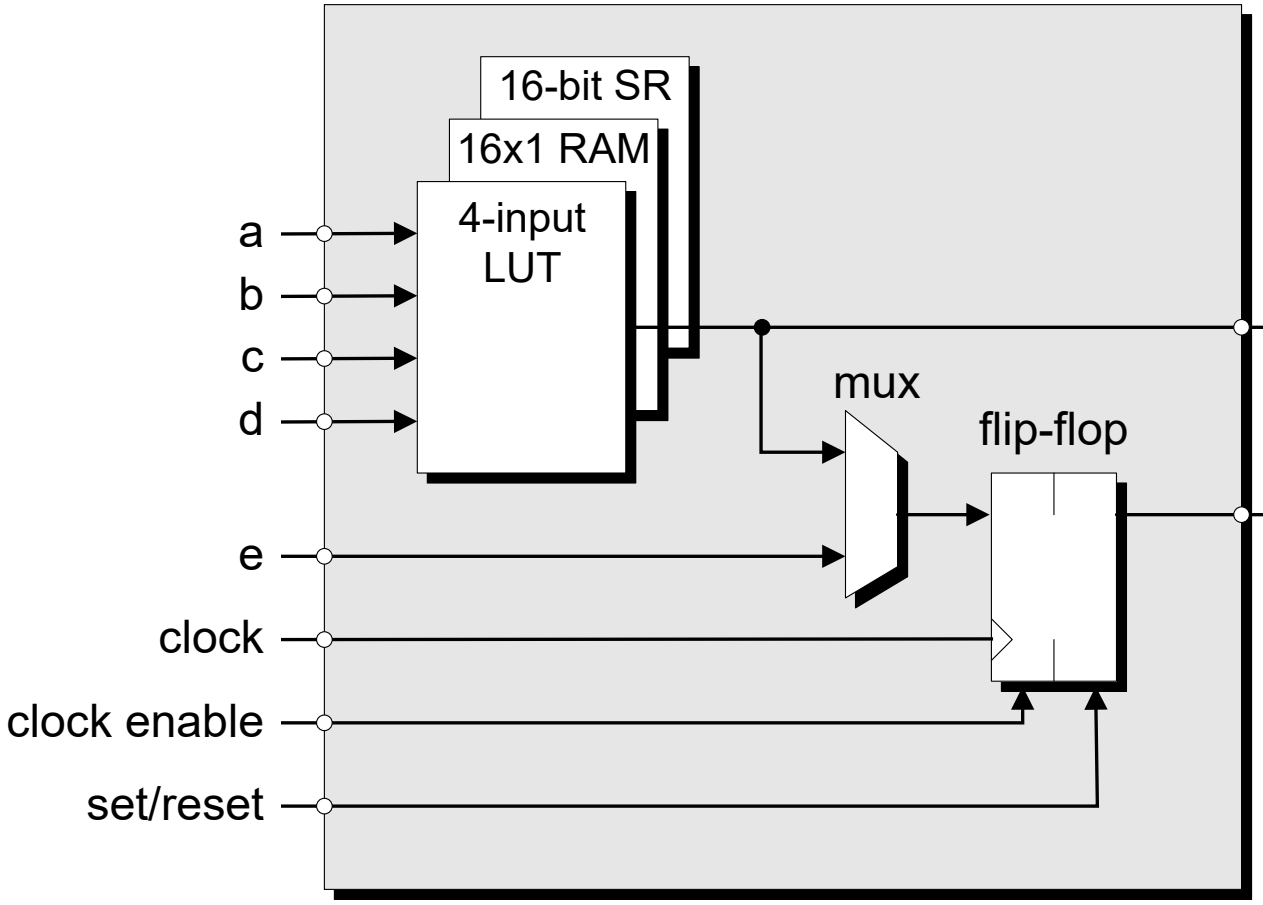
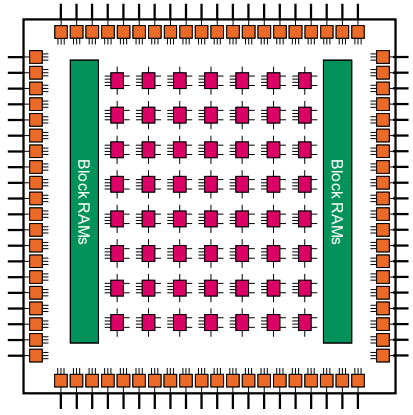




FPGA

Logic Elements





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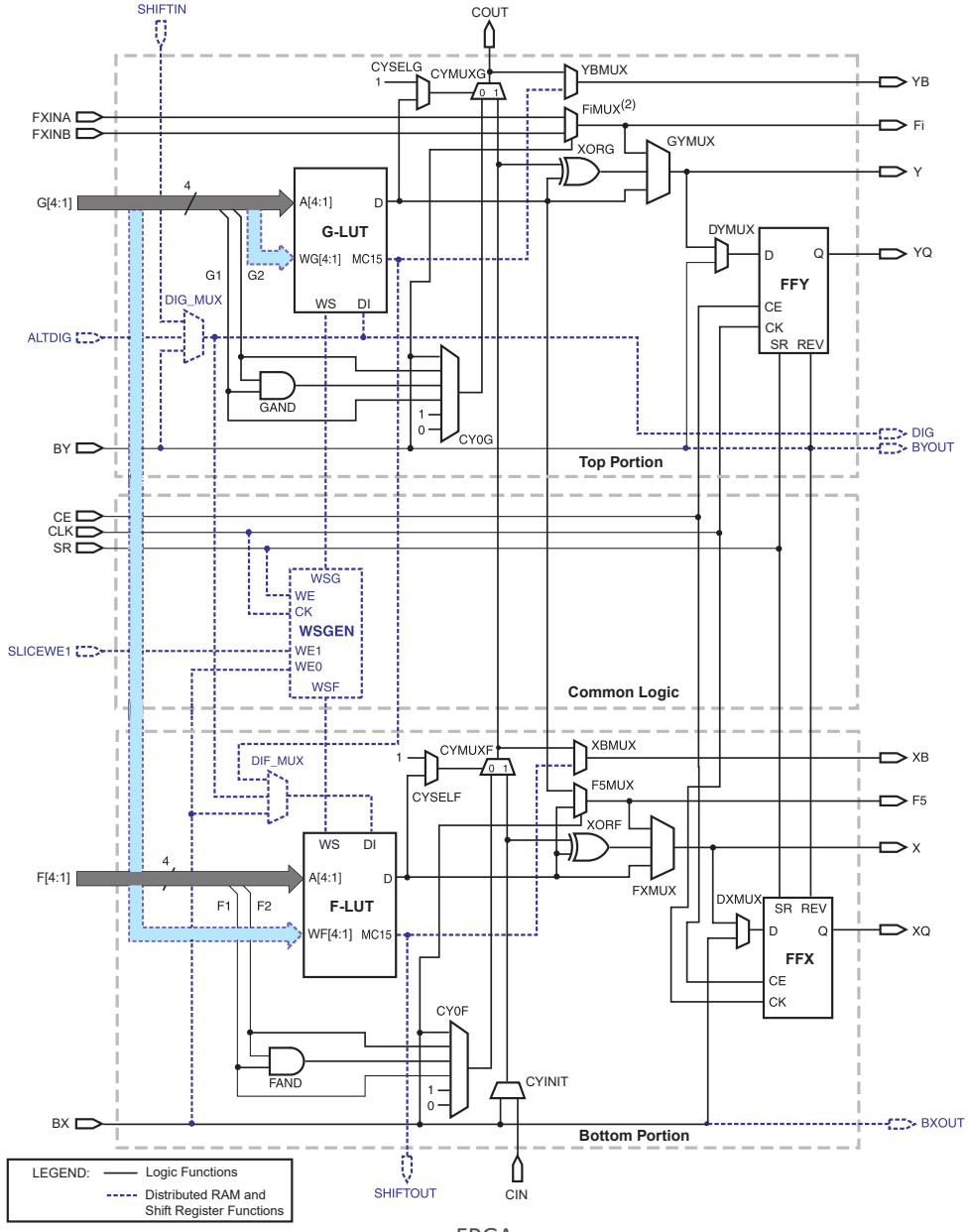
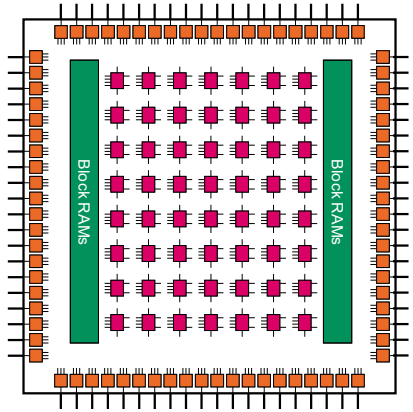
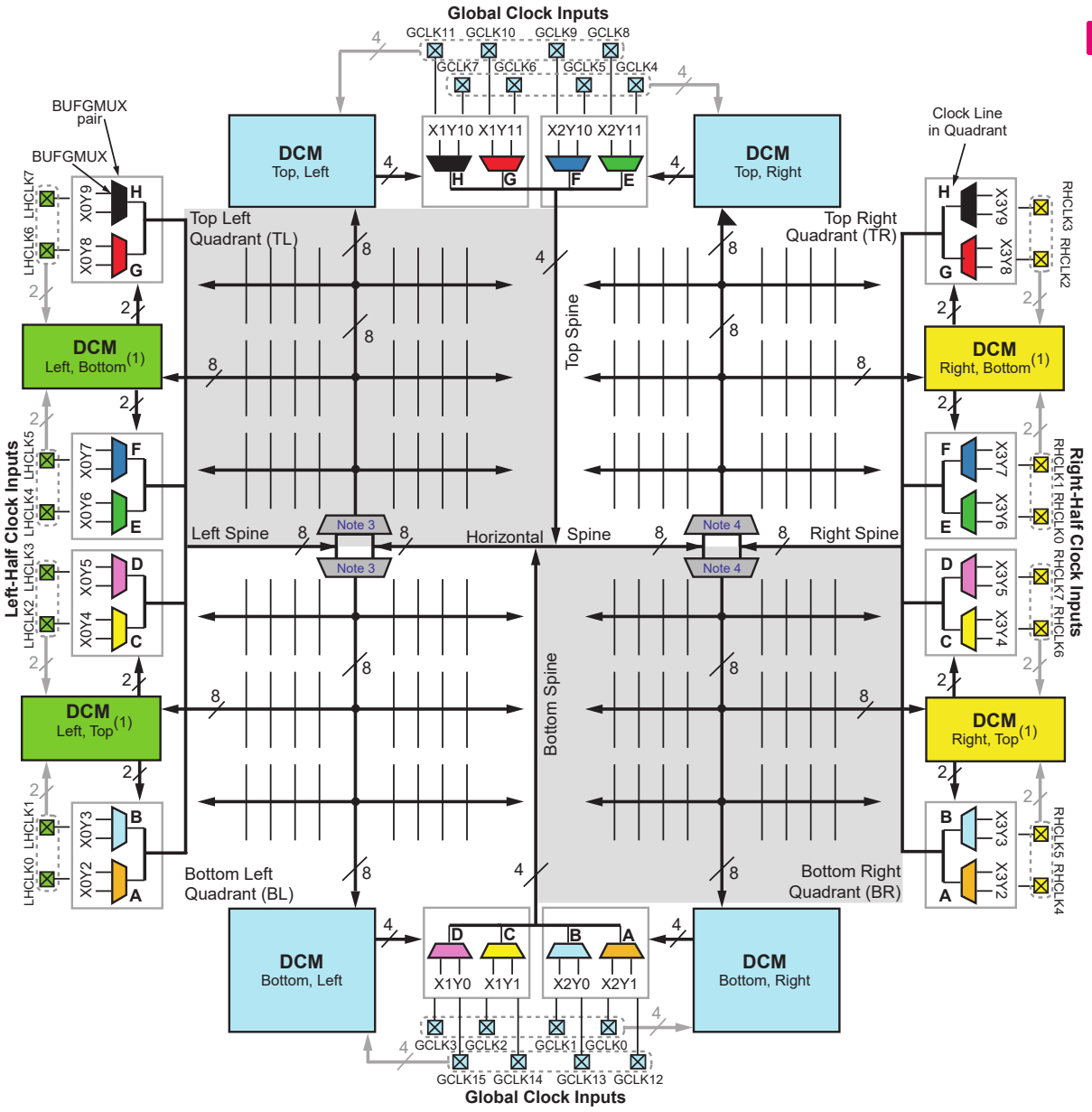
FPGA
Logic Elements





FPGA
Networks



FPGA Introduction

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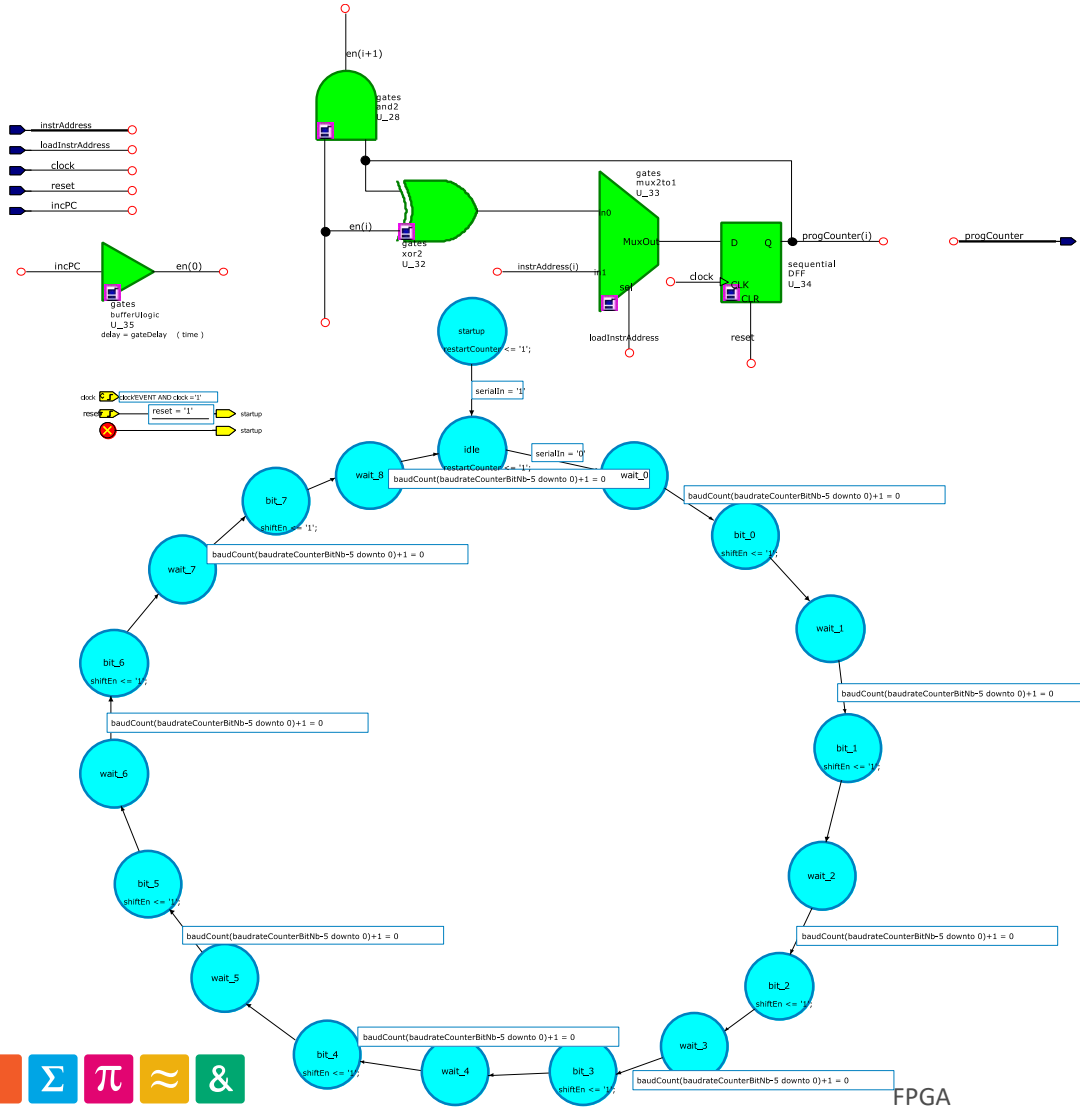
  - Programming

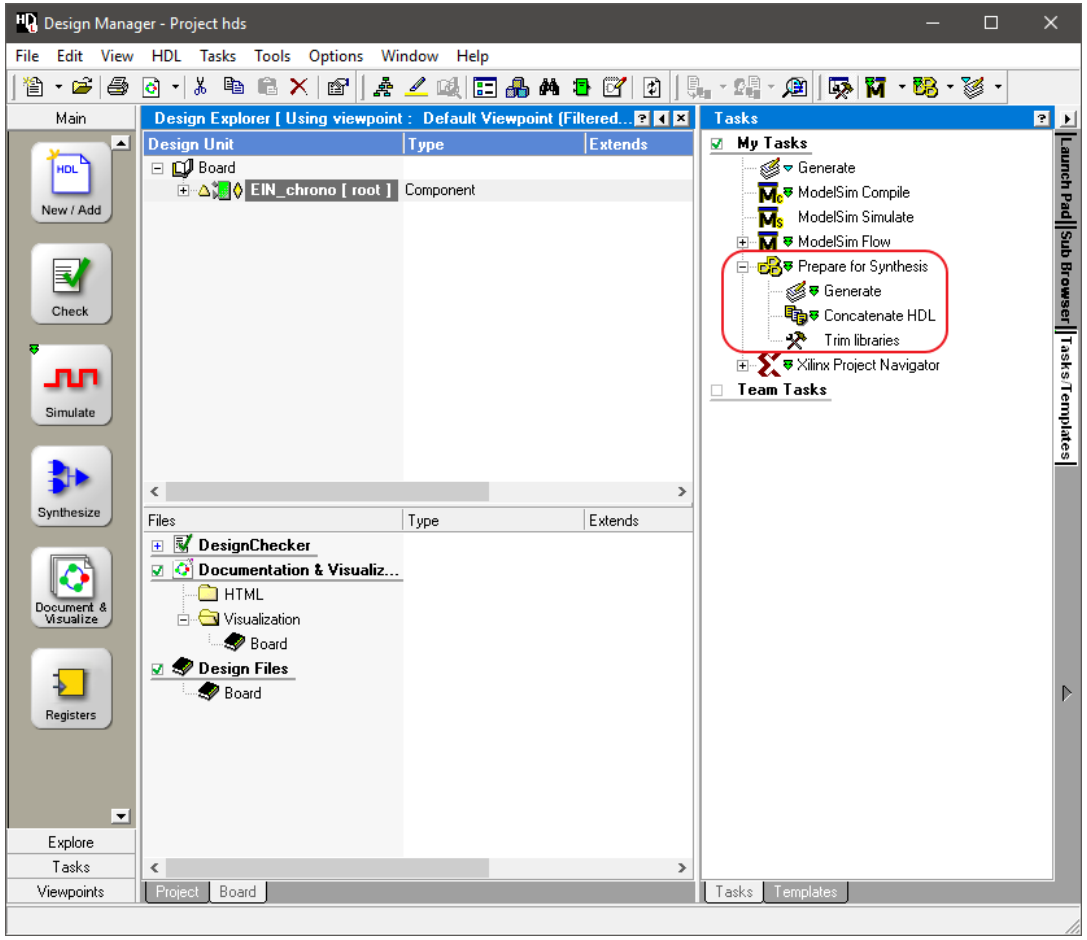
Design Flow
Implementation

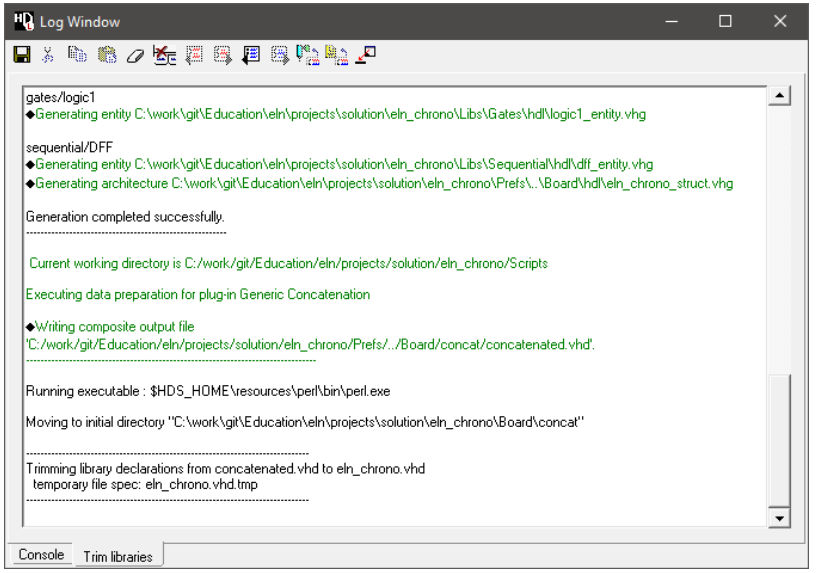



```
LIBRARY ieee;
  USE ieee.std_logic_1164.all;
  USE ieee.NUMERIC_STD.all;

ENTITY audioAmp_FPGA IS
   GENERIC(
      gainBitNb   positive := 8

   PORT(
      ADC_bClk          IN     std_logic;
      ADC_data          IN     std_logic;
      ADC_lrck          IN     std_logic;
      ADC_ovf_l         IN     std_logic;
      ADC_ovf_r         IN     std_logic;
      DAC_zero          IN     std_logic;
      clock             IN     std_ulogic;
      functionSelect    IN     std_logic;
      gain_n            IN     unsigned (gainBitNb-1 DOWNTO 0);
      reset_n           IN     std_ulogic;
      ADC_DAC_rst_n     OUT    std_logic;
      ADC_bypass        OUT    std_logic;
      ADC_osr           OUT    std_ulogic_vector (2 DOWNTO 0);
      ADC_sClk          OUT    std_logic;
      DAC_bclk          OUT    std_logic;
      DAC_data          OUT    std_logic;
      DAC_lrck          OUT    std_logic;
      DAC_mute          OUT    std_logic;
      DAC_sclk          OUT    std_logic;
      LED1              OUT    std_logic;
      audioPwmL         OUT    std_ulogic;
      audioPwmL_n       OUT    std_ulogic;
      audioPwmR         OUT    std_ulogic;
      audioPwmR_n       OUT    std_ulogic;
      stepUpPwm         OUT    std_ulogic;
      testOut           OUT    std_logic_vector (1 TO 16)

END audioAmp_FPGA ;
```

Design Flow

Generation VHDL



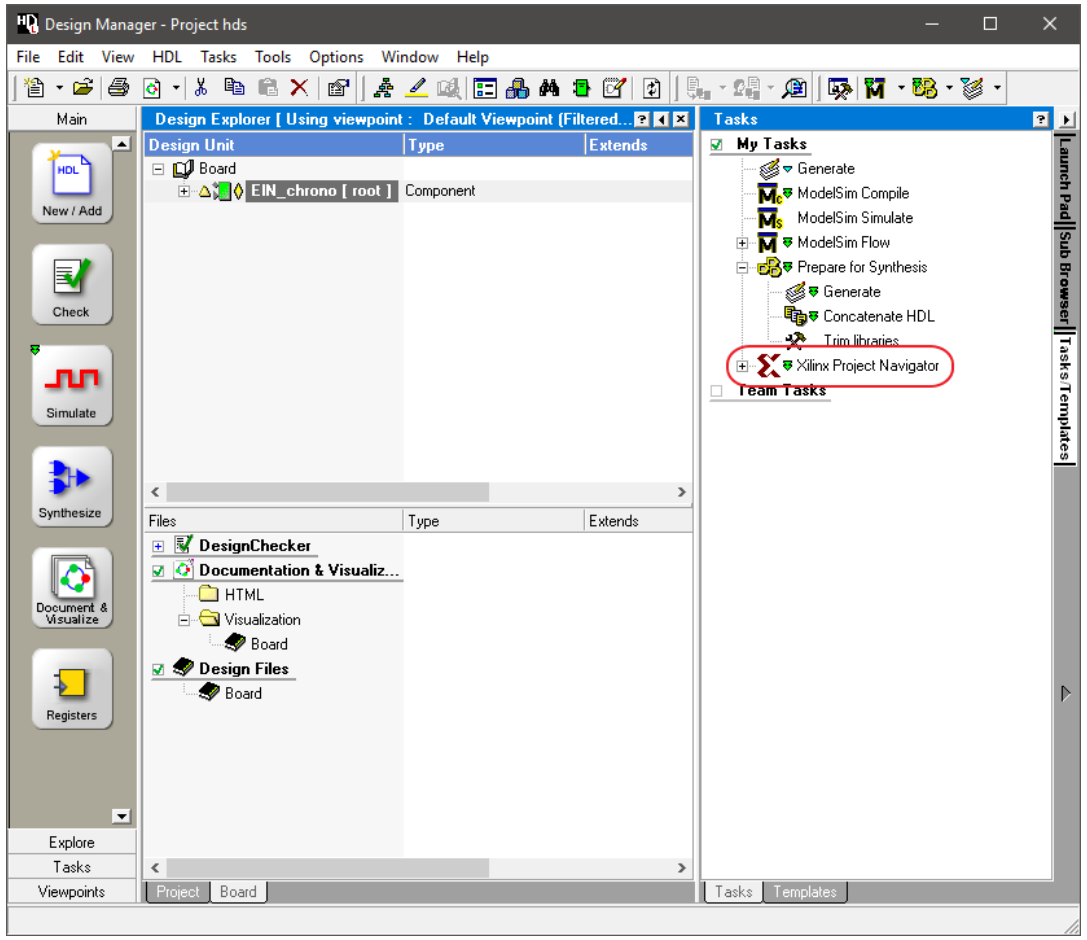


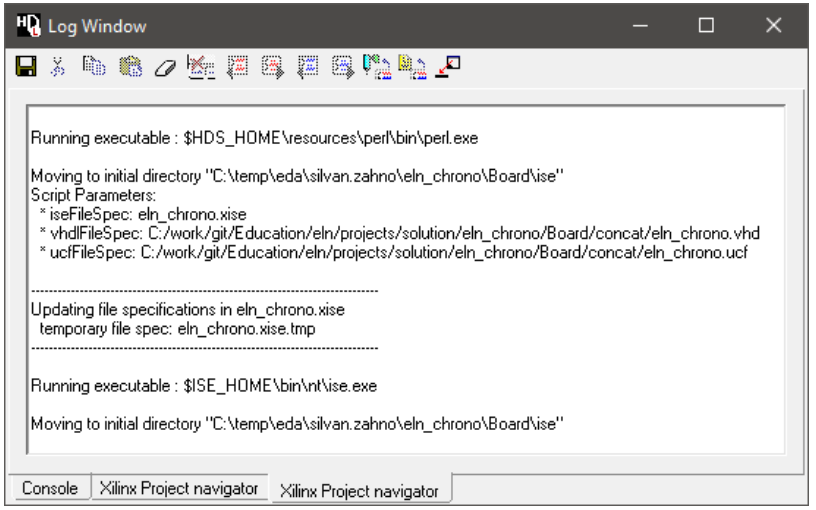
Design Flow
Generation UCF

```
#----------------------------------------------------
# Clock and reset
#
NET     "clock"         LOC = "A10";
NET     "reset_n"       LOC = "A15"     | PULLUP;
NET     "testMode"      LOC = "T10";

#----------------------------------------------------
# Buttons
#
NET     "restart_n"     LOC = "E8" ;
NET     "start_n"       LOC = "G9" ;
NET     "stop_n"        LOC = "F9" ;

#----------------------------------------------------
# LEDs_n
#
NET     "LED1"          LOC = "B16";
NET     "LED2"          LOC = "A16";
NET     "LEDs_n<1>"     LOC = "E7" ;
NET     "LEDs_n<2>"     LOC = "B14";
NET     "LEDs_n<3>"     LOC = "B13";
NET     "LEDs_n<4>"     LOC = "B11";
NET     "LEDs_n<5>"     LOC = "A8" ;
NET     "LEDs_n<6>"     LOC = "C7" ;
NET     "LEDs_n<7>"     LOC = "A14";
NET     "LEDs_n<8>"     LOC = "A11";

#----------------------------------------------------
# Motor
#
NET     "motorOn1"      LOC = "B4" ;
NET     "motorOn2"      LOC = "B3" ;
NET     "coil1_n"       LOC = "G6" ;
NET     "coil2_n"       LOC = "C5" ;
NET     "coil3_n"       LOC = "C4" ;
NET     "coil4_n"       LOC = "C3" ;

NET     "sensor_n"      LOC = "A4" ;

#----------------------------------------------------
# Globals
#
NET "*" IOSTANDARD = LVCMOS33;
```

Design Flow

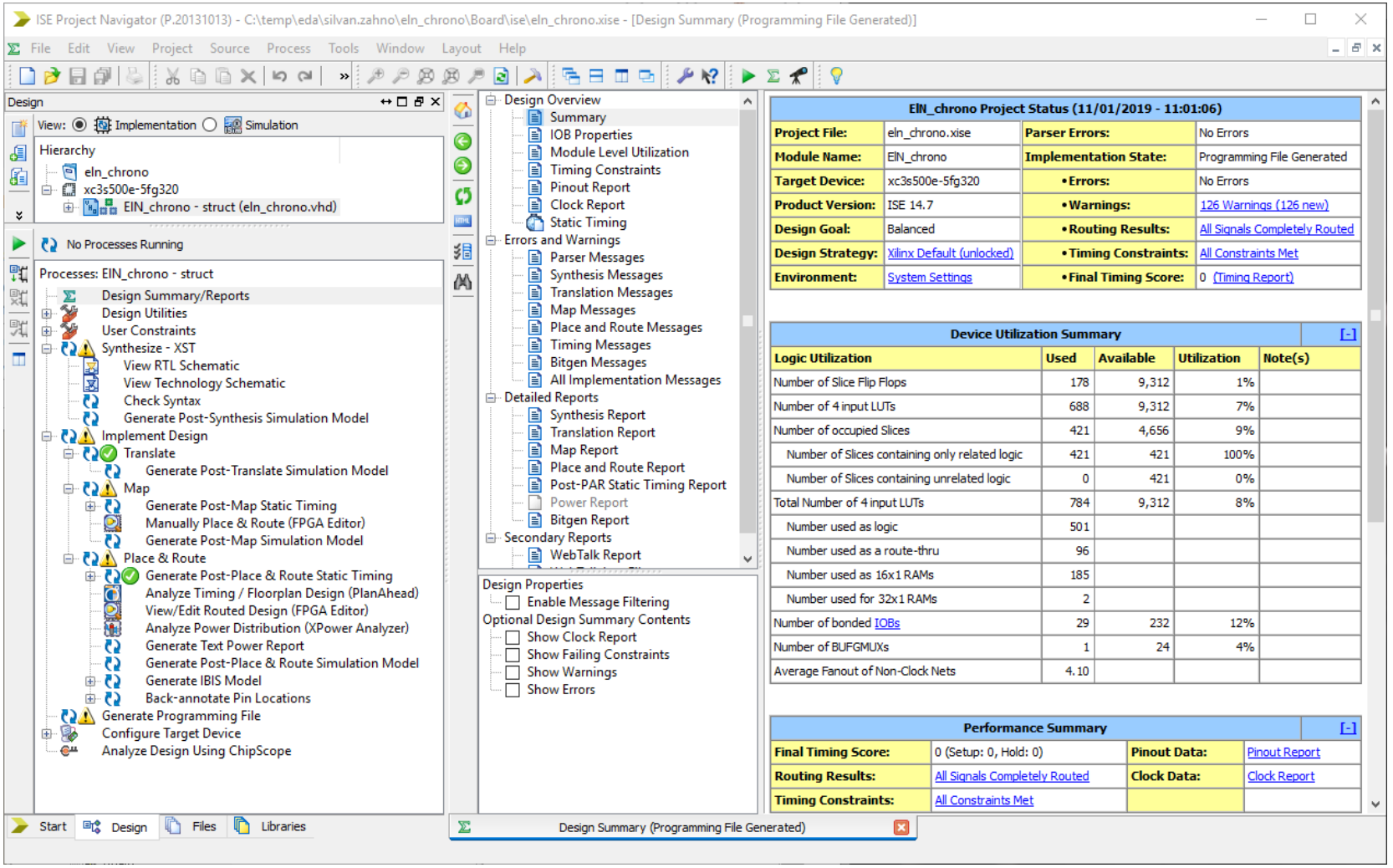
Starting Xilinx ISE





Design Flow

Xilinx ISE



Design Flow
Xilinx ISE Report

ElN_chrono Project Status (11/01/2019 - 11:01:06)			
Project File:	eln_chrono.xise	**Parser Errors:**	No Errors
Module Name:	ElN_chrono	**Implementation State:**	Programming File Generated
Target Device:	xc3s500e-5fg320	**•Errors:**	No Errors
Product Version:	ISE 14.7	**•Warnings:**	126 Warnings (126 new)
Design Goal:	Balanced	**•Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	**•Timing Constraints:**	All Constraints Met
Environment:	System Settings	**•Final Timing Score:**	0 (Timing Report)

Device Utilization Summary [-]				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	178	9,312	1%	
Number of 4 input LUTs	688	9,312	7%	
Number of occupied Slices	421	4,656	9%	
Number of Slices containing only related logic	421	421	100%	
Number of Slices containing unrelated logic	0	421	0%	
Total Number of 4 input LUTs	784	9,312	8%	
Number used as logic	501			
Number used as a route-thru	96			
Number used as 16x1 RAMs	185			
Number used for 32x1 RAMs	2			
Number of bonded IOBs	29	232	12%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	4.10			

Performance Summary [-]			
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports [-]					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Fri Nov 1 11:00:10 2019	0	62 Warnings (62 new)	204 Infos (204 new)
Translation Report	Current	Fri Nov 1 11:00:14 2019	0	0	0
Map Report	Current	Fri Nov 1 11:00:25 2019	0	60 Warnings (60 new)	4 Infos (4 new)
Place and Route Report	Current	Fri Nov 1 11:00:54 2019	0	3 Warnings (3 new)	2 Infos (2 new)
Power Report					
Post-PAR Static Timing Report	Current	Fri Nov 1 11:00:57 2019	0	0	6 Infos (6 new)
Bitgen Report	Current	Fri Nov 1 11:01:04 2019	0	1 Warning (1 new)	0

Secondary Reports [-]		
Report Name	**Status**	**Generated**
WebTalk Report	Current	Fri Nov 1 11:01:04 2019
WebTalk Log File	Current	Fri Nov 1 11:01:06 2019

Design Flow

Report Synthesis

```
=========================================================================
*                            Design Summary                             *
=========================================================================
Top Level Output File Name         : ELN_chrono.ngc
Primitive and Black Box Usage:
------------------------------
# BELS                             : 889
#      BUF                         : 1
#      GND                         : 1
#      INV                         : 17
#      LUT1                        : 95
#      LUT2                        : 47
#      LUT2_D                      : 1
#      LUT2_L                      : 3
#      LUT3                        : 199
#      LUT3_D                      : 6
#      LUT3_L                      : 3
#      LUT4                        : 193
#      LUT4_D                      : 16
#      LUT4_L                      : 15
#      MUXCY                       : 52
#      MUXF5                       : 141
#      MUXF6                       : 51
#      MUXF7                       : 7
#      VCC                         : 1
#      XORCY                       : 40
# FlipFlops/Latches                : 178
#      FDC                         : 48
#      FDCE                        : 71
#      FDE                         : 44
#      FDP                         : 4
#      FDPE                        : 11
# RAMS                             : 187
#      RAM16X1D                    : 187
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 27
#      IBUF                        : 6
#      OBUF                        : 21

Device utilization summary:
---------------------------
Selected Device : 3s500efg320-5

 Number of Slices:                      624  out of   4656    13%
 Number of Slice Flip Flops:            178  out of   9312     1%
 Number of 4 input LUTs:                969  out of   9312    10%
    Number used as logic:               595
    Number used as RAMs:                374
 Number of IOs:                          29
 Number of bonded IOBs:                  28  out of    232    12%
 Number of GCLKs:                         1  out of     24     4%
```

```
=========================================================================
*                            Timing Report                              *
=========================================================================

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
clock                              | BUFGP                  | 365   |
-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:
----------------------------------------
-----------------------------------+----------------------------------------+-------+
Control Signal                     | Buffer(FF name)                        | Load  |
-----------------------------------+----------------------------------------+-------+
resetSynch(I7/out11_INV_0:O)       | NONE(I0/I_lcdCtl/I_ser/resetCounter_0)| 133   |
reset(I1/out11_INV_0:O)            | NONE(I6/Q)                             | 1     |
-----------------------------------+----------------------------------------+-------+

Timing Summary:
---------------
Speed Grade: -5

   Minimum period: 10.079ns (Maximum Frequency: 99.215MHz)
   Minimum input arrival time before clock: 5.798ns
   Maximum output required time after clock: 10.466ns
   Maximum combinational path delay: 8.860ns
```

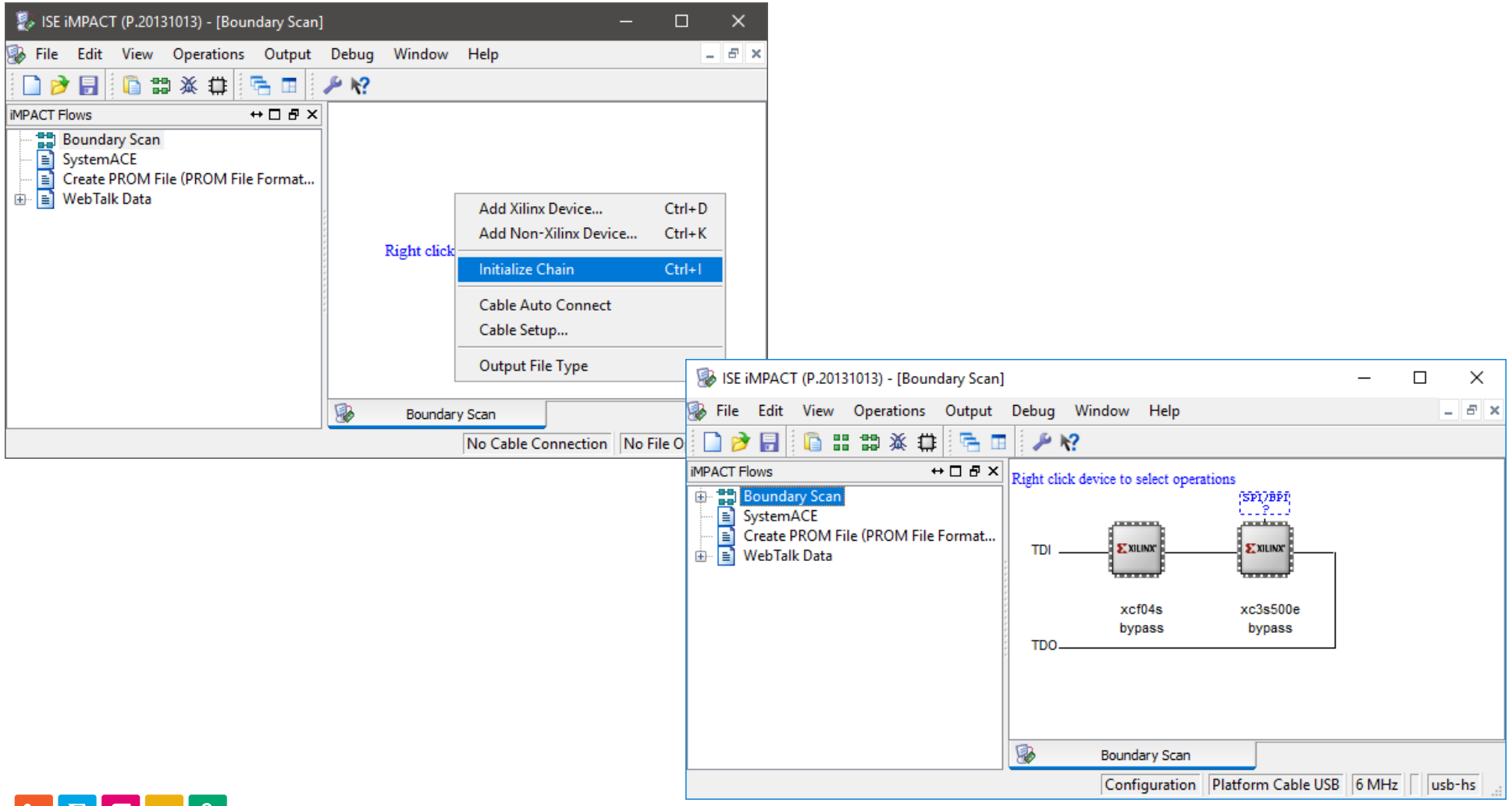
Design Flow

Report Place & Route

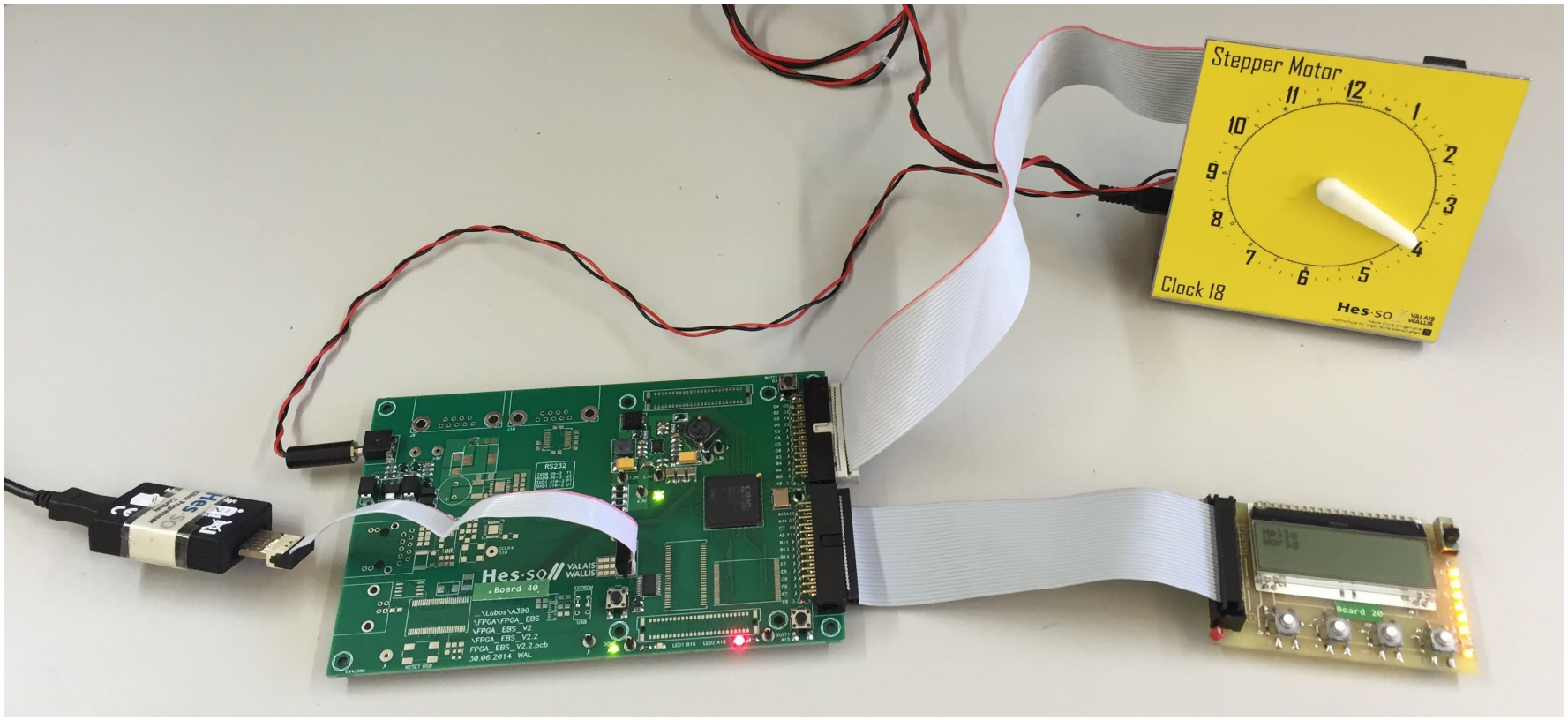
```
Design Information
------------------
Command Line   : map -intstyle ise -p xc3s500e-fg320-5 -cm area -ir off -pr off
-c 100 -o ELN_chrono_map.ncd ELN_chrono.ngd ELN_chrono.pcf
Target Device  : xc3s500e
Target Package : fg320
Target Speed   : -5
Mapper Version : spartan3e -- $Revision: 1.55 $
Mapped Date    : Fri Nov 01 11:00:17 2019

Design Summary
--------------
Number of errors:      0
Number of warnings:   60
Logic Utilization:
  Number of Slice Flip Flops:           178 out of   9,312    1%
  Number of 4 input LUTs:               688 out of   9,312    7%
Logic Distribution:
  Number of occupied Slices:            421 out of   4,656    9%
    Number of Slices containing only related logic:     421 out of     421 100%
    Number of Slices containing unrelated logic:          0 out of     421   0%
      *See NOTES below for an explanation of the effects of unrelated logic.
  Total Number of 4 input LUTs:         784 out of   9,312    8%
    Number used as logic:               501
    Number used as a route-thru:         96
    Number used as 16x1 RAMs:           185
    Number used for 32x1 RAMs:            2
      (Two LUTs used per 32x1 RAM)

  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.

  Number of bonded IOBs:                 29 out of     232   12%
  Number of BUFGMUXs:                     1 out of      24    4%

Average Fanout of Non-Clock Nets:               4.10

Peak Memory Usage:  300 MB
Total REAL time to MAP completion:  8 secs
Total CPU time to MAP completion:   2 secs
```

```
Design Summary Report:

 Number of External IOBs                          29 out of 232    12%

   Number of External Input IOBs                  8

      Number of External Input IBUFs              8
        Number of LOCed External Input IBUFs      8 out of 8     100%


   Number of External Output IOBs                21

      Number of External Output IOBs              21
        Number of LOCed External Output IOBs      21 out of 21    100%


   Number of External Bidir IOBs                  0


   Number of BUFGMUXs                        1 out of 24      4%
   Number of Slices                        421 out of 4656    9%
      Number of SLICEMs                    111 out of 2328    4%



Overall effort level (-ol):   High
Placer effort level (-pl):    High
Placer cost table entry (-t): 1
Router effort level (-rl):    High
```

Design Flow
Programming

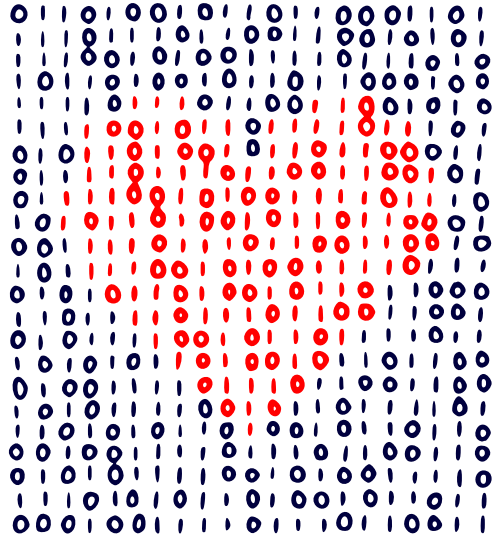


Design Flow
Programming



FPGA

- We now know everything about:
  - ASIC’s
  - FPGA’s
  - Implementation



References

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  https://www.xilinx.com/
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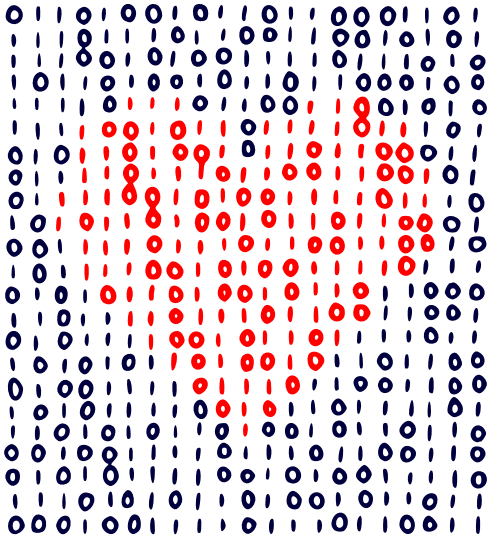
  https://www.microsemi.com/product-directory/1636-fpga-soc

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