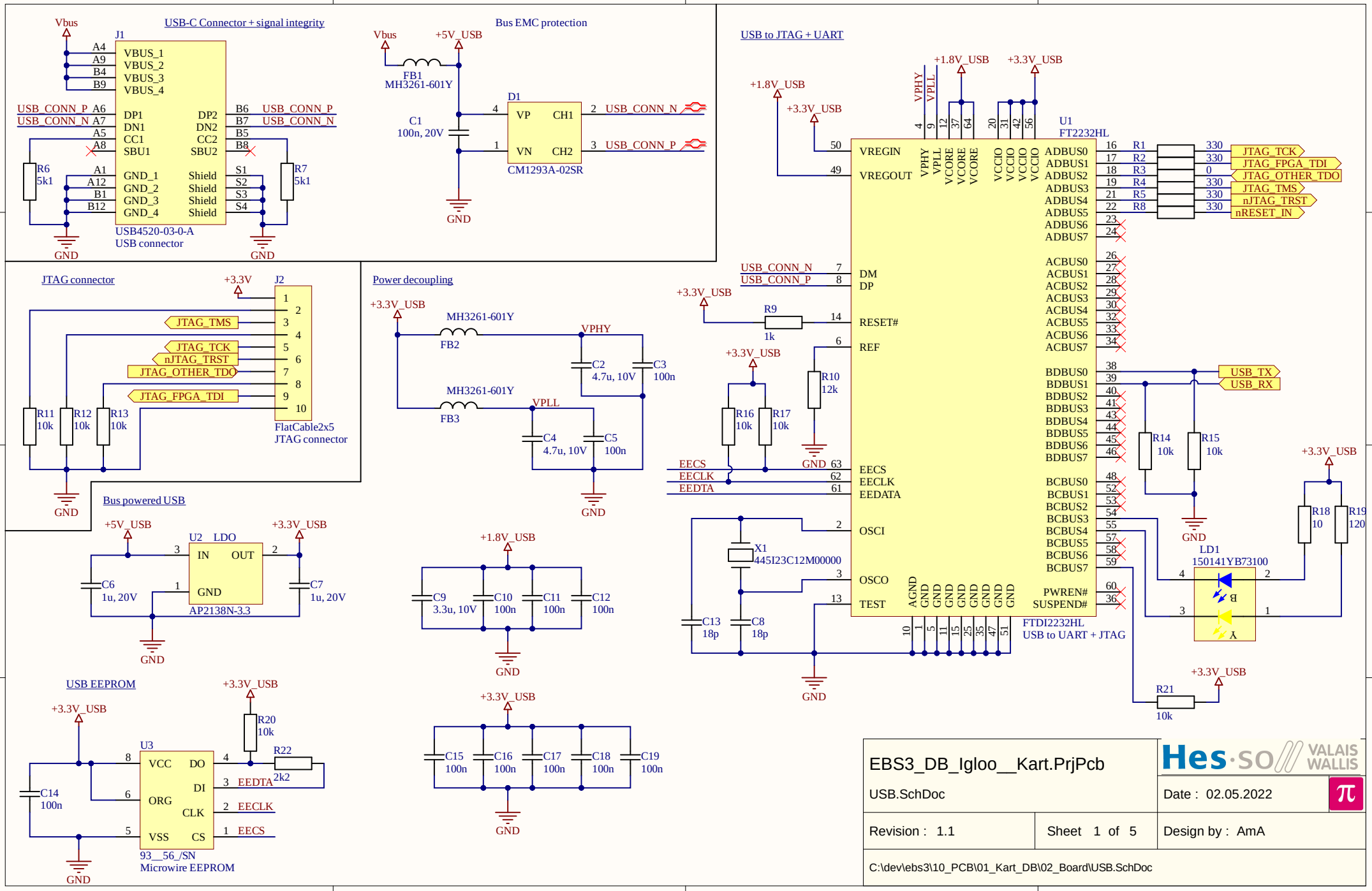
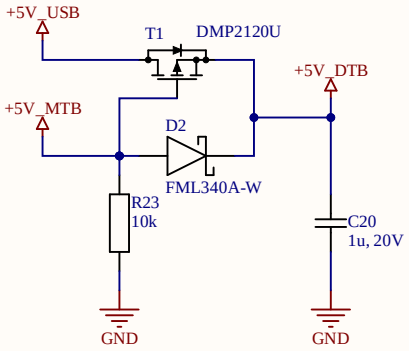
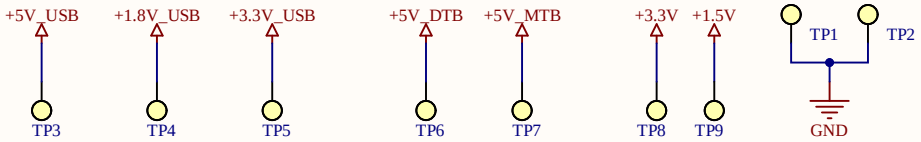

USB-C Connector + signal integrity
J1
USB4520-03-0-A
USB connector
Bus EMC protection
FB1
MH3261-601Y
D1
CM1293A-02SR
C1
100n, 20V
USB to JTAG + UART
U1
FT2232HL
FTDI2232HL
USB to UART + JTAG
JTAG connector
J2
FlatCable2x5
JTAG connector
Power decoupling
Bus powered USB
U2 LDO
AP2138N-3.3
USB EEPROM
U3
93__56_/SN
Microwire EEPROM
X1
445I23C12M00000
LD1
150141YB73100
EBS3_DB_Igloo__Kart.PrjPcb
USB.SchDoc
Date : 02.05.2022
Revision : 1.1
Sheet 1 of 5
Design by : AmA
C:\dev\ebs3\10_PCB\01_Kart_DB\02_Board\USB.SchDoc

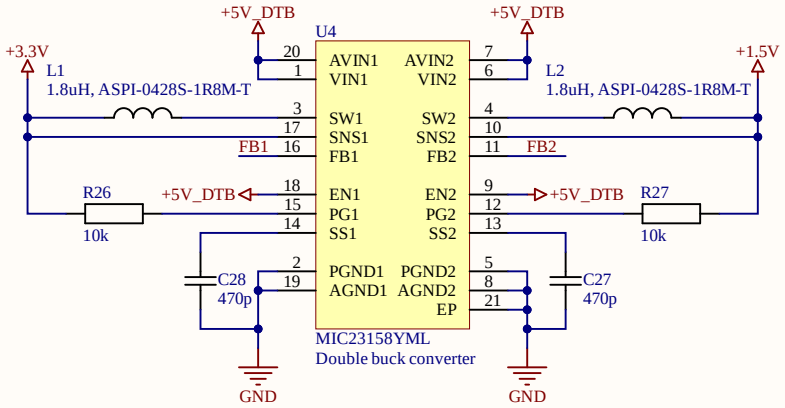
5V selector

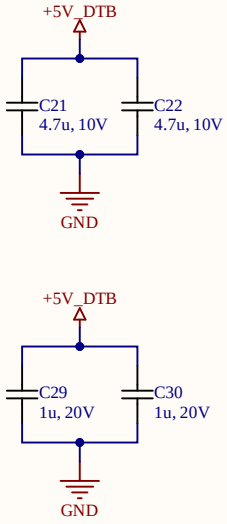


Test points

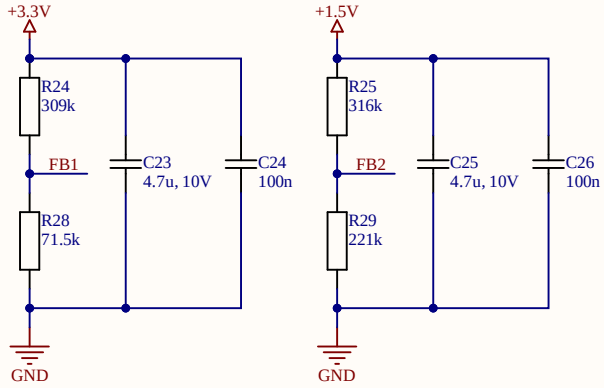


Buck converters

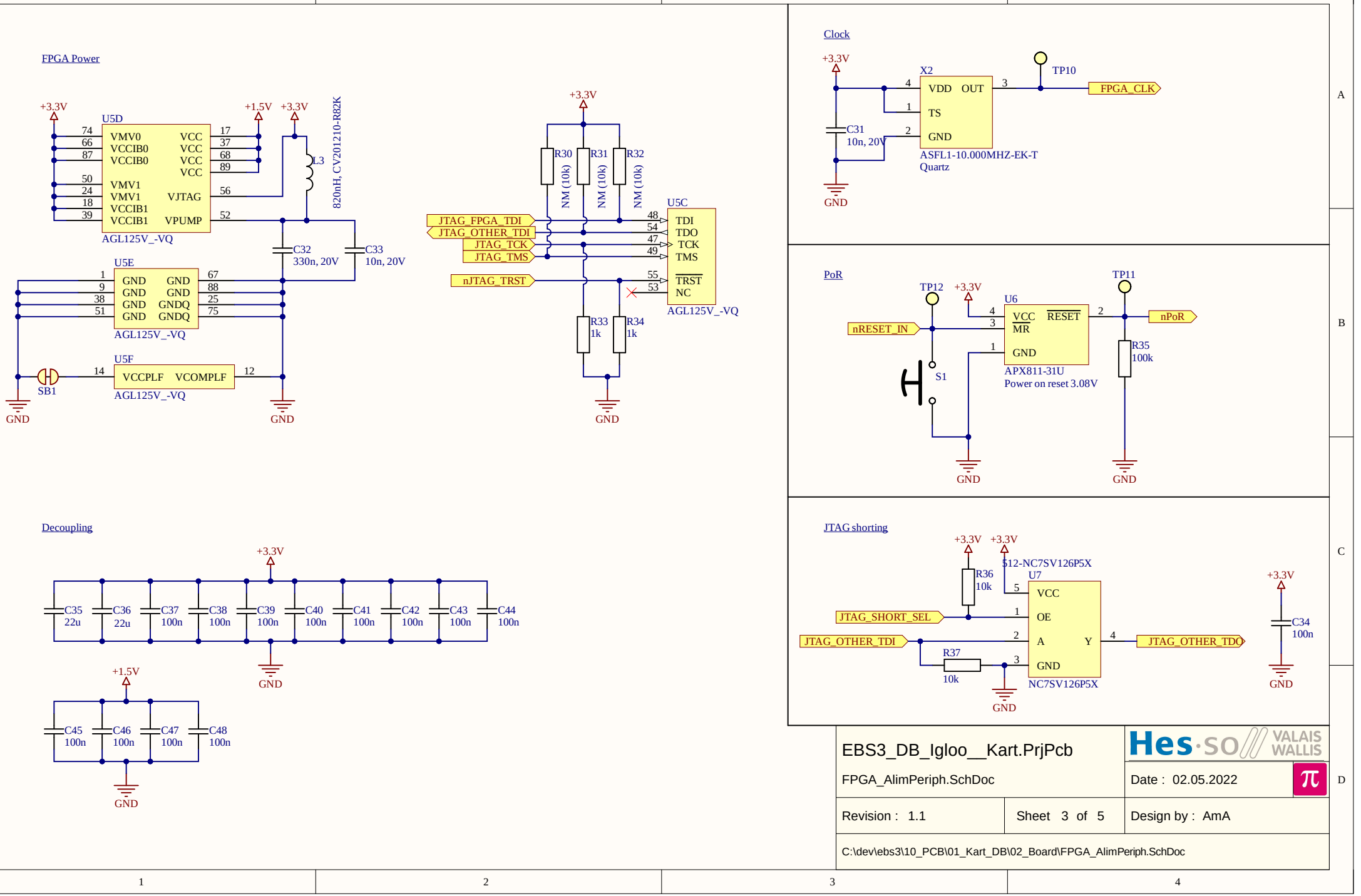




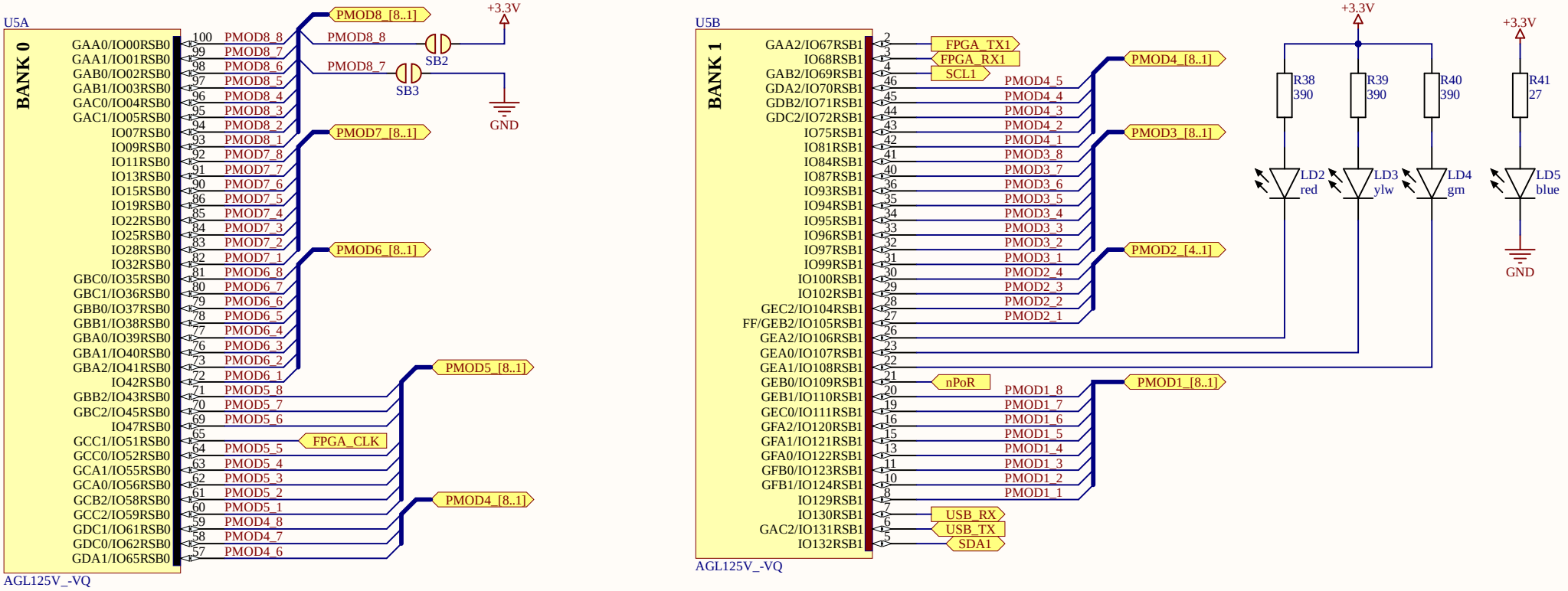
Output voltage definition

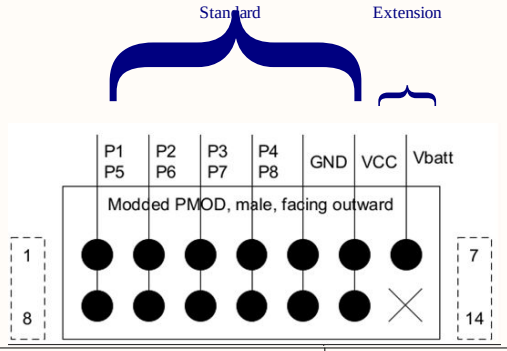


EBS3_DB_Igloo__Kart.PrjPcb		Hes·SO VALAIS WALLIS
Power.SchDoc		Date : 02.05.2022
Revision : 1.1	Sheet 2 of 5	Design by : AmA
C:\dev\ebs3\10_PCB\01_Kart_DB\02_Board\Power.SchDoc		

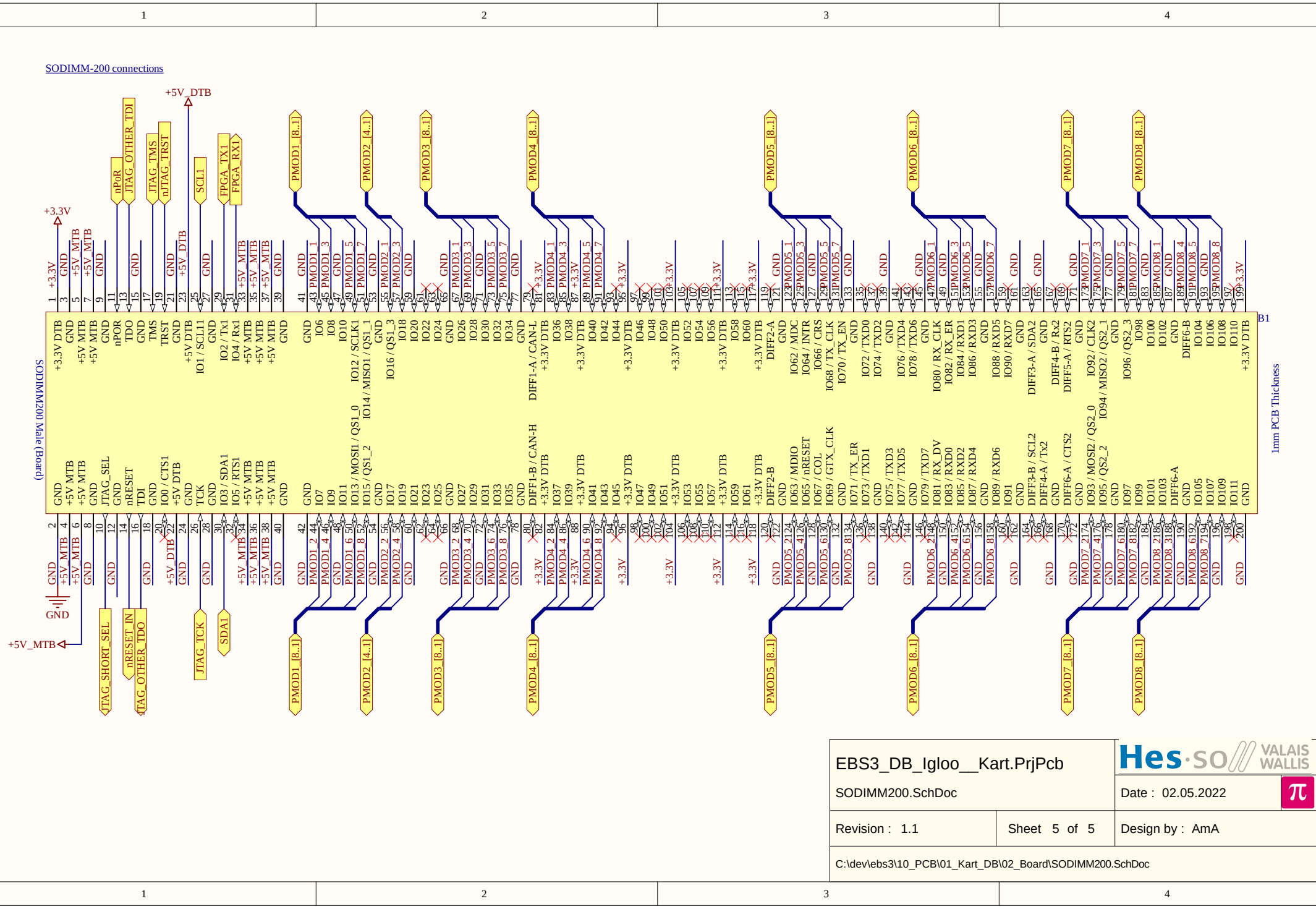

FPGA Power
+3.3V
+1.5V
+3.3V
U5D
VMV0
VCCIB0
VCCIB0
VMV1
VMV1
VCCIB1
VCCIB1
VCC
VCC
VCC
VCC
VJTAG
VPUMP
AGL125V_-VQ
L3
820nH, CV201210-R82K
C32
330n, 20V
C33
10n, 20V
U5E
GND
GND
GND
GND
GND
GND
GNDQ
GNDQ
AGL125V_-VQ
U5F
VCCPLF
VCOMPLF
AGL125V_-VQ
SB1
GND
GND
+3.3V
R30
R31
R32
NM (10k)
NM (10k)
NM (10k)
U5C
JTAG_FPGA_TDI
JTAG_OTHER_TDI
JTAG_TCK
JTAG_TMS
nJTAG_TRST
TDI
TDO
TCK
TMS
TRST
NC
AGL125V_-VQ
R33
1k
R34
1k
GND
Clock
+3.3V
X2
VDD
OUT
TS
GND
ASFL1-10.000MHZ-EK-T
Quartz
TP10
FPGA_CLK
C31
10n, 20V
GND
PoR
TP12
+3.3V
U6
VCC
RESET
MR
GND
APX811-31U
Power on reset 3.08V
TP11
nPoR
nRESET_IN
S1
R35
100k
GND
GND
JTAG shorting
+3.3V
+3.3V
512-NC7SV126P5X
U7
R36
10k
JTAG_SHORT_SEL
JTAG_OTHER_TDI
R37
10k
VCC
OE
A
Y
GND
NC7SV126P5X
JTAG_OTHER_TDO
+3.3V
C34
100n
GND
GND
Decoupling
+3.3V
C35
22u
C36
22u
C37
100n
C38
100n
C39
100n
C40
100n
C41
100n
C42
100n
C43
100n
C44
100n
GND
+1.5V
C45
100n
C46
100n
C47
100n
C48
100n
GND
EBS3_DB_Igloo__Kart.PrjPcb
FPGA_AlimPeriph.SchDoc
Hes·SO VALAIS WALLIS
Date : 02.05.2022
Revision : 1.1
Sheet 3 of 5
Design by : AmA
C:\dev\ebs3\10_PCB\01_Kart_DB\02_Board\FPGA_AlimPeriph.SchDoc

FPGA IOs





EBS3_DB_Igloo__Kart.PrjPcb		Hes·SO VALAIS WALLIS
FPGA_IO.SchDoc		Date : 02.05.2022
Revision : 1.1	Sheet 4 of 5	Design by : AmA
C:\dev\ebs3\10_PCB\01_Kart_DB\02_Board\FPGA_IO.SchDoc		


SODIMM-200 connections
SODIMM200 Male (Board)
1mm PCB Thickness
B1
+3.3V
+5V_DTB
+5V_MTB
GND
nPoR
JTAG_OTHER_TDI
JTAG_TMS
nJTAG_TRST
SCL1
FPGA_TX1
FPGA_RX1
PMOD1_[8..1]
PMOD2_[4..1]
PMOD3_[8..1]
PMOD4_[8..1]
PMOD5_[8..1]
PMOD6_[8..1]
PMOD7_[8..1]
PMOD8_[8..1]
JTAG_SHORT_SEL
nRESET_IN
JTAG_OTHER_TDO
JTAG_TCK
SDA1
EBS3_DB_Igloo__Kart.PrjPcb
SODIMM200.SchDoc
Revision : 1.1
Sheet 5 of 5
Date : 02.05.2022
Design by : AmA
C:\dev\ebs3\10_PCB\01_Kart_DB\02_Board\SODIMM200.SchDoc
Hes·SO VALAIS WALLIS