Unified Clock System (UCS)

The Unified Clock System (UCS) module provides the various clocks for a device. This chapter describes the operation of the UCS module, which is implemented in all devices.

Topic **Page**

5.1 Unified Clock System (UCS) Introduction

The UCS module supports low system cost and ultralow power consumption. Using three internal clock signals, the user can select the best balance of performance and low power consumption. The UCS module can be configured to operate without any external components, with one or two external crystals, or with resonators, under full software control.

The UCS module includes up to five clock sources:

- XT1CLK: Low-frequency or high-frequency oscillator that can be used either with low-frequency 32768 Hz watch crystals, standard crystals, resonators, or external clock sources in the 4 MHz to 32 MHz range. XT1CLK can be used as a clock reference into the FLL. Some devices only support the low frequency oscillator for XT1CLK. See the device-specific data sheet for supported functions.
- VLOCLK: Internal very low power, low frequency oscillator with 10 kHz typical frequency
- REFOCLK: Internal, trimmed, low-frequency oscillator with 32768 Hz typical frequency, with the ability to be used as a clock reference into the FLL
- DCOCLK: Internal digitally-controlled oscillator (DCO) that can be stabilized by the FLL
- XT2CLK: Optional high-frequency oscillator that can be used with standard crystals, resonators, or external clock sources in the 4 MHz to 32 MHz range. XT2CLK can be used as a clock reference into the FLL.

Three clock signals are available from the UCS module:

- ACLK: Auxiliary clock. The ACLK is software selectable as XT1CLK, REFOCLK, VLOCLK, DCOCLK, DCOCLKDIV, and when available, XT2CLK. DCOCLKDIV is the DCOCLK frequency divided by 1, 2, 4, 8, 16, or 32 within the FLL block. ACLK can be divided by 1, 2, 4, 8, 16, or 32. ACLK/n is ACLK divided by 1, 2, 4, 8, 16, or 32 and is available externally at a pin. ACLK is software selectable by individual peripheral modules.
- MCLK: Master clock. MCLK is software selectable as XT1CLK, REFOCLK, VLOCLK, DCOCLK, DCOCLKDIV, and when available, XT2CLK. DCOCLKDIV is the DCOCLK frequency divided by 1, 2, 4, 8, 16, or 32 within the FLL block. MCLK can be divided by 1, 2, 4, 8, 16, or 32. MCLK is used by the CPU and system.
- SMCLK: Subsystem master clock. SMCLK is software selectable as XT1CLK, REFOCLK, VLOCLK, DCOCLK, DCOCLKDIV, and when available, XT2CLK. DCOCLKDIV is the DCOCLK frequency divided by 1, 2, 4, 8, 16, or 32 within the FLL block. SMCLK can be divided by 1, 2, 4, 8, 16, or 32. SMCLK is software selectable by individual peripheral modules.

The block diagram of the UCS module is shown in Figure 5-1.

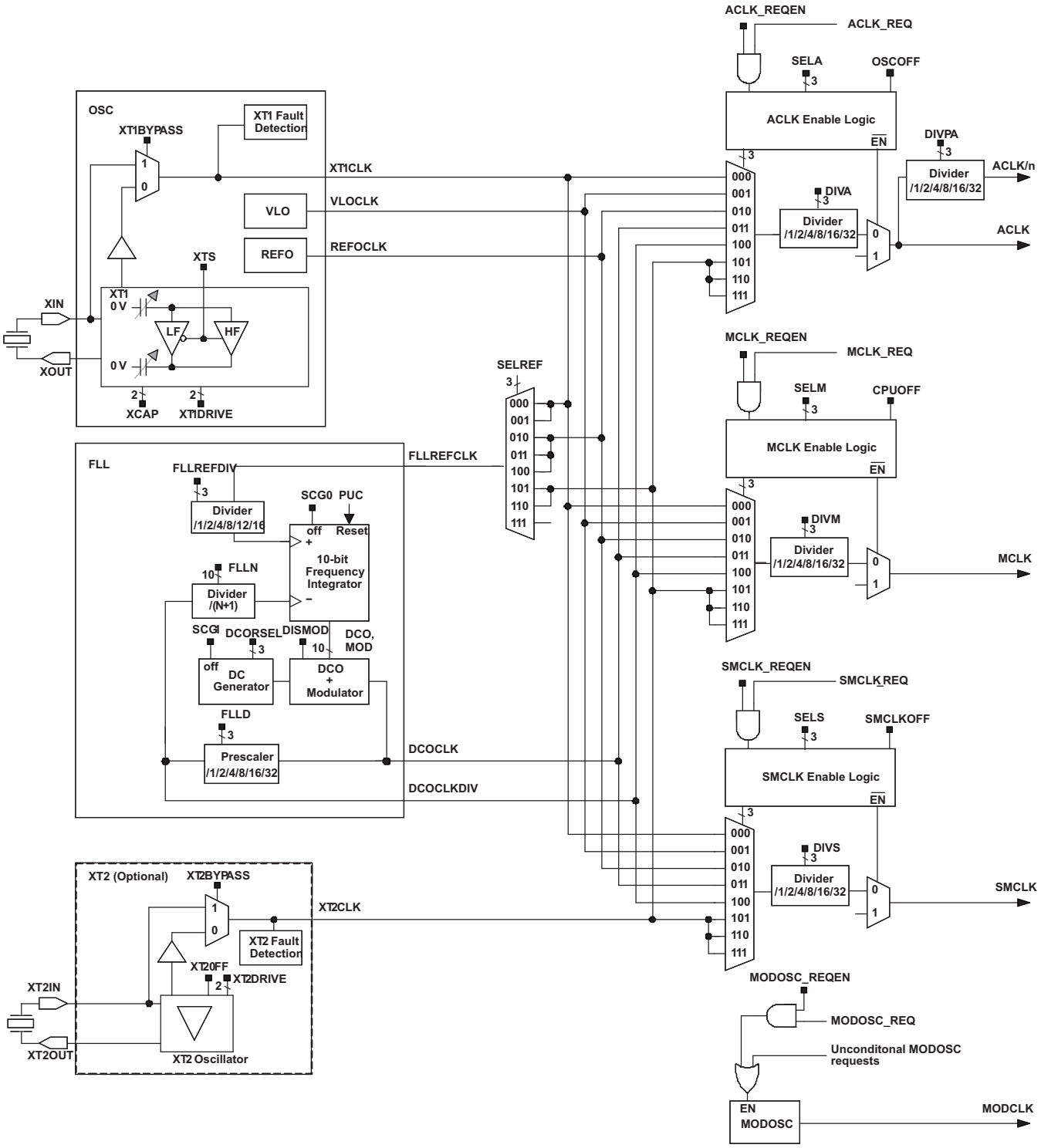

Figure 5-1. UCS Block Diagram

5.2 UCS Operation

After a PUC, the UCS module default configuration is:

- XT1 in LF mode is selected as the oscillator source for XT1CLK. XT1CLK is selected for ACLK.
- DCOCLKDIV is selected for MCLK.
- DCOCLKDIV is selected for SMCLK.
- FLL operation is enabled and XT1CLK is selected as the FLL reference clock, FLLREFCLK.
- On devices that have XIN and XOUT shared with general-purpose I/O, XIN and XOUT pins are set to general-purpose I/Os and XT1 remains disabled until the I/O ports are configured for XT1 operation. If XIN and XOUT are not shared with general-purpose I/O, XT1 is enabled.
- When available, XT2IN and XT2OUT pins are set to general-purpose I/Os and XT2 is disabled.

As previously stated, FLL operation with XT1 is selected by default. If the crystal pins (XIN, XOUT) are shared with general-purpose I/Os, XT1 will remain disabled until the PSEL bits associated with the crystal pins are set. If XIN and XOUT are not shared with general-purpose I/O, XT1 is enabled. When a 32,768 Hz crystal is used for XT1CLK, the fault control logic immediately causes ACLK to be sourced by the REFOCLK, because XT1 is not stable immediately (see Section 5.2.12). Once crystal startup is obtained and settled, the FLL stabilizes MCLK and SMCLK to 1.048576 MHz and f_{DCO} = 2.097152 MHz.

Status register control bits (SCG0, SCG1, OSCOFF, and CPUOFF) configure the MSP430 operating modes and enable or disable portions of the UCS module (see the SYS chapter). Registers UCSCTL0 through UCSCTL8, configure the UCS module.

The UCS module can be configured or reconfigured by software at any time during program execution.

NOTE: For devices using RTC_B, RTC_C, or RTC_D (RTC modules supporting LPM3.5) setting bit RTCHOLD = 0 in register RTCCTL1 also enables XT1, independent from UCS configuration.

5.2.1 UCS Module Features for Low-Power Applications

Conflicting requirements typically exist in battery-powered applications:

- Low clock frequency for energy conservation and time keeping
- High clock frequency for fast response times and fast burst processing capabilities
- Clock stability over operating temperature and supply voltage
- Low-cost applications with less-constrained clock accuracy requirements

The UCS module addresses these conflicting requirements by allowing the user to select from the three available clock signals: ACLK, MCLK, and SMCLK.

All three available clock signals can be sourced via any of the available clock sources (XT1CLK, VLOCLK, REFOCLK, DCOCLK, DCOCLKDIV, or XT2CLK), giving complete flexibility in the system clock configuration. A flexible clock distribution and divider system is provided to fine tune the individual clock requirements.

5.2.2 Internal Very-Low-Power Low-Frequency Oscillator (VLO)

The internal VLO provides a typical frequency of 10 kHz (see device-specific data sheet for parameters) without requiring a crystal. The VLO provides for a low-cost ultralow-power clock source for applications that do not require an accurate time base.

The VLO is enabled when it is used to source ACLK, MCLK, or SMCLK (SELA = {1} or SELM = {1} or SELS = {1}).

5.2.3 Internal Trimmed Low-Frequency Reference Oscillator (REFO)

The internal trimmed low-frequency REFO can be used for cost-sensitive applications where a crystal is not required or desired. REFO is internally trimmed to 32.768 kHz typical and provides for a stable reference frequency that can be used as FLLREFCLK. REFO, combined with the FLL, provides for a flexible range of system clock settings without the need for a crystal. REFO consumes no power when not being used.

REFO is enabled under any of the following conditions:

- REFO is a source for ACLK (SELA = {2}) and in active mode (AM) through LPM3 (OSCOFF = 0)
- REFO is a source for MCLK (SELM = {2}) and in active mode (AM) (CPUOFF = 0)
- REFO is a source for SMCLK (SELS = {2}) and in active mode (AM) through LPM1 (SMCLKOFF = 0)
- REFO is a source for FLLREFCLK (SELREF = {2}) and the DCO is a source for ACLK (SELA = {3,4}) and in active mode (AM) through LPM3 (OSCOFF = 0)
- REFO is a source for FLLREFCLK (SELREF = {2}) and the DCO is a source for MCLK (SELM = {3,4}) and in active mode (AM) (CPUOFF = 0)
- REFO is a source for FLLREFCLK (SELREF = {2}) and the DCO is a source for SMCLK (SELS = {3,4}) and in active mode (AM) through LPM1 (SMCLKOFF = 0)

NOTE: REFO Enable for MSP430F543x, MSP430F541x devices

REFO is enabled under any of the following conditions:

- REFO is a source for ACLK (SELA = {2}), MCLK (SELM = {2}), or SMCLK (SELS = {2}) and in active mode (AM) through LPM3 (OSCOFF = 0)
- REFO is a source for FLLREFCLK (SELREF = {2}) and the DCO is a source for ACLK, MCLK, or SMCLK (SELA = {3,4}), MCLK (SELM = {3,4}), or SMCLK (SELS = {3,4}) and in active mode (AM) through LPM3 (OSCOFF = 0)

5.2.4 XT1 Oscillator

The XT1 oscillator supports ultralow-current consumption using a 32,768 Hz watch crystal in low-frequency (LF) mode (XTS = 0) . A watch crystal connects to XIN and XOUT without any other external components. The software-selectable XCAP bits configure the internally provided load capacitance for the XT1 crystal in LF mode. This capacitance can be selected as 2 pF, 6 pF, 9 pF, or 12 pF (typical). Additional external capacitors can be added if necessary.

On some devices, the XT1 oscillator also supports high-speed crystals or resonators when in high-frequency (HF) mode (XTS = 1). The high-speed crystal or resonator connects to XIN and XOUT and requires external capacitors on both terminals. These capacitors should be sized according to the crystal or resonator specifications.

The drive settings of XT1 in LF mode can be increased with the XT1DRIVE bits. At power up, the XT1 starts with the highest drive settings for fast, reliable startup. If needed, user software can reduce the drive strength to further reduce power. In HF mode, different crystal or resonator ranges are supported by choosing the proper XT1DRIVE settings .

XT1 may be used with an external clock signal on the XIN pin in either LF or HF mode by setting XT1BYPASS. When used with an external signal, the external frequency must meet the data sheet parameters for the chosen mode. XT1 is powered down when used in bypass mode.

Some devices support XT1 bypass operation with external clock inputs that reside on a different external supply domain, called DV_{IO}. Please refer to the device specific datasheet. On these devices, DV_{IO} has a voltage range of 1.8V ± 10 %. When using the XT1 bypass operation with external clock inputs that reside on DV_{IO}, it is required that XT1BYPASSLV = 1. For example, when XT1BYPASSLV = 1, it is assumed the external clock signal swings from 0V to DV_{IO}. With XT1BYPASS = 0, it is assumed the external clock signal swings from 0V to DV_{CC}. The usage of XT1BYPASSLV allows for interfacing to external clock sources that reside on either the DV_{CC} or DV_{IO} supply domains. When used with an external signal, the external frequency must meet the data sheet parameters for the chosen mode. XT1 is powered down when used in bypass mode.

On many devices, the XT1 pins are shared with general-purpose I/O ports (refer to the device specific datasheet for availability). At power up, the default operation is XT1, LF mode of operation. However, for devices that have XT1 shared with general-purpose I/O ports, XT1 will remain disabled until the ports shared with XT1 are configured for XT1 operation. The configuration of the shared I/O is determined by the PSEL bit associated with XIN and the XT1BYPASS bit. Setting the PSEL bit causes the XIN and XOUT ports to be configured for XT1 operation. If XT1BYPASS is also set, XT1 is configured for bypass mode of operation, and the oscillator associated with XT1 is powered down. In bypass mode of operation, XIN can accept an external clock input signal and XOUT is configured as a general-purpose I/O. The PSEL bit associated with XOUT is a don't care. If the PSEL bit associated with XIN is cleared, both XIN and XOUT ports are configured as general-purpose I/Os, and XT1 is disabled.

On devices where XT1 is not shared with general-purpose I/O ports, XT1 is enabled at power up. In bypass mode of operation (XT1BYPASS = 1), XIN can accept an external clock input signal, and XT1 is powered down.

XT1 is enabled under any of the following conditions:

- XT1 is a source for ACLK (SELA = {0}) and in active mode (AM) through LPM3 (OSCOFF = 0)
- XT1 is a source for MCLK (SELM = {0}) and in active mode (AM) (CPUOFF = 0)
- XT1 is a source for SMCLK (SELS = {0}) and in active mode (AM) through LPM1 (SMCLKOFF = 0)
- XT1 is a source for FLLREFCLK (SELREF = {0}) and the DCO is a source for ACLK (SELA = {3,4}) and in active mode (AM) through LPM3 (OSCOFF = 0)
- XT1 is a source for FLLREFCLK (SELREF = {0}) and the DCO is a source for MCLK (SELM = {3,4}) and in active mode (AM) (CPUOFF = 0)
- XT1 is a source for FLLREFCLK (SELREF = {0}) and the DCO is a source for SMCLK (SELS = {3,4}) and in active mode (AM) through LPM1 (SMCLKOFF = 0)
- XT1OFF = 0. XT1 enabled in active mode (AM) through LPM4. For devices that support LPMx.5, XT1 also remains enabled.

NOTE: XT1 Enable for MSP430F543x, MSP430F541x devices

XT1 is enabled under any of the following conditions:

- XT1 is a source for ACLK, MCLK, or SMCLK (SELA = {0}), MCLK (SELM = {0}), or SMCLK (SELS = {0}) and in active mode (AM) through LPM3 (OSCOFF = 0)
- XT1 is a source for FLLREFCLK (SELREF = {0}) and the DCO is a source for ACLK, MCLK, or SMCLK (SELA = {3,4}), MCLK (SELM = {3,4}), or SMCLK (SELS = {3,4}) and in active mode (AM) through LPM3 (OSCOFF = 0)
- XT1OFF = 0. XT1 enabled in active mode (AM) through LPM4.

5.2.5 XT2 Oscillator

Some devices have a second crystal oscillator, XT2. XT2 sources XT2CLK, and its characteristics are identical to XT1 in HF mode. The XT2DRIVE bits select the frequency range of operation of XT2.

XT2 may be used with external clock signals on the XT2IN pin by setting XT2BYPASS. When used with an external signal, the external frequency must meet the data-sheet parameters for XT2. XT2 is powered down when used in bypass mode.

Some devices support XT2 bypass operation with external clock inputs that reside on a different external supply domain, called DV_{IO}. Please refer to the device specific datasheet. On these devices, DV_{IO} has a voltage range of 1.8V ± 10 %. When using the XT2 bypass operation with external clock inputs that reside on DV_{IO}, it is required that XT2BYPASSLV = 1. For example, when XT2BYPASSLV = 1, it is assumed the external clock signal swings from 0V to DV_{IO}. With XT2BYPASS = 0, it is assumed the external clock signal swings from 0V to DV_{CC}. The usage of XT2BYPASSLV allows for interfacing to external clock sources that reside on either the DV_{CC} or DV_{IO} supply domains. When used with an external signal, the external frequency must meet the data sheet parameters for the chosen mode. XT2 is powered down when used in bypass mode.

The XT2 pins are shared with general-purpose I/O ports. At power up, the default operation is XT2. However, XT2 remains disabled until the ports shared with XT2 are configured for XT2 operation. The configuration of the shared I/O is determined by the PSEL bit associated with XT2IN and the XT2BYPASS bit. Setting the PSEL bit causes the XT2IN and XT2OUT ports to be configured for XT2 operation. If XT2BYPASS is also set, XT2 is configured for bypass mode of operation, and the oscillator associated with XT2 is powered down. In bypass mode of operation, XT2IN can accept an external clock input signal and XT2OUT is configured as a general-purpose I/O. The PSEL bit associated with XT2OUT is a don't care.

If the PSEL bit associated with XT2IN is cleared, both XT2IN and XT2OUT ports are configured as general-purpose I/Os, and XT2 is disabled.

XT2 is enabled under any of the following conditions:

- XT2 is a source for ACLK (SELA = {5,6,7}) and in active mode (AM) through LPM3 (OSCOFF = 0)
- XT2 is a source for MCLK (SELM = {5,6,7}) and in active mode (AM) (CPUOFF = 0)
- XT2 is a source for SMCLK (SELS = {5,6,7}) and in active mode (AM) through LPM1 (SMCLKOFF = 0)
- XT2 is a source for FLLREFCLK (SELREF = {5,6}) and the DCO is a source for ACLK (SELA = {3,4}) and in active mode (AM) through LPM3 (OSCOFF = 0)
- XT2 is a source for FLLREFCLK (SELREF = {5,6}) and the DCO is a source for MCLK (SELM = {3,4}) and in active mode (AM) (CPUOFF = 0)
- XT2 is a source for FLLREFCLK (SELREF = {5,6}) and the DCO is a source for SMCLK (SELS = {3,4}) and in active mode (AM) through LPM1 (SMCLKOFF = 0)
- XT2OFF = 0. XT2 enabled in active mode (AM) through LPM4. For devices that support LPMx.5, XT2 also remains enabled.

NOTE: XT2 Enable for MSP430F543x, MSP430F541x devices

XT2 is enabled under any of the following conditions:

- XT2 is a source for ACLK, MCLK, or SMCLK (SELA = {5,6,7}), MCLK (SELM = {5,6,7}), or SMCLK (SELS = {5,6,7}) and in active mode (AM) through LPM3 (OSCOFF = 0)
- XT2 is a source for FLLREFCLK (SELREF = {5,6,7}) and the DCO is a source for ACLK, MCLK, or SMCLK (SELA = {3,4}), MCLK (SELM = {3,4}), or SMCLK (SELS = {3,4}) and in active mode (AM) through LPM3 (OSCOFF = 0)
- XT2OFF = 0. XT2 enabled in active mode (AM) through LPM4.

5.2.6 Digitally-Controlled Oscillator (DCO)

The DCO is an integrated digitally controlled oscillator. The DCO frequency can be adjusted by software using the DCORSEL, DCO, and MOD bits. The DCO frequency can be optionally stabilized by the FLL to a multiple frequency of FLLREFCLK/n. The FLL can accept different reference sources selectable via the SELREF bits. Reference sources include XT1CLK, REFOCLK, or XT2CLK (if available) . The value of n is defined by the FLLREFDIV bits (n = 1, 2, 4, 8, 12, or 16). The default is n = 1. There may be scenarios in which FLL operation is not required or desired; in these cases, no FLLREFCLK is necessary. This can be accomplished by setting SELREF = {7}.

NOTE: For the F543x and F541x non-A versions only.

Setting SELREF = {7} sets XT2CLK as the FLL reference clock.

The FLLD bits configure the FLL prescaler divider value D to 1, 2, 4, 8, 16, or 32. By default, D = 2, and MCLK and SMCLK are sourced from DCOCLKDIV, providing a clock frequency DCOCLK/2.

The divider (N + 1) and the divider value D define the DCOCLK and DCOCLKDIV frequencies. The divider (N + 1) can be set using the FLLN bits, where N > 0. The smallest divider (N + 1) that can be used is a divider of two. The logic will cause FLLN = 1h, if FLLN = 0h is unintentionally written. Therefore setting FLLN = 0h is also equivalent to setting FLLN = 1h and will result in a divider of 2. All other FLLN settings behave as described e.g. FLLN = 2h results in a divider of 3, FLLN = 3h results in a divider of 4, etc.

$f_{DCOCLK} = D \times (N + 1) \times (f_{FLLREFCLK} \div n)$

$f_{DCOCLKDIV} = (N + 1) \times (f_{FLLREFCLK} \div n)$

Adjusting DCO Frequency

By default, FLL operation is enabled. FLL operation can be disabled by setting SCG0 or SCG1. Once disabled, the DCO continues to operate at the current settings defined in UCSCTL0 and UCSCTL1. The DCO frequency can be adjusted manually if desired. Otherwise, the DCO frequency is stabilized by the FLL operation.

After a PUC, DCORSEL = {2} and DCO = {0}. MCLK and SMCLK are sourced from DCOCLKDIV. Because the CPU executes code from MCLK, which is sourced from the fast-starting DCO, code execution begins from PUC in less than 5 µs.

The frequency of DCOCLK is set by the following functions:

- The three DCORSEL bits select one of eight nominal frequency ranges for the DCO. These ranges are defined for an individual device in the device-specific data sheet.
- The five DCO bits divide the DCO range selected by the DCORSEL bits into 32 frequency steps, separated by approximately 8%.
- The five MOD bits switch between the frequency selected by the DCO bits and the next-higher frequency set by {DCO + 1}. When DCO = {31}, the MOD bits have no effect, because the DCO is already at the highest setting for the selected DCORSEL range.

5.2.7 Frequency Locked Loop (FLL)

The FLL continuously counts up or down a frequency integrator. The output of the frequency integrator that drives the DCO can be read in UCSCTL0, UCSCTL1 (bits MOD and DCO). The count is adjusted +1 with the frequency $f_{FLLREFCLK}/n$ (n = 1, 2, 4, 8, 12, or 16) or –1 with the frequency $f_{DCOCLK}/[D \times (N+1)]$.

NOTE: Reading MOD and DCO bits

The integrator is updated via the DCOCLK, which may differ in frequency of operation of MCLK. It is possible that immediate reads of a previously written value are not visible to the user since the update to the integrator has not occurred. This is normal. Once the integrator is updated at the next successive DCOCLK, the correct value can be read.

In addition, since the MCLK can be asynchronous to the integrator updates, reading the values may be cause a corrupted value to be read under this condition. In this case, a majority vote method should be performed.

Five of the integrator bits (UCSCTL0 bits 12 to 8) set the DCO frequency tap. Thirty-two taps are implemented for the DCO, and each is approximately 8% higher than the previous. The modulator mixes two adjacent DCO frequencies to produce fractional taps.

For a given DCO bias range setting, time must be allowed for the DCO to settle on the proper tap for normal operation. $(n \times 32)$ $f_{FLLREFCLK}$ cycles are required between taps requiring a worst case of $(n \times 32 \times 32)$ $f_{FLLREFCLK}$ cycles for the DCO to settle. The value n is defined by the FLLREFDIV bits (n = 1, 2, 4, 8, 12, or 16).

5.2.8 DCO Modulator

The modulator mixes two DCO frequencies, f_{DCO} and $f_{DCO}+1$ to produce an intermediate effective frequency between f_{DCO} and $f_{DCO}+1$ and spread the clock energy, reducing electromagnetic interference (EMI). The modulator mixes f_{DCO} and $f_{DCO}+1$ for 32 DCOCLK clock cycles and is configured with the MOD bits. When MOD = {0}, the modulator is off.

The modulator mixing formula is:

$t = (32 - MOD) \times t_{DCO} + MOD \times t_{DCO+1}$

Figure 5-2 shows the modulator operation.

When FLL operation is enabled, the modulator settings and DCO are controlled by the FLL hardware. If FLL operation is not desired, the modulator settings and DCO control can be configured with software.

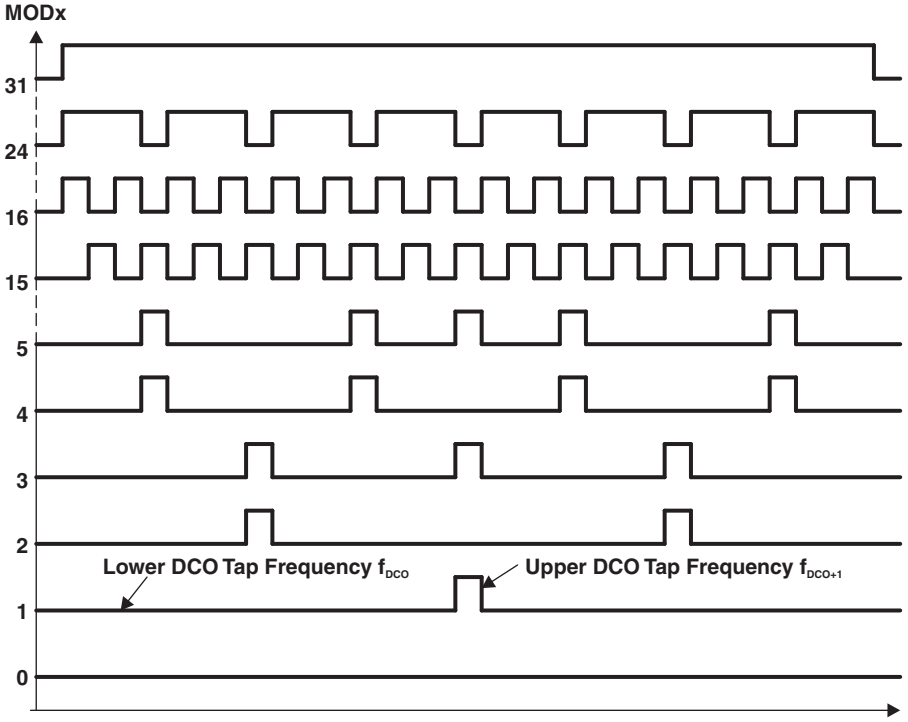

Figure 5-2. Modulator Patterns

5.2.9 Disabling FLL Hardware and Modulator

The FLL is disabled when the status register bits SCG0 or SCG1 are set. When the FLL is disabled, the DCO runs at the previously selected tap and DCOCLK is not automatically stabilized.

The DCO modulator is disabled when DISMOD is set. When the DCO modulator is disabled, the DCOCLK is adjusted to the DCO tap selected by the DCO bits.

NOTE: DCO operation without FLL

When the FLL operation is disabled, the DCO continues to operate at the current settings. Because it is not stabilized by the FLL, temperature and voltage variations influence the frequency of operation. See the device-specific data sheet for voltage and temperature coefficients to ensure reliable operation.

5.2.10 FLL Operation From Low-Power Modes

An interrupt service request clears SCG1, CPUOFF, and OSCOFF if set, but does not clear SCG0. This means that for FLL operation from within an interrupt service routine entered from LPM1, 3, or 4, the FLL remains disabled and the DCO operates at the previous setting as defined in UCSCTL0 and UCSCTL1. SCG0 can be cleared by user software if FLL operation is required.

5.2.11 Operation From Low-Power Modes, Requested by Peripheral Modules

A peripheral module requests its clock sources automatically from the UCS module if required for its proper operation, regardless of the current mode of operation, as shown in Figure 5-3.

A peripheral module asserts one of three possible clock request signals based on its control bits: ACLK_REQ, MCLK_REQ, or SMCLK_REQ. These request signals are based on the configuration and clock selection of the respective module. For example, if a timer selects ACLK as its clock source and the timer is enabled, the timer generates an ACLK_REQ signal to the UCS system. The UCS, in turn, enables ACLK regardless of the LPM settings.

Any clock request from a peripheral module causes its respective clock off signal to be overridden, but does not change the setting of clock off control bit. For example, a peripheral module may require ACLK that is currently disabled by the OSCOFF bit (OSCOFF = 1). The module can request ACLK by generating an ACLK_REQ. This causes the OSCOFF bit to have no effect, thereby allowing ACLK to be available to the requesting peripheral module. The OSCOFF bit remains at its current setting (OSCOFF = 1).

If the requested source is not active, the software NMI handler must take care of the required actions. For the previous example, if ACLK was sourced by XT1 and XT1 was not enabled, an oscillator fault condition occurs and the software must handle the event. The watchdog, due to its security requirement, actively selects the VLOCLK source if the originally selected clock source is not available.

Due to the clock request feature, care must be taken in the application when entering low-power modes to save power. Although the device enters the selected low-power mode, a clock request may exhibit more current consumption than the specified values in the data sheet.

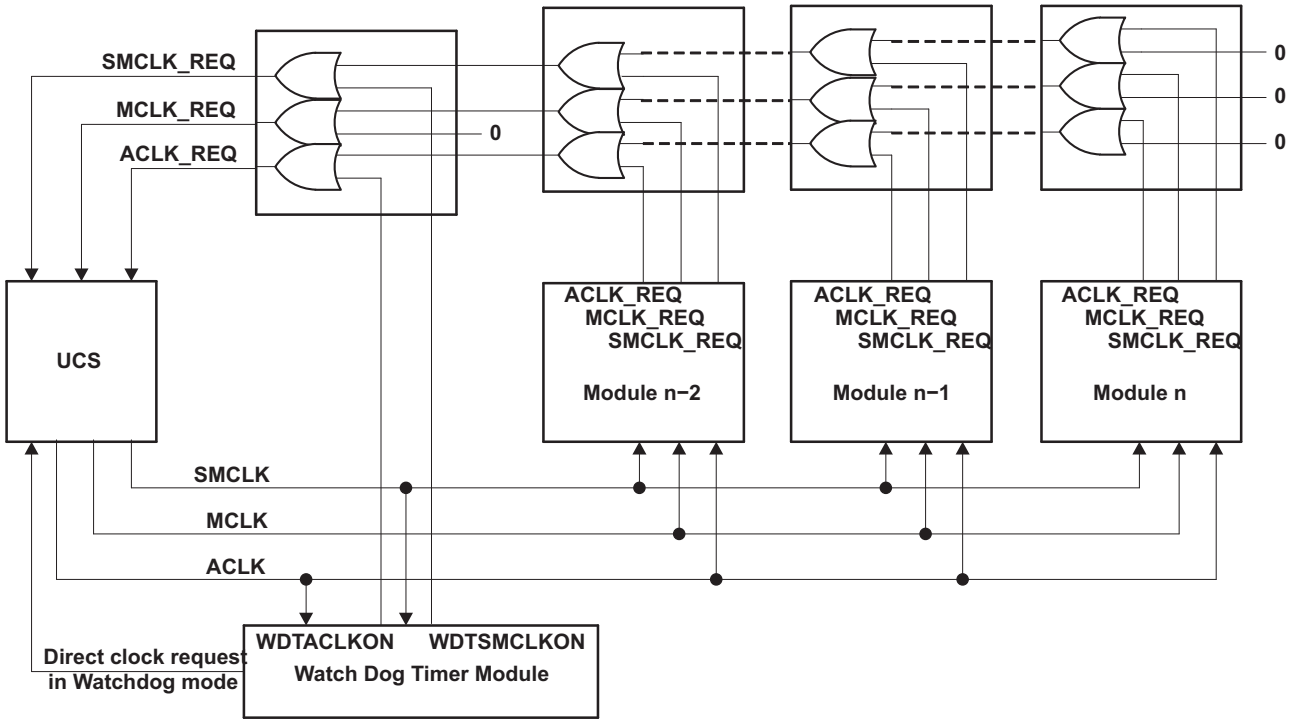

Figure 5-3. Module Request Clock System

By default, the clock request logic is enabled. The clock request logic can be disabled by clearing ACLKREQEN, MCLKREQEN, or SMCLKREQEN, for each respective system clock. When ACLKREQEN or MCLKREQEN bits are set, or active, the clock is available to the system and prevents entry into a low-power mode until all modules requesting the clock are disabled. When ACLKREQEN or MCLKREQEN bits are cleared, or disabled, the clock is always halted as defined by the low-power modes. The SMCLKREQEN logic behaves similarly, but is also influenced by the SMCLKOFF bit in the UCSCTL6 register.Table 5-1 shows the relationship between the system clocks and the low-power modes in conjunction with the clock request logic.

Table 5-1. Clock Request System and Power Modes

Mode	ACLK		MCLK		SMCLK			
					SMCLKOFF = 0		SMCLKOFF = 1	
	ACLKREQEN = 0	ACLKREQEN = 1	MCLKREQEN = 0	MCLKREQEN = 1	SMCLKREQEN = 0	SMCLKREQEN = 1	SMCLKREQEN = 0	SMCLKREQEN = 1
AM	Active	Active	Active	Active	Active	Active	Disabled	Active
LPM0	Active	Active	Disabled	Active	Active	Active	Disabled	Active
LPM1	Active	Active	Disabled	Active	Active	Active	Disabled	Active
LPM2	Active	Active	Disabled	Active	Disabled	Active	Disabled	Active
LPM3	Active	Active	Disabled	Active	Disabled	Active	Disabled	Active
LPM4	Disabled	Active	Disabled	Active	Disabled	Active	Disabled	Active
LPM3.5 (1)	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
LPM4.5 (1)	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled

(1) Any clock request prior to entry into LPM3.5 or LPM4.5 is ignored and LPM3.5 or LPM4.5 entry occurs. For the special case when XT1OFF = 0 or XT2OFF = 0, the LPMx.5 request is ignored and the device does not enter LPMx.5.

5.2.12 UCS Module Fail-Safe Operation

The UCS module incorporates an oscillator-fault fail-safe feature. This feature detects an oscillator fault for XT1, DCO, and XT2 as shown in Figure 5-4. The available fault conditions are:

- Low-frequency oscillator fault (XT1LFOFFG) for XT1 in LF mode
- High-frequency oscillator fault (XT1HFOFFG) for XT1 in HF mode
- High-frequency oscillator fault (XT2OFFG) for XT2
- DCO fault flag (DCOFFG) for the DCO

The crystal oscillator fault bits XT1LFOFFG, XT1HFOFFG, and XT2OFFG are set if the corresponding crystal oscillator is turned on and not operating properly. Once set, the fault bits remain set until reset in software, regardless if the fault condition no longer exists. If the user clears the fault bits and the fault condition still exists, the fault bits are automatically set, otherwise they remain cleared.

When using XT1 operation in LF mode as the reference source into the FLL (SELREF = {0}), a crystal fault automatically causes the FLL reference source, FLLREFCLK, to be sourced by the REFO. XT1LFOFFG is set. When using XT1 operation in HF mode as the reference source into the FLL, a crystal fault causes no FLLREFCLK signal to be generated and the FLL continues to count down to zero in an attempt to lock FLLREFCLK and DCOCLK/[D × (N + 1)]. The DCO tap moves to the lowest position (DCO are cleared) and the DCOFFG is set. DCOFFG is also set if the N-multiplier value is set too high for the selected DCO frequency range, resulting in the DCO tap moving to the highest position (UCSCTL0.12 to UCSCTL0.8 are set). The DCOFFG remains set until cleared by the user. If the user clears the DCOFFG and the fault condition remains, it is automatically set, otherwise it remains cleared. XT1HFOFFG is set.

When using XT2 as the reference source into the FLL, a crystal fault causes no FLLREFCLK signal to be generated, and the FLL continues to count down to zero in an attempt to lock FLLREFCLK and DCOCLK/[D × (N + 1)]. The DCO tap moves to the lowest position (DCO are cleared) and the DCOFFG is set. DCOFFG is also set if the N-multiplier value is set too high for the selected DCO frequency range, resulting in the DCO tap moving to the highest position (UCSCTL0.12 to UCSCTL0.8 are set). The DCOFFG remains set until cleared by the user. If the user clears the DCOFFG and the fault condition remains, it is automatically set, otherwise it remains cleared. XT2OFFG is set.

The OFIFG oscillator-fault interrupt flag is set and latched at POR or when any oscillator fault (XT1LFOFFG, XT1HFOFFG, XT2OFFG, or DCOFFG) is detected. When OFIFG is set and OFIE is set, the OFIFG requests an NMI. When the interrupt is granted, the OFIE is not reset automatically as it is in previous MSP430 families. It is no longer required to reset the OFIE. NMI entry and exit circuitry removes this requirement. The OFIFG flag must be cleared by software. The source of the fault can be identified by checking the individual fault bits.

If a fault is detected for the oscillator sourcing MCLK, MCLK is automatically switched to the DCO for its clock source (DCOCLKDIV) for all clock sources except XT1 LF mode. If MCLK is sourced from XT1 in LF mode, an oscillator fault causes MCLK to be automatically switched to the REFO for its clock source (REFOCLK). This does not change the SELM bit settings. This condition must be handled by user software.

If a fault is detected for the oscillator sourcing SMCLK, SMCLK is automatically switched to the DCO for its clock source (DCOCLKDIV) for all clock sources except XT1 LF mode. If SMCLK is sourced from XT1 in LF mode, an oscillator fault causes SMCLK to be automatically switched to the REFO for its clock source (REFOCLK). This does not change the SELS bit settings. This condition must be handled by user software.

If a fault is detected for the oscillator sourcing ACLK, ACLK is automatically switched to the DCO for its clock source (DCOCLKDIV) for all clock sources except XT1 LF mode. If ACLK is sourced from XT1 in LF mode, an oscillator fault causes ACLK to be automatically switched to the REFO for its clock source (REFOCLK). This does not change the SELA bit settings. This condition must be handled by user software.

NOTE: DCO active during oscillator fault

DCOCLKDIV is active even at the lowest DCO tap. The clock signal is available for the CPU to execute code and service an NMI during an oscillator fault.

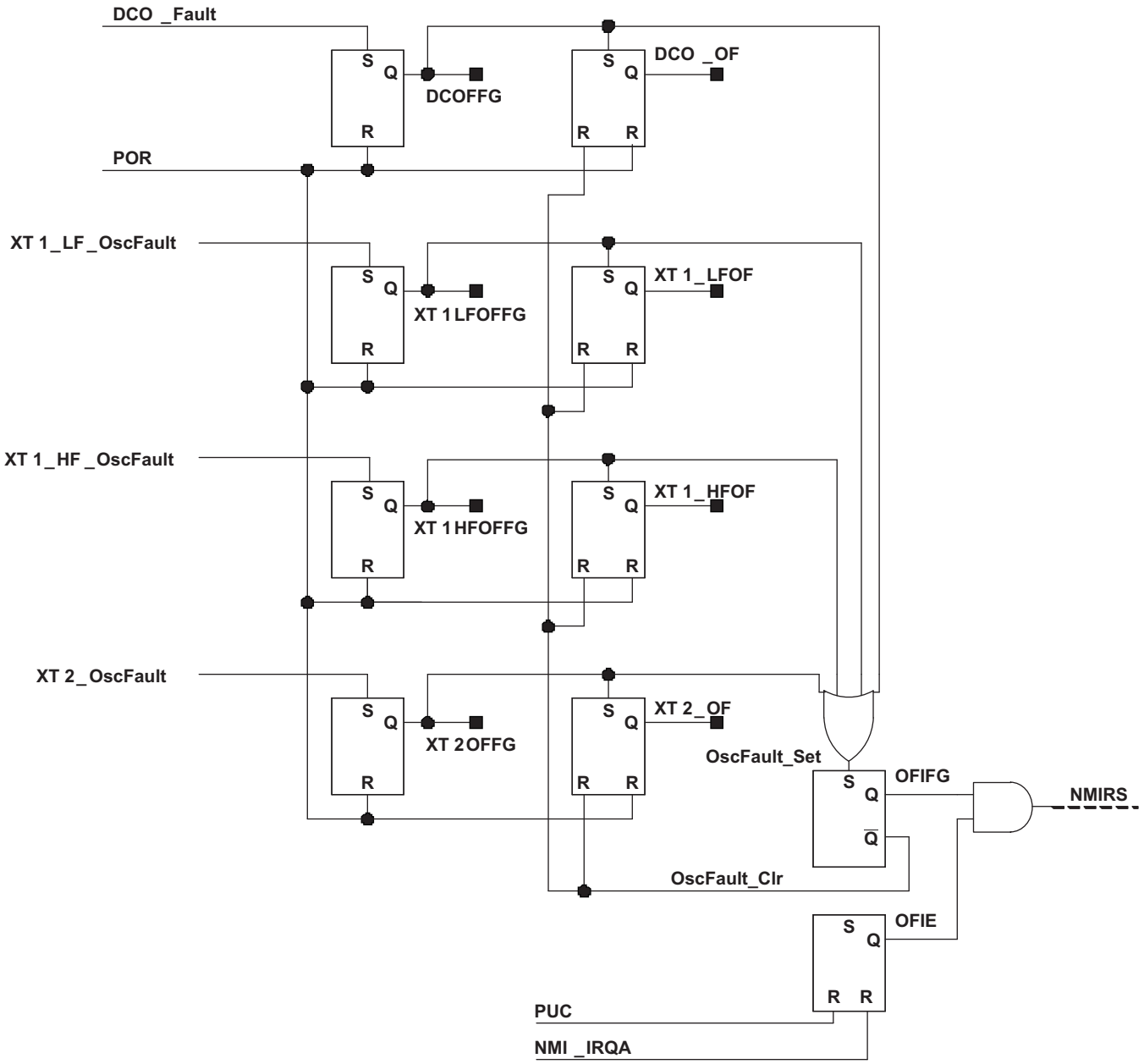

Figure 5-4. Oscillator Fault Logic

NOTE: Fault conditions

DCO_Fault: DCOFFG is set if DCO bits in UCSCTL0 register value equals {0} or {31}.

XT1_LF_OscFault: This signal is set after the XT1 (LF mode) oscillator has stopped operation and cleared after operation resumes. The fault condition causes XT1LFOFFG to be set and remain set. If the user clears XT1LFOFFG and the fault condition still exists, XT1LFOFFG remains set.

XT1_HF_OscFault: This signal is set after the XT1 (HF mode) oscillator has stopped operation and cleared after operation resumes. The fault condition causes XT1HFOFFG to be set and remain set. If the user clears XT1HFOFFG and the fault condition still exists, XT1HFOFFG remains set.

XT2_OscFault: This signal is set after the XT2 oscillator has stopped operation and cleared after operation resumes. The fault condition causes XT2OFFG to be set and remain set. If the user clears XT2OFFG and the fault condition still exists, XT2OFFG remains set.

NOTE: Fault logic

Please note that as long as a fault condition still exists, the OFIFG remains set. The application must take special care when clearing the OFIFG signal. If no fault condition remains when the OFIFG signal is cleared, the clock logic switches back to the original user settings prior to the fault condition.

NOTE: Fault logic counters

Each crystal oscillator circuit has hardware counters. These counters are reset each time a fault condition occurs on its respective oscillator, causing the fault flag to be set. The counters begin to count after the fault condition is removed. Once the maximum count is reached, the fault flag is removed.

In XT1 LF mode, the maximum count is 8192. In XT1 HF mode (and XT2 when available), the maximum count is 1024. In bypass modes, regardless of LF or HF settings, the maximum count is 8192.

5.2.13 Synchronization of Clock Signals

When switching MCLK or SMCLK from one clock source to the another, the switch is synchronized to avoid critical race conditions as shown in Figure 5-5:

- The current clock cycle continues until the next rising edge.
- The clock remains high until the next rising edge of the new clock.
- The new clock source is selected and continues with a full high period.

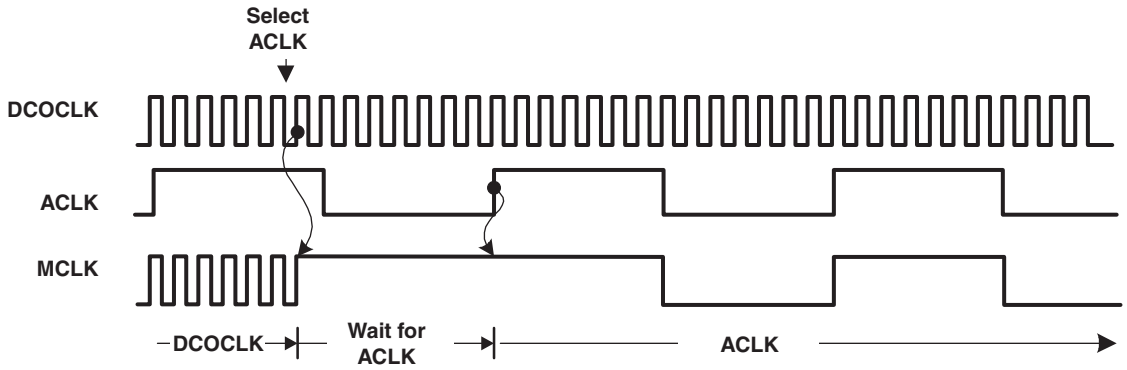

Figure 5-5. Switch MCLK from DCOCLK to XT1CLK

5.3 Module Oscillator (MODOSC)

The UCS module also supports an internal oscillator, MODOSC, that is used by the flash memory controller module and, optionally, by other modules in the system. The MODOSC sources MODCLK.

5.3.1 MODOSC Operation

To conserve power, MODOSC is powered down when not needed and enabled only when required. When the MODOSC source is required, the respective module requests it. MODOSC is enabled based on unconditional and conditional requests. Setting MODOSCREQEN enables conditional requests. Unconditional requests are always enabled. It is not necessary to set MODOSCREQEN for modules that use unconditional requests; for example, flash controller or ADC12_A.

The flash memory controller only requires MODCLK when performing write or erase operations. When performing such operations, the flash memory controller issues an unconditional request for the MODOSC source. Upon doing so, the MODOSC source is enabled, if not already enabled from other modules' previous requests.

The ADC12_A may optionally use MODOSC as a clock source for its conversion clock. The user chooses the ADC12OSC as the conversion clock source. During a conversion, the ADC12_A module issues an unconditional request for the ADC12OSC clock source. Upon doing so, the MODOSC source is enabled, if not already enabled from other modules' previous requests.

5.4 UCS Module Registers

The UCS module registers are listed in Table 5-2. The base address can be found in the device-specific data sheet. The address offset is listed in Table 5-2.

NOTE: All registers have word or byte register access. For a generic register *ANYREG*, the suffix "_L" (*ANYREG_L*) refers to the lower byte of the register (bits 0 through 7). The suffix "_H" (*ANYREG_H*) refers to the upper byte of the register (bits 8 through 15).

Table 5-2. UCS Registers

Offset	Acronym	Register Name	Type	Access	Reset	Section
00h	UCSCTL0	Unified Clock System Control 0	Read/write	Word	0000h	Section 5.4.1
00h	UCSCTL0_L		Read/write	Byte	00h	
01h	UCSCTL0_H		Read/write	Byte	00h	
02h	UCSCTL1	Unified Clock System Control 1	Read/write	Word	0020h	Section 5.4.2
02h	UCSCTL1_L		Read/write	Byte	20h	
03h	UCSCTL1_H		Read/write	Byte	00h	
04h	UCSCTL2	Unified Clock System Control 2	Read/write	Word	101Fh	Section 5.4.3
04h	UCSCTL2_L		Read/write	Byte	1Fh	
05h	UCSCTL2_H		Read/write	Byte	10h	
06h	UCSCTL3	Unified Clock System Control 3	Read/write	Word	0000h	Section 5.4.4
06h	UCSCTL3_L		Read/write	Byte	00h	
07h	UCSCTL3_H		Read/write	Byte	00h	
08h	UCSCTL4	Unified Clock System Control 4	Read/write	Word	0044h	Section 5.4.5
08h	UCSCTL4_L		Read/write	Byte	44h	
09h	UCSCTL4_H		Read/write	Byte	00h	
0Ah	UCSCTL5	Unified Clock System Control 5	Read/write	Word	0000h	Section 5.4.6
0Ah	UCSCTL5_L		Read/write	Byte	00h	
0Bh	UCSCTL5_H		Read/write	Byte	00h	
0Ch	UCSCTL6	Unified Clock System Control 6	Read/write	Word	C1CDh	Section 5.4.7
0Ch	UCSCTL6_L		Read/write	Byte	CDh	
0Dh	UCSCTL6_H		Read/write	Byte	C1h	
0Eh	UCSCTL7	Unified Clock System Control 7	Read/write	Word	0703h	Section 5.4.8
0Eh	UCSCTL7_L		Read/write	Byte	03h	
0Fh	UCSCTL7_H		Read/write	Byte	07h	
10h	UCSCTL8	Unified Clock System Control 8	Read/write	Word	0707h	Section 5.4.9
10h	UCSCTL8_L		Read/write	Byte	07h	
11h	UCSCTL8_H		Read/write	Byte	07h	
12h	UCSCTL9	Unified Clock System Control 9[(1)]	Read/write	Word	0000h	Section 5.4.10
12h	UCSCTL9_L		Read/write	Byte	00h	
13h	UCSCTL9_H		Read/write	Byte	00h	

(1) This register is not available on all devices. See the device-specific data sheet.

5.4.1 UCSCTL0 Register

Unified Clock System Control 0 Register

Figure 5-6. UCSCTL0 Register

15	14	13	12	11	10	9	8
Reserved			DCO				
r0	r0	r0	rw-0	rw-0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
MOD					Reserved		
rw-0	rw-0	rw-0	rw-0	rw-0	r0	r0	r0

Table 5-3. UCSCTL0 Register Description

Bit	Field	Type	Reset	Description
15-13	Reserved	R	0h	Reserved. Always reads as 0.
12-8	DCO	RW	0h	DCO tap selection. These bits select the DCO tap and are modified automatically during FLL operation.
7-3	MOD	RW	0h	Modulation bit counter. These bits select the modulation pattern. All MOD bits are modified automatically during FLL operation. The DCO register value is incremented when the modulation bit counter rolls over from 31 to 0. If the modulation bit counter decrements from 0 to the maximum count, the DCO register value is also decremented.
2-0	Reserved	R	0h	Reserved. Always reads as 0.

5.4.2 UCSCTL1 Register

Unified Clock System Control 1 Register

Figure 5-7. UCSCTL1 Register

15	14	13	12	11	10	9	8
Reserved							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
Reserved	DCORSEL			Reserved		Reserved	DISMOD
r0	rw-0	rw-1	rw-0	r0	r0	rw-0	rw-0

Table 5-4. UCSCTL1 Register Description

Bit	Field	Type	Reset	Description
15-7	Reserved	R	0h	Reserved. Always reads as 0.
6-4	DCORSEL	RW	2h	DCO frequency range select. These bits select the DCO frequency range of operation defined in the device-specific datasheet.
3-2	Reserved	R	0h	Reserved. Always reads as 0.
1	Reserved	RW	0h	Reserved. Always reads as 0.
0	DISMOD	RW	0h	Modulation. This bit enables or disables the modulation. 0b = Modulation enabled 1b = Modulation disabled

5.4.3 UCSCTL2 Register

Unified Clock System Control 2 Register

Figure 5-8. UCSCTL2 Register

15	14	13	12	11	10	9	8
Reserved	FLLD			Reserved		FLLN	
r0	rw-0	rw-0	rw-1	r0	r0	rw-0	rw-0
7	6	5	4	3	2	1	0
FLLN							
rw-0	rw-0	rw-0	rw-1	rw-1	rw-1	rw-1	rw-1

Table 5-5. UCSCTL2 Register Description

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	Reserved. Always reads as 0.
14-12	FLLD	RW	1h	FLL loop divider. These bits divide f(DCOCLK) in the FLL feedback loop. This results in an additional multiplier for the multiplier bits. See also multiplier bits. 000b = f(DCOCLK)/1 001b = f(DCOCLK)/2 010b = f(DCOCLK)/4 011b = f(DCOCLK)/8 100b = f(DCOCLK)/16 101b = f(DCOCLK)/32 110b = Reserved for future use. Defaults to f(DCOCLK)/32. 111b = Reserved for future use. Defaults to f(DCOCLK)/32.
11-10	Reserved	R	0h	Reserved. Always reads as 0.
9-0	FLLN	RW	1Fh	Multiplier bits. These bits set the multiplier value N of the DCO. N must be greater than 0. Writing zero to FLLN causes N to be set to 1.

5.4.4 UCSCTL3 Register

Unified Clock System Control 3 Register

Figure 5-9. UCSCTL3 Register

15	14	13	12	11	10	9	8
Reserved							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
Reserved	SELREF			Reserved	FLLREFDIV		
r0	rw-0	rw-0	rw-0	r0	rw-0	rw-0	rw-0

Table 5-6. UCSCTL3 Register Description

Bit	Field	Type	Reset	Description
15-7	Reserved	R	0h	Reserved. Always reads as 0.
6-4	SELREF	RW	0h	FLL reference select. These bits select the FLL reference clock source. 000b = XT1CLK 001b = Reserved for future use. Defaults to XT1CLK. 010b = REFOCLK 011b = Reserved for future use. Defaults to REFOCLK. 100b = Reserved for future use. Defaults to REFOCLK. 101b = XT2CLK when available, otherwise REFOCLK. 110b = Reserved for future use. XT2CLK when available, otherwise REFOCLK. 111b = Reserved for future use. XT2CLK when available, otherwise REFOCLK.
3	Reserved	R	0h	Reserved. Always reads as 0.
2-0	FLLREFDIV	RW	0h	FLL reference divider. These bits define the divide factor for f(FLLREFCLK). The divided frequency is used as the FLL reference frequency. 000b = f(FLLREFCLK)/1 001b = f(FLLREFCLK)/2 010b = f(FLLREFCLK)/4 011b = f(FLLREFCLK)/8 100b = f(FLLREFCLK)/12 101b = f(FLLREFCLK)/16 110b = Reserved for future use. Defaults to f(FLLREFCLK)/16. 111b = Reserved for future use. Defaults to f(FLLREFCLK)/16.

5.4.5 UCSCTL4 Register

Unified Clock System Control 4 Register

Figure 5-10. UCSCTL4 Register

15	14	13	12	11	10	9	8
Reserved					SELA		
r0	r0	r0	r0	r0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
Reserved	SELS			Reserved	SELM		
r0	rw-1	rw-0	rw-0	r0	rw-1	rw-0	rw-0

Table 5-7. UCSCTL4 Register Description

Bit	Field	Type	Reset	Description
15-11	Reserved	R	0h	Reserved. Always reads as 0.
10-8	SELA	RW	0h	Selects the ACLK source 000b = XT1CLK 001b = VLOCLK 010b = REFOCLK 011b = DCOCLK 100b = DCOCLKDIV 101b = XT2CLK when available, otherwise DCOCLKDIV 110b = Reserved for future use. Defaults to XT2CLK when available, otherwise DCOCLKDIV. 111b = Reserved for future use. Defaults to XT2CLK when available, otherwise DCOCLKDIV.
7	Reserved	R	0h	Reserved. Always reads as 0.
6-4	SELS	RW	4h	Selects the SMCLK source 000b = XT1CLK 001b = VLOCLK 010b = REFOCLK 011b = DCOCLK 100b = DCOCLKDIV 101b = XT2CLK when available, otherwise DCOCLKDIV 110b = Reserved for future use. Defaults to XT2CLK when available, otherwise DCOCLKDIV. 111b = Reserved for future use. Defaults to XT2CLK when available, otherwise DCOCLKDIV.
3	Reserved	R	0h	Reserved. Always reads as 0.
2-0	SELM	RW	4h	Selects the MCLK source 000b = XT1CLK 001b = VLOCLK 010b = REFOCLK 011b = DCOCLK 100b = DCOCLKDIV 101b = XT2CLK when available, otherwise DCOCLKDIV 110b = Reserved for future use. Defaults to XT2CLK when available, otherwise DCOCLKDIV. 111b = Reserved for future use. Defaults to XT2CLK when available, otherwise DCOCLKDIV.

5.4.6 UCSCTL5 Register

Unified Clock System Control 5 Register

Figure 5-11. UCSCTL5 Register

15	14	13	12	11	10	9	8
Reserved	DIVPA			Reserved	DIVA		
r0	rw-0	rw-0	rw-0	r0	rw-0	rw-0	rw-0
7	6	5	4	3	2	1	0
Reserved	DIVS			Reserved	DIVM		
r0	rw-0	rw-0	rw-0	r0	rw-0	rw-0	rw-0

Table 5-8. UCSCTL5 Register Description

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	Reserved. Always reads as 0.
14-12	DIVPA	RW	0h	ACLK source divider available at external pin. Divides the frequency of ACLK and presents it to an external pin. 000b = f(ACLK)/1 001b = f(ACLK)/2 010b = f(ACLK)/4 011b = f(ACLK)/8 100b = f(ACLK)/16 101b = f(ACLK)/32 110b = Reserved for future use. Defaults to f(ACLK)/32. 111b = Reserved for future use. Defaults to f(ACLK)/32.
11	Reserved	R	0h	Reserved. Always reads as 0.
10-8	DIVA	RW	0h	ACLK source divider. Divides the frequency of the ACLK clock source. 000b = f(ACLK)/1 001b = f(ACLK)/2 010b = f(ACLK)/4 011b = f(ACLK)/8 100b = f(ACLK)/16 101b = f(ACLK)/32 110b = Reserved for future use. Defaults to f(ACLK)/32. 111b = Reserved for future use. Defaults to f(ACLK)/32.
7	Reserved	R	0h	Reserved. Always reads as 0.
6-4	DIVS	RW	0h	SMCLK source divider 000b = f(SMCLK)/1 001b = f(SMCLK)/2 010b = f(SMCLK)/4 011b = f(SMCLK)/8 100b = f(SMCLK)/16 101b = f(SMCLK)/32 110b = Reserved for future use. Defaults to f(SMCLK)/32. 111b = Reserved for future use. Defaults to f(SMCLK)/32.
3	Reserved	R	0h	Reserved. Always reads as 0.

Table 5-8. UCSCTL5 Register Description (continued)

Bit	Field	Type	Reset	Description
2-0	DIVM	RW	0h	MCLK source divider 000b = f(MCLK)/1 001b = f(MCLK)/2 010b = f(MCLK)/4 011b = f(MCLK)/8 100b = f(MCLK)/16 101b = f(MCLK)/32 110b = Reserved for future use. Defaults to f(MCLK)/32. 111b = Reserved for future use. Defaults to f(MCLK)/32.

5.4.7 UCSCTL6 Register

Unified Clock System Control 6 Register

Figure 5-12. UCSCTL6 Register

15	14	13	12	11	10	9	8
XT2DRIVE		Reserved	XT2BYPASS	Reserved			XT2OFF
rw-1	rw-1	r0	rw-0	r0	r0	r0	rw-1
7	6	5	4	3	2	1	0
XT1DRIVE		XTS	XT1BYPASS	XCAP		SMCLKOFF	XT1OFF
rw-1	rw-1	rw-0	rw-0	rw-1	rw-1	rw-0	rw-1

Table 5-9. UCSCTL6 Register Description

Bit	Field	Type	Reset	Description
15-14	XT2DRIVE	RW	3h	The XT2 oscillator current can be adjusted to its drive needs. Initially, it starts with the highest supply current for reliable and quick startup. If needed, user software can reduce the drive strength. 00b = Lowest current consumption. XT2 oscillator operating range is 4 MHz to 8 MHz. 01b = Increased drive strength XT2 oscillator. XT2 oscillator operating range is 8 MHz to 16 MHz. 10b = Increased drive capability XT2 oscillator. XT2 oscillator operating range is 16 MHz to 24 MHz. 11b = Maximum drive capability and maximum current consumption for both XT2 oscillator. XT2 oscillator operating range is 24 MHz to 32 MHz.
13	Reserved	R	0h	Reserved. Always reads as 0.
12	XT2BYPASS	RW	0h	XT2 bypass select 0b = XT2 sourced internally 1b = XT2 sourced externally from pin
11-9	Reserved	R	0h	Reserved. Always reads as 0.
8	XT2OFF	RW	1h	Turns off the XT2 oscillator 0b = XT2 is on if XT2 is selected via the port selection and XT2 is not in bypass mode of operation 1b = XT2 is off if it is not used as a source for ACLK, MCLK, or SMCLK or is not used as a reference source required for FLL operation
7-6	XT1DRIVE	RW	3h	The XT1 oscillator current can be adjusted to its drive needs. Initially, it starts with the highest supply current for reliable and quick startup. If needed, user software can reduce the drive strength. 00b = Lowest current consumption for XT1 LF mode. XT1 oscillator operating range in HF mode is 4 MHz to 8 MHz. 01b = Increased drive strength for XT1 LF mode. XT1 oscillator operating range in HF mode is 8 MHz to 16 MHz. 10b = Increased drive capability for XT1 LF mode. XT1 oscillator operating range in HF mode is 16 MHz to 24 MHz. 11b = Maximum drive capability and maximum current consumption for XT1 LF mode. XT1 oscillator operating range in HF mode is 24 MHz to 32 MHz.
5	XTS	RW	0h	XT1 mode select 0b = Low-frequency mode. XCAP bits define the capacitance at the XIN and XOUT pins. 1b = High-frequency mode. XCAP bits are not used.
4	XT1BYPASS	RW	0h	XT1 bypass select 0b = XT1 sourced internally 1b = XT1 sourced externally from pin

Table 5-9. UCSCTL6 Register Description (continued)

Bit	Field	Type	Reset	Description
3-2	XCAP	RW	3h	Oscillator capacitor selection. These bits select the capacitors applied to the LF crystal or resonator in the LF mode (XTS = 0). The effective capacitance (seen by the crystal) is C(eff) ≈ (C(XIN) + 2 pF) / 2. It is assumed that C(XIN) = C(XOUT) and that a parasitic capacitance of 2 pF is added by the package and the printed circuit board. For details about the typical internal and the effective capacitors, see the device-specific data sheet.
1	SMCLKOFF	RW	0h	SMCLK off. This bit turns off the SMCLK. 0b = SMCLK on 1b = SMCLK off
0	XT1OFF	RW	1h	XT1 off. This bit turns off the XT1. 0b = XT1 is on if XT1 is selected via the port selection and XT1 is not in bypass mode of operation. 1b = XT1 is off if it is not used as a source for ACLK, MCLK, or SMCLK or is not used as a reference source required for FLL operation.

5.4.8 UCSCTL7 Register

Unified Clock System Control 7 Register

Figure 5-13. UCSCTL7 Register

15	14	13	12	11	10	9	8
Reserved		Reserved		Reserved		Reserved	
r0	r0	rw-0	rw-(0)	rw-(1)	rw-(1)	r-1	r-1
7	6	5	4	3	2	1	0
Reserved			Reserved	XT2OFFG(1)	XT1HFOFFG(1)	XT1LFOFFG	DCOFFG
r0	r0	r0	rw-(0)	rw-(0)	rw-(0)	rw-(1)	rw-(1)

(1) Not available on all devices. When not available, this bit is reserved.

Table 5-10. UCSCTL7 Register Description

Bit	Field	Type	Reset	Description
15-14	Reserved	R	0h	Reserved. Always reads as 0.
13-12	Reserved	RW	0h	Reserved. Must always be written with 0.
11-10	Reserved	RW	3h	Reserved. The states of these bits should be ignored.
9-8	Reserved	R	3h	Reserved. The states of these bits should be ignored.
7-5	Reserved	R	0h	Reserved. Always reads as 0.
4	Reserved	RW	0h	Reserved. The state of this bit should be ignored.
3	XT2OFFG(1)	RW	0h	XT2 oscillator fault flag. If this bit is set, the OFIFG flag is also set. XT2OFFG is set if a XT2 fault condition exists. XT2OFFG can be cleared via software. If the XT2 fault condition still remains, XT2OFFG is set. 0b = No fault condition occurred after the last reset. 1b = XT2 fault. An XT2 fault occurred after the last reset.
2	XT1HFOFFG(1)	RW	0h	XT1 oscillator fault flag (HF mode). If this bit is set, the OFIFG flag is also set. XT1HFOFFG is set if a XT1 fault condition exists. XT1HFOFFG can be cleared via software. If the XT1 fault condition still remains, XT1HFOFFG is set. 0b = No fault condition occurred after the last reset. 1b = XT1 fault. An XT1 fault occurred after the last reset.
1	XT1LFOFFG	RW	1h	XT1 oscillator fault flag (LF mode). If this bit is set, the OFIFG flag is also set. XT1LFOFFG is set if a XT1 fault condition exists. XT1LFOFFG can be cleared via software. If the XT1 fault condition still remains, XT1LFOFFG is set. 0b = No fault condition occurred after the last reset. 1b = XT1 fault (LF mode). A XT1 fault occurred after the last reset.
0	DCOFFG	RW	1h	DCO fault flag. If this bit is set, the OFIFG flag is also set. The DCOFFG bit is set if DCO = {0} or DCO = {31}. DCOFFG can be cleared via software. If the DCO fault condition still remains, DCOFFG is set. 0b = No fault condition occurred after the last reset. 1b = DCO fault. A DCO fault occurred after the last reset.

(1) Not available on all devices. When not available, this bit is reserved.

5.4.9 UCSCTL8 Register

Unified Clock System Control 8 Register

Figure 5-14. UCSCTL8 Register

15	14	13	12	11	10	9	8
Reserved					Reserved		
r0	r0	r0	r0	r0	rw-(1)	rw-(1)	rw-(1)
7	6	5	4	3	2	1	0
Reserved			Reserved	MODOSCREQEN	SMCLKREQEN	MCLKREQEN	ACLKREQEN
r0	r0	r0	rw-(0)	rw-(0)	rw-(1)	rw-(1)	rw-(1)

Table 5-11. UCSCTL8 Register Description

Bit	Field	Type	Reset	Description
15-11	Reserved	R	0h	Reserved. Always reads as 0.
10-8	Reserved	R	0h	Reserved. Must always be written as 1.
7-5	Reserved	R	0h	Reserved. Always reads as 0.
4	Reserved	R	0h	Reserved. Must always be written as 0.
3	MODOSCREQEN	RW	0h	MODOSC clock request enable. Setting this enables conditional module requests for MODOSC. 0b = MODOSC conditional requests are disabled. 1b = MODOSC conditional requests are enabled.
2	SMCLKREQEN	RW	1h	SMCLK clock request enable. Setting this enables conditional module requests for SMCLK 0b = SMCLK conditional requests are disabled. 1b = SMCLK conditional requests are enabled.
1	MCLKREQEN	RW	1h	MCLK clock request enable. Setting this enables conditional module requests for MCLK 0b = MCLK conditional requests are disabled. 1b = MCLK conditional requests are enabled.
0	ACLKREQEN	RW	1h	ACLK clock request enable. Setting this enables conditional module requests for ACLK 0b = ACLK conditional requests are disabled. 1b = ACLK conditional requests are enabled.

5.4.10 UCSCTL9 Register

Unified Clock System Control 9 Register

This register is not available on all devices. See the device-specific data sheet.

Figure 5-15. UCSCTL9 Register

15	14	13	12	11	10	9	8
Reserved							
r0	r0	r0	r0	r0	r0	r0	r0
7	6	5	4	3	2	1	0
Reserved						XT2BYPASSLV	XT1BYPASSLV
r0	r0	r0	r0	r0	r0	rw-0	rw-0

Table 5-12. UCSCTL9 Register Description

Bit	Field	Type	Reset	Description
15-2	Reserved	R	0h	Reserved. Always reads as 0.
1	XT2BYPASSLV	RW	0h	Selects XT2 bypass input swing level. Must be set for reduced swing operation. 0b = Input range from 0 to DVCC 1b = Input range from 0 to DVIO
0	XT1BYPASSLV	RW	0h	Selects XT1 bypass input swing level. Must be set for reduced swing operation. 0b = Input range from 0 to DVCC 1b = Input range from 0 to DVIO