Arasan
The Bus Stops Here

PRODUCT OVERVIEW

MMC / eMMC Host IP

Features

Compliance
- MMC Specification version 3.31, 4.1, and 4.2
- eMMC / MMC version 4.3
- JESD84 - A43

Card Types Support
- MMCplus
- MMCmobile

Functional Support
- Boot Operation Mode
- Sector address allows host to access high capacity card
- Sleep mode for power saving
- CID register recognizes eMMC or card
- Reliable write definition
- Definition for erase unit and erase timeout for high capacity memory
- 1-bit, 4-bit, and 8-bit bus widths
- CRC7 for command and CRC16 for data
- Temporary and permanent write protection
- Supports card erase, lock, unlock and force erase
- Multiple card mode and SPI mode
- 2GB or more memory size
- Supports block length or sector size of 512 bytes
- Supports error injection
- Incremental burst transfers on DMA mode
- Register transfer on non-DMA mode
- Supports retry and split

System Architecture
- Up to 416 Mbit/s data transfer rate
- 32-bit system bus
- Host clock rate: 0 to 52 MHz

Optional Bus I/F
- AHB bus - 32bit; 300MHz
- PCI or PCIe bus
- Custom bus I/F

Overview

The Arasan MMC / eMMC Host IP is compliant to the MMC3.31, MMC4.1, MMC4.2, and eMMC (MMC4.3) specifications. With the new eMMC solution, a host system can gain access to all major classes of mass storage memory sub-systems; these include embedded memory, memory cards, or hard disk drives with one MMC bus.

Standard MMC features including the support for SPI and MMC-8-bit modes. The controller includes a DMA controller and a FIFO that is expandable from a

MMC / eMMC Host IP

MMC / eMMC Interface:

The MMC / eMMC interface conforms to the MMC system specifications 3.31, 4.1, 4.2 and 4.3. The interface supports 1-bit, 4-bit, and 8-bit MMC modes, Error Correction Code (ECC), MMCplus and MMCmobile card types.

eMMC or MMC 4.3 provides enhanced features to the previous MMC specification:

i. Power-on boot mode allows the master (MMC host) to read boot data from the slave (MMC device).
ii. The explicit sleep mode allows the host to instruct the controller to directly enter sleep mode.
III. Sector address definition allows the host to access high capacity cards
iv. CID register can now differentiate and recognize between eMMC or a card in the system.
v. Definition for erase unit and erase timeout for high capacity memory.
vi. Reliable write definition.

AHB/APB Interface Option:

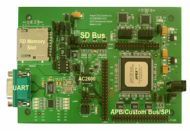
The Arasan MMC / eMMC Host IP provides a programmed I/O method in which various bus interfaces can be implemented. Using the AHB/APB interface, the host driver can transfer data using the Buffer Data Port register. The AHB slave has direct access to the Host Control registers and these registers can be programmed by the ARM processor through the AHB slave interface. Data transactions are performed through the AHB slave interface with Programmed I/O method. The AHB Interface initiates a read or write transaction with the memory if the data transaction is an DMA data transfer.

Custom Interface Option:

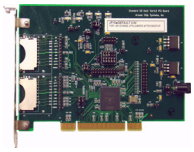
The Arasan MMC / eMMC Host IP provides a programmed I/O method in which various bus interfaces can be implemented. In selecting a PCI interface, a bus interface can be implemented to support a master or target implementation meeting the PCI 2.2 specifications. In addition, the PCIe1.x can also be implemented.

Because of the flexibility of the design, a custom interface can also be implemented to interface natively to any system. General purpose buses such as 8-bit or 16-bit parallel buses are optional modules as well as common bus system like AXI. Custom buses with special requirements can also be implemented.

Host Hardware Validation Platform (HVP):
The HVP is designed for validation and compliance testing of SD host devices .



Host Hardware Development Kit (HDK):
The HDK is a PCI plug-in card for SD host prototyping and driver development.



Benefits:

- Fully compliant core with proven silicon
- Premier direct support from Arasan IP core designers
- Easy-to-use industry standard test environment
- Unencrypted source code allows easy implementation
- ReUse Methodology Manual guidelines (RMM) compliant verilog code ensured using Spyglass

Deliverables:

- RMM Compliant Synthesizable RTL design in Verilog
- Easy-to-use test environment
- Synthesis scripts
- Technical documents

Optional Items:

- MMC / eMMC Host Hardware Validation Platform (HVP)
- MMC / eMMC Device Hardware Development Kit (HDK)

Supported Platforms/Simulators:

- Platforms: Solaris, Unix, Linux and Win XP
- Verilog simulators: Synopsys VCS, Cadence NC-Verilog, MTI ModelSim-Verilog

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Data Sheet Links:

MMC / eMMC Host IP:
http://www.arasan.com/datasheets/login.php

For a complete directory of Arasan IPs, please visit:
www.arasan.com