Chair for Circuit and System Design

Lecture
EDA Tools

Tools, Methods and Algorithms used for Designing Circuits and Systems

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Chair for Circuit and System Design

Introduction

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Objectives

EDA Tools **Lecture**:
Introduction to established methods, tools and languages used in different areas of IC Design

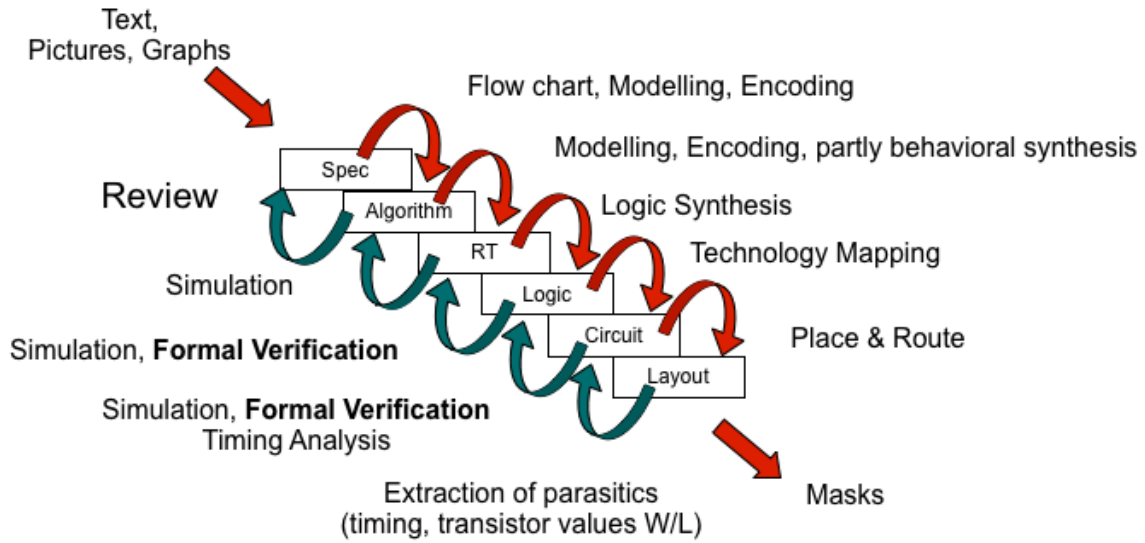
What does EDA stand for?

- Electronic Design Automation

IC Design (Overview):

- **Specification**
- **Design**
- **Verification**
- Layout, Manufacturing, Test
- Validation

Certain tools and methods exist for each step.



Chair for Circuit and System Design

Introduction
-
Transistor History

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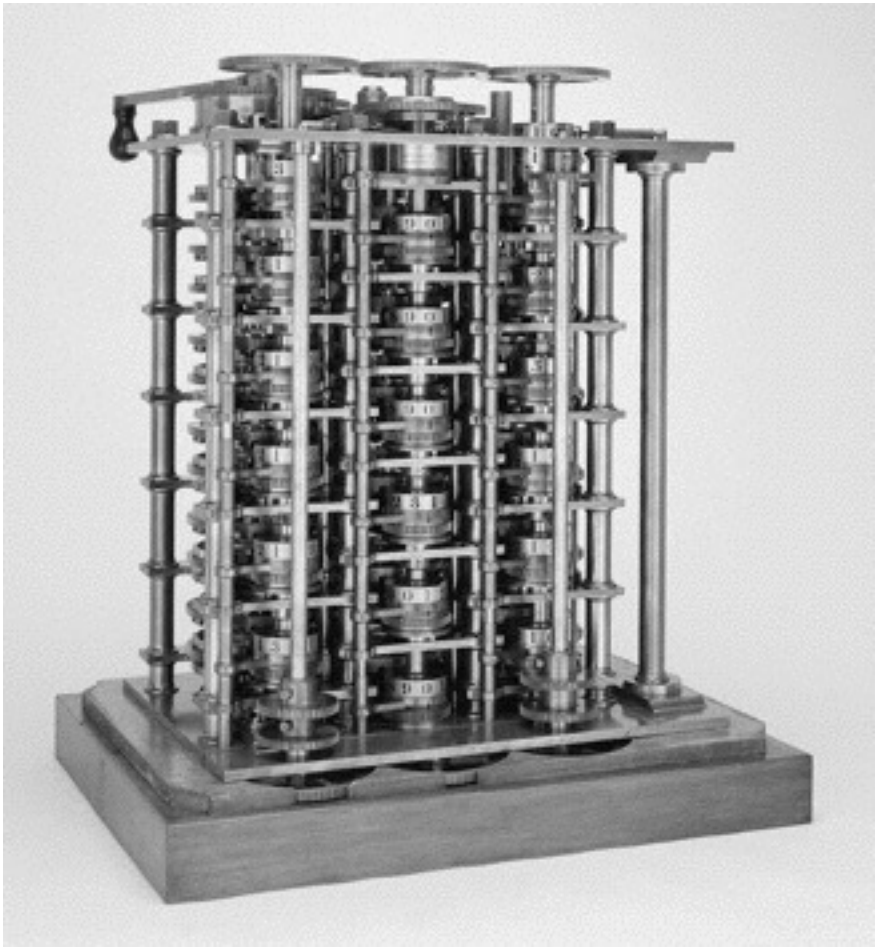
The First Computer

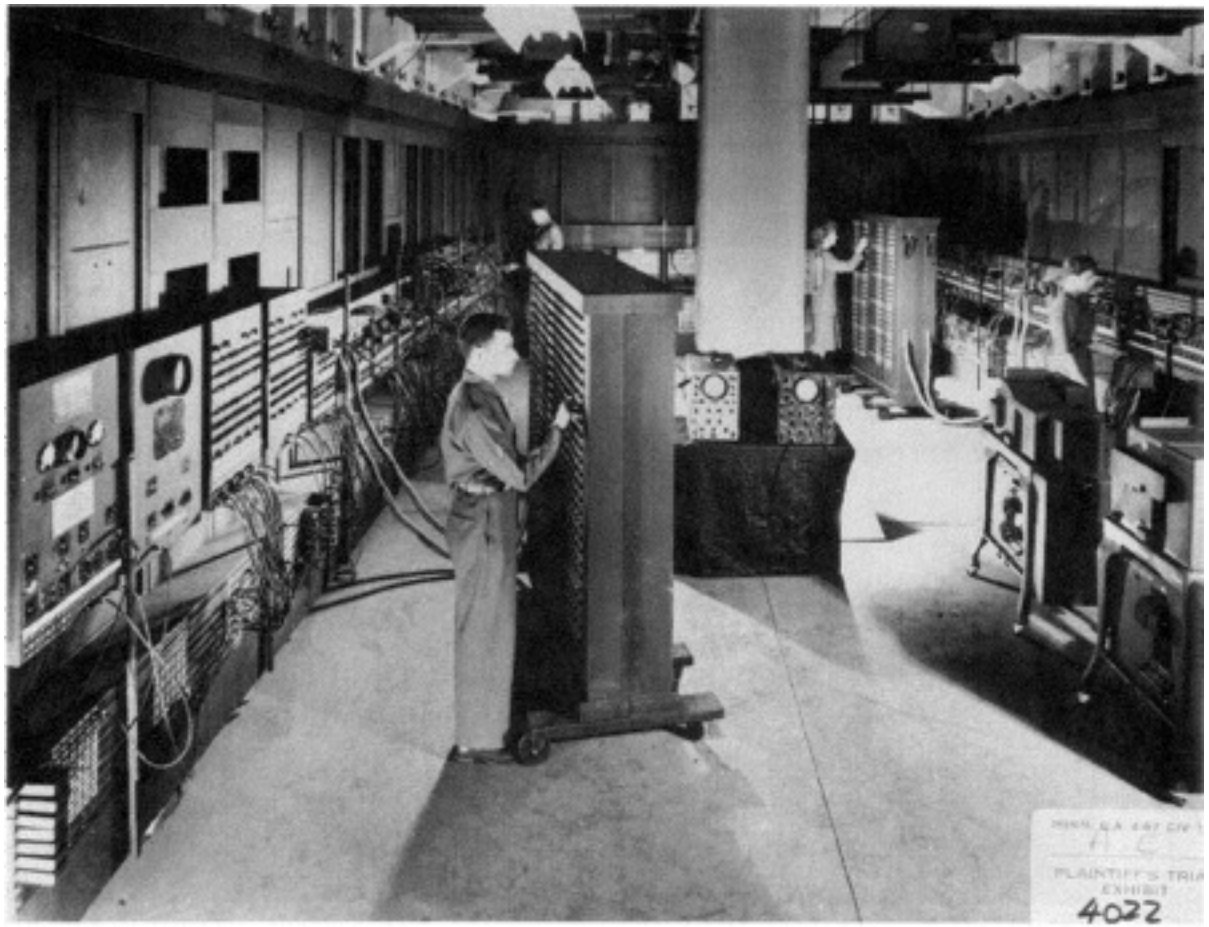


The Babbage Difference Engine (1832)

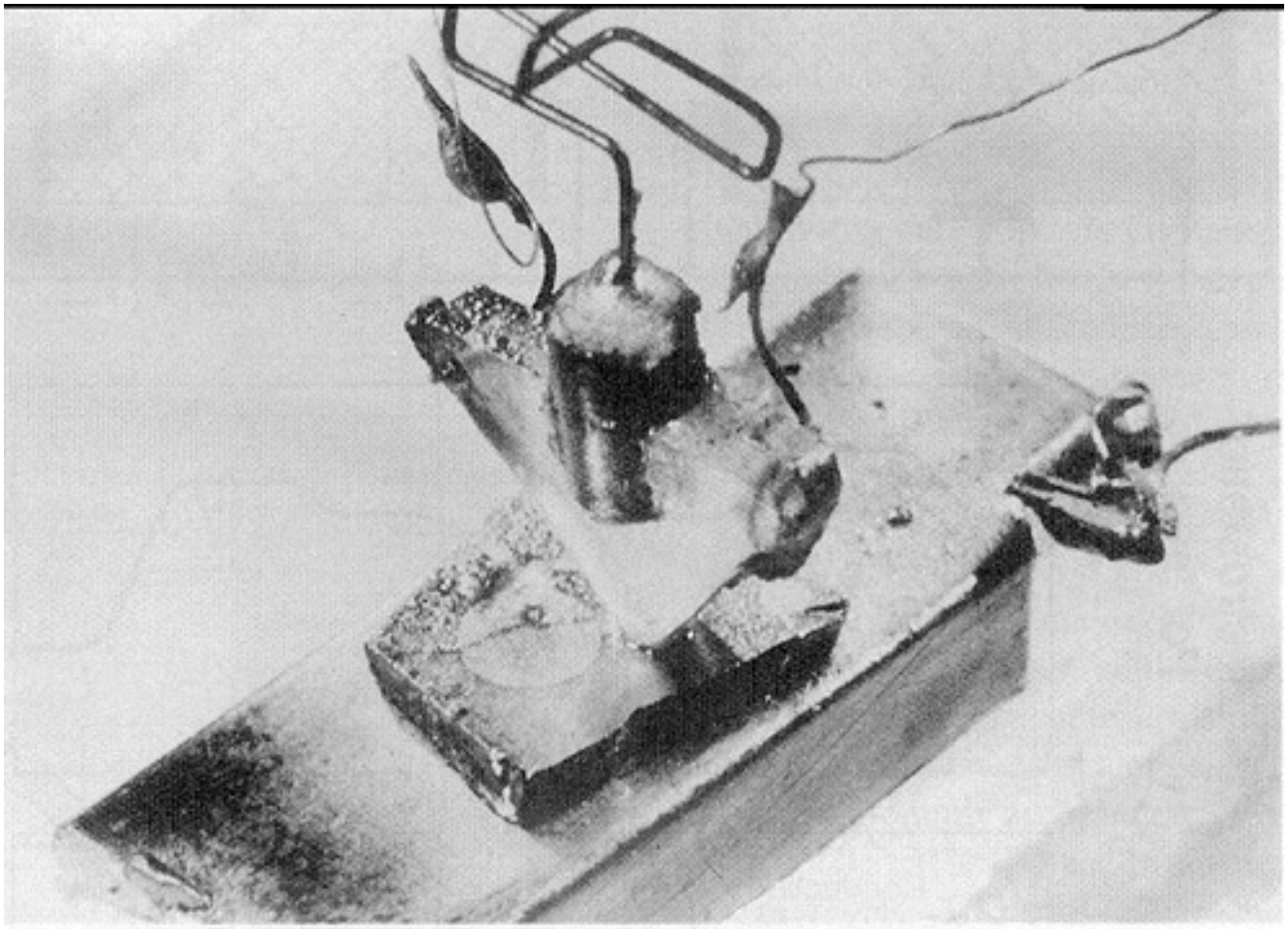
25,000 parts

cost: £17,470

ENIAC - The _first_ electronic computer (1946)

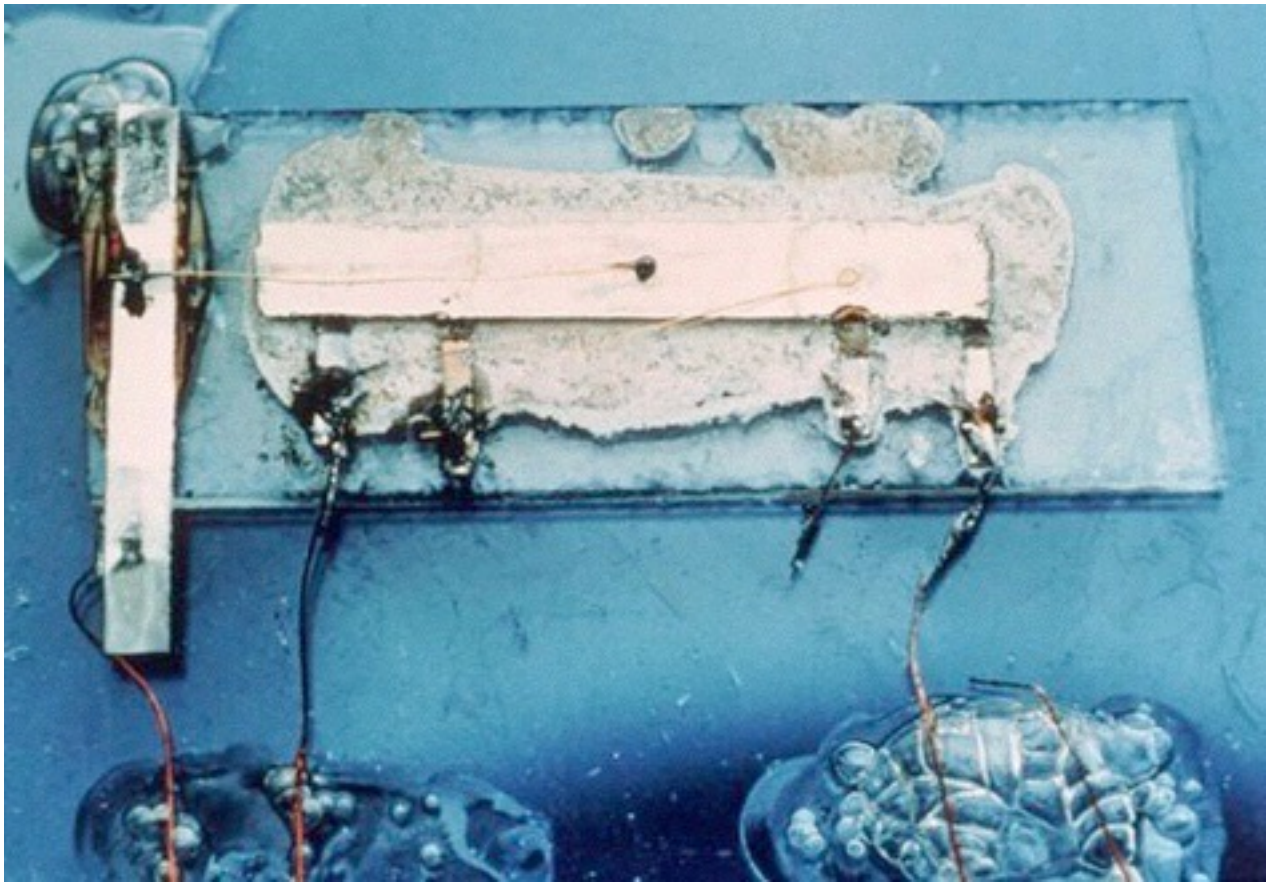


The Transistor Revolution



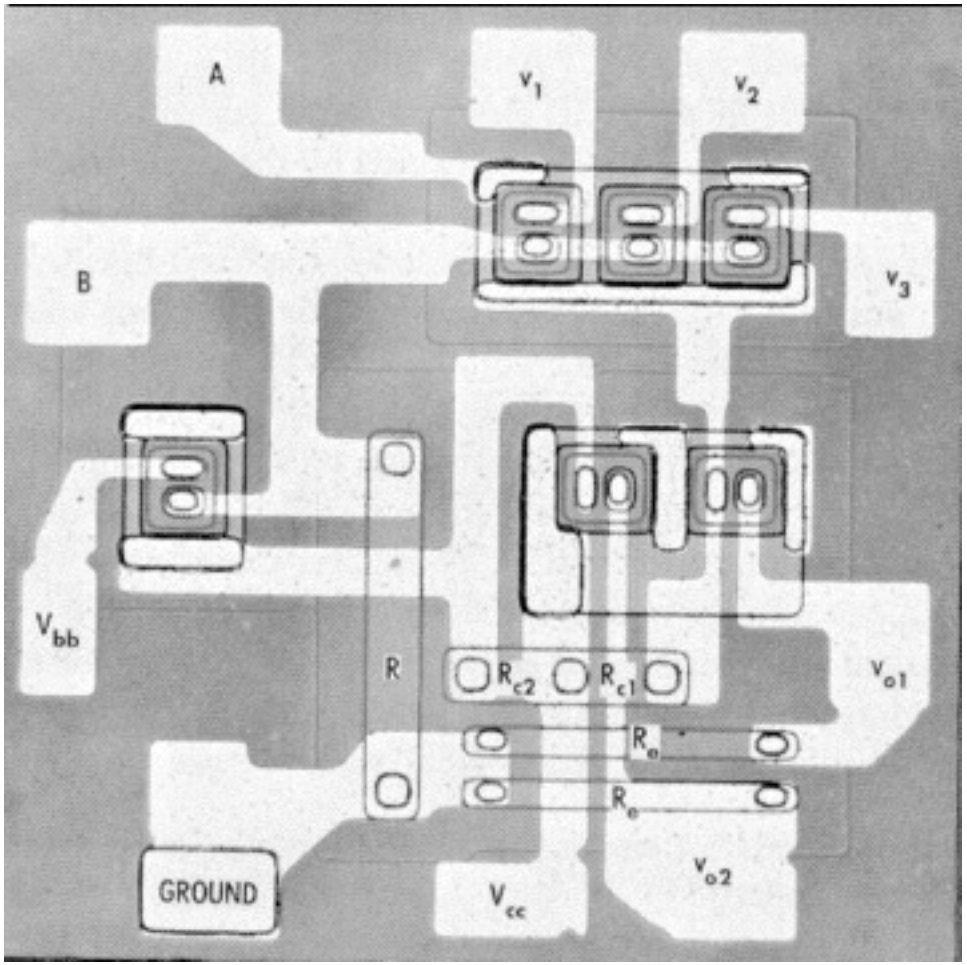
First bipolar transistor
Bell Labs, 1948

The First Integrated Circuits



First Integrated Cicuit,
Jack Kilby, TI 1958

The First Integrated Circuits



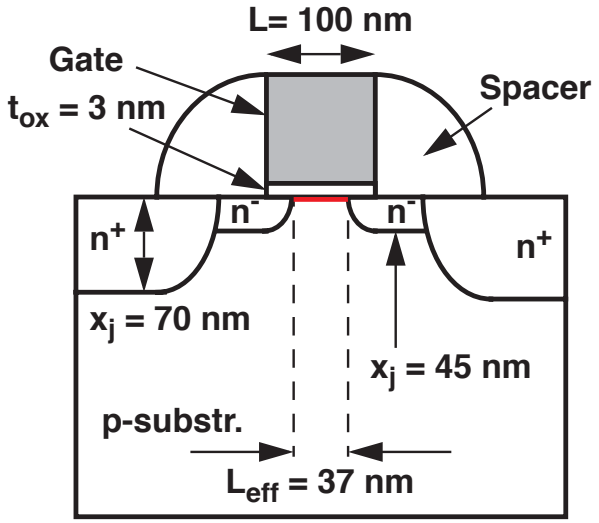
Bipolar logic
1960's

ECL 3-input Gate
Motorola 1966

Technology: MOS

What is: MOS

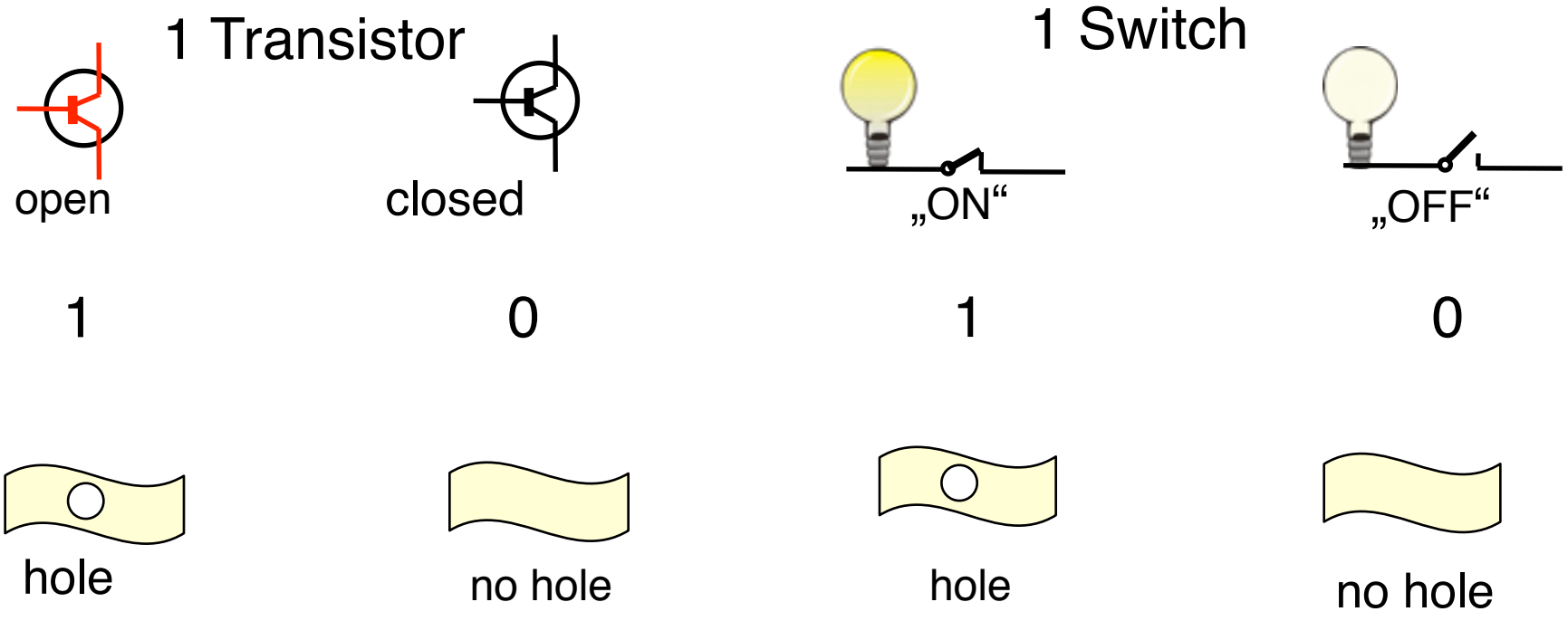
- acronym for **M**etal-**O**xide-**S**emiconductor
- today: Polysilicon-Silicondioxide-Semiconductor
- past: Aluminium gate
  today: Polysilicon, Polysilicid
- future: again metal as gate (better conductance)



- usage: **CMOS** in deep submicro area for logic and storage applications

deep submicro - L_{eff} in nano meter

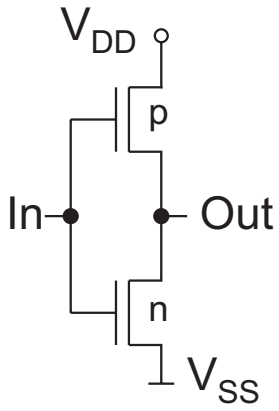
Recall: **Digital Logic - What is a „Bit“?**



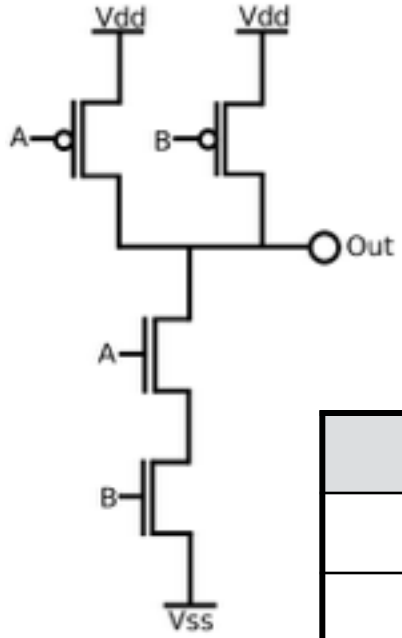
Bit = Representation of an information with two possible values (0,1)

Recall: **Basic digital circuit elements**

Inverter



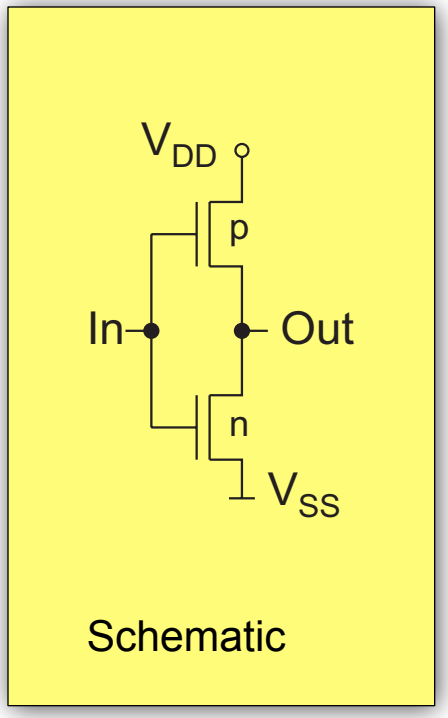
IN	OUT
1	0
0	1



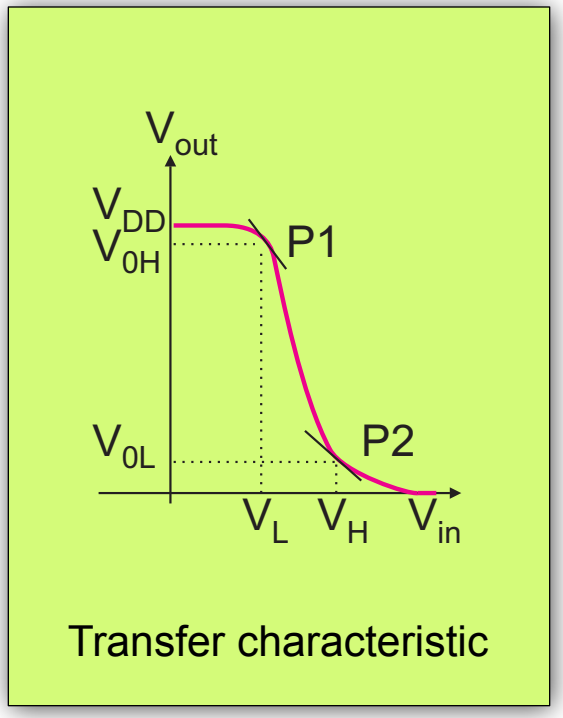
NAND-Gate

A	B	OUT
0	0	1
0	1	1
1	0	1
1	1	0

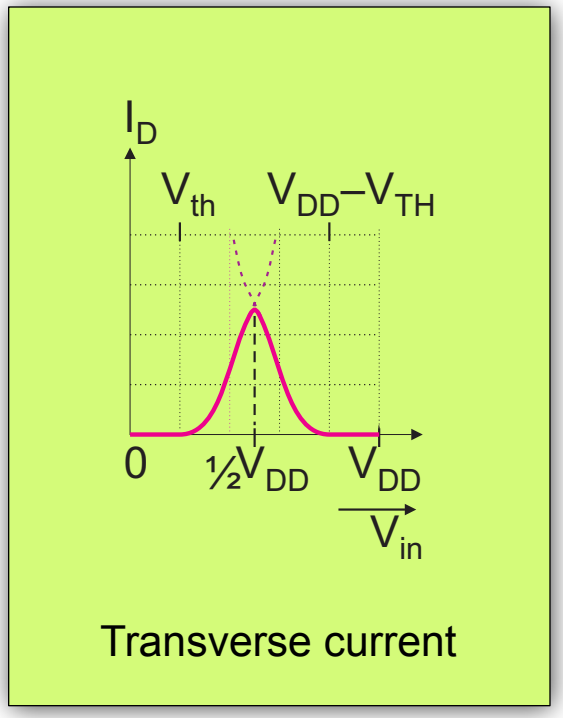
CMOS-Inverter



Schematic



Transfer characteristic



Transverse current

From this behaviour the transfer characteristic can be determined.

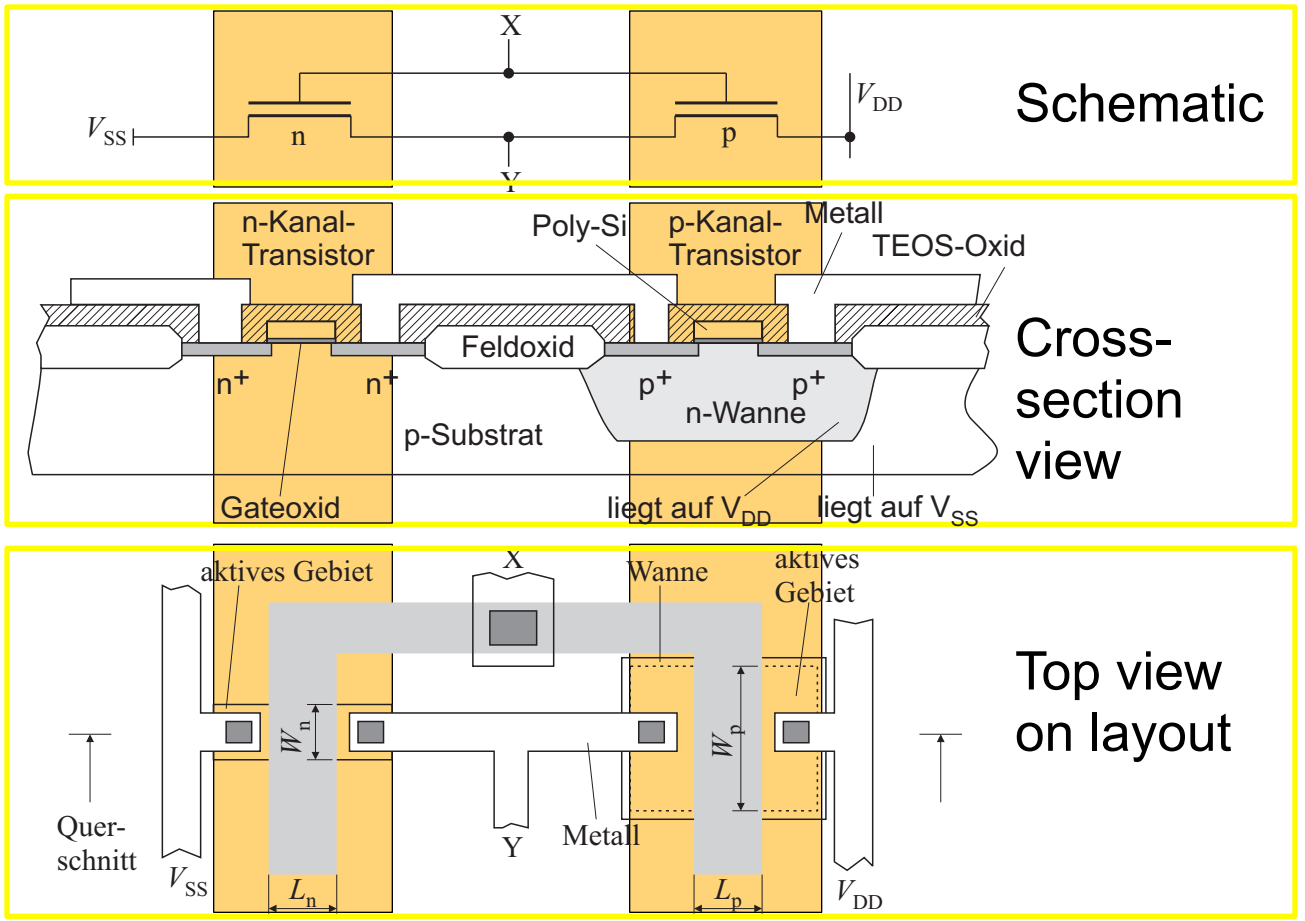
Current flows only at the moment of switching (Ideal behaviour).

CMOS -Inverter

Transfer of electrical circuit to a layout:

The figure shows the correlations between schematic and geometrical structure.

$W_p / W_n \sim \mu_n / \mu_p$



Summary CMOS

- Broadly used in all the major digital IC's
  (microprocessors, microcontrollers, static RAM…)
- The established manufacturing process
- Low power dissipation (no static cross current/flow)
- Uses complementary and symmetrical pairs of p-type and n-type MOSFETs

Chair for Circuit and System Design

Introduction
-
Technology

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Semiconductor-Technology

Realisation of electrical functionality with integrated semiconductor structures using dedicated technological methods and processes applied to a silicon wafer:

- (Photo-)Resisting / Lithography
- Oxidation
- Etching
- Doping (Ion-Implantation)
- Chemical-mechanical planarization etc.

The collection of these steps is called “**Technology**”.

IC-Packaging

- Bonding
- Encapsulation

IC-Testing(!)

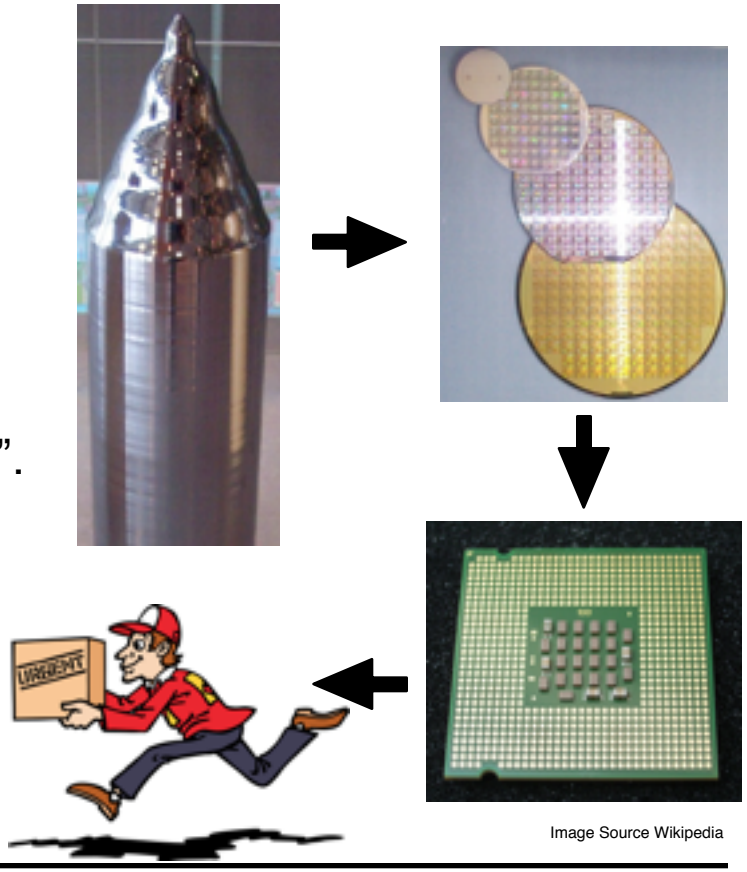


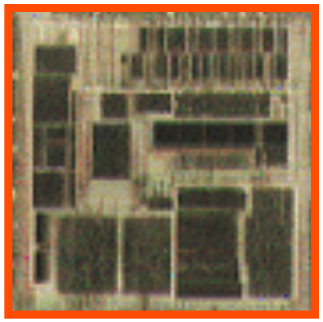
Image Source Wikipedia

Technology nodes - Moore's Law

„Every 18 moths the integration density doubles.“

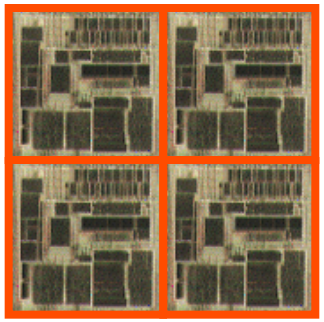
Gordon Moore, 1964/1975

1996



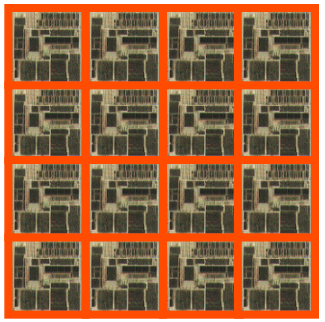
1 Chip

1999



4 Chips

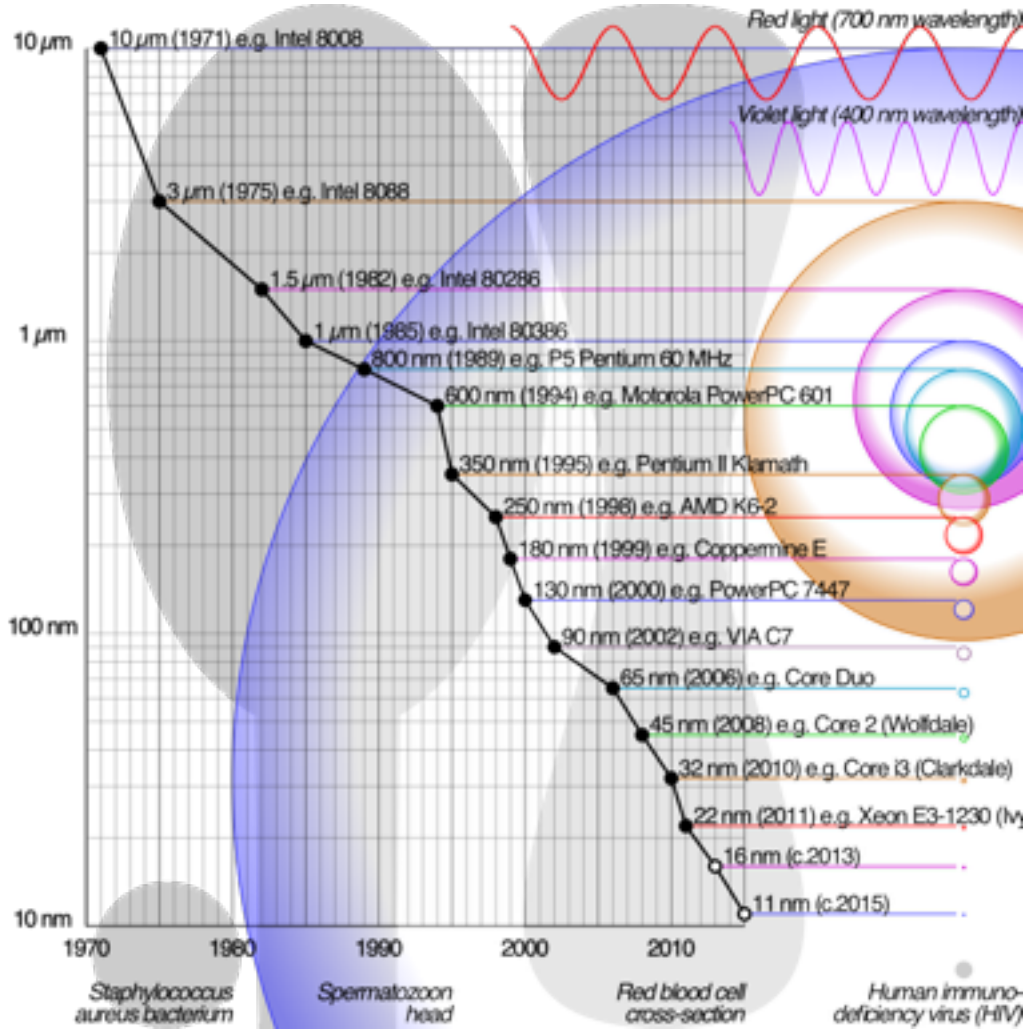
2002

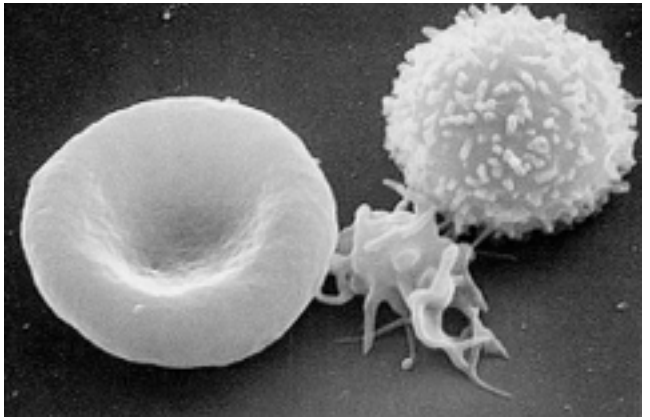


16 Chips

10 µm	1971
6 µm	1974
3 µm	1977
1.5 µm	1982
1 µm	1985
800 nm	1989
600 nm	1994
350 nm	1995
250 nm	1997
180 nm	1999
130 nm	2001
90 nm	2004
65 nm	2006
45 nm	2008
32 nm	2010
22 nm	2012
14 nm	2014
10 nm	*2016 –2017*
7 nm	*2017 – 2018*
5 nm	*2020 – 2021*

Technology nodes - Moore's Law and Cells





leukocyte, red blood cell ~ 7um

"Comparison semiconductor process nodes" by Cmglee (Wikipedia)

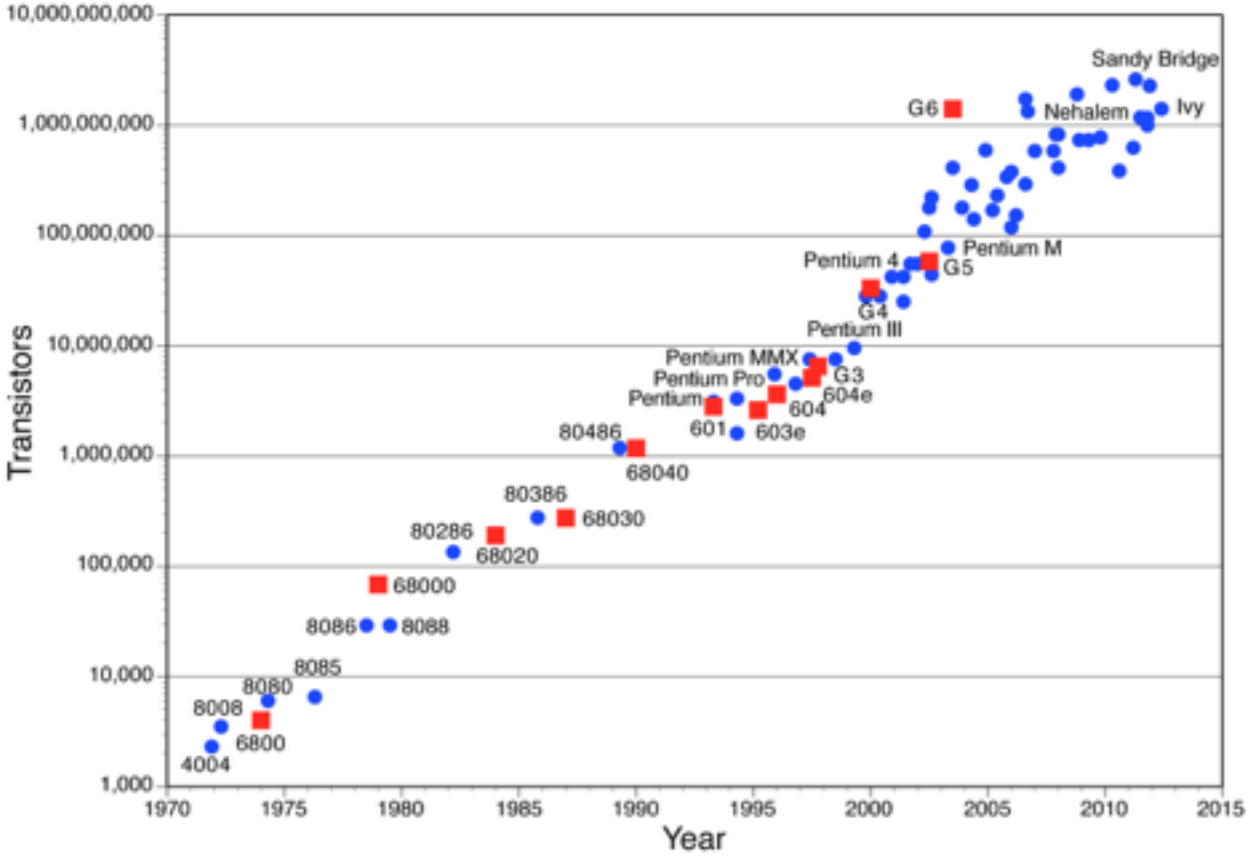
Moore's Law: INTEL Microprocessors

Moore's Law can also be applied to microprocessors:

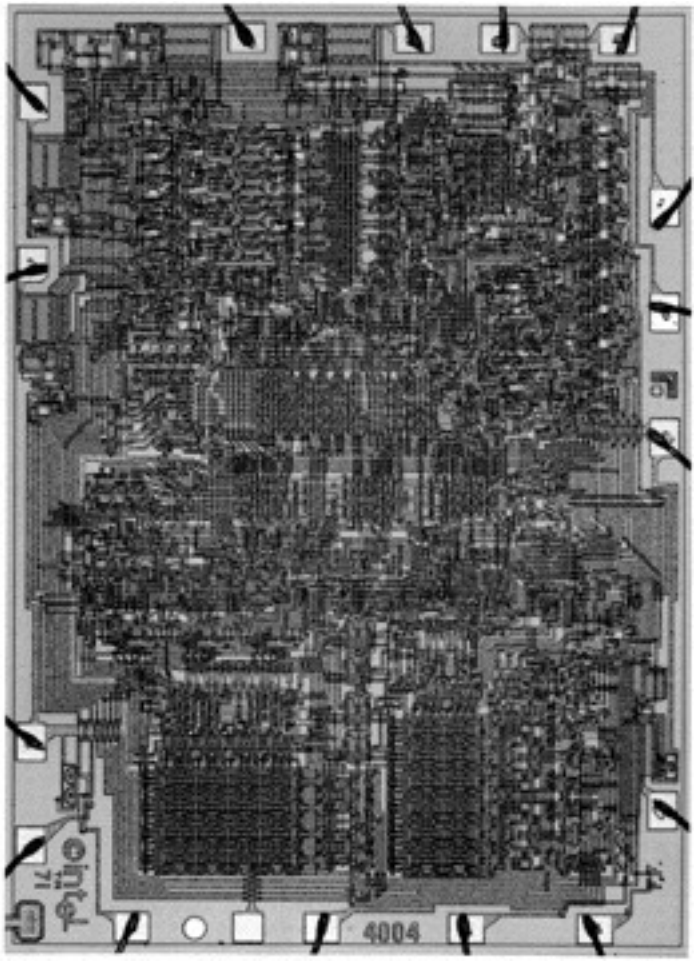
- at first every 4 to 6 years
- reduced to 2 years (number of transistors doubles every 2 years)

Conclusion:

- processing speed doubles every 18-20 months
- memory density doubles every 18-20 months
- the Intel P4 3 GHz CPU you buy today for $250 will cost
  - $125 in eighteen months… $62.50 in three years… $36.25 in four and a half years… $18.12 in six years… and free with your breakfast cereal 1.5 years later…
  - … by that time your $250 will buy you a 96 GHz CPU



Intel 4004 Micro-Processor

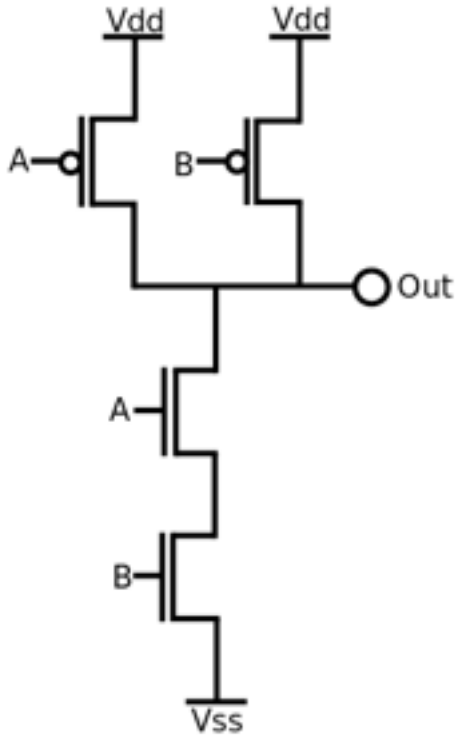


1971
1000 transistors
1 MHz operation

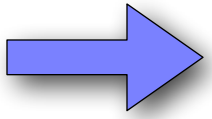
Full-Custom design
no design tools
no description languages

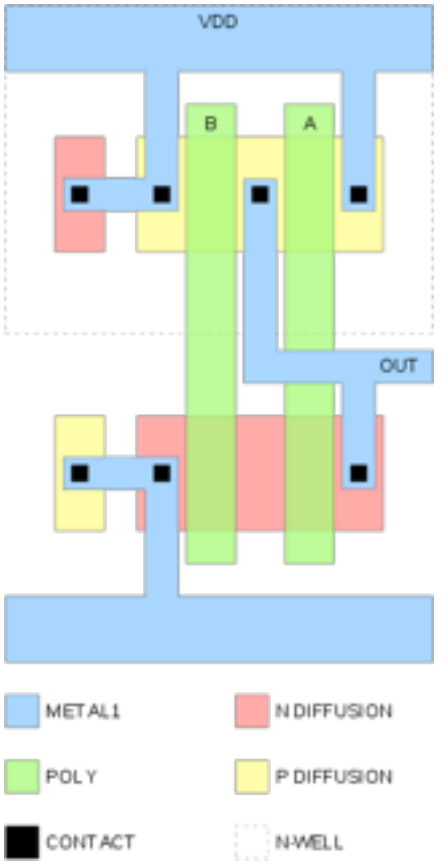
Example Full-Custom-Design

AND - Gate: 2-input-NAND



Transistorcircuit



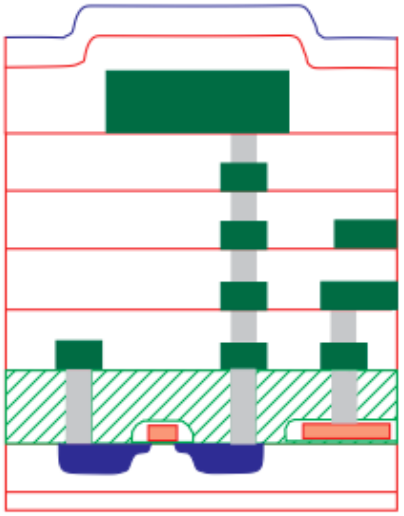


Layout

Profile view of CMOS logic technologies

0,350 µm technology

interconnect - 5 layers:

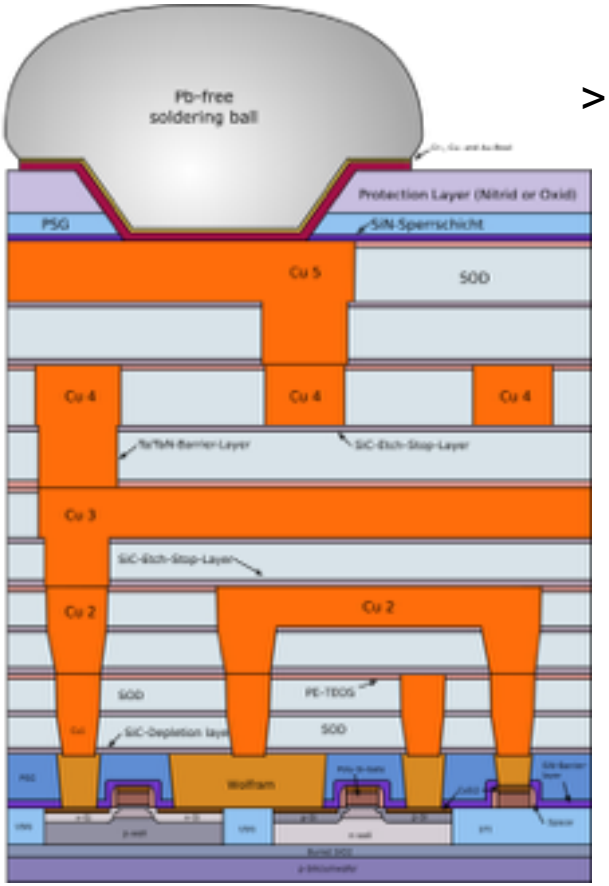


interconnect layer, consists of dielectric SiO_2, plugs, wires (Al)

plugs (Wolfram)

silicon

Transistor, polysilicide gate with spacer



> 0,1 µm technology

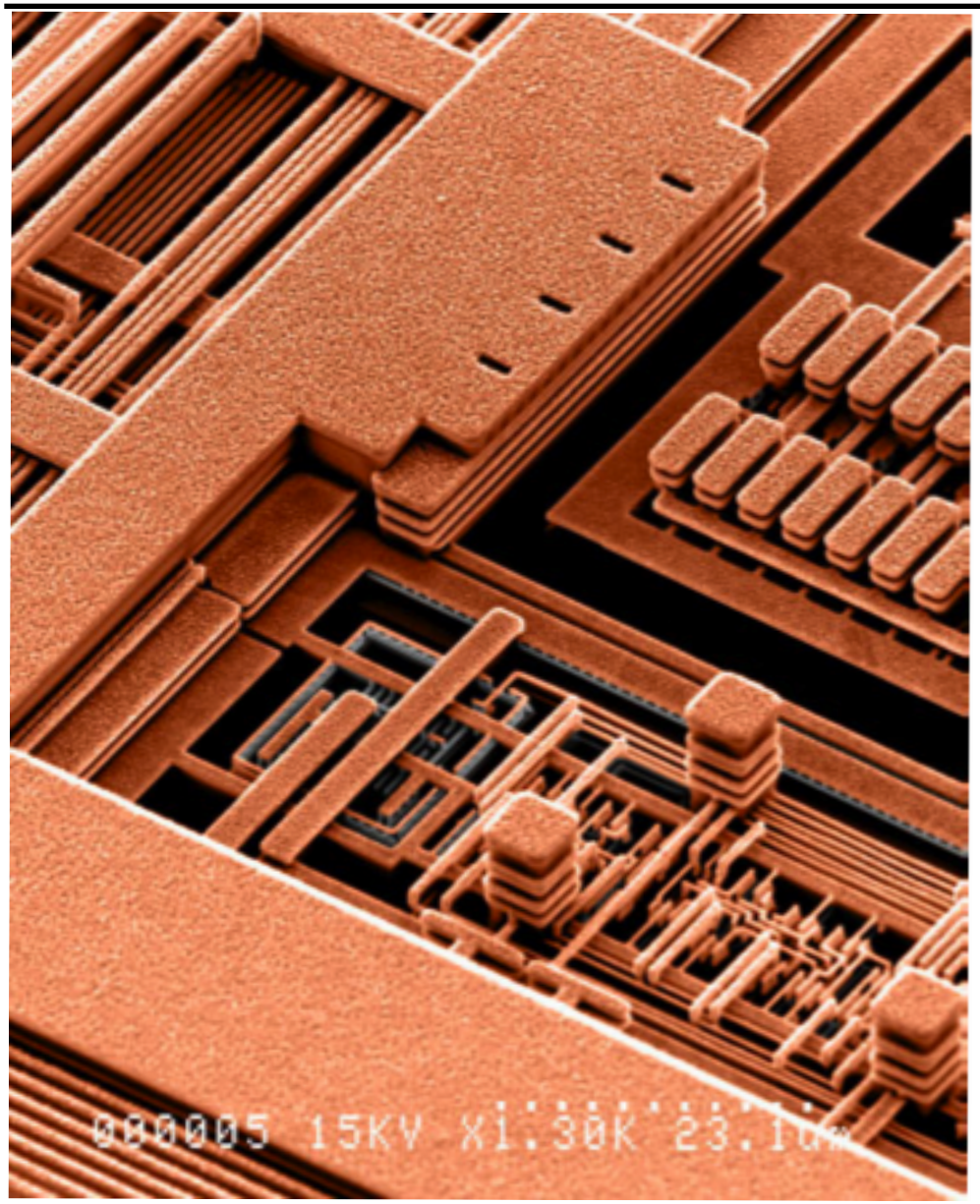
interconnect - 10 layers:

dielectric (low ε)

plugs (Cu)

wire (Cu)

"deep sub - µm"



copper wire without isolation

Chair for Circuit and System Design

Introduction
-
IC-Design

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Market segments for large digital ICs

Logic applications have become the technology driver, very large circuits are called „Systems on a Chip“, SoC.

There are three different approaches for designing large digital ICs:

- **Full Custom**:

  mass products with high performance, large design efforts with a lot of manual steps in the design process
  e.g.: micro processors, memories, DSPs, consumer applications, often including analog circuits

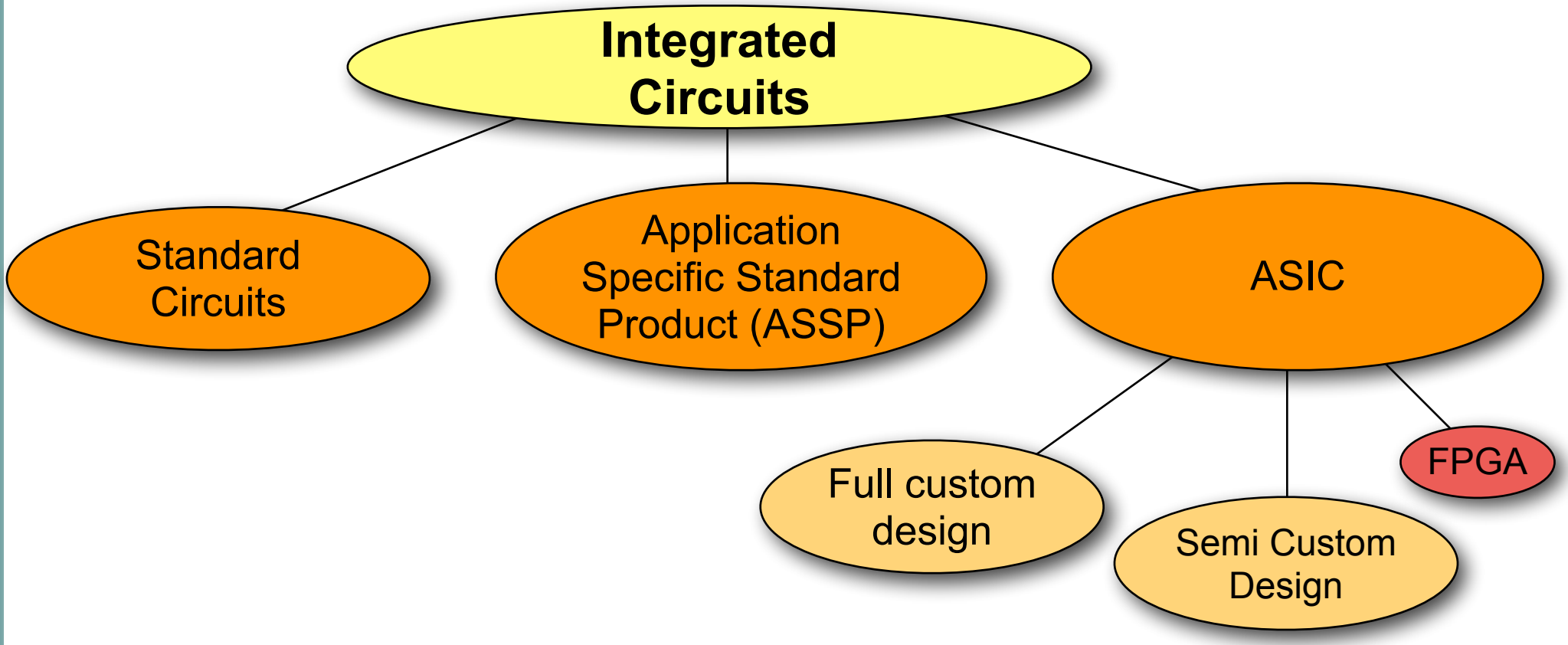
- **Semi Custom**:

  medium number of application specific components, extensive use of automated design methods. e.g.: large logic components for complex systems (base stations for cellular phone networks)

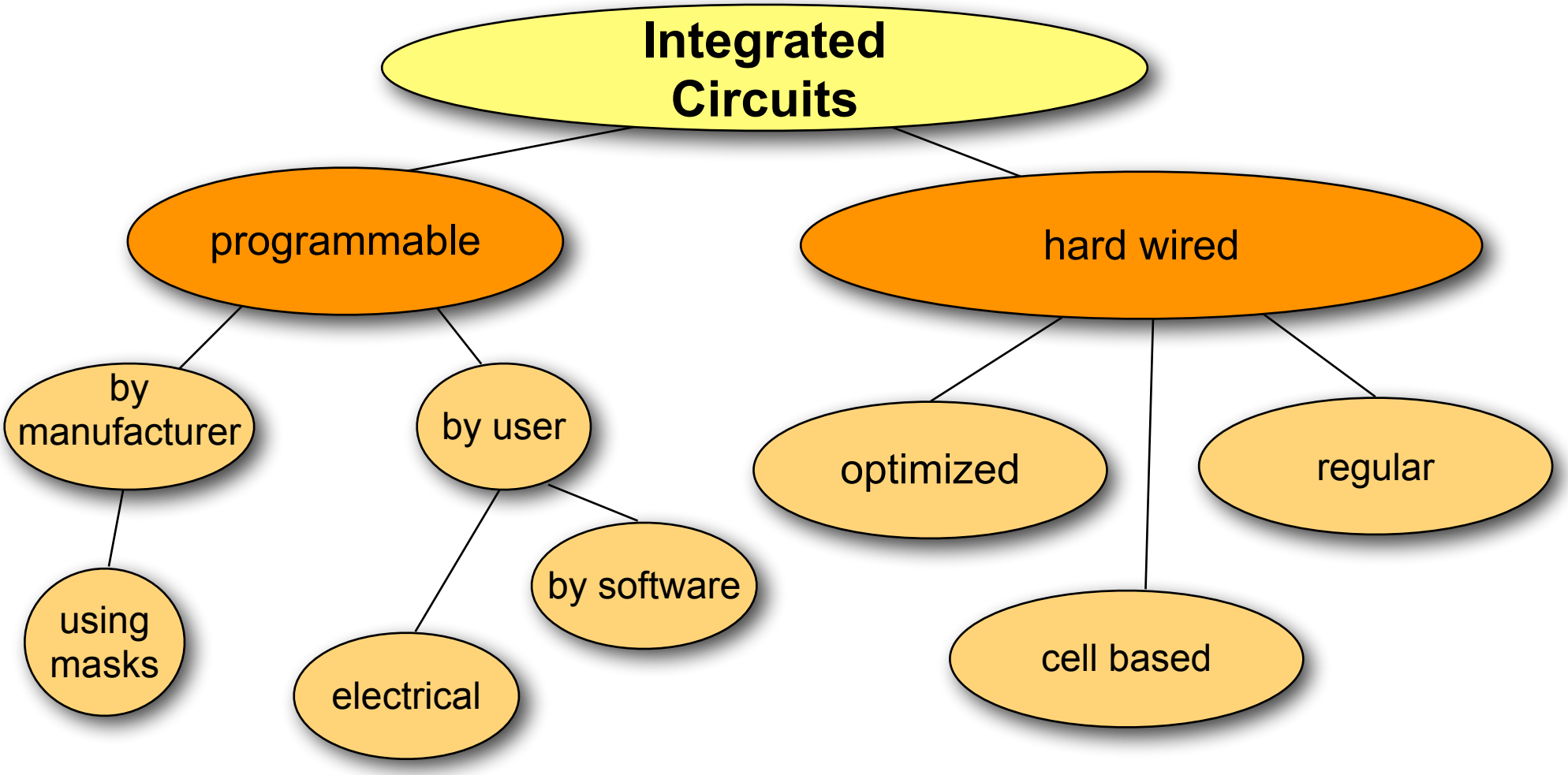
- **FPGA**:

  small number of application specific components, logic behavior is programmed (e.g. Field Programmable Gate Arrays) rather than designing a set of masks for components
  e.g.: logic components for small number of complex systems and prototypes (e.g. measurement equipment) with considerably less performance (compared to Full and Semi Custom designs)

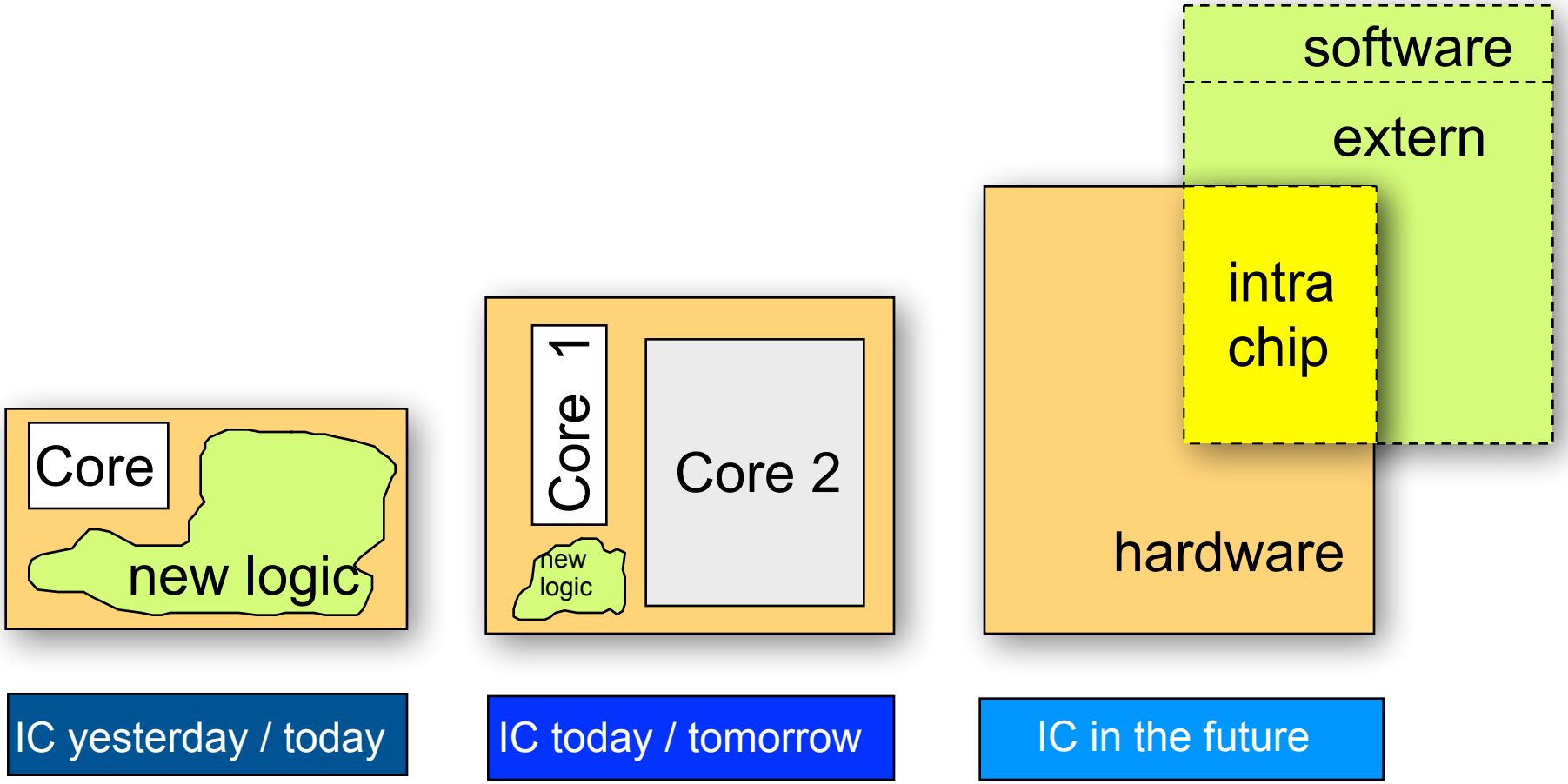
Classification of circuits - market based



Classification of circuits - structure based



Development of IC structure



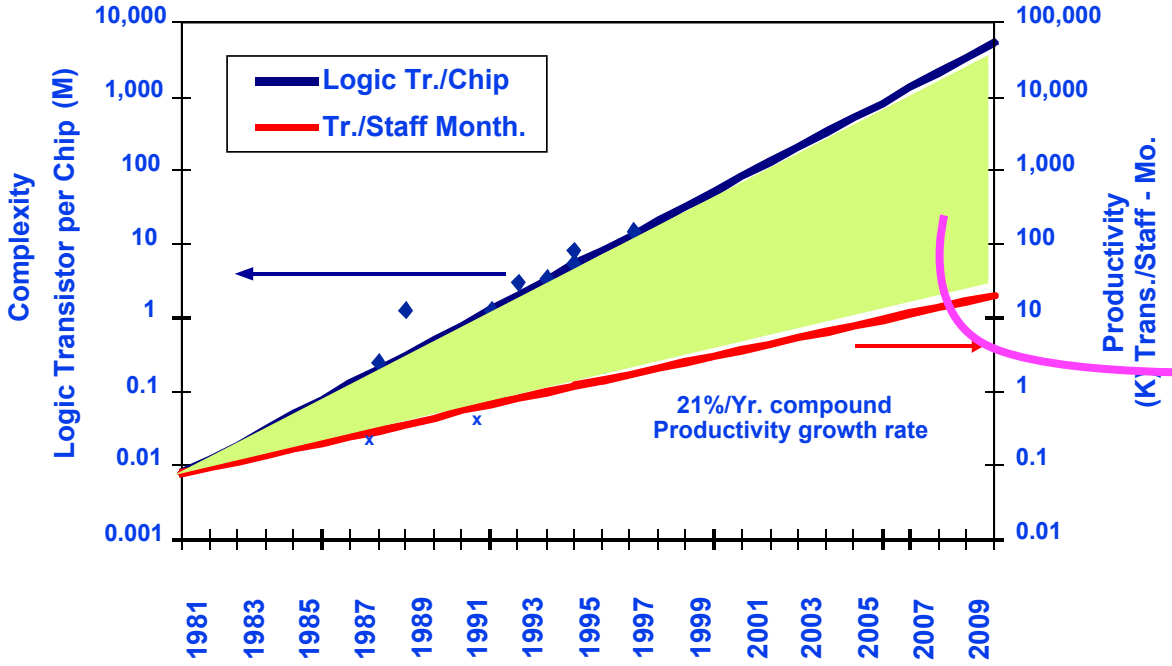
Constraints that limit IC's

- **Size** (mobile phone, smart card, sensor technology)
- **Reliability** (automobile, other applications relevant to security)
- Savings in **IC costs** (consumer)
- Savings in **Mounting and Connection** technology (consumer)
- Savings in **Power Dissipation** (heat! cooling! battery lifetime!)
- **Enhanced Functionality** (number of inter-chip connections)

Functionality grows with shrinking design size

Remaining demand for using smaller technologies

Problem: Design Gap



Complexity outpaces design productivity

Design Gap

Big Problem

Solution:

- "programmable" ICs (processors, µC, application specific: ASIC), FPGAs
- automated design steps, standardised design tools
- extensive library concepts (ReUse) + prefab (half-finished) chips
  ⇒ mask-programmable ASICs, Structured ASICs

HDLs

Problem: Design Productivity

How to design chips with more and more functions?

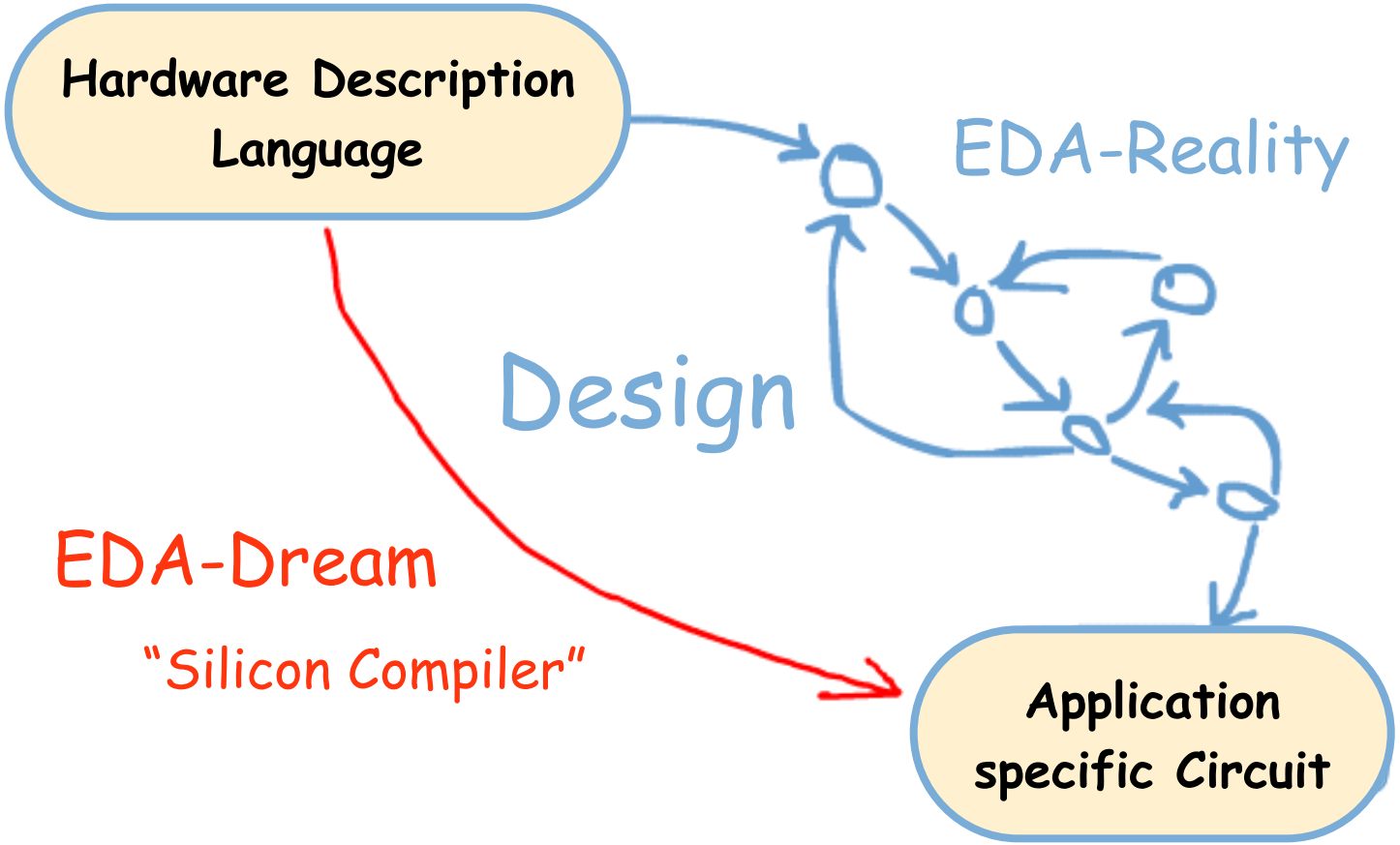
Design engineering population does not double every two years…

- Hence, more efficient design methods are needed!
  - Productivity of development has to be raised,
    yet it stays behind the increase of chip complexity (21 %/year)
  - Efficient organisation of the development has top priority
  - Work on the highest level of abstraction
  - Automation by applying efficient algorithms

Use of structured computer-aided design processes:

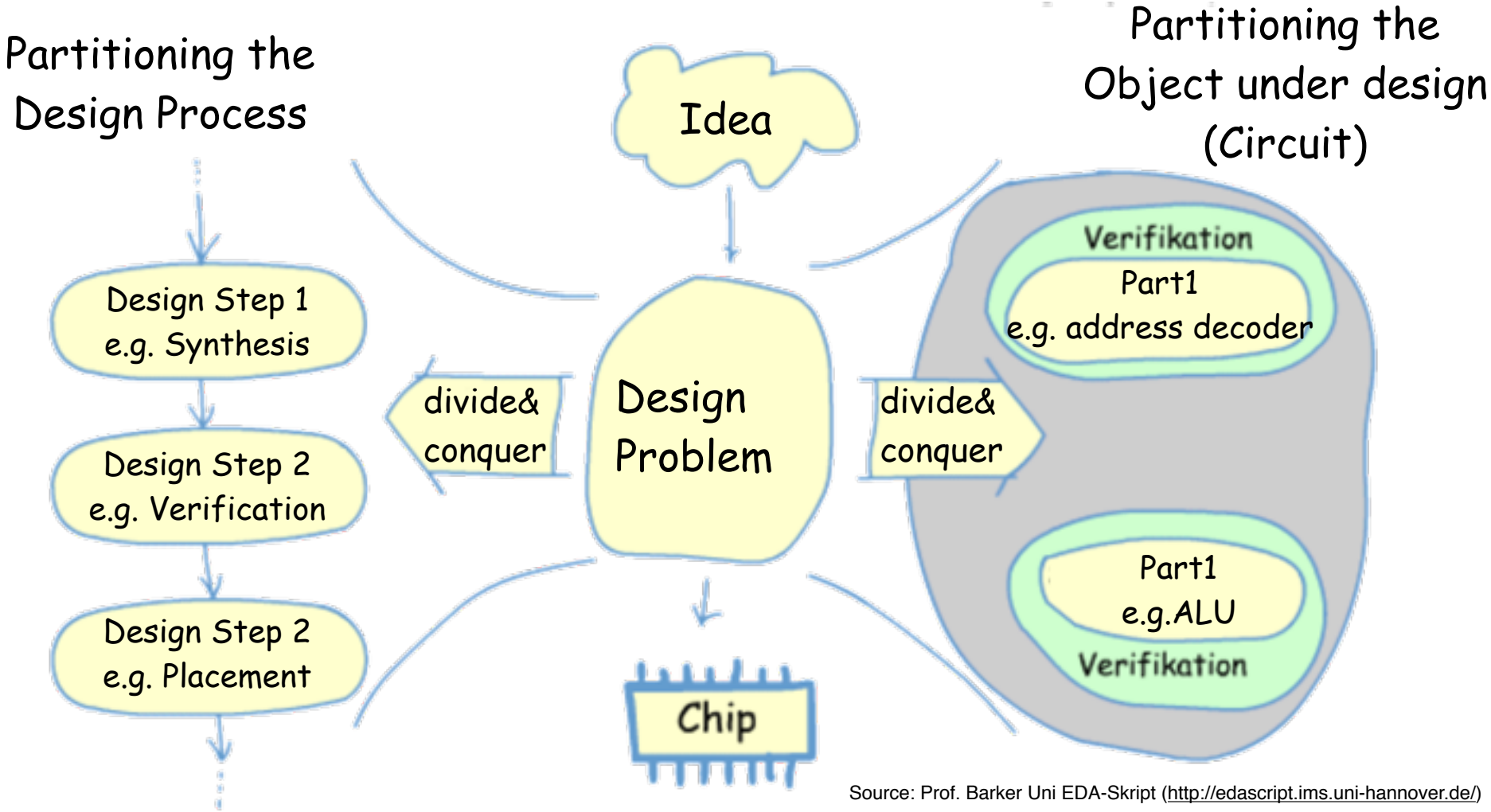
Hardware Description Languages **Verilog, VHDL, SystemC**

Automated Design Process for Electronic



Source: Prof. Barker Uni EDA-Skript (http://edascript.ims.uni-hannover.de/)

Cope with Complexity — Divide & Conquer



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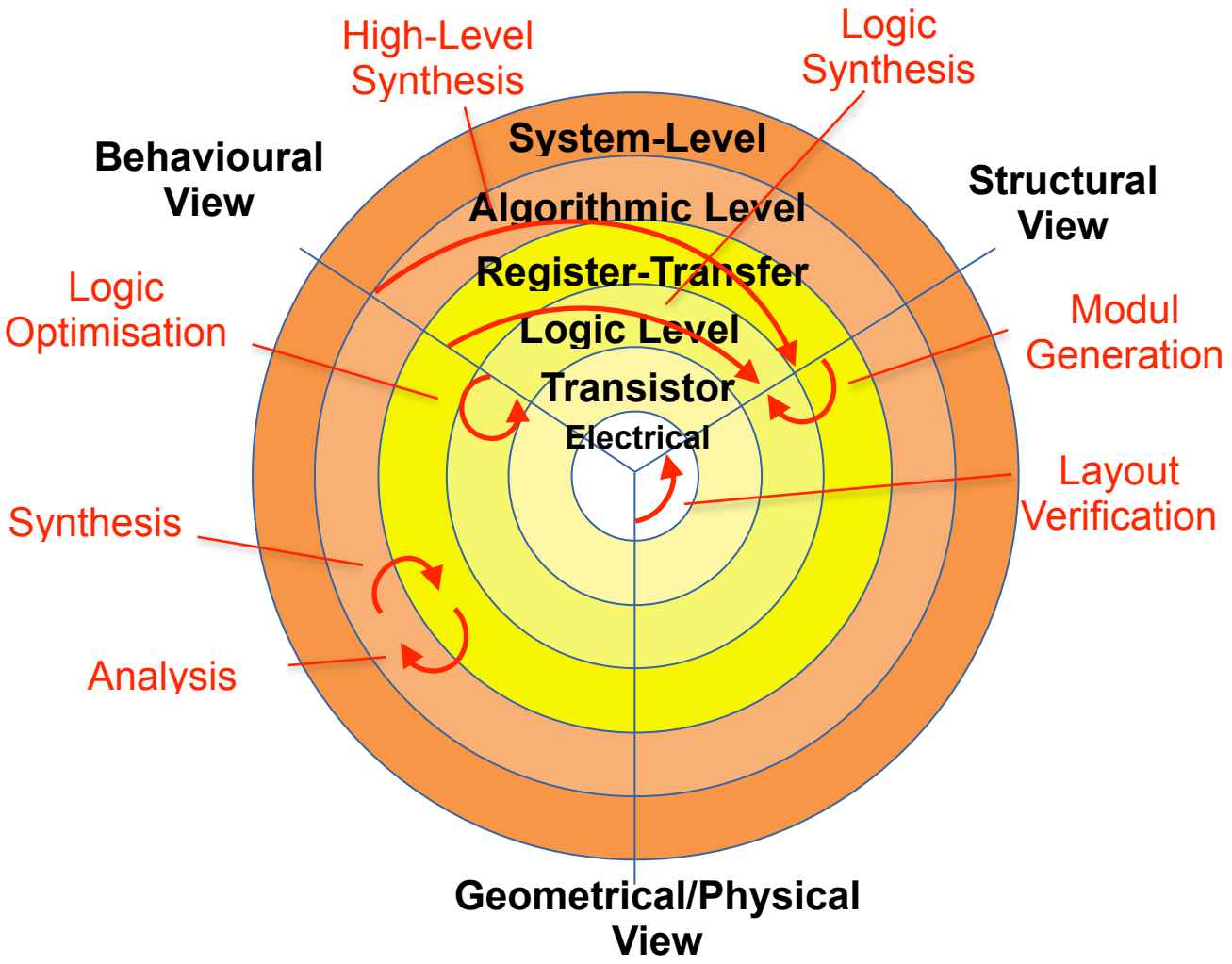
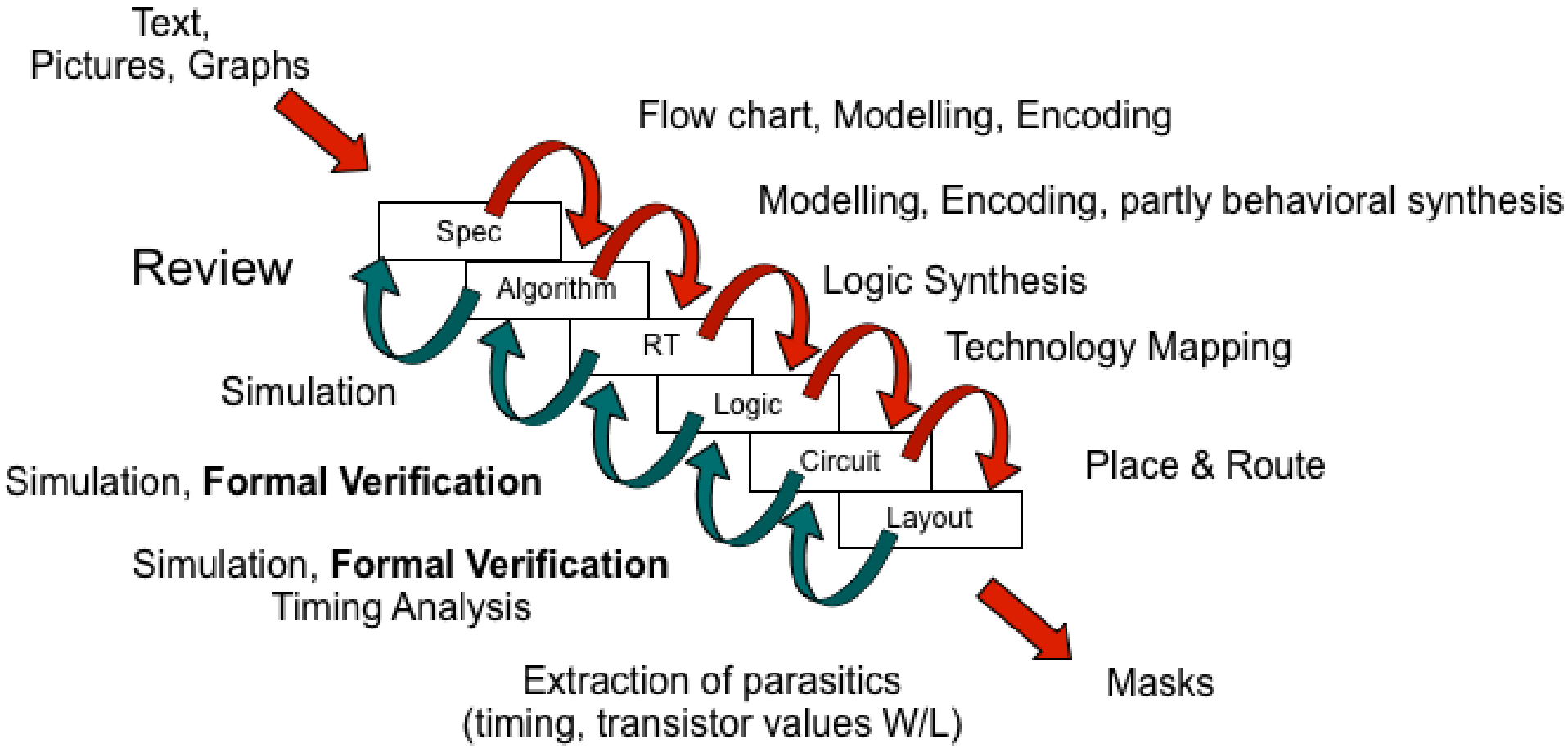
EDA Tooling in IC Design



- **Description/ Specification**
- **Generation**
- **Synthesis**
- **Analysis/ Simulation**
- **Optimisation**
- **Verification**

Circuit Design Process - Waterfall



Specifics in Designing/Engineering Hardware

- Hardware verification takes up 70-80% of ASIC design time

- Hardware has to be correct: Design errors are expensive!!!
  - Re-design: rising costs for masks >> 3 million USD per ASIC

- Hardware verification is costly:
  - Functional Simulation, Design Rule Check, Equivalence Checks, Timing Analysis, Board Validation
  - “compute farms”: IBM 500 Workstations, Intel Pentium 4 >> 1000 Workstations

- Hardware design teams are big and spread

- Hardware design is entry for any software design activities

Hardware Complexity Example

Increasing Complexity:

- Gate count: (2004)
  - Lucent 40GBit/s Sonet/SDH/G709 processing
    >> 10 million gates

- Simulation time:
  - 1 Sonet/SDH frame >> 10 min sim time (real-time ca. 1 usec!!)
  - general testcase: 10 - 100 frames per simulation run
  - special testcase >> 300 frames
  - total >> 1000 testcases

about 350 days simulation time

verification team: 14 people, using parallelization, compute-farms - regression runs about 3 days

design team: 4 people!!

EDA is a partner in IC Design

EDA-Industry's to do:

- Adjust algorithms (e.g. layout, calculation of conductor length/ capacity)
- Adjust methods to new parameters/data sets (e.g. Physical Synthesis, i.e. first perform pre-synthesis with approximated placing, then layout, to better estimate conductor length)
- Simulation/Verification methods (cycle-based, transaction-based, ability to simulate larger systems (= more data) in the same amount of time)
- More formal methods!!!

Goal: able to handle the new and larger systems.