Possible exam questions

EDA Tools 1 / Winter semester

Specification

- Which types of circuits exist? Provide a classification.
- Explain Moore's Law.
- Name reasons why the physical size of ICs should be decreased over time.
- Name concepts for realization of digital integrated circuits. (realization of IC dependent on quantity and temporal availability)
- Explain the V model.
- Depict the waterfall model.
- Which requirements have to be fulfilled by a specification?
- Name three languages used for requirement specification and when they can be used.
- Explain the terms *system specification*, *Lastenheft* (*requirements document*) and *Pflichtenheft* (*functional specification*).
- What are the differences between formal and non-formal specification languages? Which advantages/disadvantages arise?

VHDL

- What are the differences between RT and logic/gate level? Explain in detail.
- What is the basic idea of RTL synthesis?
- Write down the VHDL syntax for a simple multiplexer (inputs: `a`, `b`, `sel`; outputs: `out`).
- Write down the VHDL syntax for a simple D flip flop (inputs: `clk`, `reset`, `d`, `en`; outputs: `q`).
- Discuss the term *sensitivity list* regarding simulation and synthesized circuit.
- In RTL code, how can you determine the amount of flip flops that will be generated during synthesis?

SystemC

- Explain the design flow of digital HW/SW systems.
- Name three possibilities to describe parallel behavior in SystemC and explain their differences.
- Explain the general structure of a SystemC program and compare to VHDL.
- How can communication be abstracted from signals to channels? Explain the terms *interface*, *channel* and *port* in this context.
- What is the impact of the Model of Computation? Illustrate by comparing two different MoCs.
- Which model of computation is used in the SystemC kernel?
- Why is `sc_fifo` commonly used for functional modelling?
- What is Transaction Level Modeling? Which advantages does it offer and how and when can they be utilized?

High Level Synthesis

- What is the difference between the traditional digital design flow and the HLS-driven design flow?
- Consider you have 1 adder, 1 multiplier and 1 subtractor. Draw an implementation of the boolean function $ax^2 + (b - c)x + d$. How many clock cycles are necessary for computation?
- Explain the terms *CFG*, *DFG*, *Scheduling*, *Allocation* and *Binding*.

Verification

- Define the term *verification*.
- Which methods for verification do exist?
- Explain the difference between simulation and formal verification.
- Define the term *validation*.

Simulation

- What is simulation?
- Compare analog and digital simulation.
- Name three delay models and their corresponding properties.

- Consider the following VHDL statement:

  ```
  sig_a <= sig_b AFTER 5 ns;
  ```

  Assume the simulator granularity is set to 10 ns. By which amount will simulation time advance when this statement is executed?

- How can signal values be modeled for digital simulation? Name four examples and their corresponding values.

- Explain the term *delta cycle*.

- Assume a zero delay simulation model and a simulator granularity of 10 ns. The following VHDL statements are given:

  ```
  sig_a <= '0' AFTER 0 ns, '1' AFTER 1 ns;
  sig_b <= '1' AFTER 0 ns, '1' AFTER 1 ns;
  ```

  The circuit behavior is described as:

  ```
  sig_c <= sig_a OR sig_b;
  sig_d <= NOT sig_c;
  sig_e <= sig_a XOR sig_d;
  ```

  `sig_a` ... `sig_e` are signals of `std_logic`.

  Make a table containing simulation times, delta cycles and signal assignments!

EDA Tools 2 / Summer semester

Representations

- What are the differences between formal verification, simulation and emulation? What are the limitations of formal verification?

- Which properties of boolean functions are desired?

- Explain the term BDT and name its most important properties.

- Explain the terms BDD, OBDD and ROBDD and name their defining properties. How can they be constructed?

- Explain Shannon's decomposition. What is it used for?

- Illustrate the rules to remove redundancy in ROBDDs.

- Define the term *isomorphism* regarding two ROBDDs.

- Discuss the term *variable order* regarding ROBDDs and discuss ROBDD complexities. Explain a method to derive a good variable order.

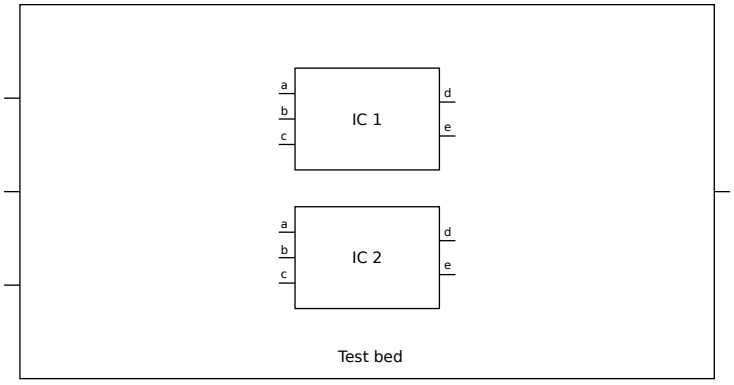
- How can an ROBDD be implemented in a digital circuit?

- Create an ROBDD for the function $f = (x_1 \wedge x_2) \vee x_3$. Use the variable order $x_2 < x_3 < x_1$.

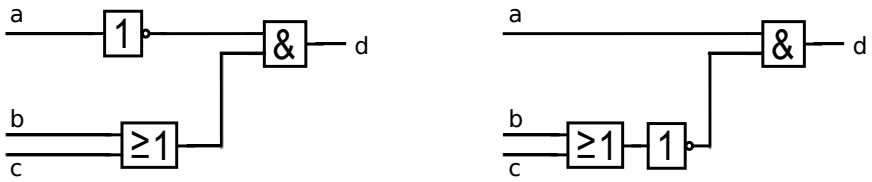
- Define the ITE operator and give the three basic boolean functions NOT, AND, OR in ITE form.
- Derive an ITE form of the following boolean formula: $f(x, y) = (x \oplus y) \Rightarrow x$

Equivalence Checking

- Explain three different use cases of equivalence checking. When and why is it used?
- Name three methods for equivalence checking of boolean functions.
- What does the term *Boolean Satisfiability Problem* mean?
- Explain the flow for checking two combinatorial circuits for equivalence.
- Name and explain an algorithm for SAT Solving. Which methods can be used to reduce execution time? Explain using an example.
- Explain the term *counter example* regarding equivalence checks.
- For the following two circuits, create one large circuit whose only output might become one if and only if the circuits are different. How is such a circuit called?



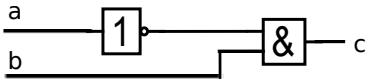
- For the following two circuits, generate a CNF which should be satisfiable if the circuits are not equivalent.

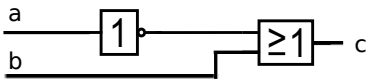


- Set $x_1 = x_2 = x_5 = 1$ in the following CNF and simplify: $(\overline{x_1} \vee x_2 \vee x_3) \wedge (\overline{x_2} \vee x_4) \wedge (\overline{x_3} \vee x_5) \wedge (\overline{x_5} \vee x_4)$
- Check if the following CNF is satisfiable by applying the Davis Putnam algorithm step by step: $f(a, b, c, d) = (a \vee c) \wedge (\overline{a} \vee \overline{c}) \wedge (b \vee c \vee \overline{d}) \wedge (\overline{b} \vee \overline{c} \vee \overline{d}) \wedge (b \vee \overline{c} \vee d) \wedge (\overline{b} \vee c \vee d)$
- Check the following formulas for equivalence using a BDD approach:

  $f\,(x_1, x_2, x_3, x_4) = x_1x_2x_3 \vee \overline{x_2}x_4 \vee \overline{x_3}x_4$ and
  $g\,(x_1, x_2, x_3, x_4) = x_1x_4 \vee \overline{x_1}\,\overline{x_2}x_4 \vee x_1x_2x_3 \vee x_2\overline{x_3}x_4$

- Generate a set of input stimuli for the following two circuits using the ATPG method:





Temporal Logics

- Name basic temporal logics and the differences between them.
- Explain the following temporal operators: X, F, U.
- Develop corresponding CTL formulas for the following cases.
  - "Eventually, p will definitely happen"
  - "p will occur infinitely often"
  - "Eventually the system will restrict to states in which p always holds"
- Explain the following CTL formula: $AG(\overline{p} \rightarrow EX\ q)$

Model Checking

- What is the difference between safety and lifeness properties? Explain using an example for each property type.
- Explain the general idea of Bounded Model Checking. Which type of systems can be checked by Bounded Model Checking?
- Explain the general idea of Symbolic Model Checking. Which type of systems can be checked by Symbolic Model Checking?