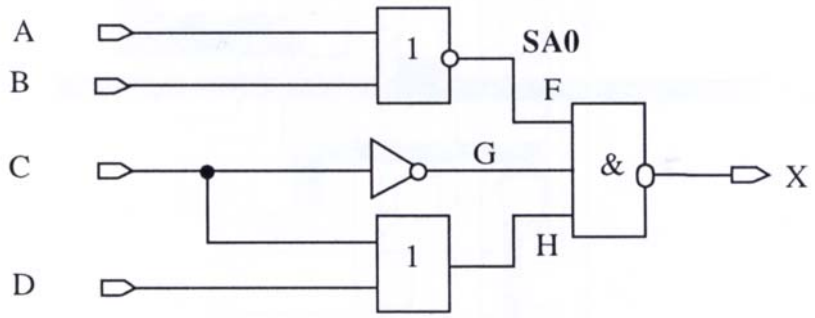
Lessons for Test pattern generation

Lesson 1: stuck-at-Faultmodel

Take a look at the following gatelevel netlist:

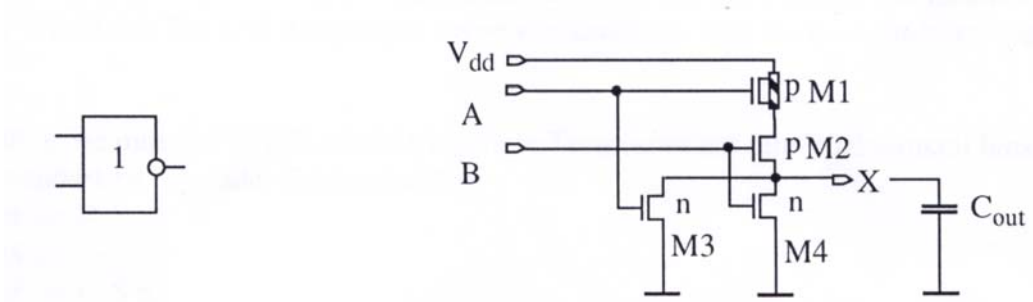


a) Develop a test pattern fort he primary inputs A ... D which allows the controllability of a stuck-at-0 fault at node F and the observability at the primary output X.

b) Proof your test pattern using a SPICE simulation.

Lesson 2: stuck-short-Faultmodel

There is a stuck-short fault at D-S at transistor M1 inside a NOR gate.

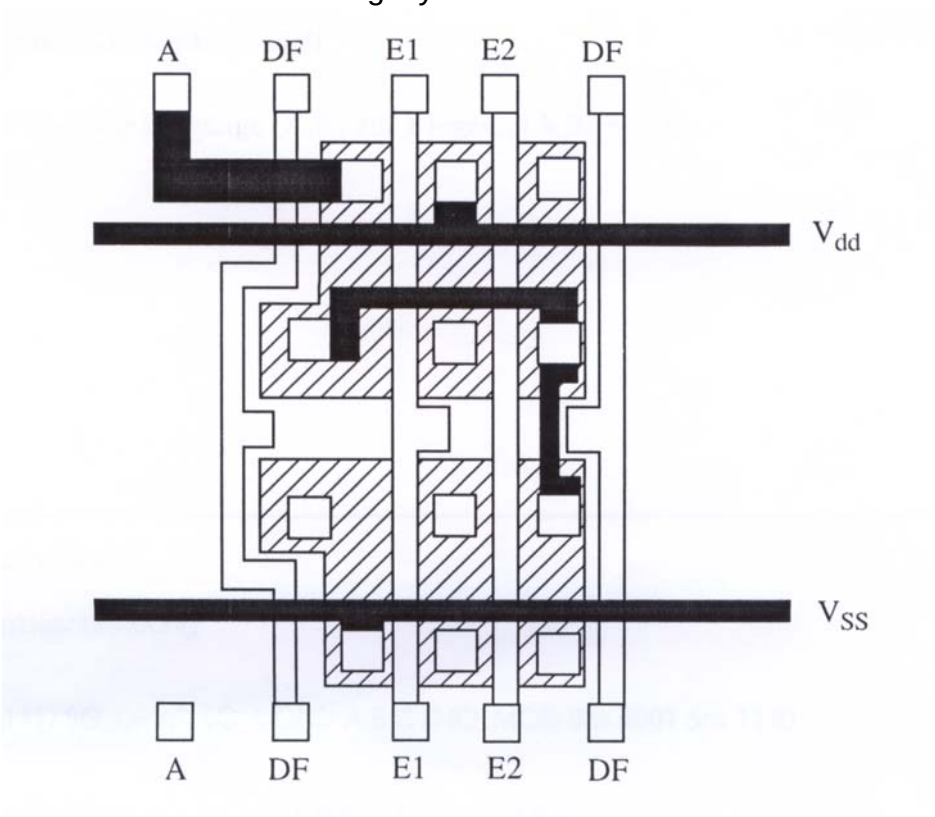


a) Develop a switch-level test to detect this fault

b) Check your test pattern in a SPICE simulation. Use a PWL source (piecewise linear voltage) for the stimulation of the inputs. What can you observe at the output (level and current)?

Lesson 3: Complete set of test pattern

Take a look at the following layout:



a) What is the function of this layout? Sketch it as transistor schematic.

b) Develop a complete set of test pattern for this circuit which allows the detection of all stuck-at-0/1 and of stuck-off/stuck-on faults.

c) Check your test pattern in a SPICE simulation with the following fault models:
   a. Stuck-on D-S p1
   b. Stuck-on D-S n1
   c. Stuck-off D-S p2
   d. Stuck-off D-S n2