Chemnitz University of Technology
Chair Circuit and Systems Design

Examination **"Components and Architectures of embedded systems"**

Name, Forename: _____

Matrikel number: _____

Number of sheets in addition to task description: _____

Examiner: Prof. Dr.-Ing. habil. G. Herrmann

Date: July 21th 2014
Duration: **120 Minutes**
Allowed auxiliaries: **None**

Please also state your procedure of solution for all calculations!
Please do not use a red pen!
Please write your matrikel number on every sheet you submit.
You can also write on this exam sheet.

Task:	1	2	3	4	5	6	7	8	9
Maximum points:	6	8	7	11	2	15	3	9	9
Reached points:									

Sum
70

Task 1 — 6 points — Basic Terms

Explain the purpose of the following microprocessor components in 1-2 sentences each: Control Unit, ALU, Address Unit, Register Set/File (4 points)

What should an architectural description of a computer contain?

Task 2 — 8 points — Computer Classification

a) Sketch the principles of SISD and MIMD after Flynn. (4 points)

b) Sketch a Stack Architecture and give advantages and disadvantages.

Task 3 7 points Arithmetic components

Give a general sketch of a serial adder operating on two 4 Bit inputs. (4 points)

Perform a binary multiplication of 13_d with 6_d. Write down also the intermediate results.

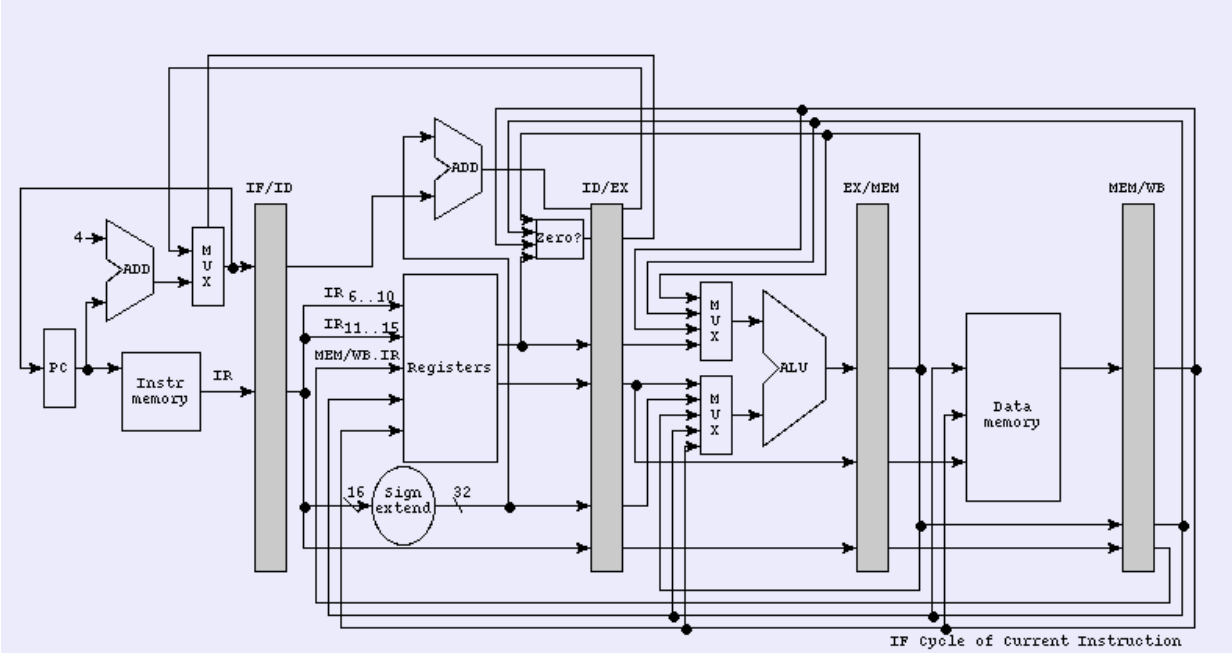
Task 4 11 points Pipelining

a) Why is it necessary to have a branch prediction unit in a pipelined machine? (2 points)

b) Explain the Write-After-Read hazard. In which pipeline type(s) may it occur?

c) What are the main components of a Tomasulo machine? How is it possible to avoid WAW hazards with such a structure?. (4 points)

d) In the DLX-figure below: What is the purpose of the adder and the multiplexer in the first (IF) stage? Which part of he DLX integer pipeline is used especially for branch decision calculation? Please mark it in the figure below. (3 points)



INTEGER datapath of pipeline

Task 5 2 points Calculation of power indications

Calculate the CPI value of a CPU based on the following values:

The CPU consists of 4 pipeline stages. Every 5th instruction causes a data hazard that leads to a 1 cycle stall. Every 10th instruction is a branch that leads to a 2 cycle delay.

Task 6 15 points DLX Assembler

Analyze the following code consisting of .d and .s file. We work on a DLX Basic Pipeline like in the simulator DLXView that allows Forwarding. Assume the following pipeline problems:

- ld to ld lead to 1 stall (Structural hazard)
- ld result is available at the end of MEM
- multd needs 5 EX cycles to complete
- Machine uses delayed-slot mechanism

Tasks to solve/answer:

a) After execution of the code: what is the result of *fget 56 d* and *fget 0x48 d* ?

b) Do a simple unrolling of the code. Write down the unoptimized unrolled code. Mark all hazards that lead to stalls (it is not necessary to give the exact number of stalls). (5 points)

c) Apply register renaming and optimize the code to get minimum runtime. (8 points)

content of .d-file:

```
        .data   0
        .double 1.00, 1.01, 1.02, 1.03, 1.04, 1.05, 1.06, 1.07, 1.08

        .data   0x80
        .double 2.0
```

content of .s-file:

```
        addi    r1, r0, 56
        ld      f0, 128
loop:   ld      f2, 0(r1)
        multd   f4, f2, f0
        sd      64(r1), f4
        subi    r1, r1, 8
        bnez    r1, loop
        nop
        trap    #0
```

Task 7 3 points IP-Cores/Busses

a) What is an On-Chip Bus? (1 points)

b) Give at least 4 examples for types of IP cores!

Task 8 9 points Cache

a) Describe in short words the operation principle of a cache (not the internal structure) (3 points)

b) What are the two types of locality a caching it taking advantage of. (2 points)

c) Caches can be combined for data and instructions or separate. What is the reason for both approaches (give two advantages of each)

Task 9 9 points VHDL lab

a) Have a look at the VHDL code below. Explain the basic functionality and timing of the model. (4 points)

b) What are the output values 10 ns after applying "0111" to inA, "0011" to inB and '0' to inC if there is a rising clock edge at 5 ns and reset_n is ‘1’? (2 points)

c) Modify the code so that if inC=’1’:

- cout returns the carry generated by the addition of the LSB of inA and inB
- result(n) returns the value ‘1’ if inA(n) = inB(n) and ‘0’ if inA(n) != inB(n) where n is the bit position.

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY exam_E IS
  PORT(
    reset_n  : in std_logic;
    clk      : in std_logic;
    inA      : in std_logic_vector(3 downto 0);
    inB      : in std_logic_vector(3 downto 0);
    inC      : in std_logic;
    result   : out std_logic_vector(3 downto 0);
    cout     : out std_logic
    );
END exam_E;

architecture task9 of exam_E is

begin

  exam_P: PROCESS(reset_n, clk)
    variable loopvar : std_logic_vector (3 downto 0);
  begin
    if reset_n = '0' then
      result <= "1111";
      cout <= ‘0’;
    elsif clk'event and clk='1' then
      cout <= ‘0’;
      if inC = '1' then
        result <= inA or inB;
      else
        loopvar := inA;
        for i in 0 to 3 loop
          if inB(i) = '1' then
            loopvar := loopvar(2 downto 0) & loopvar (3);
          end if;
        end loop;
        result <= loopvar;
      end if;
    end if;
  end PROCESS;

end task9;
```