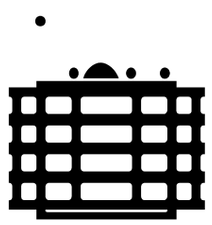
Professur Schaltkreis- und Systementwurf

Components and Architectures

Questions for Labs



TECHNISCHE UNIVERSITÄT CHEMNITZ

Questions for labs

The student draw one of the questions according to the lab from a box (blind).

The answer should have a maximum length of 3 sentences.

There is no 2nd attempt/question if answer is wrong.

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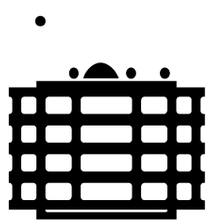
Components and Architectures

Lab1 - Introduction to DLX



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Introduction to DLX

What are the main parts of a von-Neumann-Machine?

Introduction to DLX

Give at least 3 examples of components of a processor datapath!

Introduction to DLX

How many General-Purpose-Registers are available in the DLX processor and what is their size?

Introduction to DLX

What is the function of a program counter?

Introduction to DLX

What is the functionality of a program counter?

Introduction to DLX

What will happen when the instruction

ld f6, 62

is executed?

Introduction to DLX

What will happen when the instruction

sw 10, r5

is executed?

Introduction to DLX

Please explain the instruction:

sgti r1, r2, r3

Introduction to DLX

What happens if the DLX simulator executes the instruction

```
trap #0
```

Introduction to DLX

What is the meaning of the “opcode”?

Introduction to DLX

What is the difference between a branch and a jump instruction?

Introduction to DLX

What is the meaning of the abbreviation “RISC”?

Is the DLX processor RISC or not?

Introduction to DLX

What happens when you type in the Linux terminal:

cd dlx

Introduction to DLX

What happens when you type in the Linux terminal:

cp file1.asm mydirectory/file2.asm

Introduction to DLX

What happens when you type in the Linux terminal:

cd dlx

Introduction to DLX

Why is it better to use a decrementing loop compared to an incrementing loop in DLX assembly?

Introduction to DLX

Name the phases of instruction execution in the standard DLX processor.

Introduction to DLX

What happens in the IF instruction execution phase?

Introduction to DLX

What happens in the ID instruction execution phase?

Introduction to DLX

What happens in the MEM instruction execution phase?

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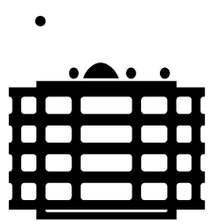
Lab2 - Introduction to Pipelining



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Introduction to Pipelining

What is an “overlapped instruction execution”?

Introduction to Pipelining

What is a pipeline hazard in general words?

Introduction to Pipelining

Explain in short words a “structural hazard”.

Introduction to Pipelining

Explain in short words a “control hazard”.

Introduction to Pipelining

Explain in short words a “data hazard”.

Introduction to Pipelining

Give a code example for a RAW hazard

Introduction to Pipelining

Give a code example for an RAW hazard.

Introduction to Pipelining

Give a code example for a WAW hazard.

Introduction to Pipelining

Give a code example for a WAR hazard.

Introduction to Pipelining

Give two examples for a pipeline stage.

Introduction to Pipelining

What is a machine cycle? Who determines the length of a machine cycle?

Introduction to Pipelining

What is the speed-up of a 6-stage-pipeline compared to a standard machine if the pipeline overhead is neglected?

Introduction to Pipelining

What is “latency” in a pipelined machine?

Introduction to Pipelining

What is a “stall” in a pipelined machine?

Introduction to Pipelining

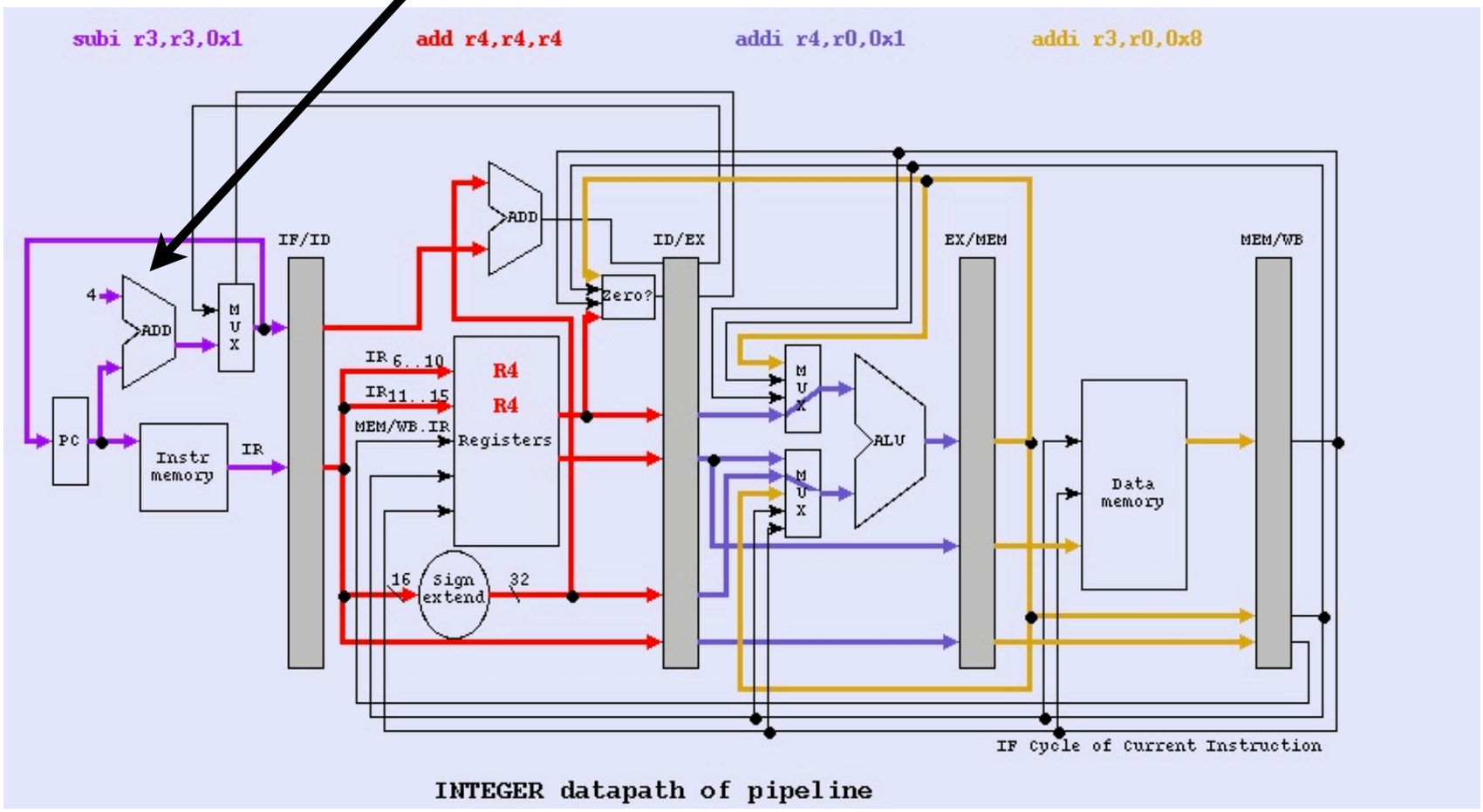
Which type of hazard is reduced by the “Forwarding”-mechanism?

Introduction to Pipelining

Which type of instruction is causing a “delayed slot”?

Introduction to Pipelining

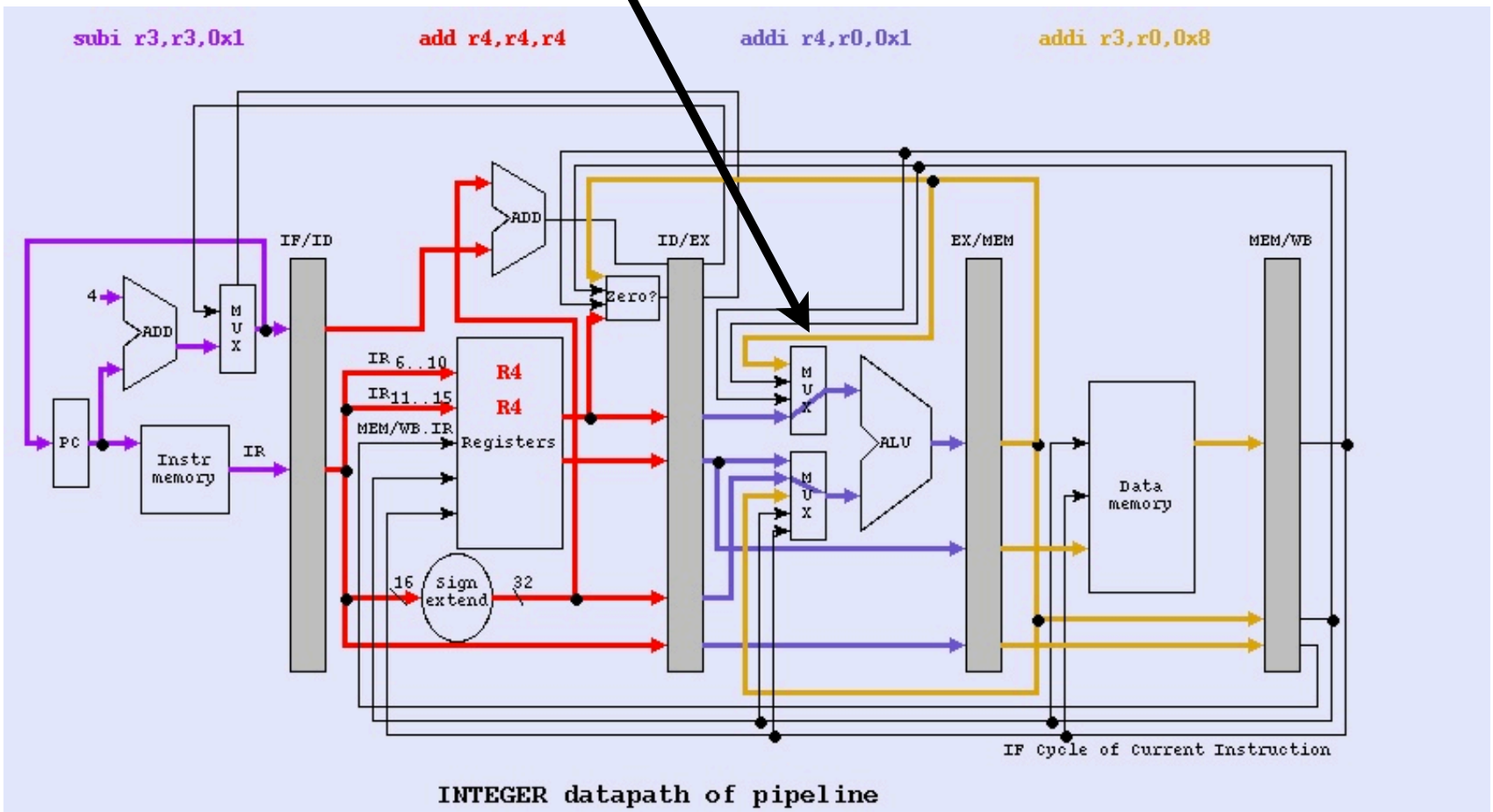
What is the purpose of the adder in the IF stage?



INTEGER datapath of pipeline

Introduction to Pipelining

What is the purpose of the MUX in the EX stage?



INTEGER datapath of pipeline

Introduction to Pipelining

Which data dependencies occur in the following code segment?

addd f6, f4, f2

addd f4, f6, f12

Introduction to Pipelining

Which data dependencies occur in the following code segment?

addi r4, r3, 2

sw 8(r3), r4

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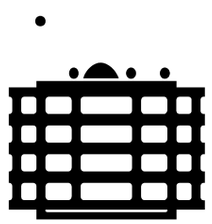
Lab3 - Dynamic Scheduling



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Freitag, 10. Oktober 14

Dynamic Scheduling

What is the difference between dynamic and static scheduling?

Dynamic Scheduling

What is an “out-of-order”-execution of code?

Dynamic Scheduling

Which hazards may lead to stalls in a Scoreboard machine?

Dynamic Scheduling

Which hazards may lead to stalls in a Tomasulo machine?

Dynamic Scheduling

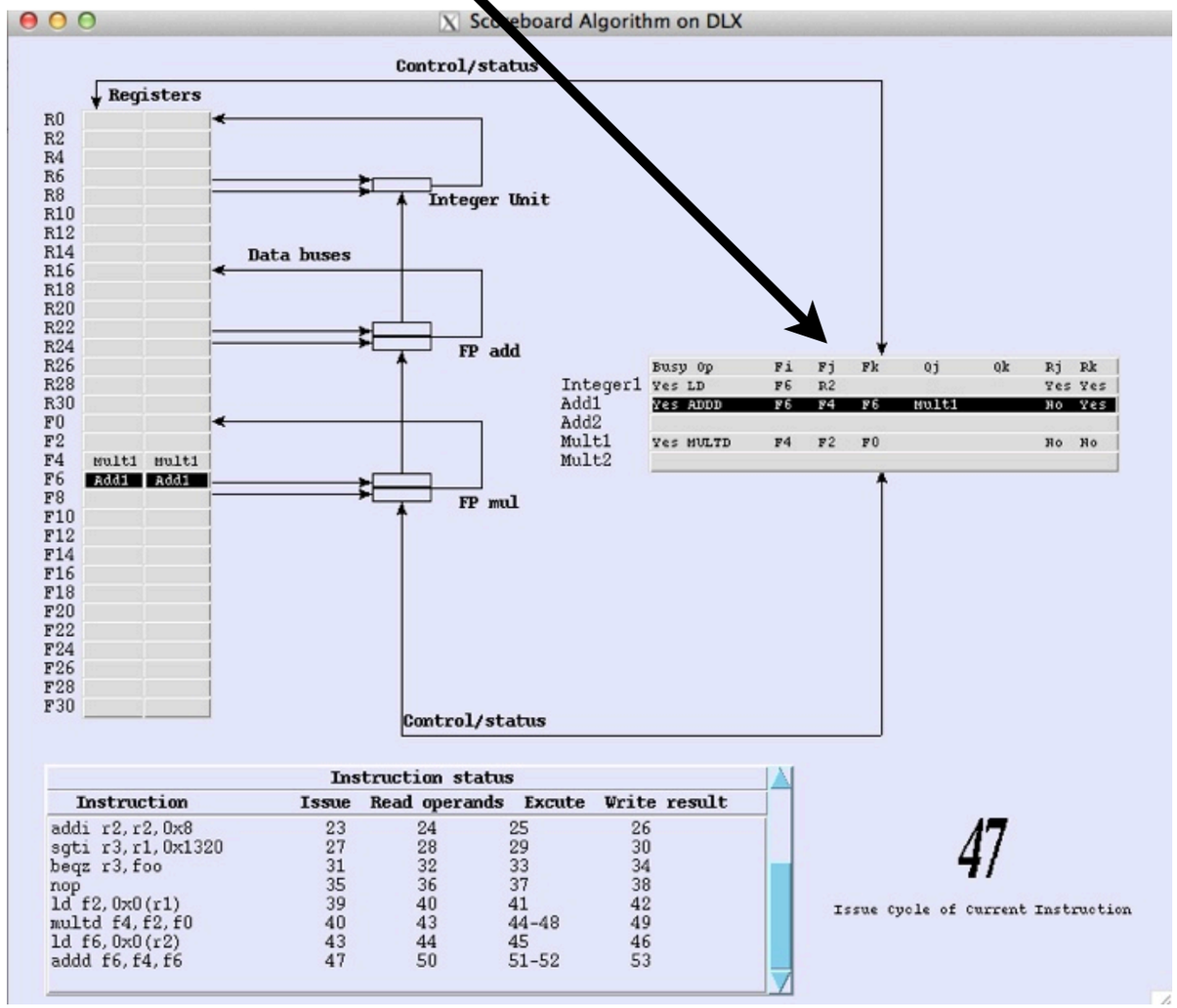
Which method to avoid stalls caused by RAW hazards is usable in Tomasulo and standard pipeline, but not in a Scoreboard?

Dynamic Scheduling

What is the functionality of the Scoreboard control unit?

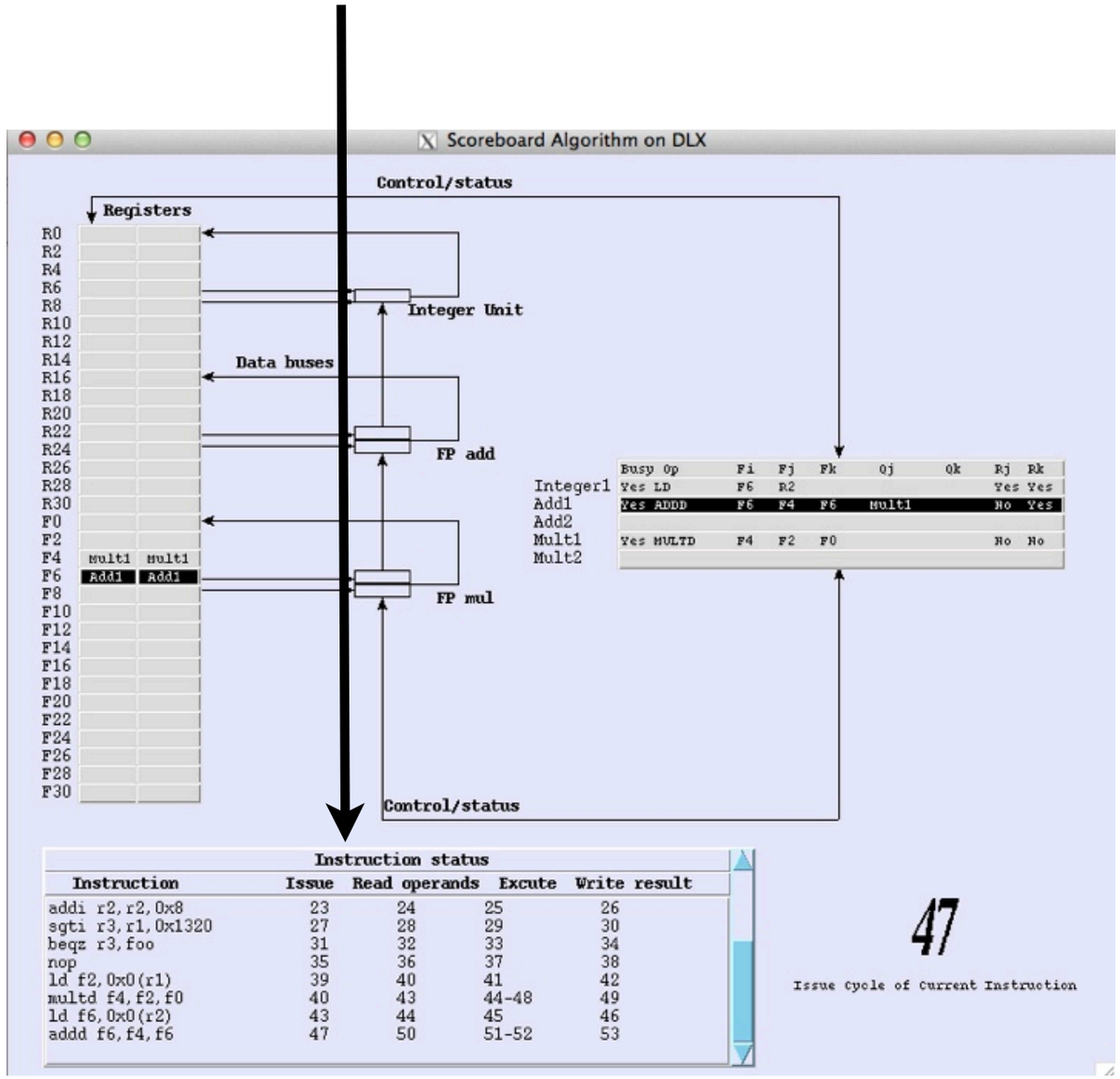
Dynamic Scheduling

What is the table on the right in a Scoreboard machine?



Dynamic Scheduling

What is the table on the bottom in a Scoreboard machine?



Dynamic Scheduling

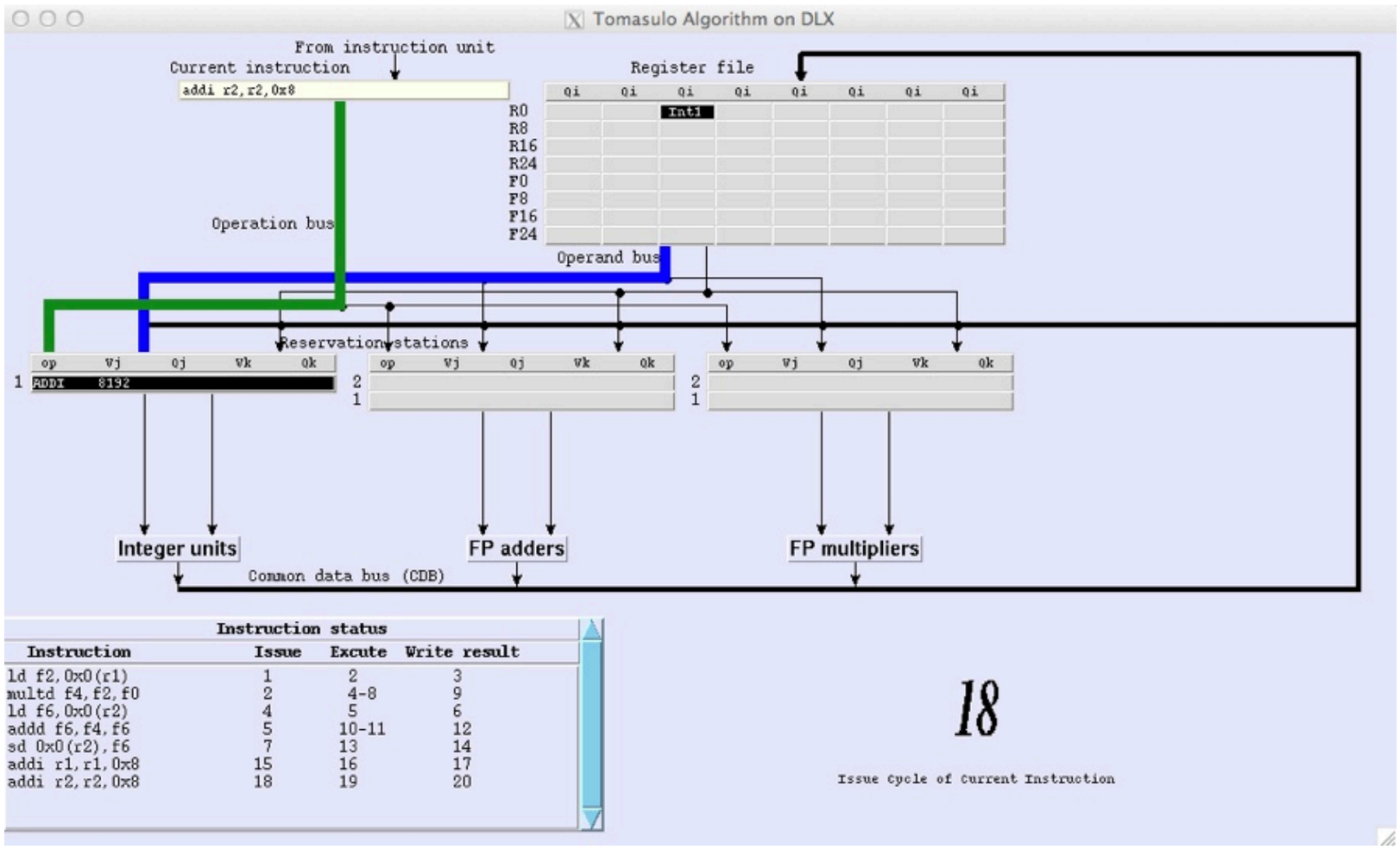
How are WAW hazards removed in the Tomasulo mechanism?

Dynamic Scheduling

How are WAR hazards removed in the Tomasulo mechanism?

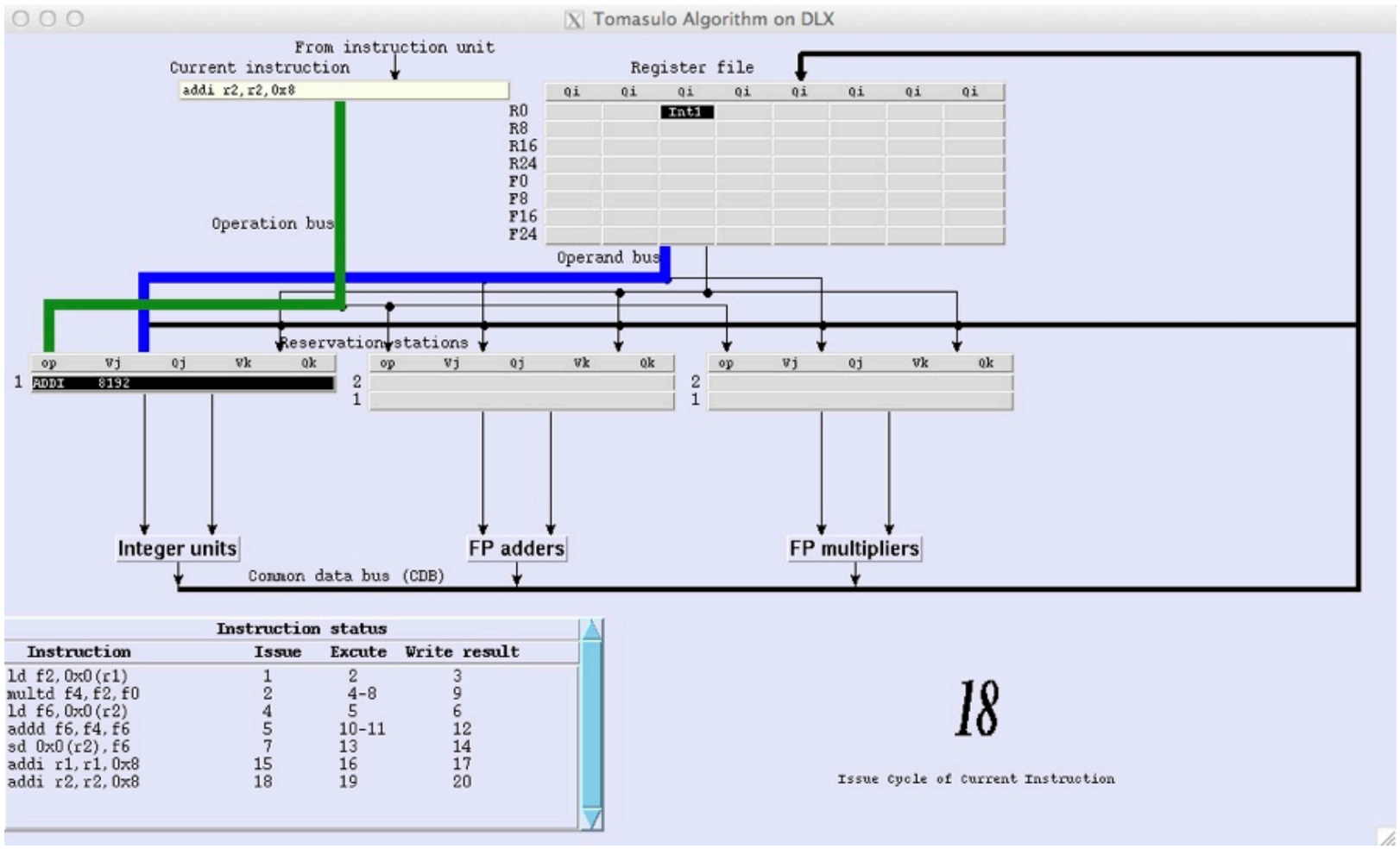
Dynamic Scheduling

Show the CDB in this Tomasulo architecture.



Dynamic Scheduling

Show the reservation stations in this Tomasulo architecture.



Dynamic Scheduling

If I have a Tomasulo machine with 3 reservation stations, two buffers and 2 CDBs - how many instructions may **start** execution in parallel?

Dynamic Scheduling

If I have a Tomasulo machine with 3 reservation stations, two buffers and 2 CDBs - how many instructions may **finish** execution in parallel?

Dynamic Scheduling

The following code is taken from f347.s. Why is the nop necessary?

```
[...]
sgti r3, r1, done
beqz r3, foo
nop
trap #0
```

Dynamic Scheduling

What is the size of the datatype “double”?

Dynamic Scheduling

Assume the following code snippet:

```
addi r2, r0, 64
sw -8(r2), f2
```

At which memory address is f2 stored?

Dynamic Scheduling

What is the purpose of the following line in the *DLX command shell*:

fget 0x20 d

Dynamic Scheduling

What is the difference between files with the ending .s and .d in DLX simulator?

Dynamic Scheduling

Which of the filetypes is mandatory for a DLX simulation: .s, .d or .i?

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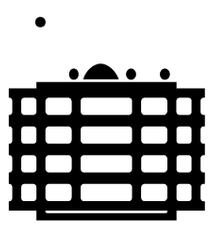
Lab4 - Loop Unrolling



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Loop Unrolling

There are no questions at the beginning of the lab - but at the end you need to explain your optimized code.