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HW/SW Codesign II

Summary

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Contents

- Estimation
- Interfaces/Synthesis
- Emulation/Rapid Prototyping
- Co-Simulation
- Co-Specification

Basics

- estimation (*Abschätzung*) is the determination of design parameters (characteristics) without implementing the system
- **definition:** Let $E(D)$ be an estimated and $M(D)$ an exact (measured) metrics of an implementation D. The _____ _____ $\boldsymbol{A}$ of the estimation is given by

$$A = 1 - \frac{|E(D) - M(D)|}{M(D)}$$

- **definition:** Let $D = \{D_1, D_2, \ldots, D_n\}$ be a set of implementations. The _____ $\boldsymbol{F}$ of an estimation method is given by

$$F = 100 \cdot \frac{2}{n(n-1)} \cdot \sum_{i=1}^{n} \sum_{j=i+1}^{n} \mu_{i,j} \qquad \mu_{i,j} = \begin{cases} 1, & if \quad (E(D_i) > E(D_j) \wedge M(D_i) > M(D_j)) \vee \\ & \quad (E(D_i) < E(D_j) \wedge M(D_i) < M(D_j)) \vee \\ & \quad (E(D_i) = E(D_j) \wedge M(D_i) = M(D_j)) \\ 0, & else \end{cases}$$

Hardware

- _____
  - clock period T: depends on technology resources
  - latency L: given by the number of clock steps
  - execution time T_{ex}: $T_{ex} = T * L$
  - throughput R: $R=P/T_{ex}$ in case of pipelining with depth of P

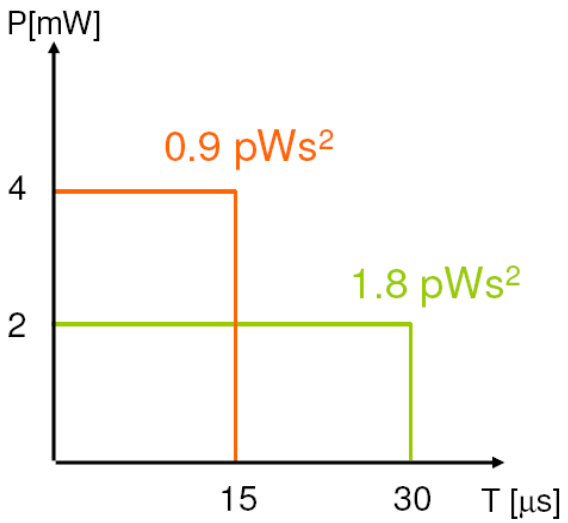
- _____
  - metrics proportional to silicon area
    - chip area in mm²
    - number of transistors, number of gates
    - number of logic blocks (FPGA)
  - package
  - number of I/O pins

Energy Consumption (I)

- power dissipation
  - P in $[W]$
  - important for dimensioning of packaging, power supply and cooling

- energy
  - $E = P_{avg} * T_{execution}$ in $[Ws]$
  - important for mobile devices (battery life time)
  - metrics for systems that operates at a _____ rate

- energy-delay product
  - $EDP = E * T_{exe}$ in $[Ws^2]$
  - metrics for systems that operates at _____ rates



Software

- performace
  - execution time T
    - estimation on basis of source-/ intermediate-/ target code

$$T = I_C \cdot CPI \cdot \tau = \frac{I_C \cdot CPI}{f}$$

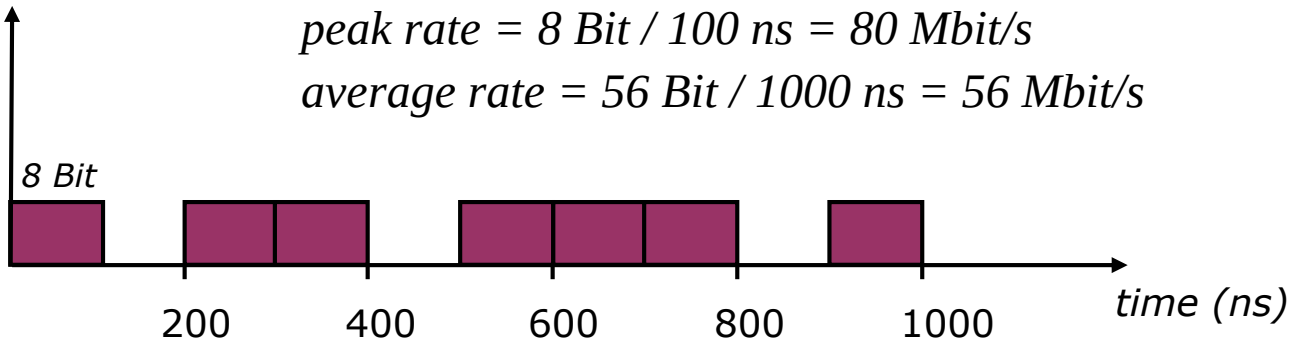
  - worst-case execution time (important for real-time systems)

    - estimation with program analysis techniques
    - modelling of cache effects possible

- cost metrics
  - size of basic block i
  - size of data memory

Communication Performance

- amount of information per time



- communication time T_{com}

$$T_{com} = T_{offset} + \frac{messagesize}{bitrate}$$

T_{offset} ...	time for initializing
messagesize ...	in bit
bitrate ...	in bit/sec

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Interface

- **definition**[1]

  An interface is a (dis)connection point of two (sub)systems. The systems can be separated at this point. The interface is defined as _____, even if it is a border of this system.

- **definition**[1]

  Hardware interfaces of communicating systems are standardised specifications about the concurrency of signals. So the information exchange is possible without taking care about the details of the complete system. Three classes of properties can be defined by the hardware interface:
  - _____ properties
  - _____ properties
  - _____ properties

[1]*Bernd Schürmann: Grundlagen der Rechnerkommunikation. Friedr. Vieweg & Sohn Verlag, Wiesbaden 2004*

P2P vs. Bus Communication

- an interface module converts internal signals of the system in standardised signals of the interface

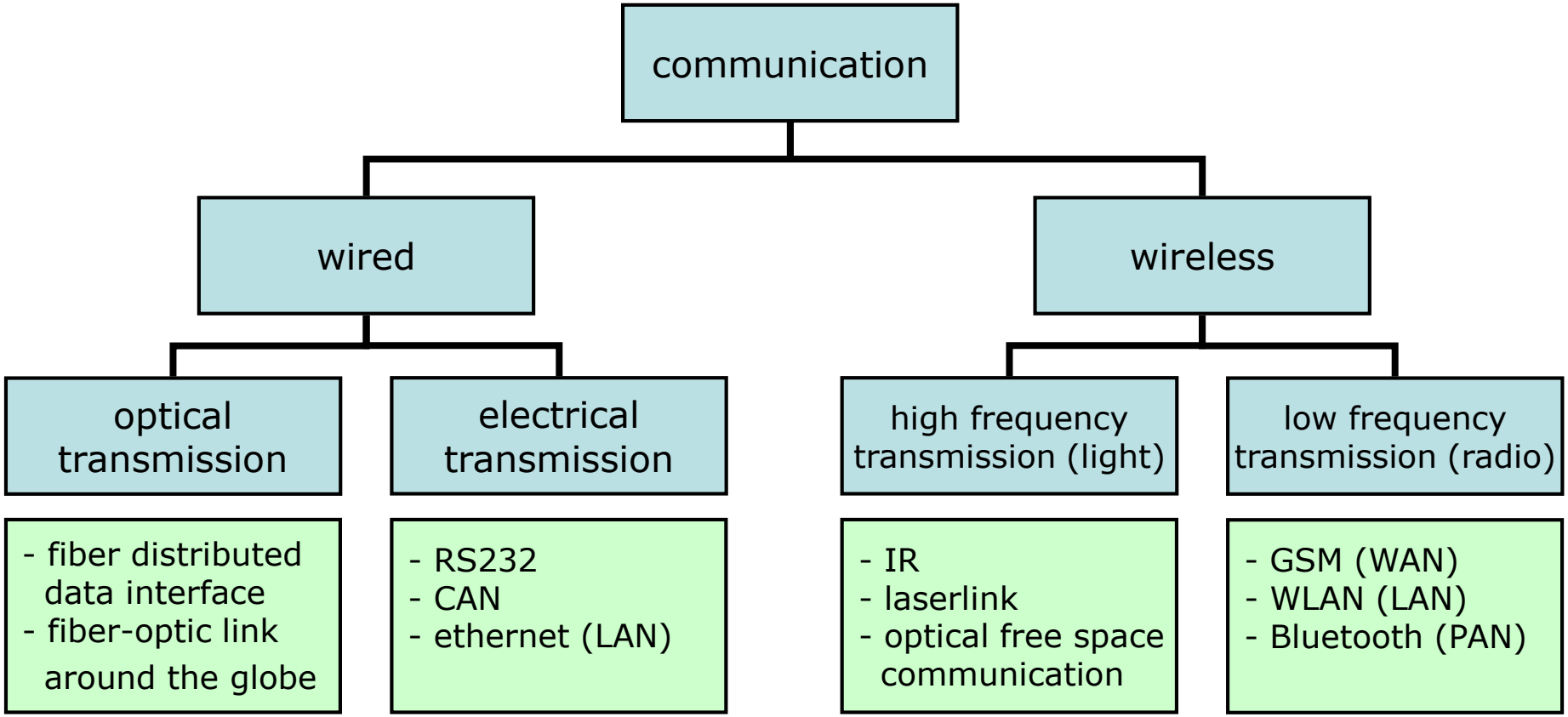
- **definition:** A communication is called point-to-point (P2P), if it is limited to _____ by (electrical, mechanical and/or functional) properties of interface module
  - intermediate stations (router, hubs, …) are not allowed

- **definition:** A bus is a multi-conductor line, which allows data- and information-interchange between different system components […]. It connects all according components of a system […]. The information-interchange between the components is realised by _____.

  → one transmitter (at one time), many (possible) receivers

Different Classification

- e.g. communication can be classified by the used transmission medium

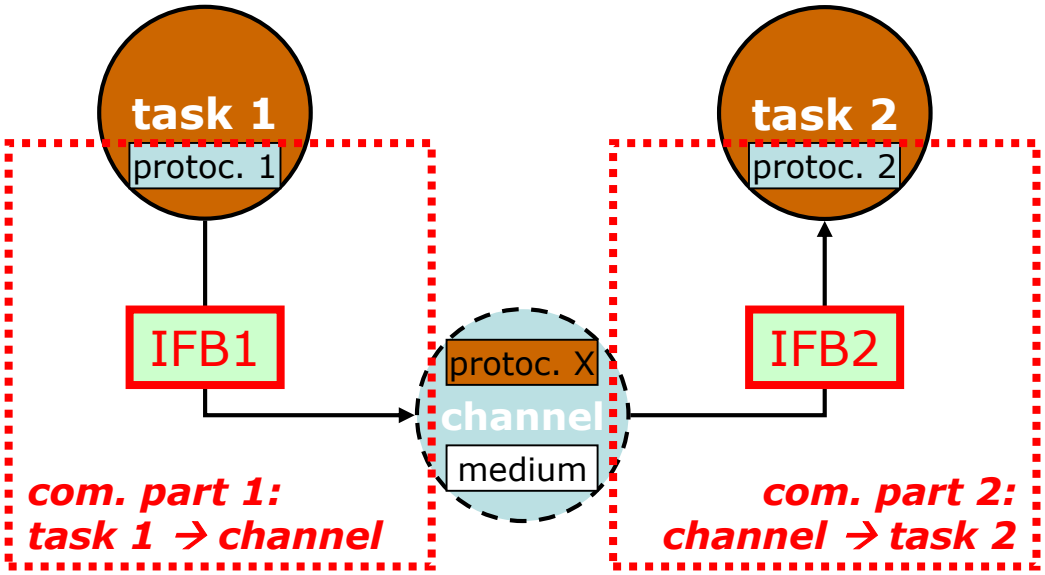


Some Wired and Wireless Interface Standards

- **EIA-232** (formerly RS232): asynchronous, serial P2P-communication
- Controller Area Network (**CAN**): fieldbus for asynchronous, serial communication
- Universal Serial Bus (**USB**): logical bus for serial communication (using physical P2P communication)
- **Bluetooth**: wireless standard for asynchronous and synchronous communication with a range from 1 up to 100m
- **WLAN**: set of wireless standards for communication in different infrastructural modes

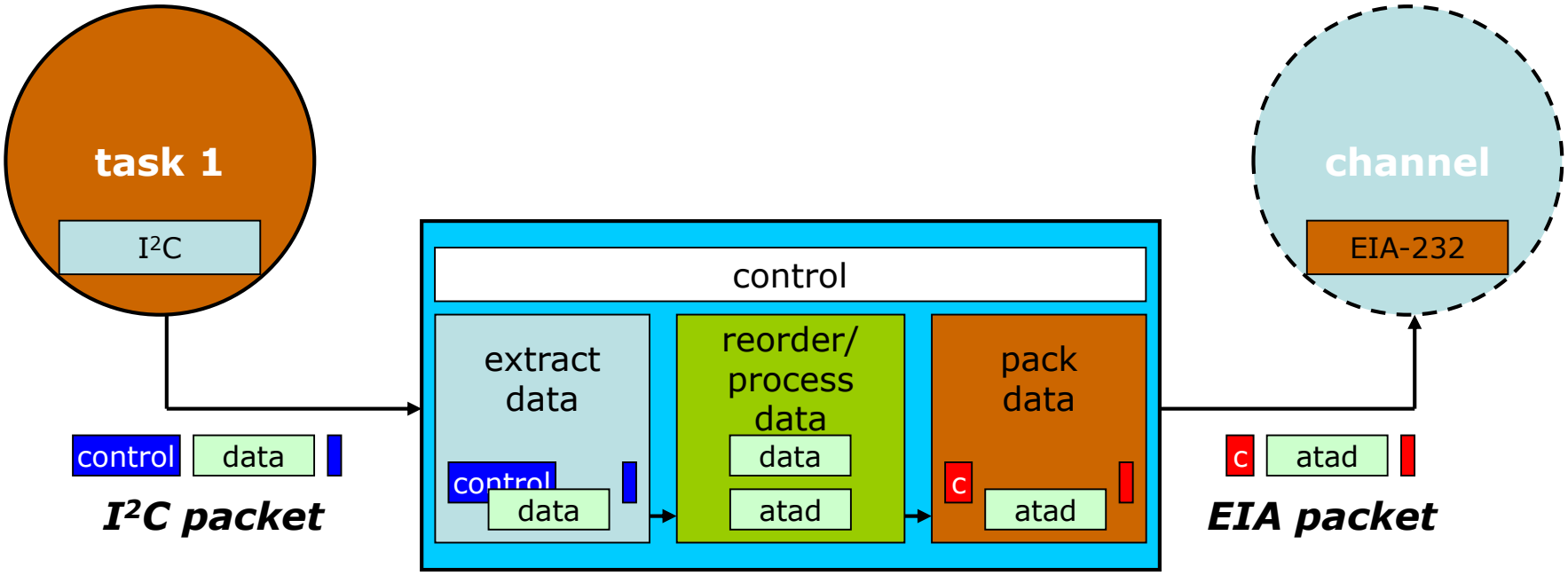
Interface Synthesis Approach

- divide communication in two parts

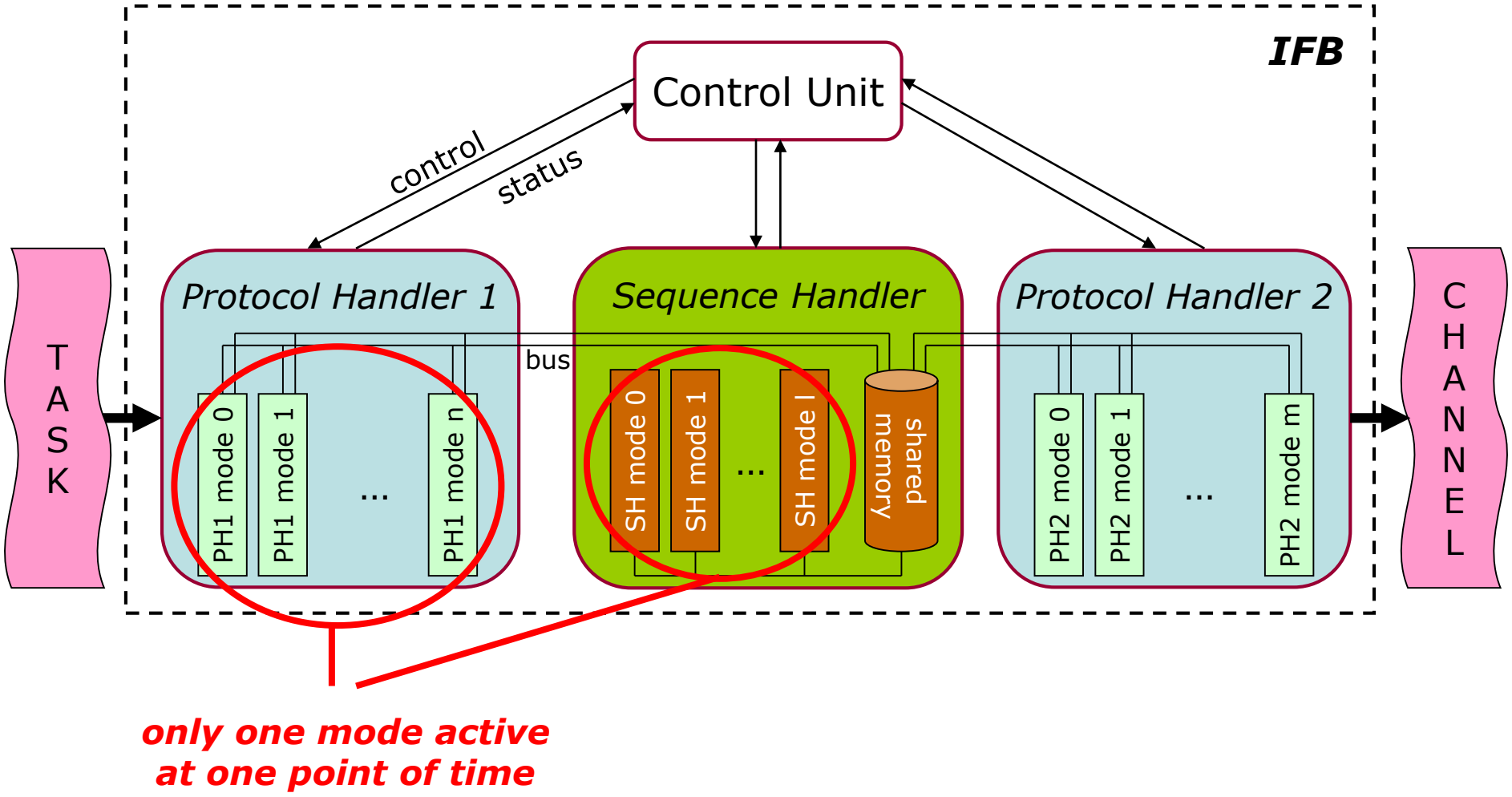


- introduce ***Interface Blocks (IFB)*** to translate between
  - protocol 1 (task 1) and protocol X (channel)
  - protocol X (channel) and protocol 2 (task 2)

Interface Block – Idea



Interface Block – Structural Template



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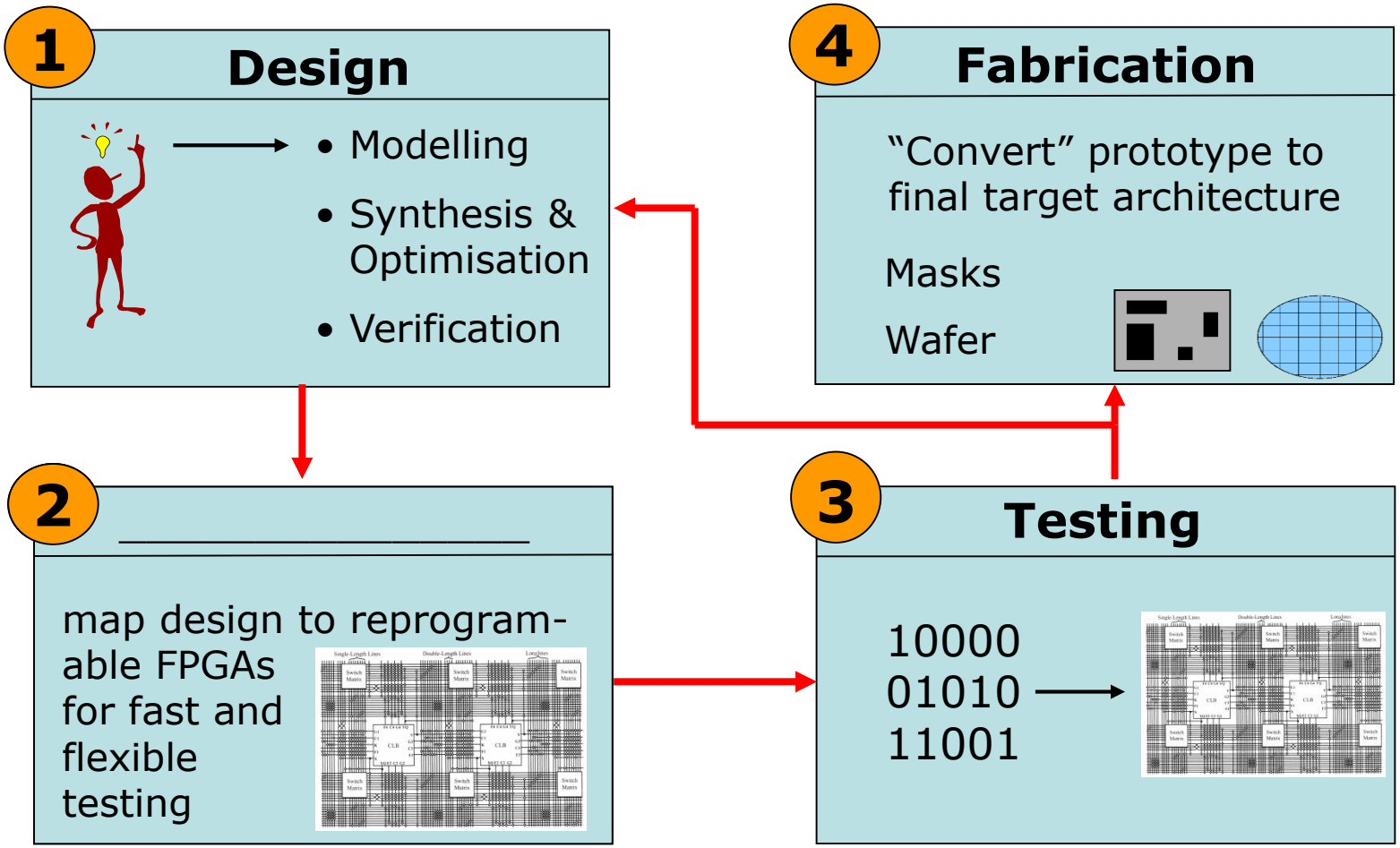
Idea


1
Design
• Modelling
• Synthesis & Optimisation
• Verification
2
map design to reprogram-able FPGAs for fast and flexible testing
3
Testing
10000
01010
11001
4
Fabrication
"Convert" prototype to final target architecture
Masks
Wafer

Prototype

- **definition**

  A prototype (of an embedded system) is an implementation with complete function coverage of the system specification and relaxed constraints for

  – _____
  – _____
  – _____

- remark
  – prototype executes functionality much faster than a simulation

Emulation Systems

- problems of FPGA based prototyping:
  - FPGA capacity is limited
  - implementation of interconnection between blocks and chips is different from final design
  - number of I/O pins is limited
  - visibility of probes (test points)

→ solution: homogeneous prototype architectures

  - minimises problems
  - limits of single technology
  - named: _____

Rapid Prototyping

- _____ uses a **heterogeneous hardware platform** (remember: emulation uses a homogenous platform)

- rapid prototyping systems offer
  - modules
    - processors
    - special chips (ASICs)
    - FPGAs
    - memory
  - flexible interconnection structure
    - FPGAs
    - FPICS (field-programmable interconnects)

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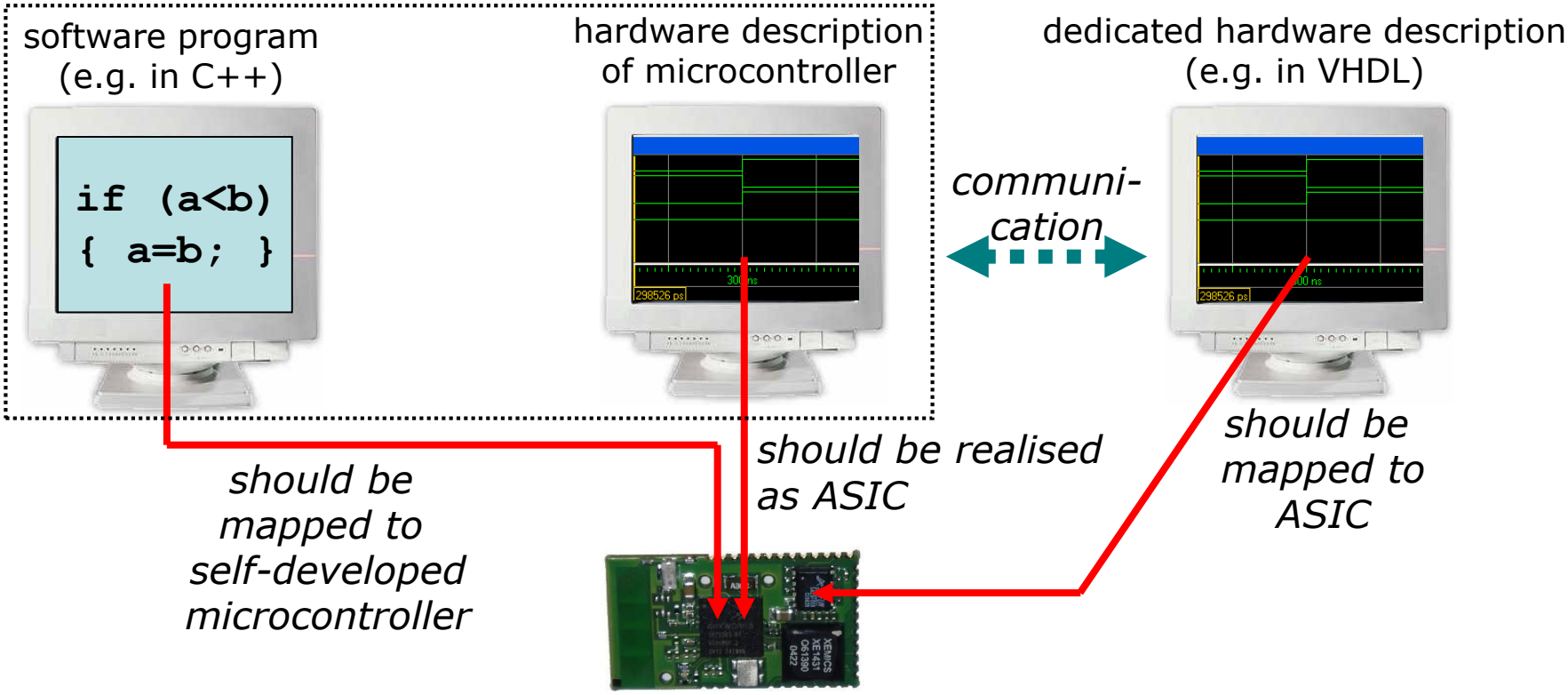
Problems in Simulation of HW/SW Systems



→ microcontroller simulated on a PC
→ hardware simulation on a PC
→ **how to run/simulate the software in a simulated MC?**
→ **how to simulate _____?**

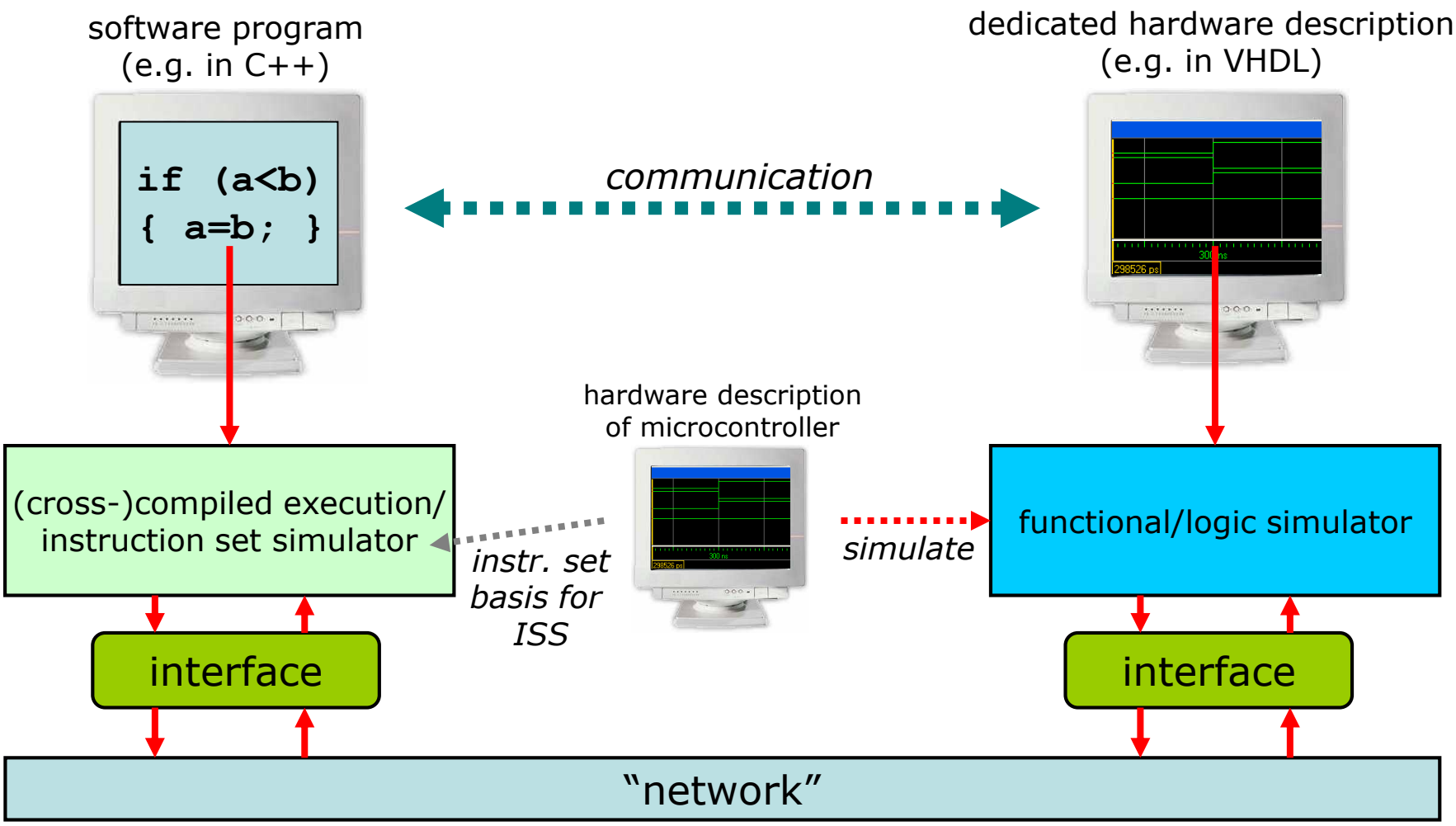
Co-Simulation?

- **definition**

- goal is to verify as much of the whole systems functionality (hardware and software) as possible before fabricating parts of it (especially hardware)

- can also help to get rough parameters for HW/SW bi-partitioning decisions (runtime of different partitions, …)

Intuitive Idea



Possible Realisations

- use _____ and interconnect them
- advantages:
  - improve simulation speed
  - use adequate simulator with required level of simulation detail for different domains
- disadvantages:
  - common interface for simulators necessary
  - low timing details due to different simulation times on different domains
- depending on availability of target processor, related compiler, instruction set simulator, … different concepts for distribution of simulation possible:
  - exact processor model
  - bus model
  - instruction set simulator model
  - compiled model
  - hardware model

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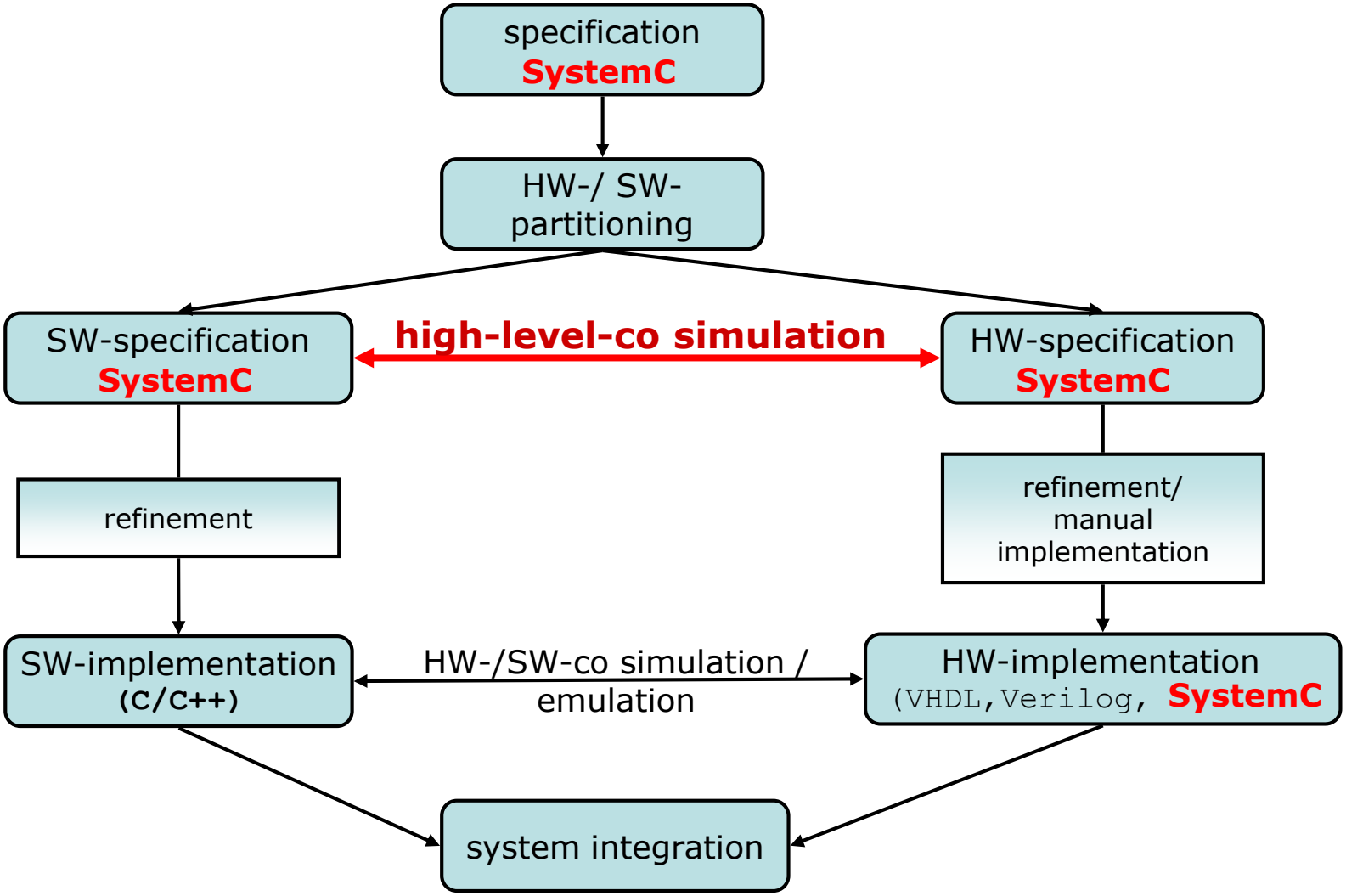
VHDL vs. SystemC

- VHDL
  - dedicated language with own syntax and semantics
  - system description on _____ level and below
  - optimised for synthesis (of synchronous systems) and simulation (on different levels)

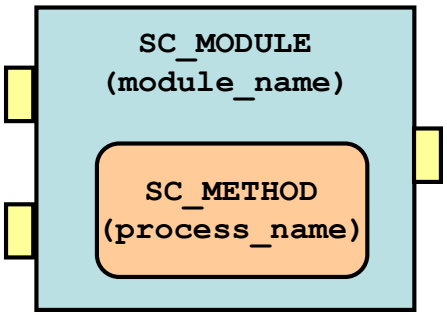
- SystemC
  - class library for C++
  - description on _____ level and (partly) below → HW and SW
  - optimised for simulation (class library contains simulation kernel) of whole system (faster but less detailed than VHDL)
  - no compiler "SystemC → executable system" yet

SystemC Design Flow



Modules

- modules are the basic building blocks
  → design partitioning
- includes:
  - processes → function
  - other modules → hierarchy
- a module is a _____




```
# include<systemc.h>

SC_MODULE(module_name)
{
  // declaration of module ports
  // declaration of local channels
  // declaration of module variables
  // declaration of processes
  // declaration of sub-modules
  // declaration of help functions
  // module instantiation

  /* module constructor */
  SC_CTOR(module_name)
  {
    // port mapping
    // module variable init.
    // process registration and
    // sensitivities
    SC_METHOD(process);
    sensitive << input1 << input2;
   }
};
```

Questions?

Exam

- _____

- written test, 90 minutes

- no facilities allowed besides
  - a **dictionary** without any personal notes
  - a **calculator** (only arithmetic calculation, without text memory)

- requirements:
  - overview over all subjects
  - detailed knowledge about definitions
  - practical usage/examples of algorithms/methods
  - **overview of practical course, basic knowledge of VHDL**

- Thank you, **good luck for exam**, and have nice holidays!