ENTWURF VON SOFTWARE FÜR EINGEBETTETE SYSTEME (SWES)

DESIGN OF SOFTWARE FOR EMBEDDED SYSTEMS (SWES)

Dr. Peter Tröger
Operating Systems Group, TU Chemnitz

COURSE ORGANIZATION

- Weekly lectures (starting today) + tutorials (starting next week)
- 5 assignment sheets, minimum of 50% of all points needed
- OPAL: News, slides (after lecture !), discussion forum, time plans
- Written final exam
- Module 565050 (adopted from Dr. habil. D. Müller)
  - Basic concepts and terminology
  - Control theory for practitioners
  - Programming for embedded systems in C and Ada
  - Model-driven development for embedded systems, PLC systems
  - Safety and security standards

THE PROJECT

- 5 weeks of project work
  - Work on a piece of embedded (real-time) software
  - Targeting Raspberry PI with extension board, available in our lab
  - Project results are submitted as assignment solutions
  - Teams of 2 persons
  - Q&A in tutorial sessions and OPAL forum
  - First project-related task with assignment sheet 3 (mid-November)

- Submission system for both non-project and project assignments
  - You hand-in either code or a PDF document —> DEMO

BASIC CONCEPTS AND TERMINOLOGY

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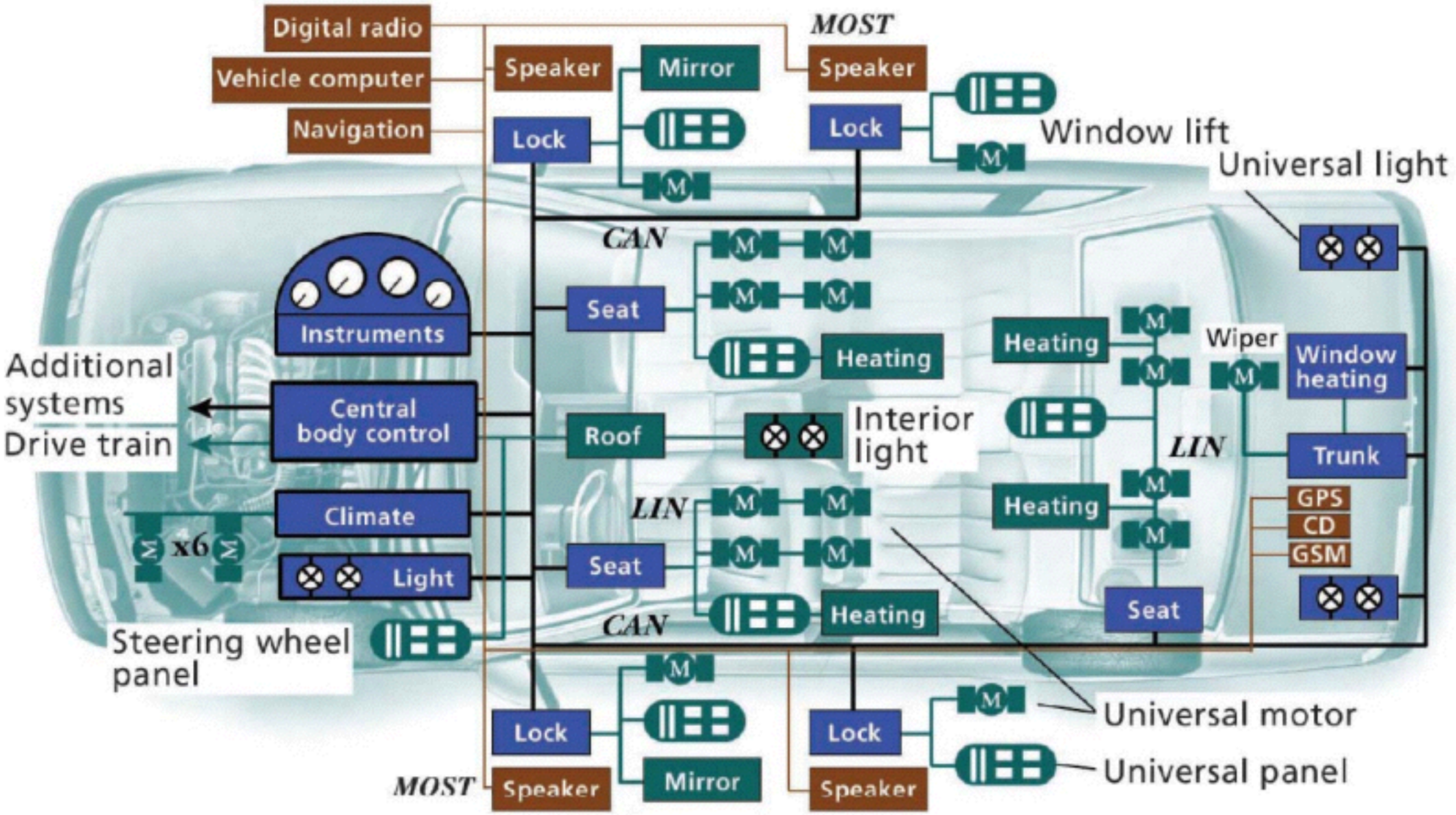
EMBEDDED SYSTEM

- Computer system in a context
  - Specific dedicated task (vs. all-purpose computer)
  - Often hardware/software co-design
  - Optimize design based on application characteristics
  - Often non-visible for user
  - Often real-time systems (max. response time ≤ deadline)
  - High cost pressure - low memory size, simple CPUs
  - Energy efficiency
- Everywhere: Cell phones, printer,s automobiles, aviation products, household devices, medical devices, children toys, …

EMBEDDED SYSTEMS



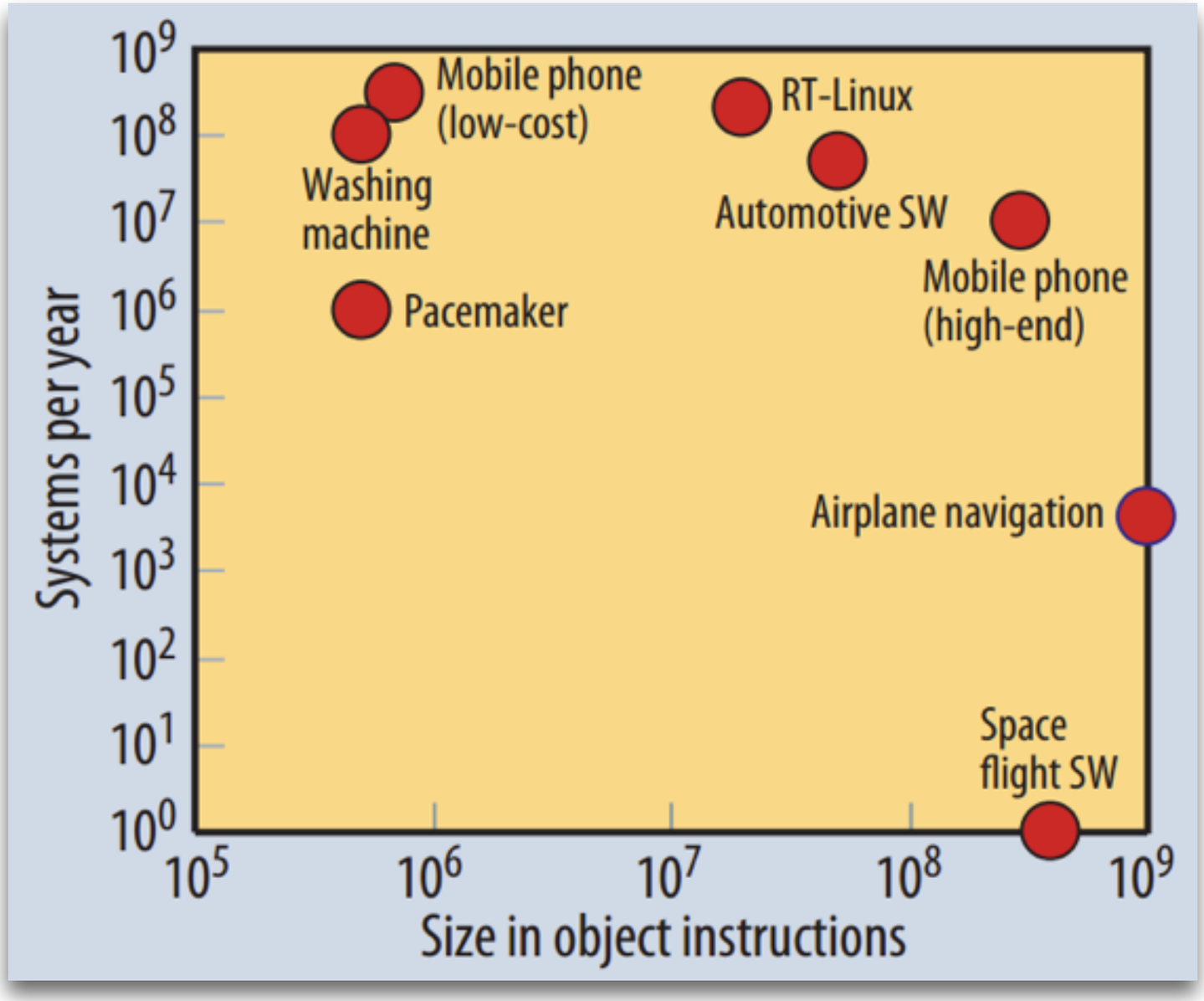
CAN Controller area network
GPS Global Positioning System
GSM Global System for Mobile Communications
LIN Local interconnect network
MOST Media-oriented systems transport

[Leen02]

[http://didik.blog.undip.ac.id/]

SOFTWARE FOR EMBEDDED SYSTEMS

- Ebert and Jones, 2009
  - Worldwide market of 160 billion €
  - ~30 embedded processors per person in developed countries
  - 98% of all produced microprocessors for embedded applications



CHALLENGES

- How to minimize power consumption and costs ?
  - Amount and type of **hardware** needed
  - Power-aware **software** and operating systems
- How can you interact with the physical world ?
  - **Hardware** sensors and actuators
  - Real-time **software** constraints
- How to ensure **non-functional properties** ?
  - 1990-2000: 40% of recalled pacemakers due to firmware errors
  - New cars with > 20 electronic control units (ECU), 1GB of software in premium car

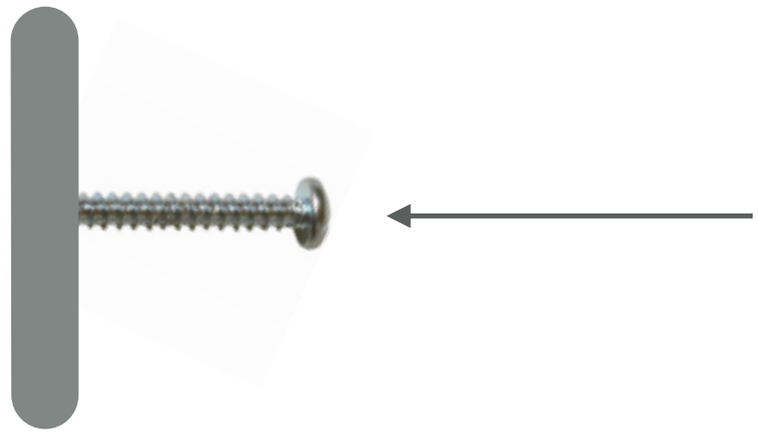
PROBLEM AREAS

Software

Hardware

Non-functional properties

HARDWARE



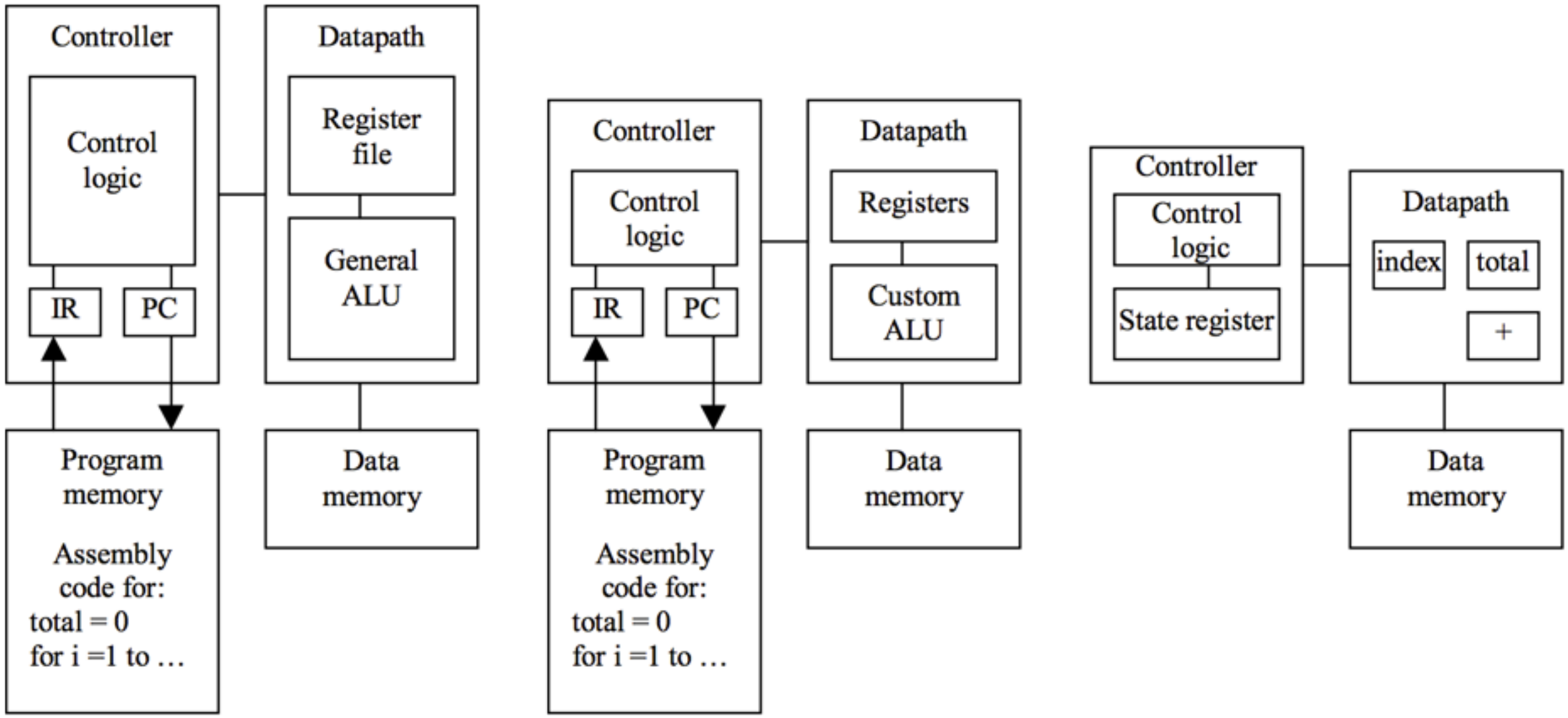
Desired functionality

General purpose

Application-specific

Single-purpose

HARDWARE



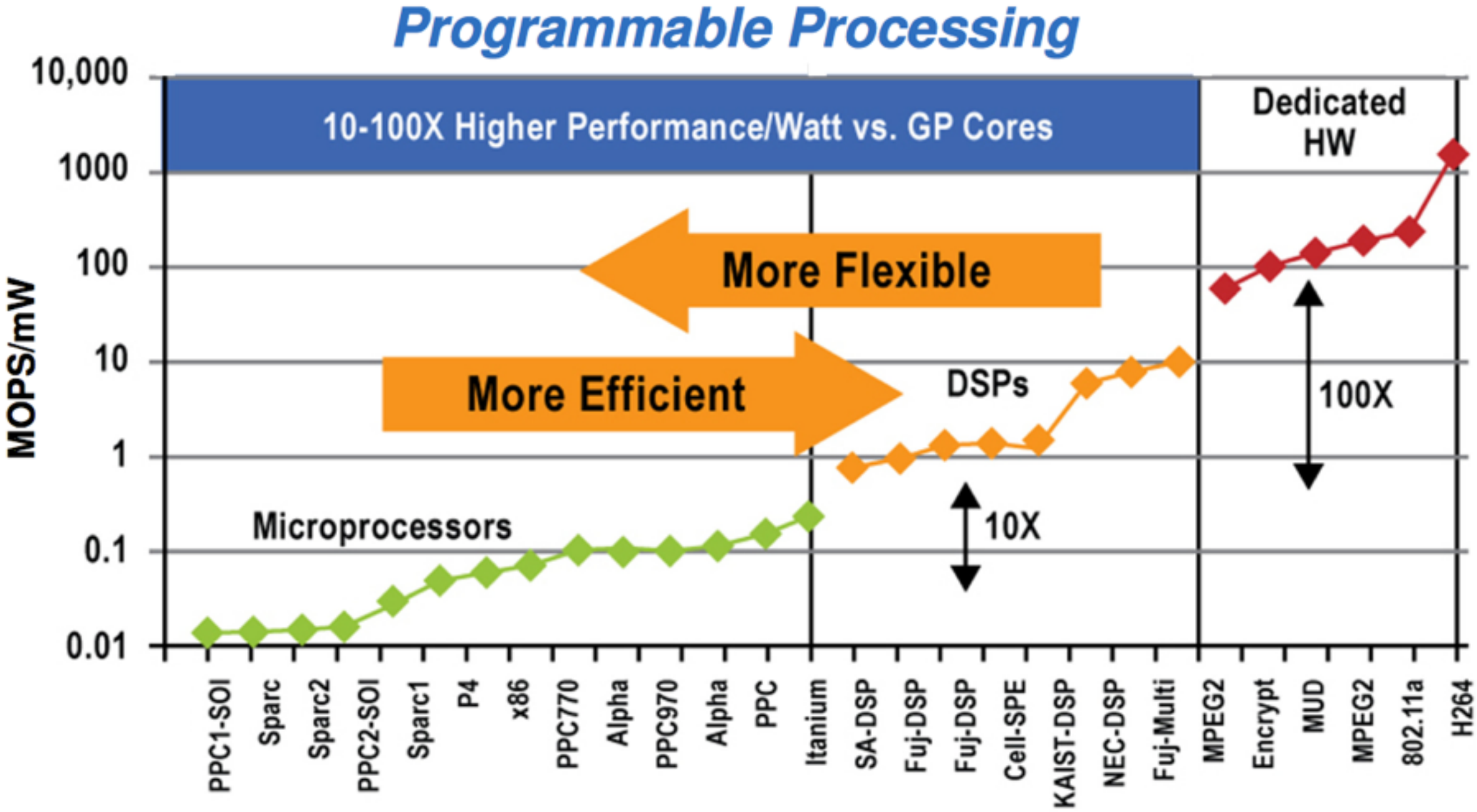
[Vahid / Givargis]

General purpose | Application-specific | Single-purpose

HARDWARE

- General-purpose hardware
  - Main goal is flexible usage with best-possible performance
  - **Programmable** for all use cases
- Application-specific hardware
  - **Programmable** for restricted performance-optimized uses cases
  - Examples: Video stream processing, audio encoding
- Single-purpose hardware
  - Integrated circuit to perform exactly one task in the fastest way
  - **Not programmable,** algorithms fixed in hardware

FLEXIBLE OR EFFICIENT?



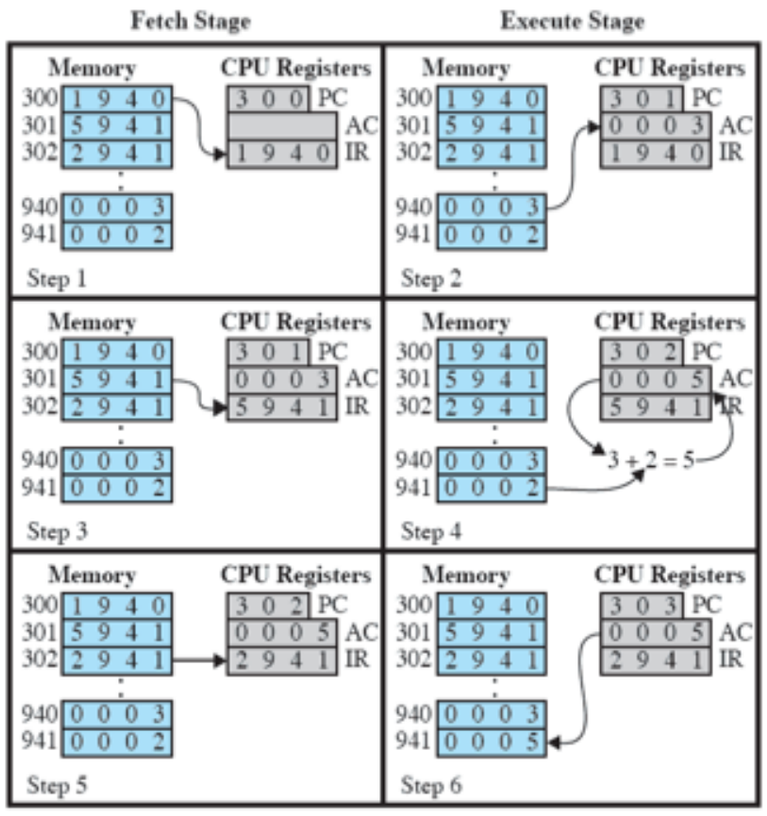
Source: "High-performance Energy-Efficient Reconfigurable Accelerator Circuits for the Sub-45nm Era" July 2011 by Ram K. Krishnamurthy, Circuits Research Labs, Intel Corp.

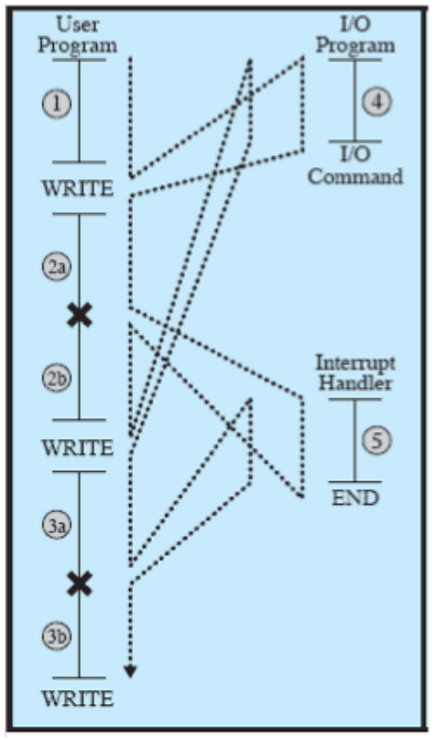
[Altera]

HARDWARE

	General purpose		Application-specific	Single purpose
Programmable in	Software	Hardware	Software	-
Performance	low	medium	medium	high
Energy Efficiency	low	medium	medium	high
Feature Flexibility	very high	medium	low	very low
Per unit price savings	low	low	medium	very high
Example	Microprocessor	PLD / FPGA	DSP	ASIC / ASSP

GENERAL PURPOSE CHIP





[Stallings]

- **Microprocessor**: Multi-purpose, programmable device
- Central Processing Units (CPUs) + volatile memory + I/O devices

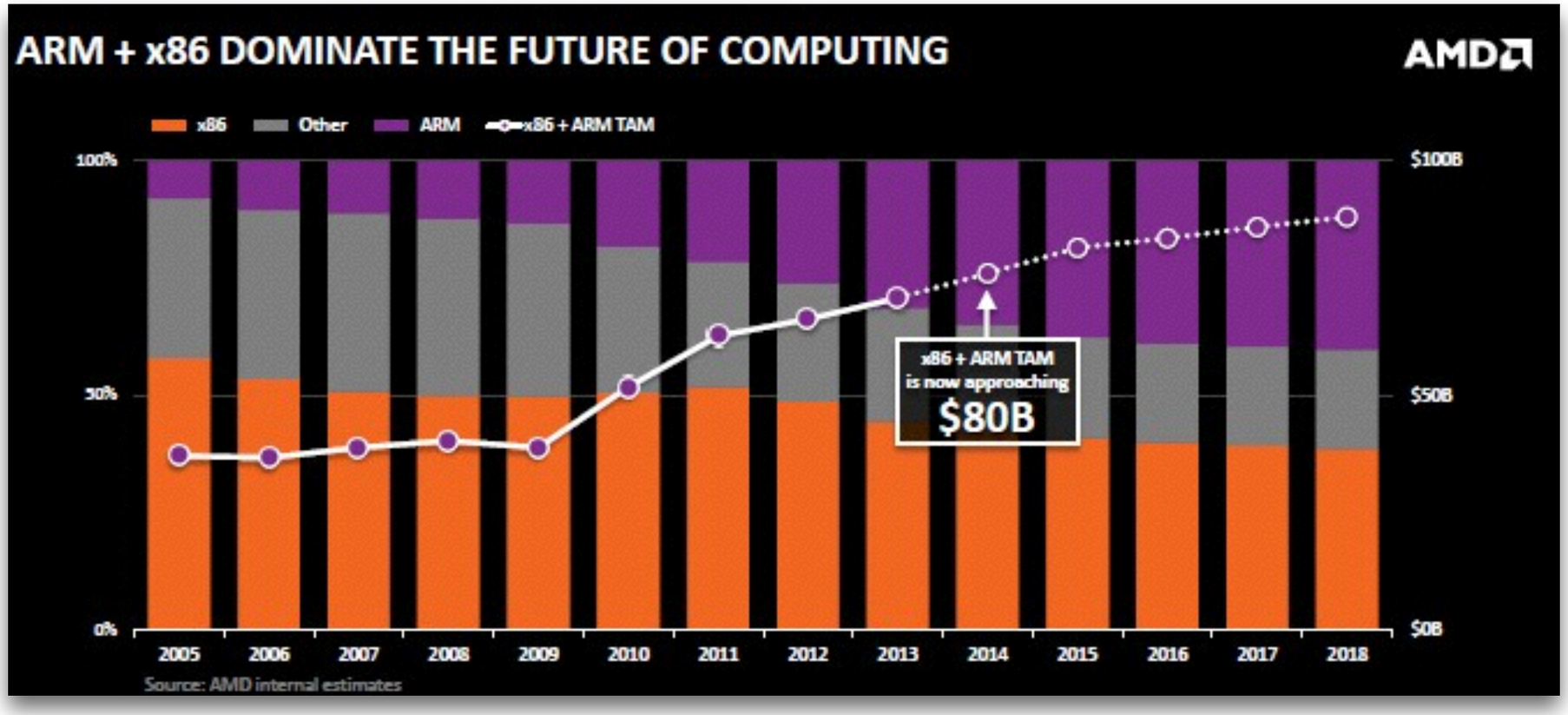
- Fetch instruction and execute it - typically memory access, computation, and / or I/O
- I/O devices and memory controller may interrupt the instruction processing

GENERAL PURPOSE CHIP

- **RISC** - Reduced Instruction Set Computer
  - MIPS, ARM, DEC Alpha, Sparc, IBM 801, Power, etc.
  - Small number of instructions, few data types in hardware
  - Instruction size constant, few addressing modes
  - Relies on optimization in software
- **CISC** - Complex Instruction Set Computer
  - VAX, Intel X86, IBM 360/370, etc.
  - Large number of complex instructions, may take multiple cycles
  - Variable length instructions, smaller code size
  - Focus on optimization in hardware
  - RISC designs lend themselves to exploitation of instruction level parallelism

ARM

- ARM design started in 1983 by Acorn Computers Ltd. Roger Wilson and Steve Furber
  - 1990 renamed to Advanced RISC Machines Ltd., 1998 renamed to ARM Ltd.
  - 32-Bit and 64-Bit RISC processor architecture
- ARM **does not manufacture itself,** licenses to others: ATMEL, Intel, IBM, Nintendo, ...
- ARM targets low-power and low-cost embedded applications



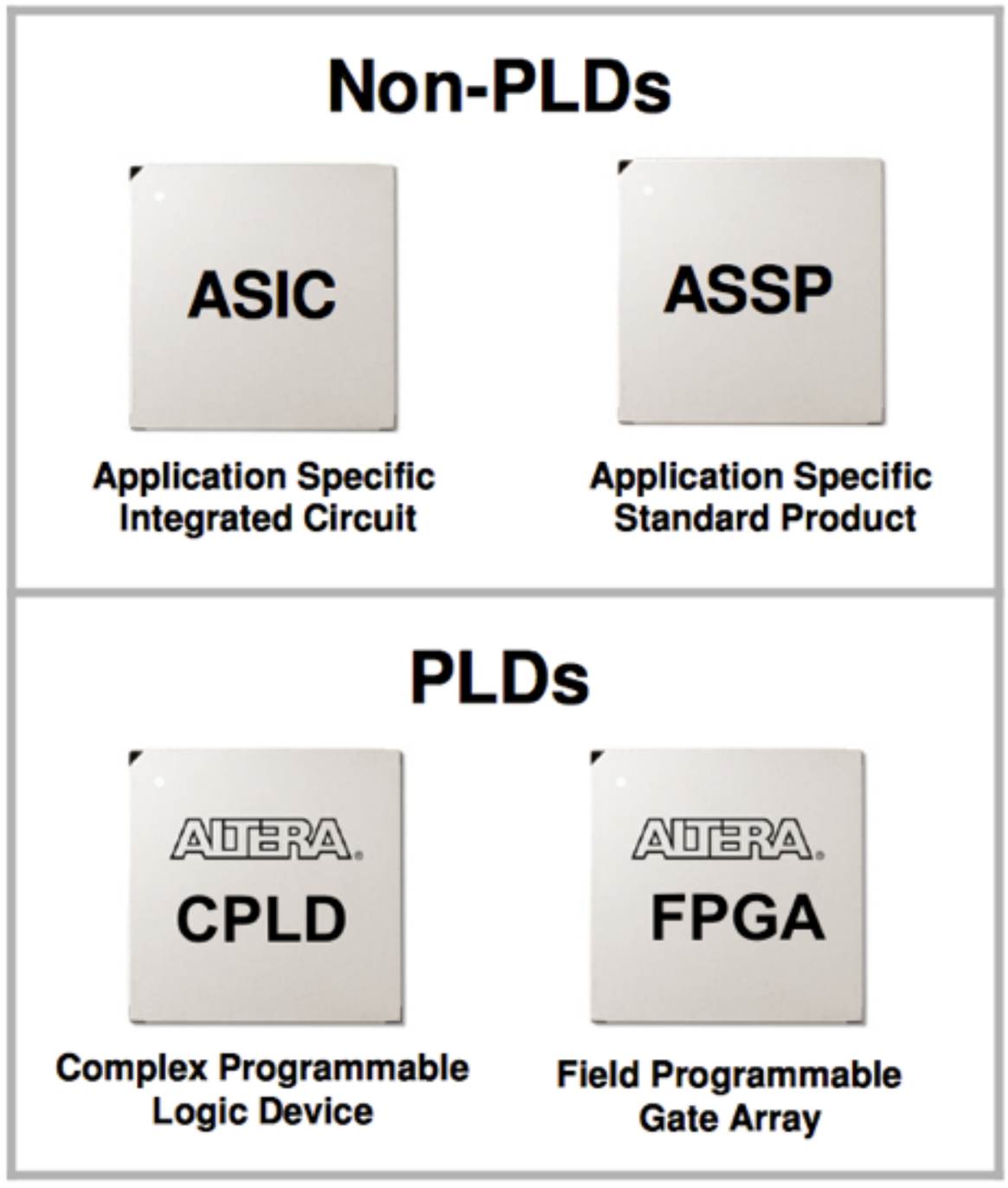
[enterprisetech.com]

GENERAL PURPOSE CHIP

- **Programmable logic device (PLD)**
  - Type of semiconductor hardware that can be „re-wired“ after production

FPGA Design Cost	3.200.000 $
FPGA Starting Unit Price	4x375 $ = 1500 $
ASIC Design Cost	85.000.000 $
ASIC Starting Unit Price	400 $
ASIC market delay	3 months
Early entry device volume	49 %

Processor Blade Example [Xilink]



[Ty Garibay, Altera]

GENERAL PURPOSE CHIP

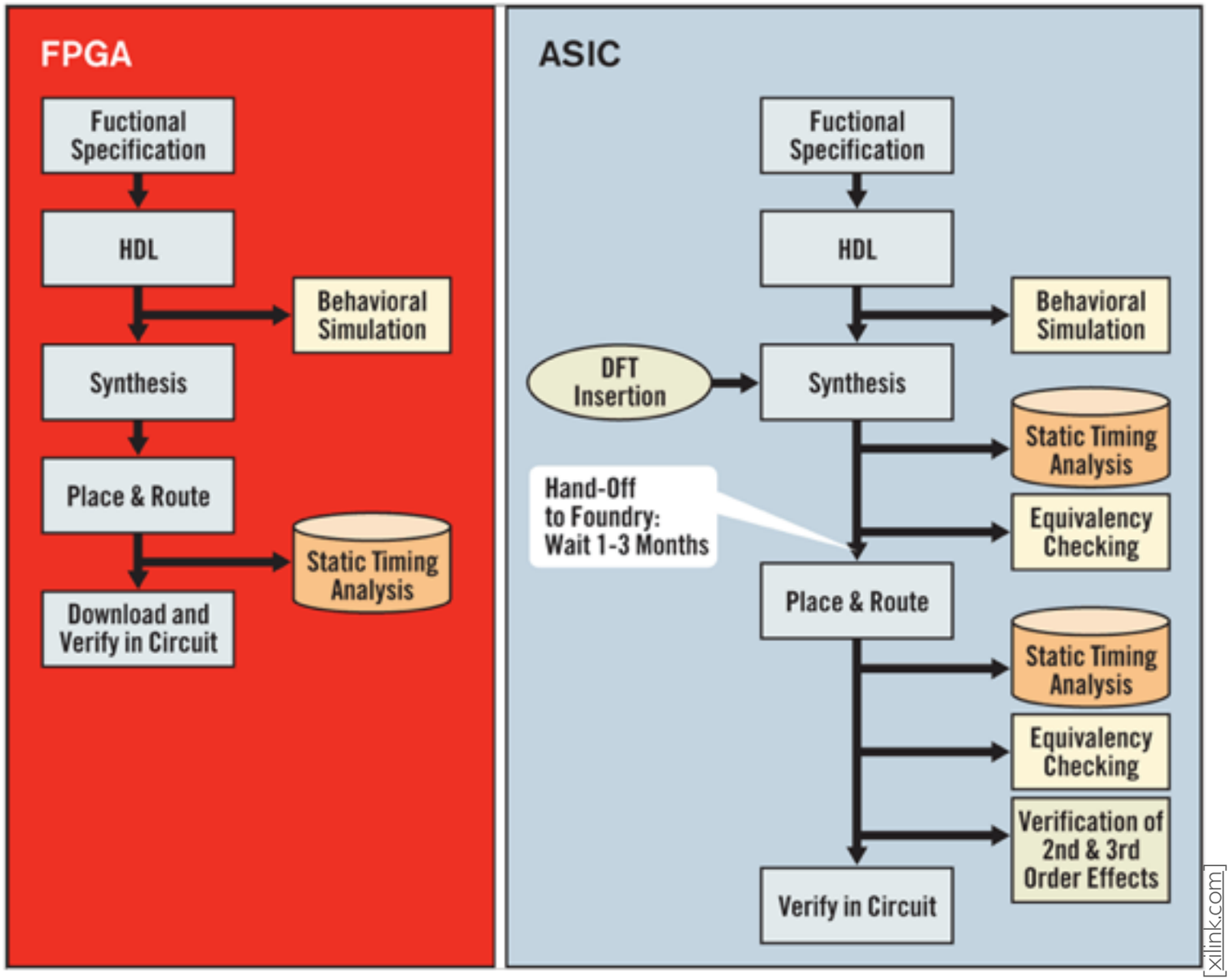
- **Field Programmable Gate Arrays (FPGA)**
  - Reconfigurable technology
    - Hardware (!) functionality can be changed at runtime
    - Errors can be corrected/masked
  - Very short development times, suitable for low number of units
  - Hardware description languages: VHDL and Verilog
  - May be used to validate ASIC design
  - SRAM- and Flash-based FPGAs allow reconfigurable computing

APPLICATION-SPECIFIC CHIP

- **Digital signal processor (DSP)**
  - Specialized microprocessor for digital processing of analogous signals
  - A/D converter for input (e.g., camera)m D/A converter for output
  - Often fixed point arithmetics (faster)
  - Real-time requirements (mostly soft RT), no multitasking
  - Multimedia applications (image and audio processing)
  - Cryptography
  - Programmable in software

SINGLE PURPOSE CHIP

- **Application-specific integrated circuit (ASIC)**
  - Hardware device for being used in one product
- **Application-specific standard part (ASSP)**
  - ASIC for re-use in multiple products (e.g. USB host controller)



PROGRAMMABILITY TRADEOFF

Software Programmability
µP: C-code DSP: C-code or Models

W

- Std-cell/Custom
- Multiple customers
- Buy & program SW

W

- Std-cell/Custom
- Multiple customers
- Buy & program SW
- Optimized for DSP

Hardware Programmability
RTL code (VHDL, Verilog)

W

- Programmable Fabric
- Multiple customers
- Buy & program HW

Limited or No Software Programmability
Embedded µP, Embedded DSP: C-code or Models

N

- Std-Cell
- Multiple customers
- Buy complete product

May contain embedded µP,DSP

N

- Std-cell
- One customer
- Provide design, buy devices

Software	*Instruction-based C-code programming or behavioral modeling Higher abstraction, less silicon efficiency*
Hardware	*RTL-based detailed design "Wired speed" efficiency*

W  *Supports wide range of applications and unit volumes*

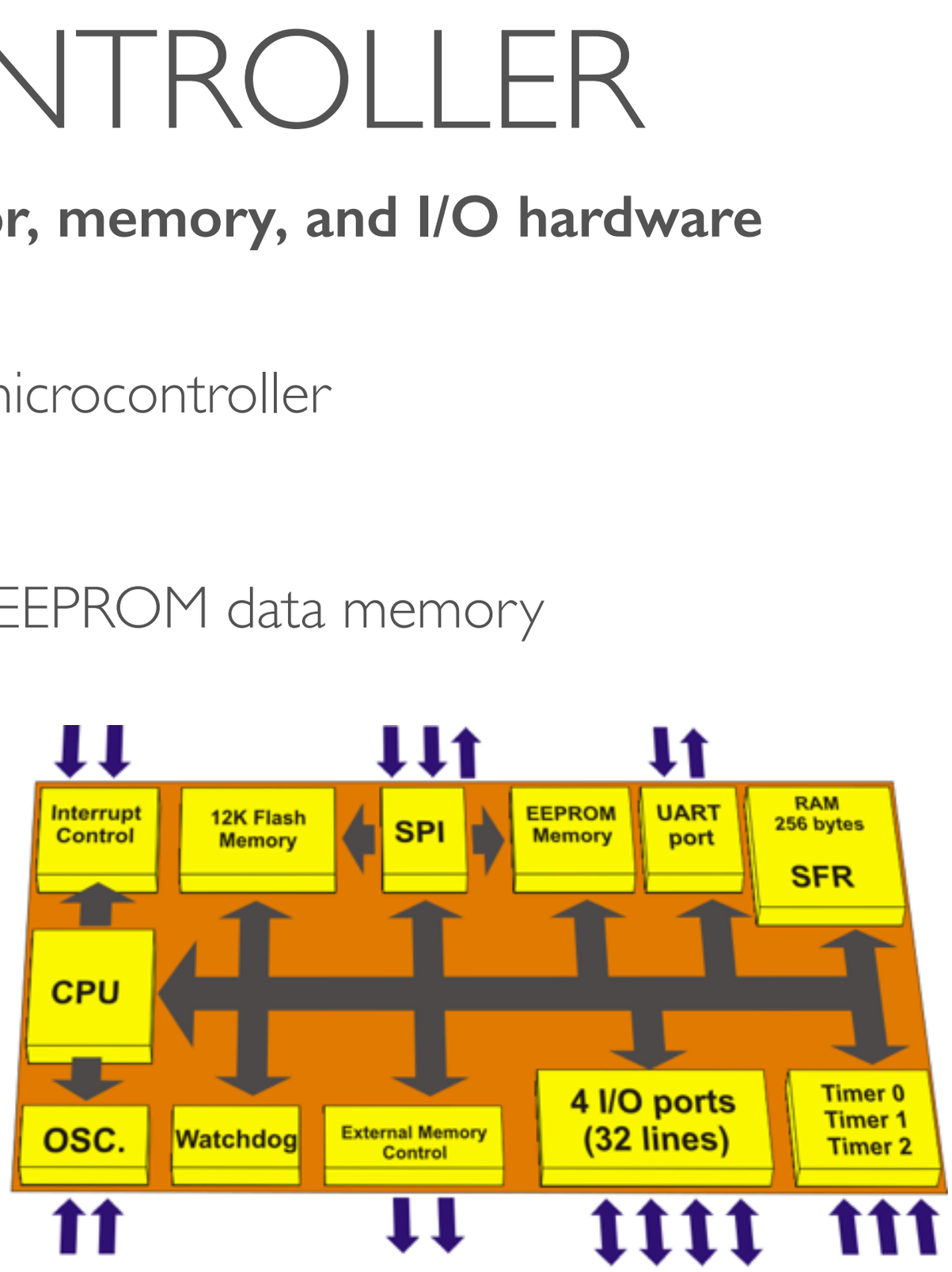
N 

Only for narrow /single applications with high unit volumes

[Ty Garibay, Altera]

MICROCONTROLLER

- **Integrated circuit with processor, memory, and I/O hardware** (µC, uC, MCU)
- Example: Atmel AT89S8253 8-bit microcontroller
  - MCS 51 instruction set
  - 12 kByte Flash memory, 2 kByte EEPROM data memory
  - 256 x 8 Bit internal RAM
  - 32 programmable I/O lines
  - UART serial port
  - Three 16-bit timers
  - 2.7V - 5.5V operating range
  - Power saving mode



[mikroe.com]

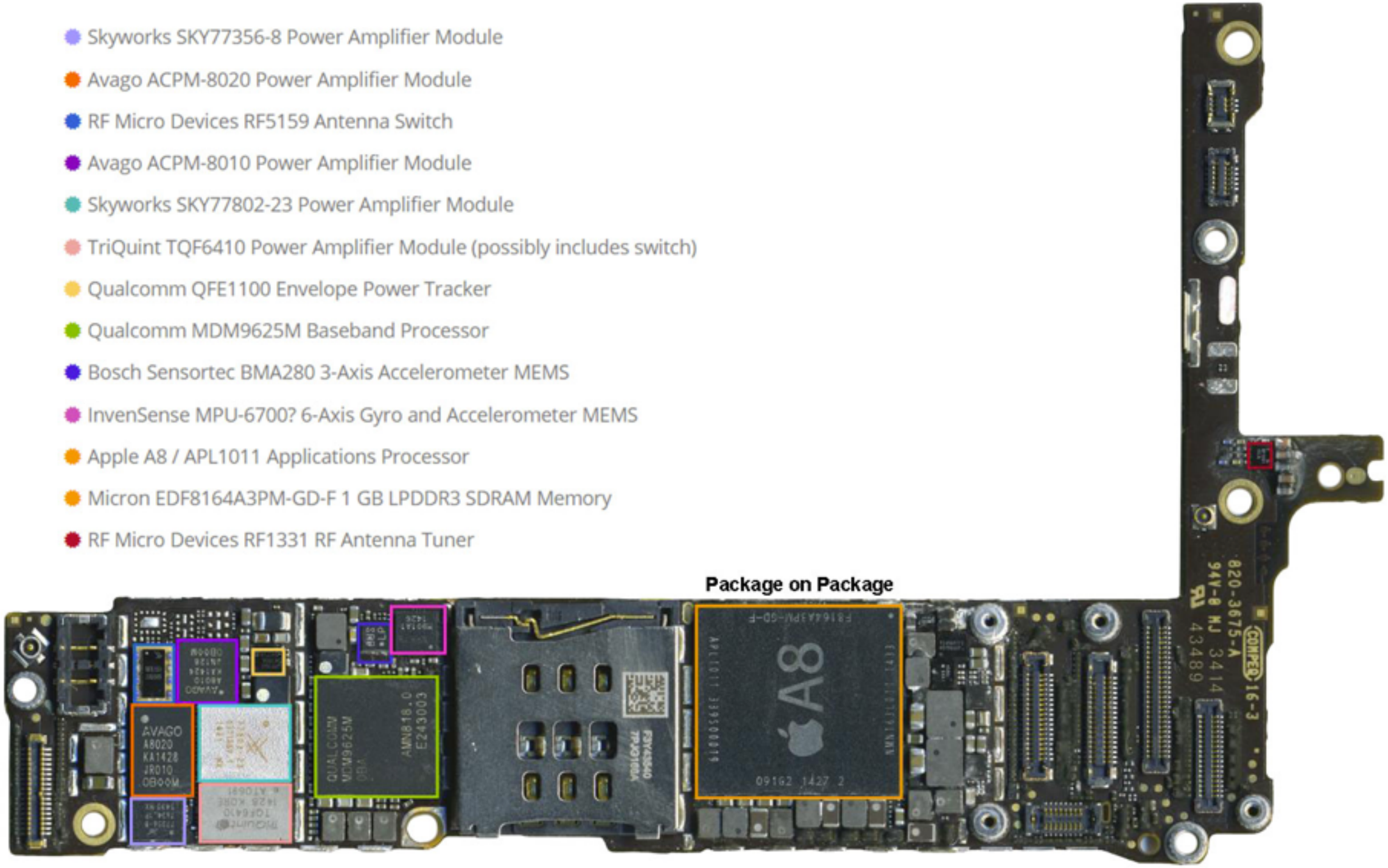
SYSTEM ON CHIP

- **System on chip (SoC)**
  - Combines functional blocks (‚IP cores‘) in one large IC
    - CPU, ROM, RAM, flash, Ethernet, Bluetooth, audio, USB, time, voltage, …
  - Soft-IP-Core in hardware description language (Verilog, VHDL)
    - Can be parameterized (cache sizes, bus sizes, …), see opencores.org
    - Licensed by companies such as ARM and MIPS
  - Hard-IP-Core already built or integrated in FPGA
  - Replace multi-chip setup, reduces power and space demands
  - Typically with debugging interface (JTAG, USB)

EXAMPLE: APPLE IPHONE 6

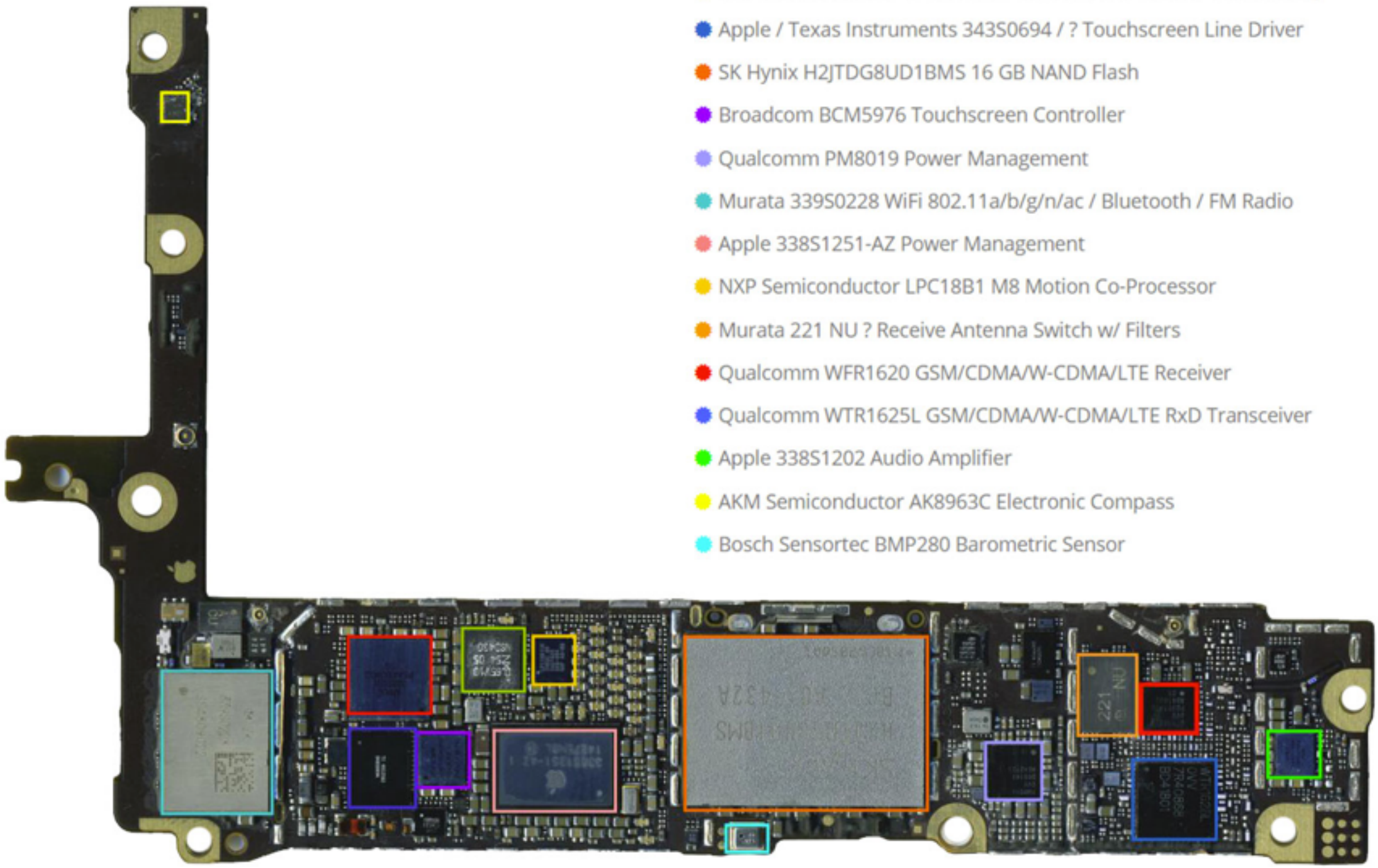
EXAMPLE: APPLE IPHONE 6

- Skyworks SKY77356-8 Power Amplifier Module
- Avago ACPM-8020 Power Amplifier Module
- RF Micro Devices RF5159 Antenna Switch
- Avago ACPM-8010 Power Amplifier Module
- Skyworks SKY77802-23 Power Amplifier Module
- TriQuint TQF6410 Power Amplifier Module (possibly includes switch)
- Qualcomm QFE1100 Envelope Power Tracker
- Qualcomm MDM9625M Baseband Processor
- Bosch Sensortec BMA280 3-Axis Accelerometer MEMS
- InvenSense MPU-6700? 6-Axis Gyro and Accelerometer MEMS
- Apple A8 / APL1011 Applications Processor
- Micron EDF8164A3PM-GD-F 1 GB LPDDR3 SDRAM Memory
- RF Micro Devices RF1331 RF Antenna Tuner



[techinsights.com]

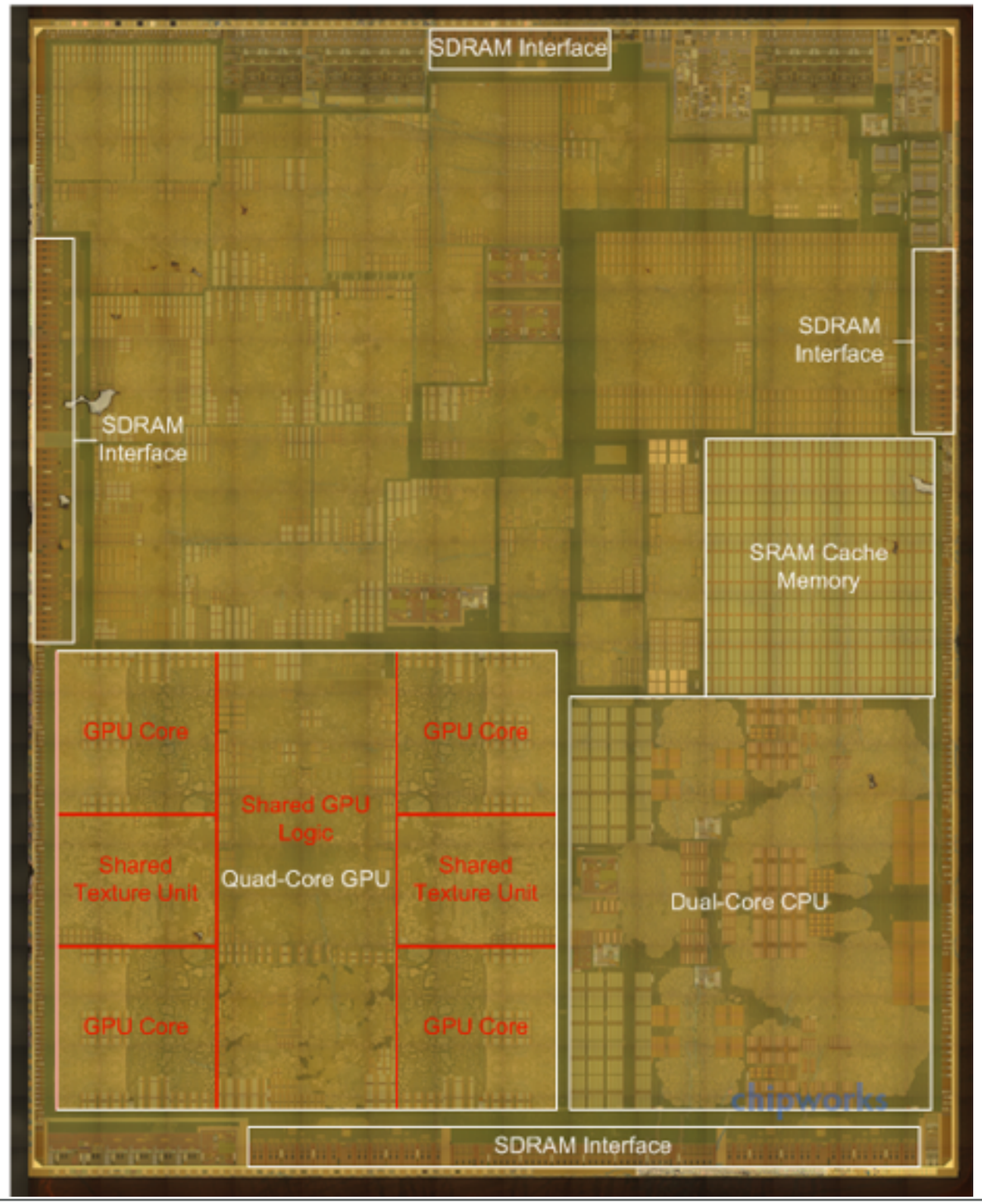
EXAMPLE: APPLE IPHONE 6



- NXP Semiconductor PN548 NFC Controller w/ Secure Element Chip
- Apple / Texas Instruments 343S0694 / ? Touchscreen Line Driver
- SK Hynix H2JTDG8UD1BMS 16 GB NAND Flash
- Broadcom BCM5976 Touchscreen Controller
- Qualcomm PM8019 Power Management
- Murata 339S0228 WiFi 802.11a/b/g/n/ac / Bluetooth / FM Radio
- Apple 338S1251-AZ Power Management
- NXP Semiconductor LPC18B1 M8 Motion Co-Processor
- Murata 221 NU ? Receive Antenna Switch w/ Filters
- Qualcomm WFR1620 GSM/CDMA/W-CDMA/LTE Receiver
- Qualcomm WTR1625L GSM/CDMA/W-CDMA/LTE RxD Transceiver
- Apple 338S1202 Audio Amplifier
- AKM Semiconductor AK8963C Electronic Compass
- Bosch Sensortec BMP280 Barometric Sensor

[techinsights.com]

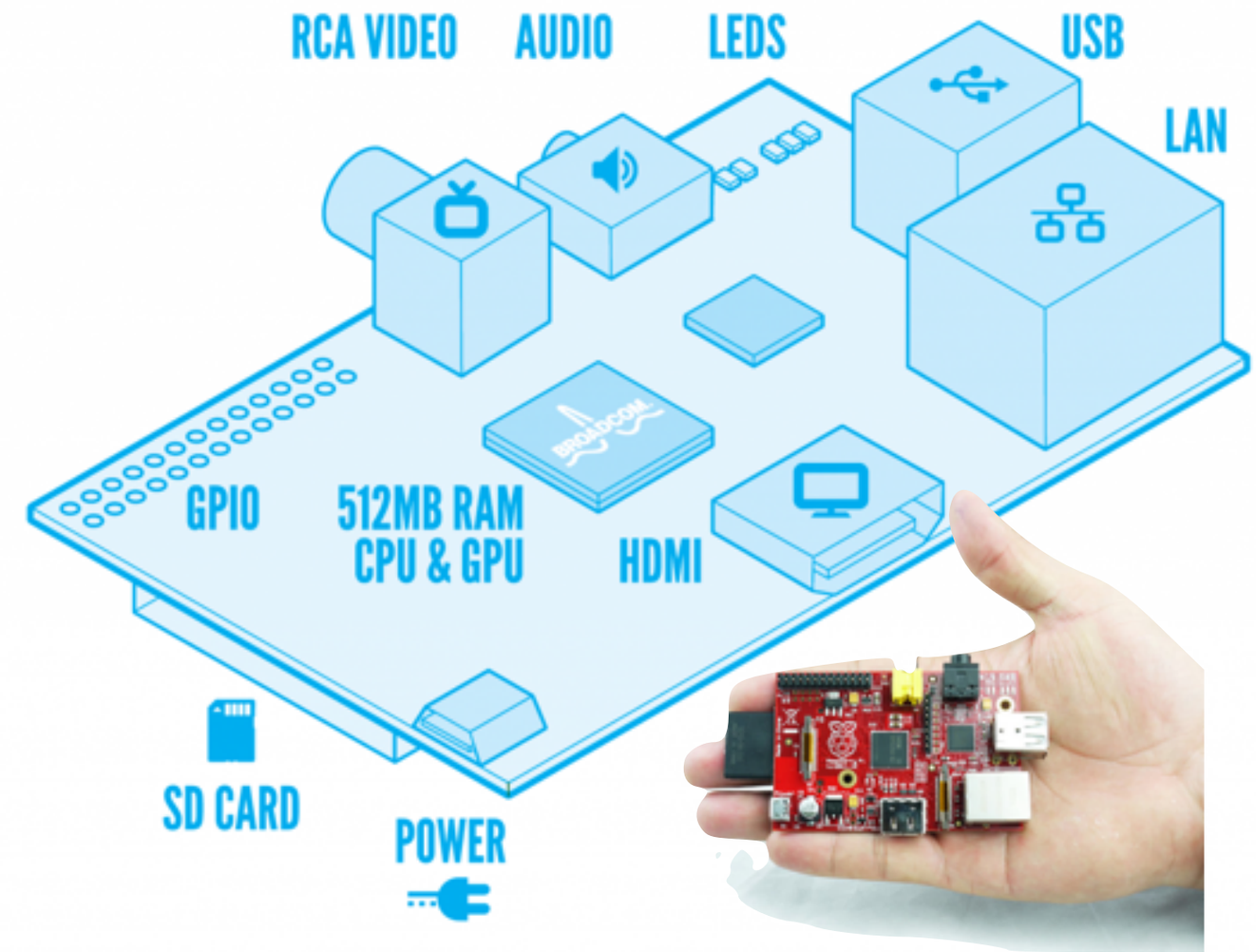
EXAMPLE: APPLE A8 SOC



[www.anandtech.com]

EXAMPLE: RASPBERRY PI

- Broadcom BCM2835 SoC
  - ARM11 processor
  - Videocore 4 GPU
  - General purpose I/O (GPIO) pins
  - Audio, USB, HDMI, I2C, UART
  - Timers
  - Interrupt controller



[raspberrypi.org]