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Hardware /Software Codesign I

Target Architectures for HW/SW Systems

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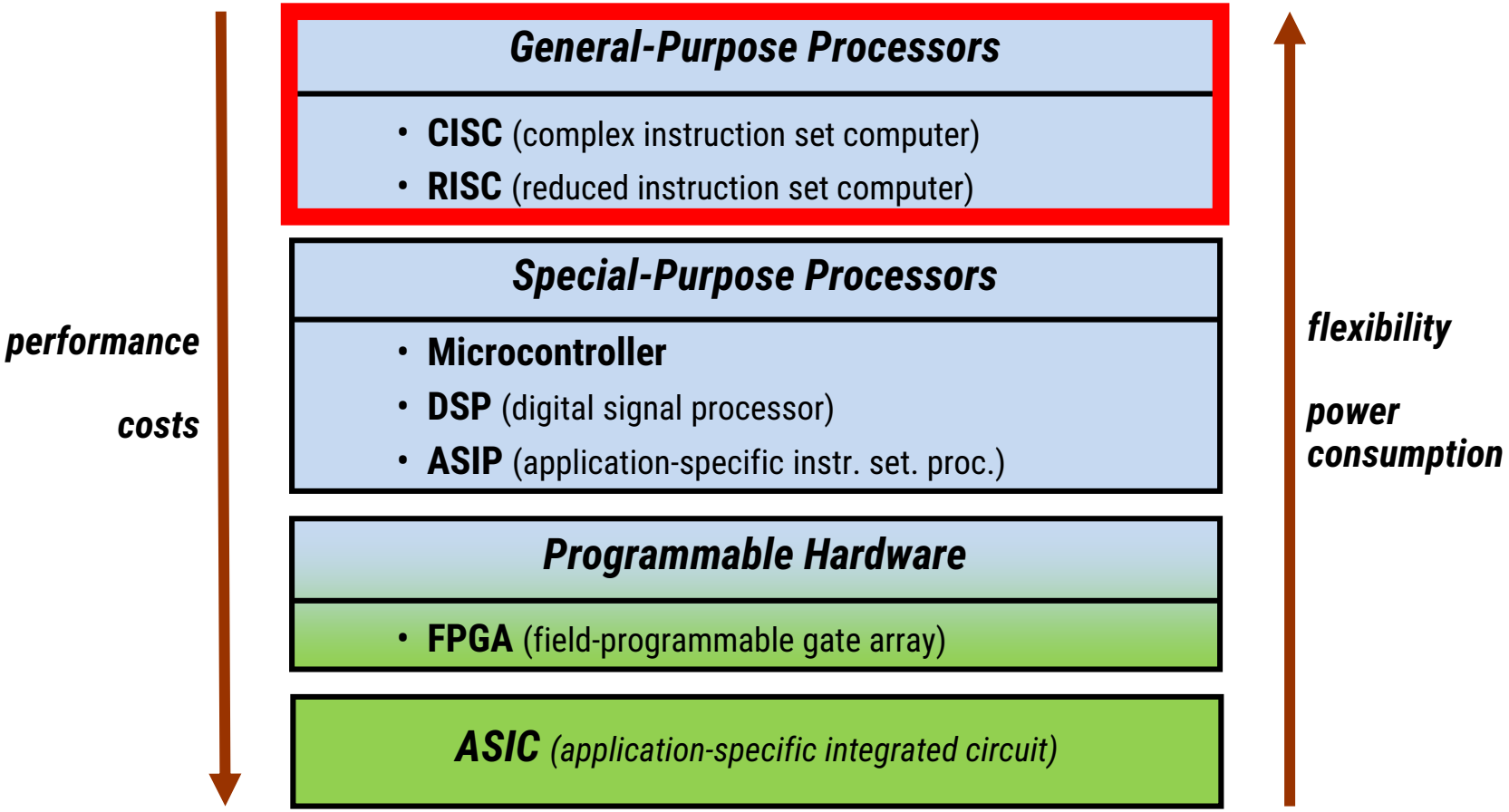
Implementation Alternatives



General-purpose Processors (GP)

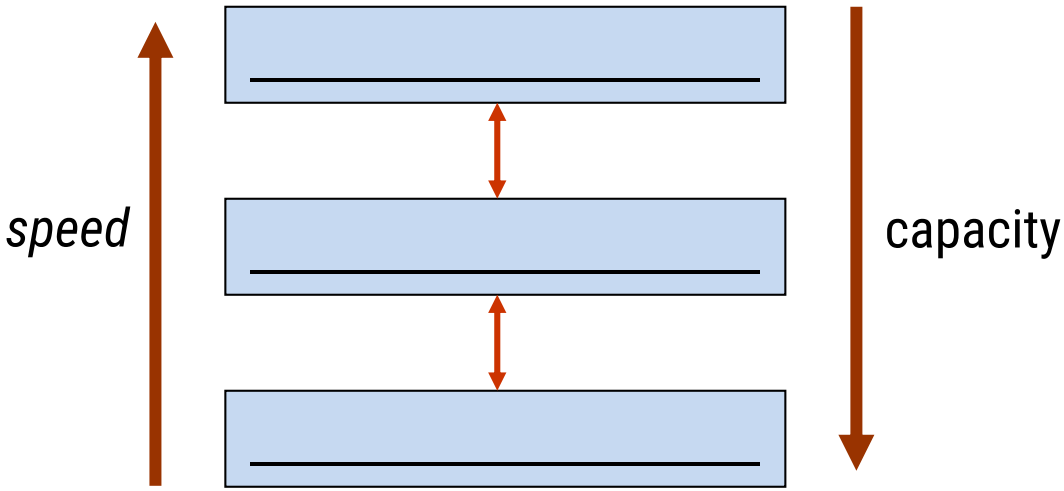
- types
  - complex instruction set processor
  - reduced instruction set processor
- properties
  - high performance for many applications
  - not optimised for a single application
  - high power consumption
- development
  - highly optimised circuit structures
  - design time >100 person years
  - profitable in large volumes only
- application areas
  - PCs, workstations, game consoles

Reasons for High Performance (I)

- exploitation of parallelism
  - several scalar units (_____)
    - e.g. integer units, floating point units, load/store units
    - parallelizable instructions are recognized by processor and mapped to units (dynamic scheduling)
    - complex control unit
  - deep instruction pipelines (_____)
    - e.g. fetch | decode | read | execute | write back
    - depth of pipeline depends on scalar unit
    - branch prediction

Reasons for High Performance (II)

- several layers of memory hierarchy



- leading technologies
  - gate count, clock rate, structure dimensions

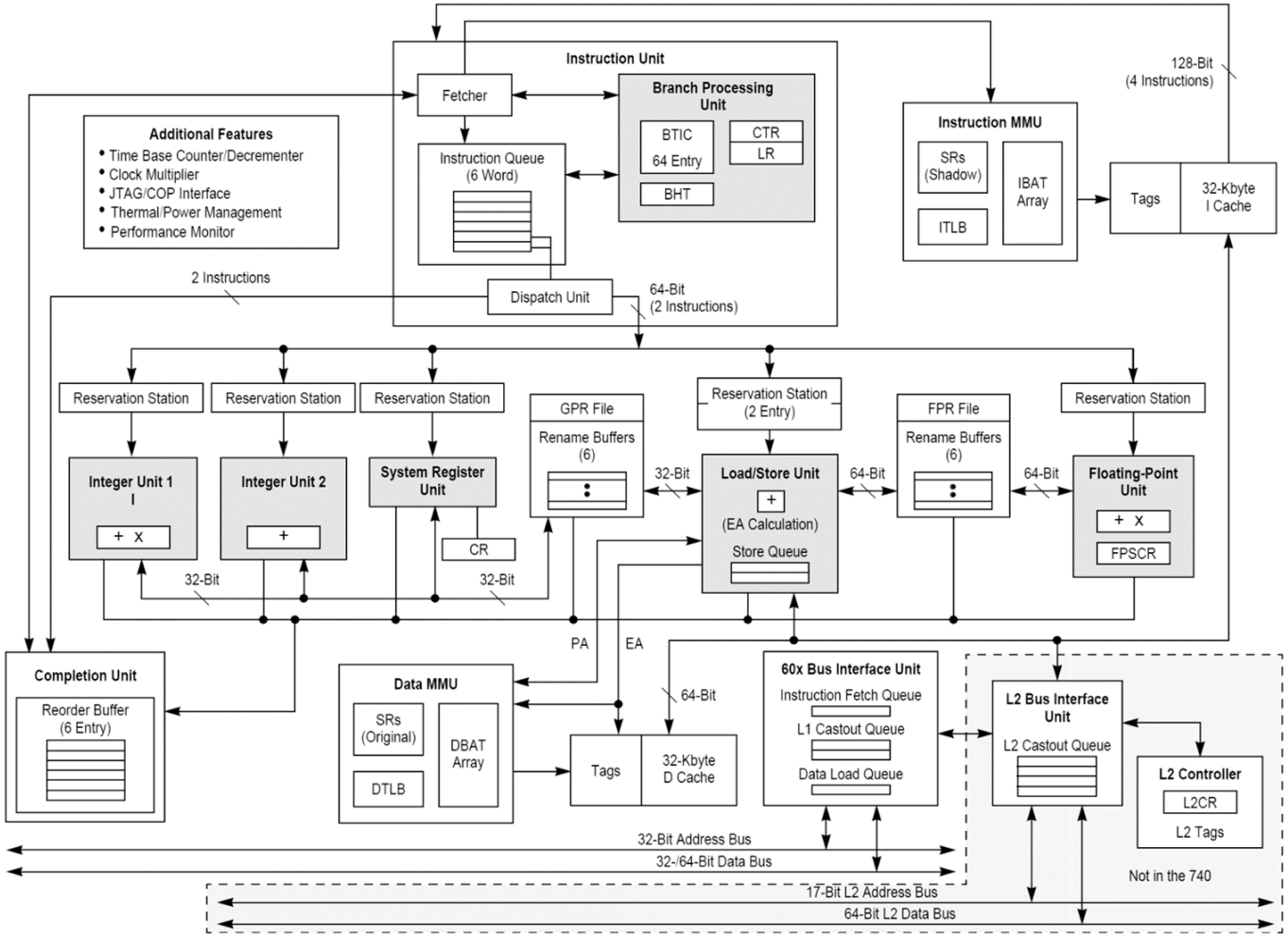
Parallelism

- bit level
  - wider data paths (8 bit → 16 bit → 32 bit → 64 bit)
- word level
  - multimedia instruction sets (MMX, SSE, …)
- _____level
  - pipelining
  - multiple issue (superscalar processors, very large instruction word (VLIW) processors)
- _____level
  - multithreaded processors
- thread/program level
  - multiprocessors, multi-core processors
  - multicomputer

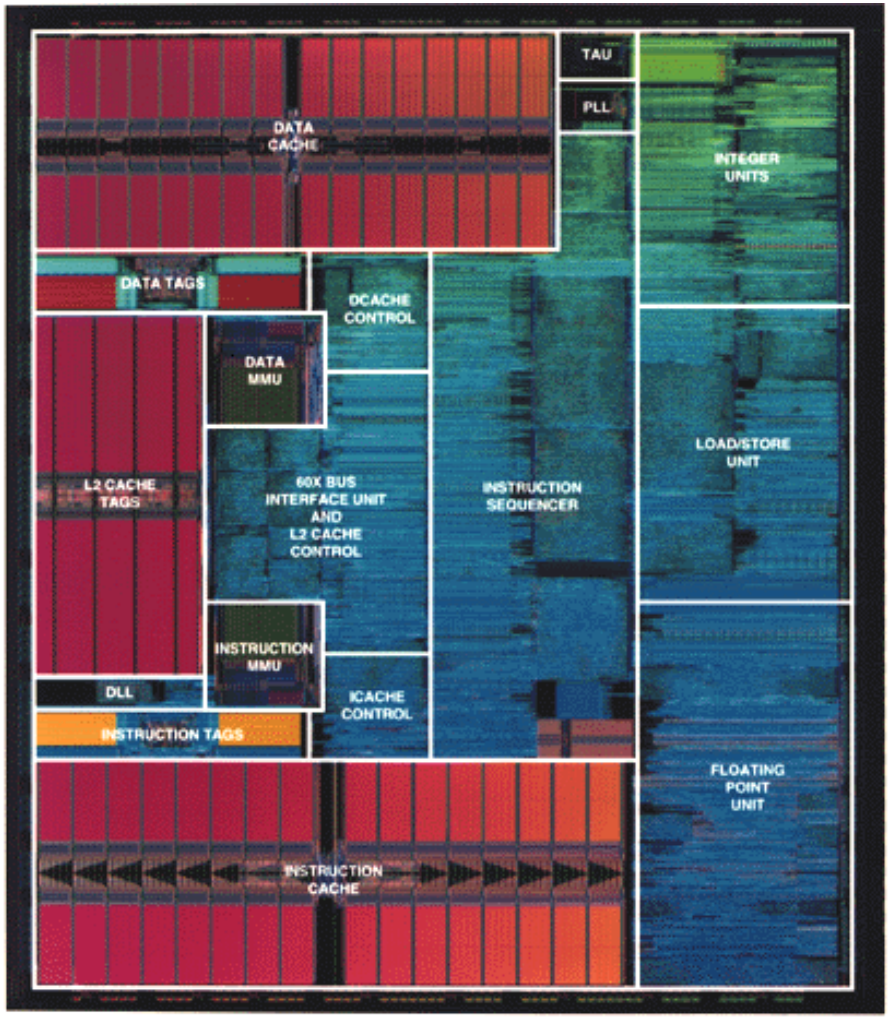
GP Processors Examples

processor	type	scalar units x pipeline depth	clock [MHz]	1st level cache instr./data	2nd level cache
21264 ALPHA (DIGITAL)	64 bit RISC	4 x 7	600	64 KB / 64 KB	extern
R10000 (MIPS)	64 bit RISC	4 x 10	250	32 KB / 32 KB	512 KB-16 MB extern
PowerPC750 (IBM/Motorola)	32 bit RISC	3 x 6	466	32 KB / 32 KB	256 KB – 1 MB extern
UltraSparc III (SUN)	64 bit RISC	4 x 9	400	16 KB / 16 KB	512 KB – 16 MB extern
Pentium III (Intel)	32 bit CISC	3 x 12	500	16 KB / 16 KB	512 KB extern
K6-III (AMD)	32 bit CISC	6 x 7	450	32 KB / 32 KB	256 KB intern

IBM PowerPC 750 - Structure



IBM PowerPC 750 - Layout



Real Time

- execution times difficult to predict due to
  - dynamic scheduling
  - caching
  - branch prediction
  - interrupts

  → GP processors **not** suitable for _____

- complex I/O and memory interfaces

Multimedia Extensions

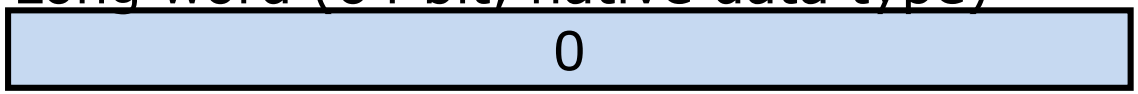
- multimedia applications
  - e.g. audio/video playback, video conferencing, …
  - 8/16 bit data types (e.g. pixel)
  - many arithmetic operations (e. g. multiplication, addition)
  - huge data sets, huge I/O bandwidth
  - large data parallelism

- _____ model
  - 32/64 bit registers and ALUs split into smaller units
  - instructions work in parallel on these units

- examples
  - MMX (Intel), VIS (UltraSparc), MDMX (MIPS), MAX-2 (HP)

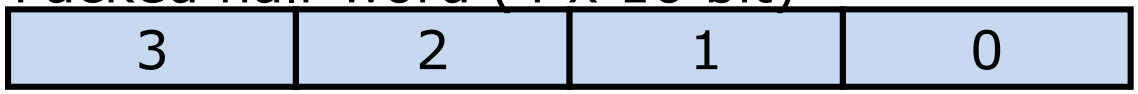
Sub-words

Long word (64 bit, native data type)

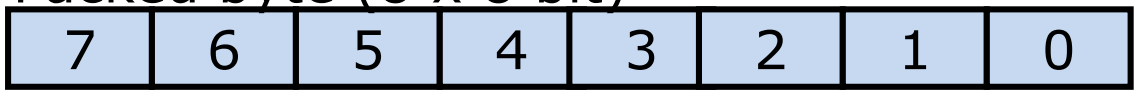


Packed word (2 x 32 bit)

Packed half-word (4 x 16 bit)

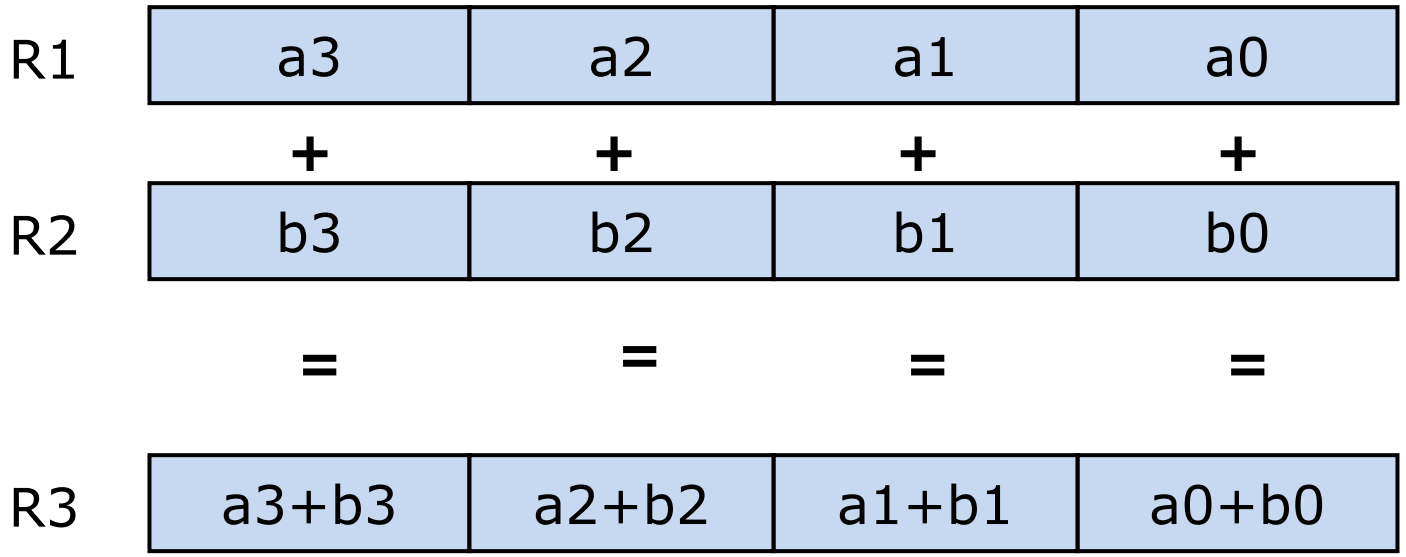


Packed byte (8 x 8 bit)

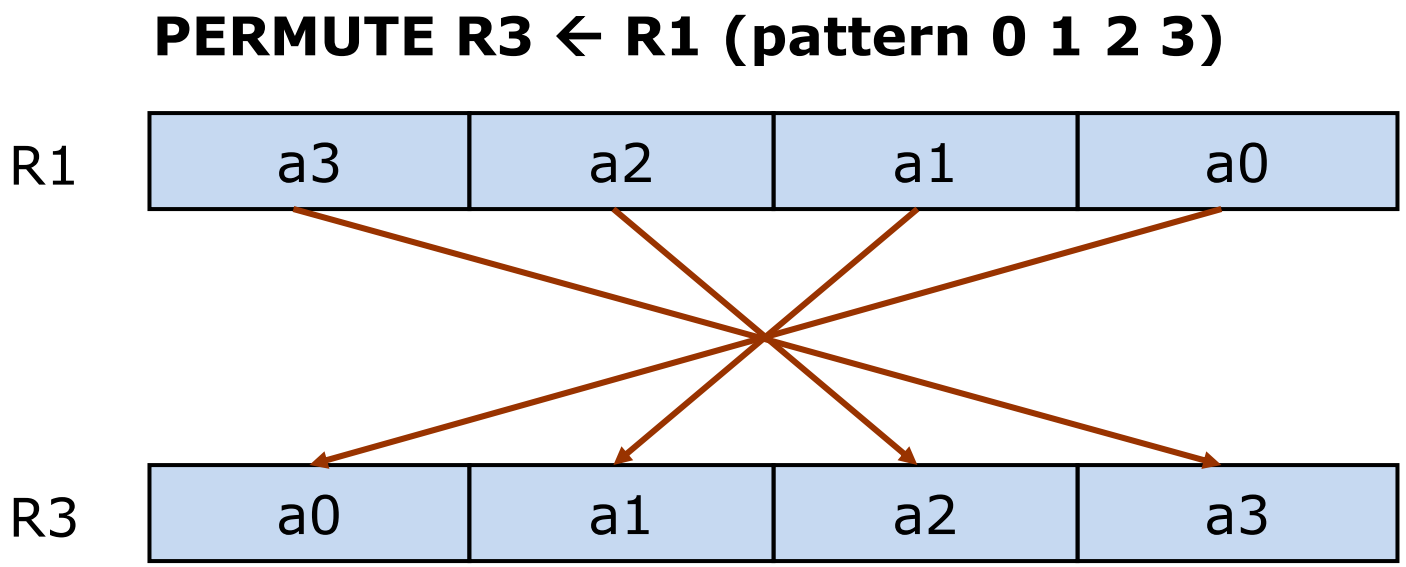


Sub-word Instructions (I)

ADD R3 ← R1, R2



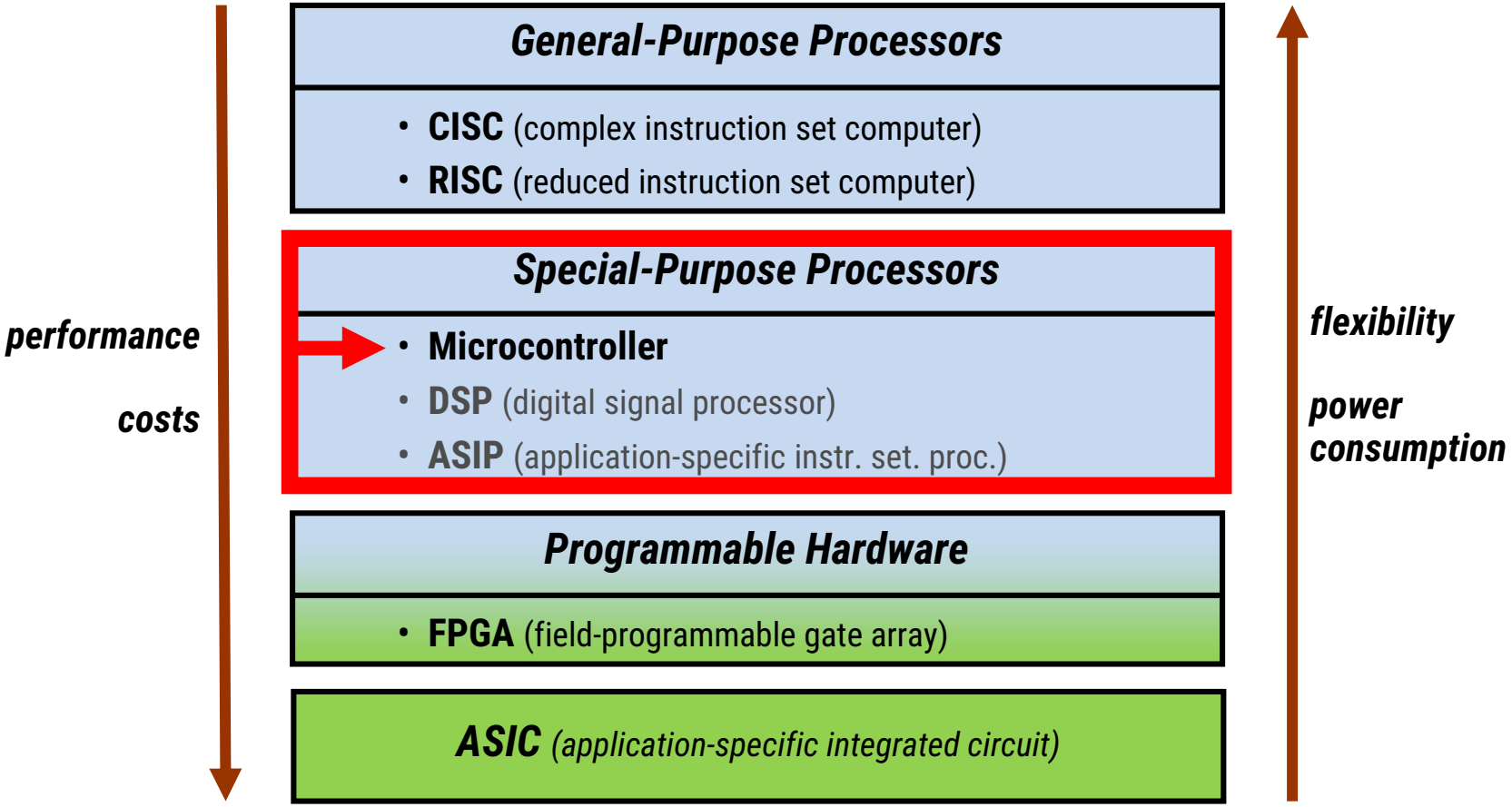
Sub-word Instructions (II)



Multimedia Instruction Sets

- sub-word model sufficient?
  - trade-off between utilisation of _____ and available _____
- SW development
  - manual customised assembler routines
  - programming languages necessary
    - data types with defined data width
    - different overflow semantics
  - compiler necessary
    - automatic detection of sub-word parallelism

Implementation Alternatives



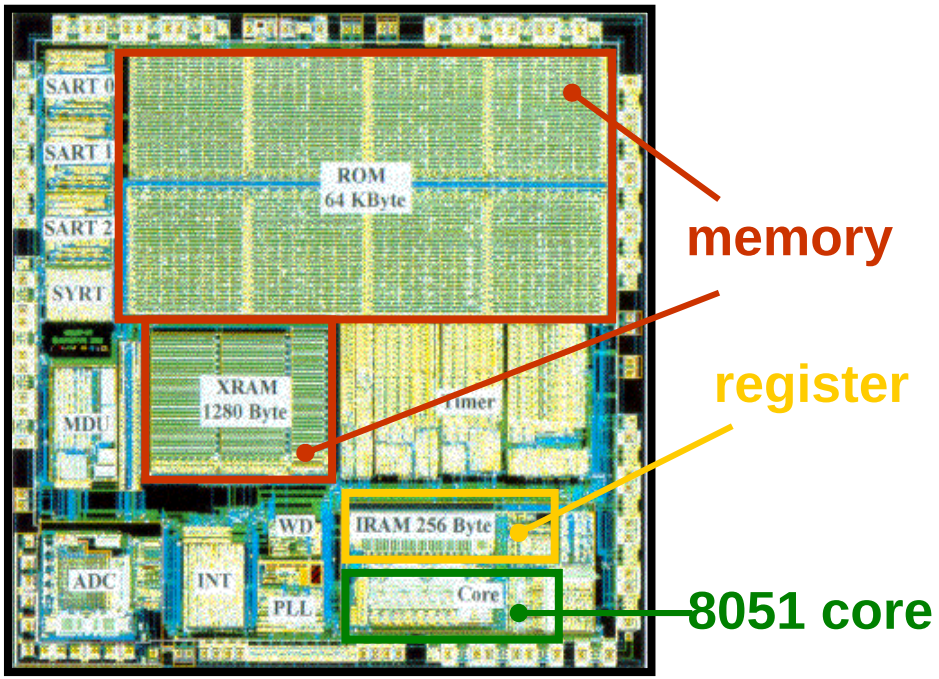
Microcontroller (MC)

- _____ applications
  - many control commands (branches, jumps)
  - few arithmetic operations
  - low data throughput
  - multitasking

- microcontrollers are optimised
  - many bit- and logic operations
  - registers often implemented in RAM → context switch by pointer operation
    - minimal interrupt latency
    - very fast context switches
  - peripheral units integrated (A/D, DA, CAN, timer, …)

Low Cost MC

- systems with 4 or 8 bit processors
  - code size dominates chip area and thus costs
  - low performance requirements
- e.g. SIECO51
  (Siemens Automotive)

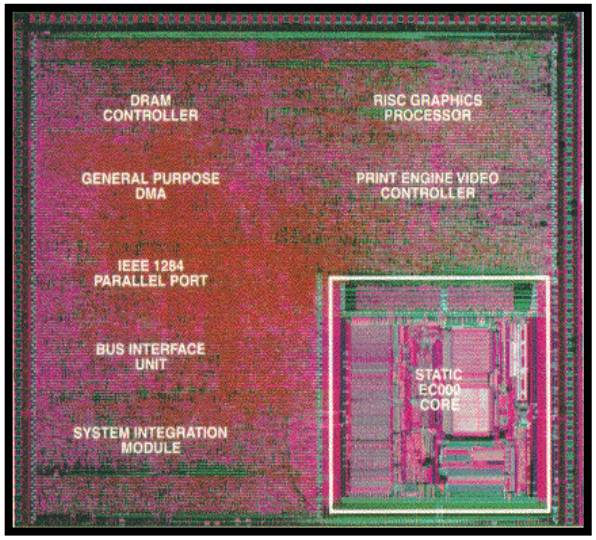


High Performance MC

- systems with 16/32/64 bit processors
  - e.g. Motorola MC683xx, Intel x196, …
- application domains
  - control-dominant parts and additionally
    - high data rates (telecommunication, automotive)
    - high computational requirements (control systems, signal processing)
  - microcontroller core as block of a _____

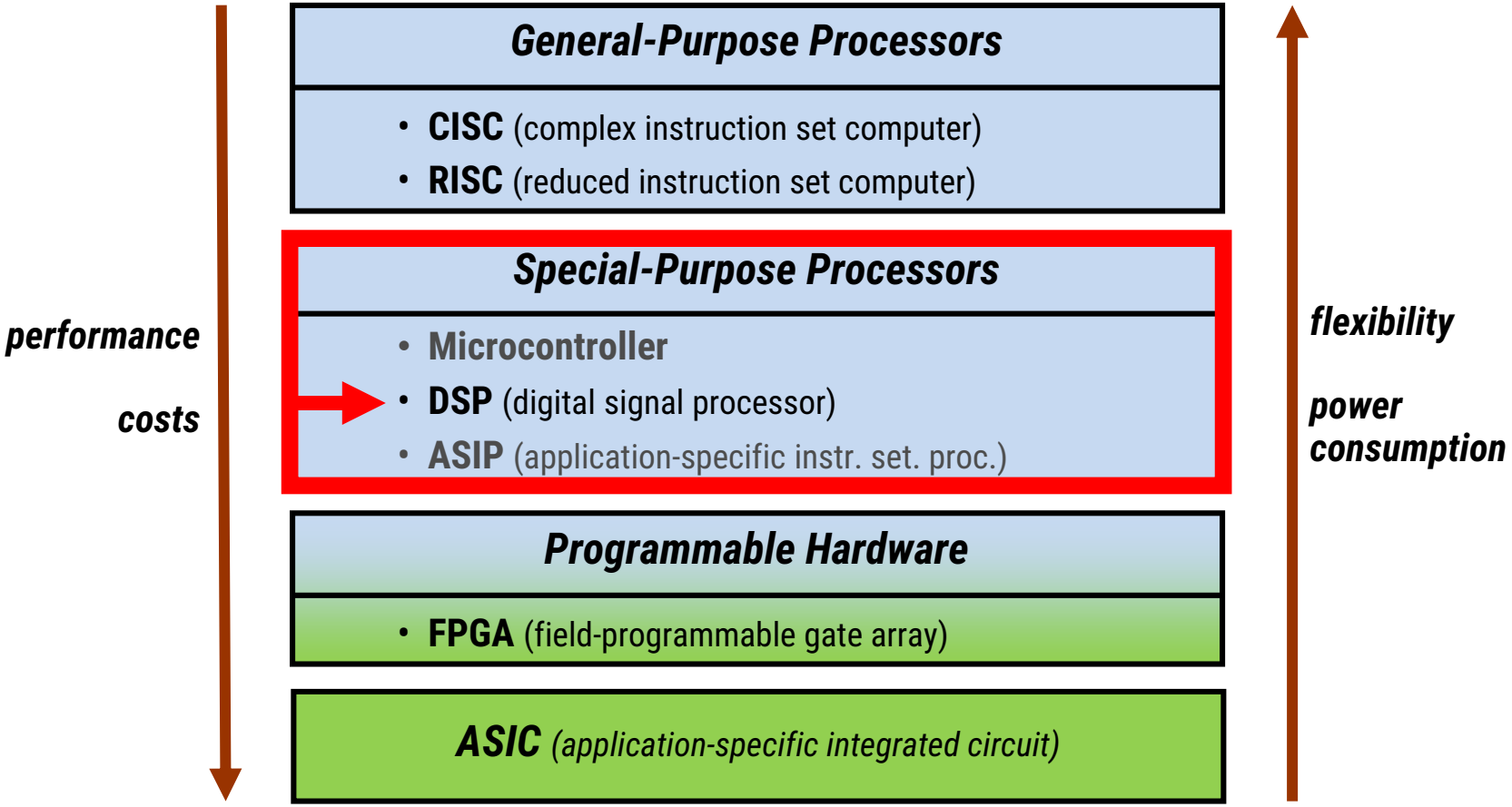
Device Families

- e.g. Motorola MC683xx family
  - core processors: 16/32/64 bit
  - memory: ROM, RAM, EPROM,…
  - peripherals: TPU, SIO, DMA, …
  - co-processors: fuzzy control, graphics, …
  - user defined blocks
  - bus system, interrupt system



MC68322
graphic processor

Implementation Alternatives

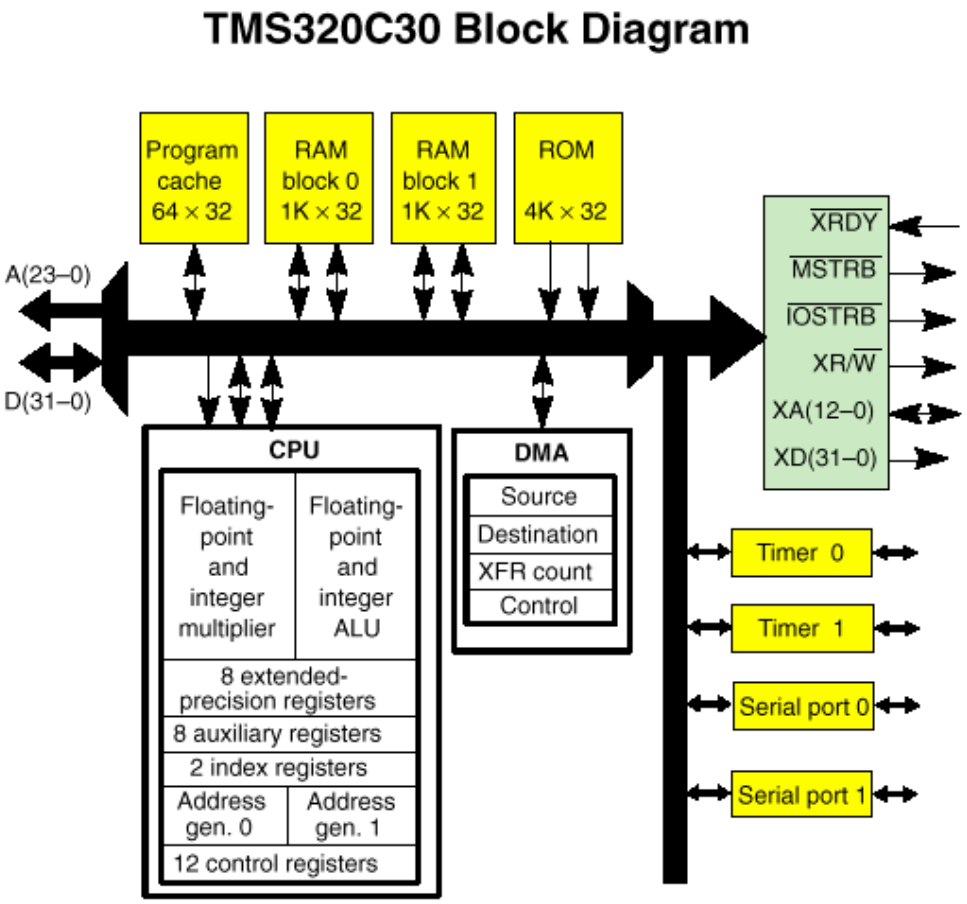


Digital Signal Processors (DSP)

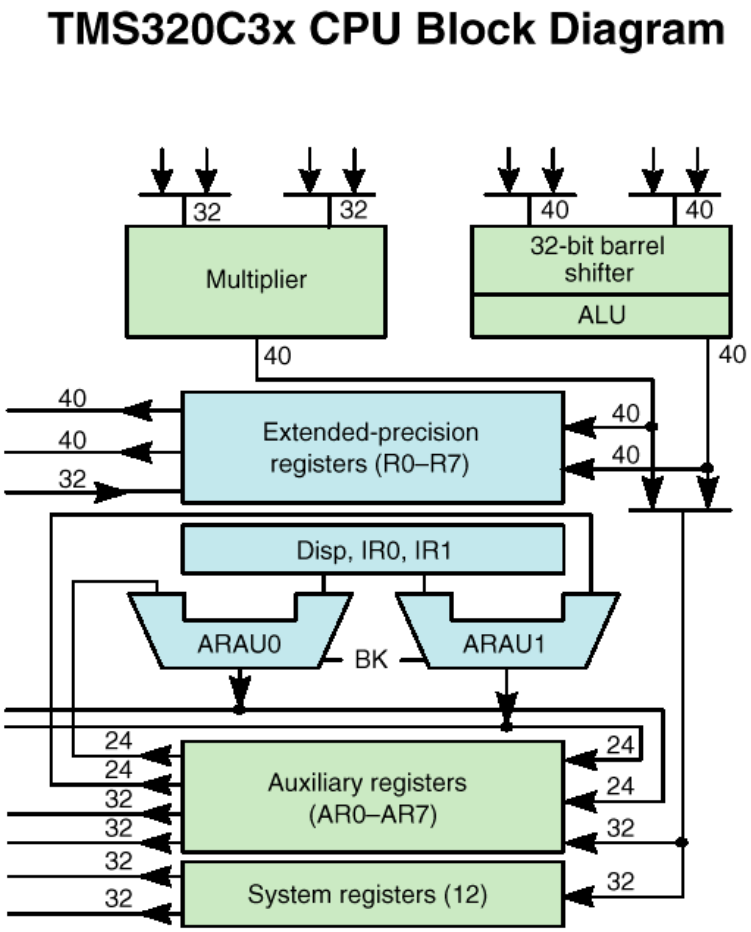
- signal processing applications
  - _____ code
  - many arithmetic operations, few branches and jumps
  - lots of parallelism
  - high data throughput

- DSP are optimised
  - parallel instructions (MAC – multiply & accumulate)
  - Harvard architecture (→ simultaneous access to instructions and data), multiple accesses to operands
  - zero overhead loops
  - special addressing modes (circular, bit reverse)

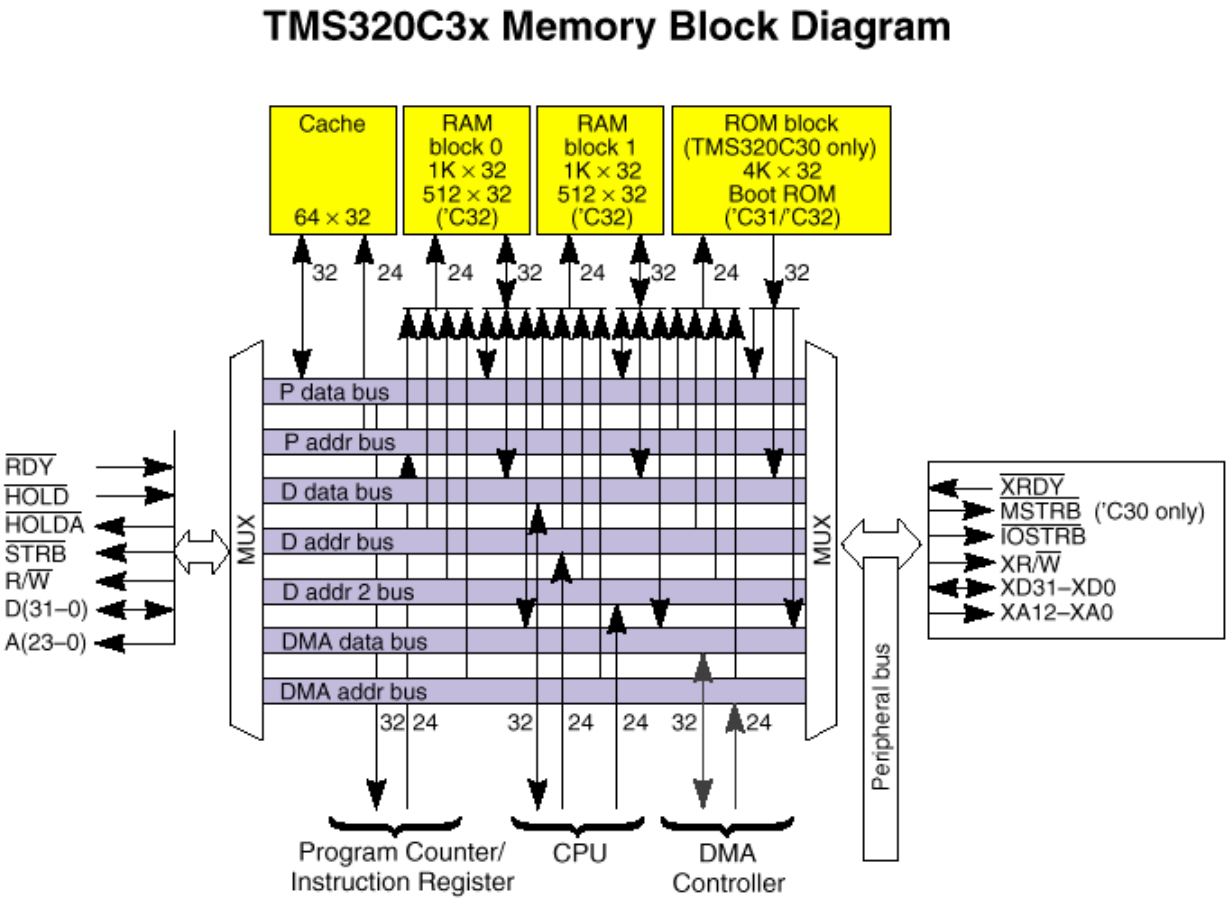
TMS320C3x


TMS320C30 Block Diagram
Program cache 64 × 32
RAM block 0 1K × 32
RAM block 1 1K × 32
ROM 4K × 32
A(23–0)
D(31–0)
XRDY
MSTRB
IOSTRB
XR/W
XA(12–0)
XD(31–0)
CPU
Floating-point and integer multiplier
Floating-point and integer ALU
8 extended-precision registers
8 auxiliary registers
2 index registers
Address gen. 0
Address gen. 1
12 control registers
DMA
Source
Destination
XFR count
Control
Timer 0
Timer 1
Serial port 0
Serial port 1

TMS320C3x - CPU



TMS320C3x - Memory



MAC – Multiply & Accumulate

```
sum = 0.0;
for (i=0; i<N; i++)
  sum = sum + a[i]*b[i];
```

(repeat next instruction N-1 times)

MAC - instruction

```
    LDF     0, R0
    LDF     0, R1
    RPTS    N-1
    MPYF3   *(AR0)++, *(AR1)++, R0
||  ADDF3   R0, R1, R1
    ADDF3   R0, R1, R1
```

Arithmetic

- number formats
  - mantissa determines accuracy
  - exponent determines dynamics
- _____ point
  - smaller, cheaper and faster than floating point (same mantissa width)
  - application design more difficult due to rounding and scaling problems
  - sufficient for many DSP applications
- _____ point
  - high dynamics (large range of numbers)
  - simplified application design

Program Development

- assembler, compiler
  - many DSP features not supported by compiler → can only be used in assembler
  - programming in C → profiling → time-critical parts in assembler
- libraries
  - programming in C, link with hand-optimised libraries
  - e.g. libraries for image processing, speech processing
- code generators
  - design environments for modelling, simulation and code generation
  - e.g. Synopsys COSSAP, MATLAB

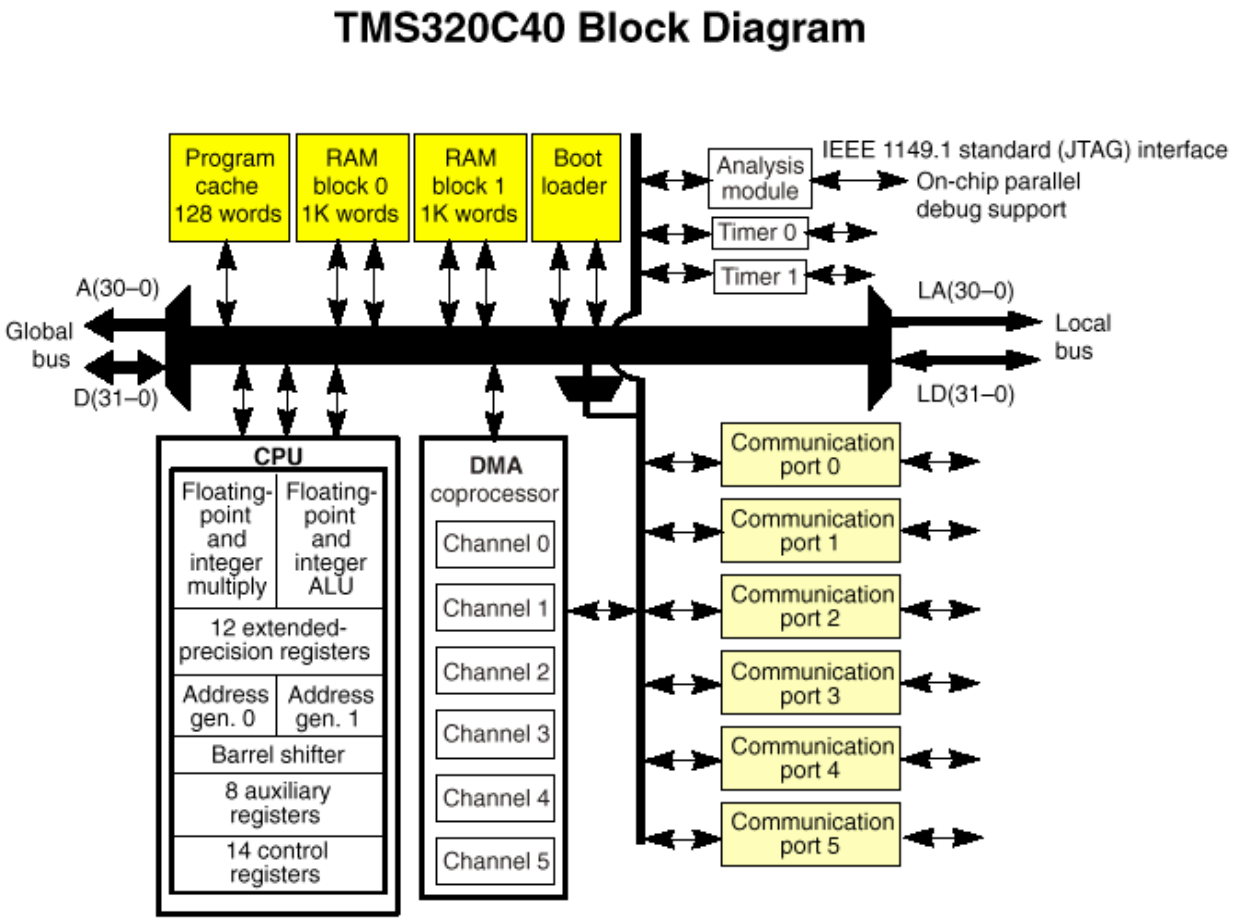
Trends

- multi-DSP systems
  - for high-performance applications
  - processors have (simple) interfaces to connect to other processors (e.g. TMS320C4x, ADSP21060 "SHARC")
  - multiple processors on one chip (e.g. TSM320C80)

- VLIW DSPs
  - several functional units
  - compiler recognises parallelism and schedules the instructions to the functional units
  - e.g. TMS320C6x (8 functional units)

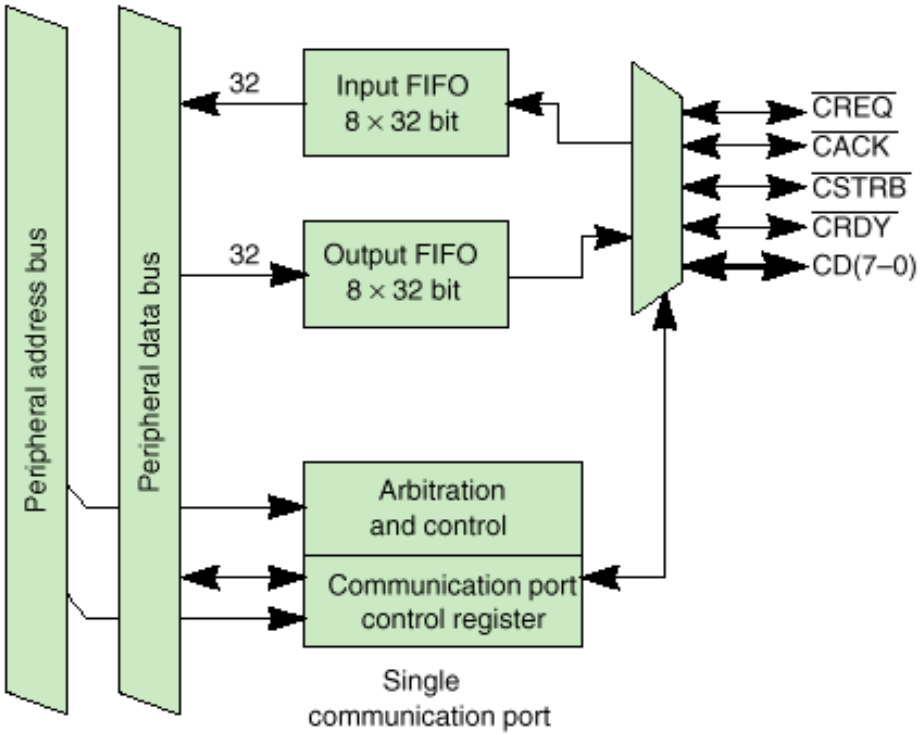
- _____
  - DSP applications on GP processors

TMS320C4x (I)


TMS320C40 Block Diagram
Program cache 128 words
RAM block 0 1K words
RAM block 1 1K words
Boot loader
Analysis module
IEEE 1149.1 standard (JTAG) interface
On-chip parallel debug support
Timer 0
Timer 1
A(30–0)
Global bus
D(31–0)
LA(30–0)
Local bus
LD(31–0)
CPU
Floating-point and integer multiply
Floating-point and integer ALU
12 extended-precision registers
Address gen. 0
Address gen. 1
Barrel shifter
8 auxiliary registers
14 control registers
DMA coprocessor
Channel 0
Channel 1
Channel 2
Channel 3
Channel 4
Channel 5
Communication port 0
Communication port 1
Communication port 2
Communication port 3
Communication port 4
Communication port 5

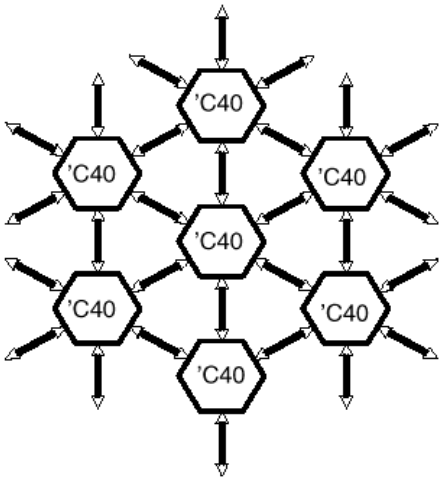
TMS320C4x (II)

TMS320C4x Communication Ports Block Diagram



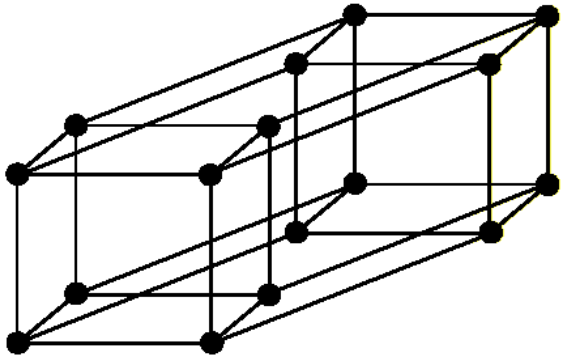
TMS320C4x (III)

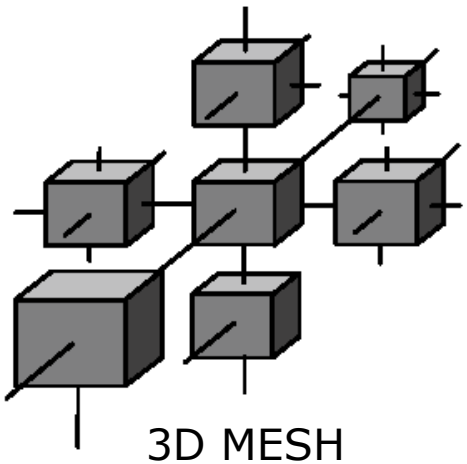
- different topologies for processor interconnection



hexagonal grid

4D hypercube

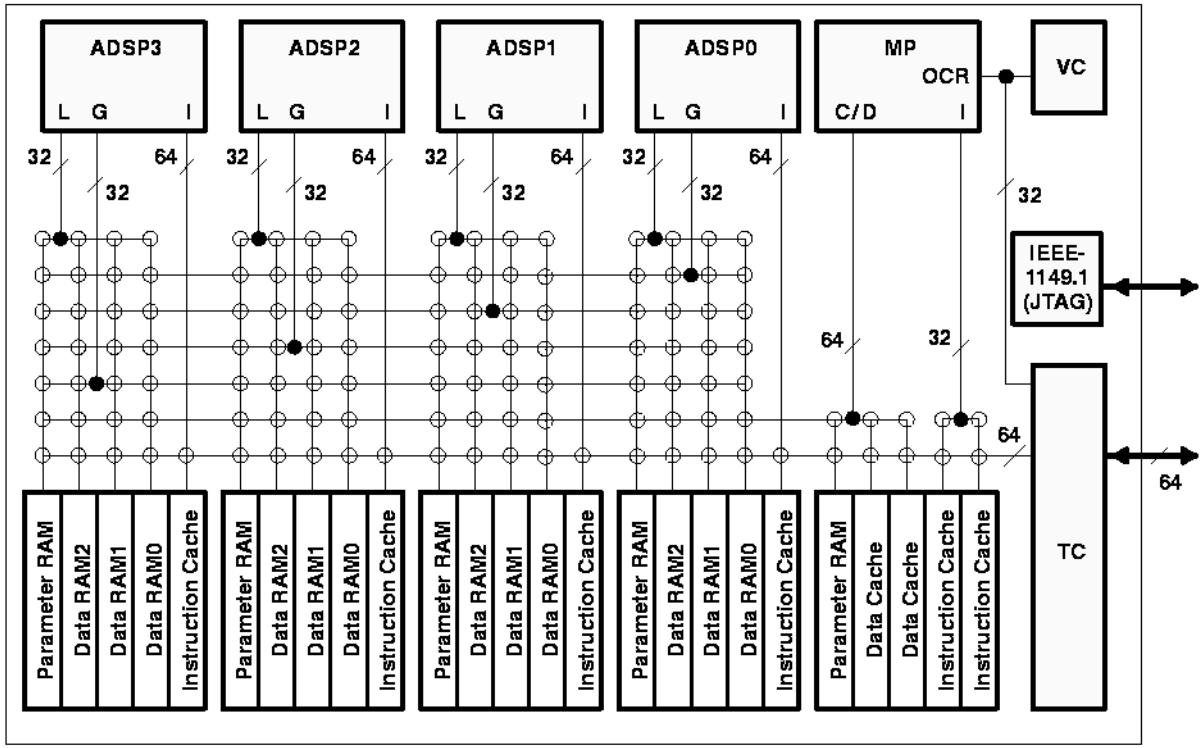




3D MESH

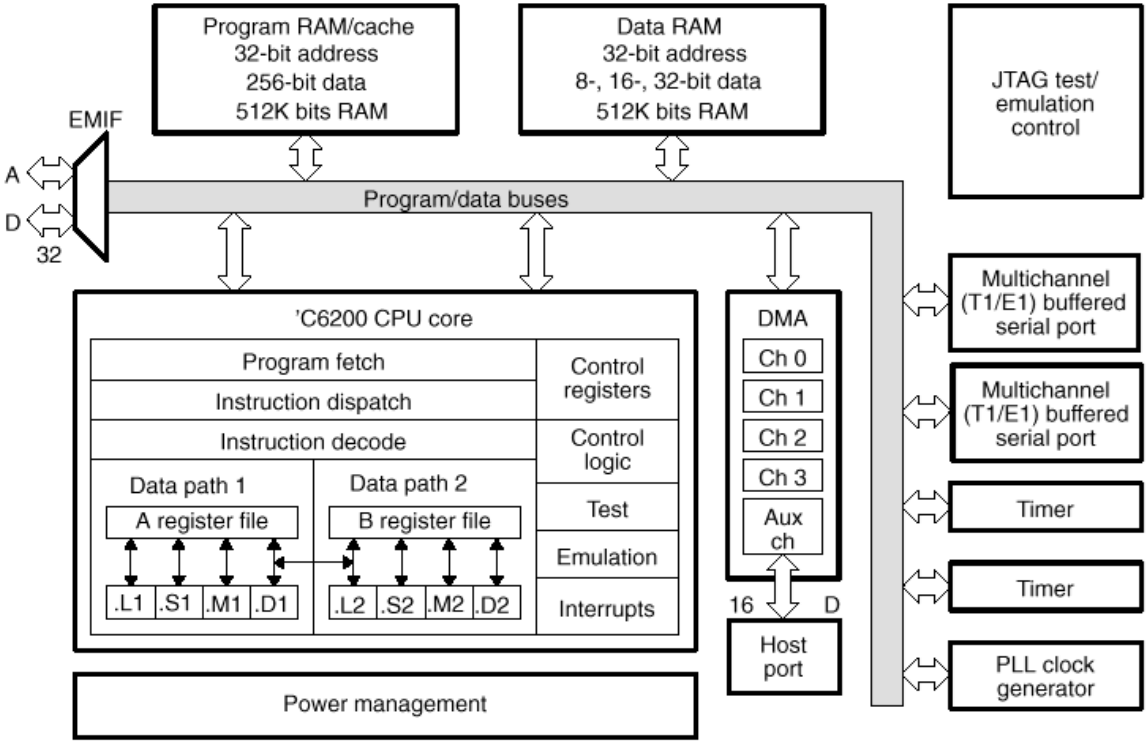
TMS320C80

- multiple processor - specialised for video/audio applications



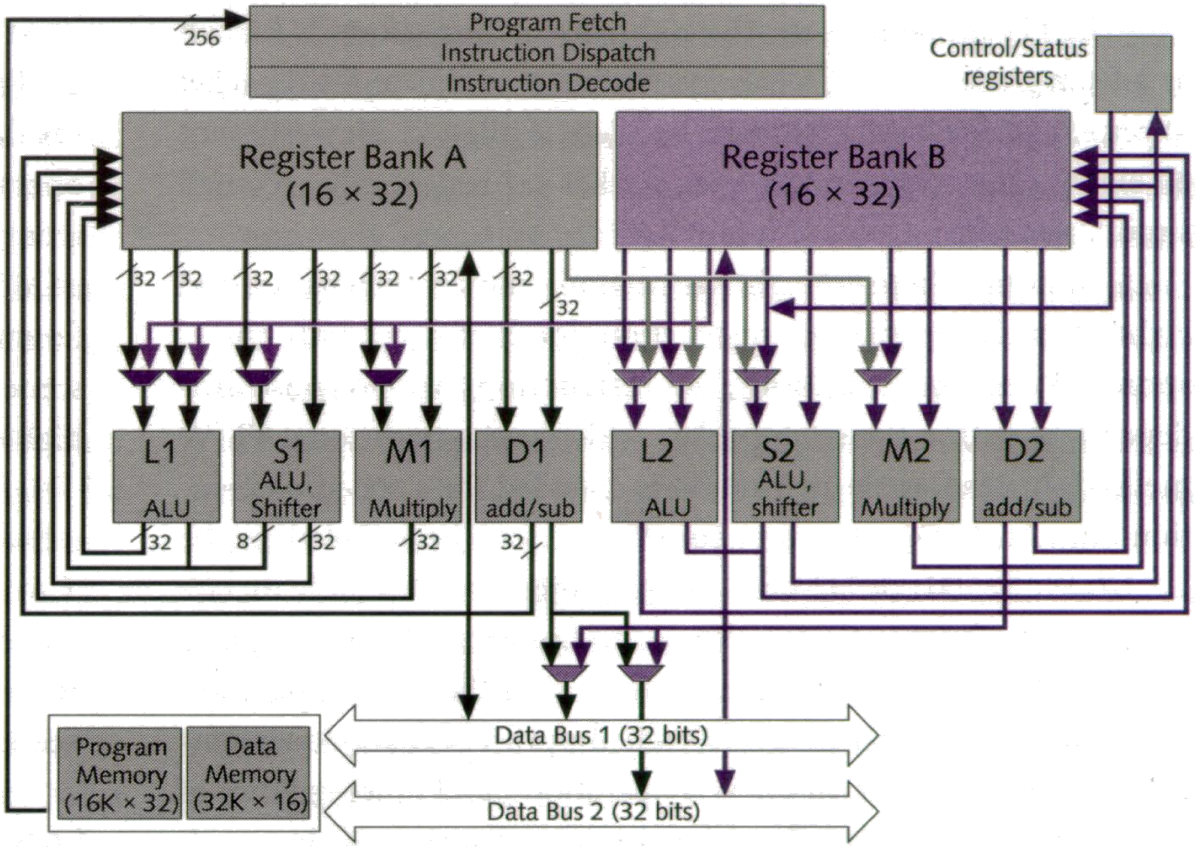
TMS320C6x (I)

- very large instruction set DSP
- CPU core with peripherals:



TMS320C6x (II)

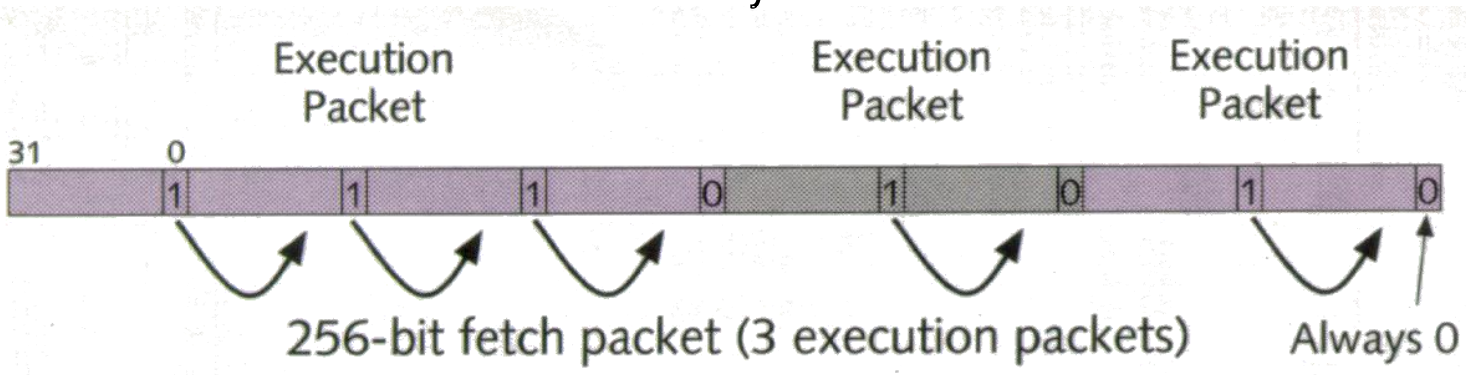
- core architecture:



VLIW Architectures

- problems
  - useful only for applications with enough parallelism
  - _____
  - development of efficient compilers difficult

- TMS320C6x
  - method to increase code density

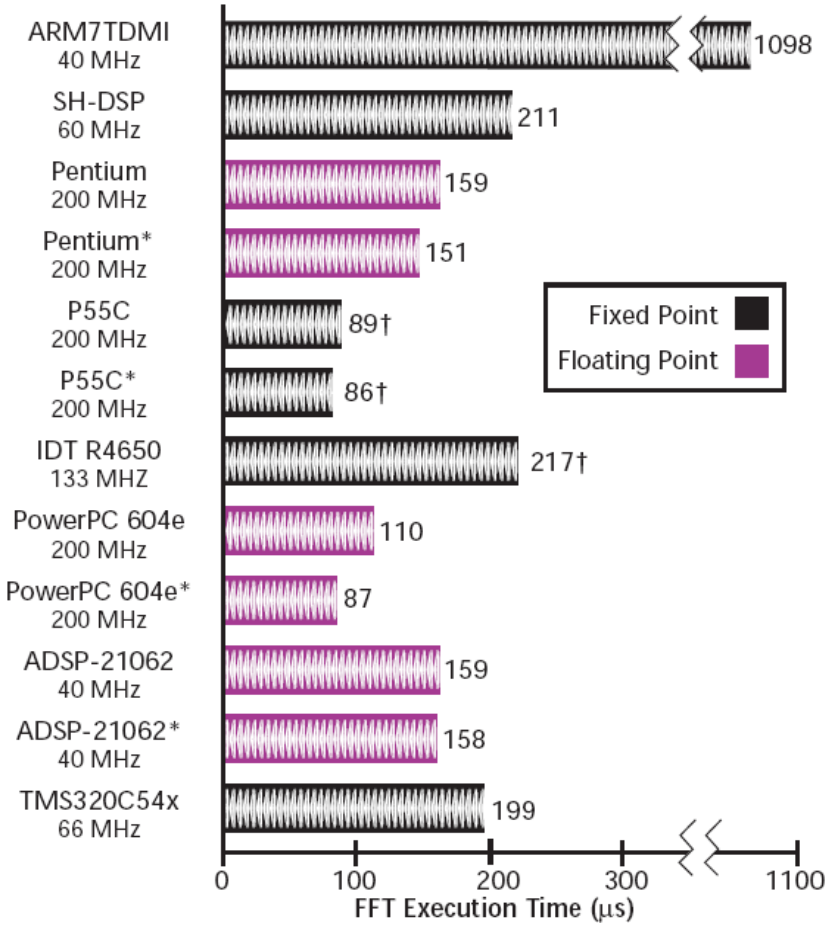


Desktop DSPs

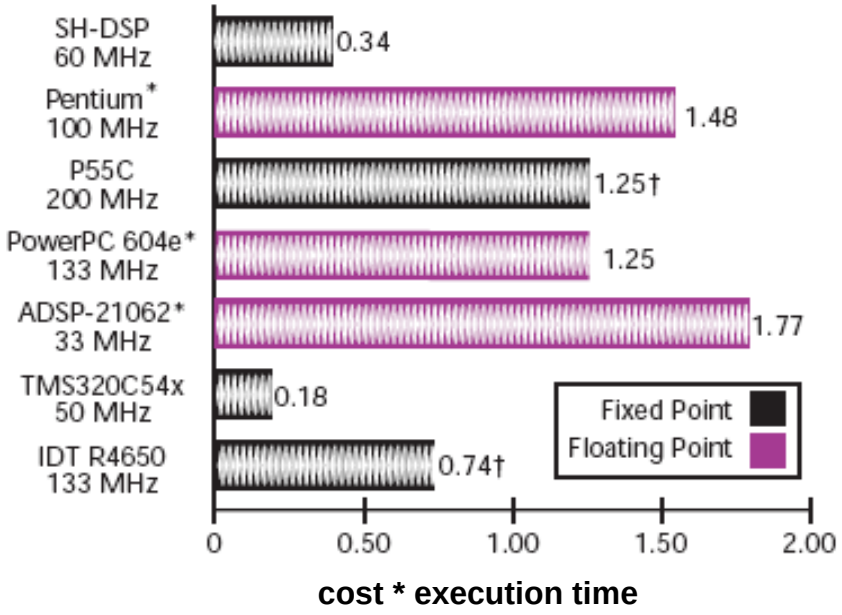
- GP processors for DSP applications
  - high clock rates
  - integer multiplication in one cycle
  - address generation, loop control can be done parallel using several scalar units
- drawbacks
  - not well-suited for hard real time
  - _____
- desktop DSP
  - no hard real time requirements
  - GP processors already allocated

BDT Benchmarks[1] (I)

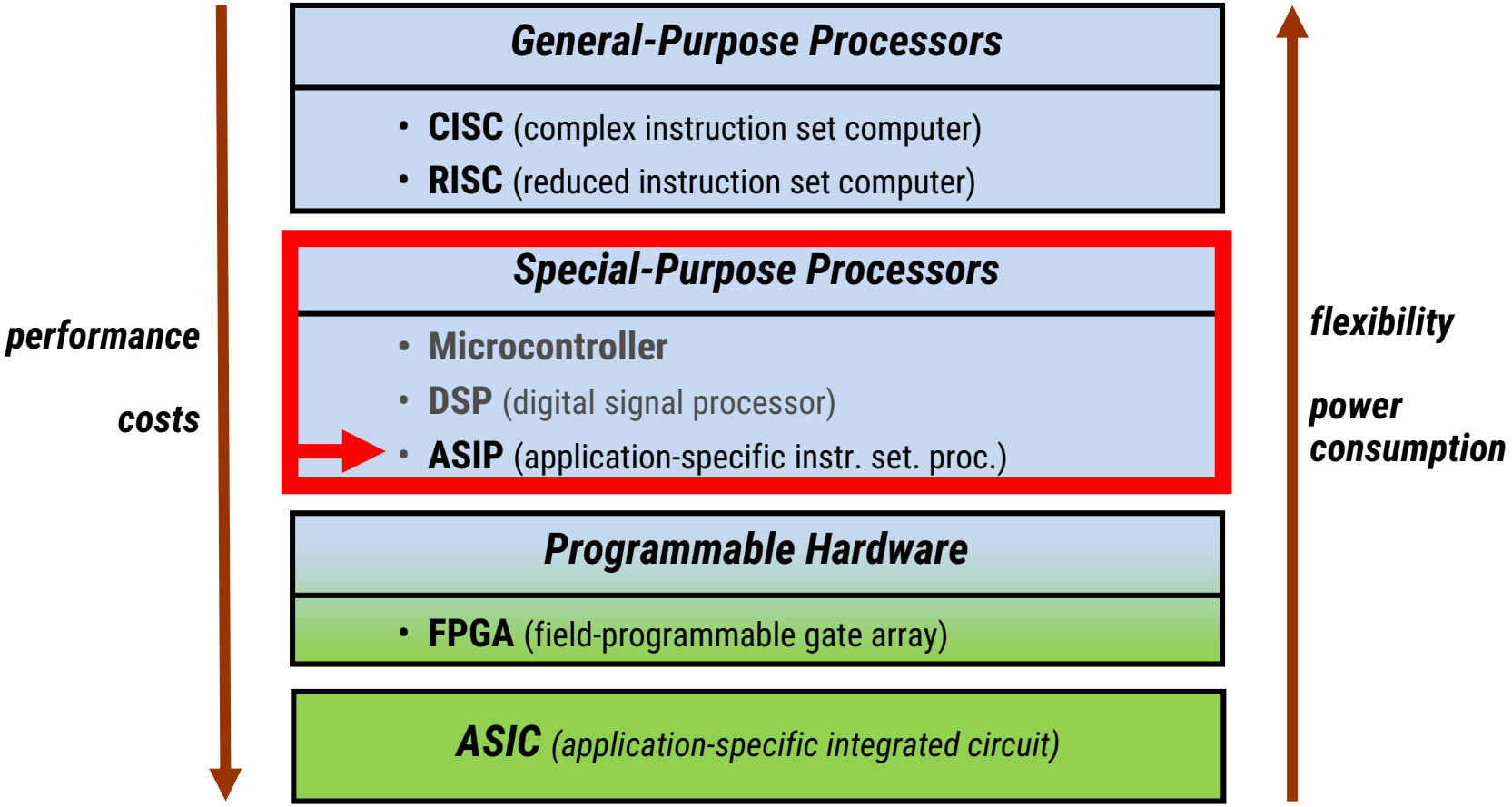
[1] *Berkeley Design Technology's DSP processor benchmarking*



Processor	Application	Fixed Point	Floating Point
PowerPC 604e	Desktop PCs	Excellent	Excellent
Pentium	Desktop PCs	Poor	Excellent
P55C	Desktop PCs	Excellent	Excellent
ARM7 TDMI	Embedded	Poor	n/a
SH-DSP	Embedded	Excellent	n/a
R4650	Embedded	Good	Poor



Implementation Alternatives

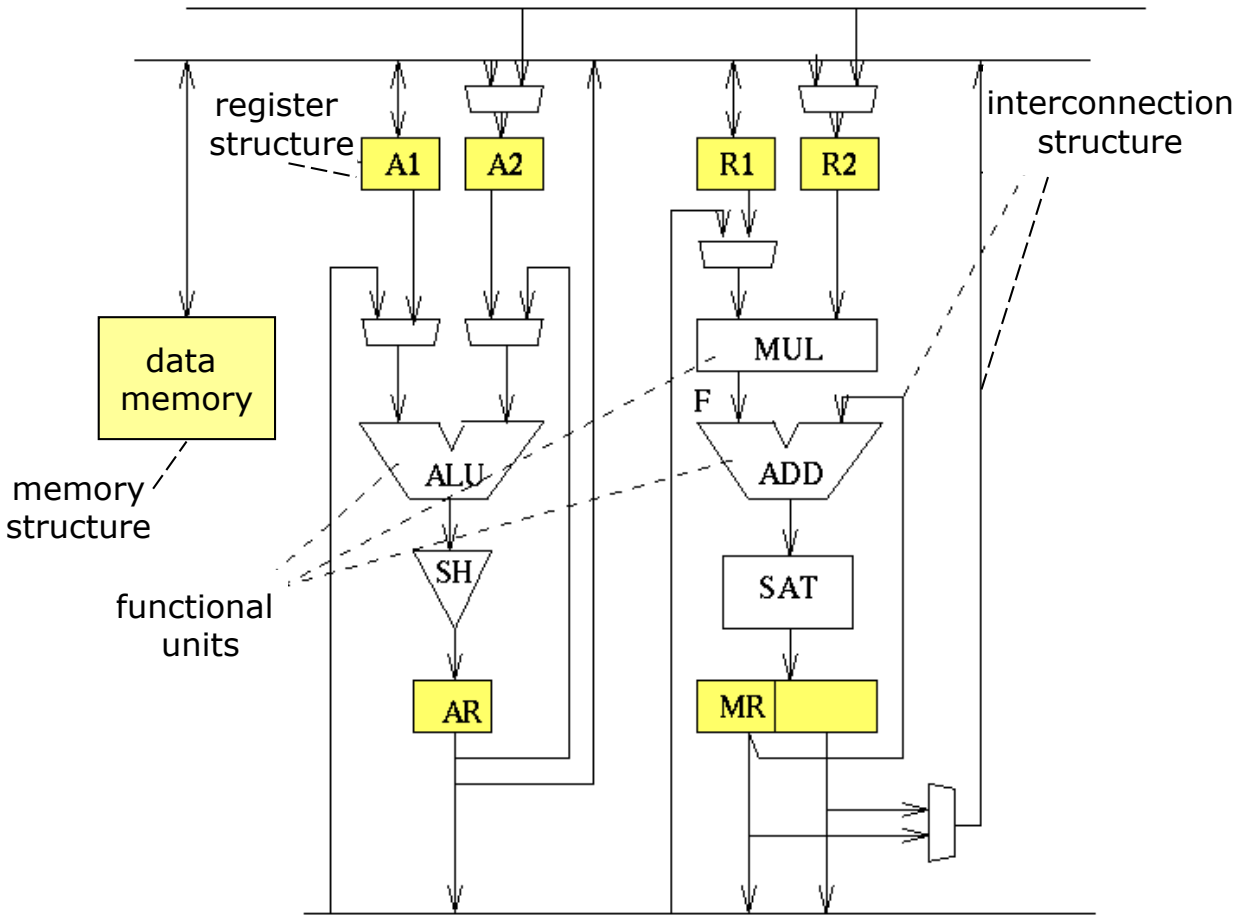


Application-specific Instruction Set Processors (ASIP)

- further specialisation of
  - instruction set (e.g. operator chaining)
  - functional units (e.g. pixel operations, special mathematical func.)
  - memory architecture (e.g. multiple memory blocks with parallel access)

- advantages over other processors
  - higher performance
  - lower costs at huge volumes (smaller chip areas, fewer pins)
  - smaller code size
  - lower power consumption

Example: ASIP Data Path



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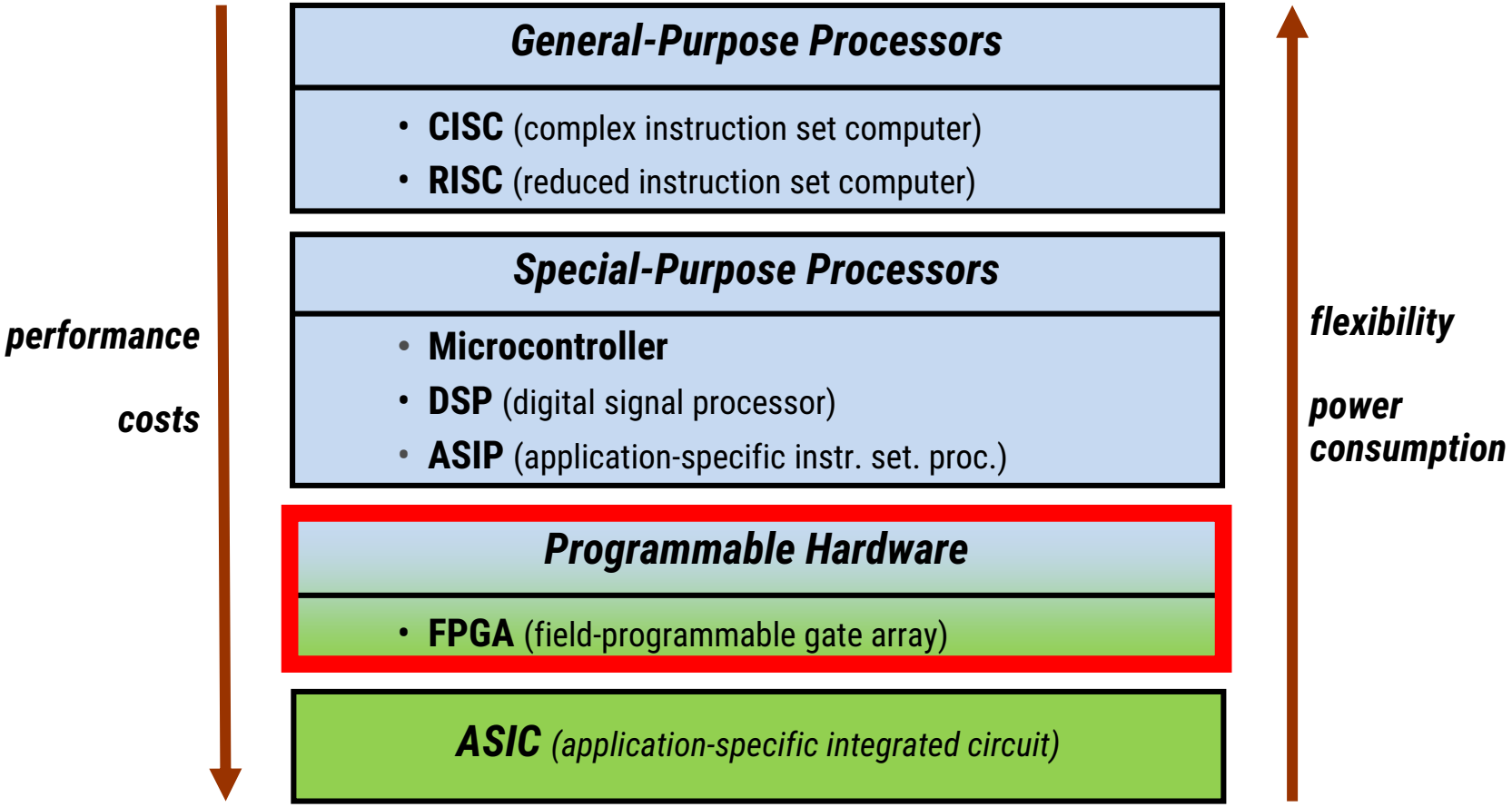
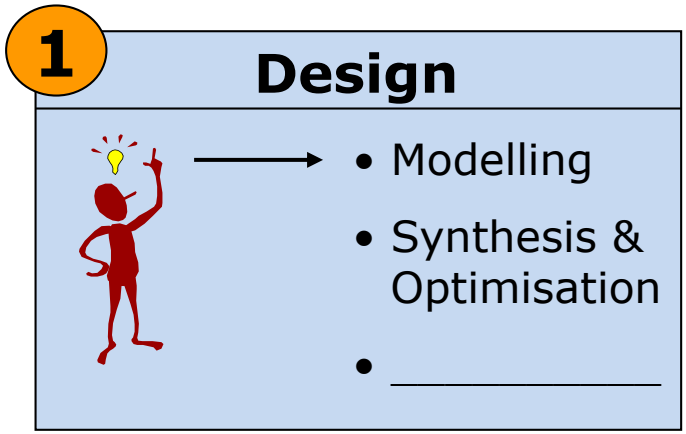
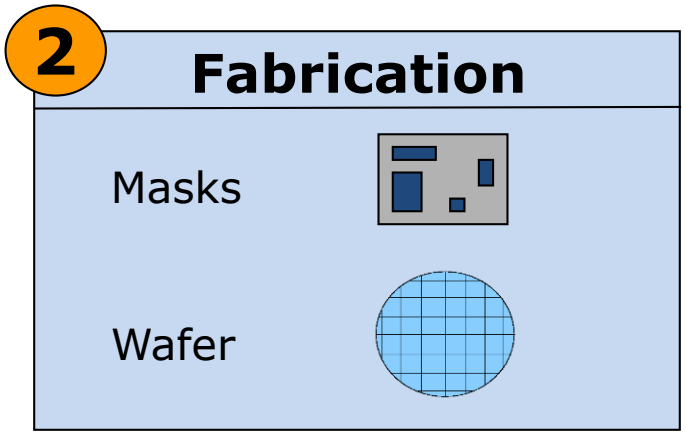
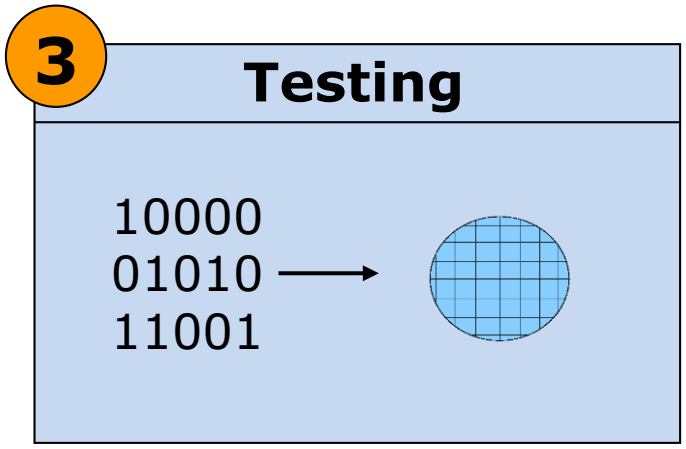
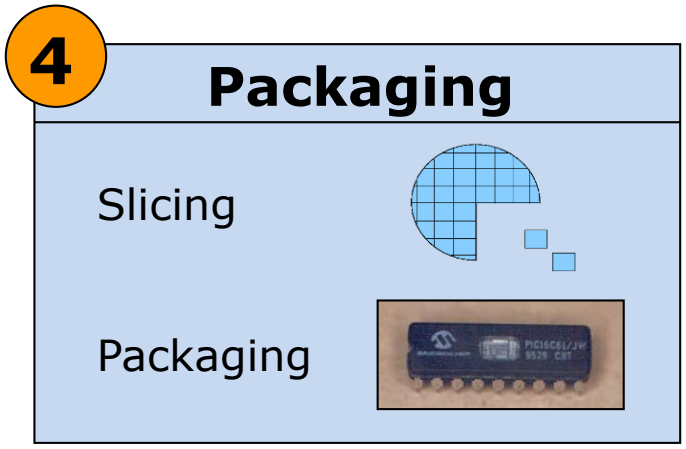


Integrated Circuit - Phases

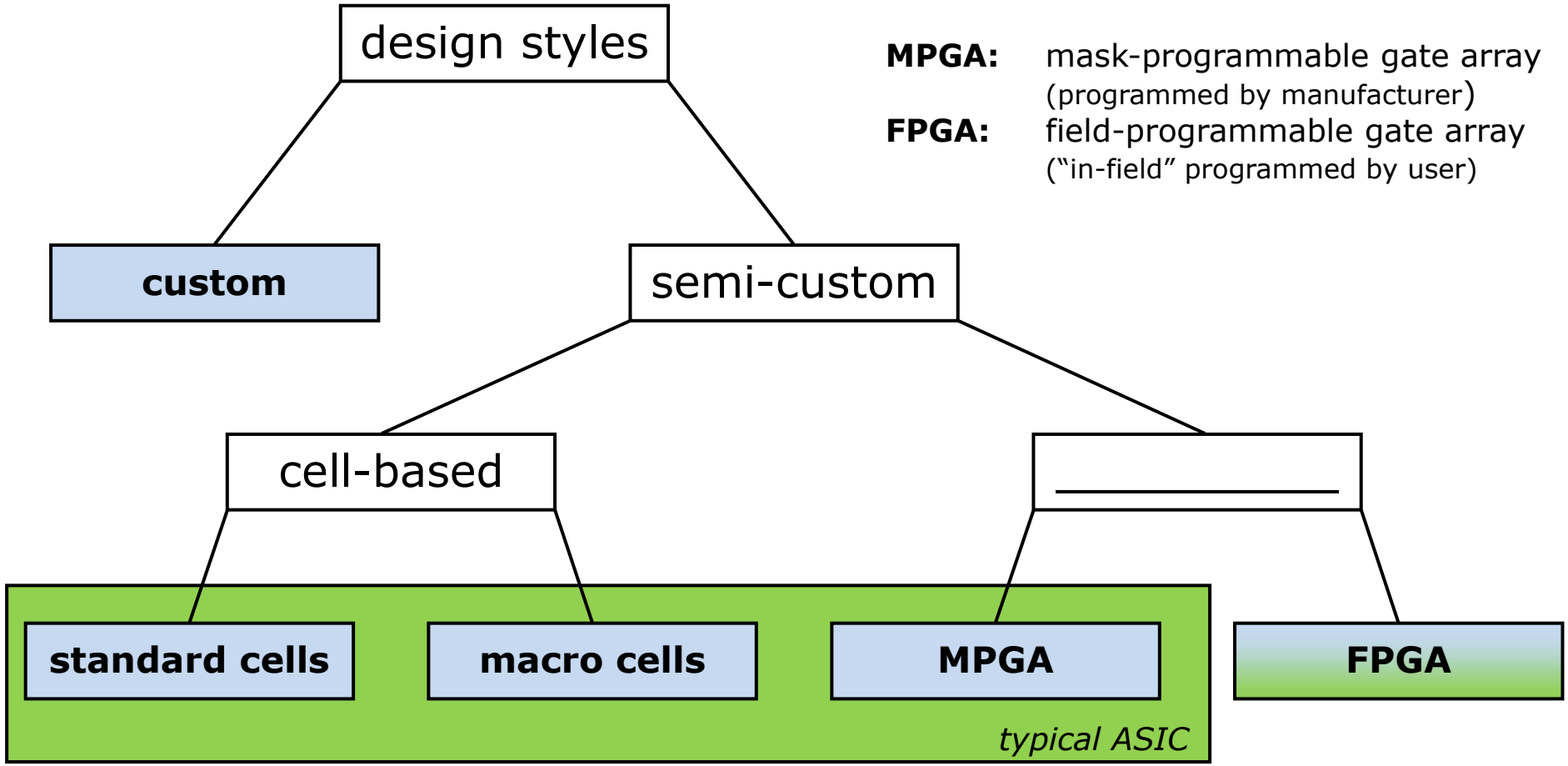








Integrated Circuit – Design Styles



MPGA: mask-programmable gate array (programmed by manufacturer)

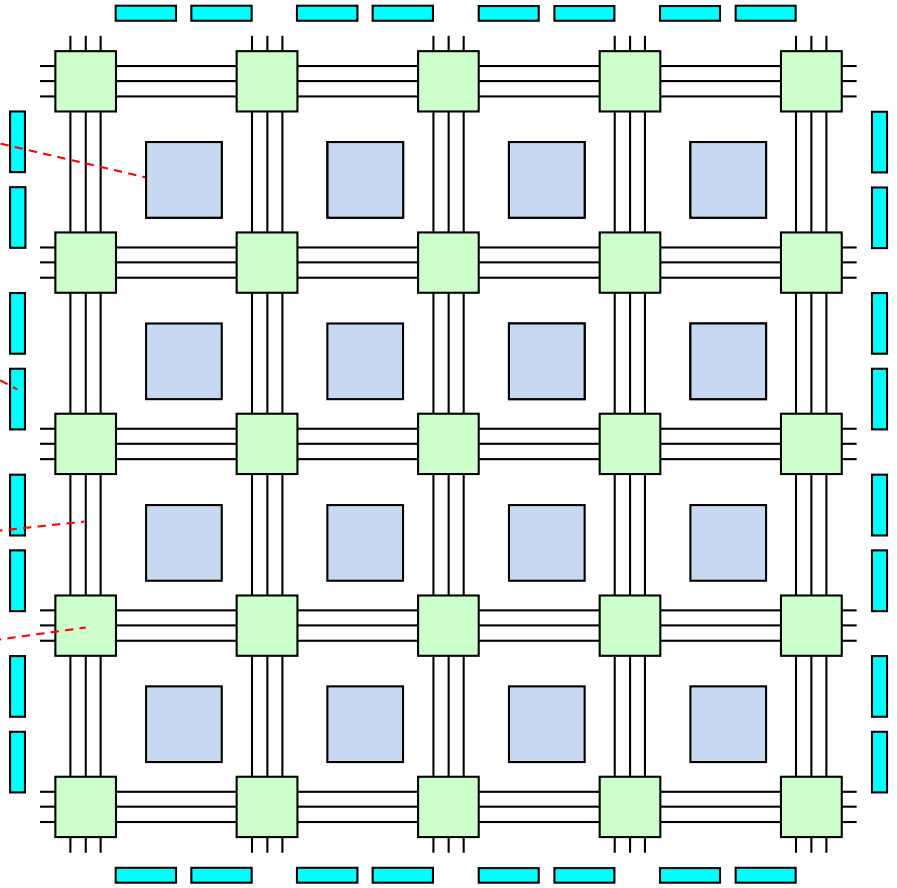
FPGA: field-programmable gate array ("in-field" programmed by user)

Design Styles - Comparison

	custom	cell-based	MPGA	FPGA
density	very high	high	high	medium-low
performance	very high	high	high	medium-low
design time	very long	short	short	very short
manufacturing time	medium	medium	short	very short
cost- low volume	very high	high	high	low
cost- high volume	low	low	low	high

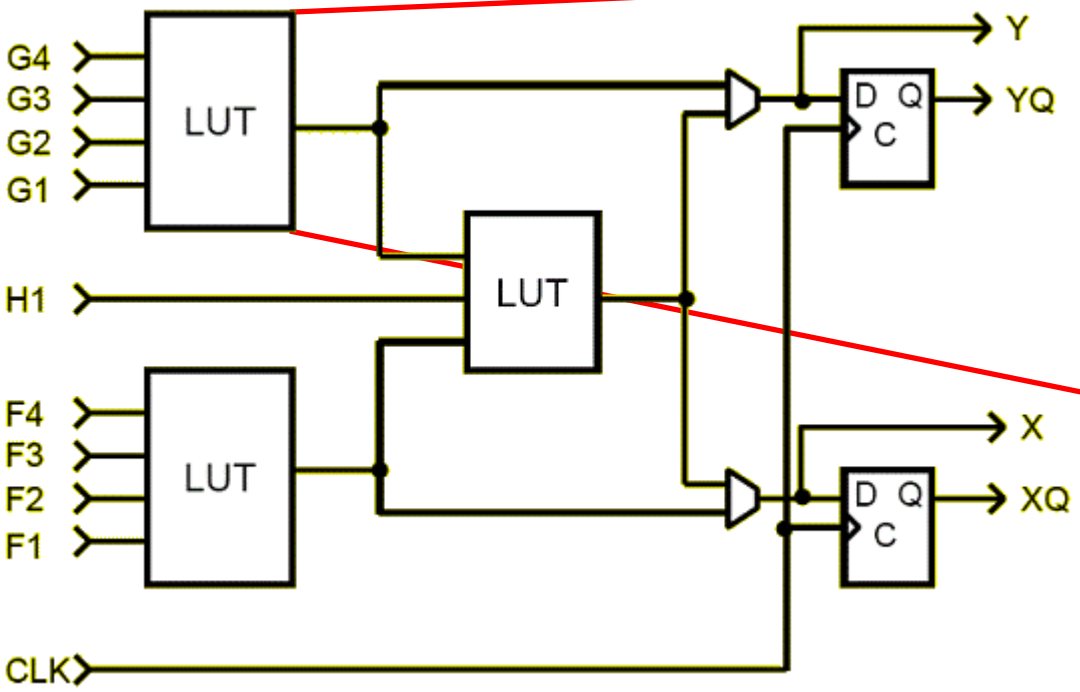
FPGA - Structure

- _____
- _____
- interconnection
  - lines
  - switch matrices



Logic Block (I)

- logic blocks realises the binary functions and state machines



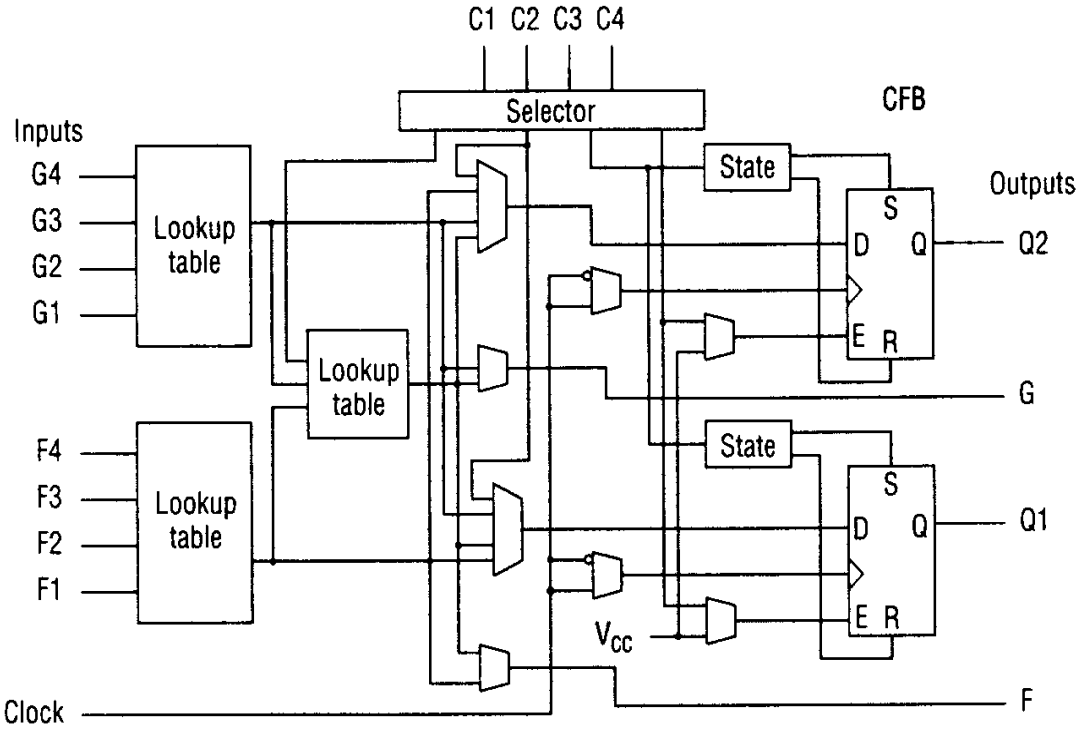
G1	G2	G3	G4	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
...				
1	1	1	0	0
1	1	1	1	1

AND with 4 inputs

→ **any _____ can be described**
(with not more than 4 inputs)

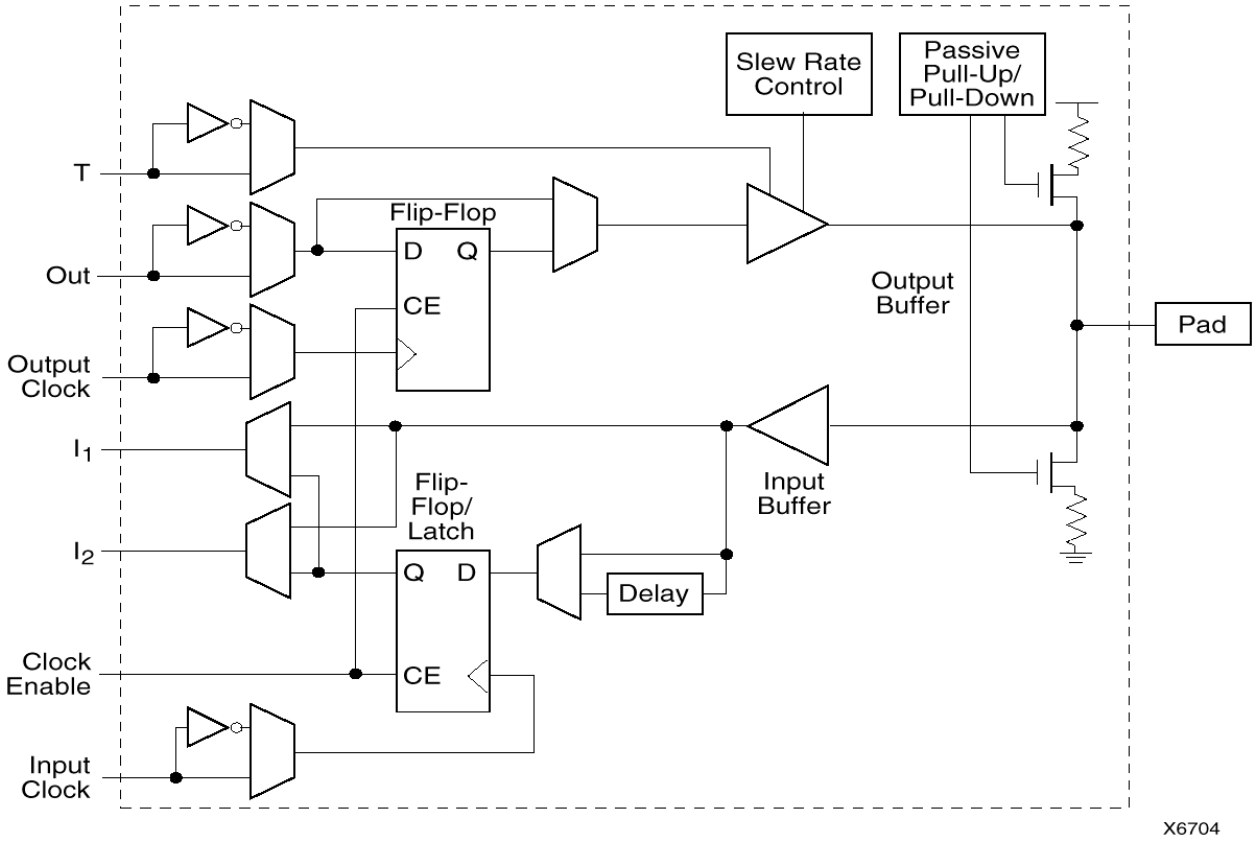
Logic Block (II)

- e. g. Xilinx 4000 series: lookup tables, flip-flops, multiplexer



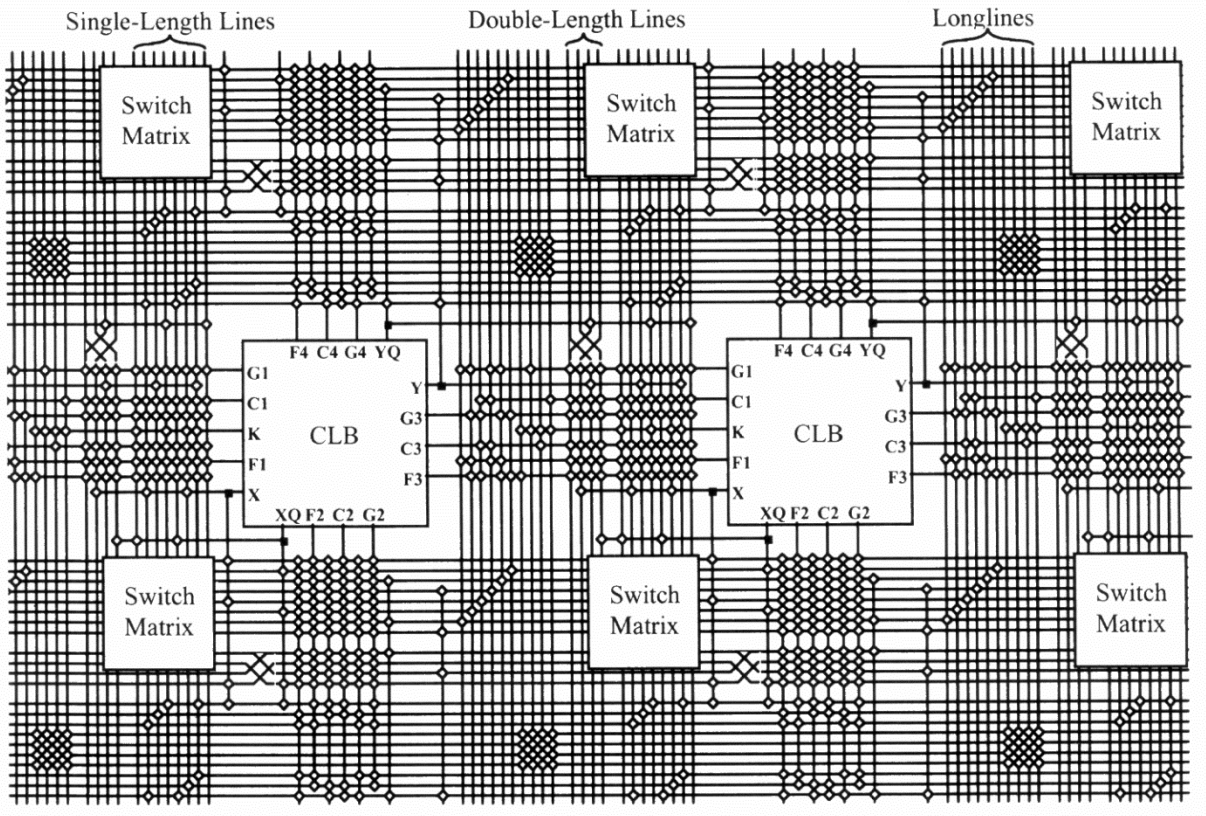
I/O-Block

- e. g. Xilinx 4000 series



Interconnection

- e. g. Xilinx 4000 series



Switch Technologies

switch type	reprogrammable	volatile
EPROM	yes (out of circuit)	no
EEPROM	yes (in circuit)	no
Antifuse	no	no
SRAM	yes (in circuit)	yes

FPGAs

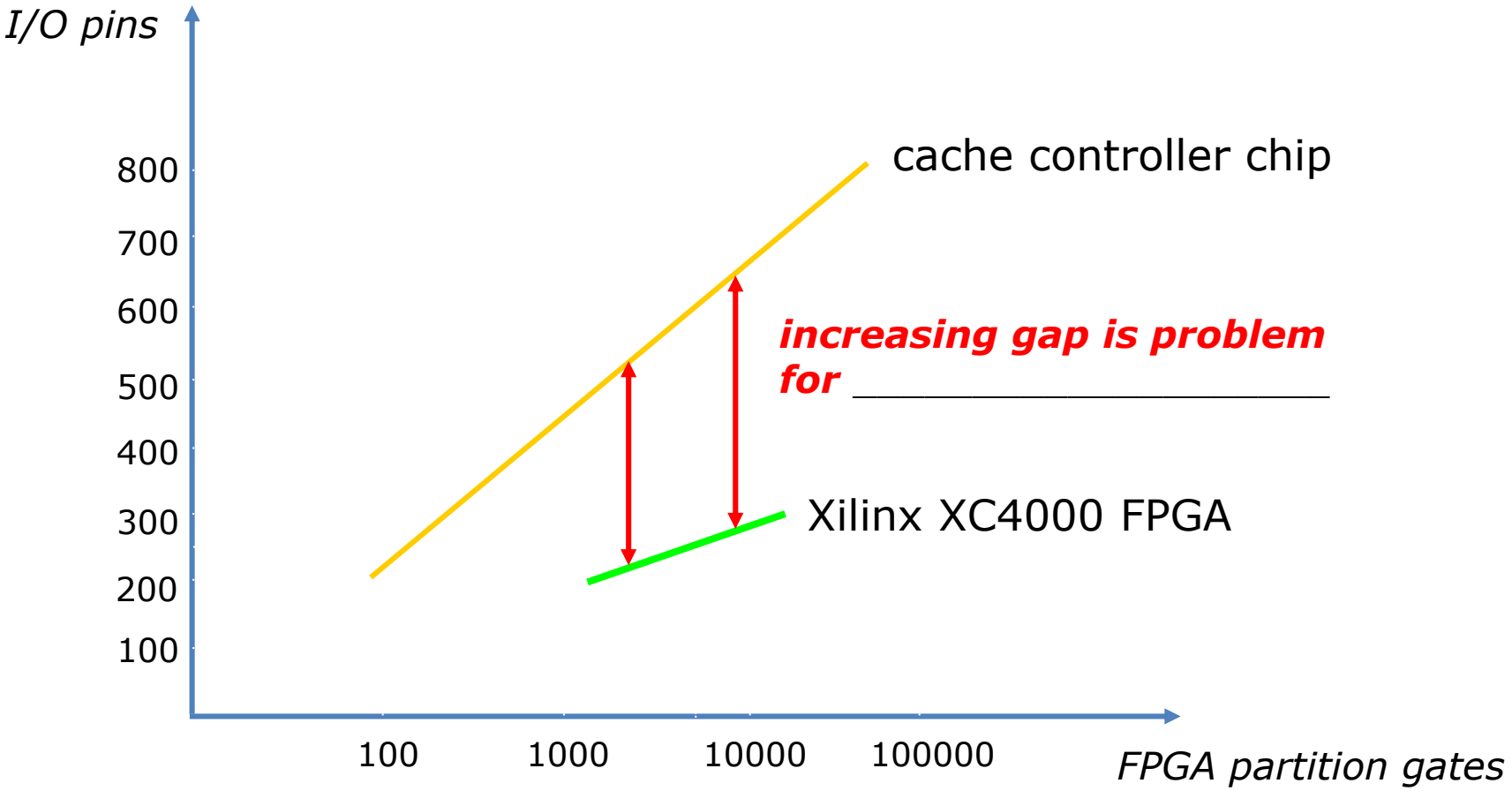
I/O Pin Restrictions

- Rent's Rule
  - relation between gates and I/O pins of a partition

$$N_p = k_p N_g^{\beta}$$

  - N_p... number of I/O pins
  - N_g... number of gates
  - k_p... factor of proportionality
  - β in range of 0.5 (regular designs like SRAM) and 0.75 (random logic)

Example


I/O pins
800
700
600
500
400
300
200
100
cache controller chip
increasing gap is problem for _____
Xilinx XC4000 FPGA
100
1000
10000
100000
FPGA partition gates

Example – Year 2000

- family Xilinx “Virtex-II”: *1.5V core, 150nm, up to 420 MHz*

Device	System Gates	CLB (1 CLB = 4 slices = Max 128 bits)			Multiplier Blocks	SelectRAM Blocks		DCMs	Max I/O Pads(1)
		Array Row x Col.	Slices	Maximum Distributed RAM Kbits		18 Kbit Blocks	Max RAM (Kbits)		
XC2V40	40K	8 x 8	256	8	4	4	72	4	88
XC2V80	80K	16 x 8	512	16	8	8	144	4	120
XC2V250	250K	24 x 16	1,536	48	24	24	432	8	200
XC2V500	500K	32 x 24	3,072	96	32	32	576	8	264
XC2V1000	1M	40 x 32	5,120	160	40	40	720	8	432
XC2V1500	1.5M	48 x 40	7,680	240	48	48	864	8	528
XC2V2000	2M	56 x 48	10,752	336	56	56	1,008	8	624
XC2V3000	3M	64 x 56	14,336	448	96	96	1,728	12	720
XC2V4000	4M	80 x 72	23,040	720	120	120	2,160	12	912
XC2V6000	6M	96 x 88	33,792	1,056	144	144	2,592	12	1,104
XC2V8000	8M	112 x 104	46,592	1,456	168	168	3,024	12	1,108

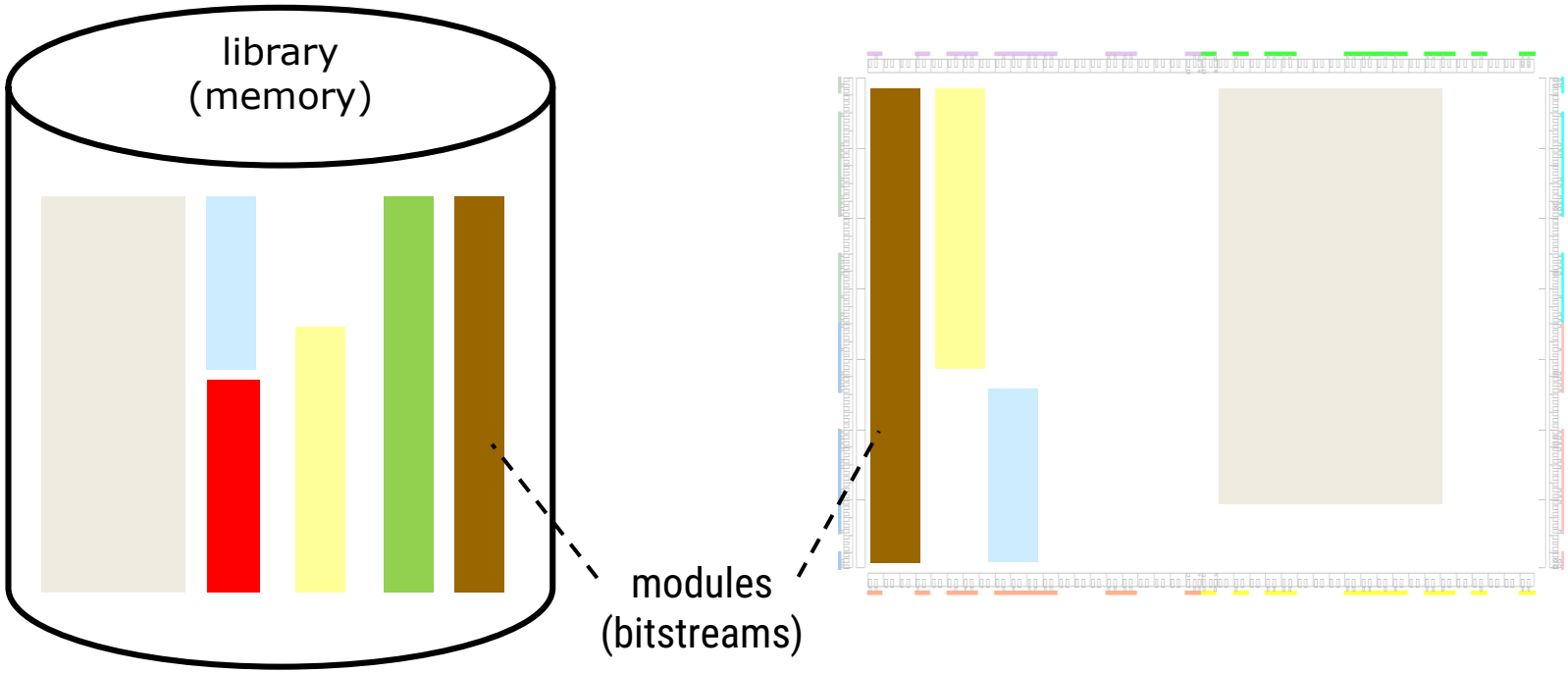
Example – Year 2009

- family Xilinx “Virtex-6”: *1.0V core, 40 nm, up to 600 MHz*

Part Number	XC6VLX75T	XC6VLX130T	XC6VLX195T	XC6VLX240T	XC6VLX365T	XC6VLX550T	XC6VLX760
EasyPath™ FPGA Cost Reduction Solutions (1)	XCE6VLX75T	XCE6VLX130T	XCE6VLX195T	XCE6VLX240T	XCE6VLX365T	XCE6VLX550T	XCE6VLX760
Slices (2)	11,640	20,000	31,200	37,680	56,880	85,920	118,560
Logic Cells (3)	74,496	128,000	199,680	241,152	364,032	549,888	758,784
CLB Flip-Flops	93,120	160,000	249,600	301,440	455,040	687,360	948,480
Maximum Distributed RAM (Kbits)	1,045	1,740	3,040	3,650	4,130	6,200	8,280
Block RAM/FIFO w/ ECC (36Kbits each)	156	264	344	416	416	632	720
Total Block RAM (Kbits)	5,616	9,504	12,384	14,976	14,976	22,752	25,920
Mixed Mode Clock Managers (MMCM)	6	10	10	12	12	18	18
Maximum Single-Ended I/O	360	600	600	720	720	1,200	1,200
Maximum Differential I/O Pairs	180	300	300	360	360	600	600
DSP48E1 Slices	288	480	640	768	576	864	864
PCI Express® Interface Blocks	1	2	2	2	2	2	–
10/100/1000 Ethernet MAC Blocks	4	4	4	4	4	4	–
GTX Low-Power Transceivers	12	20	20	24	24	36	–
GTH High-Speed Transceivers	–	–	–	–	–	–	–
Commercial	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2, -3	-L1, -1, -2	-L1, -1, -2
Industrial	-L1, -1, -2	-L1, -1, -2	-L1, -1, -2	-L1, -1, -2	-L1, -1, -2	-L1, -1	-L1, -1
Configuration Memory (Mbits)	25.0	41.7	58.7	70.4	91.6	137.4	176.3

Reconfiguration

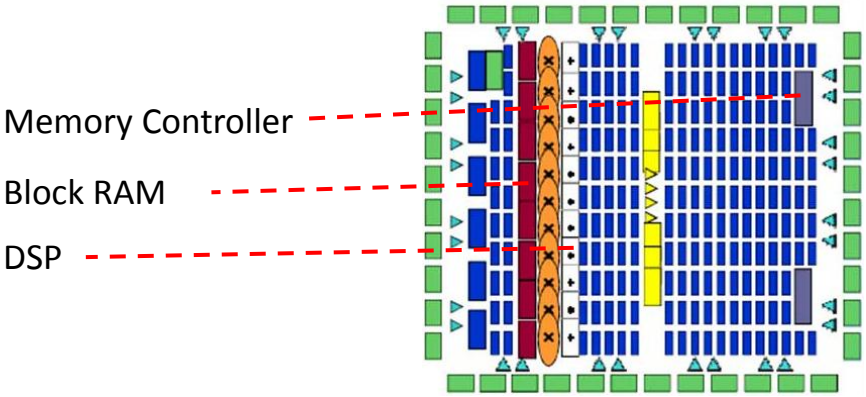
- change configuration of FPGA

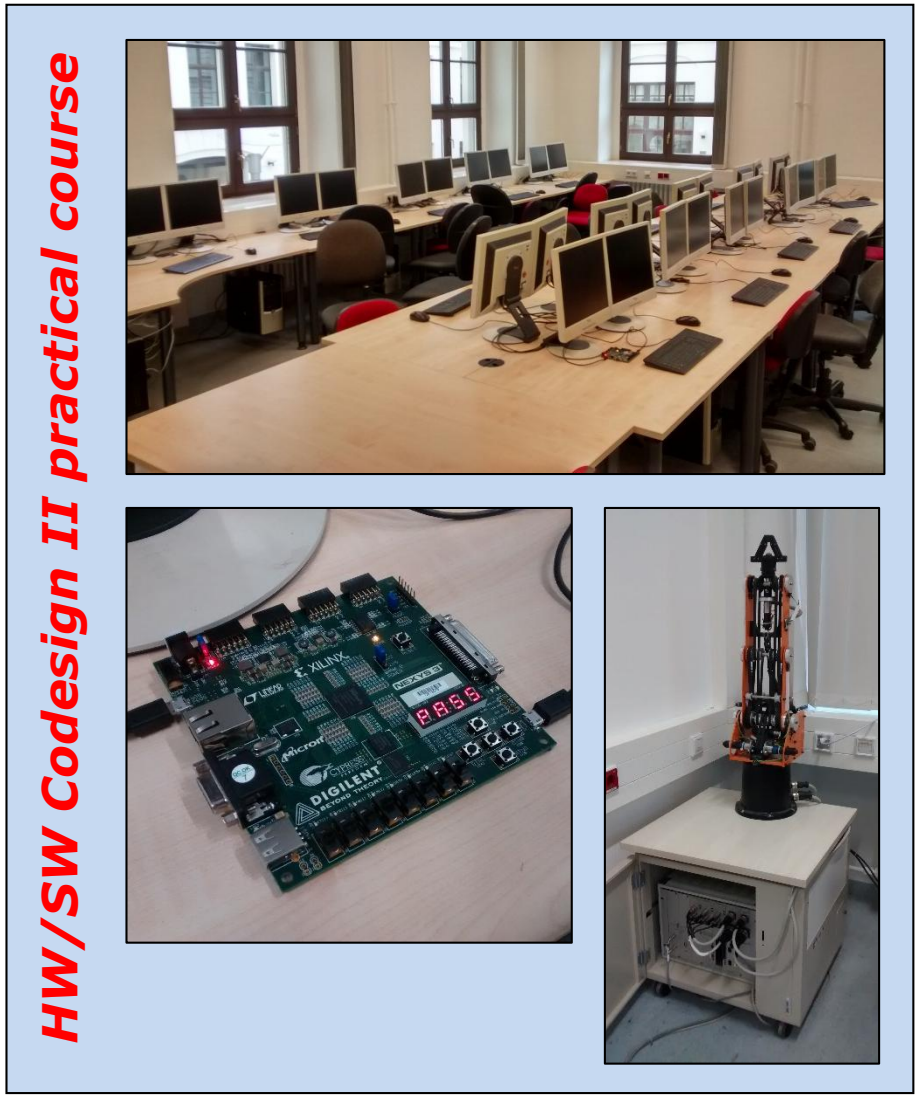


- technology provided, but still a lot of research necessary

Extensions

- special blocks
  - RAM
  - Multipliers
  - DSP
  - …
- e. g. Xilinx Spartan 6





FPGA Development

- to implement system:
  - set all lookup tables
  - set all multiplexer and flip-flop configurations
  - set up routing (by definition of wire connections)

  → e.g.: “Virtex-6” with **25 – 170 million** bits configuration memory
  → **TOO COMPLEX to develop manually**

- usage of hardware description language (HDL) to _____ (not “programming”) the system on higher level (algorithm, register-transfer)

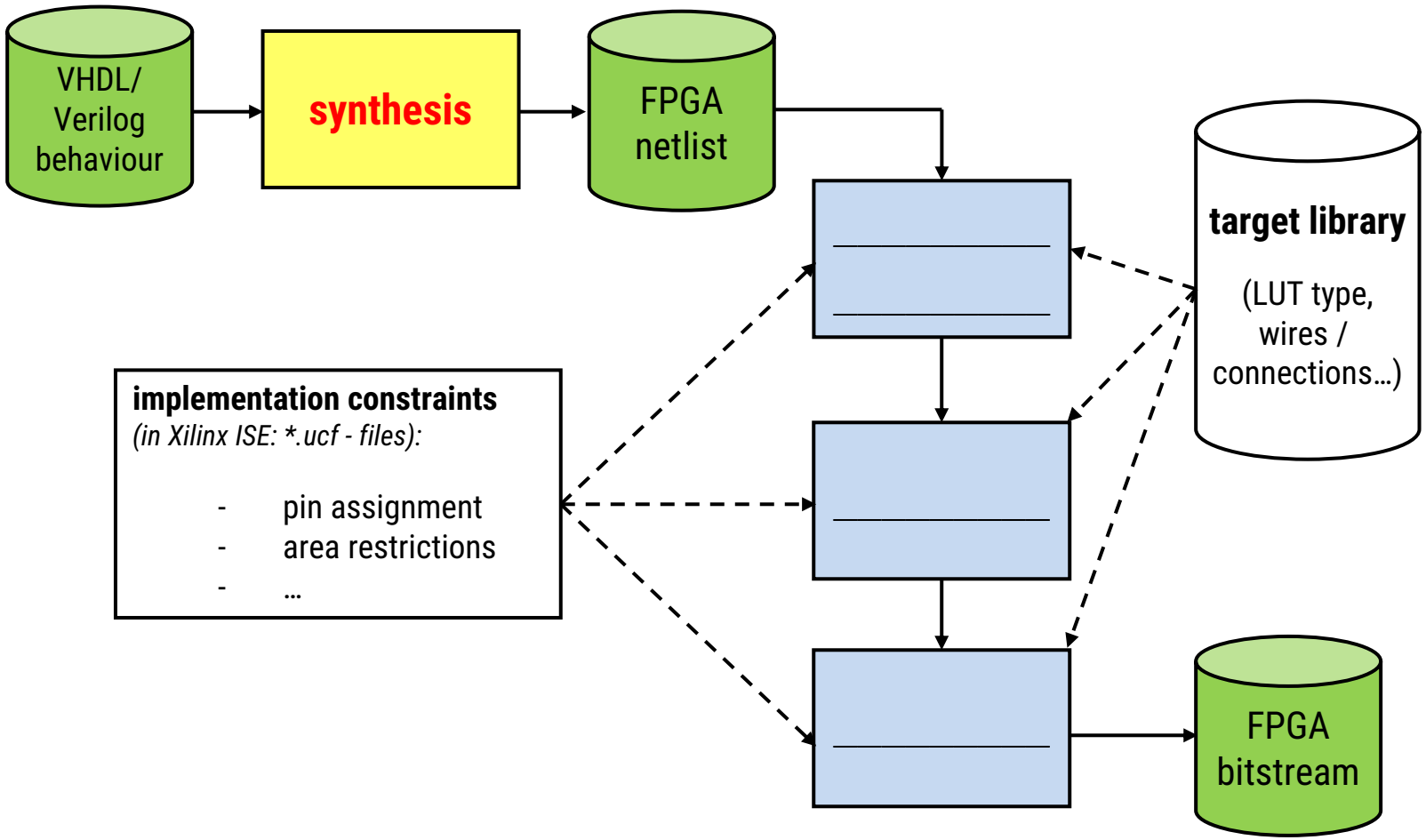
- _____ used to transform the description to a bitfile (configuration memory content) for selected FPGA

HDL vs. Programming Language

	HDL	Programming Language
operations	parallel	_____
description	structure and behaviour	behaviour
timing	important to consider	implicit sequential
aim	simulation, synthesis, documentation, exchange	implementation
abstraction level	(algorithm), register-transfer, logic	algorithm

- VHDL = **V**ery High Speed Integrated Circuit **H**ardware **D**escription **L**anguage
- VHDL = HDL for behavioural and structural description on _____

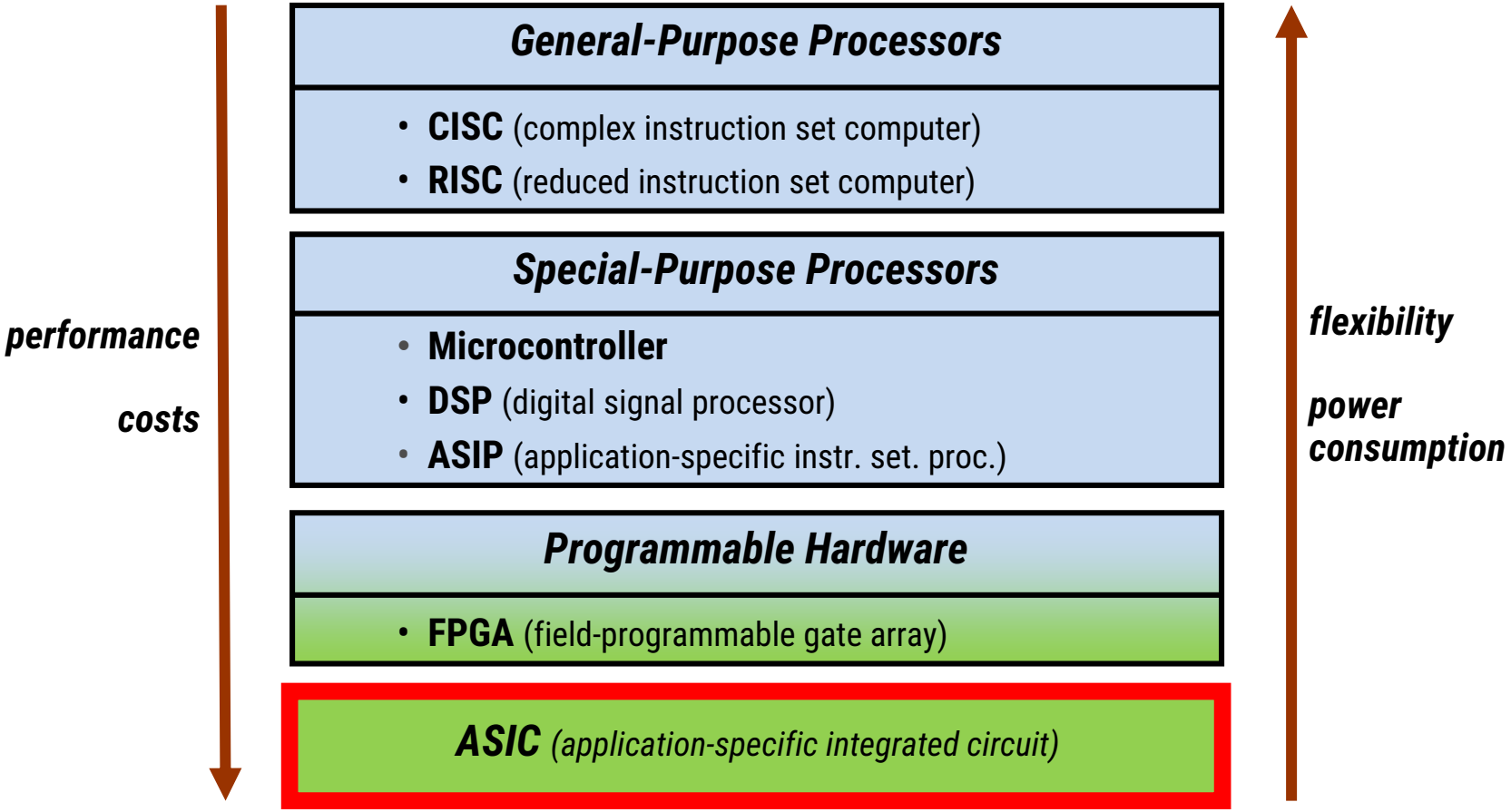
HW-Synthesis Process



FPGA Application Domains

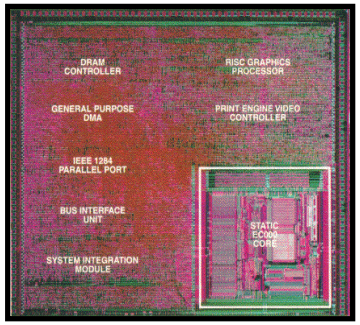
- glue logic (connect two incompatible hardware components)
- rapid prototyping, emulation
- embedded systems:
  - faster than processors, more flexible than ASIC
    - → ASIC replacement
      - when volume too small to justify ASIC
      - for reduced time-to-market
    - → processor replacement
      - controller as part of configurable systems-on-a-chip
- trend: more dedicated components (e.g. for communication)

Implementation Alternatives



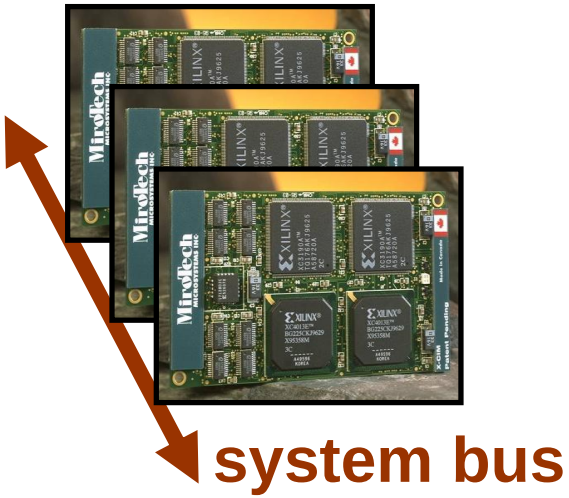
System Structures (I)

- "system on a chip" (SoC)



- board systems

- multi-board systems



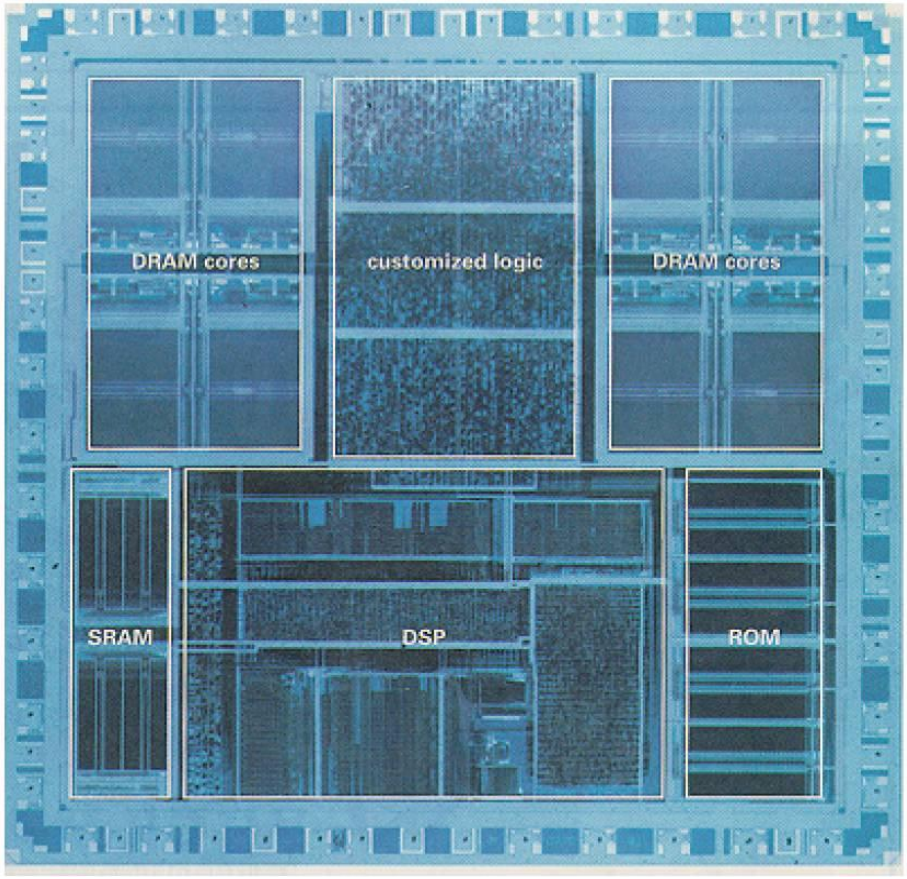
System Structures (II)

- comparison

	system on a chip	board system	multi-board system
weight, size, power consumption	low	high	very high
reliability	very high	high-low	low
cost (high volume)	low	high	high

System On A Chip (I)

- e. g. audio processing SoC (Siemens)
  - 16 bit DSP
  - 15k system gates
  - SRAM, ROM
  - 1Mbit DRAM



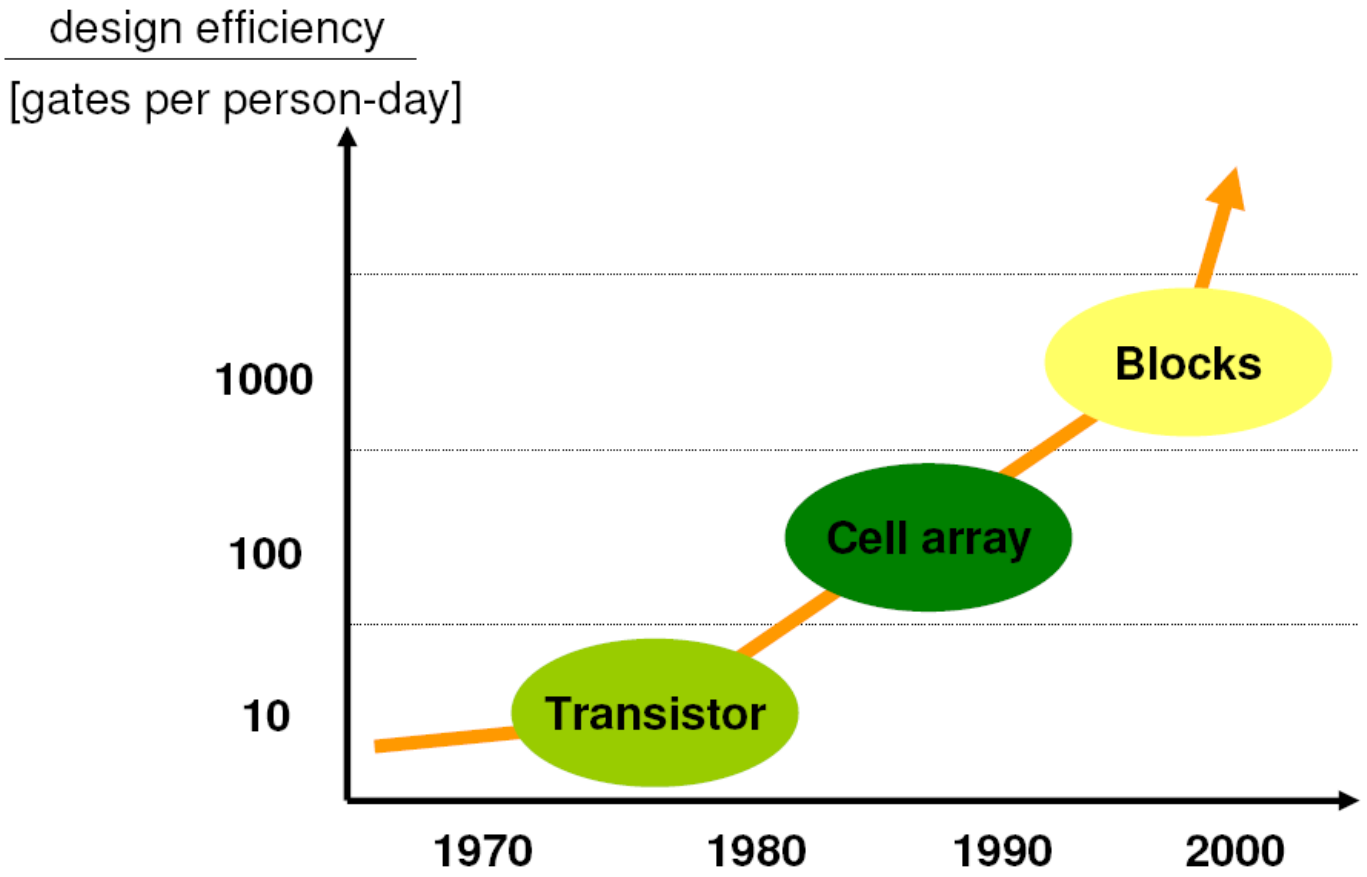
System On A Chip (II)

- integration of analog components
  - power electronics (amplifier for actors, …)
  - sensors
- high electromagnetic compatibility, low radiation
- block-oriented design style
  - integration of processor cores, memory, coprocessors, interfaces,…

→ _____

→ **blocks may be** _____

Block-Oriented Design



IP Block Types (I)

- _____ blocks
  - described in a hardware description language (HDL)
  - synthesisable
- firm blocks
  - HDL and net lists, possibly floor planning
  - partly synthesisable
- _____ blocks
  - complete layout for target technology
  - cannot be synthesised

IP Block Types (II)

- comparison

block type	flexibility	predictability	Portability	IP protection
soft	very flexible	unpredictable	unlimited	none
firm	flexible	unpredictable	library mapping	none
hard	inflexible	highly predictable	process mapping	good

IP Libraries

- DesignWare Foundatoin Library (Synopsys)[1]

Some available IPs with estimated design effort in person days:

Absolute Value	3
Adder	4
Adder-Subtractor	3
Arithmetic Shifter	4
Decrementer	3
Divider	20
Incrementer	3
Incrementer-Decrementer	3
Multiplier-Accumulator	13
Multiplier	10
Duplex Adder/Subtractor	20
Multistage Pipelined Multipliers	12

[1] http://www.synopsys.com/news/pubs/dwtb/jan98/frame_dw1.html

IP Based Design

- methods and standards for
  - design of reusable IP blocks
  - interfacing IP blocks → *Virtual Socket Interface Alliance (VSI)*[1]

- actual problems
  - evaluation of IP blocks
  - development of web-based, computer-aided design (CAD) tools
  - (co)simulation of IP blocks

[1] http://www.vsi.org/