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HW/SW Codesign II

Emulation and (Rapid) Prototyping

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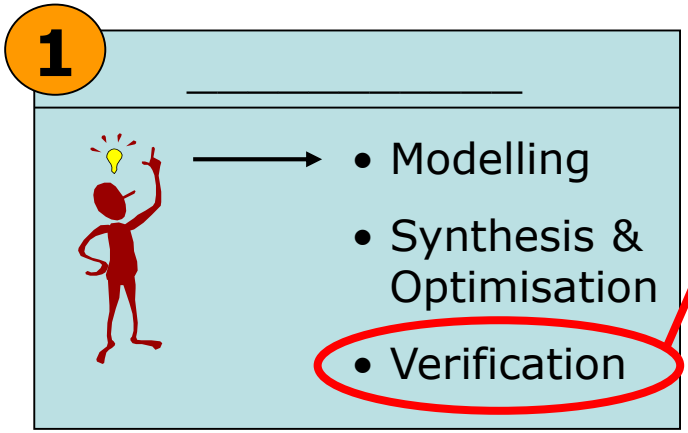
Sommersemester 2015

Contents

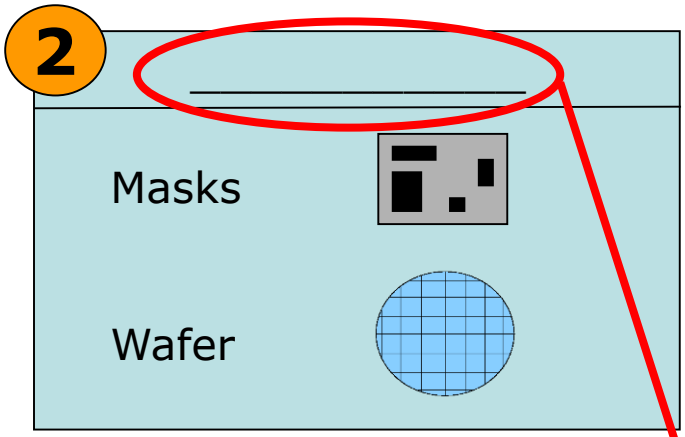
- Prototyping
- Emulation
- Rapid Prototyping

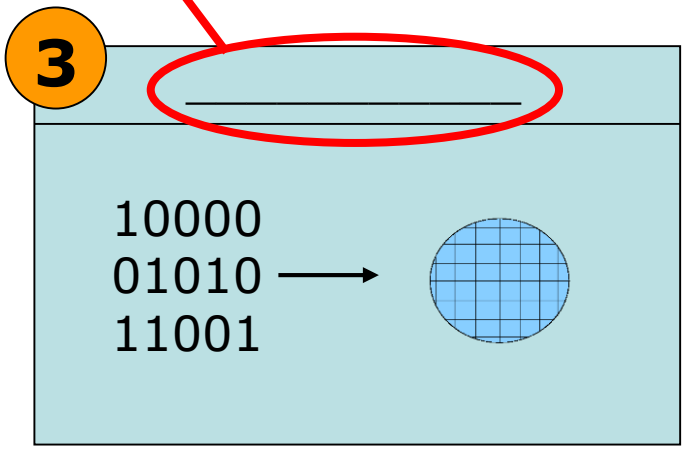
IC Design



very slow, complete tests impossible

faster, but if error is found:
redesign and refabrication
→ **design errors very expensive**



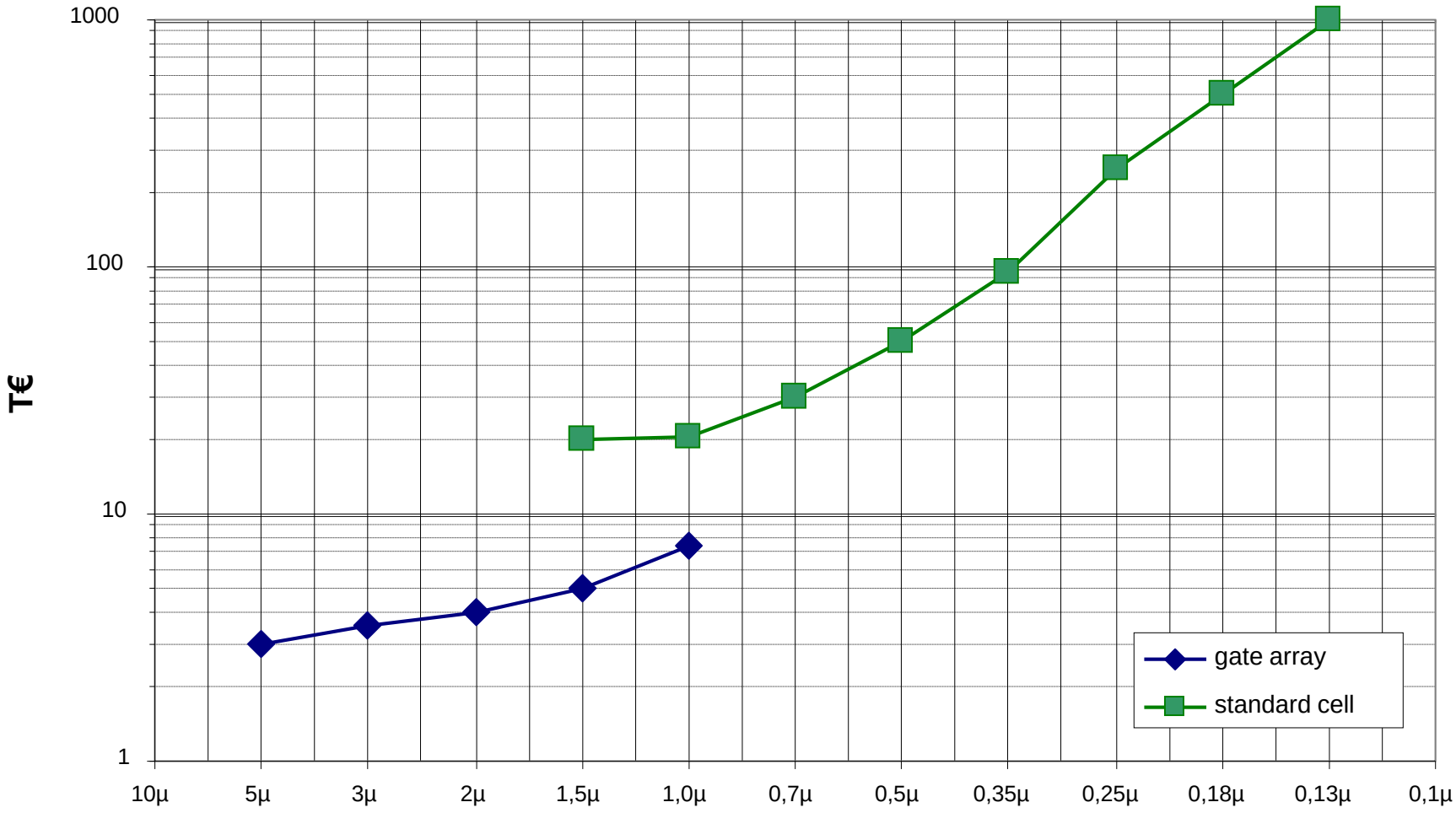


very expensive

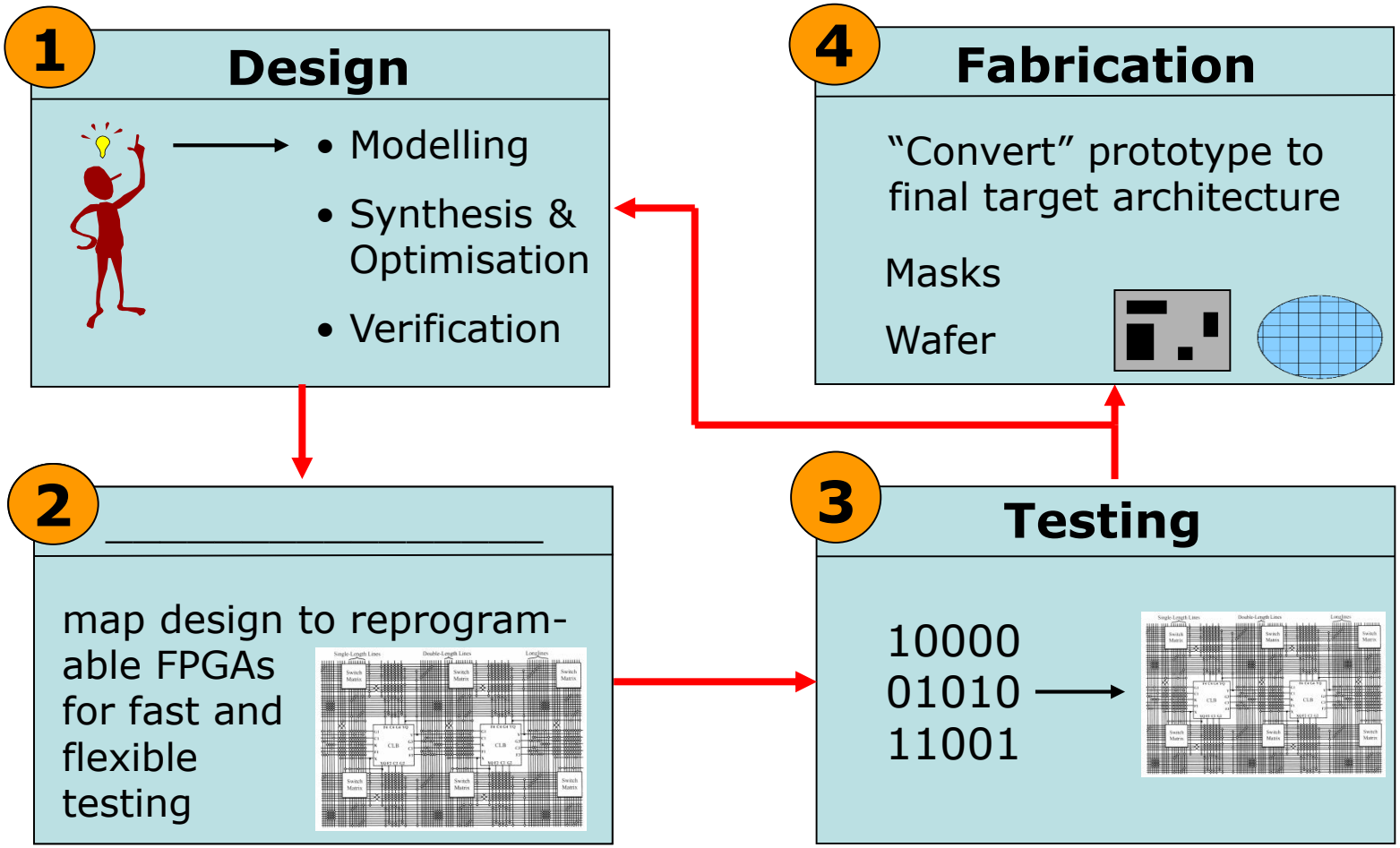
Simulation of Complex ASICs

design level	description language	primitives	simulation time *(cycles/instruction)*
algorithm	HLL	instruction sets	10-100
architecture	HLL, HDL	functional blocks	1K-10K
register transfer	HDL	RTL primitives	1M-10M
logic	HDL, netlist	logic gates	10M-100M

Costs for Mask and Prototype Fabrication



Solution


1
Design
• Modelling
• Synthesis & Optimisation
• Verification
2
map design to reprogram-able FPGAs for fast and flexible testing
3
Testing
10000
01010
11001
4
Fabrication
"Convert" prototype to final target architecture
Masks
Wafer

Pro and Contra for FPGA Based Prototyping

- advantages in comparison to _____
  - no masks necessary
  - fast turnaround
  - low NRE (non-recurring engineering) changes
  - low risk
  - efficient design verification
  - low testing cost

- disadvantages in comparison to mask prototype fabrication
  - _____
  - chip costs
  - slower speed
  - no accurate timing information

Prototype

- **definition**

  A prototype (of an embedded system) is an implementation with _____ of the system specification and relaxed constraints for

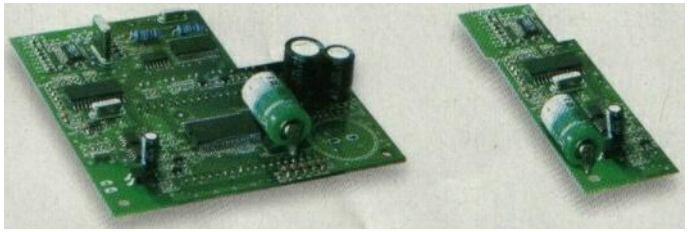
  - _____
  - design size
  - design cost

- remark
  - prototype executes functionality much faster than a simulation

Prototype to Final Design

- design step from prototype to final design removes prototype limitations

prototype *final*



- may be complex if the prototyping and fabrication architectures differ much
  - _____
  - general purpose processor ←→ microcontroller

- testing still necessary due to missing information about prototype limits (especially timing)

Problems of FPGA Based Prototyping

- FPGA capacity is limited
- implementation of interconnection between blocks and chips is different from final design
- number of I/O pins is limited
- visibility of probes (test points)

- **homogeneous prototype architectures**
  - minimises problems
  - limits of single technology
  - named: _____

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- Prototyping
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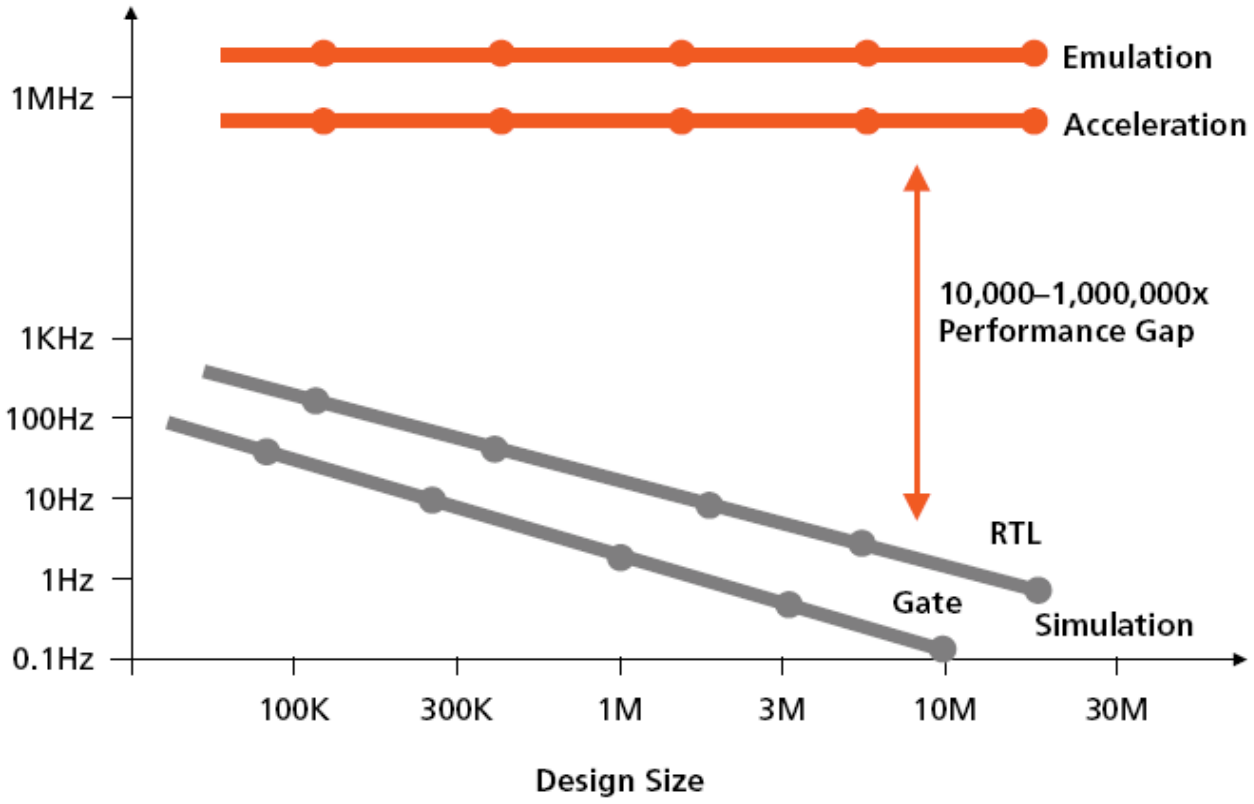
Emulation Systems - Parameters

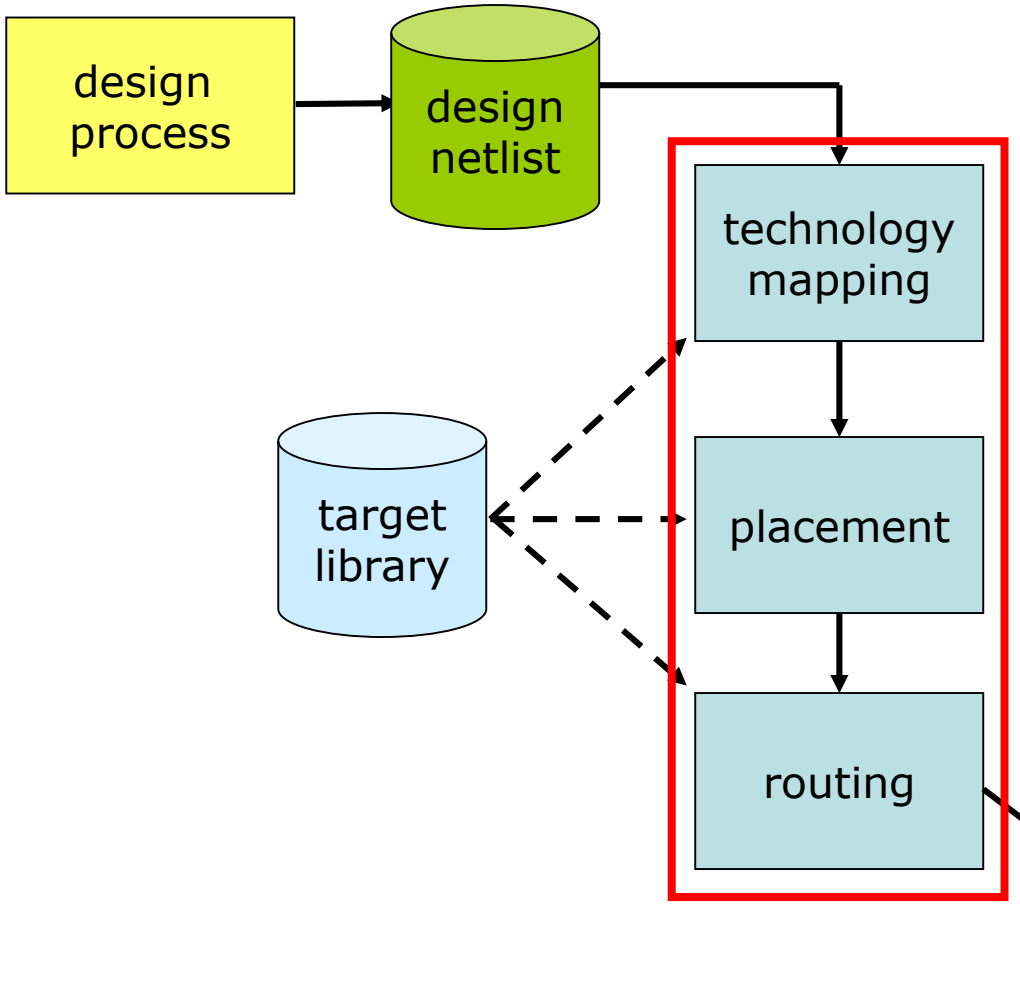
- FPGA type
  - number of gates
  - number of I/O pins
  - mapping efficiency
  - memory blocks
  - function blocks
  - internal interconnection structure
- system of many FPGAs
  - number of FPGAs
  - _____
- software for prototype design (mapping)
  - partitioning of design netlist
  - solving the clock skew problems
  - logic analyzing, stimulus generator

Time Improvement



Quelle: *Incisive Enterprise Palladium Series with incisive XE software, Cadence Design Systems, Inc., 2006*

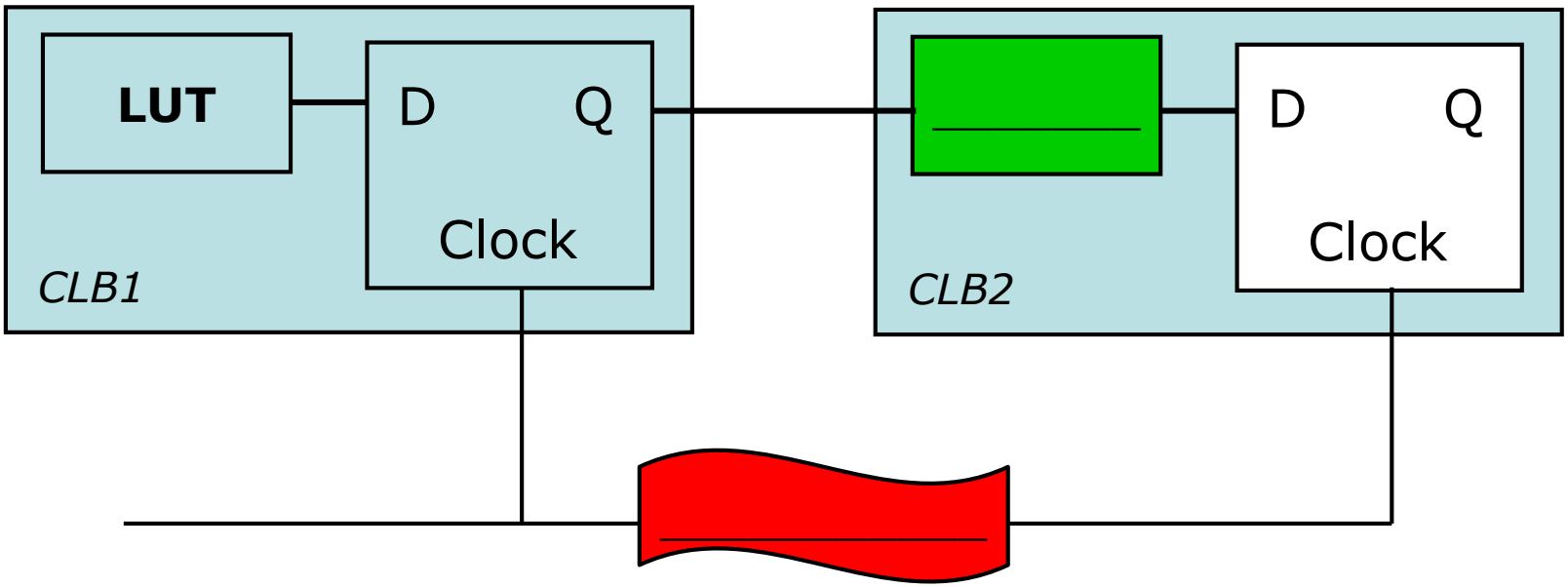
Mapping Software



has to compile a FPGA prototype system which correspondents as much as possible with the final system on the final platform and eliminates typical FPGA problems (clock skew, line lengths, …)

Clock Skew

- no homogenous clock all over the FPGA due to connection delays (clock distribution delay)



hold-time violation occurs when *routing delay > LUT delay*

Clock Skew Solutions

- hardware:
  - dedicated clock distribution networks
  - _____ clock distribution

- software:
  - optimising placement and routing (path analysis)
  - inserting combinatorial clock enables

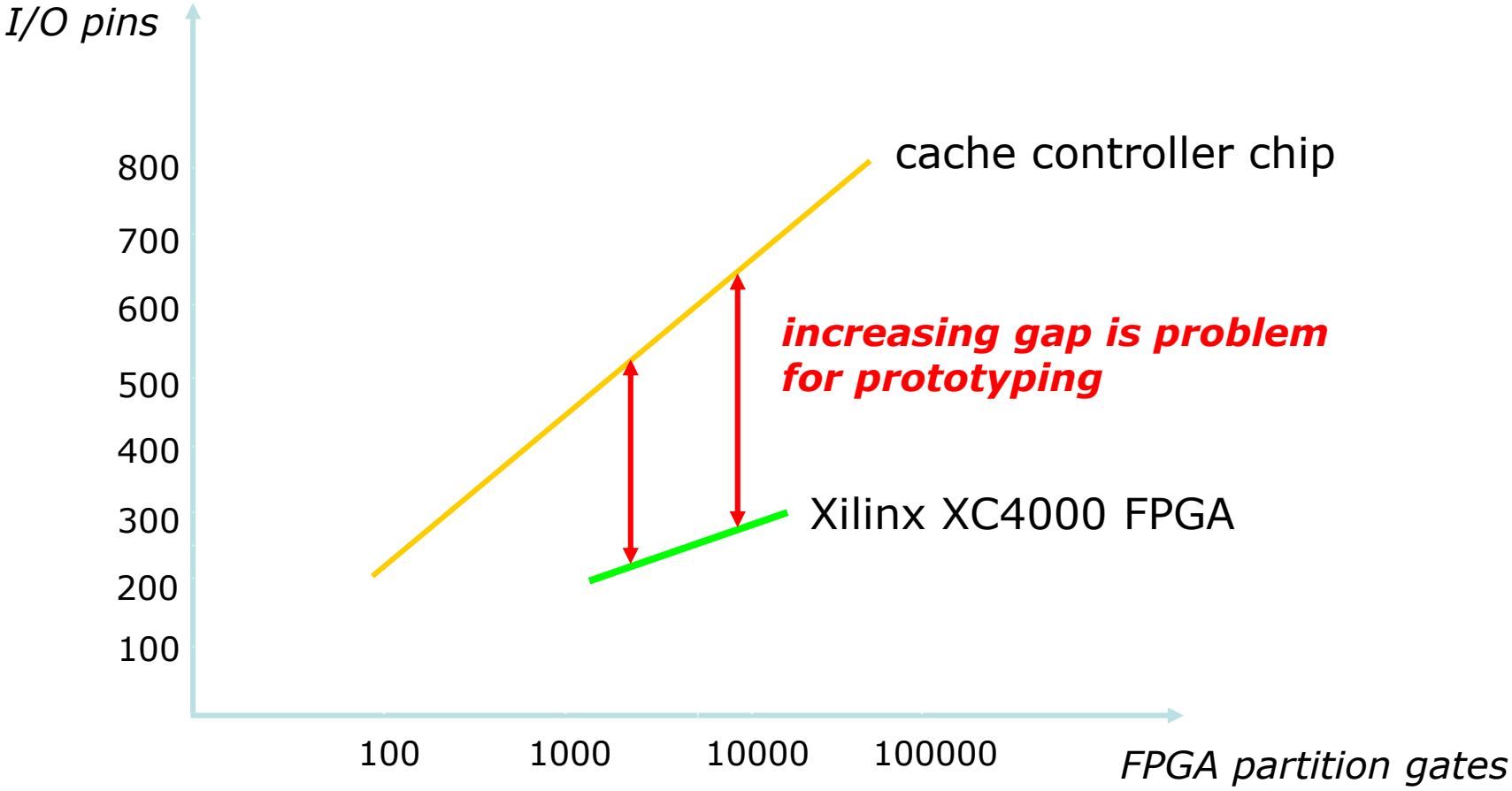
I/O Pin Restrictions

- Rent's Rule
  - relation between gates and I/O pins of a partition

$$\_\_\_\_\_$$

  - N_p... number of I/O pins
  - N_g... number of gates
  - k_p... factor of proportionality
  - β in range of 0.5 (regular designs like SRAM) and 0.75 (random logic)

Example

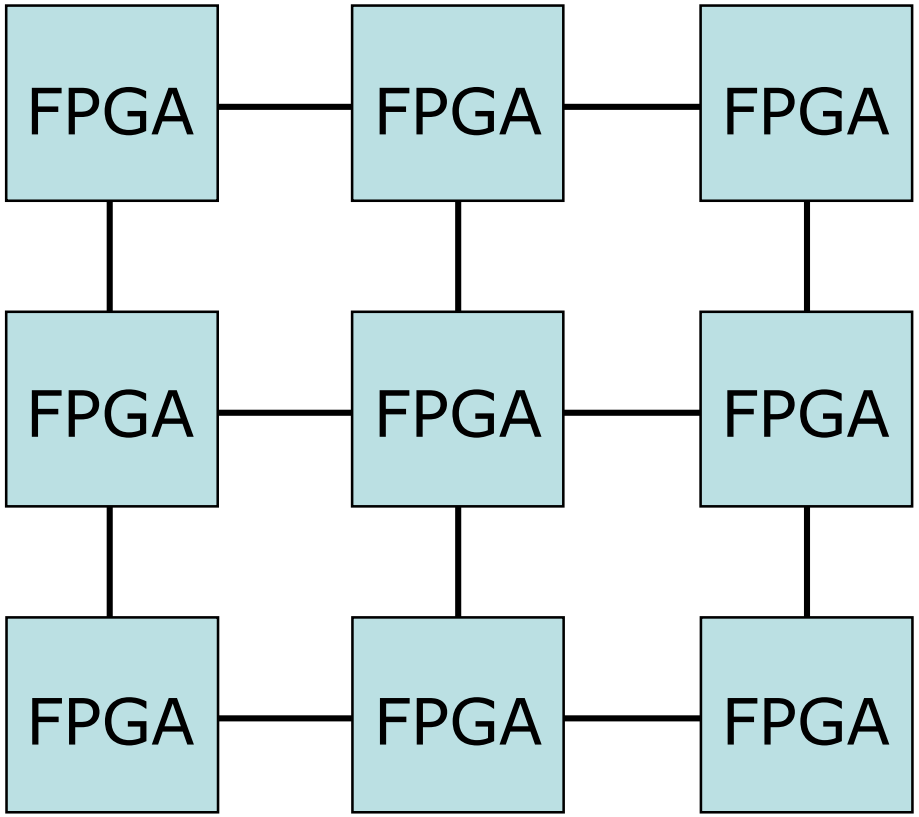

I/O pins
800
700
600
500
400
300
200
100
cache controller chip
increasing gap is problem
for prototyping
Xilinx XC4000 FPGA
100
1000
10000
100000
FPGA partition gates

Multi-FPGA Systems

- to emulate bigger systems it is necessary to build an emulation system of many FPGAs, which differs in
  - number of FPGAs
  - interconnection topologies
    - _____ (nearest neighbouring)
    - _____ (full and partial)

MESH Interconnection

- nearest neighbour interconnection

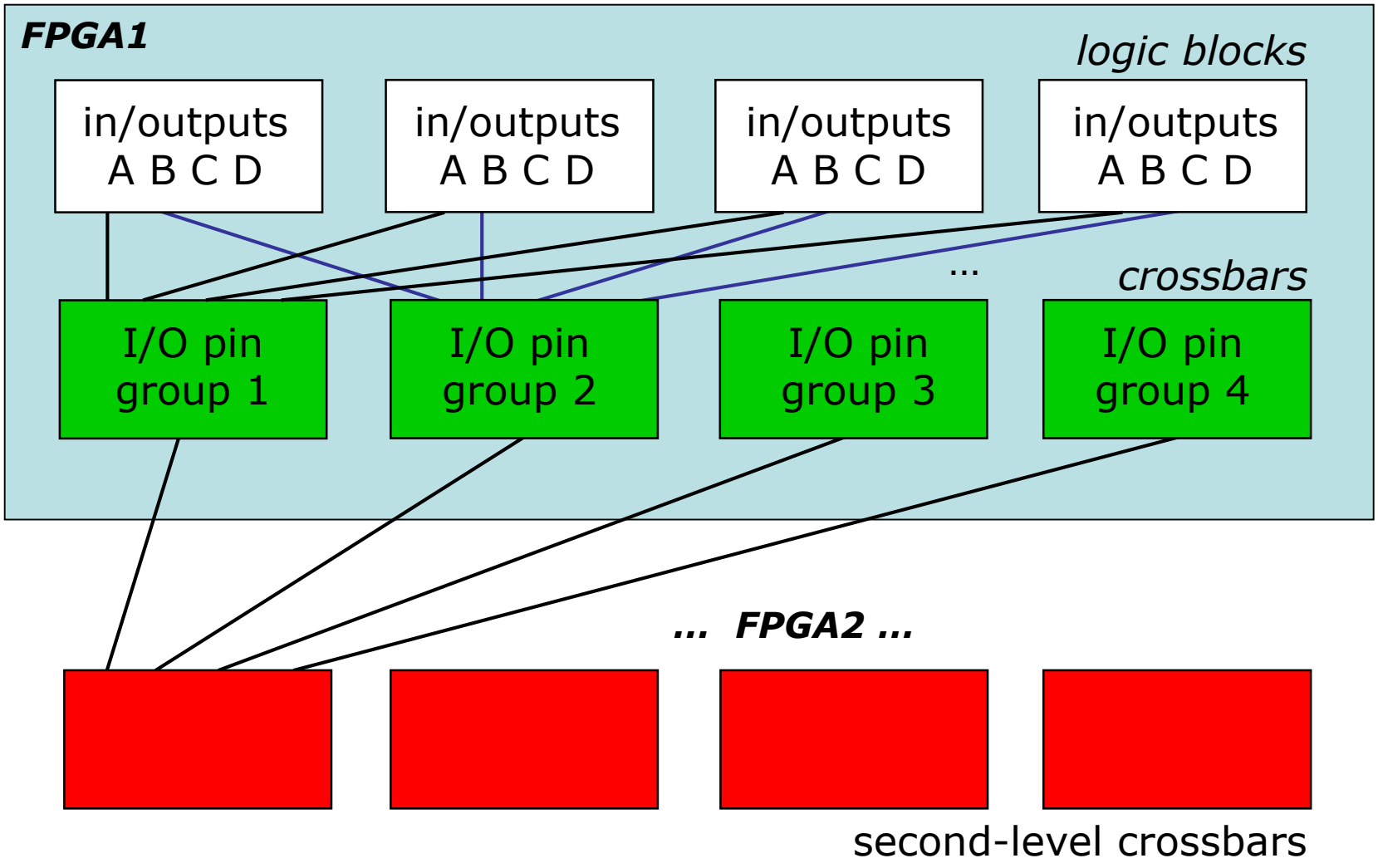


Advantages and Disadvantages

- advantages
  - uniform: all chips the same
  - easy to layout on PCB

- disadvantages
  - _____
  - logic utilisation of FPGA is limited by pins, which are used for interconnection
  - long and unpredictable delays
  - no natural hierarchical extension

Partial Crossbar Interconnection (I)



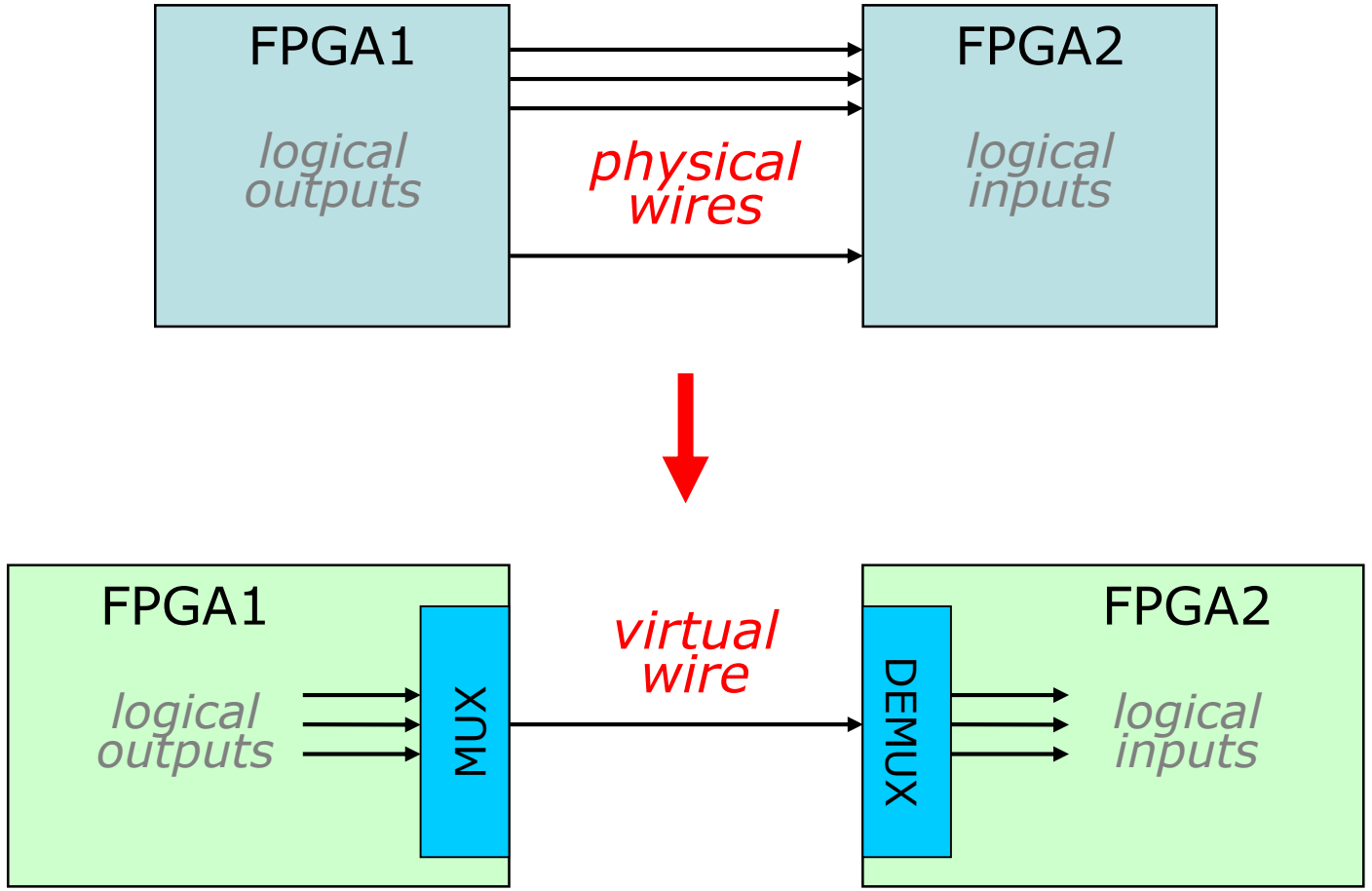
Partial Crossbar Interconnection (II)

- partial crossbar consists of a _____ connected to logic blocks but not to each other
- I/O pins of each FPGA are divided into subsets
- each subset is connected by a full crossbar circuit switch
- partial crossbar is a potentially blocking network
- partial crossbar's size is proportional to the number of FPGA pins
- all interconnections go through one / three crossbar chips for a one-level / two-level partial crossbar interconnect → delays are uniform and bounded

Virtual Wires (I)

- map several logic wires to a single physically wire (_____)
- all registers are clocked with a virtual clock
- the clock period allows the communication of two neighboured FPGAs
- for partitioning no further limitations for I/O pins
  → leads to good FPGA – utilisation
- decreases system speed (due to virtual clock)

Virtual Wires (II)



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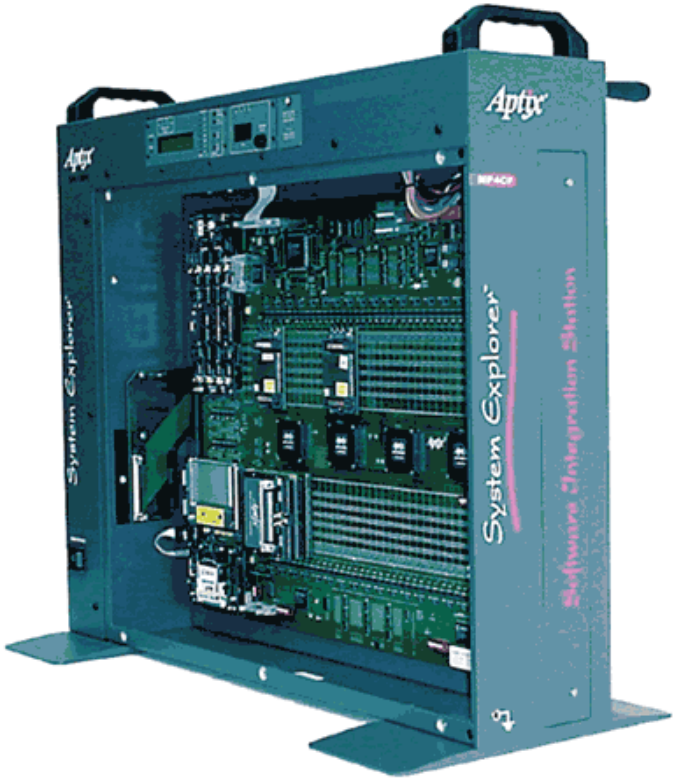
Rapid Prototyping

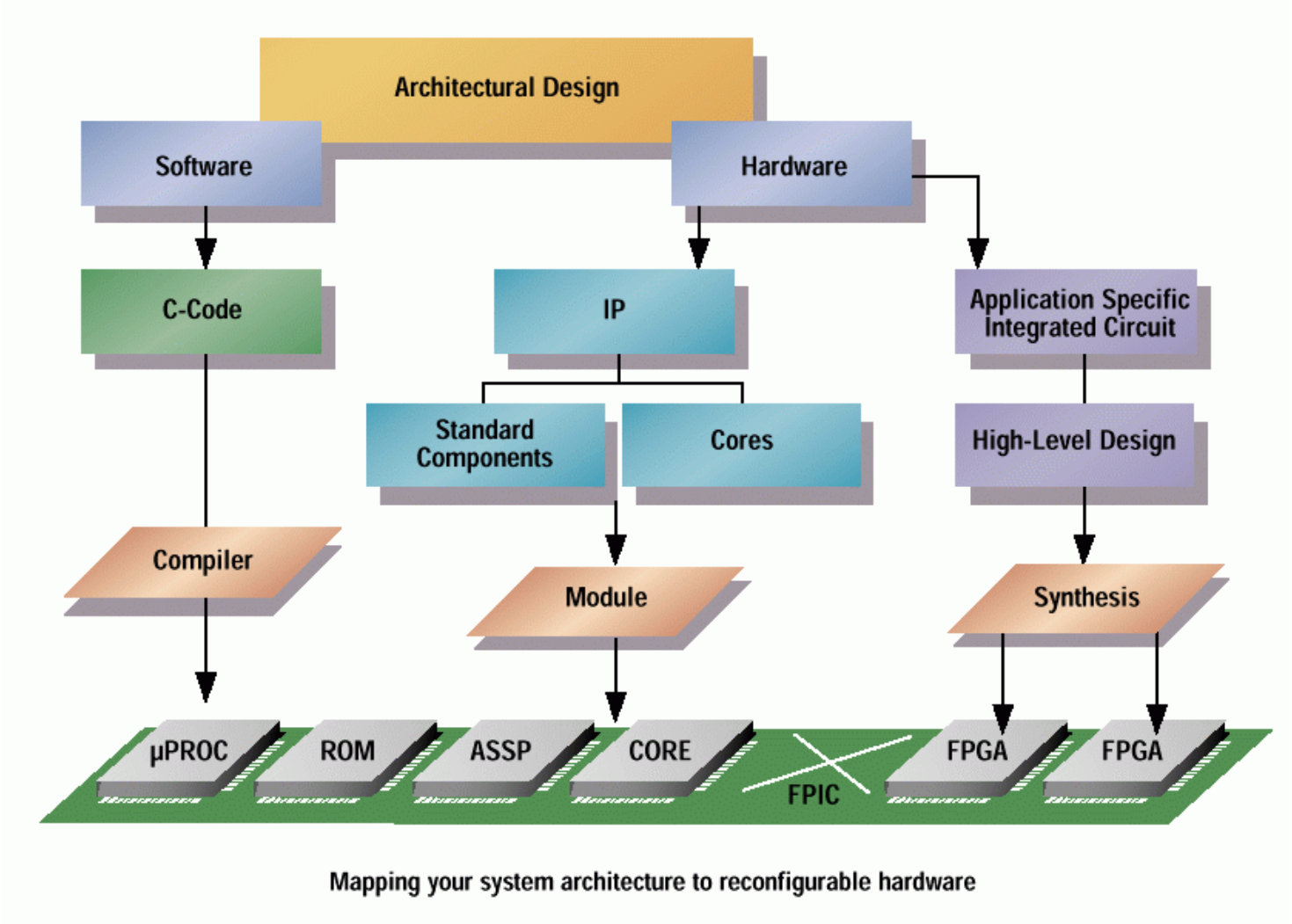
- rapid prototyping uses a _____ hardware platform (remember: emulation uses a homogenous platform)

- rapid prototyping systems offer
  - modules
    - processors
    - special chips (ASICs)
    - FPGAs
    - memory
  - flexible interconnection structure
    - FPGAs
    - FPICS (field-programmable interconnects)

Example – Aptix Exporer



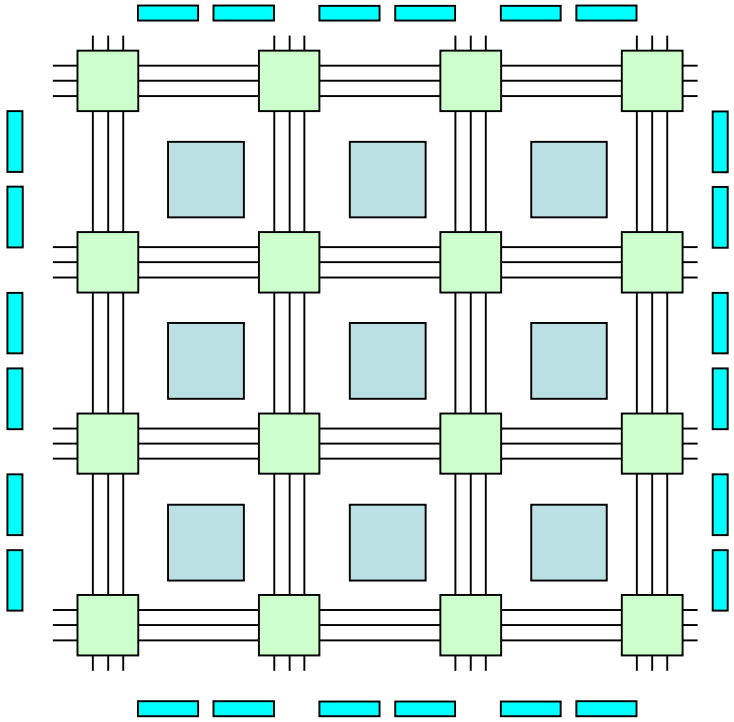
Design Flow – Aptix Explorer



Mapping your system architecture to reconfigurable hardware

Example – Digilent Nexys 3 (I)

- Digilent Nexys 3 board with **Xilinx Spartan6 XC6LX16-CS324**
  - 2278 logic blocks
  - 576 kbit block RAM
  - 32 DSP slices
  - 500MHz+ clock speeds (DCM)
- peripheries
  - Buttons, Switches, …
  - LEDs, Seven Segment Display
  - RS232, USB, Ethernet, VGA, …
- used in practical course



Example – Digilent Nexys 3 (II)