Chapter C4
A64 Instruction Set Encoding

This chapter describes the encoding of the A64 instruction set. It contains the following section:

- *A64 instruction set encoding* on page C4-380.

In this chapter:

- In the decode tables, an entry of - for a field value means the value of the field does not affect the decoding.
- In the decode diagrams, a shaded field indicates that the bits in that field are not used in that level of decode.

C4.1 A64 instruction set encoding

The A64 instruction encoding is:

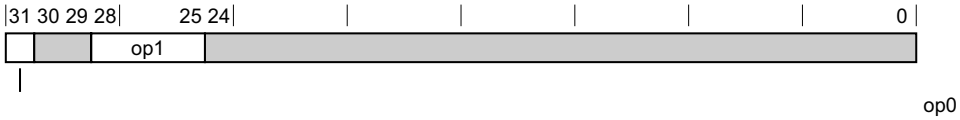


Table C4-1 Main encoding table for the A64 instruction set

Decode fields		Decode group or instruction page
op0	**op1**	
0	0000	*Reserved* on page C4-380
1	0000	*SME encodings* on page C4-381
-	0001	Unallocated.
-	0010	*SVE encodings* on page C4-391
-	0011	Unallocated.
-	100x	*Data Processing -- Immediate* on page C4-523
-	101x	*Branches, Exception Generating and System instructions* on page C4-527
-	x1x0	*Loads and Stores* on page C4-537
-	x101	*Data Processing -- Register* on page C4-576
-	x111	*Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587

C4.1.1 Reserved

This section describes the encoding of the Reserved group. The encodings in this section are decoded from *A64 instruction set encoding*.

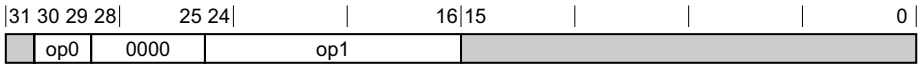


Table C4-2 Encoding table for the Reserved group

Decode fields		Decode group or instruction page
op0	**op1**	
00	000000000	UDF
-	!= 000000000	Unallocated.
!= 00	-	Unallocated.

C4.1.2 SME encodings

This section describes the encoding of the SME encodings group. The encodings in this section are decoded from *A64 instruction set encoding* on page C4-380.

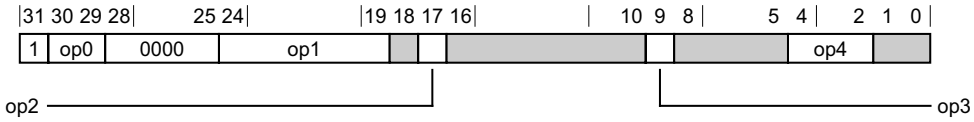


Table C4-3 Encoding table for the SME encodings group

Decode fields					Decode group or instruction page
op0	op1	op2	op3	op4	
0x	x0xxx	-	-	-	Unallocated.
0x	x10xxx	-	-	xx0	*SME Outer Product - 32 bit* on page C4-381
0x	x10xxx	-	-	xx1	Unallocated.
0x	x11xxx	-	-	x0x	*SME Outer Product - 64 bit* on page C4-384
0x	x11xxx	-	-	x1x	Unallocated.
10	0xx000	0	-	0xx	*SME Move into Array* on page C4-385
10	0xx000	0	-	1xx	Unallocated.
10	0xx000	1	0	-	*SME Move from Array* on page C4-386
10	0xx000	1	1	-	Unallocated.
10	0xx001	-	-	-	*SME Misc* on page C4-387
10	0xx010	-	-	x0x	*SME Add Vector to Array* on page C4-388
10	0xx010	-	-	x1x	Unallocated.
10	0xx011	-	-	-	Unallocated.
10	0xx1xx	-	-	-	Unallocated.
10	1xxxxx	-	-	-	Unallocated.
11	-	-	-	-	*SME Memory* on page C4-389

C4.1.3 SME Outer Product - 32 bit

This section describes the encoding of the SME Outer Product - 32 bit group. The encodings in this section are decoded from *SME encodings*.

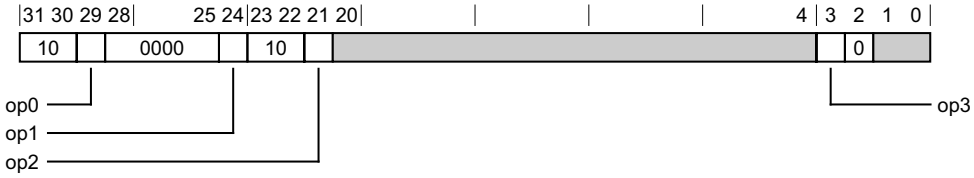
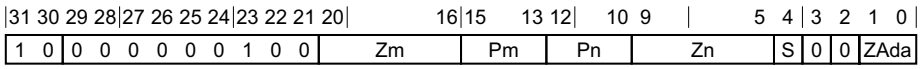


Table C4-4 Encoding table for the SME Outer Product - 32 bit group

Decode fields				Decode group or instruction page
op0	op1	op2	op3	
0	0	0	0	*SME FP32 outer product*
0	0	0	1	Unallocated.
0	0	1	-	Unallocated.
0	1	0	0	*SME BF16 outer product*
0	1	1	0	*SME FP16 outer product* on page C4-383
0	1	-	1	Unallocated.
1	-	-	0	*SME Int8 outer product* on page C4-383
1	-	-	1	Unallocated.

SME FP32 outer product

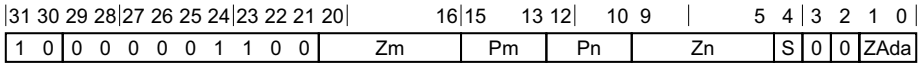
This section describes the encoding of the SME FP32 outer product instruction class. The encodings in this section are decoded from *SME Outer Product - 32 bit* on page C4-381.



Decode fields	Instruction page	Feature
S		
0	FMOPA (non-widening)	FEAT_SME
1	FMOPS (non-widening)	FEAT_SME

SME BF16 outer product

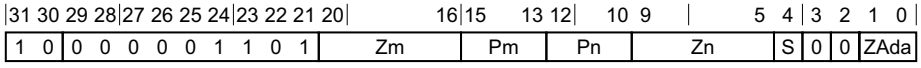
This section describes the encoding of the SME BF16 outer product instruction class. The encodings in this section are decoded from *SME Outer Product - 32 bit* on page C4-381.



Decode fields	Instruction page	Feature
S		
0	BFMOPA	FEAT_SME
1	BFMOPS	FEAT_SME

SME FP16 outer product

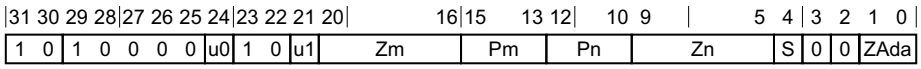
This section describes the encoding of the SME FP16 outer product instruction class. The encodings in this section are decoded from *SME Outer Product - 32 bit* on page C4-381.



Decode fields	Instruction page	Feature
S		
0	FMOPA (widening)	FEAT_SME
1	FMOPS (widening)	FEAT_SME

SME Int8 outer product

This section describes the encoding of the SME Int8 outer product instruction class. The encodings in this section are decoded from *SME Outer Product - 32 bit* on page C4-381.



Decode fields			Instruction page	Feature
u0	u1	S		
0	0	0	SMOPA	FEAT_SME
0	0	1	SMOPS	FEAT_SME
0	1	0	SUMOPA	FEAT_SME
0	1	1	SUMOPS	FEAT_SME
1	0	0	USMOPA	FEAT_SME

Decode fields			Instruction page	Feature
u0	u1	S		
1	0	1	USMOPS	FEAT_SME
1	1	0	UMOPA	FEAT_SME
1	1	1	UMOPS	FEAT_SME

C4.1.4 SME Outer Product - 64 bit

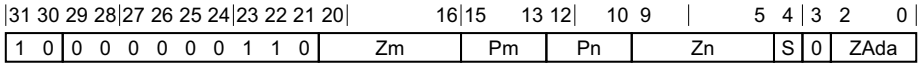
This section describes the encoding of the SME Outer Product - 64 bit group. The encodings in this section are decoded from *SME encodings* on page C4-381.

Table C4-5 Encoding table for the SME Outer Product - 64 bit group

Decode fields			Decode group or instruction page
op0	op1	op2	
0	0	0	*SME FP64 outer product* on page C4-384
0	0	1	Unallocated.
0	1	-	Unallocated.
1	-	-	*SME Int16 outer product* on page C4-385

SME FP64 outer product

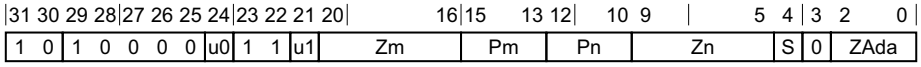
This section describes the encoding of the SME FP64 outer product instruction class. The encodings in this section are decoded from *SME Outer Product - 64 bit*.



Decode fields	Instruction page	Feature
S		
0	FMOPA (non-widening)	FEAT_SME_F64F64
1	FMOPS (non-widening)	FEAT_SME_F64F64

SME Int16 outer product

This section describes the encoding of the SME Int16 outer product instruction class. The encodings in this section are decoded from *SME Outer Product - 64 bit* on page C4-384.



Decode fields			Instruction page	Feature
u0	u1	S		
0	0	0	SMOPA	FEAT_SME_I16I64
0	0	1	SMOPS	FEAT_SME_I16I64
0	1	0	SUMOPA	FEAT_SME_I16I64
0	1	1	SUMOPS	FEAT_SME_I16I64
1	0	0	USMOPA	FEAT_SME_I16I64
1	0	1	USMOPS	FEAT_SME_I16I64
1	1	0	UMOPA	FEAT_SME_I16I64
1	1	1	UMOPS	FEAT_SME_I16I64

C4.1.5 SME Move into Array

This section describes the encoding of the SME Move into Array group. The encodings in this section are decoded from *SME encodings* on page C4-381.

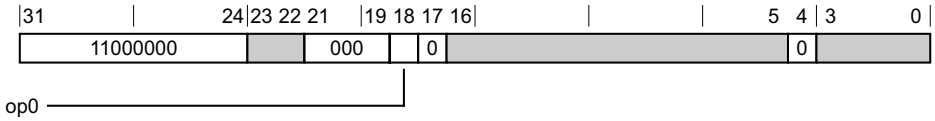
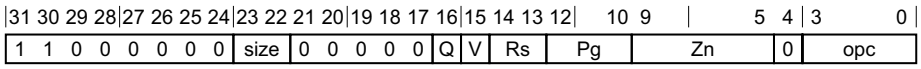


Table C4-6 Encoding table for the SME Move into Array group

Decode fields	Decode group or instruction page
op0	
0	*SME move vector to array* on page C4-386
1	Unallocated.

SME move vector to array

This section describes the encoding of the SME move vector to array instruction class. The encodings in this section are decoded from *SME Move into Array* on page C4-385.



Decode fields		Instruction page	Feature
size	Q		
0x	1	Unallocated.	-
00	0	MOVA (vector to tile) - Encoding	FEAT_SME
01	0	MOVA (vector to tile) - Encoding	FEAT_SME
10	0	MOVA (vector to tile) - Encoding	FEAT_SME
10	1	Unallocated.	-
11	0	MOVA (vector to tile) - Encoding	FEAT_SME
11	1	MOVA (vector to tile) - Encoding	FEAT_SME

C4.1.6 SME Move from Array

This section describes the encoding of the SME Move from Array group. The encodings in this section are decoded from *SME encodings* on page C4-381.

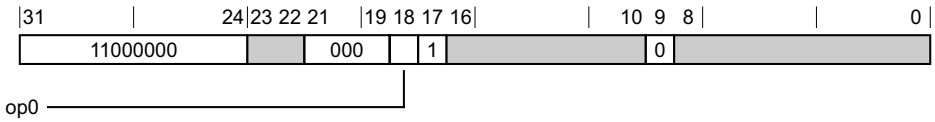
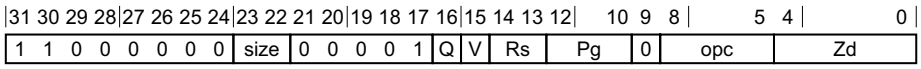


Table C4-7 Encoding table for the SME Move from Array group

Decode fields	Decode group or instruction page
op0	
0	*SME move array to vector* on page C4-387
1	Unallocated.

SME move array to vector

This section describes the encoding of the SME move array to vector instruction class. The encodings in this section are decoded from *SME Move from Array* on page C4-386.



Decode fields		Instruction page	Feature
size	Q		
0x	1	Unallocated.	-
00	0	MOVA (tile to vector) - Encoding	FEAT_SME
01	0	MOVA (tile to vector) - Encoding	FEAT_SME
10	0	MOVA (tile to vector) - Encoding	FEAT_SME
10	1	Unallocated.	-
11	0	MOVA (tile to vector) - Encoding	FEAT_SME
11	1	MOVA (tile to vector) - Encoding	FEAT_SME

C4.1.7 SME Misc

This section describes the encoding of the SME Misc group. The encodings in this section are decoded from *SME encodings* on page C4-381.

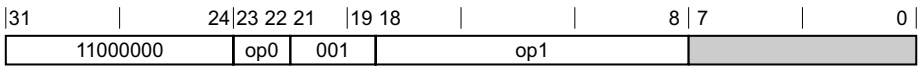


Table C4-8 Encoding table for the SME Misc group

Decode fields		Decode group or instruction page	Feature
op0	op1		
00	00000000000	ZERO	FEAT_SME
00	!= 00000000000	Unallocated.	-
!= 00	-	Unallocated.	-

C4.1.8 SME Add Vector to Array

This section describes the encoding of the SME Add Vector to Array group. The encodings in this section are decoded from *SME encodings* on page C4-381.

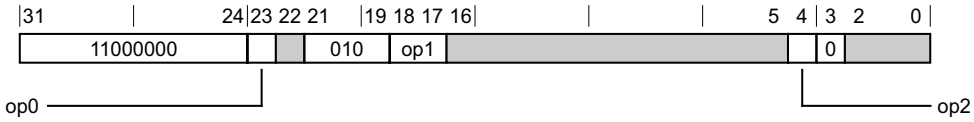
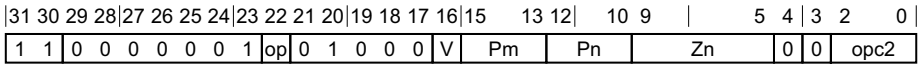


Table C4-9 Encoding table for the SME Add Vector to Array group

Decode fields			Decode group or instruction page
op0	op1	op2	
0	-	-	Unallocated.
1	00	0	*SME add vector to array* on page C4-388
1	00	1	Unallocated.
1	!= 00	-	Unallocated.

SME add vector to array

This section describes the encoding of the SME add vector to array instruction class. The encodings in this section are decoded from *SME Add Vector to Array*.



Decode fields			Instruction page	Feature
op	V	opc2		
0	-	1xx	Unallocated.	-
0	0	0xx	ADDHA - Encoding	FEAT_SME
0	1	0xx	ADDVA - Encoding	FEAT_SME
1	0	-	ADDHA - Encoding	FEAT_SME_I16I64
1	1	-	ADDVA - Encoding	FEAT_SME_I16I64

C4.1.9 SME Memory

This section describes the encoding of the SME Memory group. The encodings in this section are decoded from *SME encodings* on page C4-381.

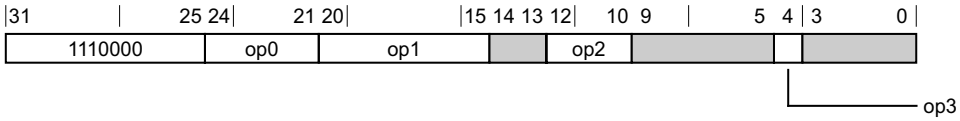
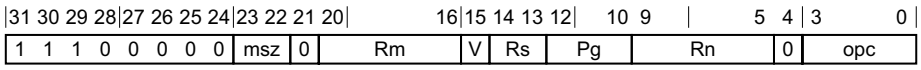


Table C4-10 Encoding table for the SME Memory group

Decode fields				Decode group or instruction page	Feature
op0	op1	op2	op3		
0xx0	-	-	0	*SME load array vector (elements)* on page C4-389	-
0xx1	-	-	0	*SME store array vector (elements)* on page C4-390	-
0xxx	-	-	1	Unallocated.	-
100x	000000	000	0	*SME save and restore array* on page C4-390	-
100x	000000	000	1	Unallocated.	-
100x	000000	!= 000	-	Unallocated.	-
100x	!= 000000	-	-	Unallocated.	-
101x	-	-	-	Unallocated.	-
110x	-	-	-	Unallocated.	-
1110	-	-	0	LD1Q	FEAT_SME
1111	-	-	0	ST1Q	FEAT_SME
111x	-	-	1	Unallocated.	-

SME load array vector (elements)

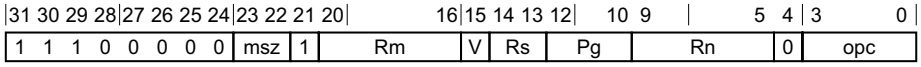
This section describes the encoding of the SME load array vector (elements) instruction class. The encodings in this section are decoded from *SME Memory*.



Decode fields	Instruction page	Feature
msz		
00	LD1B	FEAT_SME
01	LD1H	FEAT_SME
10	LD1W	FEAT_SME
11	LD1D	FEAT_SME

SME store array vector (elements)

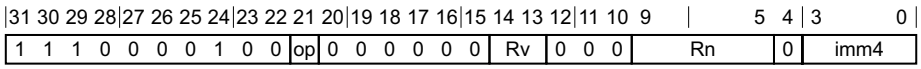
This section describes the encoding of the SME store array vector (elements) instruction class. The encodings in this section are decoded from *SME Memory* on page C4-389.



Decode fields	Instruction page	Feature
msz		
00	ST1B	FEAT_SME
01	ST1H	FEAT_SME
10	ST1W	FEAT_SME
11	ST1D	FEAT_SME

SME save and restore array

This section describes the encoding of the SME save and restore array instruction class. The encodings in this section are decoded from *SME Memory* on page C4-389.



Decode fields	Instruction page	Feature
op		
0	LDR	FEAT_SME
1	STR	FEAT_SME

C4.1.10 SVE encodings

This section describes the encoding of the SVE encodings group. The encodings in this section are decoded from *A64 instruction set encoding* on page C4-380.

Table C4-11 Encoding table for the SVE encodings group

Decode fields					Decode group or instruction page
op0	op1	op2	op3	op4	
000	0x	0xxxx	x1xxxx	-	*SVE Integer Multiply-Add - Predicated* on page C4-404
000	0x	0xxxx	000xxx	-	*SVE Integer Binary Arithmetic - Predicated* on page C4-405
000	0x	0xxxx	001xxx	-	*SVE Integer Reduction* on page C4-408
000	0x	0xxxx	100xxx	-	*SVE Bitwise Shift - Predicated* on page C4-410
000	0x	0xxxx	101xxx	-	*SVE Integer Unary Arithmetic - Predicated* on page C4-412
000	0x	1xxxx	000xxx	-	*SVE integer add/subtract vectors (unpredicated)* on page C4-394
000	0x	1xxxx	001xxx	-	*SVE Bitwise Logical - Unpredicated* on page C4-414
000	0x	1xxxx	0100xx	-	*SVE Index Generation* on page C4-415
000	0x	1xxxx	0101xx	-	*SVE Stack Allocation* on page C4-416
000	0x	1xxxx	011xxx	-	*SVE2 Integer Multiply - Unpredicated* on page C4-418
000	0x	1xxxx	100xxx	-	*SVE Bitwise Shift - Unpredicated* on page C4-420
000	0x	1xxxx	1010xx	-	*SVE address generation* on page C4-395
000	0x	1xxxx	1011xx	-	*SVE Integer Misc - Unpredicated* on page C4-421
000	0x	1xxxx	11xxxx	-	*SVE Element Count* on page C4-423
000	1x	00xxx	-	-	*SVE Bitwise Immediate* on page C4-426
000	1x	01xxx	-	-	*SVE Integer Wide Immediate - Predicated* on page C4-427
000	1x	1xxxx	001000	-	DUP (indexed)
000	1x	1xxxx	001001	-	Unallocated.
000	1x	1xxxx	00101x	-	*SVE table lookup (three sources)* on page C4-395
000	1x	1xxxx	0011x1	-	Unallocated.
000	1x	1xxxx	001100	-	TBL - Encoding
000	1x	1xxxx	001110	-	*SVE Permute Vector - Unpredicated* on page C4-428
000	1x	1xxxx	010xxx	-	*SVE Permute Predicate* on page C4-429
000	1x	1xxxx	011xxx	-	*SVE permute vector elements* on page C4-396
000	1x	1xxxx	10xxxx	-	*SVE Permute Vector - Predicated* on page C4-431

Table C4-11 Encoding table for the SVE encodings group (continued)

Decode fields					Decode group or instruction page
op0	op1	op2	op3	op4	
000	1x	1xxxx	11xxxx	-	SEL (vectors)
000	10	1xxxx	000xxx	-	*SVE Permute Vector - Extract* on page C4-435
000	11	1xxxx	000xxx	-	*SVE Permute Vector - Segments* on page C4-435
001	0x	0xxxx	-	-	*SVE Integer Compare - Vectors* on page C4-436
001	0x	1xxxx	-	-	*SVE integer compare with unsigned immediate* on page C4-396
001	1x	0xxxx	x0xxxx	-	*SVE integer compare with signed immediate* on page C4-397
001	1x	00xxx	01xxxx	-	*SVE predicate logical operations* on page C4-397
001	1x	00xxx	11xxxx	-	*SVE Propagate Break* on page C4-438
001	1x	01xxx	01xxxx	-	*SVE Partition Break* on page C4-438
001	1x	01xxx	11xxxx	-	*SVE Predicate Misc* on page C4-440
001	1x	1xxxx	00xxxx	-	*SVE Integer Compare - Scalars* on page C4-444
001	1x	1xxxx	01xxxx	0	*SVE broadcast predicate element* on page C4-398
001	1x	1xxxx	01xxxx	1	Unallocated.
001	1x	1xxxx	11xxxx	-	*SVE Integer Wide Immediate - Unpredicated* on page C4-445
001	1x	100xx	10xxxx	-	*SVE Predicate Count* on page C4-448
001	1x	101xx	1000xx	-	*SVE Inc/Dec by Predicate Count* on page C4-449
001	1x	101xx	1001xx	-	*SVE Write FFR* on page C4-452
001	1x	101xx	101xxx	-	Unallocated.
001	1x	11xxx	10xxxx	-	Unallocated.
010	0x	0xxxx	0xxxxx	-	*SVE Integer Multiply-Add - Unpredicated* on page C4-453
010	0x	0xxxx	10xxxx	-	*SVE2 Integer - Predicated* on page C4-456
010	0x	0xxxx	11000x	-	*SVE clamp* on page C4-398
010	0x	0xxxx	11001x	-	Unallocated.
010	0x	0xxxx	1101xx	-	Unallocated.
010	0x	0xxxx	111xxx	-	Unallocated.
010	0x	1xxxx	-	-	*SVE Multiply - Indexed* on page C4-460
010	1x	0xxxx	0xxxxx	-	*SVE2 Widening Integer Arithmetic* on page C4-468
010	1x	0xxxx	10xxxx	-	*SVE Misc* on page C4-470
010	1x	0xxxx	11xxxx	-	*SVE2 Accumulate* on page C4-472
010	1x	1xxxx	0xxxxx	-	*SVE2 Narrowing* on page C4-475
010	1x	1xxxx	100xxx	-	*SVE2 character match* on page C4-399

Table C4-11 Encoding table for the SVE encodings group (continued)

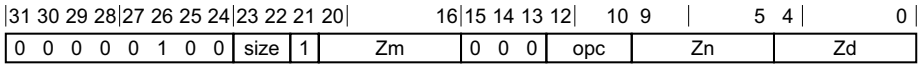
Decode fields					Decode group or instruction page
op0	op1	op2	op3	op4	
010	1x	1xxxx	101xxx	-	*SVE2 Histogram Computation - Segment* on page C4-477
010	1x	1xxxx	110xxx	-	HISTCNT
010	1x	1xxxx	111xxx	-	*SVE2 Crypto Extensions* on page C4-478
011	0x	0xxxx	0xxxxx	-	FCMLA (vectors)
011	0x	00x1x	1xxxxx	-	Unallocated.
011	0x	00000	100xxx	-	FCADD
011	0x	00000	101xxx	-	Unallocated.
011	0x	00000	11xxxx	-	Unallocated.
011	0x	00001	1xxxxx	-	Unallocated.
011	0x	0010x	100xxx	-	Unallocated.
011	0x	0010x	101xxx	-	*SVE floating-point convert precision odd elements* on page C4-399
011	0x	0010x	11xxxx	-	Unallocated.
011	0x	010xx	100xxx	-	*SVE2 floating-point pairwise operations* on page C4-400
011	0x	010xx	101xxx	-	Unallocated.
011	0x	010xx	11xxxx	-	Unallocated.
011	0x	011xx	1xxxxx	-	Unallocated.
011	0x	1xxxx	x0x01x	-	Unallocated.
011	0x	1xxxx	00000x	-	*SVE floating-point multiply-add (indexed)* on page C4-400
011	0x	1xxxx	0001xx	-	*SVE floating-point complex multiply-add (indexed)* on page C4-401
011	0x	1xxxx	001000	-	*SVE floating-point multiply (indexed)* on page C4-401
011	0x	1xxxx	001001	-	Unallocated.
011	0x	1xxxx	0011xx	-	Unallocated.
011	0x	1xxxx	01x0xx	-	*SVE Floating Point Widening Multiply-Add - Indexed* on page C4-480
011	0x	1xxxx	01x1xx	-	Unallocated.
011	0x	1xxxx	10x00x	-	*SVE Floating Point Widening Multiply-Add* on page C4-481
011	0x	1xxxx	10x1xx	-	Unallocated.
011	0x	1xxxx	110xxx	-	Unallocated.
011	0x	1xxxx	111000	-	Unallocated.
011	0x	1xxxx	111001	-	*SVE floating point matrix multiply accumulate* on page C4-401
011	0x	1xxxx	11101x	-	Unallocated.
011	0x	1xxxx	1111xx	-	Unallocated.

Table C4-11 Encoding table for the SVE encodings group (continued)

Decode fields					Decode group or instruction page
op0	op1	op2	op3	op4	
011	1x	0xxx	x1xxxx	-	*SVE floating-point compare vectors* on page C4-402
011	1x	0xxx	000xxx	-	*SVE floating-point arithmetic (unpredicated)* on page C4-402
011	1x	0xxx	100xxx	-	*SVE Floating Point Arithmetic - Predicated* on page C4-483
011	1x	0xxx	101xxx	-	*SVE Floating Point Unary Operations - Predicated* on page C4-485
011	1x	000xx	001xxx	-	*SVE floating-point recursive reduction* on page C4-403
011	1x	001xx	0010xx	-	Unallocated.
011	1x	001xx	0011xx	-	*SVE Floating Point Unary Operations - Unpredicated* on page C4-489
011	1x	010xx	001xxx	-	*SVE Floating Point Compare - with Zero* on page C4-489
011	1x	011xx	001xxx	-	*SVE Floating Point Accumulating Reduction* on page C4-490
011	1x	1xxxx	-	-	*SVE Floating Point Multiply-Add* on page C4-491
100	-	-	-	-	*SVE Memory - 32-bit Gather and Unsized Contiguous* on page C4-492
101	-	-	-	-	*SVE Memory - Contiguous Load* on page C4-499
110	-	-	-	-	*SVE Memory - 64-bit Gather* on page C4-506
111	-	-	0x0xxx	-	*SVE Memory - Contiguous Store and Unsized Contiguous* on page C4-512
111	-	-	0x1xxx	-	*SVE Memory - Non-temporal and Multi-register Store* on page C4-513
111	-	-	1x0xxx	-	*SVE Memory - Scatter with Optional Sign Extend* on page C4-516
111	-	-	101xxx	-	*SVE Memory - Scatter* on page C4-518
111	-	-	111xxx	-	*SVE Memory - Contiguous Store with Immediate Offset* on page C4-521

SVE integer add/subtract vectors (unpredicated)

This section describes the encoding of the SVE integer add/subtract vectors (unpredicated) instruction class. The encodings in this section are decoded from *SVE encodings* on page C4-391.

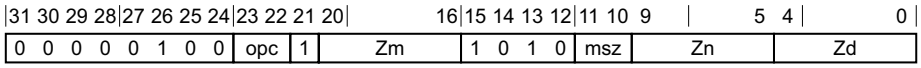


Decode fields	Instruction page
opc	
000	ADD (vectors, unpredicated)
001	SUB (vectors, unpredicated)
01x	Unallocated.
100	SQADD (vectors, unpredicated)

Decode fields	Instruction page
opc	
101	UQADD (vectors, unpredicated)
110	SQSUB (vectors, unpredicated)
111	UQSUB (vectors, unpredicated)

SVE address generation

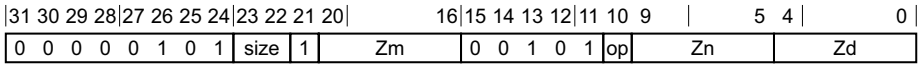
This section describes the encoding of the SVE address generation instruction class. The encodings in this section are decoded from *SVE encodings* on page C4-391.



Decode fields	Instruction page
opc	
00	ADR - Encoding
01	ADR - Encoding
1x	ADR - Encoding

SVE table lookup (three sources)

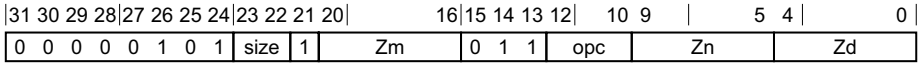
This section describes the encoding of the SVE table lookup (three sources) instruction class. The encodings in this section are decoded from *SVE encodings* on page C4-391.



Decode fields	Instruction page
op	
0	TBL
1	TBX

SVE permute vector elements

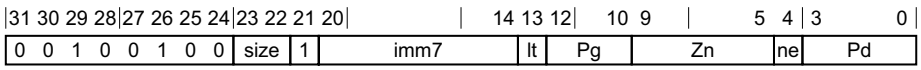
This section describes the encoding of the SVE permute vector elements instruction class. The encodings in this section are decoded from *SVE encodings* on page C4-391.



Decode fields	Instruction page
opc	
000	ZIP1, ZIP2 (vectors) - Encoding
001	ZIP1, ZIP2 (vectors) - Encoding
010	UZP1, UZP2 (vectors) - Encoding
011	UZP1, UZP2 (vectors) - Encoding
100	TRN1, TRN2 (vectors) - Encoding
101	TRN1, TRN2 (vectors) - Encoding
11x	Unallocated.

SVE integer compare with unsigned immediate

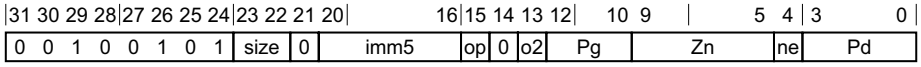
This section describes the encoding of the SVE integer compare with unsigned immediate instruction class. The encodings in this section are decoded from *SVE encodings* on page C4-391.



Decode fields		Instruction page
lt	ne	
0	0	CMP<cc> (immediate) - Encoding
0	1	CMP<cc> (immediate) - Encoding
1	0	CMP<cc> (immediate) - Encoding
1	1	CMP<cc> (immediate) - Encoding

SVE integer compare with signed immediate

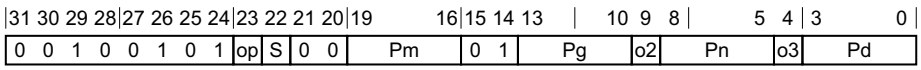
This section describes the encoding of the SVE integer compare with signed immediate instruction class. The encodings in this section are decoded from *SVE encodings* on page C4-391.



Decode fields			Instruction page
op	o2	ne	
0	0	0	CMP<cc> (immediate) - Encoding
0	0	1	CMP<cc> (immediate) - Encoding
0	1	0	CMP<cc> (immediate) - Encoding
0	1	1	CMP<cc> (immediate) - Encoding
1	0	0	CMP<cc> (immediate) - Encoding
1	0	1	CMP<cc> (immediate) - Encoding
1	1	-	Unallocated.

SVE predicate logical operations

This section describes the encoding of the SVE predicate logical operations instruction class. The encodings in this section are decoded from *SVE encodings* on page C4-391.

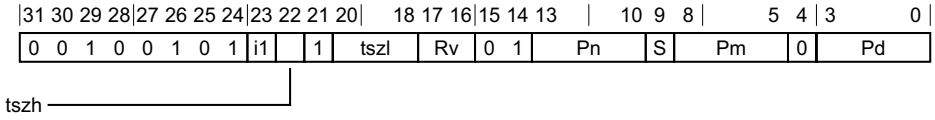


Decode fields				Instruction page
op	S	o2	o3	
0	0	0	0	AND (predicates)
0	0	0	1	BIC (predicates)
0	0	1	0	EOR (predicates)
0	0	1	1	SEL (predicates)
0	1	0	0	ANDS
0	1	0	1	BICS
0	1	1	0	EORS
0	1	1	1	Unallocated.
1	0	0	0	ORR (predicates)
1	0	0	1	ORN (predicates)

Decode fields				Instruction page
op	S	o2	o3	
1	0	1	0	NOR
1	0	1	1	NAND
1	1	0	0	ORRS
1	1	0	1	ORNS
1	1	1	0	NORS
1	1	1	1	NANDS

SVE broadcast predicate element

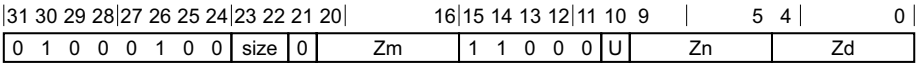
This section describes the encoding of the SVE broadcast predicate element instruction class. The encodings in this section are decoded from *SVE encodings* on page C4-391.



Decode fields	Instruction page	Feature
S		
0	PSEL	FEAT_SME
1	Unallocated.	-

SVE clamp

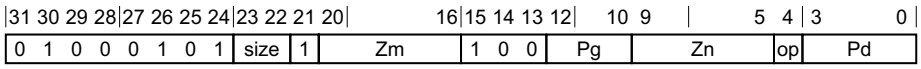
This section describes the encoding of the SVE clamp instruction class. The encodings in this section are decoded from *SVE encodings* on page C4-391.



Decode fields	Instruction page	Feature
U		
0	SCLAMP	FEAT_SME
1	UCLAMP	FEAT_SME

SVE2 character match

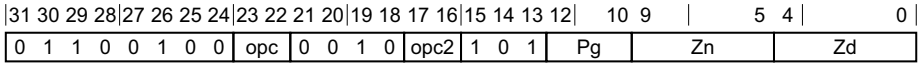
This section describes the encoding of the SVE2 character match instruction class. The encodings in this section are decoded from *SVE encodings* on page C4-391.



Decode fields	Instruction page
op	
0	MATCH
1	NMATCH

SVE floating-point convert precision odd elements

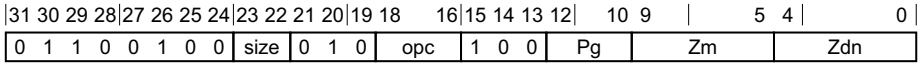
This section describes the encoding of the SVE floating-point convert precision odd elements instruction class. The encodings in this section are decoded from *SVE encodings* on page C4-391.



Decode fields		Instruction page	Feature
opc	opc2		
x0	11	Unallocated.	-
00	0x	Unallocated.	-
00	10	FCVTXNT	-
01	-	Unallocated.	-
10	00	FCVTNT - Encoding	-
10	01	FCVTLT - Encoding	-
10	10	BFCVTNT	FEAT_BF16
11	0x	Unallocated.	-
11	10	FCVTNT - Encoding	-
11	11	FCVTLT - Encoding	-

SVE2 floating-point pairwise operations

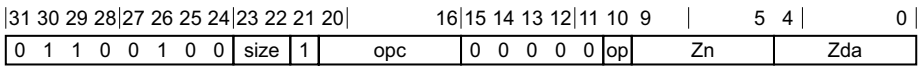
This section describes the encoding of the SVE2 floating-point pairwise operations instruction class. The encodings in this section are decoded from *SVE encodings* on page C4-391.



Decode fields	Instruction page
opc	
000	FADDP
001	Unallocated.
01x	Unallocated.
100	FMAXNMP
101	FMINNMP
110	FMAXP
111	FMINP

SVE floating-point multiply-add (indexed)

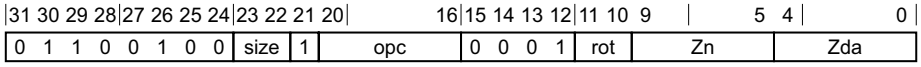
This section describes the encoding of the SVE floating-point multiply-add (indexed) instruction class. The encodings in this section are decoded from *SVE encodings* on page C4-391.



Decode fields		Instruction page
size	op	
0x	0	FMLA (indexed) - Encoding
0x	1	FMLS (indexed) - Encoding
10	0	FMLA (indexed) - Encoding
10	1	FMLS (indexed) - Encoding
11	0	FMLA (indexed) - Encoding
11	1	FMLS (indexed) - Encoding

SVE floating-point complex multiply-add (indexed)

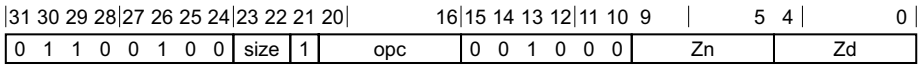
This section describes the encoding of the SVE floating-point complex multiply-add (indexed) instruction class. The encodings in this section are decoded from *SVE encodings* on page C4-391.



Decode fields	Instruction page
size	
0x	Unallocated.
10	FCMLA (indexed) - Encoding
11	FCMLA (indexed) - Encoding

SVE floating-point multiply (indexed)

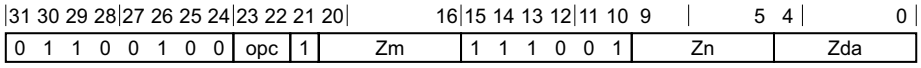
This section describes the encoding of the SVE floating-point multiply (indexed) instruction class. The encodings in this section are decoded from *SVE encodings* on page C4-391.



Decode fields	Instruction page
size	
0x	FMUL (indexed) - Encoding
10	FMUL (indexed) - Encoding
11	FMUL (indexed) - Encoding

SVE floating point matrix multiply accumulate

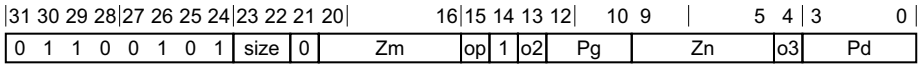
This section describes the encoding of the SVE floating point matrix multiply accumulate instruction class. The encodings in this section are decoded from *SVE encodings* on page C4-391.



Decode fields	Instruction page	Feature
opc		
00	Unallocated.	-
01	BFMMLA	FEAT_BF16
10	FMMLA - Encoding	FEAT_F32MM
11	FMMLA - Encoding	FEAT_F64MM

SVE floating-point compare vectors

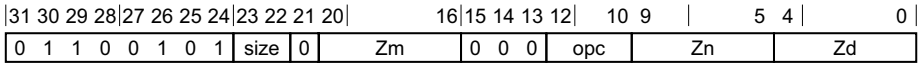
This section describes the encoding of the SVE floating-point compare vectors instruction class. The encodings in this section are decoded from *SVE encodings* on page C4-391.



Decode fields			Instruction page
op	o2	o3	
0	0	0	FCM<cc> (vectors) - Encoding
0	0	1	FCM<cc> (vectors) - Encoding
0	1	0	FCM<cc> (vectors) - Encoding
0	1	1	FCM<cc> (vectors) - Encoding
1	0	0	FCM<cc> (vectors) - Encoding
1	0	1	FAC<cc> - Encoding
1	1	0	Unallocated.
1	1	1	FAC<cc> - Encoding

SVE floating-point arithmetic (unpredicated)

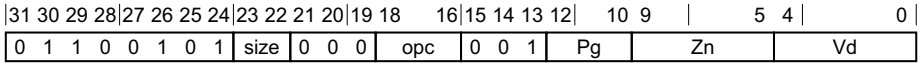
This section describes the encoding of the SVE floating-point arithmetic (unpredicated) instruction class. The encodings in this section are decoded from *SVE encodings* on page C4-391.



Decode fields	Instruction page
opc	
000	FADD (vectors, unpredicated)
001	FSUB (vectors, unpredicated)
010	FMUL (vectors, unpredicated)
011	FTSMUL
10x	Unallocated.
110	FRECPS
111	FRSQRTS

SVE floating-point recursive reduction

This section describes the encoding of the SVE floating-point recursive reduction instruction class. The encodings in this section are decoded from *SVE encodings* on page C4-391.



Decode fields	Instruction page
opc	
000	FADDV
001	Unallocated.
01x	Unallocated.
100	FMAXNMV
101	FMINNMV
110	FMAXV
111	FMINV

C4.1.11 SVE Integer Multiply-Add - Predicated

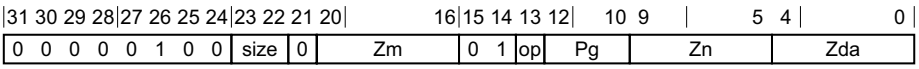
This section describes the encoding of the SVE Integer Multiply-Add - Predicated group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

Table C4-12 Encoding table for the SVE Integer Multiply-Add - Predicated group

Decode fields	Decode group or instruction page
op0	
0	*SVE integer multiply-accumulate writing addend (predicated)* on page C4-404
1	*SVE integer multiply-add writing multiplicand (predicated)* on page C4-404

SVE integer multiply-accumulate writing addend (predicated)

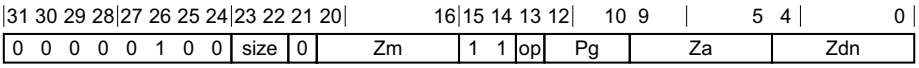
This section describes the encoding of the SVE integer multiply-accumulate writing addend (predicated) instruction class. The encodings in this section are decoded from *SVE Integer Multiply-Add - Predicated*.



Decode fields	Instruction page
op	
0	MLA (vectors)
1	MLS (vectors)

SVE integer multiply-add writing multiplicand (predicated)

This section describes the encoding of the SVE integer multiply-add writing multiplicand (predicated) instruction class. The encodings in this section are decoded from *SVE Integer Multiply-Add - Predicated*.



Decode fields	Instruction page
op	
0	MAD
1	MSB

C4.1.12 SVE Integer Binary Arithmetic - Predicated

This section describes the encoding of the SVE Integer Binary Arithmetic - Predicated group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

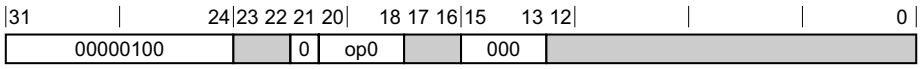
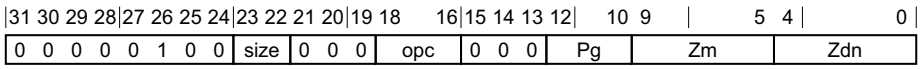


Table C4-13 Encoding table for the SVE Integer Binary Arithmetic - Predicated group

Decode fields op0	Decode group or instruction page
00x	*SVE integer add/subtract vectors (predicated)* on page C4-405
01x	*SVE integer min/max/difference (predicated)* on page C4-406
100	*SVE integer multiply vectors (predicated)* on page C4-406
101	*SVE integer divide vectors (predicated)* on page C4-407
11x	*SVE bitwise logical operations (predicated)* on page C4-407

SVE integer add/subtract vectors (predicated)

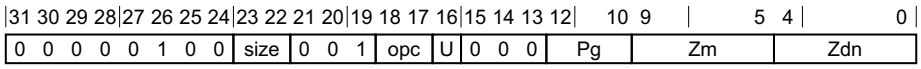
This section describes the encoding of the SVE integer add/subtract vectors (predicated) instruction class. The encodings in this section are decoded from *SVE Integer Binary Arithmetic - Predicated*.



Decode fields opc	Instruction page
000	ADD (vectors, predicated)
001	SUB (vectors, predicated)
010	Unallocated.
011	SUBR (vectors)
1xx	Unallocated.

SVE integer min/max/difference (predicated)

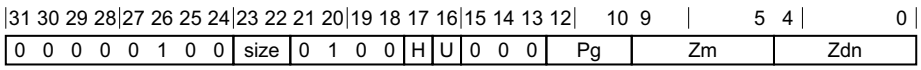
This section describes the encoding of the SVE integer min/max/difference (predicated) instruction class. The encodings in this section are decoded from *SVE Integer Binary Arithmetic - Predicated* on page C4-405.



Decode fields		Instruction page
opc	U	
00	0	SMAX (vectors)
00	1	UMAX (vectors)
01	0	SMIN (vectors)
01	1	UMIN (vectors)
10	0	SABD
10	1	UABD
11	-	Unallocated.

SVE integer multiply vectors (predicated)

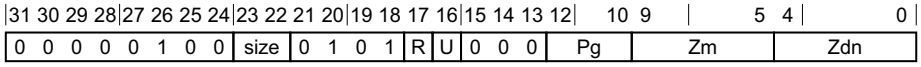
This section describes the encoding of the SVE integer multiply vectors (predicated) instruction class. The encodings in this section are decoded from *SVE Integer Binary Arithmetic - Predicated* on page C4-405.



Decode fields		Instruction page
H	U	
0	0	MUL (vectors, predicated)
0	1	Unallocated.
1	0	SMULH (predicated)
1	1	UMULH (predicated)

SVE integer divide vectors (predicated)

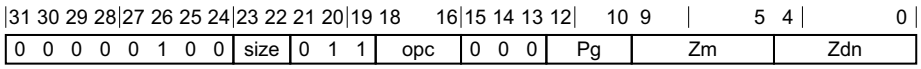
This section describes the encoding of the SVE integer divide vectors (predicated) instruction class. The encodings in this section are decoded from *SVE Integer Binary Arithmetic - Predicated* on page C4-405.



Decode fields		Instruction page
R	U	
0	0	SDIV
0	1	UDIV
1	0	SDIVR
1	1	UDIVR

SVE bitwise logical operations (predicated)

This section describes the encoding of the SVE bitwise logical operations (predicated) instruction class. The encodings in this section are decoded from *SVE Integer Binary Arithmetic - Predicated* on page C4-405.



Decode fields	Instruction page
opc	
000	ORR (vectors, predicated)
001	EOR (vectors, predicated)
010	AND (vectors, predicated)
011	BIC (vectors, predicated)
1xx	Unallocated.

C4.1.13 SVE Integer Reduction

This section describes the encoding of the SVE Integer Reduction group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

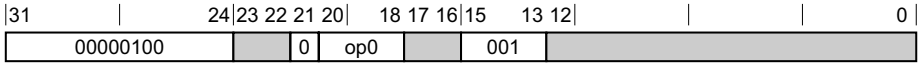
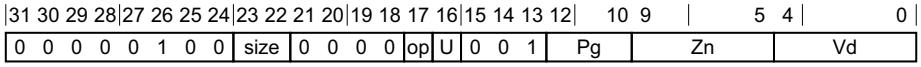


Table C4-14 Encoding table for the SVE Integer Reduction group

Decode fields	Decode group or instruction page
op0	
000	*SVE integer add reduction (predicated)* on page C4-408
010	*SVE integer min/max reduction (predicated)* on page C4-409
0x1	Unallocated.
10x	*SVE constructive prefix (predicated)* on page C4-409
110	*SVE bitwise logical reduction (predicated)* on page C4-409
111	Unallocated.

SVE integer add reduction (predicated)

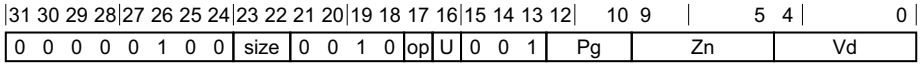
This section describes the encoding of the SVE integer add reduction (predicated) instruction class. The encodings in this section are decoded from *SVE Integer Reduction*.



Decode fields		Instruction page
op	U	
0	0	SADDV
0	1	UADDV
1	-	Unallocated.

SVE integer min/max reduction (predicated)

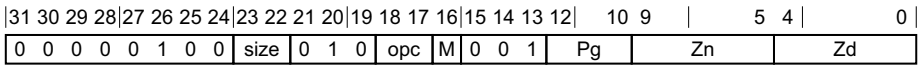
This section describes the encoding of the SVE integer min/max reduction (predicated) instruction class. The encodings in this section are decoded from *SVE Integer Reduction* on page C4-408.



Decode fields		Instruction page
op	U	
0	0	SMAXV
0	1	UMAXV
1	0	SMINV
1	1	UMINV

SVE constructive prefix (predicated)

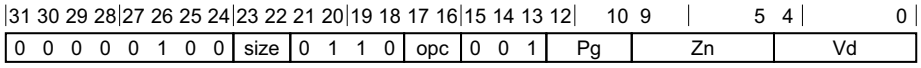
This section describes the encoding of the SVE constructive prefix (predicated) instruction class. The encodings in this section are decoded from *SVE Integer Reduction* on page C4-408.



Decode fields	Instruction page
opc	
00	MOVPRFX (predicated)
01	Unallocated.
1x	Unallocated.

SVE bitwise logical reduction (predicated)

This section describes the encoding of the SVE bitwise logical reduction (predicated) instruction class. The encodings in this section are decoded from *SVE Integer Reduction* on page C4-408.



Decode fields	Instruction page
opc	
00	ORV
01	EORV
10	ANDV
11	Unallocated.

C4.1.14 SVE Bitwise Shift - Predicated

This section describes the encoding of the SVE Bitwise Shift - Predicated group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

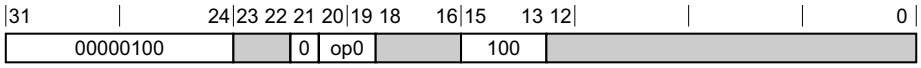
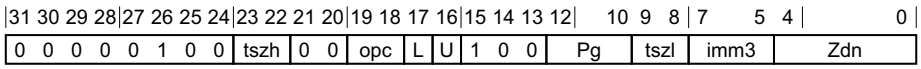


Table C4-15 Encoding table for the SVE Bitwise Shift - Predicated group

Decode fields	Decode group or instruction page
op0	
0x	*SVE bitwise shift by immediate (predicated)* on page C4-410
10	*SVE bitwise shift by vector (predicated)* on page C4-411
11	*SVE bitwise shift by wide elements (predicated)* on page C4-412

SVE bitwise shift by immediate (predicated)

This section describes the encoding of the SVE bitwise shift by immediate (predicated) instruction class. The encodings in this section are decoded from *SVE Bitwise Shift - Predicated*.

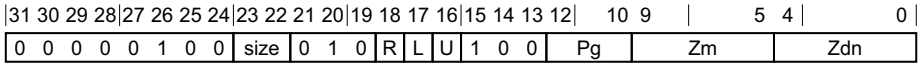


Decode fields			Instruction page
opc	L	U	
00	0	0	ASR (immediate, predicated)
00	0	1	LSR (immediate, predicated)
00	1	0	Unallocated.

Decode fields			Instruction page
opc	L	U	
00	1	1	LSL (immediate, predicated)
01	0	0	ASRD
01	0	1	Unallocated.
01	1	0	SQSHL (immediate)
01	1	1	UQSHL (immediate)
10	-	-	Unallocated.
11	0	0	SRSHR
11	0	1	URSHR
11	1	0	Unallocated.
11	1	1	SQSHLU

SVE bitwise shift by vector (predicated)

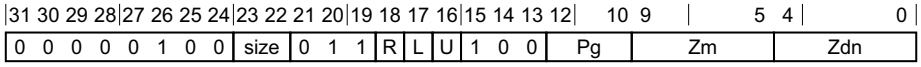
This section describes the encoding of the SVE bitwise shift by vector (predicated) instruction class. The encodings in this section are decoded from *SVE Bitwise Shift - Predicated* on page C4-410.



Decode fields			Instruction page
R	L	U	
-	1	0	Unallocated.
0	0	0	ASR (vectors)
0	0	1	LSR (vectors)
0	1	1	LSL (vectors)
1	0	0	ASRR
1	0	1	LSRR
1	1	1	LSLR

SVE bitwise shift by wide elements (predicated)

This section describes the encoding of the SVE bitwise shift by wide elements (predicated) instruction class. The encodings in this section are decoded from *SVE Bitwise Shift - Predicated* on page C4-410.



Decode fields			Instruction page
R	L	U	
0	0	0	ASR (wide elements, predicated)
0	0	1	LSR (wide elements, predicated)
0	1	0	Unallocated.
0	1	1	LSL (wide elements, predicated)
1	-	-	Unallocated.

C4.1.15 SVE Integer Unary Arithmetic - Predicated

This section describes the encoding of the SVE Integer Unary Arithmetic - Predicated group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

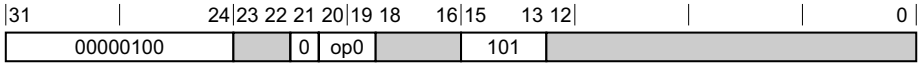
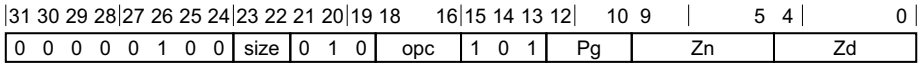


Table C4-16 Encoding table for the SVE Integer Unary Arithmetic - Predicated group

Decode fields	Decode group or instruction page
op0	
0x	Unallocated.
10	*SVE integer unary operations (predicated)* on page C4-412
11	*SVE bitwise unary operations (predicated)* on page C4-413

SVE integer unary operations (predicated)

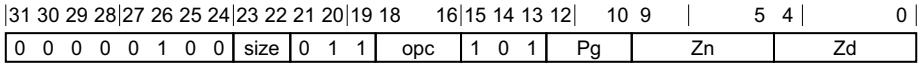
This section describes the encoding of the SVE integer unary operations (predicated) instruction class. The encodings in this section are decoded from *SVE Integer Unary Arithmetic - Predicated*.



Decode fields	Instruction page
opc	
000	SXTB, SXTH, SXTW - Encoding
001	UXTB, UXTH, UXTW - Encoding
010	SXTB, SXTH, SXTW - Encoding
011	UXTB, UXTH, UXTW - Encoding
100	SXTB, SXTH, SXTW - Encoding
101	UXTB, UXTH, UXTW - Encoding
110	ABS
111	NEG

SVE bitwise unary operations (predicated)

This section describes the encoding of the SVE bitwise unary operations (predicated) instruction class. The encodings in this section are decoded from *SVE Integer Unary Arithmetic - Predicated* on page C4-412.



Decode fields	Instruction page
opc	
000	CLS
001	CLZ
010	CNT
011	CNOT
100	FABS
101	FNEG
110	NOT (vector)
111	Unallocated.

C4.1.16 SVE Bitwise Logical - Unpredicated

This section describes the encoding of the SVE Bitwise Logical - Unpredicated group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

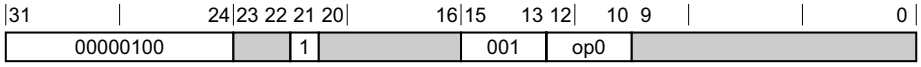
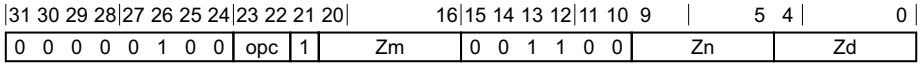


Table C4-17 Encoding table for the SVE Bitwise Logical - Unpredicated group

Decode fields op0	Decode group or instruction page
0xx	Unallocated.
100	*SVE bitwise logical operations (unpredicated)* on page C4-414
101	XAR
11x	*SVE2 bitwise ternary operations* on page C4-415

SVE bitwise logical operations (unpredicated)

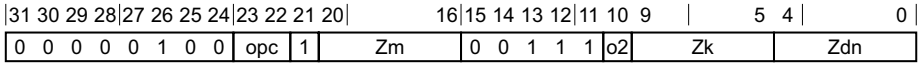
This section describes the encoding of the SVE bitwise logical operations (unpredicated) instruction class. The encodings in this section are decoded from *SVE Bitwise Logical - Unpredicated*.



Decode fields opc	Instruction page
00	AND (vectors, unpredicated)
01	ORR (vectors, unpredicated)
10	EOR (vectors, unpredicated)
11	BIC (vectors, unpredicated)

SVE2 bitwise ternary operations

This section describes the encoding of the SVE2 bitwise ternary operations instruction class. The encodings in this section are decoded from *SVE Bitwise Logical - Unpredicated* on page C4-414.



Decode fields		Instruction page
opc	o2	
00	0	EOR3
00	1	BSL
01	0	BCAX
01	1	BSL1N
1x	0	Unallocated.
10	1	BSL2N
11	1	NBSL

C4.1.17 SVE Index Generation

This section describes the encoding of the SVE Index Generation group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

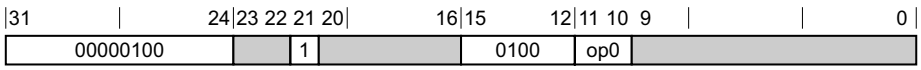


Table C4-18 Encoding table for the SVE Index Generation group

Decode fields	Decode group or instruction page
op0	
00	INDEX (immediates)
01	INDEX (scalar, immediate)
10	INDEX (immediate, scalar)
11	INDEX (scalars)

C4.1.18 SVE Stack Allocation

This section describes the encoding of the SVE Stack Allocation group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

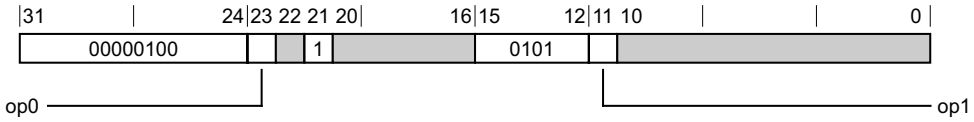
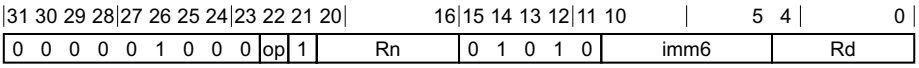


Table C4-19 Encoding table for the SVE Stack Allocation group

Decode fields		Decode group or instruction page
op0	op1	
0	0	*SVE stack frame adjustment* on page C4-416
0	1	*SVE integer arithmetic* on page C4-417
1	0	*SVE stack frame size* on page C4-417
1	1	*Streaming SVE stack frame size* on page C4-418

SVE stack frame adjustment

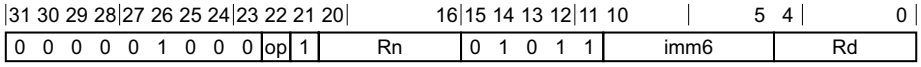
This section describes the encoding of the SVE stack frame adjustment instruction class. The encodings in this section are decoded from *SVE Stack Allocation*.



Decode fields	Instruction page
op	
0	ADDVL
1	ADDPL

SVE integer arithmetic

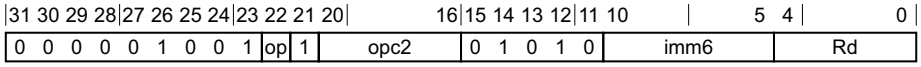
This section describes the encoding of the SVE integer arithmetic instruction class. The encodings in this section are decoded from *SVE Stack Allocation* on page C4-416.



Decode fields		Instruction page	Feature
op			
0		ADDSVL	FEAT_SME
1		ADDSPL	FEAT_SME

SVE stack frame size

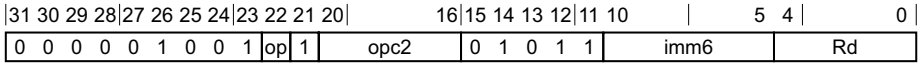
This section describes the encoding of the SVE stack frame size instruction class. The encodings in this section are decoded from *SVE Stack Allocation* on page C4-416.



Decode fields		Instruction page
op	opc2	
0	0xxxx	Unallocated.
0	10xxx	Unallocated.
0	110xx	Unallocated.
0	1110x	Unallocated.
0	11110	Unallocated.
0	11111	RDVL
1	-	Unallocated.

Streaming SVE stack frame size

This section describes the encoding of the Streaming SVE stack frame size instruction class. The encodings in this section are decoded from *SVE Stack Allocation* on page C4-416.



Decode fields		Instruction page	Feature
op	opc2		
0	0xxxx	Unallocated.	-
0	10xxx	Unallocated.	-
0	110xx	Unallocated.	-
0	1110x	Unallocated.	-
0	11110	Unallocated.	-
0	11111	RDSVL	FEAT_SME
1	-	Unallocated.	-

C4.1.19 SVE2 Integer Multiply - Unpredicated

This section describes the encoding of the SVE2 Integer Multiply - Unpredicated group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

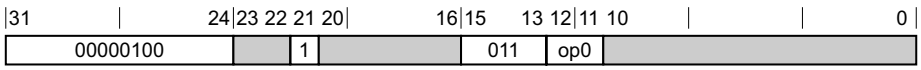
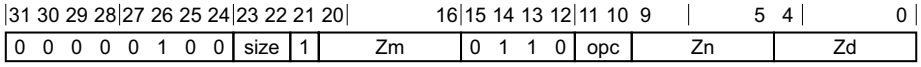


Table C4-20 Encoding table for the SVE2 Integer Multiply - Unpredicated group

Decode fields	Decode group or instruction page
op0	
0x	*SVE2 integer multiply vectors (unpredicated)* on page C4-419
10	*SVE2 signed saturating doubling multiply high (unpredicated)* on page C4-419
11	Unallocated.

SVE2 integer multiply vectors (unpredicated)

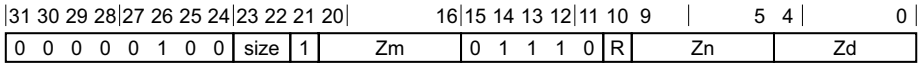
This section describes the encoding of the SVE2 integer multiply vectors (unpredicated) instruction class. The encodings in this section are decoded from *SVE2 Integer Multiply - Unpredicated* on page C4-418.



Decode fields		Instruction page
size	opc	
-	00	MUL (vectors, unpredicated)
-	10	SMULH (unpredicated)
-	11	UMULH (unpredicated)
00	01	PMUL
01	01	Unallocated.
1x	01	Unallocated.

SVE2 signed saturating doubling multiply high (unpredicated)

This section describes the encoding of the SVE2 signed saturating doubling multiply high (unpredicated) instruction class. The encodings in this section are decoded from *SVE2 Integer Multiply - Unpredicated* on page C4-418.



Decode fields	Instruction page
R	
0	SQDMULH (vectors)
1	SQRDMULH (vectors)

C4.1.20 SVE Bitwise Shift - Unpredicated

This section describes the encoding of the SVE Bitwise Shift - Unpredicated group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

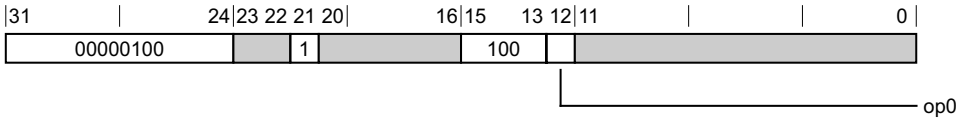
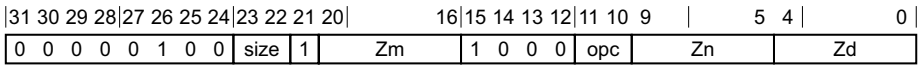


Table C4-21 Encoding table for the SVE Bitwise Shift - Unpredicated group

Decode fields	Decode group or instruction page
op0	
0	*SVE bitwise shift by wide elements (unpredicated)* on page C4-420
1	*SVE bitwise shift by immediate (unpredicated)* on page C4-420

SVE bitwise shift by wide elements (unpredicated)

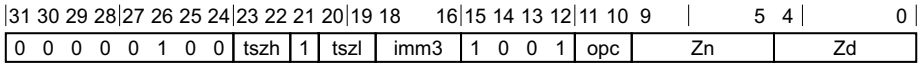
This section describes the encoding of the SVE bitwise shift by wide elements (unpredicated) instruction class. The encodings in this section are decoded from *SVE Bitwise Shift - Unpredicated*.



Decode fields	Instruction page
opc	
00	ASR (wide elements, unpredicated)
01	LSR (wide elements, unpredicated)
10	Unallocated.
11	LSL (wide elements, unpredicated)

SVE bitwise shift by immediate (unpredicated)

This section describes the encoding of the SVE bitwise shift by immediate (unpredicated) instruction class. The encodings in this section are decoded from *SVE Bitwise Shift - Unpredicated*.



Decode fields	Instruction page
opc	
00	ASR (immediate, unpredicated)
01	LSR (immediate, unpredicated)
10	Unallocated.
11	LSL (immediate, unpredicated)

C4.1.21 SVE Integer Misc - Unpredicated

This section describes the encoding of the SVE Integer Misc - Unpredicated group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

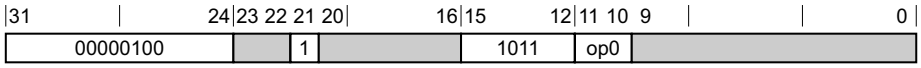
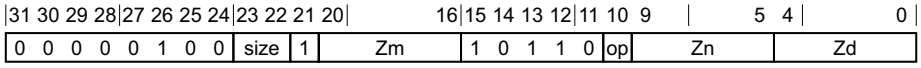


Table C4-22 Encoding table for the SVE Integer Misc - Unpredicated group

Decode fields	Decode group or instruction page
op0	
0x	*SVE floating-point trig select coefficient* on page C4-421
10	*SVE floating-point exponential accelerator* on page C4-422
11	*SVE constructive prefix (unpredicated)* on page C4-422

SVE floating-point trig select coefficient

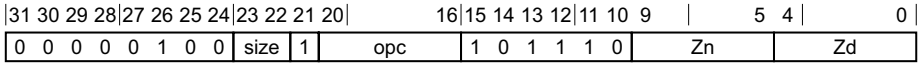
This section describes the encoding of the SVE floating-point trig select coefficient instruction class. The encodings in this section are decoded from *SVE Integer Misc - Unpredicated*.



Decode fields	Instruction page
op	
0	FTSSEL
1	Unallocated.

SVE floating-point exponential accelerator

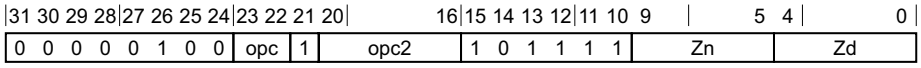
This section describes the encoding of the SVE floating-point exponential accelerator instruction class. The encodings in this section are decoded from *SVE Integer Misc - Unpredicated* on page C4-421.



Decode fields	Instruction page
opc	
00000	FEXPA
00001	Unallocated.
0001x	Unallocated.
001xx	Unallocated.
01xxx	Unallocated.
1xxxx	Unallocated.

SVE constructive prefix (unpredicated)

This section describes the encoding of the SVE constructive prefix (unpredicated) instruction class. The encodings in this section are decoded from *SVE Integer Misc - Unpredicated* on page C4-421.



Decode fields		Instruction page
opc	opc2	
00	00000	MOVPRFX (unpredicated)
00	00001	Unallocated.
00	0001x	Unallocated.
00	001xx	Unallocated.
00	01xxx	Unallocated.
00	1xxxx	Unallocated.
01	-	Unallocated.
1x	-	Unallocated.

C4.1.22 SVE Element Count

This section describes the encoding of the SVE Element Count group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

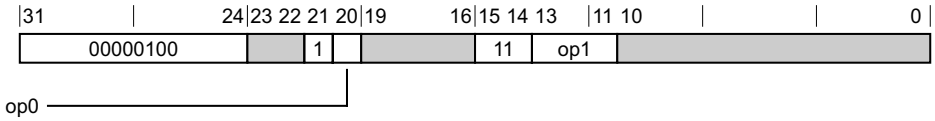
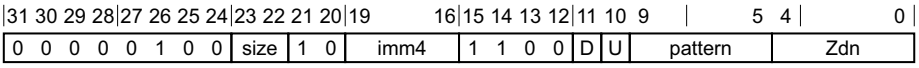


Table C4-23 Encoding table for the SVE Element Count group

Decode fields		Decode group or instruction page
op0	op1	
0	00x	*SVE saturating inc/dec vector by element count* on page C4-423
0	100	*SVE element count* on page C4-424
0	101	Unallocated.
1	000	*SVE inc/dec vector by element count* on page C4-424
1	100	*SVE inc/dec register by element count* on page C4-425
1	x01	Unallocated.
-	01x	Unallocated.
-	11x	*SVE saturating inc/dec register by element count* on page C4-425

SVE saturating inc/dec vector by element count

This section describes the encoding of the SVE saturating inc/dec vector by element count instruction class. The encodings in this section are decoded from *SVE Element Count*.

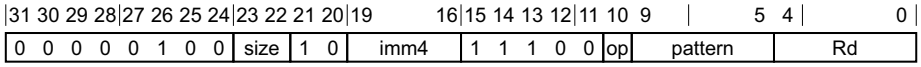


Decode fields			Instruction page
size	D	U	
00	-	-	Unallocated.
01	0	0	SQINCH (vector)
01	0	1	UQINCH (vector)
01	1	0	SQDECH (vector)
01	1	1	UQDECH (vector)
10	0	0	SQINCW (vector)
10	0	1	UQINCW (vector)
10	1	0	SQDECW (vector)

Decode fields			Instruction page
size	D	U	
10	1	1	UQDECW (vector)
11	0	0	SQINCD (vector)
11	0	1	UQINCD (vector)
11	1	0	SQDECD (vector)
11	1	1	UQDECD (vector)

SVE element count

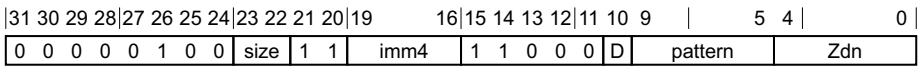
This section describes the encoding of the SVE element count instruction class. The encodings in this section are decoded from *SVE Element Count* on page C4-423.



Decode fields		Instruction page
size	op	
-	1	Unallocated.
00	0	CNTB, CNTD, CNTH, CNTW - Encoding
01	0	CNTB, CNTD, CNTH, CNTW - Encoding
10	0	CNTB, CNTD, CNTH, CNTW - Encoding
11	0	CNTB, CNTD, CNTH, CNTW - Encoding

SVE inc/dec vector by element count

This section describes the encoding of the SVE inc/dec vector by element count instruction class. The encodings in this section are decoded from *SVE Element Count* on page C4-423.

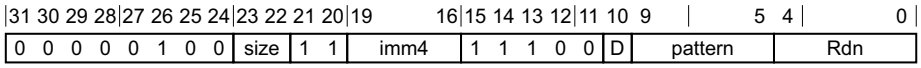


Decode fields		Instruction page
size	D	
00	-	Unallocated.
01	0	INCD, INCH, INCW (vector) - Encoding
01	1	DECD, DECH, DECW (vector) - Encoding
10	0	INCD, INCH, INCW (vector) - Encoding

Decode fields		Instruction page
size	D	
10	1	DECD, DECH, DECW (vector) - Encoding
11	0	INCD, INCH, INCW (vector) - Encoding
11	1	DECD, DECH, DECW (vector) - Encoding

SVE inc/dec register by element count

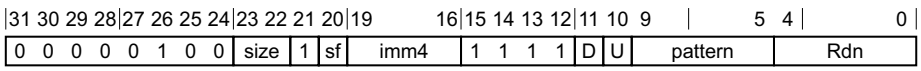
This section describes the encoding of the SVE inc/dec register by element count instruction class. The encodings in this section are decoded from *SVE Element Count* on page C4-423.



Decode fields		Instruction page
size	D	
00	0	INCB, INCD, INCH, INCW (scalar) - Encoding
00	1	DECB, DECD, DECH, DECW (scalar) - Encoding
01	0	INCB, INCD, INCH, INCW (scalar) - Encoding
01	1	DECB, DECD, DECH, DECW (scalar) - Encoding
10	0	INCB, INCD, INCH, INCW (scalar) - Encoding
10	1	DECB, DECD, DECH, DECW (scalar) - Encoding
11	0	INCB, INCD, INCH, INCW (scalar) - Encoding
11	1	DECB, DECD, DECH, DECW (scalar) - Encoding

SVE saturating inc/dec register by element count

This section describes the encoding of the SVE saturating inc/dec register by element count instruction class. The encodings in this section are decoded from *SVE Element Count* on page C4-423.



Decode fields				Instruction page
size	sf	D	U	
00	0	0	0	SQINCB - Encoding
00	0	0	1	UQINCB - Encoding
00	0	1	0	SQDECB - Encoding

Decode fields				Instruction page
size	sf	D	U	
00	0	1	1	UQDECB - Encoding
00	1	0	0	SQINCB - Encoding
00	1	0	1	UQINCB - Encoding
00	1	1	0	SQDECB - Encoding
00	1	1	1	UQDECB - Encoding
01	0	0	0	SQINCH (scalar) - Encoding
01	0	0	1	UQINCH (scalar) - Encoding
01	0	1	0	SQDECH (scalar) - Encoding
01	0	1	1	UQDECH (scalar) - Encoding
01	1	0	0	SQINCH (scalar) - Encoding
01	1	0	1	UQINCH (scalar) - Encoding
01	1	1	0	SQDECH (scalar) - Encoding
01	1	1	1	UQDECH (scalar) - Encoding
10	0	0	0	SQINCW (scalar) - Encoding
10	0	0	1	UQINCW (scalar) - Encoding
10	0	1	0	SQDECW (scalar) - Encoding
10	0	1	1	UQDECW (scalar) - Encoding
10	1	0	0	SQINCW (scalar) - Encoding
10	1	0	1	UQINCW (scalar) - Encoding
10	1	1	0	SQDECW (scalar) - Encoding
10	1	1	1	UQDECW (scalar) - Encoding
11	0	0	0	SQINCD (scalar) - Encoding
11	0	0	1	UQINCD (scalar) - Encoding
11	0	1	0	SQDECD (scalar) - Encoding
11	0	1	1	UQDECD (scalar) - Encoding
11	1	0	0	SQINCD (scalar) - Encoding
11	1	0	1	UQINCD (scalar) - Encoding
11	1	1	0	SQDECD (scalar) - Encoding
11	1	1	1	UQDECD (scalar) - Encoding

C4.1.23 SVE Bitwise Immediate

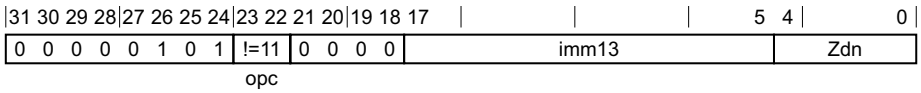
This section describes the encoding of the SVE Bitwise Immediate group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

Table C4-24 Encoding table for the SVE Bitwise Immediate group

Decode fields		Decode group or instruction page
op0	op1	
11	00	DUPM
!= 11	00	*SVE bitwise logical with immediate (unpredicated)*
-	!= 00	Unallocated.

SVE bitwise logical with immediate (unpredicated)

This section describes the encoding of the SVE bitwise logical with immediate (unpredicated) instruction class. The encodings in this section are decoded from *SVE Bitwise Immediate* on page C4-426.



Decode fields	Instruction page
opc	
00	ORR (immediate)
01	EOR (immediate)
10	AND (immediate)

C4.1.24 SVE Integer Wide Immediate - Predicated

This section describes the encoding of the SVE Integer Wide Immediate - Predicated group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

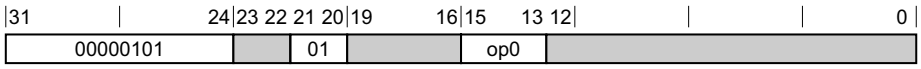


Table C4-25 Encoding table for the SVE Integer Wide Immediate - Predicated group

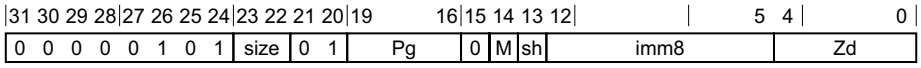
Decode fields	Decode group or instruction page
op0	
0xx	*SVE copy integer immediate (predicated)* on page C4-428

Table C4-25 Encoding table for the SVE Integer Wide Immediate - Predicated group (continued)

Decode fields	Decode group or instruction page
op0	
10x	Unallocated.
110	FCPY
111	Unallocated.

SVE copy integer immediate (predicated)

This section describes the encoding of the SVE copy integer immediate (predicated) instruction class. The encodings in this section are decoded from *SVE Integer Wide Immediate - Predicated* on page C4-427.



Decode fields	Instruction page
M	
0	CPY (immediate, zeroing)
1	CPY (immediate, merging)

C4.1.25 SVE Permute Vector - Unpredicated

This section describes the encoding of the SVE Permute Vector - Unpredicated group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

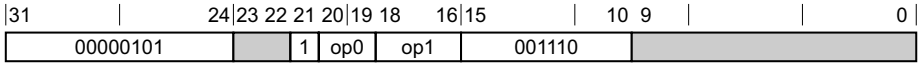


Table C4-26 Encoding table for the SVE Permute Vector - Unpredicated group

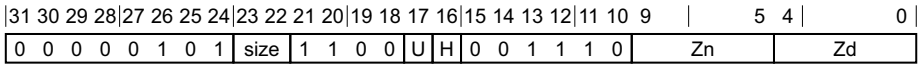
Decode fields		Decode group or instruction page
op0	op1	
00	000	DUP (scalar)
00	100	INSR (scalar)
00	x10	Unallocated.
00	xx1	Unallocated.
01	-	Unallocated.
10	0xx	*SVE unpack vector elements* on page C4-429
10	100	INSR (SIMD&FP scalar)

Table C4-26 Encoding table for the SVE Permute Vector - Unpredicated group (continued)

Decode fields		Decode group or instruction page
op0	op1	
10	110	Unallocated.
10	1x1	Unallocated.
11	000	REV (vector)
11	!= 000	Unallocated.

SVE unpack vector elements

This section describes the encoding of the SVE unpack vector elements instruction class. The encodings in this section are decoded from *SVE Permute Vector - Unpredicated* on page C4-428.



Decode fields		Instruction page
U	H	
0	0	SUNPKHI, SUNPKLO - Encoding
0	1	SUNPKHI, SUNPKLO - Encoding
1	0	UUNPKHI, UUNPKLO - Encoding
1	1	UUNPKHI, UUNPKLO - Encoding

C4.1.26 SVE Permute Predicate

This section describes the encoding of the SVE Permute Predicate group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

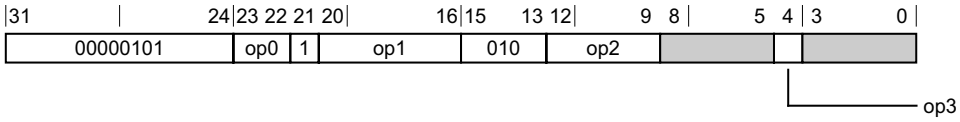


Table C4-27 Encoding table for the SVE Permute Predicate group

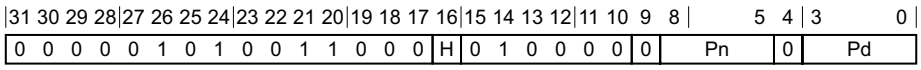
Decode fields				Decode group or instruction page
op0	op1	op2	op3	
00	1000x	0000	0	*SVE unpack predicate elements* on page C4-430
01	1000x	0000	0	Unallocated.
10	1000x	0000	0	Unallocated.

Table C4-27 Encoding table for the SVE Permute Predicate group (continued)

Decode fields				Decode group or instruction page
op0	op1	op2	op3	
11	1000x	0000	0	Unallocated.
-	0xxxx	xxx0	0	*SVE permute predicate elements* on page C4-431
-	0xxxx	xxx1	0	Unallocated.
-	10100	0000	0	REV (predicate)
-	10101	0000	0	Unallocated.
-	10x0x	1000	0	Unallocated.
-	10x0x	x100	0	Unallocated.
-	10x0x	xx10	0	Unallocated.
-	10x0x	xxx1	0	Unallocated.
-	10x1x	-	0	Unallocated.
-	11xxx	-	0	Unallocated.
-	-	-	1	Unallocated.

SVE unpack predicate elements

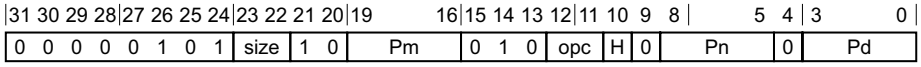
This section describes the encoding of the SVE unpack predicate elements instruction class. The encodings in this section are decoded from *SVE Permute Predicate* on page C4-429.



Decode fields	Instruction page
H	
0	PUNPKHI, PUNPKLO - Encoding
1	PUNPKHI, PUNPKLO - Encoding

SVE permute predicate elements

This section describes the encoding of the SVE permute predicate elements instruction class. The encodings in this section are decoded from *SVE Permute Predicate* on page C4-429.



Decode fields		Instruction page
opc	H	
00	0	ZIP1, ZIP2 (predicates) - Encoding
00	1	ZIP1, ZIP2 (predicates) - Encoding
01	0	UZP1, UZP2 (predicates) - Encoding
01	1	UZP1, UZP2 (predicates) - Encoding
10	0	TRN1, TRN2 (predicates) - Encoding
10	1	TRN1, TRN2 (predicates) - Encoding
11	-	Unallocated.

C4.1.27 SVE Permute Vector - Predicated

This section describes the encoding of the SVE Permute Vector - Predicated group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

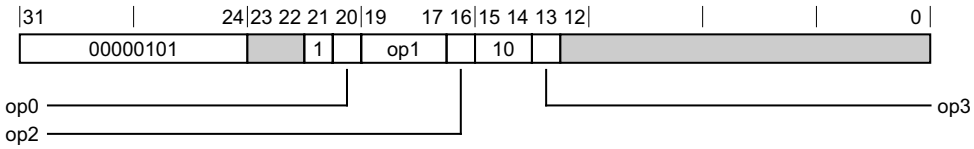


Table C4-28 Encoding table for the SVE Permute Vector - Predicated group

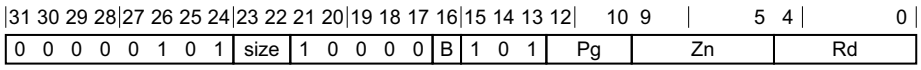
Decode fields				Decode group or instruction page
op0	op1	op2	op3	
0	000	0	0	CPY (SIMD&FP scalar)
0	000	1	0	COMPACT
0	000	-	1	*SVE extract element to general register* on page C4-432
0	001	-	0	*SVE extract element to SIMD&FP scalar register* on page C4-432
0	01x	-	0	*SVE reverse within elements* on page C4-433
0	01x	-	1	Unallocated.
0	100	0	1	CPY (scalar)
0	100	1	1	Unallocated.

Table C4-28 Encoding table for the SVE Permute Vector - Predicated group (continued)

Decode fields				Decode group or instruction page
op0	op1	op2	op3	
0	100	-	0	*SVE conditionally broadcast element to vector* on page C4-433
0	101	-	0	*SVE conditionally extract element to SIMD&FP scalar* on page C4-434
0	110	0	0	SPLICE - Encoding
0	110	1	0	SPLICE - Encoding
0	110	-	1	Unallocated.
0	111	0	0	*SVE reverse doublewords* on page C4-434
0	111	0	1	Unallocated.
0	111	1	-	Unallocated.
0	x01	-	1	Unallocated.
1	000	-	0	Unallocated.
1	000	-	1	*SVE conditionally extract element to general register* on page C4-434
1	!= 000	-	-	Unallocated.

SVE extract element to general register

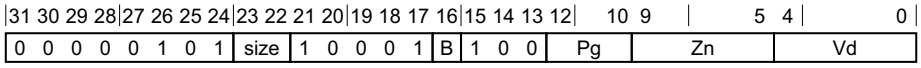
This section describes the encoding of the SVE extract element to general register instruction class. The encodings in this section are decoded from *SVE Permute Vector - Predicated* on page C4-431.



Decode fields	Instruction page
B	
0	LASTA (scalar)
1	LASTB (scalar)

SVE extract element to SIMD&FP scalar register

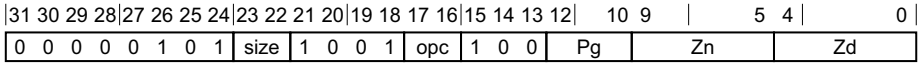
This section describes the encoding of the SVE extract element to SIMD&FP scalar register instruction class. The encodings in this section are decoded from *SVE Permute Vector - Predicated* on page C4-431.



Decode fields	Instruction page
B	
0	LASTA (SIMD&FP scalar)
1	LASTB (SIMD&FP scalar)

SVE reverse within elements

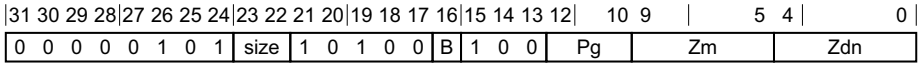
This section describes the encoding of the SVE reverse within elements instruction class. The encodings in this section are decoded from *SVE Permute Vector - Predicated* on page C4-431.



Decode fields	Instruction page
opc	
00	REVB, REVH, REVW - Encoding
01	REVB, REVH, REVW - Encoding
10	REVB, REVH, REVW - Encoding
11	RBIT

SVE conditionally broadcast element to vector

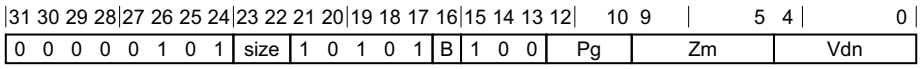
This section describes the encoding of the SVE conditionally broadcast element to vector instruction class. The encodings in this section are decoded from *SVE Permute Vector - Predicated* on page C4-431.



Decode fields	Instruction page
B	
0	CLASTA (vectors)
1	CLASTB (vectors)

SVE conditionally extract element to SIMD&FP scalar

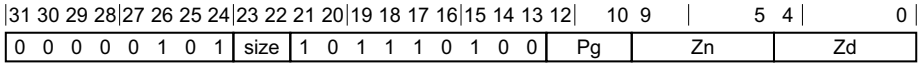
This section describes the encoding of the SVE conditionally extract element to SIMD&FP scalar instruction class. The encodings in this section are decoded from *SVE Permute Vector - Predicated* on page C4-431.



Decode fields	Instruction page
B	
0	CLASTA (SIMD&FP scalar)
1	CLASTB (SIMD&FP scalar)

SVE reverse doublewords

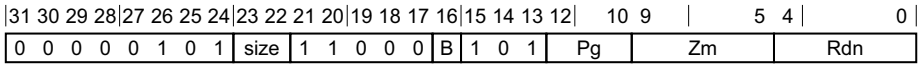
This section describes the encoding of the SVE reverse doublewords instruction class. The encodings in this section are decoded from *SVE Permute Vector - Predicated* on page C4-431.



Decode fields	Instruction page	Feature
size		
00	REVD	FEAT_SME
01	Unallocated.	-
1x	Unallocated.	-

SVE conditionally extract element to general register

This section describes the encoding of the SVE conditionally extract element to general register instruction class. The encodings in this section are decoded from *SVE Permute Vector - Predicated* on page C4-431.



Decode fields	Instruction page
B	
0	CLASTA (scalar)
1	CLASTB (scalar)

C4.1.28 SVE Permute Vector - Extract

This section describes the encoding of the SVE Permute Vector - Extract group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

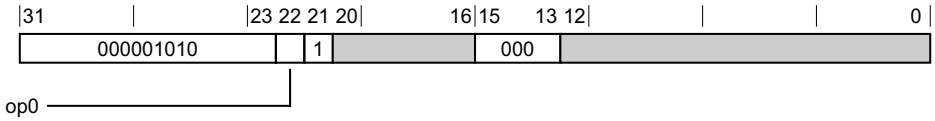


Table C4-29 Encoding table for the SVE Permute Vector - Extract group

Decode fields	Decode group or instruction page
op0	
0	EXT - Encoding
1	EXT - Encoding

C4.1.29 SVE Permute Vector - Segments

This section describes the encoding of the SVE Permute Vector - Segments group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

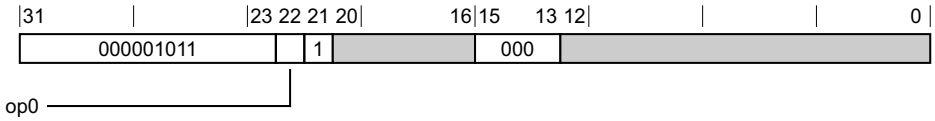
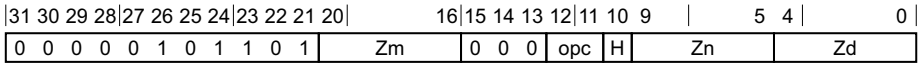


Table C4-30 Encoding table for the SVE Permute Vector - Segments group

Decode fields	Decode group or instruction page
op0	
0	*SVE permute vector segments* on page C4-435
1	Unallocated.

SVE permute vector segments

This section describes the encoding of the SVE permute vector segments instruction class. The encodings in this section are decoded from *SVE Permute Vector - Segments*.



Decode fields		Instruction page	Feature
opc	H		
00	0	ZIP1, ZIP2 (vectors) - Encoding	FEAT_F64MM
00	1	ZIP1, ZIP2 (vectors) - Encoding	FEAT_F64MM
01	0	UZP1, UZP2 (vectors) - Encoding	FEAT_F64MM
01	1	UZP1, UZP2 (vectors) - Encoding	FEAT_F64MM
10	-	Unallocated.	-
11	0	TRN1, TRN2 (vectors) - Encoding	FEAT_F64MM
11	1	TRN1, TRN2 (vectors) - Encoding	FEAT_F64MM

C4.1.30 SVE Integer Compare - Vectors

This section describes the encoding of the SVE Integer Compare - Vectors group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

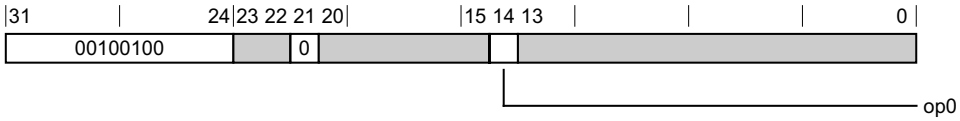
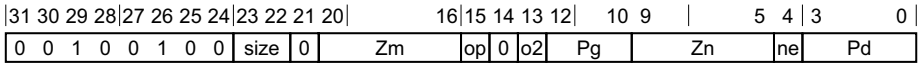


Table C4-31 Encoding table for the SVE Integer Compare - Vectors group

Decode fields	Decode group or instruction page
op0	
0	*SVE integer compare vectors* on page C4-436
1	*SVE integer compare with wide elements* on page C4-437

SVE integer compare vectors

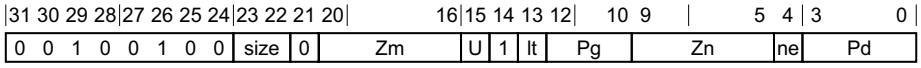
This section describes the encoding of the SVE integer compare vectors instruction class. The encodings in this section are decoded from *SVE Integer Compare - Vectors*.



Decode fields			Instruction page
op	o2	ne	
0	0	0	CMP<cc> (vectors) - Encoding
0	0	1	CMP<cc> (vectors) - Encoding
0	1	0	CMP<cc> (wide elements) - Encoding
0	1	1	CMP<cc> (wide elements) - Encoding
1	0	0	CMP<cc> (vectors) - Encoding
1	0	1	CMP<cc> (vectors) - Encoding
1	1	0	CMP<cc> (vectors) - Encoding
1	1	1	CMP<cc> (vectors) - Encoding

SVE integer compare with wide elements

This section describes the encoding of the SVE integer compare with wide elements instruction class. The encodings in this section are decoded from *SVE Integer Compare - Vectors* on page C4-436.



Decode fields			Instruction page
U	lt	ne	
0	0	0	CMP<cc> (wide elements) - Encoding
0	0	1	CMP<cc> (wide elements) - Encoding
0	1	0	CMP<cc> (wide elements) - Encoding
0	1	1	CMP<cc> (wide elements) - Encoding
1	0	0	CMP<cc> (wide elements) - Encoding
1	0	1	CMP<cc> (wide elements) - Encoding
1	1	0	CMP<cc> (wide elements) - Encoding
1	1	1	CMP<cc> (wide elements) - Encoding

C4.1.31 SVE Propagate Break

This section describes the encoding of the SVE Propagate Break group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

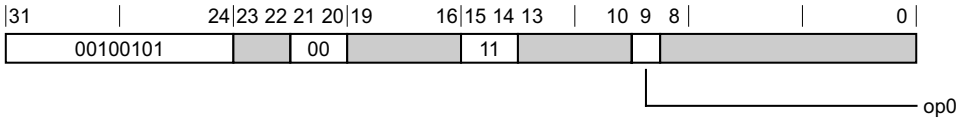
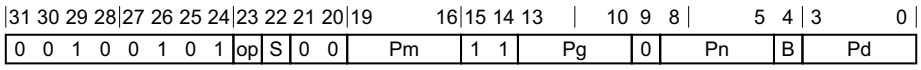


Table C4-32 Encoding table for the SVE Propagate Break group

Decode fields	Decode group or instruction page
op0	
0	*SVE propagate break from previous partition* on page C4-438
1	Unallocated.

SVE propagate break from previous partition

This section describes the encoding of the SVE propagate break from previous partition instruction class. The encodings in this section are decoded from *SVE Propagate Break*.



Decode fields			Instruction page
op	S	B	
0	0	0	BRKPA
0	0	1	BRKPB
0	1	0	BRKPAS
0	1	1	BRKPBS
1	-	-	Unallocated.

C4.1.32 SVE Partition Break

This section describes the encoding of the SVE Partition Break group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

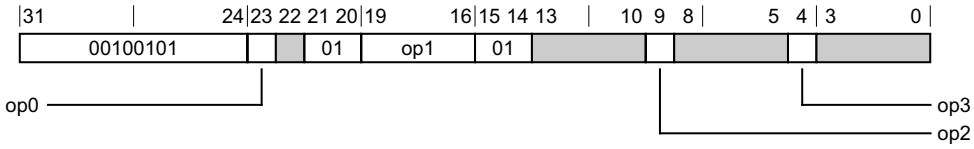
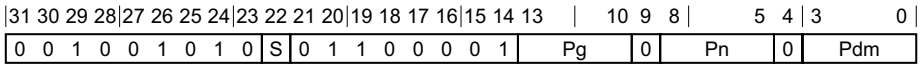


Table C4-33 Encoding table for the SVE Partition Break group

Decode fields				Decode group or instruction page
op0	op1	op2	op3	
0	1000	0	0	*SVE propagate break to next partition*
0	1000	0	1	Unallocated.
0	x000	1	-	Unallocated.
0	x1xx	-	-	Unallocated.
0	xx1x	-	-	Unallocated.
0	xxx1	-	-	Unallocated.
1	0000	1	-	Unallocated.
1	!= 0000	-	-	Unallocated.
-	0000	0	-	*SVE partition break condition* on page C4-440

SVE propagate break to next partition

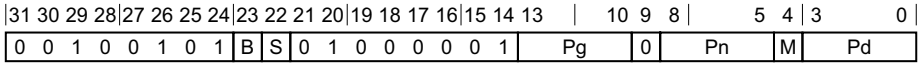
This section describes the encoding of the SVE propagate break to next partition instruction class. The encodings in this section are decoded from *SVE Partition Break* on page C4-438.



Decode fields	Instruction page
S	
0	BRKN
1	BRKNS

SVE partition break condition

This section describes the encoding of the SVE partition break condition instruction class. The encodings in this section are decoded from *SVE Partition Break* on page C4-438.



Decode fields			Instruction page
B	S	M	
-	1	1	Unallocated.
0	0	-	BRKA
0	1	0	BRKAS
1	0	-	BRKB
1	1	0	BRKBS

C4.1.33 SVE Predicate Misc

This section describes the encoding of the SVE Predicate Misc group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

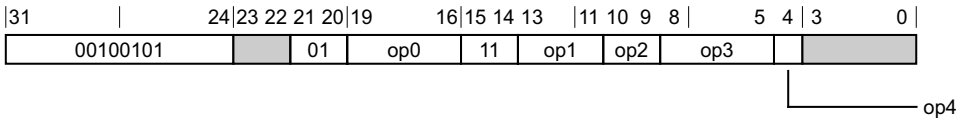


Table C4-34 Encoding table for the SVE Predicate Misc group

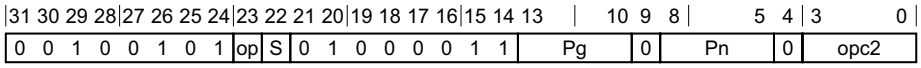
Decode fields					Decode group or instruction page
op0	op1	op2	op3	op4	
0000	-	x0	-	0	*SVE predicate test* on page C4-441
0100	-	x0	-	0	Unallocated.
0x10	-	x0	-	0	Unallocated.
0xx1	-	x0	-	0	Unallocated.
0xxx	-	x1	-	0	Unallocated.
1000	000	00	-	0	*SVE predicate first active* on page C4-442
1000	000	!= 00	-	0	Unallocated.
1000	100	10	0000	0	*SVE predicate zero* on page C4-442
1000	100	10	!= 0000	0	Unallocated.
1000	110	00	-	0	*SVE predicate read from FFR (predicated)* on page C4-442
1001	000	0x	-	0	Unallocated.

Table C4-34 Encoding table for the SVE Predicate Misc group (continued)

Decode fields					Decode group or instruction page
op0	op1	op2	op3	op4	
1001	000	10	-	0	PNEXT
1001	000	11	-	0	Unallocated.
1001	100	10	-	0	Unallocated.
1001	110	00	0000	0	*SVE predicate read from FFR (unpredicated)* on page C4-443
1001	110	00	!= 0000	0	Unallocated.
100x	010	-	-	0	Unallocated.
100x	100	0x	-	0	*SVE predicate initialize* on page C4-443
100x	100	11	-	0	Unallocated.
100x	110	!= 00	-	0	Unallocated.
100x	xx1	-	-	0	Unallocated.
110x	-	-	-	0	Unallocated.
1x1x	-	-	-	0	Unallocated.
-	-	-	-	1	Unallocated.

SVE predicate test

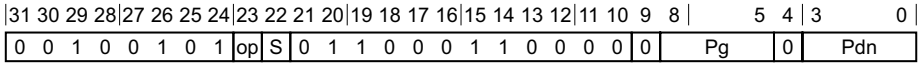
This section describes the encoding of the SVE predicate test instruction class. The encodings in this section are decoded from *SVE Predicate Misc* on page C4-440.



Decode fields			Instruction page
op	S	opc2	
0	0	-	Unallocated.
0	1	0000	PTEST
0	1	0001	Unallocated.
0	1	001x	Unallocated.
0	1	01xx	Unallocated.
0	1	1xxx	Unallocated.
1	-	-	Unallocated.

SVE predicate first active

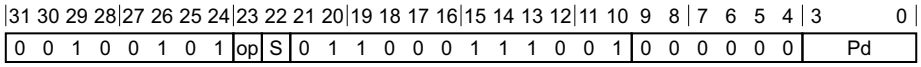
This section describes the encoding of the SVE predicate first active instruction class. The encodings in this section are decoded from *SVE Predicate Misc* on page C4-440.



Decode fields		Instruction page
op	S	
0	0	Unallocated.
0	1	PFIRST
1	-	Unallocated.

SVE predicate zero

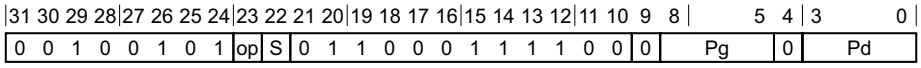
This section describes the encoding of the SVE predicate zero instruction class. The encodings in this section are decoded from *SVE Predicate Misc* on page C4-440.



Decode fields		Instruction page
op	S	
0	0	PFALSE
0	1	Unallocated.
1	-	Unallocated.

SVE predicate read from FFR (predicated)

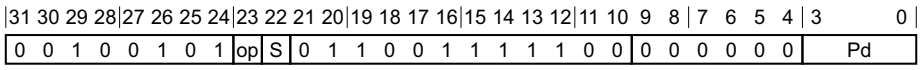
This section describes the encoding of the SVE predicate read from FFR (predicated) instruction class. The encodings in this section are decoded from *SVE Predicate Misc* on page C4-440.



Decode fields		Instruction page
op	S	
0	0	RDFFR (predicated)
0	1	RDFFRS
1	-	Unallocated.

SVE predicate read from FFR (unpredicated)

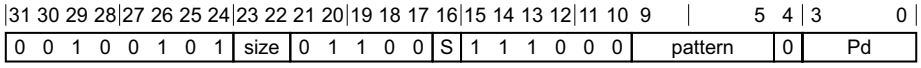
This section describes the encoding of the SVE predicate read from FFR (unpredicated) instruction class. The encodings in this section are decoded from *SVE Predicate Misc* on page C4-440.



Decode fields		Instruction page
op	S	
0	0	RDFFR (unpredicated)
0	1	Unallocated.
1	-	Unallocated.

SVE predicate initialize

This section describes the encoding of the SVE predicate initialize instruction class. The encodings in this section are decoded from *SVE Predicate Misc* on page C4-440.



Decode fields	Instruction page
S	
0	PTRUE
1	PTRUES

C4.1.34 SVE Integer Compare - Scalars

This section describes the encoding of the SVE Integer Compare - Scalars group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

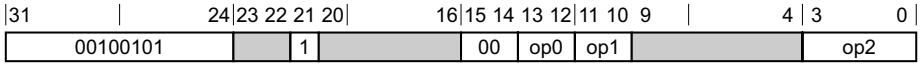
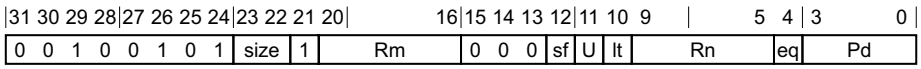


Table C4-35 Encoding table for the SVE Integer Compare - Scalars group

Decode fields			Decode group or instruction page
op0	op1	op2	
0x	-	-	*SVE integer compare scalar count and limit* on page C4-444
10	00	0000	*SVE conditionally terminate scalars* on page C4-445
10	00	!= 0000	Unallocated.
11	00	-	*SVE pointer conflict compare* on page C4-445
1x	!= 00	-	Unallocated.

SVE integer compare scalar count and limit

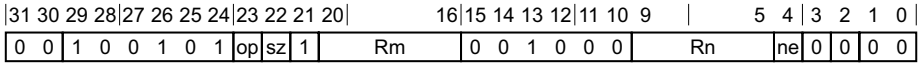
This section describes the encoding of the SVE integer compare scalar count and limit instruction class. The encodings in this section are decoded from *SVE Integer Compare - Scalars*.



Decode fields			Instruction page
U	lt	eq	
0	0	0	WHILEGE
0	0	1	WHILEGT
0	1	0	WHILELT
0	1	1	WHILELE
1	0	0	WHILEHS
1	0	1	WHILEHI
1	1	0	WHILELO
1	1	1	WHILELS

SVE conditionally terminate scalars

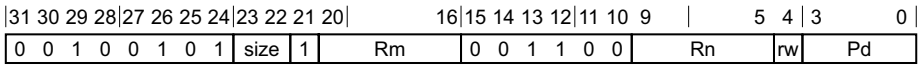
This section describes the encoding of the SVE conditionally terminate scalars instruction class. The encodings in this section are decoded from *SVE Integer Compare - Scalars* on page C4-444.



Decode fields		Instruction page
op	ne	
0	-	Unallocated.
1	0	CTERMEQ, CTERMNE - Encoding
1	1	CTERMEQ, CTERMNE - Encoding

SVE pointer conflict compare

This section describes the encoding of the SVE pointer conflict compare instruction class. The encodings in this section are decoded from *SVE Integer Compare - Scalars* on page C4-444.



Decode fields	Instruction page
rw	
0	WHILEWR
1	WHILERW

C4.1.35 SVE Integer Wide Immediate - Unpredicated

This section describes the encoding of the SVE Integer Wide Immediate - Unpredicated group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

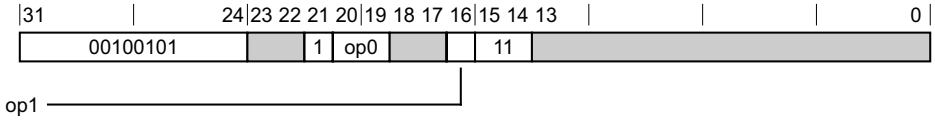
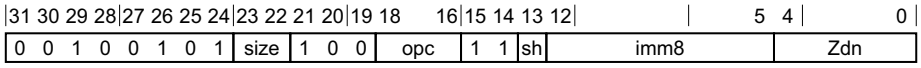


Table C4-36 Encoding table for the SVE Integer Wide Immediate - Unpredicated group

Decode fields		Decode group or instruction page
op0	op1	
00	-	*SVE integer add/subtract immediate (unpredicated)*
01	-	*SVE integer min/max immediate (unpredicated)* on page C4-447
10	-	*SVE integer multiply immediate (unpredicated)* on page C4-447
11	0	*SVE broadcast integer immediate (unpredicated)* on page C4-447
11	1	*SVE broadcast floating-point immediate (unpredicated)* on page C4-448

SVE integer add/subtract immediate (unpredicated)

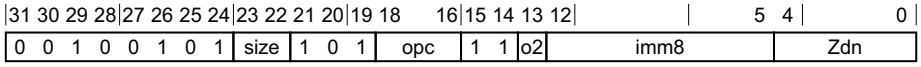
This section describes the encoding of the SVE integer add/subtract immediate (unpredicated) instruction class. The encodings in this section are decoded from *SVE Integer Wide Immediate - Unpredicated* on page C4-445.



Decode fields	Instruction page
opc	
000	ADD (immediate)
001	SUB (immediate)
010	Unallocated.
011	SUBR (immediate)
100	SQADD (immediate)
101	UQADD (immediate)
110	SQSUB (immediate)
111	UQSUB (immediate)

SVE integer min/max immediate (unpredicated)

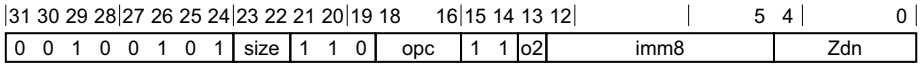
This section describes the encoding of the SVE integer min/max immediate (unpredicated) instruction class. The encodings in this section are decoded from *SVE Integer Wide Immediate - Unpredicated* on page C4-445.



Decode fields		Instruction page
opc	o2	
0xx	1	Unallocated.
000	0	SMAX (immediate)
001	0	UMAX (immediate)
010	0	SMIN (immediate)
011	0	UMIN (immediate)
1xx	-	Unallocated.

SVE integer multiply immediate (unpredicated)

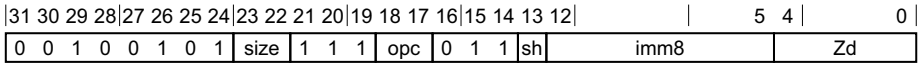
This section describes the encoding of the SVE integer multiply immediate (unpredicated) instruction class. The encodings in this section are decoded from *SVE Integer Wide Immediate - Unpredicated* on page C4-445.



Decode fields		Instruction page
opc	o2	
000	0	MUL (immediate)
000	1	Unallocated.
001	-	Unallocated.
01x	-	Unallocated.
1xx	-	Unallocated.

SVE broadcast integer immediate (unpredicated)

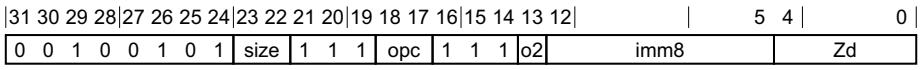
This section describes the encoding of the SVE broadcast integer immediate (unpredicated) instruction class. The encodings in this section are decoded from *SVE Integer Wide Immediate - Unpredicated* on page C4-445.



Decode fields	Instruction page
opc	
00	DUP (immediate)
01	Unallocated.
1x	Unallocated.

SVE broadcast floating-point immediate (unpredicated)

This section describes the encoding of the SVE broadcast floating-point immediate (unpredicated) instruction class. The encodings in this section are decoded from *SVE Integer Wide Immediate - Unpredicated* on page C4-445.



Decode fields		Instruction page
opc	o2	
00	0	FDUP
00	1	Unallocated.
01	-	Unallocated.
1x	-	Unallocated.

C4.1.36 SVE Predicate Count

This section describes the encoding of the SVE Predicate Count group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

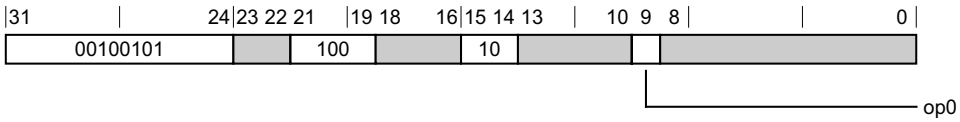
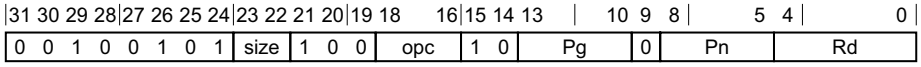


Table C4-37 Encoding table for the SVE Predicate Count group

Decode fields	Decode group or instruction page
op0	
0	*SVE predicate count* on page C4-449
1	Unallocated.

SVE predicate count

This section describes the encoding of the SVE predicate count instruction class. The encodings in this section are decoded from *SVE Predicate Count* on page C4-448.



Decode fields	Instruction page
opc	
000	CNTP
001	Unallocated.
01x	Unallocated.
1xx	Unallocated.

C4.1.37 SVE Inc/Dec by Predicate Count

This section describes the encoding of the SVE Inc/Dec by Predicate Count group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

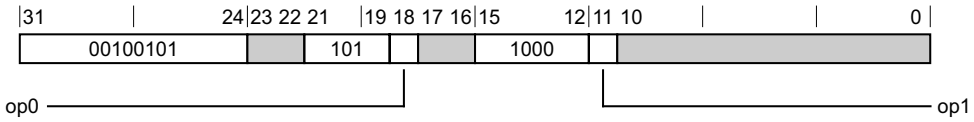
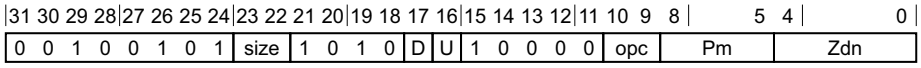


Table C4-38 Encoding table for the SVE Inc/Dec by Predicate Count group

Decode fields		Decode group or instruction page
op0	op1	
0	0	*SVE saturating inc/dec vector by predicate count* on page C4-449
0	1	*SVE saturating inc/dec register by predicate count* on page C4-450
1	0	*SVE inc/dec vector by predicate count* on page C4-451
1	1	*SVE inc/dec register by predicate count* on page C4-451

SVE saturating inc/dec vector by predicate count

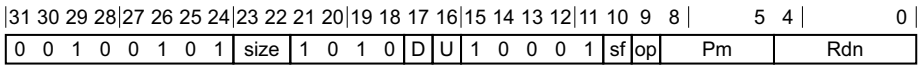
This section describes the encoding of the SVE saturating inc/dec vector by predicate count instruction class. The encodings in this section are decoded from *SVE Inc/Dec by Predicate Count*.



Decode fields			Instruction page
D	U	opc	
-	-	01	Unallocated.
-	-	1x	Unallocated.
0	0	00	SQINCP (vector)
0	1	00	UQINCP (vector)
1	0	00	SQDECP (vector)
1	1	00	UQDECP (vector)

SVE saturating inc/dec register by predicate count

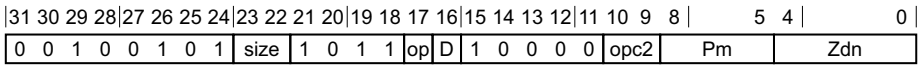
This section describes the encoding of the SVE saturating inc/dec register by predicate count instruction class. The encodings in this section are decoded from *SVE Inc/Dec by Predicate Count* on page C4-449.



Decode fields				Instruction page
D	U	sf	op	
-	-	-	1	Unallocated.
0	0	0	0	SQINCP (scalar) - Encoding
0	0	1	0	SQINCP (scalar) - Encoding
0	1	0	0	UQINCP (scalar) - Encoding
0	1	1	0	UQINCP (scalar) - Encoding
1	0	0	0	SQDECP (scalar) - Encoding
1	0	1	0	SQDECP (scalar) - Encoding
1	1	0	0	UQDECP (scalar) - Encoding
1	1	1	0	UQDECP (scalar) - Encoding

SVE inc/dec vector by predicate count

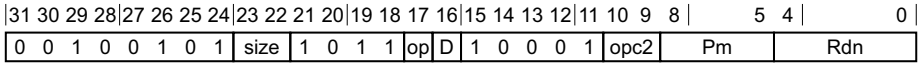
This section describes the encoding of the SVE inc/dec vector by predicate count instruction class. The encodings in this section are decoded from *SVE Inc/Dec by Predicate Count* on page C4-449.



Decode fields			Instruction page
op	D	opc2	
0	-	01	Unallocated.
0	-	1x	Unallocated.
0	0	00	INCP (vector)
0	1	00	DECP (vector)
1	-	-	Unallocated.

SVE inc/dec register by predicate count

This section describes the encoding of the SVE inc/dec register by predicate count instruction class. The encodings in this section are decoded from *SVE Inc/Dec by Predicate Count* on page C4-449.



Decode fields			Instruction page
op	D	opc2	
0	-	01	Unallocated.
0	-	1x	Unallocated.
0	0	00	INCP (scalar)
0	1	00	DECP (scalar)
1	-	-	Unallocated.

C4.1.38 SVE Write FFR

This section describes the encoding of the SVE Write FFR group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

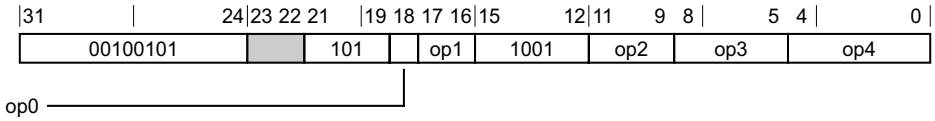
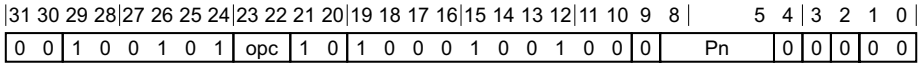


Table C4-39 Encoding table for the SVE Write FFR group

Decode fields					Decode group or instruction page
op0	op1	op2	op3	op4	
0	00	000	-	00000	*SVE FFR write from predicate* on page C4-452
1	00	000	0000	00000	*SVE FFR initialise* on page C4-452
1	00	000	1xxx	00000	Unallocated.
1	00	000	x1xx	00000	Unallocated.
1	00	000	xx1x	00000	Unallocated.
1	00	000	xxx1	00000	Unallocated.
-	00	000	-	!= 00000	Unallocated.
-	00	!= 000	-	-	Unallocated.
-	!= 00	-	-	-	Unallocated.

SVE FFR write from predicate

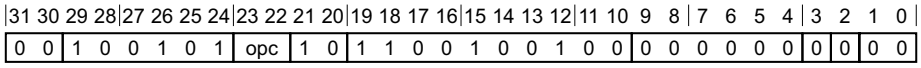
This section describes the encoding of the SVE FFR write from predicate instruction class. The encodings in this section are decoded from *SVE Write FFR*.



Decode fields	Instruction page
opc	
00	WRFFR
01	Unallocated.
1x	Unallocated.

SVE FFR initialise

This section describes the encoding of the SVE FFR initialise instruction class. The encodings in this section are decoded from *SVE Write FFR*.



Decode fields	Instruction page
opc	
00	SETFFR
01	Unallocated.
1x	Unallocated.

C4.1.39 SVE Integer Multiply-Add - Unpredicated

This section describes the encoding of the SVE Integer Multiply-Add - Unpredicated group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

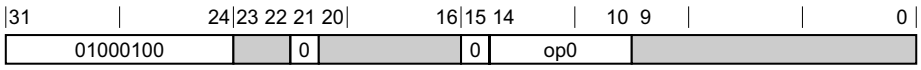
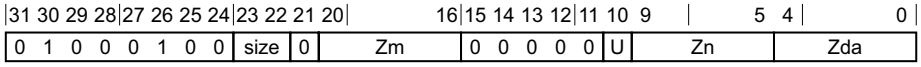


Table C4-40 Encoding table for the SVE Integer Multiply-Add - Unpredicated group

Decode fields	Decode group or instruction page
op0	
0000x	*SVE integer dot product (unpredicated)* on page C4-454
0001x	*SVE2 saturating multiply-add interleaved long* on page C4-454
001xx	CDOT (vectors)
01xxx	*SVE2 complex integer multiply-add* on page C4-454
10xxx	*SVE2 integer multiply-add long* on page C4-455
110xx	*SVE2 saturating multiply-add long* on page C4-455
1110x	*SVE2 saturating multiply-add high* on page C4-455
11110	*SVE mixed sign dot product* on page C4-456
11111	Unallocated.

SVE integer dot product (unpredicated)

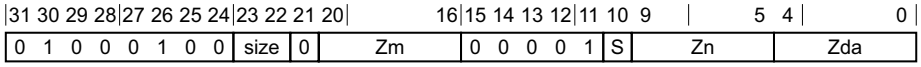
This section describes the encoding of the SVE integer dot product (unpredicated) instruction class. The encodings in this section are decoded from *SVE Integer Multiply-Add - Unpredicated* on page C4-453.



Decode fields	Instruction page
U	
0	SDOT (vectors)
1	UDOT (vectors)

SVE2 saturating multiply-add interleaved long

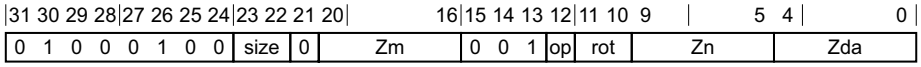
This section describes the encoding of the SVE2 saturating multiply-add interleaved long instruction class. The encodings in this section are decoded from *SVE Integer Multiply-Add - Unpredicated* on page C4-453.



Decode fields	Instruction page
S	
0	SQDMLALBT
1	SQDMLSLBT

SVE2 complex integer multiply-add

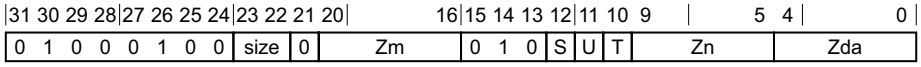
This section describes the encoding of the SVE2 complex integer multiply-add instruction class. The encodings in this section are decoded from *SVE Integer Multiply-Add - Unpredicated* on page C4-453.



Decode fields	Instruction page
op	
0	CMLA (vectors)
1	SQRDCMLAH (vectors)

SVE2 integer multiply-add long

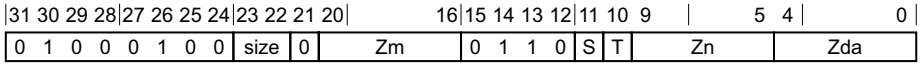
This section describes the encoding of the SVE2 integer multiply-add long instruction class. The encodings in this section are decoded from *SVE Integer Multiply-Add - Unpredicated* on page C4-453.



Decode fields			Instruction page
S	U	T	
0	0	0	SMLALB (vectors)
0	0	1	SMLALT (vectors)
0	1	0	UMLALB (vectors)
0	1	1	UMLALT (vectors)
1	0	0	SMLSLB (vectors)
1	0	1	SMLSLT (vectors)
1	1	0	UMLSLB (vectors)
1	1	1	UMLSLT (vectors)

SVE2 saturating multiply-add long

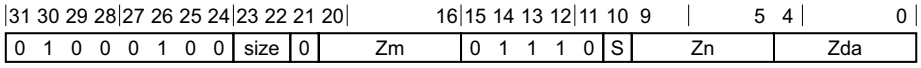
This section describes the encoding of the SVE2 saturating multiply-add long instruction class. The encodings in this section are decoded from *SVE Integer Multiply-Add - Unpredicated* on page C4-453.



Decode fields		Instruction page
S	T	
0	0	SQDMLALB (vectors)
0	1	SQDMLALT (vectors)
1	0	SQDMLSLB (vectors)
1	1	SQDMLSLT (vectors)

SVE2 saturating multiply-add high

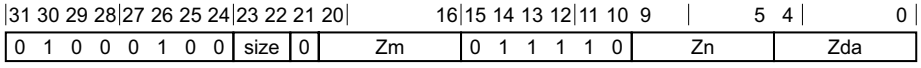
This section describes the encoding of the SVE2 saturating multiply-add high instruction class. The encodings in this section are decoded from *SVE Integer Multiply-Add - Unpredicated* on page C4-453.



Decode fields	Instruction page
S	
0	SQRDMLAH (vectors)
1	SQRDMLSH (vectors)

SVE mixed sign dot product

This section describes the encoding of the SVE mixed sign dot product instruction class. The encodings in this section are decoded from *SVE Integer Multiply-Add - Unpredicated* on page C4-453.



Decode fields	Instruction page	Feature
size		
0x	Unallocated.	-
10	USDOT (vectors)	FEAT_I8MM
11	Unallocated.	-

C4.1.40 SVE2 Integer - Predicated

This section describes the encoding of the SVE2 Integer - Predicated group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

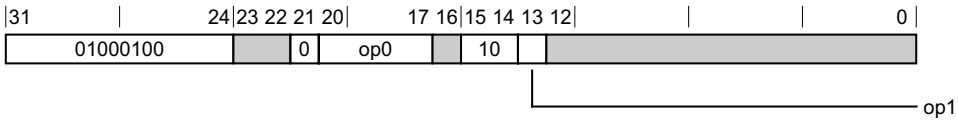


Table C4-41 Encoding table for the SVE2 Integer - Predicated group

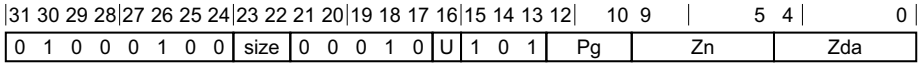
Decode fields		Decode group or instruction page
op0	op1	
0010	1	*SVE2 integer pairwise add and accumulate long* on page C4-457
0011	1	Unallocated.
011x	1	Unallocated.
0x0x	1	*SVE2 integer unary operations (predicated)* on page C4-457

Table C4-41 Encoding table for the SVE2 Integer - Predicated group (continued)

Decode fields		Decode group or instruction page
op0	op1	
0xxx	0	*SVE2 saturating/rounding bitwise shift left (predicated)* on page C4-458
10xx	0	*SVE2 integer halving add/subtract (predicated)* on page C4-458
10xx	1	*SVE2 integer pairwise arithmetic* on page C4-459
11xx	0	*SVE2 saturating add/subtract* on page C4-459
11xx	1	Unallocated.

SVE2 integer pairwise add and accumulate long

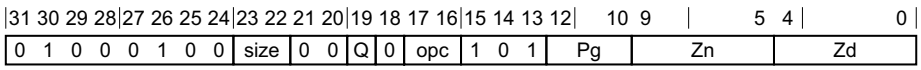
This section describes the encoding of the SVE2 integer pairwise add and accumulate long instruction class. The encodings in this section are decoded from *SVE2 Integer - Predicated* on page C4-456.



Decode fields	Instruction page
U	
0	SADALP
1	UADALP

SVE2 integer unary operations (predicated)

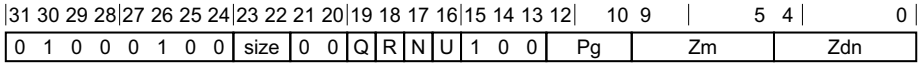
This section describes the encoding of the SVE2 integer unary operations (predicated) instruction class. The encodings in this section are decoded from *SVE2 Integer - Predicated* on page C4-456.



Decode fields		Instruction page
Q	opc	
-	1x	Unallocated.
0	00	URECPE
0	01	URSQRTE
1	00	SQABS
1	01	SQNEG

SVE2 saturating/rounding bitwise shift left (predicated)

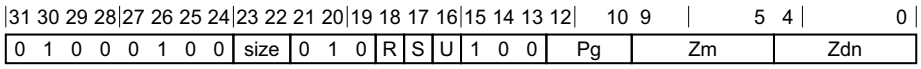
This section describes the encoding of the SVE2 saturating/rounding bitwise shift left (predicated) instruction class. The encodings in this section are decoded from *SVE2 Integer - Predicated* on page C4-456.



Decode fields				Instruction page
Q	R	N	U	
0	-	0	-	Unallocated.
0	0	1	0	SRSHL
0	0	1	1	URSHL
0	1	1	0	SRSHLR
0	1	1	1	URSHLR
1	0	0	0	SQSHL (vectors)
1	0	0	1	UQSHL (vectors)
1	0	1	0	SQRSHL
1	0	1	1	UQRSHL
1	1	0	0	SQSHLR
1	1	0	1	UQSHLR
1	1	1	0	SQRSHLR
1	1	1	1	UQRSHLR

SVE2 integer halving add/subtract (predicated)

This section describes the encoding of the SVE2 integer halving add/subtract (predicated) instruction class. The encodings in this section are decoded from *SVE2 Integer - Predicated* on page C4-456.

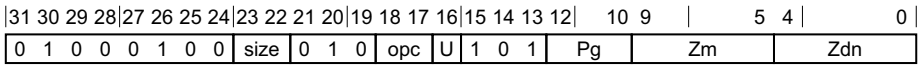


Decode fields			Instruction page
R	S	U	
0	0	0	SHADD
0	0	1	UHADD
0	1	0	SHSUB
0	1	1	UHSUB

Decode fields			Instruction page
R	S	U	
1	0	0	SRHADD
1	0	1	URHADD
1	1	0	SHSUBR
1	1	1	UHSUBR

SVE2 integer pairwise arithmetic

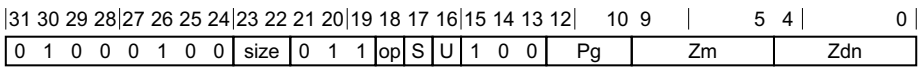
This section describes the encoding of the SVE2 integer pairwise arithmetic instruction class. The encodings in this section are decoded from *SVE2 Integer - Predicated* on page C4-456.



Decode fields		Instruction page
opc	U	
00	0	Unallocated.
00	1	ADDP
01	-	Unallocated.
10	0	SMAXP
10	1	UMAXP
11	0	SMINP
11	1	UMINP

SVE2 saturating add/subtract

This section describes the encoding of the SVE2 saturating add/subtract instruction class. The encodings in this section are decoded from *SVE2 Integer - Predicated* on page C4-456.



Decode fields			Instruction page
op	S	U	
0	0	0	SQADD (vectors, predicated)
0	0	1	UQADD (vectors, predicated)
0	1	0	SQSUB (vectors, predicated)

Decode fields			Instruction page
op	S	U	
0	1	1	UQSUB (vectors, predicated)
1	0	0	SUQADD
1	0	1	USQADD
1	1	0	SQSUBR
1	1	1	UQSUBR

C4.1.41 SVE Multiply - Indexed

This section describes the encoding of the SVE Multiply - Indexed group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

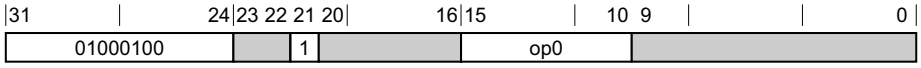
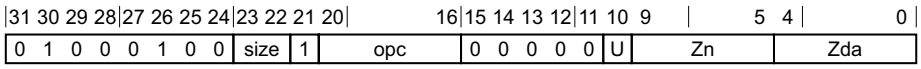


Table C4-42 Encoding table for the SVE Multiply - Indexed group

Decode fields	Decode group or instruction page
op0	
00000x	*SVE integer dot product (indexed)* on page C4-461
00001x	*SVE2 integer multiply-add (indexed)* on page C4-461
00010x	*SVE2 saturating multiply-add high (indexed)* on page C4-462
00011x	*SVE mixed sign dot product (indexed)* on page C4-462
001xxx	*SVE2 saturating multiply-add (indexed)* on page C4-463
0100xx	*SVE2 complex integer dot product (indexed)* on page C4-463
0101xx	Unallocated.
0110xx	*SVE2 complex integer multiply-add (indexed)* on page C4-464
0111xx	*SVE2 complex saturating multiply-add (indexed)* on page C4-464
10xxxx	*SVE2 integer multiply-add long (indexed)* on page C4-464
110xxx	*SVE2 integer multiply long (indexed)* on page C4-465
1110xx	*SVE2 saturating multiply (indexed)* on page C4-466
11110x	*SVE2 saturating multiply high (indexed)* on page C4-467
111110	*SVE2 integer multiply (indexed)* on page C4-467
111111	Unallocated.

SVE integer dot product (indexed)

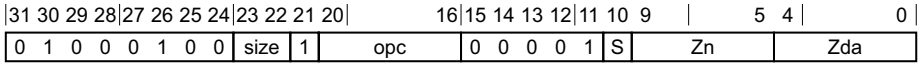
This section describes the encoding of the SVE integer dot product (indexed) instruction class. The encodings in this section are decoded from *SVE Multiply - Indexed* on page C4-460.



Decode fields		Instruction page
size	U	
0x	-	Unallocated.
10	0	SDOT (indexed) - Encoding
10	1	UDOT (indexed) - Encoding
11	0	SDOT (indexed) - Encoding
11	1	UDOT (indexed) - Encoding

SVE2 integer multiply-add (indexed)

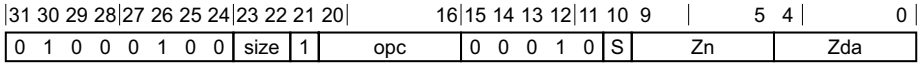
This section describes the encoding of the SVE2 integer multiply-add (indexed) instruction class. The encodings in this section are decoded from *SVE Multiply - Indexed* on page C4-460.



Decode fields		Instruction page
size	S	
0x	0	MLA (indexed) - Encoding
0x	1	MLS (indexed) - Encoding
10	0	MLA (indexed) - Encoding
10	1	MLS (indexed) - Encoding
11	0	MLA (indexed) - Encoding
11	1	MLS (indexed) - Encoding

SVE2 saturating multiply-add high (indexed)

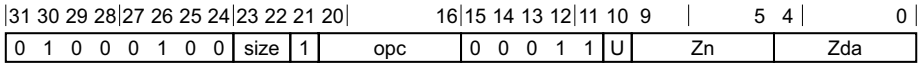
This section describes the encoding of the SVE2 saturating multiply-add high (indexed) instruction class. The encodings in this section are decoded from *SVE Multiply - Indexed* on page C4-460.



Decode fields		Instruction page
size	S	
0x	0	SQRDMLAH (indexed) - Encoding
0x	1	SQRDMLSH (indexed) - Encoding
10	0	SQRDMLAH (indexed) - Encoding
10	1	SQRDMLSH (indexed) - Encoding
11	0	SQRDMLAH (indexed) - Encoding
11	1	SQRDMLSH (indexed) - Encoding

SVE mixed sign dot product (indexed)

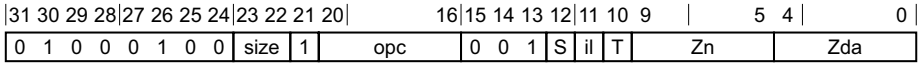
This section describes the encoding of the SVE mixed sign dot product (indexed) instruction class. The encodings in this section are decoded from *SVE Multiply - Indexed* on page C4-460.



Decode fields		Instruction page	Feature
size	U		
0x	-	Unallocated.	-
10	0	USDOT (indexed)	FEAT_I8MM
10	1	SUDOT	FEAT_I8MM
11	-	Unallocated.	-

SVE2 saturating multiply-add (indexed)

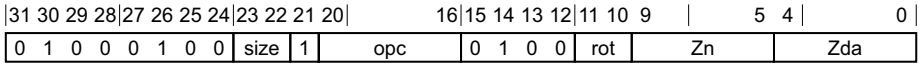
This section describes the encoding of the SVE2 saturating multiply-add (indexed) instruction class. The encodings in this section are decoded from *SVE Multiply - Indexed* on page C4-460.



Decode fields			Instruction page
size	S	T	
0x	-	-	Unallocated.
10	0	0	SQDMLALB (indexed) - Encoding
10	0	1	SQDMLALT (indexed) - Encoding
10	1	0	SQDMLSLB (indexed) - Encoding
10	1	1	SQDMLSLT (indexed) - Encoding
11	0	0	SQDMLALB (indexed) - Encoding
11	0	1	SQDMLALT (indexed) - Encoding
11	1	0	SQDMLSLB (indexed) - Encoding
11	1	1	SQDMLSLT (indexed) - Encoding

SVE2 complex integer dot product (indexed)

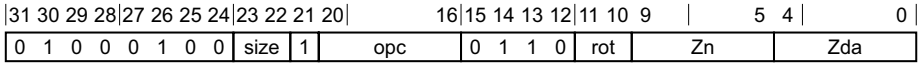
This section describes the encoding of the SVE2 complex integer dot product (indexed) instruction class. The encodings in this section are decoded from *SVE Multiply - Indexed* on page C4-460.



Decode fields	Instruction page
size	
0x	Unallocated.
10	CDOT (indexed) - Encoding
11	CDOT (indexed) - Encoding

SVE2 complex integer multiply-add (indexed)

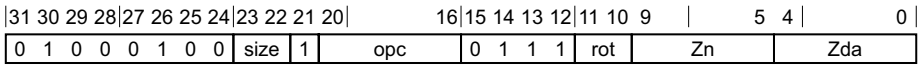
This section describes the encoding of the SVE2 complex integer multiply-add (indexed) instruction class. The encodings in this section are decoded from *SVE Multiply - Indexed* on page C4-460.



Decode fields	Instruction page
size	
0x	Unallocated.
10	CMLA (indexed) - Encoding
11	CMLA (indexed) - Encoding

SVE2 complex saturating multiply-add (indexed)

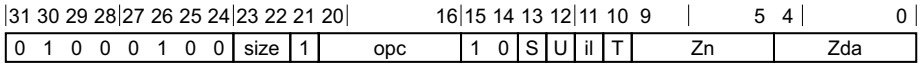
This section describes the encoding of the SVE2 complex saturating multiply-add (indexed) instruction class. The encodings in this section are decoded from *SVE Multiply - Indexed* on page C4-460.



Decode fields	Instruction page
size	
0x	Unallocated.
10	SQRDCMLAH (indexed) - Encoding
11	SQRDCMLAH (indexed) - Encoding

SVE2 integer multiply-add long (indexed)

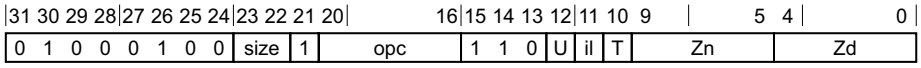
This section describes the encoding of the SVE2 integer multiply-add long (indexed) instruction class. The encodings in this section are decoded from *SVE Multiply - Indexed* on page C4-460.



Decode fields				Instruction page
size	S	U	T	
0x	-	-	-	Unallocated.
10	0	0	0	SMLALB (indexed) - Encoding
10	0	0	1	SMLALT (indexed) - Encoding
10	0	1	0	UMLALB (indexed) - Encoding
10	0	1	1	UMLALT (indexed) - Encoding
10	1	0	0	SMLSLB (indexed) - Encoding
10	1	0	1	SMLSLT (indexed) - Encoding
10	1	1	0	UMLSLB (indexed) - Encoding
10	1	1	1	UMLSLT (indexed) - Encoding
11	0	0	0	SMLALB (indexed) - Encoding
11	0	0	1	SMLALT (indexed) - Encoding
11	0	1	0	UMLALB (indexed) - Encoding
11	0	1	1	UMLALT (indexed) - Encoding
11	1	0	0	SMLSLB (indexed) - Encoding
11	1	0	1	SMLSLT (indexed) - Encoding
11	1	1	0	UMLSLB (indexed) - Encoding
11	1	1	1	UMLSLT (indexed) - Encoding

SVE2 integer multiply long (indexed)

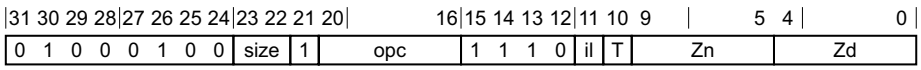
This section describes the encoding of the SVE2 integer multiply long (indexed) instruction class. The encodings in this section are decoded from *SVE Multiply - Indexed* on page C4-460.



Decode fields			Instruction page
size	U	T	
0x	-	-	Unallocated.
10	0	0	SMULLB (indexed) - Encoding
10	0	1	SMULLT (indexed) - Encoding
10	1	0	UMULLB (indexed) - Encoding
10	1	1	UMULLT (indexed) - Encoding
11	0	0	SMULLB (indexed) - Encoding
11	0	1	SMULLT (indexed) - Encoding
11	1	0	UMULLB (indexed) - Encoding
11	1	1	UMULLT (indexed) - Encoding

SVE2 saturating multiply (indexed)

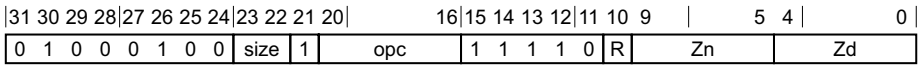
This section describes the encoding of the SVE2 saturating multiply (indexed) instruction class. The encodings in this section are decoded from *SVE Multiply - Indexed* on page C4-460.



Decode fields		Instruction page
size	T	
0x	-	Unallocated.
10	0	SQDMULLB (indexed) - Encoding
10	1	SQDMULLT (indexed) - Encoding
11	0	SQDMULLB (indexed) - Encoding
11	1	SQDMULLT (indexed) - Encoding

SVE2 saturating multiply high (indexed)

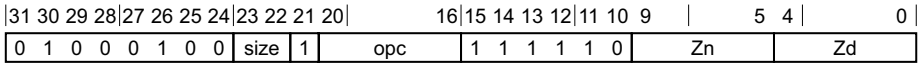
This section describes the encoding of the SVE2 saturating multiply high (indexed) instruction class. The encodings in this section are decoded from *SVE Multiply - Indexed* on page C4-460.



Decode fields		Instruction page
size	R	
0x	0	SQDMULH (indexed) - Encoding
0x	1	SQRDMULH (indexed) - Encoding
10	0	SQDMULH (indexed) - Encoding
10	1	SQRDMULH (indexed) - Encoding
11	0	SQDMULH (indexed) - Encoding
11	1	SQRDMULH (indexed) - Encoding

SVE2 integer multiply (indexed)

This section describes the encoding of the SVE2 integer multiply (indexed) instruction class. The encodings in this section are decoded from *SVE Multiply - Indexed* on page C4-460.



Decode fields	Instruction page
size	
0x	MUL (indexed) - Encoding
10	MUL (indexed) - Encoding
11	MUL (indexed) - Encoding

C4.1.42 SVE2 Widening Integer Arithmetic

This section describes the encoding of the SVE2 Widening Integer Arithmetic group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

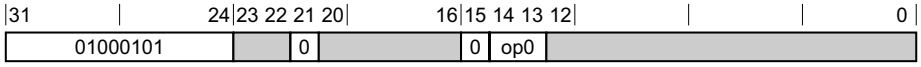
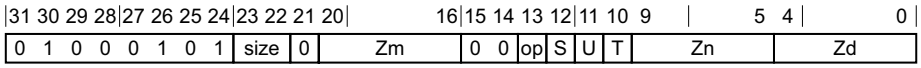


Table C4-43 Encoding table for the SVE2 Widening Integer Arithmetic group

Decode fields	Decode group or instruction page
op0	
0x	*SVE2 integer add/subtract long* on page C4-468
10	*SVE2 integer add/subtract wide* on page C4-469
11	*SVE2 integer multiply long* on page C4-469

SVE2 integer add/subtract long

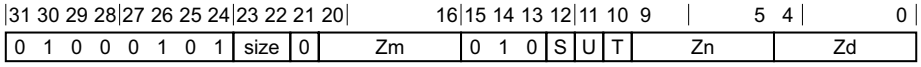
This section describes the encoding of the SVE2 integer add/subtract long instruction class. The encodings in this section are decoded from *SVE2 Widening Integer Arithmetic*.



Decode fields				Instruction page
op	S	U	T	
0	0	0	0	SADDLB
0	0	0	1	SADDLT
0	0	1	0	UADDLB
0	0	1	1	UADDLT
0	1	0	0	SSUBLB
0	1	0	1	SSUBLT
0	1	1	0	USUBLB
0	1	1	1	USUBLT
1	0	-	-	Unallocated.
1	1	0	0	SABDLB
1	1	0	1	SABDLT
1	1	1	0	UABDLB
1	1	1	1	UABDLT

SVE2 integer add/subtract wide

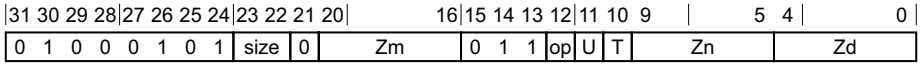
This section describes the encoding of the SVE2 integer add/subtract wide instruction class. The encodings in this section are decoded from *SVE2 Widening Integer Arithmetic* on page C4-468.



Decode fields			Instruction page
S	U	T	
0	0	0	SADDWB
0	0	1	SADDWT
0	1	0	UADDWB
0	1	1	UADDWT
1	0	0	SSUBWB
1	0	1	SSUBWT
1	1	0	USUBWB
1	1	1	USUBWT

SVE2 integer multiply long

This section describes the encoding of the SVE2 integer multiply long instruction class. The encodings in this section are decoded from *SVE2 Widening Integer Arithmetic* on page C4-468.



Decode fields			Instruction page
op	U	T	
0	0	0	SQDMULLB (vectors)
0	0	1	SQDMULLT (vectors)
0	1	0	PMULLB
0	1	1	PMULLT
1	0	0	SMULLB (vectors)
1	0	1	SMULLT (vectors)
1	1	0	UMULLB (vectors)
1	1	1	UMULLT (vectors)

C4.1.43 SVE Misc

This section describes the encoding of the SVE Misc group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

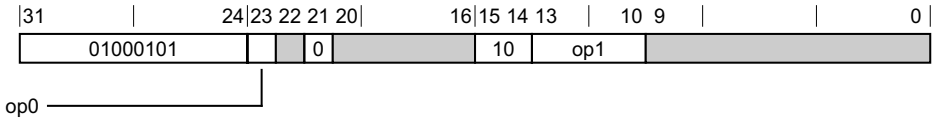
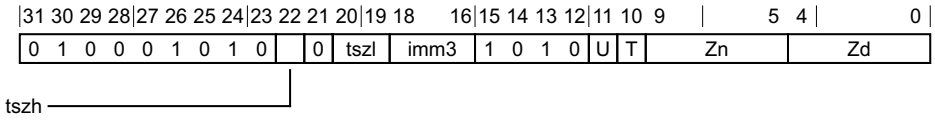


Table C4-44 Encoding table for the SVE Misc group

Decode fields		Decode group or instruction page
op0	op1	
0	10xx	*SVE2 bitwise shift left long* on page C4-470
1	10xx	Unallocated.
-	00xx	*SVE2 integer add/subtract interleaved long* on page C4-470
-	010x	*SVE2 bitwise exclusive-or interleaved* on page C4-471
-	0110	*SVE integer matrix multiply accumulate* on page C4-471
-	0111	Unallocated.
-	11xx	*SVE2 bitwise permute* on page C4-472

SVE2 bitwise shift left long

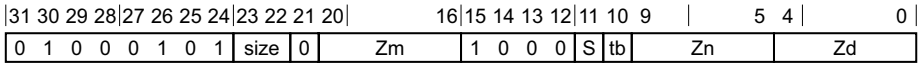
This section describes the encoding of the SVE2 bitwise shift left long instruction class. The encodings in this section are decoded from *SVE Misc*.



Decode fields		Instruction page
U	T	
0	0	SSHLLB
0	1	SSHLLT
1	0	USHLLB
1	1	USHLLT

SVE2 integer add/subtract interleaved long

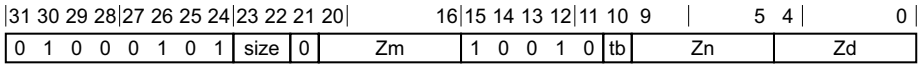
This section describes the encoding of the SVE2 integer add/subtract interleaved long instruction class. The encodings in this section are decoded from *SVE Misc*.



Decode fields		Instruction page
S	tb	
0	0	SADDLBT
0	1	Unallocated.
1	0	SSUBLBT
1	1	SSUBLTB

SVE2 bitwise exclusive-or interleaved

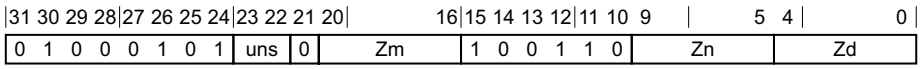
This section describes the encoding of the SVE2 bitwise exclusive-or interleaved instruction class. The encodings in this section are decoded from *SVE Misc* on page C4-470.



Decode fields	Instruction page
tb	
0	EORBT
1	EORTB

SVE integer matrix multiply accumulate

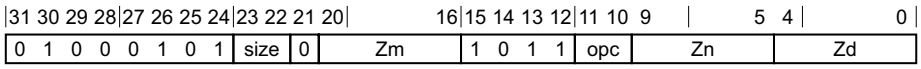
This section describes the encoding of the SVE integer matrix multiply accumulate instruction class. The encodings in this section are decoded from *SVE Misc* on page C4-470.



Decode fields	Instruction page	Feature
uns		
00	SMMLA	FEAT_I8MM
01	Unallocated.	-
10	USMMLA	FEAT_I8MM
11	UMMLA	FEAT_I8MM

SVE2 bitwise permute

This section describes the encoding of the SVE2 bitwise permute instruction class. The encodings in this section are decoded from *SVE Misc* on page C4-470.



Decode fields	Instruction page	Feature
opc		
00	BEXT	FEAT_SVE_BitPerm
01	BDEP	FEAT_SVE_BitPerm
10	BGRP	FEAT_SVE_BitPerm
11	Unallocated.	-

C4.1.44 SVE2 Accumulate

This section describes the encoding of the SVE2 Accumulate group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

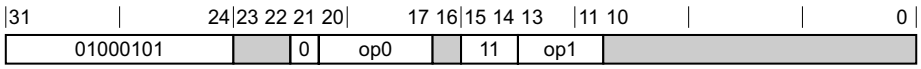
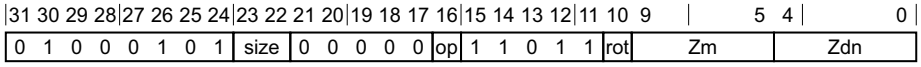


Table C4-45 Encoding table for the SVE2 Accumulate group

Decode fields		Decode group or instruction page
op0	op1	
0000	011	*SVE2 complex integer add* on page C4-473
!= 0000	011	Unallocated.
-	00x	*SVE2 integer absolute difference and accumulate long* on page C4-473
-	010	*SVE2 integer add/subtract long with carry* on page C4-473
-	10x	*SVE2 bitwise shift right and accumulate* on page C4-474
-	110	*SVE2 bitwise shift and insert* on page C4-474
-	111	*SVE2 integer absolute difference and accumulate* on page C4-475

SVE2 complex integer add

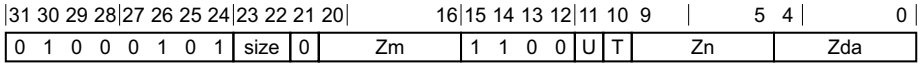
This section describes the encoding of the SVE2 complex integer add instruction class. The encodings in this section are decoded from *SVE2 Accumulate* on page C4-472.



Decode fields	Instruction page
op	
0	CADD
1	SQCADD

SVE2 integer absolute difference and accumulate long

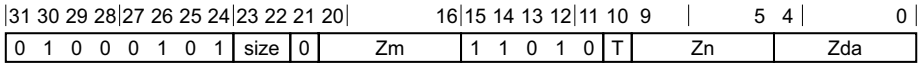
This section describes the encoding of the SVE2 integer absolute difference and accumulate long instruction class. The encodings in this section are decoded from *SVE2 Accumulate* on page C4-472.



Decode fields		Instruction page
U	T	
0	0	SABALB
0	1	SABALT
1	0	UABALB
1	1	UABALT

SVE2 integer add/subtract long with carry

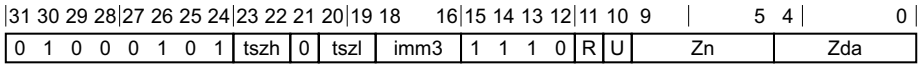
This section describes the encoding of the SVE2 integer add/subtract long with carry instruction class. The encodings in this section are decoded from *SVE2 Accumulate* on page C4-472.



Decode fields		Instruction page
size	T	
0x	0	ADCLB
0x	1	ADCLT
1x	0	SBCLB
1x	1	SBCLT

SVE2 bitwise shift right and accumulate

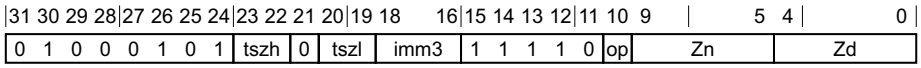
This section describes the encoding of the SVE2 bitwise shift right and accumulate instruction class. The encodings in this section are decoded from *SVE2 Accumulate* on page C4-472.



Decode fields		Instruction page
R	U	
0	0	SSRA
0	1	USRA
1	0	SRSRA
1	1	URSRA

SVE2 bitwise shift and insert

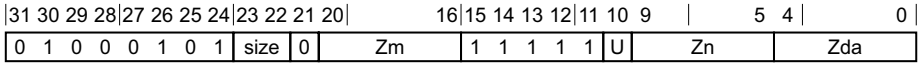
This section describes the encoding of the SVE2 bitwise shift and insert instruction class. The encodings in this section are decoded from *SVE2 Accumulate* on page C4-472.



Decode fields	Instruction page
op	
0	SRI
1	SLI

SVE2 integer absolute difference and accumulate

This section describes the encoding of the SVE2 integer absolute difference and accumulate instruction class. The encodings in this section are decoded from *SVE2 Accumulate* on page C4-472.



Decode fields	Instruction page
U	
0	SABA
1	UABA

C4.1.45 SVE2 Narrowing

This section describes the encoding of the SVE2 Narrowing group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

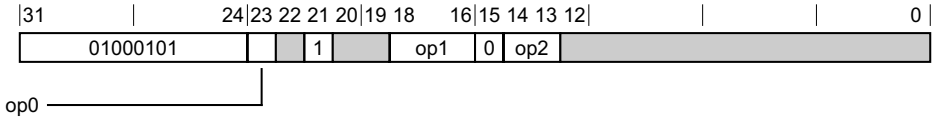
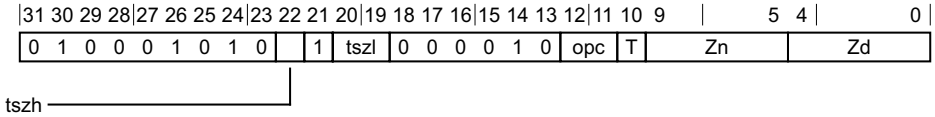


Table C4-46 Encoding table for the SVE2 Narrowing group

Decode fields			Decode group or instruction page
op0	op1	op2	
0	000	10	*SVE2 saturating extract narrow* on page C4-475
0	!= 000	10	Unallocated.
0	-	0x	*SVE2 bitwise shift right narrow* on page C4-476
1	-	0x	Unallocated.
1	-	10	Unallocated.
-	-	11	*SVE2 integer add/subtract narrow high part* on page C4-477

SVE2 saturating extract narrow

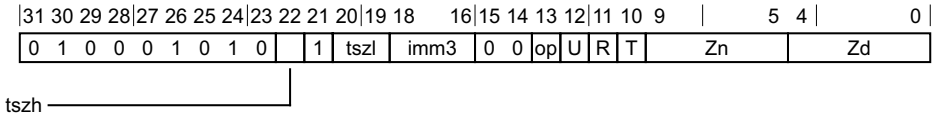
This section describes the encoding of the SVE2 saturating extract narrow instruction class. The encodings in this section are decoded from *SVE2 Narrowing*.



Decode fields		Instruction page
opc	T	
00	0	SQXTNB
00	1	SQXTNT
01	0	UQXTNB
01	1	UQXTNT
10	0	SQXTUNB
10	1	SQXTUNT
11	-	Unallocated.

SVE2 bitwise shift right narrow

This section describes the encoding of the SVE2 bitwise shift right narrow instruction class. The encodings in this section are decoded from *SVE2 Narrowing* on page C4-475.

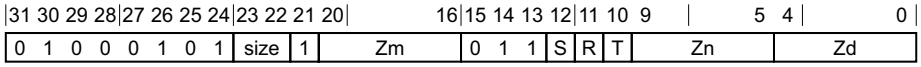


Decode fields				Instruction page
op	U	R	T	
0	0	0	0	SQSHRUNB
0	0	0	1	SQSHRUNT
0	0	1	0	SQRSHRUNB
0	0	1	1	SQRSHRUNT
0	1	0	0	SHRNB
0	1	0	1	SHRNT
0	1	1	0	RSHRNB
0	1	1	1	RSHRNT
1	0	0	0	SQSHRNB
1	0	0	1	SQSHRNT
1	0	1	0	SQRSHRNB

Decode fields				Instruction page
op	U	R	T	
1	0	1	1	SQRSHRNT
1	1	0	0	UQSHRNB
1	1	0	1	UQSHRNT
1	1	1	0	UQRSHRNB
1	1	1	1	UQRSHRNT

SVE2 integer add/subtract narrow high part

This section describes the encoding of the SVE2 integer add/subtract narrow high part instruction class. The encodings in this section are decoded from *SVE2 Narrowing* on page C4-475.



Decode fields			Instruction page
S	R	T	
0	0	0	ADDHNB
0	0	1	ADDHNT
0	1	0	RADDHNB
0	1	1	RADDHNT
1	0	0	SUBHNB
1	0	1	SUBHNT
1	1	0	RSUBHNB
1	1	1	RSUBHNT

C4.1.46 SVE2 Histogram Computation - Segment

This section describes the encoding of the SVE2 Histogram Computation - Segment group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

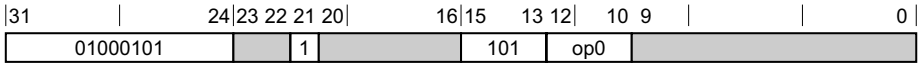


Table C4-47 Encoding table for the SVE2 Histogram Computation - Segment group

Decode fields	Decode group or instruction page
op0	
000	HISTSEG
!= 000	Unallocated.

C4.1.47 SVE2 Crypto Extensions

This section describes the encoding of the SVE2 Crypto Extensions group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

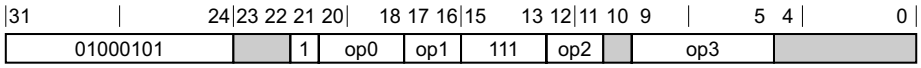
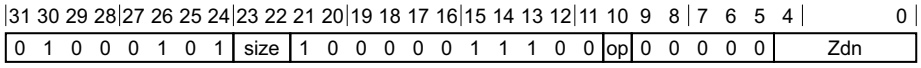


Table C4-48 Encoding table for the SVE2 Crypto Extensions group

Decode fields				Decode group or instruction page
op0	op1	op2	op3	
000	00	00	00000	*SVE2 crypto unary operations* on page C4-478
000	00	00	!= 00000	Unallocated.
000	00	x1	-	Unallocated.
000	01	0x	-	Unallocated.
000	01	11	-	Unallocated.
000	1x	00	-	*SVE2 crypto destructive binary operations* on page C4-479
000	1x	x1	-	Unallocated.
!= 000	-	0x	-	Unallocated.
!= 000	-	11	-	Unallocated.
-	-	10	-	*SVE2 crypto constructive binary operations* on page C4-479

SVE2 crypto unary operations

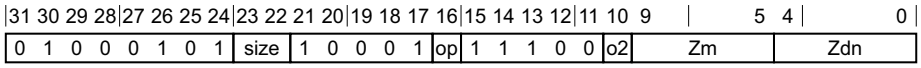
This section describes the encoding of the SVE2 crypto unary operations instruction class. The encodings in this section are decoded from *SVE2 Crypto Extensions*.



Decode fields		Instruction page	Feature
size	op		
00	0	AESMC	FEAT_SVE_AES
00	1	AESIMC	FEAT_SVE_AES
01	-	Unallocated.	-
1x	-	Unallocated.	-

SVE2 crypto destructive binary operations

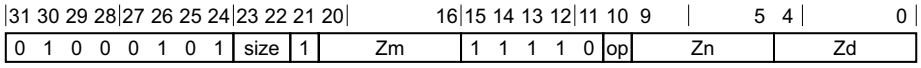
This section describes the encoding of the SVE2 crypto destructive binary operations instruction class. The encodings in this section are decoded from *SVE2 Crypto Extensions* on page C4-478.



Decode fields			Instruction page	Feature
size	op	o2		
00	0	0	AESE	FEAT_SVE_AES
00	0	1	AESD	FEAT_SVE_AES
00	1	0	SM4E	FEAT_SVE_SM4
00	1	1	Unallocated.	-
01	-	-	Unallocated.	-
1x	-	-	Unallocated.	-

SVE2 crypto constructive binary operations

This section describes the encoding of the SVE2 crypto constructive binary operations instruction class. The encodings in this section are decoded from *SVE2 Crypto Extensions* on page C4-478.



Decode fields		Instruction page	Feature
size	op		
00	0	SM4EKEY	FEAT_SVE_SM4
00	1	RAX1	FEAT_SVE_SHA3
01	-	Unallocated.	-
1x	-	Unallocated.	-

C4.1.48 SVE Floating Point Widening Multiply-Add - Indexed

This section describes the encoding of the SVE Floating Point Widening Multiply-Add - Indexed group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

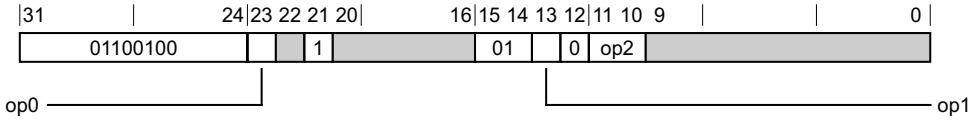
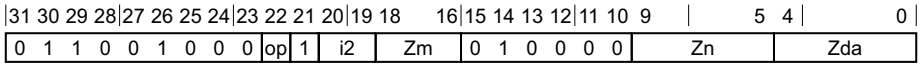


Table C4-49 Encoding table for the SVE Floating Point Widening Multiply-Add - Indexed group

Decode fields			Decode group or instruction page
op0	op1	op2	
0	0	00	*SVE BFloat16 floating-point dot product (indexed)* on page C4-480
0	0	!= 00	Unallocated.
0	1	-	Unallocated.
1	-	-	*SVE floating-point multiply-add long (indexed)* on page C4-481

SVE BFloat16 floating-point dot product (indexed)

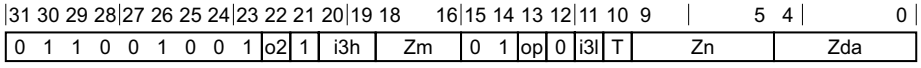
This section describes the encoding of the SVE BFloat16 floating-point dot product (indexed) instruction class. The encodings in this section are decoded from *SVE Floating Point Widening Multiply-Add - Indexed*.



Decode fields	Instruction page	Feature
op		
0	Unallocated.	-
1	BFDOT (indexed)	FEAT_BF16

SVE floating-point multiply-add long (indexed)

This section describes the encoding of the SVE floating-point multiply-add long (indexed) instruction class. The encodings in this section are decoded from *SVE Floating Point Widening Multiply-Add - Indexed* on page C4-480.



Decode fields			Instruction page	Feature
o2	op	T		
0	0	0	FMLALB (indexed)	-
0	0	1	FMLALT (indexed)	-
0	1	0	FMLSLB (indexed)	-
0	1	1	FMLSLT (indexed)	-
1	0	0	BFMLALB (indexed)	FEAT_BF16
1	0	1	BFMLALT (indexed)	FEAT_BF16
1	1	-	Unallocated.	-

C4.1.49 SVE Floating Point Widening Multiply-Add

This section describes the encoding of the SVE Floating Point Widening Multiply-Add group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

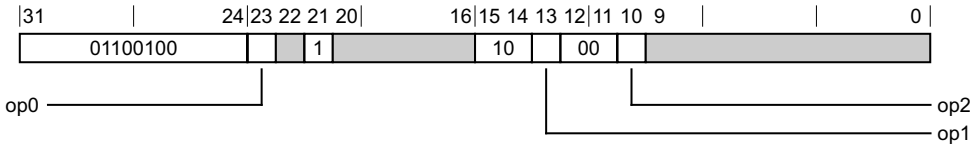
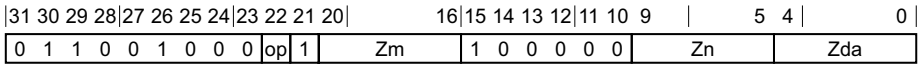


Table C4-50 Encoding table for the SVE Floating Point Widening Multiply-Add group

Decode fields			Decode group or instruction page
op0	op1	op2	
0	0	0	*SVE BFloat16 floating-point dot product*
0	0	1	Unallocated.
0	1	-	Unallocated.
1	-	-	*SVE floating-point multiply-add long*

SVE BFloat16 floating-point dot product

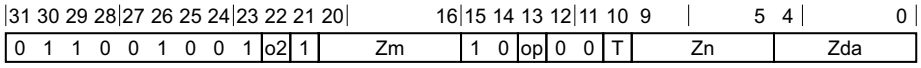
This section describes the encoding of the SVE BFloat16 floating-point dot product instruction class. The encodings in this section are decoded from *SVE Floating Point Widening Multiply-Add* on page C4-481.



Decode fields	Instruction page	Feature
op		
0	Unallocated.	-
1	BFDOT (vectors)	FEAT_BF16

SVE floating-point multiply-add long

This section describes the encoding of the SVE floating-point multiply-add long instruction class. The encodings in this section are decoded from *SVE Floating Point Widening Multiply-Add* on page C4-481.



Decode fields			Instruction page	Feature
o2	op	T		
0	0	0	FMLALB (vectors)	-
0	0	1	FMLALT (vectors)	-
0	1	0	FMLSLB (vectors)	-
0	1	1	FMLSLT (vectors)	-
1	0	0	BFMLALB (vectors)	FEAT_BF16
1	0	1	BFMLALT (vectors)	FEAT_BF16
1	1	-	Unallocated.	-

C4.1.50 SVE Floating Point Arithmetic - Predicated

This section describes the encoding of the SVE Floating Point Arithmetic - Predicated group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

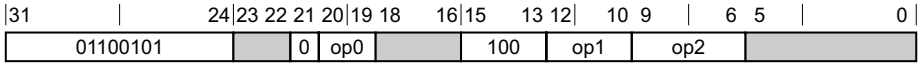
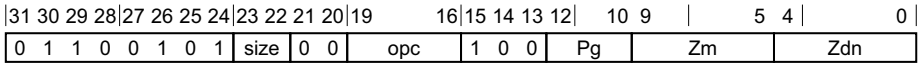


Table C4-51 Encoding table for the SVE Floating Point Arithmetic - Predicated group

Decode fields			Decode group or instruction page
op0	op1	op2	
0x	-	-	*SVE floating-point arithmetic (predicated)* on page C4-483
10	000	-	FTMAD
10	!= 000	-	Unallocated.
11	-	0000	*SVE floating-point arithmetic with immediate (predicated)* on page C4-484
11	-	!= 0000	Unallocated.

SVE floating-point arithmetic (predicated)

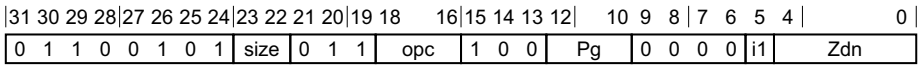
This section describes the encoding of the SVE floating-point arithmetic (predicated) instruction class. The encodings in this section are decoded from *SVE Floating Point Arithmetic - Predicated*.



Decode fields	Instruction page
opc	
0000	FADD (vectors, predicated)
0001	FSUB (vectors, predicated)
0010	FMUL (vectors, predicated)
0011	FSUBR (vectors)
0100	FMAXNM (vectors)
0101	FMINNM (vectors)
0110	FMAX (vectors)
0111	FMIN (vectors)
1000	FABD
1001	FSCALE
1010	FMULX
1011	Unallocated.
1100	FDIVR
1101	FDIV
111x	Unallocated.

SVE floating-point arithmetic with immediate (predicated)

This section describes the encoding of the SVE floating-point arithmetic with immediate (predicated) instruction class. The encodings in this section are decoded from *SVE Floating Point Arithmetic - Predicated* on page C4-483.



Decode fields	Instruction page
opc	
000	FADD (immediate)
001	FSUB (immediate)
010	FMUL (immediate)
011	FSUBR (immediate)

Decode fields	Instruction page
opc	
100	FMAXNM (immediate)
101	FMINNM (immediate)
110	FMAX (immediate)
111	FMIN (immediate)

C4.1.51 SVE Floating Point Unary Operations - Predicated

This section describes the encoding of the SVE Floating Point Unary Operations - Predicated group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

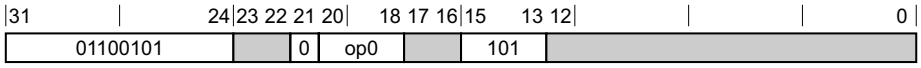
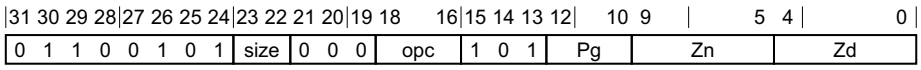


Table C4-52 Encoding table for the SVE Floating Point Unary Operations - Predicated group

Decode fields	Decode group or instruction page
op0	
00x	*SVE floating-point round to integral value* on page C4-485
010	*SVE floating-point convert precision* on page C4-486
011	*SVE floating-point unary operations* on page C4-486
10x	*SVE integer convert to floating-point* on page C4-487
11x	*SVE floating-point convert to integer* on page C4-488

SVE floating-point round to integral value

This section describes the encoding of the SVE floating-point round to integral value instruction class. The encodings in this section are decoded from *SVE Floating Point Unary Operations - Predicated*.

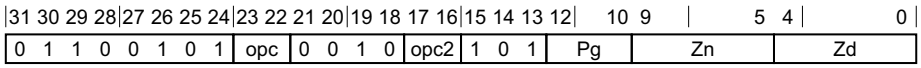


Decode fields	Instruction page
opc	
000	FRINT<r> - Encoding
001	FRINT<r> - Encoding
010	FRINT<r> - Encoding
011	FRINT<r> - Encoding

Decode fields	Instruction page
opc	
100	FRINT<r> - Encoding
101	Unallocated.
110	FRINT<r> - Encoding
111	FRINT<r> - Encoding

SVE floating-point convert precision

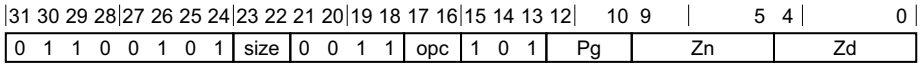
This section describes the encoding of the SVE floating-point convert precision instruction class. The encodings in this section are decoded from *SVE Floating Point Unary Operations - Predicated* on page C4-485.



Decode fields		Instruction page	Feature
opc	opc2		
x0	11	Unallocated.	-
00	0x	Unallocated.	-
00	10	FCVTX	-
01	-	Unallocated.	-
10	00	FCVT - Encoding	-
10	01	FCVT - Encoding	-
10	10	BFCVT	FEAT_BF16
11	00	FCVT - Encoding	-
11	01	FCVT - Encoding	-
11	10	FCVT - Encoding	-
11	11	FCVT - Encoding	-

SVE floating-point unary operations

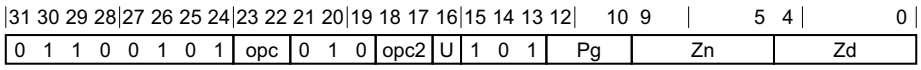
This section describes the encoding of the SVE floating-point unary operations instruction class. The encodings in this section are decoded from *SVE Floating Point Unary Operations - Predicated* on page C4-485.



Decode fields	Instruction page
opc	
00	FRECPX
01	FSQRT
1x	Unallocated.

SVE integer convert to floating-point

This section describes the encoding of the SVE integer convert to floating-point instruction class. The encodings in this section are decoded from *SVE Floating Point Unary Operations - Predicated* on page C4-485.

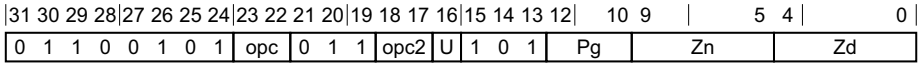


Decode fields			Instruction page
opc	opc2	U	
00	-	-	Unallocated.
01	00	-	Unallocated.
01	01	0	SCVTF - Encoding
01	01	1	UCVTF - Encoding
01	10	0	SCVTF - Encoding
01	10	1	UCVTF - Encoding
01	11	0	SCVTF - Encoding
01	11	1	UCVTF - Encoding
10	0x	-	Unallocated.
10	10	0	SCVTF - Encoding
10	10	1	UCVTF - Encoding
10	11	-	Unallocated.
11	00	0	SCVTF - Encoding
11	00	1	UCVTF - Encoding
11	01	-	Unallocated.
11	10	0	SCVTF - Encoding

Decode fields			Instruction page
opc	opc2	U	
11	10	1	UCVTF - Encoding
11	11	0	SCVTF - Encoding
11	11	1	UCVTF - Encoding

SVE floating-point convert to integer

This section describes the encoding of the SVE floating-point convert to integer instruction class. The encodings in this section are decoded from *SVE Floating Point Unary Operations - Predicated* on page C4-485.



Decode fields			Instruction page
opc	opc2	U	
00	-	0	FLOGB
00	-	1	Unallocated.
01	00	-	Unallocated.
01	01	0	FCVTZS - Encoding
01	01	1	FCVTZU - Encoding
01	10	0	FCVTZS - Encoding
01	10	1	FCVTZU - Encoding
01	11	0	FCVTZS - Encoding
01	11	1	FCVTZU - Encoding
10	0x	-	Unallocated.
10	10	0	FCVTZS - Encoding
10	10	1	FCVTZU - Encoding
10	11	-	Unallocated.
11	00	0	FCVTZS - Encoding
11	00	1	FCVTZU - Encoding
11	01	-	Unallocated.
11	10	0	FCVTZS - Encoding
11	10	1	FCVTZU - Encoding
11	11	0	FCVTZS - Encoding
11	11	1	FCVTZU - Encoding

C4.1.52 SVE Floating Point Unary Operations - Unpredicated

This section describes the encoding of the SVE Floating Point Unary Operations - Unpredicated group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

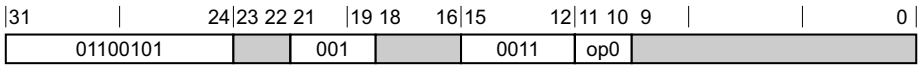
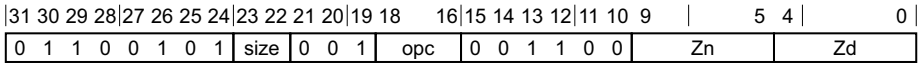


Table C4-53 Encoding table for the SVE Floating Point Unary Operations - Unpredicated group

Decode fields	Decode group or instruction page
op0	
00	*SVE floating-point reciprocal estimate (unpredicated)* on page C4-489
!= 00	Unallocated.

SVE floating-point reciprocal estimate (unpredicated)

This section describes the encoding of the SVE floating-point reciprocal estimate (unpredicated) instruction class. The encodings in this section are decoded from *SVE Floating Point Unary Operations - Unpredicated*.



Decode fields	Instruction page
opc	
0xx	Unallocated.
10x	Unallocated.
110	FRECPE
111	FRSQRTE

C4.1.53 SVE Floating Point Compare - with Zero

This section describes the encoding of the SVE Floating Point Compare - with Zero group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

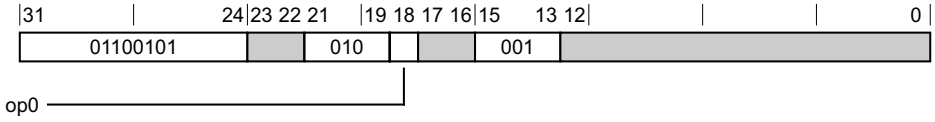
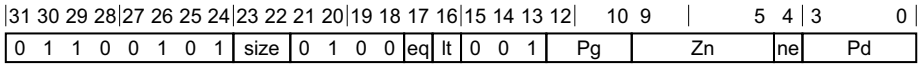


Table C4-54 Encoding table for the SVE Floating Point Compare - with Zero group

Decode fields	Decode group or instruction page
op0	
0	*SVE floating-point compare with zero*
1	Unallocated.

SVE floating-point compare with zero

This section describes the encoding of the SVE floating-point compare with zero instruction class. The encodings in this section are decoded from *SVE Floating Point Compare - with Zero* on page C4-489.



Decode fields			Instruction page
eq	lt	ne	
0	0	0	FCM<cc> (zero) - Encoding
0	0	1	FCM<cc> (zero) - Encoding
0	1	0	FCM<cc> (zero) - Encoding
0	1	1	FCM<cc> (zero) - Encoding
1	-	1	Unallocated.
1	0	0	FCM<cc> (zero) - Encoding
1	1	0	FCM<cc> (zero) - Encoding

C4.1.54 SVE Floating Point Accumulating Reduction

This section describes the encoding of the SVE Floating Point Accumulating Reduction group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

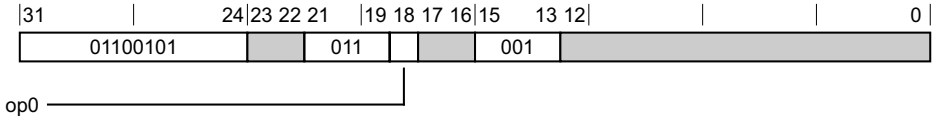
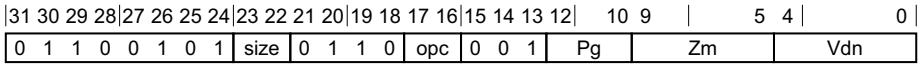


Table C4-55 Encoding table for the SVE Floating Point Accumulating Reduction group

Decode fields op0	Decode group or instruction page
0	*SVE floating-point serial reduction (predicated)*
1	Unallocated.

SVE floating-point serial reduction (predicated)

This section describes the encoding of the SVE floating-point serial reduction (predicated) instruction class. The encodings in this section are decoded from *SVE Floating Point Accumulating Reduction* on page C4-490.



Decode fields opc	Instruction page
00	FADDA
01	Unallocated.
1x	Unallocated.

C4.1.55 SVE Floating Point Multiply-Add

This section describes the encoding of the SVE Floating Point Multiply-Add group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

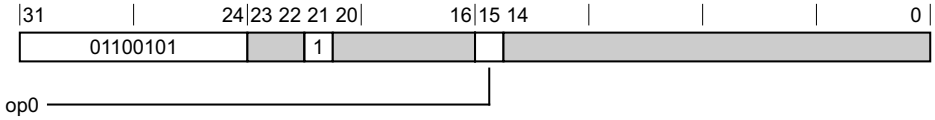
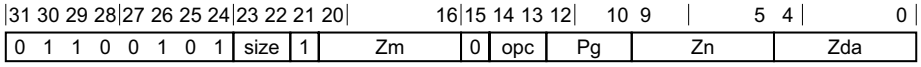


Table C4-56 Encoding table for the SVE Floating Point Multiply-Add group

Decode fields op0	Decode group or instruction page
0	*SVE floating-point multiply-accumulate writing addend* on page C4-492
1	*SVE floating-point multiply-accumulate writing multiplicand* on page C4-492

SVE floating-point multiply-accumulate writing addend

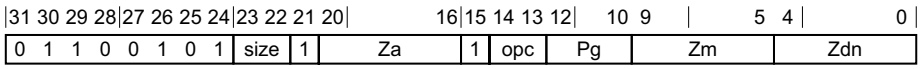
This section describes the encoding of the SVE floating-point multiply-accumulate writing addend instruction class. The encodings in this section are decoded from *SVE Floating Point Multiply-Add* on page C4-491.



Decode fields	Instruction page
opc	
00	FMLA (vectors)
01	FMLS (vectors)
10	FNMLA
11	FNMLS

SVE floating-point multiply-accumulate writing multiplicand

This section describes the encoding of the SVE floating-point multiply-accumulate writing multiplicand instruction class. The encodings in this section are decoded from *SVE Floating Point Multiply-Add* on page C4-491.



Decode fields	Instruction page
opc	
00	FMAD
01	FMSB
10	FNMAD
11	FNMSB

C4.1.56 SVE Memory - 32-bit Gather and Unsized Contiguous

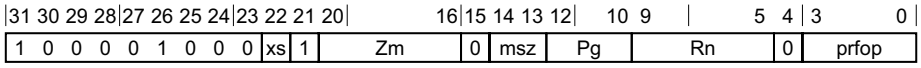
This section describes the encoding of the SVE Memory - 32-bit Gather and Unsized Contiguous group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

Table C4-57 Encoding table for the SVE Memory - 32-bit Gather and Unsized Contiguous group

Decode fields				Decode group or instruction page
op0	op1	op2	op3	
00	x1	0xx	0	*SVE 32-bit gather prefetch (scalar plus 32-bit scaled offsets)* on page C4-493
00	x1	0xx	1	Unallocated.
01	x1	0xx	-	*SVE 32-bit gather load halfwords (scalar plus 32-bit scaled offsets)* on page C4-494
10	x1	0xx	-	*SVE 32-bit gather load words (scalar plus 32-bit scaled offsets)* on page C4-494
11	0x	000	0	LDR (predicate)
11	0x	000	1	Unallocated.
11	0x	010	-	LDR (vector)
11	0x	0x1	-	Unallocated.
11	1x	0xx	0	*SVE contiguous prefetch (scalar plus immediate)* on page C4-495
11	1x	0xx	1	Unallocated.
!= 11	x0	0xx	-	*SVE 32-bit gather load (scalar plus 32-bit unscaled offsets)* on page C4-495
-	00	10x	-	*SVE2 32-bit gather non-temporal load (scalar plus 32-bit unscaled offsets)* on page C4-496
-	00	110	0	*SVE contiguous prefetch (scalar plus scalar)* on page C4-496
-	00	111	0	*SVE 32-bit gather prefetch (vector plus immediate)* on page C4-497
-	00	11x	1	Unallocated.
-	01	1xx	-	*SVE 32-bit gather load (vector plus immediate)* on page C4-497
-	1x	1xx	-	*SVE load and broadcast element* on page C4-498

SVE 32-bit gather prefetch (scalar plus 32-bit scaled offsets)

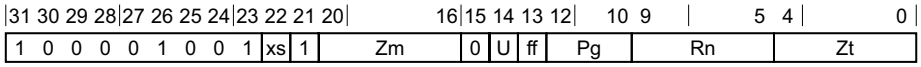
This section describes the encoding of the SVE 32-bit gather prefetch (scalar plus 32-bit scaled offsets) instruction class. The encodings in this section are decoded from *SVE Memory - 32-bit Gather and Unsized Contiguous* on page C4-492.



Decode fields	Instruction page
msz	
00	PRFB (scalar plus vector)
01	PRFH (scalar plus vector)
10	PRFW (scalar plus vector)
11	PRFD (scalar plus vector)

SVE 32-bit gather load halfwords (scalar plus 32-bit scaled offsets)

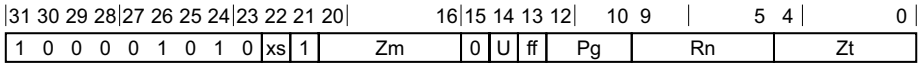
This section describes the encoding of the SVE 32-bit gather load halfwords (scalar plus 32-bit scaled offsets) instruction class. The encodings in this section are decoded from *SVE Memory - 32-bit Gather and Unsized Contiguous* on page C4-492.



Decode fields		Instruction page
U	ff	
0	0	LD1SH (scalar plus vector)
0	1	LDFF1SH (scalar plus vector)
1	0	LD1H (scalar plus vector)
1	1	LDFF1H (scalar plus vector)

SVE 32-bit gather load words (scalar plus 32-bit scaled offsets)

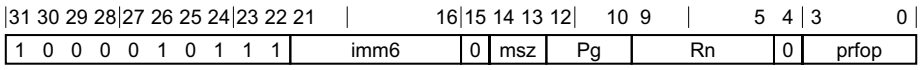
This section describes the encoding of the SVE 32-bit gather load words (scalar plus 32-bit scaled offsets) instruction class. The encodings in this section are decoded from *SVE Memory - 32-bit Gather and Unsized Contiguous* on page C4-492.



Decode fields		Instruction page
U	ff	
0	-	Unallocated.
1	0	LD1W (scalar plus vector)
1	1	LDFF1W (scalar plus vector)

SVE contiguous prefetch (scalar plus immediate)

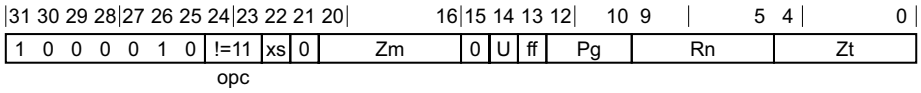
This section describes the encoding of the SVE contiguous prefetch (scalar plus immediate) instruction class. The encodings in this section are decoded from *SVE Memory - 32-bit Gather and Unsized Contiguous* on page C4-492.



Decode fields	Instruction page
msz	
00	PRFB (scalar plus immediate)
01	PRFH (scalar plus immediate)
10	PRFW (scalar plus immediate)
11	PRFD (scalar plus immediate)

SVE 32-bit gather load (scalar plus 32-bit unscaled offsets)

This section describes the encoding of the SVE 32-bit gather load (scalar plus 32-bit unscaled offsets) instruction class. The encodings in this section are decoded from *SVE Memory - 32-bit Gather and Unsized Contiguous* on page C4-492.

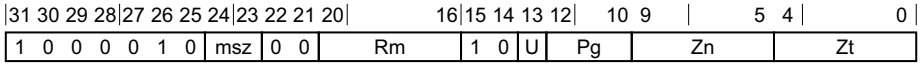


Decode fields			Instruction page
opc	U	ff	
00	0	0	LD1SB (scalar plus vector)
00	0	1	LDFF1SB (scalar plus vector)
00	1	0	LD1B (scalar plus vector)

Decode fields			Instruction page
opc	U	ff	
00	1	1	LDFF1B (scalar plus vector)
01	0	0	LD1SH (scalar plus vector)
01	0	1	LDFF1SH (scalar plus vector)
01	1	0	LD1H (scalar plus vector)
01	1	1	LDFF1H (scalar plus vector)
10	0	-	Unallocated.
10	1	0	LD1W (scalar plus vector)
10	1	1	LDFF1W (scalar plus vector)

SVE2 32-bit gather non-temporal load (scalar plus 32-bit unscaled offsets)

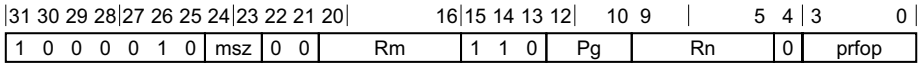
This section describes the encoding of the SVE2 32-bit gather non-temporal load (scalar plus 32-bit unscaled offsets) instruction class. The encodings in this section are decoded from *SVE Memory - 32-bit Gather and Unsized Contiguous* on page C4-492.



Decode fields		Instruction page
msz	U	
00	0	LDNT1SB
00	1	LDNT1B (vector plus scalar)
01	0	LDNT1SH
01	1	LDNT1H (vector plus scalar)
10	0	Unallocated.
10	1	LDNT1W (vector plus scalar)
11	-	Unallocated.

SVE contiguous prefetch (scalar plus scalar)

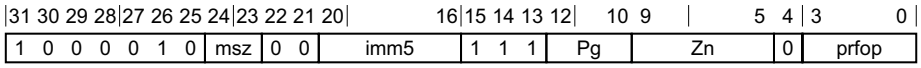
This section describes the encoding of the SVE contiguous prefetch (scalar plus scalar) instruction class. The encodings in this section are decoded from *SVE Memory - 32-bit Gather and Unsized Contiguous* on page C4-492.



Decode fields	Instruction page
msz	
00	PRFB (scalar plus scalar)
01	PRFH (scalar plus scalar)
10	PRFW (scalar plus scalar)
11	PRFD (scalar plus scalar)

SVE 32-bit gather prefetch (vector plus immediate)

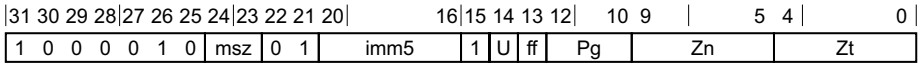
This section describes the encoding of the SVE 32-bit gather prefetch (vector plus immediate) instruction class. The encodings in this section are decoded from *SVE Memory - 32-bit Gather and Unsized Contiguous* on page C4-492.



Decode fields	Instruction page
msz	
00	PRFB (vector plus immediate)
01	PRFH (vector plus immediate)
10	PRFW (vector plus immediate)
11	PRFD (vector plus immediate)

SVE 32-bit gather load (vector plus immediate)

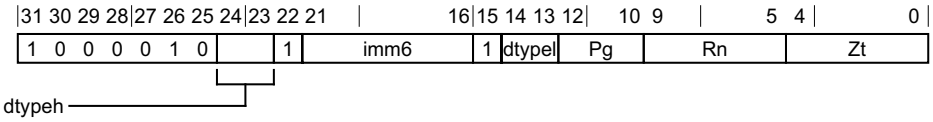
This section describes the encoding of the SVE 32-bit gather load (vector plus immediate) instruction class. The encodings in this section are decoded from *SVE Memory - 32-bit Gather and Unsized Contiguous* on page C4-492.



Decode fields			Instruction page
msz	U	ff	
00	0	0	LD1SB (vector plus immediate)
00	0	1	LDFF1SB (vector plus immediate)
00	1	0	LD1B (vector plus immediate)
00	1	1	LDFF1B (vector plus immediate)
01	0	0	LD1SH (vector plus immediate)
01	0	1	LDFF1SH (vector plus immediate)
01	1	0	LD1H (vector plus immediate)
01	1	1	LDFF1H (vector plus immediate)
10	0	-	Unallocated.
10	1	0	LD1W (vector plus immediate)
10	1	1	LDFF1W (vector plus immediate)
11	-	-	Unallocated.

SVE load and broadcast element

This section describes the encoding of the SVE load and broadcast element instruction class. The encodings in this section are decoded from *SVE Memory - 32-bit Gather and Unsized Contiguous* on page C4-492.



Decode fields		Instruction page
dtypeh	dtypel	
00	00	LD1RB - Encoding
00	01	LD1RB - Encoding
00	10	LD1RB - Encoding
00	11	LD1RB - Encoding
01	00	LD1RSW
01	01	LD1RH - Encoding
01	10	LD1RH - Encoding

Decode fields		Instruction page
dtypeh	dtypel	
01	11	LD1RH - Encoding
10	00	LD1RSH - Encoding
10	01	LD1RSH - Encoding
10	10	LD1RW - Encoding
10	11	LD1RW - Encoding
11	00	LD1RSB - Encoding
11	01	LD1RSB - Encoding
11	10	LD1RSB - Encoding
11	11	LD1RD

C4.1.57 SVE Memory - Contiguous Load

This section describes the encoding of the SVE Memory - Contiguous Load group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

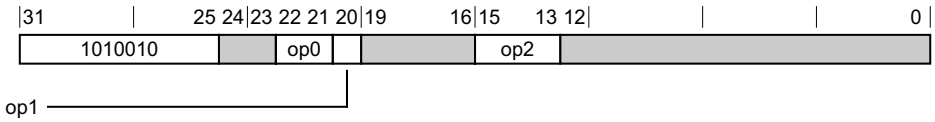


Table C4-58 Encoding table for the SVE Memory - Contiguous Load group

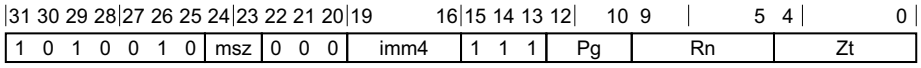
Decode fields			Decode group or instruction page
op0	op1	op2	
00	0	111	*SVE contiguous non-temporal load (scalar plus immediate)* on page C4-500
00	-	110	*SVE contiguous non-temporal load (scalar plus scalar)* on page C4-500
!= 00	0	111	*SVE load multiple structures (scalar plus immediate)* on page C4-501
!= 00	-	110	*SVE load multiple structures (scalar plus scalar)* on page C4-501
-	0	001	*SVE load and broadcast quadword (scalar plus immediate)* on page C4-502
-	0	101	*SVE contiguous load (scalar plus immediate)* on page C4-502
-	1	001	Unallocated.
-	1	101	*SVE contiguous non-fault load (scalar plus immediate)* on page C4-503
-	1	111	Unallocated.
-	-	000	*SVE load and broadcast quadword (scalar plus scalar)* on page C4-504

Table C4-58 Encoding table for the SVE Memory - Contiguous Load group (continued)

Decode fields			Decode group or instruction page
op0	op1	op2	
-	-	010	*SVE contiguous load (scalar plus scalar)* on page C4-505
-	-	011	*SVE contiguous first-fault load (scalar plus scalar)* on page C4-505
-	-	100	Unallocated.

SVE contiguous non-temporal load (scalar plus immediate)

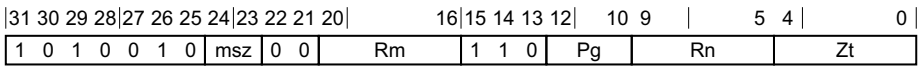
This section describes the encoding of the SVE contiguous non-temporal load (scalar plus immediate) instruction class. The encodings in this section are decoded from *SVE Memory - Contiguous Load* on page C4-499.



Decode fields	Instruction page
msz	
00	LDNT1B (scalar plus immediate)
01	LDNT1H (scalar plus immediate)
10	LDNT1W (scalar plus immediate)
11	LDNT1D (scalar plus immediate)

SVE contiguous non-temporal load (scalar plus scalar)

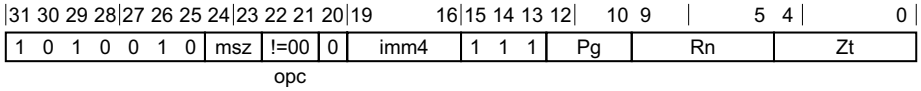
This section describes the encoding of the SVE contiguous non-temporal load (scalar plus scalar) instruction class. The encodings in this section are decoded from *SVE Memory - Contiguous Load* on page C4-499.



Decode fields	Instruction page
msz	
00	LDNT1B (scalar plus scalar)
01	LDNT1H (scalar plus scalar)
10	LDNT1W (scalar plus scalar)
11	LDNT1D (scalar plus scalar)

SVE load multiple structures (scalar plus immediate)

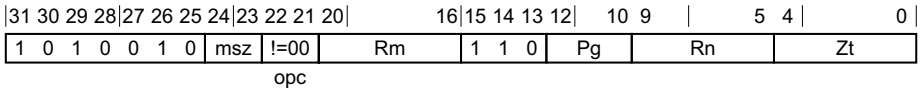
This section describes the encoding of the SVE load multiple structures (scalar plus immediate) instruction class. The encodings in this section are decoded from *SVE Memory - Contiguous Load* on page C4-499.



Decode fields		Instruction page
msz	opc	
00	01	LD2B (scalar plus immediate)
00	10	LD3B (scalar plus immediate)
00	11	LD4B (scalar plus immediate)
01	01	LD2H (scalar plus immediate)
01	10	LD3H (scalar plus immediate)
01	11	LD4H (scalar plus immediate)
10	01	LD2W (scalar plus immediate)
10	10	LD3W (scalar plus immediate)
10	11	LD4W (scalar plus immediate)
11	01	LD2D (scalar plus immediate)
11	10	LD3D (scalar plus immediate)
11	11	LD4D (scalar plus immediate)

SVE load multiple structures (scalar plus scalar)

This section describes the encoding of the SVE load multiple structures (scalar plus scalar) instruction class. The encodings in this section are decoded from *SVE Memory - Contiguous Load* on page C4-499.

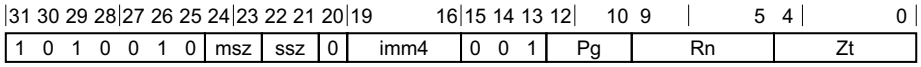


Decode fields		Instruction page
msz	opc	
00	01	LD2B (scalar plus scalar)
00	10	LD3B (scalar plus scalar)
00	11	LD4B (scalar plus scalar)
01	01	LD2H (scalar plus scalar)
01	10	LD3H (scalar plus scalar)

Decode fields		Instruction page
msz	opc	
01	11	LD4H (scalar plus scalar)
10	01	LD2W (scalar plus scalar)
10	10	LD3W (scalar plus scalar)
10	11	LD4W (scalar plus scalar)
11	01	LD2D (scalar plus scalar)
11	10	LD3D (scalar plus scalar)
11	11	LD4D (scalar plus scalar)

SVE load and broadcast quadword (scalar plus immediate)

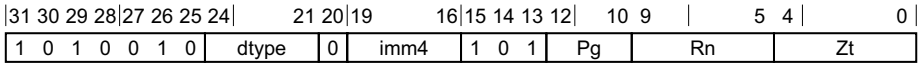
This section describes the encoding of the SVE load and broadcast quadword (scalar plus immediate) instruction class. The encodings in this section are decoded from *SVE Memory - Contiguous Load* on page C4-499.



Decode fields		Instruction page	Feature
msz	ssz		
-	1x	Unallocated.	-
00	00	LD1RQB (scalar plus immediate)	-
00	01	LD1ROB (scalar plus immediate)	FEAT_F64MM
01	00	LD1RQH (scalar plus immediate)	-
01	01	LD1ROH (scalar plus immediate)	FEAT_F64MM
10	00	LD1RQW (scalar plus immediate)	-
10	01	LD1ROW (scalar plus immediate)	FEAT_F64MM
11	00	LD1RQD (scalar plus immediate)	-
11	01	LD1ROD (scalar plus immediate)	FEAT_F64MM

SVE contiguous load (scalar plus immediate)

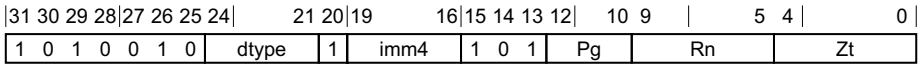
This section describes the encoding of the SVE contiguous load (scalar plus immediate) instruction class. The encodings in this section are decoded from *SVE Memory - Contiguous Load* on page C4-499.



Decode fields	Instruction page
dtype	
0000	LD1B (scalar plus immediate) - Encoding
0001	LD1B (scalar plus immediate) - Encoding
0010	LD1B (scalar plus immediate) - Encoding
0011	LD1B (scalar plus immediate) - Encoding
0100	LD1SW (scalar plus immediate)
0101	LD1H (scalar plus immediate) - Encoding
0110	LD1H (scalar plus immediate) - Encoding
0111	LD1H (scalar plus immediate) - Encoding
1000	LD1SH (scalar plus immediate) - Encoding
1001	LD1SH (scalar plus immediate) - Encoding
1010	LD1W (scalar plus immediate) - Encoding
1011	LD1W (scalar plus immediate) - Encoding
1100	LD1SB (scalar plus immediate) - Encoding
1101	LD1SB (scalar plus immediate) - Encoding
1110	LD1SB (scalar plus immediate) - Encoding
1111	LD1D (scalar plus immediate)

SVE contiguous non-fault load (scalar plus immediate)

This section describes the encoding of the SVE contiguous non-fault load (scalar plus immediate) instruction class. The encodings in this section are decoded from *SVE Memory - Contiguous Load* on page C4-499.

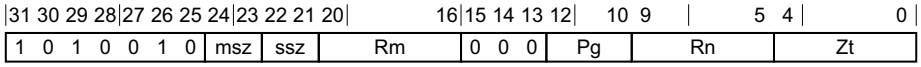


Decode fields	Instruction page
dtype	
0000	LDNF1B - Encoding
0001	LDNF1B - Encoding
0010	LDNF1B - Encoding

Decode fields	Instruction page
dtype	
0011	LDNF1B - Encoding
0100	LDNF1SW
0101	LDNF1H - Encoding
0110	LDNF1H - Encoding
0111	LDNF1H - Encoding
1000	LDNF1SH - Encoding
1001	LDNF1SH - Encoding
1010	LDNF1W - Encoding
1011	LDNF1W - Encoding
1100	LDNF1SB - Encoding
1101	LDNF1SB - Encoding
1110	LDNF1SB - Encoding
1111	LDNF1D

SVE load and broadcast quadword (scalar plus scalar)

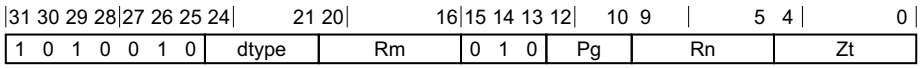
This section describes the encoding of the SVE load and broadcast quadword (scalar plus scalar) instruction class. The encodings in this section are decoded from *SVE Memory - Contiguous Load* on page C4-499.



Decode fields		Instruction page	Feature
msz	ssz		
-	1x	Unallocated.	-
00	00	LD1RQB (scalar plus scalar)	-
00	01	LD1ROB (scalar plus scalar)	FEAT_F64MM
01	00	LD1RQH (scalar plus scalar)	-
01	01	LD1ROH (scalar plus scalar)	FEAT_F64MM
10	00	LD1RQW (scalar plus scalar)	-
10	01	LD1ROW (scalar plus scalar)	FEAT_F64MM
11	00	LD1RQD (scalar plus scalar)	-
11	01	LD1ROD (scalar plus scalar)	FEAT_F64MM

SVE contiguous load (scalar plus scalar)

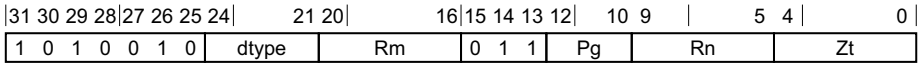
This section describes the encoding of the SVE contiguous load (scalar plus scalar) instruction class. The encodings in this section are decoded from *SVE Memory - Contiguous Load* on page C4-499.



Decode fields	Instruction page
dtype	
0000	LD1B (scalar plus scalar) - Encoding
0001	LD1B (scalar plus scalar) - Encoding
0010	LD1B (scalar plus scalar) - Encoding
0011	LD1B (scalar plus scalar) - Encoding
0100	LD1SW (scalar plus scalar)
0101	LD1H (scalar plus scalar) - Encoding
0110	LD1H (scalar plus scalar) - Encoding
0111	LD1H (scalar plus scalar) - Encoding
1000	LD1SH (scalar plus scalar) - Encoding
1001	LD1SH (scalar plus scalar) - Encoding
1010	LD1W (scalar plus scalar) - Encoding
1011	LD1W (scalar plus scalar) - Encoding
1100	LD1SB (scalar plus scalar) - Encoding
1101	LD1SB (scalar plus scalar) - Encoding
1110	LD1SB (scalar plus scalar) - Encoding
1111	LD1D (scalar plus scalar)

SVE contiguous first-fault load (scalar plus scalar)

This section describes the encoding of the SVE contiguous first-fault load (scalar plus scalar) instruction class. The encodings in this section are decoded from *SVE Memory - Contiguous Load* on page C4-499.



Decode fields dtype	Instruction page
0000	LDFF1B (scalar plus scalar) - Encoding
0001	LDFF1B (scalar plus scalar) - Encoding
0010	LDFF1B (scalar plus scalar) - Encoding
0011	LDFF1B (scalar plus scalar) - Encoding
0100	LDFF1SW (scalar plus scalar)
0101	LDFF1H (scalar plus scalar) - Encoding
0110	LDFF1H (scalar plus scalar) - Encoding
0111	LDFF1H (scalar plus scalar) - Encoding
1000	LDFF1SH (scalar plus scalar) - Encoding
1001	LDFF1SH (scalar plus scalar) - Encoding
1010	LDFF1W (scalar plus scalar) - Encoding
1011	LDFF1W (scalar plus scalar) - Encoding
1100	LDFF1SB (scalar plus scalar) - Encoding
1101	LDFF1SB (scalar plus scalar) - Encoding
1110	LDFF1SB (scalar plus scalar) - Encoding
1111	LDFF1D (scalar plus scalar)

C4.1.58 SVE Memory - 64-bit Gather

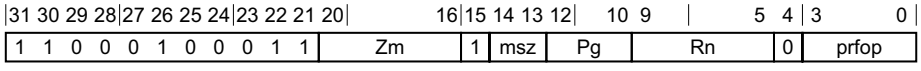
This section describes the encoding of the SVE Memory - 64-bit Gather group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

Table C4-59 Encoding table for the SVE Memory - 64-bit Gather group

Decode fields				Decode group or instruction page
op0	op1	op2	op3	
00	01	0xx	1	Unallocated.
00	11	1xx	0	*SVE 64-bit gather prefetch (scalar plus 64-bit scaled offsets)* on page C4-507
00	11	-	1	Unallocated.
00	x1	0xx	0	*SVE 64-bit gather prefetch (scalar plus unpacked 32-bit scaled offsets)* on page C4-508
!= 00	11	1xx	-	*SVE 64-bit gather load (scalar plus 64-bit scaled offsets)* on page C4-508
!= 00	x1	0xx	-	*SVE 64-bit gather load (scalar plus 32-bit unpacked scaled offsets)* on page C4-509
-	00	101	-	Unallocated.
-	00	111	0	*SVE 64-bit gather prefetch (vector plus immediate)* on page C4-509
-	00	111	1	Unallocated.
-	00	1x0	-	*SVE2 64-bit gather non-temporal load (scalar plus unpacked 32-bit unscaled offsets)* on page C4-510
-	01	1xx	-	*SVE 64-bit gather load (vector plus immediate)* on page C4-510
-	10	1xx	-	*SVE 64-bit gather load (scalar plus 64-bit unscaled offsets)* on page C4-511
-	x0	0xx	-	*SVE 64-bit gather load (scalar plus unpacked 32-bit unscaled offsets)* on page C4-512

SVE 64-bit gather prefetch (scalar plus 64-bit scaled offsets)

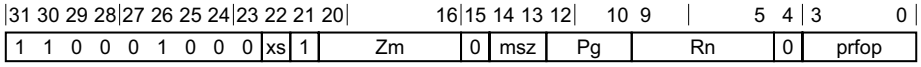
This section describes the encoding of the SVE 64-bit gather prefetch (scalar plus 64-bit scaled offsets) instruction class. The encodings in this section are decoded from *SVE Memory - 64-bit Gather* on page C4-506.



Decode fields	Instruction page
msz	
00	PRFB (scalar plus vector)
01	PRFH (scalar plus vector)
10	PRFW (scalar plus vector)
11	PRFD (scalar plus vector)

SVE 64-bit gather prefetch (scalar plus unpacked 32-bit scaled offsets)

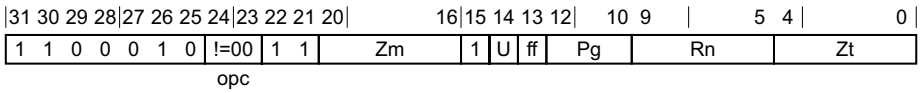
This section describes the encoding of the SVE 64-bit gather prefetch (scalar plus unpacked 32-bit scaled offsets) instruction class. The encodings in this section are decoded from *SVE Memory - 64-bit Gather* on page C4-506.



Decode fields	Instruction page
msz	
00	PRFB (scalar plus vector)
01	PRFH (scalar plus vector)
10	PRFW (scalar plus vector)
11	PRFD (scalar plus vector)

SVE 64-bit gather load (scalar plus 64-bit scaled offsets)

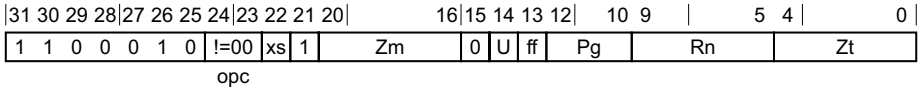
This section describes the encoding of the SVE 64-bit gather load (scalar plus 64-bit scaled offsets) instruction class. The encodings in this section are decoded from *SVE Memory - 64-bit Gather* on page C4-506.



Decode fields			Instruction page
opc	U	ff	
01	0	0	LD1SH (scalar plus vector)
01	0	1	LDFF1SH (scalar plus vector)
01	1	0	LD1H (scalar plus vector)
01	1	1	LDFF1H (scalar plus vector)
10	0	0	LD1SW (scalar plus vector)
10	0	1	LDFF1SW (scalar plus vector)
10	1	0	LD1W (scalar plus vector)
10	1	1	LDFF1W (scalar plus vector)
11	0	-	Unallocated.
11	1	0	LD1D (scalar plus vector)
11	1	1	LDFF1D (scalar plus vector)

SVE 64-bit gather load (scalar plus 32-bit unpacked scaled offsets)

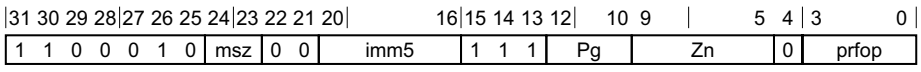
This section describes the encoding of the SVE 64-bit gather load (scalar plus 32-bit unpacked scaled offsets) instruction class. The encodings in this section are decoded from *SVE Memory - 64-bit Gather* on page C4-506.



Decode fields			Instruction page
opc	U	ff	
01	0	0	LD1SH (scalar plus vector)
01	0	1	LDFF1SH (scalar plus vector)
01	1	0	LD1H (scalar plus vector)
01	1	1	LDFF1H (scalar plus vector)
10	0	0	LD1SW (scalar plus vector)
10	0	1	LDFF1SW (scalar plus vector)
10	1	0	LD1W (scalar plus vector)
10	1	1	LDFF1W (scalar plus vector)
11	0	-	Unallocated.
11	1	0	LD1D (scalar plus vector)
11	1	1	LDFF1D (scalar plus vector)

SVE 64-bit gather prefetch (vector plus immediate)

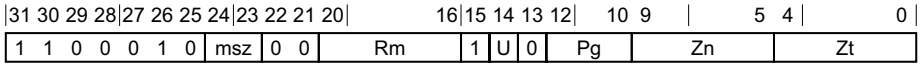
This section describes the encoding of the SVE 64-bit gather prefetch (vector plus immediate) instruction class. The encodings in this section are decoded from *SVE Memory - 64-bit Gather* on page C4-506.



Decode fields	Instruction page
msz	
00	PRFB (vector plus immediate)
01	PRFH (vector plus immediate)
10	PRFW (vector plus immediate)
11	PRFD (vector plus immediate)

SVE2 64-bit gather non-temporal load (scalar plus unpacked 32-bit unscaled offsets)

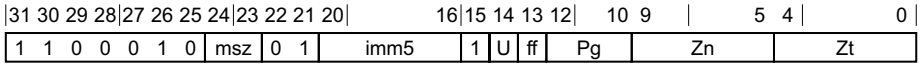
This section describes the encoding of the SVE2 64-bit gather non-temporal load (scalar plus unpacked 32-bit unscaled offsets) instruction class. The encodings in this section are decoded from *SVE Memory - 64-bit Gather* on page C4-506.



Decode fields		Instruction page
msz	U	
00	0	LDNT1SB
00	1	LDNT1B (vector plus scalar)
01	0	LDNT1SH
01	1	LDNT1H (vector plus scalar)
10	0	LDNT1SW
10	1	LDNT1W (vector plus scalar)
11	0	Unallocated.
11	1	LDNT1D (vector plus scalar)

SVE 64-bit gather load (vector plus immediate)

This section describes the encoding of the SVE 64-bit gather load (vector plus immediate) instruction class. The encodings in this section are decoded from *SVE Memory - 64-bit Gather* on page C4-506.

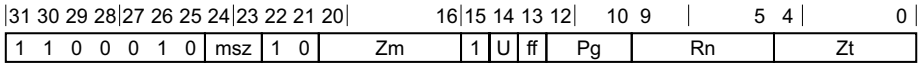


Decode fields			Instruction page
msz	U	ff	
00	0	0	LD1SB (vector plus immediate)
00	0	1	LDFF1SB (vector plus immediate)
00	1	0	LD1B (vector plus immediate)
00	1	1	LDFF1B (vector plus immediate)
01	0	0	LD1SH (vector plus immediate)
01	0	1	LDFF1SH (vector plus immediate)
01	1	0	LD1H (vector plus immediate)
01	1	1	LDFF1H (vector plus immediate)

Decode fields			Instruction page
msz	U	ff	
10	0	0	LD1SW (vector plus immediate)
10	0	1	LDFF1SW (vector plus immediate)
10	1	0	LD1W (vector plus immediate)
10	1	1	LDFF1W (vector plus immediate)
11	0	-	Unallocated.
11	1	0	LD1D (vector plus immediate)
11	1	1	LDFF1D (vector plus immediate)

SVE 64-bit gather load (scalar plus 64-bit unscaled offsets)

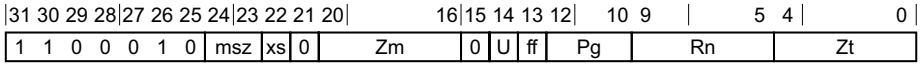
This section describes the encoding of the SVE 64-bit gather load (scalar plus 64-bit unscaled offsets) instruction class. The encodings in this section are decoded from *SVE Memory - 64-bit Gather* on page C4-506.



Decode fields			Instruction page
msz	U	ff	
00	0	0	LD1SB (scalar plus vector)
00	0	1	LDFF1SB (scalar plus vector)
00	1	0	LD1B (scalar plus vector)
00	1	1	LDFF1B (scalar plus vector)
01	0	0	LD1SH (scalar plus vector)
01	0	1	LDFF1SH (scalar plus vector)
01	1	0	LD1H (scalar plus vector)
01	1	1	LDFF1H (scalar plus vector)
10	0	0	LD1SW (scalar plus vector)
10	0	1	LDFF1SW (scalar plus vector)
10	1	0	LD1W (scalar plus vector)
10	1	1	LDFF1W (scalar plus vector)
11	0	-	Unallocated.
11	1	0	LD1D (scalar plus vector)
11	1	1	LDFF1D (scalar plus vector)

SVE 64-bit gather load (scalar plus unpacked 32-bit unscaled offsets)

This section describes the encoding of the SVE 64-bit gather load (scalar plus unpacked 32-bit unscaled offsets) instruction class. The encodings in this section are decoded from *SVE Memory - 64-bit Gather* on page C4-506.



Decode fields			Instruction page
msz	U	ff	
00	0	0	LD1SB (scalar plus vector)
00	0	1	LDFF1SB (scalar plus vector)
00	1	0	LD1B (scalar plus vector)
00	1	1	LDFF1B (scalar plus vector)
01	0	0	LD1SH (scalar plus vector)
01	0	1	LDFF1SH (scalar plus vector)
01	1	0	LD1H (scalar plus vector)
01	1	1	LDFF1H (scalar plus vector)
10	0	0	LD1SW (scalar plus vector)
10	0	1	LDFF1SW (scalar plus vector)
10	1	0	LD1W (scalar plus vector)
10	1	1	LDFF1W (scalar plus vector)
11	0	-	Unallocated.
11	1	0	LD1D (scalar plus vector)
11	1	1	LDFF1D (scalar plus vector)

C4.1.59 SVE Memory - Contiguous Store and Unsized Contiguous

This section describes the encoding of the SVE Memory - Contiguous Store and Unsized Contiguous group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

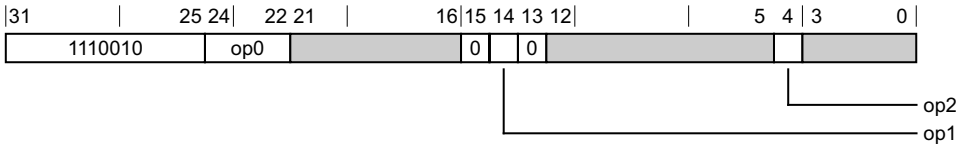
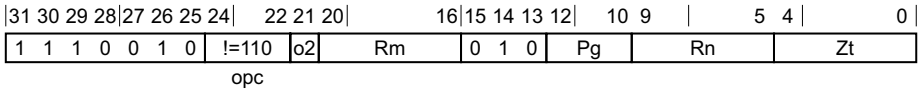


Table C4-60 Encoding table for the SVE Memory - Contiguous Store and Unsized Contiguous group

Decode fields			Decode group or instruction page
op0	op1	op2	
0xx	0	-	Unallocated.
10x	0	-	Unallocated.
110	0	0	STR (predicate)
110	0	1	Unallocated.
110	1	-	STR (vector)
111	0	-	Unallocated.
!= 110	1	-	*SVE contiguous store (scalar plus scalar)*

SVE contiguous store (scalar plus scalar)

This section describes the encoding of the SVE contiguous store (scalar plus scalar) instruction class. The encodings in this section are decoded from *SVE Memory - Contiguous Store and Unsized Contiguous* on page C4-512.



Decode fields		Instruction page
opc	o2	
00x	-	ST1B (scalar plus scalar)
01x	-	ST1H (scalar plus scalar)
10x	-	ST1W (scalar plus scalar)
111	0	Unallocated.
111	1	ST1D (scalar plus scalar)

C4.1.60 SVE Memory - Non-temporal and Multi-register Store

This section describes the encoding of the SVE Memory - Non-temporal and Multi-register Store group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

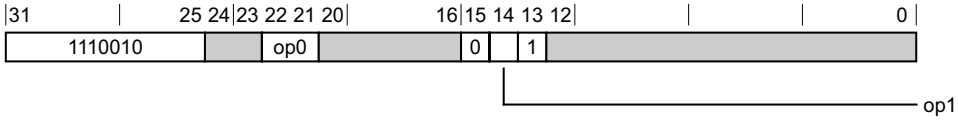
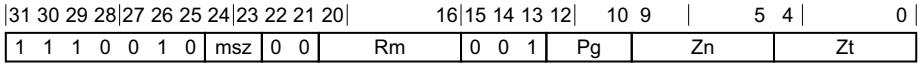


Table C4-61 Encoding table for the SVE Memory - Non-temporal and Multi-register Store group

Decode fields		Decode group or instruction page
op0	op1	
00	0	*SVE2 64-bit scatter non-temporal store (vector plus scalar)*
00	1	*SVE contiguous non-temporal store (scalar plus scalar)*
10	0	*SVE2 32-bit scatter non-temporal store (vector plus scalar)* on page C4-515
!= 00	1	*SVE store multiple structures (scalar plus scalar)* on page C4-515
x1	0	Unallocated.

SVE2 64-bit scatter non-temporal store (vector plus scalar)

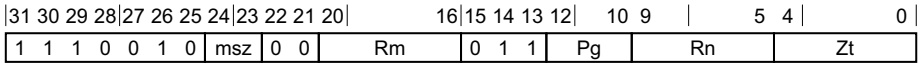
This section describes the encoding of the SVE2 64-bit scatter non-temporal store (vector plus scalar) instruction class. The encodings in this section are decoded from *SVE Memory - Non-temporal and Multi-register Store* on page C4-513.



Decode fields	Instruction page
msz	
00	STNT1B (vector plus scalar)
01	STNT1H (vector plus scalar)
10	STNT1W (vector plus scalar)
11	STNT1D (vector plus scalar)

SVE contiguous non-temporal store (scalar plus scalar)

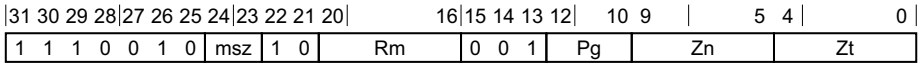
This section describes the encoding of the SVE contiguous non-temporal store (scalar plus scalar) instruction class. The encodings in this section are decoded from *SVE Memory - Non-temporal and Multi-register Store* on page C4-513.



Decode fields	Instruction page
msz	
00	STNT1B (scalar plus scalar)
01	STNT1H (scalar plus scalar)
10	STNT1W (scalar plus scalar)
11	STNT1D (scalar plus scalar)

SVE2 32-bit scatter non-temporal store (vector plus scalar)

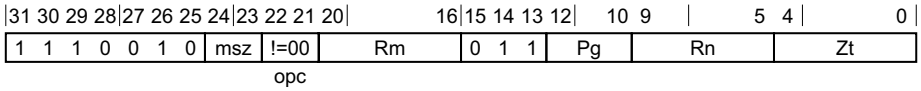
This section describes the encoding of the SVE2 32-bit scatter non-temporal store (vector plus scalar) instruction class. The encodings in this section are decoded from *SVE Memory - Non-temporal and Multi-register Store* on page C4-513.



Decode fields	Instruction page
msz	
00	STNT1B (vector plus scalar)
01	STNT1H (vector plus scalar)
10	STNT1W (vector plus scalar)
11	Unallocated.

SVE store multiple structures (scalar plus scalar)

This section describes the encoding of the SVE store multiple structures (scalar plus scalar) instruction class. The encodings in this section are decoded from *SVE Memory - Non-temporal and Multi-register Store* on page C4-513.



Decode fields		Instruction page
msz	opc	
00	01	ST2B (scalar plus scalar)
00	10	ST3B (scalar plus scalar)
00	11	ST4B (scalar plus scalar)
01	01	ST2H (scalar plus scalar)
01	10	ST3H (scalar plus scalar)
01	11	ST4H (scalar plus scalar)
10	01	ST2W (scalar plus scalar)
10	10	ST3W (scalar plus scalar)
10	11	ST4W (scalar plus scalar)
11	01	ST2D (scalar plus scalar)
11	10	ST3D (scalar plus scalar)
11	11	ST4D (scalar plus scalar)

C4.1.61 SVE Memory - Scatter with Optional Sign Extend

This section describes the encoding of the SVE Memory - Scatter with Optional Sign Extend group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

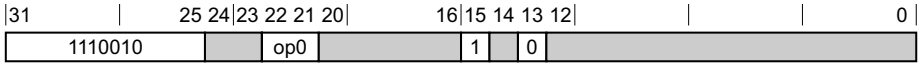
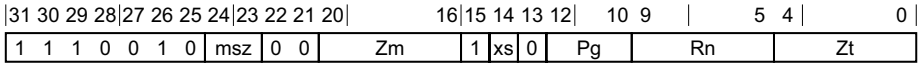


Table C4-62 Encoding table for the SVE Memory - Scatter with Optional Sign Extend group

Decode fields	Decode group or instruction page
op0	
00	*SVE 64-bit scatter store (scalar plus unpacked 32-bit unscaled offsets)* on page C4-517
01	*SVE 64-bit scatter store (scalar plus unpacked 32-bit scaled offsets)* on page C4-517
10	*SVE 32-bit scatter store (scalar plus 32-bit unscaled offsets)* on page C4-517
11	*SVE 32-bit scatter store (scalar plus 32-bit scaled offsets)* on page C4-518

SVE 64-bit scatter store (scalar plus unpacked 32-bit unscaled offsets)

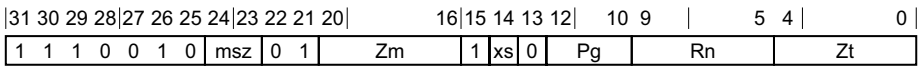
This section describes the encoding of the SVE 64-bit scatter store (scalar plus unpacked 32-bit unscaled offsets) instruction class. The encodings in this section are decoded from *SVE Memory - Scatter with Optional Sign Extend* on page C4-516.



Decode fields	Instruction page
msz	
00	ST1B (scalar plus vector)
01	ST1H (scalar plus vector)
10	ST1W (scalar plus vector)
11	ST1D (scalar plus vector)

SVE 64-bit scatter store (scalar plus unpacked 32-bit scaled offsets)

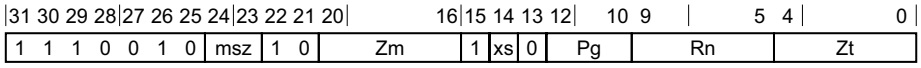
This section describes the encoding of the SVE 64-bit scatter store (scalar plus unpacked 32-bit scaled offsets) instruction class. The encodings in this section are decoded from *SVE Memory - Scatter with Optional Sign Extend* on page C4-516.



Decode fields	Instruction page
msz	
00	Unallocated.
01	ST1H (scalar plus vector)
10	ST1W (scalar plus vector)
11	ST1D (scalar plus vector)

SVE 32-bit scatter store (scalar plus 32-bit unscaled offsets)

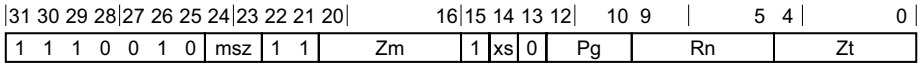
This section describes the encoding of the SVE 32-bit scatter store (scalar plus 32-bit unscaled offsets) instruction class. The encodings in this section are decoded from *SVE Memory - Scatter with Optional Sign Extend* on page C4-516.



Decode fields msz	Instruction page
00	ST1B (scalar plus vector)
01	ST1H (scalar plus vector)
10	ST1W (scalar plus vector)
11	Unallocated.

SVE 32-bit scatter store (scalar plus 32-bit scaled offsets)

This section describes the encoding of the SVE 32-bit scatter store (scalar plus 32-bit scaled offsets) instruction class. The encodings in this section are decoded from *SVE Memory - Scatter with Optional Sign Extend* on page C4-516.



Decode fields msz	Instruction page
00	Unallocated.
01	ST1H (scalar plus vector)
10	ST1W (scalar plus vector)
11	Unallocated.

C4.1.62 SVE Memory - Scatter

This section describes the encoding of the SVE Memory - Scatter group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

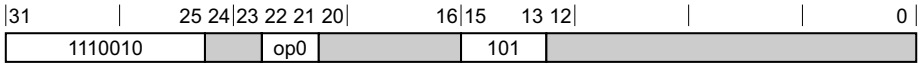
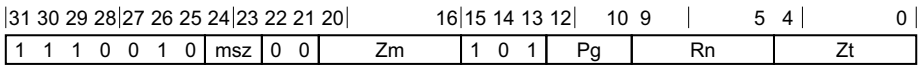


Table C4-63 Encoding table for the SVE Memory - Scatter group

Decode fields op0	Decode group or instruction page
00	*SVE 64-bit scatter store (scalar plus 64-bit unscaled offsets)*
01	*SVE 64-bit scatter store (scalar plus 64-bit scaled offsets)*
10	*SVE 64-bit scatter store (vector plus immediate)* on page C4-520
11	*SVE 32-bit scatter store (vector plus immediate)* on page C4-520

SVE 64-bit scatter store (scalar plus 64-bit unscaled offsets)

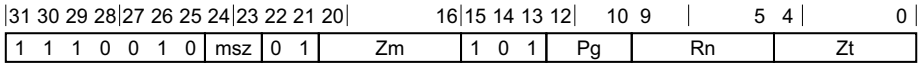
This section describes the encoding of the SVE 64-bit scatter store (scalar plus 64-bit unscaled offsets) instruction class. The encodings in this section are decoded from *SVE Memory - Scatter* on page C4-518.



Decode fields msz	Instruction page
00	ST1B (scalar plus vector)
01	ST1H (scalar plus vector)
10	ST1W (scalar plus vector)
11	ST1D (scalar plus vector)

SVE 64-bit scatter store (scalar plus 64-bit scaled offsets)

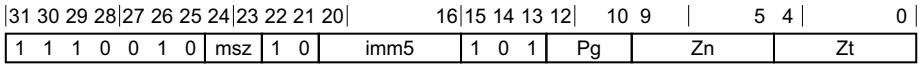
This section describes the encoding of the SVE 64-bit scatter store (scalar plus 64-bit scaled offsets) instruction class. The encodings in this section are decoded from *SVE Memory - Scatter* on page C4-518.



Decode fields	Instruction page
msz	
00	Unallocated.
01	ST1H (scalar plus vector)
10	ST1W (scalar plus vector)
11	ST1D (scalar plus vector)

SVE 64-bit scatter store (vector plus immediate)

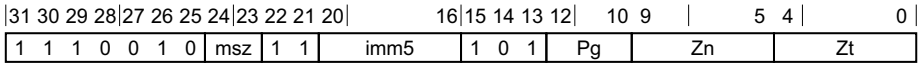
This section describes the encoding of the SVE 64-bit scatter store (vector plus immediate) instruction class. The encodings in this section are decoded from *SVE Memory - Scatter* on page C4-518.



Decode fields	Instruction page
msz	
00	ST1B (vector plus immediate)
01	ST1H (vector plus immediate)
10	ST1W (vector plus immediate)
11	ST1D (vector plus immediate)

SVE 32-bit scatter store (vector plus immediate)

This section describes the encoding of the SVE 32-bit scatter store (vector plus immediate) instruction class. The encodings in this section are decoded from *SVE Memory - Scatter* on page C4-518.



Decode fields	Instruction page
msz	
00	ST1B (vector plus immediate)
01	ST1H (vector plus immediate)
10	ST1W (vector plus immediate)
11	Unallocated.

C4.1.63 SVE Memory - Contiguous Store with Immediate Offset

This section describes the encoding of the SVE Memory - Contiguous Store with Immediate Offset group. The encodings in this section are decoded from *SVE encodings* on page C4-391.

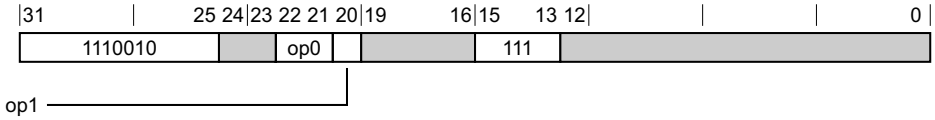
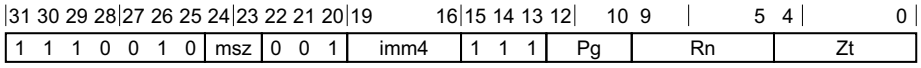


Table C4-64 Encoding table for the SVE Memory - Contiguous Store with Immediate Offset group

Decode fields		Decode group or instruction page
op0	op1	
00	1	*SVE contiguous non-temporal store (scalar plus immediate)* on page C4-521
!= 00	1	*SVE store multiple structures (scalar plus immediate)* on page C4-522
-	0	*SVE contiguous store (scalar plus immediate)* on page C4-522

SVE contiguous non-temporal store (scalar plus immediate)

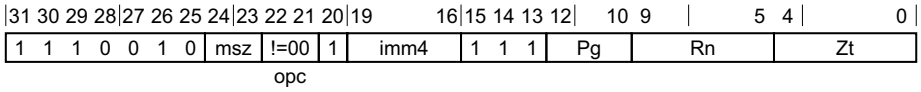
This section describes the encoding of the SVE contiguous non-temporal store (scalar plus immediate) instruction class. The encodings in this section are decoded from *SVE Memory - Contiguous Store with Immediate Offset*.



Decode fields	Instruction page
msz	
00	STNT1B (scalar plus immediate)
01	STNT1H (scalar plus immediate)
10	STNT1W (scalar plus immediate)
11	STNT1D (scalar plus immediate)

SVE store multiple structures (scalar plus immediate)

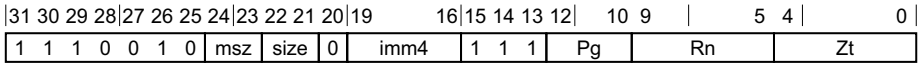
This section describes the encoding of the SVE store multiple structures (scalar plus immediate) instruction class. The encodings in this section are decoded from *SVE Memory - Contiguous Store with Immediate Offset* on page C4-521.



Decode fields		Instruction page
msz	opc	
00	01	ST2B (scalar plus immediate)
00	10	ST3B (scalar plus immediate)
00	11	ST4B (scalar plus immediate)
01	01	ST2H (scalar plus immediate)
01	10	ST3H (scalar plus immediate)
01	11	ST4H (scalar plus immediate)
10	01	ST2W (scalar plus immediate)
10	10	ST3W (scalar plus immediate)
10	11	ST4W (scalar plus immediate)
11	01	ST2D (scalar plus immediate)
11	10	ST3D (scalar plus immediate)
11	11	ST4D (scalar plus immediate)

SVE contiguous store (scalar plus immediate)

This section describes the encoding of the SVE contiguous store (scalar plus immediate) instruction class. The encodings in this section are decoded from *SVE Memory - Contiguous Store with Immediate Offset* on page C4-521.



Decode fields msz	Instruction page
00	ST1B (scalar plus immediate)
01	ST1H (scalar plus immediate)
10	ST1W (scalar plus immediate)
11	ST1D (scalar plus immediate)

C4.1.64 Data Processing -- Immediate

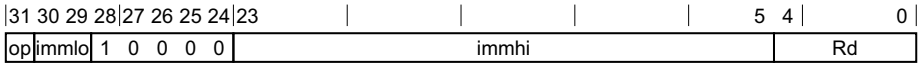
This section describes the encoding of the Data Processing -- Immediate group. The encodings in this section are decoded from *A64 instruction set encoding* on page C4-380.

Table C4-65 Encoding table for the Data Processing -- Immediate group

Decode fields op0	Decode group or instruction page
00x	*PC-rel. addressing* on page C4-523
010	*Add/subtract (immediate)* on page C4-524
011	*Add/subtract (immediate, with tags)* on page C4-524
100	*Logical (immediate)* on page C4-525
101	*Move wide (immediate)* on page C4-525
110	*Bitfield* on page C4-526
111	*Extract* on page C4-527

PC-rel. addressing

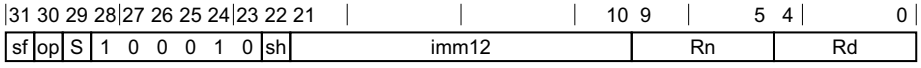
This section describes the encoding of the PC-rel. addressing instruction class. The encodings in this section are decoded from *Data Processing -- Immediate*.



Decode fields	Instruction page
op	
0	ADR
1	ADRP

Add/subtract (immediate)

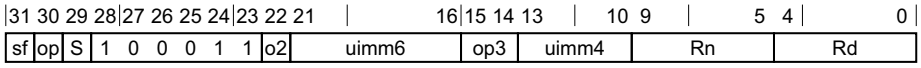
This section describes the encoding of the Add/subtract (immediate) instruction class. The encodings in this section are decoded from *Data Processing -- Immediate* on page C4-523.



Decode fields			Instruction page
sf	op	S	
0	0	0	ADD (immediate) - 32-bit variant
0	0	1	ADDS (immediate) - 32-bit variant
0	1	0	SUB (immediate) - 32-bit variant
0	1	1	SUBS (immediate) - 32-bit variant
1	0	0	ADD (immediate) - 64-bit variant
1	0	1	ADDS (immediate) - 64-bit variant
1	1	0	SUB (immediate) - 64-bit variant
1	1	1	SUBS (immediate) - 64-bit variant

Add/subtract (immediate, with tags)

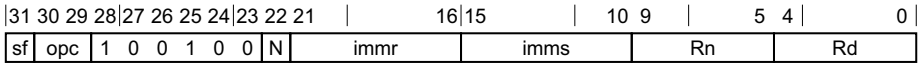
This section describes the encoding of the Add/subtract (immediate, with tags) instruction class. The encodings in this section are decoded from *Data Processing -- Immediate* on page C4-523.



Decode fields				Instruction page	Feature
sf	op	S	o2		
-	-	-	1	Unallocated.	-
0	-	-	0	Unallocated.	-
1	-	1	0	Unallocated.	-
1	0	0	0	ADDG	FEAT_MTE
1	1	0	0	SUBG	FEAT_MTE

Logical (immediate)

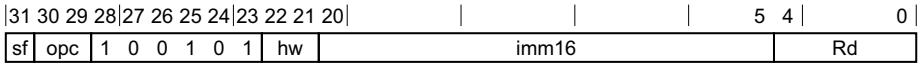
This section describes the encoding of the Logical (immediate) instruction class. The encodings in this section are decoded from *Data Processing -- Immediate* on page C4-523.



Decode fields			Instruction page
sf	opc	N	
0	-	1	Unallocated.
0	00	0	AND (immediate) - 32-bit variant
0	01	0	ORR (immediate) - 32-bit variant
0	10	0	EOR (immediate) - 32-bit variant
0	11	0	ANDS (immediate) - 32-bit variant
1	00	-	AND (immediate) - 64-bit variant
1	01	-	ORR (immediate) - 64-bit variant
1	10	-	EOR (immediate) - 64-bit variant
1	11	-	ANDS (immediate) - 64-bit variant

Move wide (immediate)

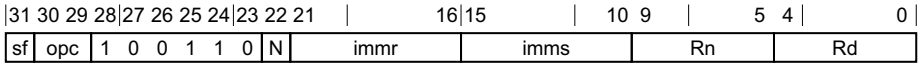
This section describes the encoding of the Move wide (immediate) instruction class. The encodings in this section are decoded from *Data Processing -- Immediate* on page C4-523.



Decode fields			Instruction page
sf	opc	hw	
-	01	-	Unallocated.
0	-	1x	Unallocated.
0	00	0x	MOVN - 32-bit variant
0	10	0x	MOVZ - 32-bit variant
0	11	0x	MOVK - 32-bit variant
1	00	-	MOVN - 64-bit variant
1	10	-	MOVZ - 64-bit variant
1	11	-	MOVK - 64-bit variant

Bitfield

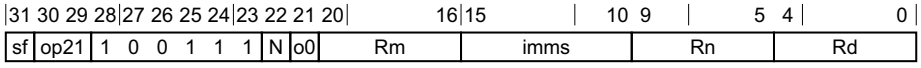
This section describes the encoding of the Bitfield instruction class. The encodings in this section are decoded from *Data Processing -- Immediate* on page C4-523.



Decode fields			Instruction page
sf	opc	N	
-	11	-	Unallocated.
0	-	1	Unallocated.
0	00	0	SBFM - 32-bit variant
0	01	0	BFM - 32-bit variant
0	10	0	UBFM - 32-bit variant
1	-	0	Unallocated.
1	00	1	SBFM - 64-bit variant
1	01	1	BFM - 64-bit variant
1	10	1	UBFM - 64-bit variant

Extract

This section describes the encoding of the Extract instruction class. The encodings in this section are decoded from *Data Processing -- Immediate* on page C4-523.



Decode fields					Instruction page
sf	op21	N	o0	imms	
-	x1	-	-	-	Unallocated.
-	00	-	1	-	Unallocated.
-	1x	-	-	-	Unallocated.
0	-	-	-	1xxxxx	Unallocated.
0	-	1	-	-	Unallocated.
0	00	0	0	0xxxxx	EXTR - 32-bit variant
1	-	0	-	-	Unallocated.
1	00	1	0	-	EXTR - 64-bit variant

C4.1.65 Branches, Exception Generating and System instructions

This section describes the encoding of the Branches, Exception Generating and System instructions group. The encodings in this section are decoded from *A64 instruction set encoding* on page C4-380.

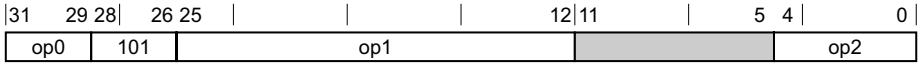


Table C4-66 Encoding table for the Branches, Exception Generating and System instructions group

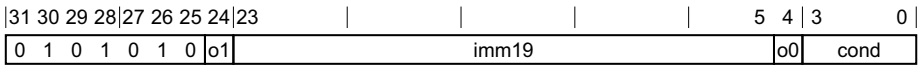
Decode fields			Decode group or instruction page
op0	op1	op2	
010	0xxxxxxxxxxxx	-	*Conditional branch (immediate)* on page C4-528
110	00xxxxxxxxxxx	-	*Exception generation* on page C4-528
110	01000000110001	-	*System instructions with register argument* on page C4-529
110	01000000110010	11111	*Hints* on page C4-530
110	01000000110011	-	*Barriers* on page C4-531
110	0100000xxx0100	-	*PSTATE* on page C4-532
110	0100100xxxxxxx	-	*System with result* on page C4-532
110	0100x01xxxxxxx	-	*System instructions* on page C4-532

Table C4-66 Encoding table for the Branches, Exception Generating and System instructions group (continued)

Decode fields			Decode group or instruction page
op0	op1	op2	
110	0100x1xxxxxxxx	-	*System register move* on page C4-533
110	1xxxxxxxxxxxx	-	*Unconditional branch (register)* on page C4-533
x00	-	-	*Unconditional branch (immediate)* on page C4-536
x01	0xxxxxxxxxxxx	-	*Compare and branch (immediate)* on page C4-536
x01	1xxxxxxxxxxxx	-	*Test and branch (immediate)* on page C4-537

Conditional branch (immediate)

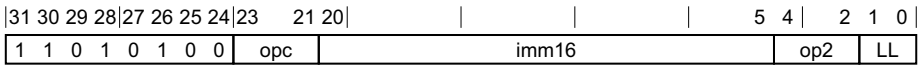
This section describes the encoding of the Conditional branch (immediate) instruction class. The encodings in this section are decoded from *Branches, Exception Generating and System instructions* on page C4-527.



Decode fields		Instruction page	Feature
o1	o0		
0	0	B.cond	-
0	1	BC.cond	FEAT_HBC
1	-	Unallocated.	-

Exception generation

This section describes the encoding of the Exception generation instruction class. The encodings in this section are decoded from *Branches, Exception Generating and System instructions* on page C4-527.

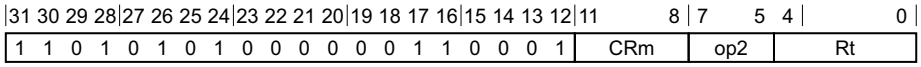


Decode fields			Instruction page	Feature
opc	op2	LL		
-	001	-	Unallocated.	-
-	01x	-	Unallocated.	-
-	1xx	-	Unallocated.	-
000	000	00	Unallocated.	-

Decode fields			Instruction page	Feature
opc	op2	LL		
000	000	01	SVC	-
000	000	10	HVC	-
000	000	11	SMC	-
001	000	x1	Unallocated.	-
001	000	00	BRK	-
001	000	1x	Unallocated.	-
010	000	x1	Unallocated.	-
010	000	00	HLT	-
010	000	1x	Unallocated.	-
011	000	00	TCANCEL	FEAT_TME
011	000	01	Unallocated.	-
011	000	1x	Unallocated.	-
100	000	-	Unallocated.	-
101	000	00	Unallocated.	-
101	000	01	DCPS1	-
101	000	10	DCPS2	-
101	000	11	DCPS3	-
110	000	-	Unallocated.	-
111	000	-	Unallocated.	-

System instructions with register argument

This section describes the encoding of the System instructions with register argument instruction class. The encodings in this section are decoded from *Branches, Exception Generating and System instructions* on page C4-527.

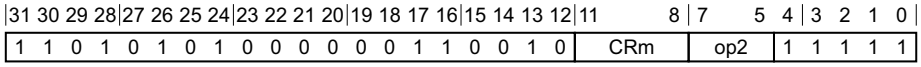


Decode fields		Instruction page	Feature
CRm	op2		
!= 0000	-	Unallocated.	-
0000	000	WFET	FEAT_WFxT

Decode fields		Instruction page	Feature
CRm	op2		
0000	001	WFIT	FEAT_WFxT
0000	01x	Unallocated.	-
0000	1xx	Unallocated.	-

Hints

This section describes the encoding of the Hints instruction class. The encodings in this section are decoded from *Branches, Exception Generating and System instructions* on page C4-527.

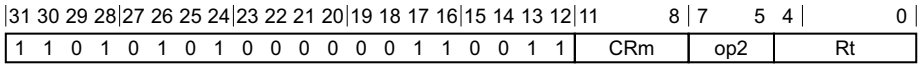


Decode fields		Instruction page	Feature
CRm	op2		
-	-	HINT	-
0000	000	NOP	-
0000	001	YIELD	-
0000	010	WFE	-
0000	011	WFI	-
0000	100	SEV	-
0000	101	SEVL	-
0000	110	DGH	-
0000	111	XPACD, XPACI, XPACLRI	FEAT_PAuth
0001	000	PACIA, PACIA1716, PACIASP, PACIAZ, PACIZA - PACIA1716 variant	FEAT_PAuth
0001	010	PACIB, PACIB1716, PACIBSP, PACIBZ, PACIZB - PACIB1716 variant	FEAT_PAuth
0001	100	AUTIA, AUTIA1716, AUTIASP, AUTIAZ, AUTIZA - AUTIA1716 variant	FEAT_PAuth
0001	110	AUTIB, AUTIB1716, AUTIBSP, AUTIBZ, AUTIZB - AUTIB1716 variant	FEAT_PAuth
0010	000	ESB	FEAT_RAS
0010	001	PSB CSYNC	FEAT_SPE
0010	010	TSB CSYNC	FEAT_TRF
0010	100	CSDB	-
0011	000	PACIA, PACIA1716, PACIASP, PACIAZ, PACIZA - PACIAZ variant	FEAT_PAuth
0011	001	PACIA, PACIA1716, PACIASP, PACIAZ, PACIZA - PACIASP variant	FEAT_PAuth
0011	010	PACIB, PACIB1716, PACIBSP, PACIBZ, PACIZB - PACIBZ variant	FEAT_PAuth

Decode fields		Instruction page	Feature
CRm	op2		
0011	011	PACIB, PACIB1716, PACIBSP, PACIBZ, PACIZB - PACIBSP variant	FEAT_PAuth
0011	100	AUTIA, AUTIA1716, AUTIASP, AUTIAZ, AUTIZA - AUTIAZ variant	FEAT_PAuth
0011	101	AUTIA, AUTIA1716, AUTIASP, AUTIAZ, AUTIZA - AUTIASP variant	FEAT_PAuth
0011	110	AUTIB, AUTIB1716, AUTIBSP, AUTIBZ, AUTIZB - AUTIBZ variant	FEAT_PAuth
0011	111	AUTIB, AUTIB1716, AUTIBSP, AUTIBZ, AUTIZB - AUTIBSP variant	FEAT_PAuth
0100	xx0	BTI	FEAT_BTI

Barriers

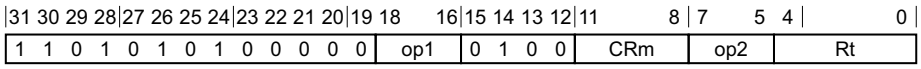
This section describes the encoding of the Barriers instruction class. The encodings in this section are decoded from *Branches, Exception Generating and System instructions* on page C4-527.



Decode fields			Instruction page	Feature
CRm	op2	Rt		
-	000	-	Unallocated.	-
-	001	!= 11111	Unallocated.	-
-	010	11111	CLREX	-
-	100	11111	DSB - Encoding	-
-	101	11111	DMB	-
-	110	11111	ISB	-
-	111	!= 11111	Unallocated.	-
-	111	11111	SB	-
xx0x	001	11111	Unallocated.	-
xx10	001	11111	DSB - Encoding	FEAT_XS
xx11	001	11111	Unallocated.	-
0000	011	11111	TCOMMIT	FEAT_TME
0001	011	-	Unallocated.	-
001x	011	-	Unallocated.	-
01xx	011	-	Unallocated.	-
1xxx	011	-	Unallocated.	-

PSTATE

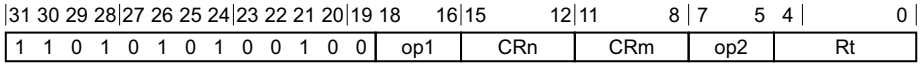
This section describes the encoding of the PSTATE instruction class. The encodings in this section are decoded from *Branches, Exception Generating and System instructions* on page C4-527.



Decode fields			Instruction page	Feature
op1	op2	Rt		
-	-	!= 11111	Unallocated.	-
-	-	11111	MSR (immediate)	-
000	000	11111	CFINV	FEAT_FlagM
000	001	11111	XAFLAG	FEAT_FlagM2
000	010	11111	AXFLAG	FEAT_FlagM2

System with result

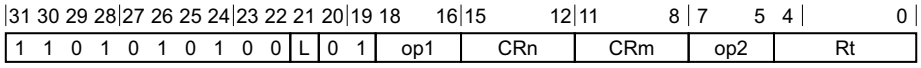
This section describes the encoding of the System with result instruction class. The encodings in this section are decoded from *Branches, Exception Generating and System instructions* on page C4-527.



Decode fields				Instruction page	Feature
op1	CRn	CRm	op2		
!= 011	-	-	-	Unallocated.	-
011	!= 0011	-	-	Unallocated.	-
011	0011	-	!= 011	Unallocated.	-
011	0011	!= 000x	011	Unallocated.	-
011	0011	0000	011	TSTART	FEAT_TME
011	0011	0001	011	TTEST	FEAT_TME

System instructions

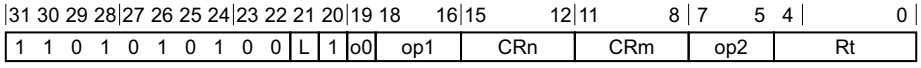
This section describes the encoding of the System instructions instruction class. The encodings in this section are decoded from *Branches, Exception Generating and System instructions* on page C4-527.



Decode fields	Instruction page
L	
0	SYS
1	SYSL

System register move

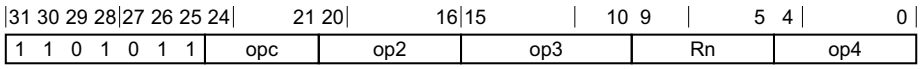
This section describes the encoding of the System register move instruction class. The encodings in this section are decoded from *Branches, Exception Generating and System instructions* on page C4-527.



Decode fields	Instruction page
L	
0	MSR (register)
1	MRS

Unconditional branch (register)

This section describes the encoding of the Unconditional branch (register) instruction class. The encodings in this section are decoded from *Branches, Exception Generating and System instructions* on page C4-527.



Decode fields					Instruction page	Feature
opc	op2	op3	Rn	op4		
-	!= 11111	-	-	-	Unallocated.	-
0000	11111	000000	-	!= 00000	Unallocated.	-
0000	11111	000000	-	00000	BR	-
0000	11111	000001	-	-	Unallocated.	-
0000	11111	000010	-	!= 11111	Unallocated.	-
0000	11111	000010	-	11111	BRAA, BRAAZ, BRAB, BRABZ - Key A, zero modifier variant	FEAT_PAuth

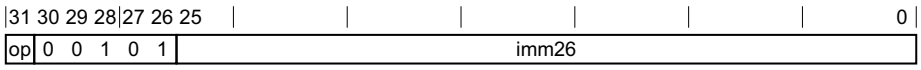
Decode fields					Instruction page	Feature
opc	op2	op3	Rn	op4		
0000	11111	000011	-	!= 11111	Unallocated.	-
0000	11111	000011	-	11111	BRAA, BRAAZ, BRAB, BRABZ - Key B, zero modifier variant	FEAT_PAuth
0000	11111	0001xx	-	-	Unallocated.	-
0000	11111	001xxx	-	-	Unallocated.	-
0000	11111	01xxxx	-	-	Unallocated.	-
0000	11111	1xxxxx	-	-	Unallocated.	-
0001	11111	000000	-	!= 00000	Unallocated.	-
0001	11111	000000	-	00000	BLR	-
0001	11111	000001	-	-	Unallocated.	-
0001	11111	000010	-	!= 11111	Unallocated.	-
0001	11111	000010	-	11111	BLRAA, BLRAAZ, BLRAB, BLRABZ - Key A, zero modifier variant	FEAT_PAuth
0001	11111	000011	-	!= 11111	Unallocated.	-
0001	11111	000011	-	11111	BLRAA, BLRAAZ, BLRAB, BLRABZ - Key B, zero modifier variant	FEAT_PAuth
0001	11111	0001xx	-	-	Unallocated.	-
0001	11111	001xxx	-	-	Unallocated.	-
0001	11111	01xxxx	-	-	Unallocated.	-
0001	11111	1xxxxx	-	-	Unallocated.	-
0010	11111	000000	-	!= 00000	Unallocated.	-
0010	11111	000000	-	00000	RET	-
0010	11111	000001	-	-	Unallocated.	-
0010	11111	000010	!= 11111	!= 11111	Unallocated.	-
0010	11111	000010	!= 11111	11111	Unallocated.	-
0010	11111	000010	11111	!= 11111	Unallocated.	-
0010	11111	000010	11111	11111	RETAA, RETAB - RETAA variant	FEAT_PAuth
0010	11111	000011	!= 11111	!= 11111	Unallocated.	-
0010	11111	000011	!= 11111	11111	Unallocated.	-
0010	11111	000011	11111	!= 11111	Unallocated.	-
0010	11111	000011	11111	11111	RETAA, RETAB - RETAB variant	FEAT_PAuth
0010	11111	0001xx	-	-	Unallocated.	-
0010	11111	001xxx	-	-	Unallocated.	-

Decode fields					Instruction page	Feature
opc	op2	op3	Rn	op4		
0010	11111	01xxxx	-	-	Unallocated.	-
0010	11111	1xxxxx	-	-	Unallocated.	-
0011	11111	-	-	-	Unallocated.	-
0100	11111	000000	!= 11111	!= 00000	Unallocated.	-
0100	11111	000000	!= 11111	00000	Unallocated.	-
0100	11111	000000	11111	!= 00000	Unallocated.	-
0100	11111	000000	11111	00000	ERET	-
0100	11111	000001	-	-	Unallocated.	-
0100	11111	000010	!= 11111	!= 11111	Unallocated.	-
0100	11111	000010	!= 11111	11111	Unallocated.	-
0100	11111	000010	11111	!= 11111	Unallocated.	-
0100	11111	000010	11111	11111	ERETAA, ERETAB - ERETAA variant	FEAT_PAuth
0100	11111	000011	!= 11111	!= 11111	Unallocated.	-
0100	11111	000011	!= 11111	11111	Unallocated.	-
0100	11111	000011	11111	!= 11111	Unallocated.	-
0100	11111	000011	11111	11111	ERETAA, ERETAB - ERETAB variant	FEAT_PAuth
0100	11111	0001xx	-	-	Unallocated.	-
0100	11111	001xxx	-	-	Unallocated.	-
0100	11111	01xxxx	-	-	Unallocated.	-
0100	11111	1xxxxx	-	-	Unallocated.	-
0101	11111	!= 000000	-	-	Unallocated.	-
0101	11111	000000	!= 11111	!= 00000	Unallocated.	-
0101	11111	000000	!= 11111	00000	Unallocated.	-
0101	11111	000000	11111	!= 00000	Unallocated.	-
0101	11111	000000	11111	00000	DRPS	-
011x	11111	-	-	-	Unallocated.	-
1000	11111	00000x	-	-	Unallocated.	-
1000	11111	000010	-	-	BRAA, BRAAZ, BRAB, BRABZ - Key A, register modifier variant	FEAT_PAuth
1000	11111	000011	-	-	BRAA, BRAAZ, BRAB, BRABZ - Key B, register modifier variant	FEAT_PAuth
1000	11111	0001xx	-	-	Unallocated.	-
1000	11111	001xxx	-	-	Unallocated.	-

Decode fields					Instruction page	Feature
opc	op2	op3	Rn	op4		
1000	11111	01xxxx	-	-	Unallocated.	-
1000	11111	1xxxxx	-	-	Unallocated.	-
1001	11111	00000x	-	-	Unallocated.	-
1001	11111	000010	-	-	BLRAA, BLRAAZ, BLRAB, BLRABZ - Key A, register modifier variant	FEAT_PAuth
1001	11111	000011	-	-	BLRAA, BLRAAZ, BLRAB, BLRABZ - Key B, register modifier variant	FEAT_PAuth
1001	11111	0001xx	-	-	Unallocated.	-
1001	11111	001xxx	-	-	Unallocated.	-
1001	11111	01xxxx	-	-	Unallocated.	-
1001	11111	1xxxxx	-	-	Unallocated.	-
101x	11111	-	-	-	Unallocated.	-
11xx	11111	-	-	-	Unallocated.	-

Unconditional branch (immediate)

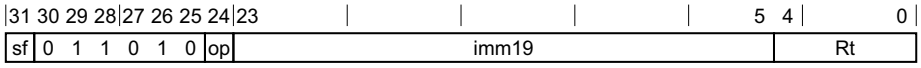
This section describes the encoding of the Unconditional branch (immediate) instruction class. The encodings in this section are decoded from *Branches, Exception Generating and System instructions* on page C4-527.



Decode fields	Instruction page
op	
0	B
1	BL

Compare and branch (immediate)

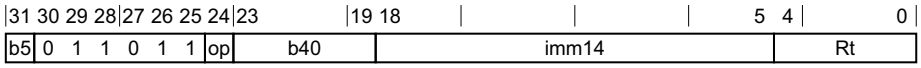
This section describes the encoding of the Compare and branch (immediate) instruction class. The encodings in this section are decoded from *Branches, Exception Generating and System instructions* on page C4-527.



Decode fields		Instruction page
sf	op	
0	0	CBZ - 32-bit variant
0	1	CBNZ - 32-bit variant
1	0	CBZ - 64-bit variant
1	1	CBNZ - 64-bit variant

Test and branch (immediate)

This section describes the encoding of the Test and branch (immediate) instruction class. The encodings in this section are decoded from *Branches, Exception Generating and System instructions* on page C4-527.



Decode fields	Instruction page
op	
0	TBZ
1	TBNZ

C4.1.66 Loads and Stores

This section describes the encoding of the Loads and Stores group. The encodings in this section are decoded from *A64 instruction set encoding* on page C4-380.

Table C4-67 Encoding table for the Loads and Stores group

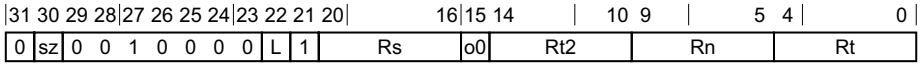
Decode fields					Decode group or instruction page
op0	op1	op2	op3	op4	
0x00	0	00	1xxxxx	-	*Compare and swap pair* on page C4-539
0x00	1	00	000000	-	*Advanced SIMD load/store multiple structures* on page C4-539
0x00	1	01	0xxxxx	-	*Advanced SIMD load/store multiple structures (post-indexed)* on page C4-540

Table C4-67 Encoding table for the Loads and Stores group (continued)

Decode fields					Decode group or instruction page
op0	op1	op2	op3	op4	
0x00	1	0x	1xxxxx	-	Unallocated.
0x00	1	10	x00000	-	*Advanced SIMD load/store single structure* on page C4-542
0x00	1	11	-	-	*Advanced SIMD load/store single structure (post-indexed)* on page C4-544
0x00	1	x0	x1xxxx	-	Unallocated.
0x00	1	x0	xx1xxx	-	Unallocated.
0x00	1	x0	xxx1xx	-	Unallocated.
0x00	1	x0	xxxx1x	-	Unallocated.
0x00	1	x0	xxxxx1	-	Unallocated.
1101	0	1x	1xxxxx	-	*Load/store memory tags* on page C4-548
1x00	0	00	1xxxxx	-	*Load/store exclusive pair* on page C4-549
1x00	1	-	-	-	Unallocated.
xx00	0	00	0xxxxx	-	*Load/store exclusive register* on page C4-549
xx00	0	01	0xxxxx	-	*Load/store ordered* on page C4-550
xx00	0	01	1xxxxx	-	*Compare and swap* on page C4-551
xx01	0	1x	0xxxxx	00	*LDAPR/STLR (unscaled immediate)* on page C4-552
xx01	-	0x	-	-	*Load register (literal)* on page C4-552
xx01	-	1x	0xxxxx	01	*Memory Copy and Memory Set* on page C4-553
xx10	-	00	-	-	*Load/store no-allocate pair (offset)* on page C4-557
xx10	-	01	-	-	*Load/store register pair (post-indexed)* on page C4-558
xx10	-	10	-	-	*Load/store register pair (offset)* on page C4-558
xx10	-	11	-	-	*Load/store register pair (pre-indexed)* on page C4-559
xx11	-	0x	0xxxxx	00	*Load/store register (unscaled immediate)* on page C4-560
xx11	-	0x	0xxxxx	01	*Load/store register (immediate post-indexed)* on page C4-561
xx11	-	0x	0xxxxx	10	*Load/store register (unprivileged)* on page C4-562
xx11	-	0x	0xxxxx	11	*Load/store register (immediate pre-indexed)* on page C4-563
xx11	-	0x	1xxxxx	00	*Atomic memory operations* on page C4-564
xx11	-	0x	1xxxxx	10	*Load/store register (register offset)* on page C4-573
xx11	-	0x	1xxxxx	x1	*Load/store register (pac)* on page C4-575
xx11	-	1x	-	-	*Load/store register (unsigned immediate)* on page C4-575

Compare and swap pair

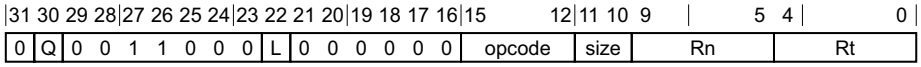
This section describes the encoding of the Compare and swap pair instruction class. The encodings in this section are decoded from *Loads and Stores* on page C4-537.



Decode fields				Instruction page	Feature
sz	L	o0	Rt2		
-	-	-	!= 11111	Unallocated.	-
0	0	0	11111	CASP, CASPA, CASPAL, CASPL - 32-bit CASP variant	FEAT_LSE
0	0	1	11111	CASP, CASPA, CASPAL, CASPL - 32-bit CASPL variant	FEAT_LSE
0	1	0	11111	CASP, CASPA, CASPAL, CASPL - 32-bit CASPA variant	FEAT_LSE
0	1	1	11111	CASP, CASPA, CASPAL, CASPL - 32-bit CASPAL variant	FEAT_LSE
1	0	0	11111	CASP, CASPA, CASPAL, CASPL - 64-bit CASP variant	FEAT_LSE
1	0	1	11111	CASP, CASPA, CASPAL, CASPL - 64-bit CASPL variant	FEAT_LSE
1	1	0	11111	CASP, CASPA, CASPAL, CASPL - 64-bit CASPA variant	FEAT_LSE
1	1	1	11111	CASP, CASPA, CASPAL, CASPL - 64-bit CASPAL variant	FEAT_LSE

Advanced SIMD load/store multiple structures

This section describes the encoding of the Advanced SIMD load/store multiple structures instruction class. The encodings in this section are decoded from *Loads and Stores* on page C4-537.

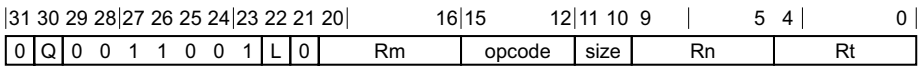


Decode fields		Instruction page
L	opcode	
0	0000	ST4 (multiple structures)
0	0001	Unallocated.
0	0010	ST1 (multiple structures) - Four registers variant
0	0011	Unallocated.
0	0100	ST3 (multiple structures)
0	0101	Unallocated.
0	0110	ST1 (multiple structures) - Three registers variant
0	0111	ST1 (multiple structures) - One register variant

Decode fields		Instruction page
L	opcode	
0	1000	ST2 (multiple structures)
0	1001	Unallocated.
0	1010	ST1 (multiple structures) - Two registers variant
0	1011	Unallocated.
0	11xx	Unallocated.
1	0000	LD4 (multiple structures)
1	0001	Unallocated.
1	0010	LD1 (multiple structures) - Four registers variant
1	0011	Unallocated.
1	0100	LD3 (multiple structures)
1	0101	Unallocated.
1	0110	LD1 (multiple structures) - Three registers variant
1	0111	LD1 (multiple structures) - One register variant
1	1000	LD2 (multiple structures)
1	1001	Unallocated.
1	1010	LD1 (multiple structures) - Two registers variant
1	1011	Unallocated.
1	11xx	Unallocated.

Advanced SIMD load/store multiple structures (post-indexed)

This section describes the encoding of the Advanced SIMD load/store multiple structures (post-indexed) instruction class. The encodings in this section are decoded from *Loads and Stores* on page C4-537.



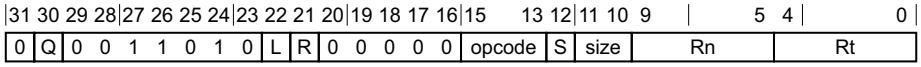
Decode fields			Instruction page
L	Rm	opcode	
0	-	0001	Unallocated.
0	-	0011	Unallocated.
0	-	0101	Unallocated.
0	-	1001	Unallocated.
0	-	1011	Unallocated.

Decode fields			Instruction page
L	Rm	opcode	
0	-	11xx	Unallocated.
0	!= 11111	0000	ST4 (multiple structures) - Register offset variant
0	!= 11111	0010	ST1 (multiple structures) - Four registers, register offset variant
0	!= 11111	0100	ST3 (multiple structures) - Register offset variant
0	!= 11111	0110	ST1 (multiple structures) - Three registers, register offset variant
0	!= 11111	0111	ST1 (multiple structures) - One register, register offset variant
0	!= 11111	1000	ST2 (multiple structures) - Register offset variant
0	!= 11111	1010	ST1 (multiple structures) - Two registers, register offset variant
0	11111	0000	ST4 (multiple structures) - Immediate offset variant
0	11111	0010	ST1 (multiple structures) - Four registers, immediate offset variant
0	11111	0100	ST3 (multiple structures) - Immediate offset variant
0	11111	0110	ST1 (multiple structures) - Three registers, immediate offset variant
0	11111	0111	ST1 (multiple structures) - One register, immediate offset variant
0	11111	1000	ST2 (multiple structures) - Immediate offset variant
0	11111	1010	ST1 (multiple structures) - Two registers, immediate offset variant
1	-	0001	Unallocated.
1	-	0011	Unallocated.
1	-	0101	Unallocated.
1	-	1001	Unallocated.
1	-	1011	Unallocated.
1	-	11xx	Unallocated.
1	!= 11111	0000	LD4 (multiple structures) - Register offset variant
1	!= 11111	0010	LD1 (multiple structures) - Four registers, register offset variant
1	!= 11111	0100	LD3 (multiple structures) - Register offset variant
1	!= 11111	0110	LD1 (multiple structures) - Three registers, register offset variant
1	!= 11111	0111	LD1 (multiple structures) - One register, register offset variant
1	!= 11111	1000	LD2 (multiple structures) - Register offset variant
1	!= 11111	1010	LD1 (multiple structures) - Two registers, register offset variant
1	11111	0000	LD4 (multiple structures) - Immediate offset variant
1	11111	0010	LD1 (multiple structures) - Four registers, immediate offset variant
1	11111	0100	LD3 (multiple structures) - Immediate offset variant
1	11111	0110	LD1 (multiple structures) - Three registers, immediate offset variant

Decode fields			Instruction page
L	Rm	opcode	
1	11111	0111	LD1 (multiple structures) - One register, immediate offset variant
1	11111	1000	LD2 (multiple structures) - Immediate offset variant
1	11111	1010	LD1 (multiple structures) - Two registers, immediate offset variant

Advanced SIMD load/store single structure

This section describes the encoding of the Advanced SIMD load/store single structure instruction class. The encodings in this section are decoded from *Loads and Stores* on page C4-537.



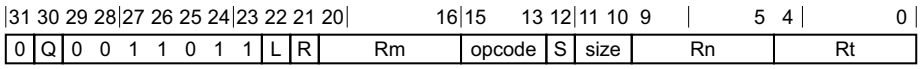
Decode fields					Instruction page
L	R	opcode	S	size	
0	-	11x	-	-	Unallocated.
0	0	000	-	-	ST1 (single structure) - 8-bit variant
0	0	001	-	-	ST3 (single structure) - 8-bit variant
0	0	010	-	x0	ST1 (single structure) - 16-bit variant
0	0	010	-	x1	Unallocated.
0	0	011	-	x0	ST3 (single structure) - 16-bit variant
0	0	011	-	x1	Unallocated.
0	0	100	-	00	ST1 (single structure) - 32-bit variant
0	0	100	-	1x	Unallocated.
0	0	100	0	01	ST1 (single structure) - 64-bit variant
0	0	100	1	01	Unallocated.
0	0	101	-	00	ST3 (single structure) - 32-bit variant
0	0	101	-	10	Unallocated.
0	0	101	0	01	ST3 (single structure) - 64-bit variant
0	0	101	0	11	Unallocated.
0	0	101	1	x1	Unallocated.
0	1	000	-	-	ST2 (single structure) - 8-bit variant
0	1	001	-	-	ST4 (single structure) - 8-bit variant
0	1	010	-	x0	ST2 (single structure) - 16-bit variant
0	1	010	-	x1	Unallocated.

Decode fields					Instruction page
L	R	opcode	S	size	
0	1	011	-	x0	ST4 (single structure) - 16-bit variant
0	1	011	-	x1	Unallocated.
0	1	100	-	00	ST2 (single structure) - 32-bit variant
0	1	100	-	10	Unallocated.
0	1	100	0	01	ST2 (single structure) - 64-bit variant
0	1	100	0	11	Unallocated.
0	1	100	1	x1	Unallocated.
0	1	101	-	00	ST4 (single structure) - 32-bit variant
0	1	101	-	10	Unallocated.
0	1	101	0	01	ST4 (single structure) - 64-bit variant
0	1	101	0	11	Unallocated.
0	1	101	1	x1	Unallocated.
1	0	000	-	-	LD1 (single structure) - 8-bit variant
1	0	001	-	-	LD3 (single structure) - 8-bit variant
1	0	010	-	x0	LD1 (single structure) - 16-bit variant
1	0	010	-	x1	Unallocated.
1	0	011	-	x0	LD3 (single structure) - 16-bit variant
1	0	011	-	x1	Unallocated.
1	0	100	-	00	LD1 (single structure) - 32-bit variant
1	0	100	-	1x	Unallocated.
1	0	100	0	01	LD1 (single structure) - 64-bit variant
1	0	100	1	01	Unallocated.
1	0	101	-	00	LD3 (single structure) - 32-bit variant
1	0	101	-	10	Unallocated.
1	0	101	0	01	LD3 (single structure) - 64-bit variant
1	0	101	0	11	Unallocated.
1	0	101	1	x1	Unallocated.
1	0	110	0	-	LD1R
1	0	110	1	-	Unallocated.
1	0	111	0	-	LD3R
1	0	111	1	-	Unallocated.
1	1	000	-	-	LD2 (single structure) - 8-bit variant

Decode fields					Instruction page
L	R	opcode	S	size	
1	1	001	-	-	LD4 (single structure) - 8-bit variant
1	1	010	-	x0	LD2 (single structure) - 16-bit variant
1	1	010	-	x1	Unallocated.
1	1	011	-	x0	LD4 (single structure) - 16-bit variant
1	1	011	-	x1	Unallocated.
1	1	100	-	00	LD2 (single structure) - 32-bit variant
1	1	100	-	10	Unallocated.
1	1	100	0	01	LD2 (single structure) - 64-bit variant
1	1	100	0	11	Unallocated.
1	1	100	1	x1	Unallocated.
1	1	101	-	00	LD4 (single structure) - 32-bit variant
1	1	101	-	10	Unallocated.
1	1	101	0	01	LD4 (single structure) - 64-bit variant
1	1	101	0	11	Unallocated.
1	1	101	1	x1	Unallocated.
1	1	110	0	-	LD2R
1	1	110	1	-	Unallocated.
1	1	111	0	-	LD4R
1	1	111	1	-	Unallocated.

Advanced SIMD load/store single structure (post-indexed)

This section describes the encoding of the Advanced SIMD load/store single structure (post-indexed) instruction class. The encodings in this section are decoded from *Loads and Stores* on page C4-537.



Decode fields						Instruction page
L	R	Rm	opcode	S	size	
0	-	-	11x	-	-	Unallocated.
0	0	-	010	-	x1	Unallocated.
0	0	-	011	-	x1	Unallocated.
0	0	-	100	-	1x	Unallocated.

Decode fields						Instruction page
L	R	Rm	opcode	S	size	
0	0	-	100	1	01	Unallocated.
0	0	-	101	-	10	Unallocated.
0	0	-	101	0	11	Unallocated.
0	0	-	101	1	x1	Unallocated.
0	0	!= 11111	000	-	-	ST1 (single structure) - 8-bit, register offset variant
0	0	!= 11111	001	-	-	ST3 (single structure) - 8-bit, register offset variant
0	0	!= 11111	010	-	x0	ST1 (single structure) - 16-bit, register offset variant
0	0	!= 11111	011	-	x0	ST3 (single structure) - 16-bit, register offset variant
0	0	!= 11111	100	-	00	ST1 (single structure) - 32-bit, register offset variant
0	0	!= 11111	100	0	01	ST1 (single structure) - 64-bit, register offset variant
0	0	!= 11111	101	-	00	ST3 (single structure) - 32-bit, register offset variant
0	0	!= 11111	101	0	01	ST3 (single structure) - 64-bit, register offset variant
0	0	11111	000	-	-	ST1 (single structure) - 8-bit, immediate offset variant
0	0	11111	001	-	-	ST3 (single structure) - 8-bit, immediate offset variant
0	0	11111	010	-	x0	ST1 (single structure) - 16-bit, immediate offset variant
0	0	11111	011	-	x0	ST3 (single structure) - 16-bit, immediate offset variant
0	0	11111	100	-	00	ST1 (single structure) - 32-bit, immediate offset variant
0	0	11111	100	0	01	ST1 (single structure) - 64-bit, immediate offset variant
0	0	11111	101	-	00	ST3 (single structure) - 32-bit, immediate offset variant
0	0	11111	101	0	01	ST3 (single structure) - 64-bit, immediate offset variant
0	1	-	010	-	x1	Unallocated.
0	1	-	011	-	x1	Unallocated.
0	1	-	100	-	10	Unallocated.
0	1	-	100	0	11	Unallocated.
0	1	-	100	1	x1	Unallocated.
0	1	-	101	-	10	Unallocated.
0	1	-	101	0	11	Unallocated.
0	1	-	101	1	x1	Unallocated.
0	1	!= 11111	000	-	-	ST2 (single structure) - 8-bit, register offset variant
0	1	!= 11111	001	-	-	ST4 (single structure) - 8-bit, register offset variant
0	1	!= 11111	010	-	x0	ST2 (single structure) - 16-bit, register offset variant
0	1	!= 11111	011	-	x0	ST4 (single structure) - 16-bit, register offset variant

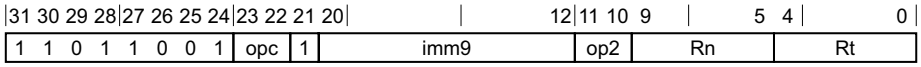
Decode fields						Instruction page
L	R	Rm	opcode	S	size	
0	1	!= 11111	100	-	00	ST2 (single structure) - 32-bit, register offset variant
0	1	!= 11111	100	0	01	ST2 (single structure) - 64-bit, register offset variant
0	1	!= 11111	101	-	00	ST4 (single structure) - 32-bit, register offset variant
0	1	!= 11111	101	0	01	ST4 (single structure) - 64-bit, register offset variant
0	1	11111	000	-	-	ST2 (single structure) - 8-bit, immediate offset variant
0	1	11111	001	-	-	ST4 (single structure) - 8-bit, immediate offset variant
0	1	11111	010	-	x0	ST2 (single structure) - 16-bit, immediate offset variant
0	1	11111	011	-	x0	ST4 (single structure) - 16-bit, immediate offset variant
0	1	11111	100	-	00	ST2 (single structure) - 32-bit, immediate offset variant
0	1	11111	100	0	01	ST2 (single structure) - 64-bit, immediate offset variant
0	1	11111	101	-	00	ST4 (single structure) - 32-bit, immediate offset variant
0	1	11111	101	0	01	ST4 (single structure) - 64-bit, immediate offset variant
1	0	-	010	-	x1	Unallocated.
1	0	-	011	-	x1	Unallocated.
1	0	-	100	-	1x	Unallocated.
1	0	-	100	1	01	Unallocated.
1	0	-	101	-	10	Unallocated.
1	0	-	101	0	11	Unallocated.
1	0	-	101	1	x1	Unallocated.
1	0	-	110	1	-	Unallocated.
1	0	-	111	1	-	Unallocated.
1	0	!= 11111	000	-	-	LD1 (single structure) - 8-bit, register offset variant
1	0	!= 11111	001	-	-	LD3 (single structure) - 8-bit, register offset variant
1	0	!= 11111	010	-	x0	LD1 (single structure) - 16-bit, register offset variant
1	0	!= 11111	011	-	x0	LD3 (single structure) - 16-bit, register offset variant
1	0	!= 11111	100	-	00	LD1 (single structure) - 32-bit, register offset variant
1	0	!= 11111	100	0	01	LD1 (single structure) - 64-bit, register offset variant
1	0	!= 11111	101	-	00	LD3 (single structure) - 32-bit, register offset variant
1	0	!= 11111	101	0	01	LD3 (single structure) - 64-bit, register offset variant
1	0	!= 11111	110	0	-	LD1R - Register offset variant
1	0	!= 11111	111	0	-	LD3R - Register offset variant
1	0	11111	000	-	-	LD1 (single structure) - 8-bit, immediate offset variant

Decode fields						Instruction page
L	R	Rm	opcode	S	size	
1	0	11111	001	-	-	LD3 (single structure) - 8-bit, immediate offset variant
1	0	11111	010	-	x0	LD1 (single structure) - 16-bit, immediate offset variant
1	0	11111	011	-	x0	LD3 (single structure) - 16-bit, immediate offset variant
1	0	11111	100	-	00	LD1 (single structure) - 32-bit, immediate offset variant
1	0	11111	100	0	01	LD1 (single structure) - 64-bit, immediate offset variant
1	0	11111	101	-	00	LD3 (single structure) - 32-bit, immediate offset variant
1	0	11111	101	0	01	LD3 (single structure) - 64-bit, immediate offset variant
1	0	11111	110	0	-	LD1R - Immediate offset variant
1	0	11111	111	0	-	LD3R - Immediate offset variant
1	1	-	010	-	x1	Unallocated.
1	1	-	011	-	x1	Unallocated.
1	1	-	100	-	10	Unallocated.
1	1	-	100	0	11	Unallocated.
1	1	-	100	1	x1	Unallocated.
1	1	-	101	-	10	Unallocated.
1	1	-	101	0	11	Unallocated.
1	1	-	101	1	x1	Unallocated.
1	1	-	110	1	-	Unallocated.
1	1	-	111	1	-	Unallocated.
1	1	!= 11111	000	-	-	LD2 (single structure) - 8-bit, register offset variant
1	1	!= 11111	001	-	-	LD4 (single structure) - 8-bit, register offset variant
1	1	!= 11111	010	-	x0	LD2 (single structure) - 16-bit, register offset variant
1	1	!= 11111	011	-	x0	LD4 (single structure) - 16-bit, register offset variant
1	1	!= 11111	100	-	00	LD2 (single structure) - 32-bit, register offset variant
1	1	!= 11111	100	0	01	LD2 (single structure) - 64-bit, register offset variant
1	1	!= 11111	101	-	00	LD4 (single structure) - 32-bit, register offset variant
1	1	!= 11111	101	0	01	LD4 (single structure) - 64-bit, register offset variant
1	1	!= 11111	110	0	-	LD2R - Register offset variant
1	1	!= 11111	111	0	-	LD4R - Register offset variant
1	1	11111	000	-	-	LD2 (single structure) - 8-bit, immediate offset variant
1	1	11111	001	-	-	LD4 (single structure) - 8-bit, immediate offset variant
1	1	11111	010	-	x0	LD2 (single structure) - 16-bit, immediate offset variant

Decode fields						Instruction page
L	R	Rm	opcode	S	size	
1	1	11111	011	-	x0	LD4 (single structure) - 16-bit, immediate offset variant
1	1	11111	100	-	00	LD2 (single structure) - 32-bit, immediate offset variant
1	1	11111	100	0	01	LD2 (single structure) - 64-bit, immediate offset variant
1	1	11111	101	-	00	LD4 (single structure) - 32-bit, immediate offset variant
1	1	11111	101	0	01	LD4 (single structure) - 64-bit, immediate offset variant
1	1	11111	110	0	-	LD2R - Immediate offset variant
1	1	11111	111	0	-	LD4R - Immediate offset variant

Load/store memory tags

This section describes the encoding of the Load/store memory tags instruction class. The encodings in this section are decoded from *Loads and Stores* on page C4-537.

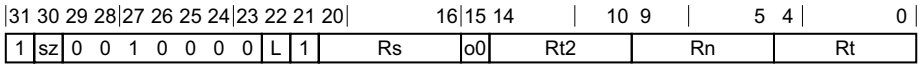


Decode fields			Instruction page	Feature
opc	imm9	op2		
00	-	01	STG - Encoding	FEAT_MTE
00	-	10	STG - Encoding	FEAT_MTE
00	-	11	STG - Encoding	FEAT_MTE
00	000000000	00	STZGM	FEAT_MTE2
01	-	00	LDG	FEAT_MTE
01	-	01	STZG - Encoding	FEAT_MTE
01	-	10	STZG - Encoding	FEAT_MTE
01	-	11	STZG - Encoding	FEAT_MTE
10	-	01	ST2G - Encoding	FEAT_MTE
10	-	10	ST2G - Encoding	FEAT_MTE
10	-	11	ST2G - Encoding	FEAT_MTE
10	!= 000000000	00	Unallocated.	-
10	000000000	00	STGM	FEAT_MTE2
11	-	01	STZ2G - Encoding	FEAT_MTE
11	-	10	STZ2G - Encoding	FEAT_MTE

Decode fields			Instruction page	Feature
opc	imm9	op2		
11	-	11	STZ2G - Encoding	FEAT_MTE
11	!= 000000000	00	Unallocated.	-
11	000000000	00	LDGM	FEAT_MTE2

Load/store exclusive pair

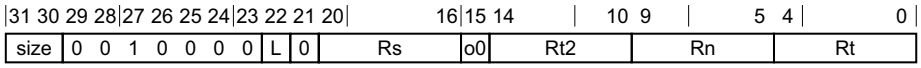
This section describes the encoding of the Load/store exclusive pair instruction class. The encodings in this section are decoded from *Loads and Stores* on page C4-537.



Decode fields			Instruction page
sz	L	o0	
0	0	0	STXP - 32-bit variant
0	0	1	STLXP - 32-bit variant
0	1	0	LDXP - 32-bit variant
0	1	1	LDAXP - 32-bit variant
1	0	0	STXP - 64-bit variant
1	0	1	STLXP - 64-bit variant
1	1	0	LDXP - 64-bit variant
1	1	1	LDAXP - 64-bit variant

Load/store exclusive register

This section describes the encoding of the Load/store exclusive register instruction class. The encodings in this section are decoded from *Loads and Stores* on page C4-537.

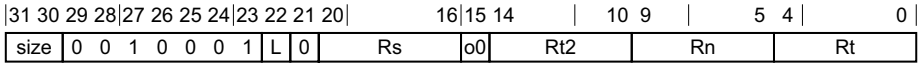


Decode fields			Instruction page
size	L	o0	
00	0	0	STXRB
00	0	1	STLXRB
00	1	0	LDXRB

Decode fields			Instruction page
size	L	o0	
00	1	1	LDAXRB
01	0	0	STXRH
01	0	1	STLXRH
01	1	0	LDXRH
01	1	1	LDAXRH
10	0	0	STXR - 32-bit variant
10	0	1	STLXR - 32-bit variant
10	1	0	LDXR - 32-bit variant
10	1	1	LDAXR - 32-bit variant
11	0	0	STXR - 64-bit variant
11	0	1	STLXR - 64-bit variant
11	1	0	LDXR - 64-bit variant
11	1	1	LDAXR - 64-bit variant

Load/store ordered

This section describes the encoding of the Load/store ordered instruction class. The encodings in this section are decoded from *Loads and Stores* on page C4-537.

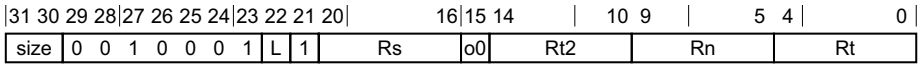


Decode fields			Instruction page	Feature
size	L	o0		
00	0	0	STLLRB	FEAT_LOR
00	0	1	STLRB	-
00	1	0	LDLARB	FEAT_LOR
00	1	1	LDARB	-
01	0	0	STLLRH	FEAT_LOR
01	0	1	STLRH	-
01	1	0	LDLARH	FEAT_LOR
01	1	1	LDARH	-
10	0	0	STLLR - 32-bit variant	FEAT_LOR
10	0	1	STLR - 32-bit variant	-

Decode fields			Instruction page	Feature
size	L	o0		
10	1	0	LDLAR - 32-bit variant	FEAT_LOR
10	1	1	LDAR - 32-bit variant	-
11	0	0	STLLR - 64-bit variant	FEAT_LOR
11	0	1	STLR - 64-bit variant	-
11	1	0	LDLAR - 64-bit variant	FEAT_LOR
11	1	1	LDAR - 64-bit variant	-

Compare and swap

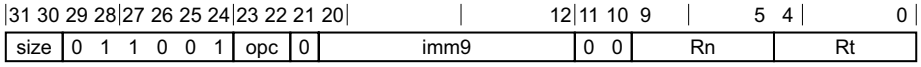
This section describes the encoding of the Compare and swap instruction class. The encodings in this section are decoded from *Loads and Stores* on page C4-537.



Decode fields				Instruction page	Feature
size	L	o0	Rt2		
-	-	-	!= 11111	Unallocated.	-
00	0	0	11111	CASB, CASAB, CASALB, CASLB - CASB variant	FEAT_LSE
00	0	1	11111	CASB, CASAB, CASALB, CASLB - CASLB variant	FEAT_LSE
00	1	0	11111	CASB, CASAB, CASALB, CASLB - CASAB variant	FEAT_LSE
00	1	1	11111	CASB, CASAB, CASALB, CASLB - CASALB variant	FEAT_LSE
01	0	0	11111	CASH, CASAH, CASALH, CASLH - CASH variant	FEAT_LSE
01	0	1	11111	CASH, CASAH, CASALH, CASLH - CASLH variant	FEAT_LSE
01	1	0	11111	CASH, CASAH, CASALH, CASLH - CASAH variant	FEAT_LSE
01	1	1	11111	CASH, CASAH, CASALH, CASLH - CASALH variant	FEAT_LSE
10	0	0	11111	CAS, CASA, CASAL, CASL - 32-bit CAS variant	FEAT_LSE
10	0	1	11111	CAS, CASA, CASAL, CASL - 32-bit CASL variant	FEAT_LSE
10	1	0	11111	CAS, CASA, CASAL, CASL - 32-bit CASA variant	FEAT_LSE
10	1	1	11111	CAS, CASA, CASAL, CASL - 32-bit CASAL variant	FEAT_LSE
11	0	0	11111	CAS, CASA, CASAL, CASL - 64-bit CAS variant	FEAT_LSE
11	0	1	11111	CAS, CASA, CASAL, CASL - 64-bit CASL variant	FEAT_LSE
11	1	0	11111	CAS, CASA, CASAL, CASL - 64-bit CASA variant	FEAT_LSE
11	1	1	11111	CAS, CASA, CASAL, CASL - 64-bit CASAL variant	FEAT_LSE

LDAPR/STLR (unscaled immediate)

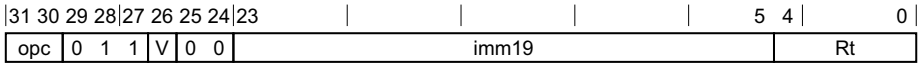
This section describes the encoding of the LDAPR/STLR (unscaled immediate) instruction class. The encodings in this section are decoded from *Loads and Stores* on page C4-537.



Decode fields		Instruction page	Feature
size	opc		
00	00	STLURB	FEAT_LRCPC2
00	01	LDAPURB	FEAT_LRCPC2
00	10	LDAPURSB - 64-bit variant	FEAT_LRCPC2
00	11	LDAPURSB - 32-bit variant	FEAT_LRCPC2
01	00	STLURH	FEAT_LRCPC2
01	01	LDAPURH	FEAT_LRCPC2
01	10	LDAPURSH - 64-bit variant	FEAT_LRCPC2
01	11	LDAPURSH - 32-bit variant	FEAT_LRCPC2
10	00	STLUR - 32-bit variant	FEAT_LRCPC2
10	01	LDAPUR - 32-bit variant	FEAT_LRCPC2
10	10	LDAPURSW	FEAT_LRCPC2
10	11	Unallocated.	-
11	00	STLUR - 64-bit variant	FEAT_LRCPC2
11	01	LDAPUR - 64-bit variant	FEAT_LRCPC2
11	10	Unallocated.	-
11	11	Unallocated.	-

Load register (literal)

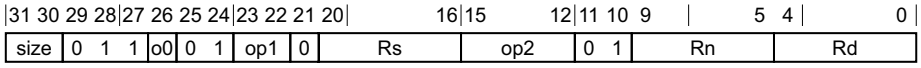
This section describes the encoding of the Load register (literal) instruction class. The encodings in this section are decoded from *Loads and Stores* on page C4-537.



Decode fields		Instruction page
opc	V	
00	0	LDR (literal) - 32-bit variant
00	1	LDR (literal, SIMD&FP) - 32-bit variant
01	0	LDR (literal) - 64-bit variant
01	1	LDR (literal, SIMD&FP) - 64-bit variant
10	0	LDRSW (literal)
10	1	LDR (literal, SIMD&FP) - 128-bit variant
11	0	PRFM (literal)
11	1	Unallocated.

Memory Copy and Memory Set

This section describes the encoding of the Memory Copy and Memory Set instruction class. The encodings in this section are decoded from *Loads and Stores* on page C4-537.



Decode fields			Instruction page	Feature
o0	op1	op2		
0	00	0000	CPYFP, CPYFM, CPYFE - Prologue variant	FEAT_MOPS
0	00	0001	CPYFPWT, CPYFMWT, CPYFEWT - Prologue variant	FEAT_MOPS
0	00	0010	CPYFPRT, CPYFMRT, CPYFERT - Prologue variant	FEAT_MOPS
0	00	0011	CPYFPT, CPYFMT, CPYFET - Prologue variant	FEAT_MOPS
0	00	0100	CPYFPWN, CPYFMWN, CPYFEWN - Prologue variant	FEAT_MOPS
0	00	0101	CPYFPWTWN, CPYFMWTWN, CPYFEWTWN - Prologue variant	FEAT_MOPS
0	00	0110	CPYFPRTWN, CPYFMRTWN, CPYFERTWN - Prologue variant	FEAT_MOPS
0	00	0111	CPYFPTWN, CPYFMTWN, CPYFETWN - Prologue variant	FEAT_MOPS
0	00	1000	CPYFPRN, CPYFMRN, CPYFERN - Prologue variant	FEAT_MOPS
0	00	1001	CPYFPWTRN, CPYFMWTRN, CPYFEWTRN - Prologue variant	FEAT_MOPS
0	00	1010	CPYFPRTRN, CPYFMRTRN, CPYFERTRN - Prologue variant	FEAT_MOPS

Decode fields			Instruction page	Feature
o0	op1	op2		
0	00	1011	CPYFPTRN, CPYFMTRN, CPYFETRN - Prologue variant	FEAT_MOPS
0	00	1100	CPYFPN, CPYFMN, CPYFEN - Prologue variant	FEAT_MOPS
0	00	1101	CPYFPWTN, CPYFMWTN, CPYFEWTN - Prologue variant	FEAT_MOPS
0	00	1110	CPYFPRTN, CPYFMRTN, CPYFERTN - Prologue variant	FEAT_MOPS
0	00	1111	CPYFPTN, CPYFMTN, CPYFETN - Prologue variant	FEAT_MOPS
0	01	0000	CPYFP, CPYFM, CPYFE - Main variant	FEAT_MOPS
0	01	0001	CPYFPWT, CPYFMWT, CPYFEWT - Main variant	FEAT_MOPS
0	01	0010	CPYFPRT, CPYFMRT, CPYFERT - Main variant	FEAT_MOPS
0	01	0011	CPYFPT, CPYFMT, CPYFET - Main variant	FEAT_MOPS
0	01	0100	CPYFPWN, CPYFMWN, CPYFEWN - Main variant	FEAT_MOPS
0	01	0101	CPYFPWTWN, CPYFMWTWN, CPYFEWTWN - Main variant	FEAT_MOPS
0	01	0110	CPYFPRTWN, CPYFMRTWN, CPYFERTWN - Main variant	FEAT_MOPS
0	01	0111	CPYFPTWN, CPYFMTWN, CPYFETWN - Main variant	FEAT_MOPS
0	01	1000	CPYFPRN, CPYFMRN, CPYFERN - Main variant	FEAT_MOPS
0	01	1001	CPYFPWTRN, CPYFMWTRN, CPYFEWTRN - Main variant	FEAT_MOPS
0	01	1010	CPYFPRTRN, CPYFMRTRN, CPYFERTRN - Main variant	FEAT_MOPS
0	01	1011	CPYFPTRN, CPYFMTRN, CPYFETRN - Main variant	FEAT_MOPS
0	01	1100	CPYFPN, CPYFMN, CPYFEN - Main variant	FEAT_MOPS
0	01	1101	CPYFPWTN, CPYFMWTN, CPYFEWTN - Main variant	FEAT_MOPS
0	01	1110	CPYFPRTN, CPYFMRTN, CPYFERTN - Main variant	FEAT_MOPS
0	01	1111	CPYFPTN, CPYFMTN, CPYFETN - Main variant	FEAT_MOPS
0	10	0000	CPYFP, CPYFM, CPYFE - Epilogue variant	FEAT_MOPS
0	10	0001	CPYFPWT, CPYFMWT, CPYFEWT - Epilogue variant	FEAT_MOPS
0	10	0010	CPYFPRT, CPYFMRT, CPYFERT - Epilogue variant	FEAT_MOPS
0	10	0011	CPYFPT, CPYFMT, CPYFET - Epilogue variant	FEAT_MOPS
0	10	0100	CPYFPWN, CPYFMWN, CPYFEWN - Epilogue variant	FEAT_MOPS
0	10	0101	CPYFPWTWN, CPYFMWTWN, CPYFEWTWN - Epilogue variant	FEAT_MOPS
0	10	0110	CPYFPRTWN, CPYFMRTWN, CPYFERTWN - Epilogue variant	FEAT_MOPS
0	10	0111	CPYFPTWN, CPYFMTWN, CPYFETWN - Epilogue variant	FEAT_MOPS
0	10	1000	CPYFPRN, CPYFMRN, CPYFERN - Epilogue variant	FEAT_MOPS
0	10	1001	CPYFPWTRN, CPYFMWTRN, CPYFEWTRN - Epilogue variant	FEAT_MOPS
0	10	1010	CPYFPRTRN, CPYFMRTRN, CPYFERTRN - Epilogue variant	FEAT_MOPS

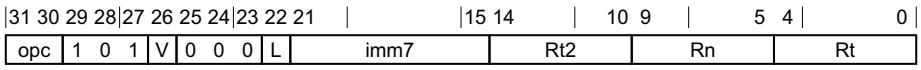
Decode fields			Instruction page	Feature
o0	op1	op2		
0	10	1011	CPYFPTRN, CPYFMTRN, CPYFETRN - Epilogue variant	FEAT_MOPS
0	10	1100	CPYFPN, CPYFMN, CPYFEN - Epilogue variant	FEAT_MOPS
0	10	1101	CPYFPWTN, CPYFMWTN, CPYFEWTN - Epilogue variant	FEAT_MOPS
0	10	1110	CPYFPRTN, CPYFMRTN, CPYFERTN - Epilogue variant	FEAT_MOPS
0	10	1111	CPYFPTN, CPYFMTN, CPYFETN - Epilogue variant	FEAT_MOPS
0	11	0000	SETP, SETM, SETE - Prologue variant	FEAT_MOPS
0	11	0001	SETPT, SETMT, SETET - Prologue variant	FEAT_MOPS
0	11	0010	SETPN, SETMN, SETEN - Prologue variant	FEAT_MOPS
0	11	0011	SETPTN, SETMTN, SETETN - Prologue variant	FEAT_MOPS
0	11	0100	SETP, SETM, SETE - Main variant	FEAT_MOPS
0	11	0101	SETPT, SETMT, SETET - Main variant	FEAT_MOPS
0	11	0110	SETPN, SETMN, SETEN - Main variant	FEAT_MOPS
0	11	0111	SETPTN, SETMTN, SETETN - Main variant	FEAT_MOPS
0	11	1000	SETP, SETM, SETE - Epilogue variant	FEAT_MOPS
0	11	1001	SETPT, SETMT, SETET - Epilogue variant	FEAT_MOPS
0	11	1010	SETPN, SETMN, SETEN - Epilogue variant	FEAT_MOPS
0	11	1011	SETPTN, SETMTN, SETETN - Epilogue variant	FEAT_MOPS
0	11	11xx	Unallocated.	-
1	00	0000	CPYP, CPYM, CPYE - Prologue variant	FEAT_MOPS
1	00	0001	CPYPWT, CPYMWT, CPYEWT - Prologue variant	FEAT_MOPS
1	00	0010	CPYPRT, CPYMRT, CPYERT - Prologue variant	FEAT_MOPS
1	00	0011	CPYPT, CPYMT, CPYET - Prologue variant	FEAT_MOPS
1	00	0100	CPYPWN, CPYMWN, CPYEWN - Prologue variant	FEAT_MOPS
1	00	0101	CPYPWTWN, CPYMWTWN, CPYEWTWN - Prologue variant	FEAT_MOPS
1	00	0110	CPYPRTWN, CPYMRTWN, CPYERTWN - Prologue variant	FEAT_MOPS
1	00	0111	CPYPTWN, CPYMTWN, CPYETWN - Prologue variant	FEAT_MOPS
1	00	1000	CPYPRN, CPYMRN, CPYERN - Prologue variant	FEAT_MOPS
1	00	1001	CPYPWTRN, CPYMWTRN, CPYEWTRN - Prologue variant	FEAT_MOPS
1	00	1010	CPYPRTRN, CPYMRTRN, CPYERTRN - Prologue variant	FEAT_MOPS
1	00	1011	CPYPTRN, CPYMTRN, CPYETRN - Prologue variant	FEAT_MOPS
1	00	1100	CPYPN, CPYMN, CPYEN - Prologue variant	FEAT_MOPS
1	00	1101	CPYPWTN, CPYMWTN, CPYEWTN - Prologue variant	FEAT_MOPS

Decode fields			Instruction page	Feature
o0	op1	op2		
1	00	1110	CPYPRTN, CPYMRTN, CPYERTN - Prologue variant	FEAT_MOPS
1	00	1111	CPYPTN, CPYMTN, CPYETN - Prologue variant	FEAT_MOPS
1	01	0000	CPYP, CPYM, CPYE - Main variant	FEAT_MOPS
1	01	0001	CPYPWT, CPYMWT, CPYEWT - Main variant	FEAT_MOPS
1	01	0010	CPYPRT, CPYMRT, CPYERT - Main variant	FEAT_MOPS
1	01	0011	CPYPT, CPYMT, CPYET - Main variant	FEAT_MOPS
1	01	0100	CPYPWN, CPYMWN, CPYEWN - Main variant	FEAT_MOPS
1	01	0101	CPYPWTWN, CPYMWTWN, CPYEWTWN - Main variant	FEAT_MOPS
1	01	0110	CPYPRTWN, CPYMRTWN, CPYERTWN - Main variant	FEAT_MOPS
1	01	0111	CPYPTWN, CPYMTWN, CPYETWN - Main variant	FEAT_MOPS
1	01	1000	CPYPRN, CPYMRN, CPYERN - Main variant	FEAT_MOPS
1	01	1001	CPYPWTRN, CPYMWTRN, CPYEWTRN - Main variant	FEAT_MOPS
1	01	1010	CPYPRTRN, CPYMRTRN, CPYERTRN - Main variant	FEAT_MOPS
1	01	1011	CPYPTRN, CPYMTRN, CPYETRN - Main variant	FEAT_MOPS
1	01	1100	CPYPN, CPYMN, CPYEN - Main variant	FEAT_MOPS
1	01	1101	CPYPWTN, CPYMWTN, CPYEWTN - Main variant	FEAT_MOPS
1	01	1110	CPYPRTN, CPYMRTN, CPYERTN - Main variant	FEAT_MOPS
1	01	1111	CPYPTN, CPYMTN, CPYETN - Main variant	FEAT_MOPS
1	10	0000	CPYP, CPYM, CPYE - Epilogue variant	FEAT_MOPS
1	10	0001	CPYPWT, CPYMWT, CPYEWT - Epilogue variant	FEAT_MOPS
1	10	0010	CPYPRT, CPYMRT, CPYERT - Epilogue variant	FEAT_MOPS
1	10	0011	CPYPT, CPYMT, CPYET - Epilogue variant	FEAT_MOPS
1	10	0100	CPYPWN, CPYMWN, CPYEWN - Epilogue variant	FEAT_MOPS
1	10	0101	CPYPWTWN, CPYMWTWN, CPYEWTWN - Epilogue variant	FEAT_MOPS
1	10	0110	CPYPRTWN, CPYMRTWN, CPYERTWN - Epilogue variant	FEAT_MOPS
1	10	0111	CPYPTWN, CPYMTWN, CPYETWN - Epilogue variant	FEAT_MOPS
1	10	1000	CPYPRN, CPYMRN, CPYERN - Epilogue variant	FEAT_MOPS
1	10	1001	CPYPWTRN, CPYMWTRN, CPYEWTRN - Epilogue variant	FEAT_MOPS
1	10	1010	CPYPRTRN, CPYMRTRN, CPYERTRN - Epilogue variant	FEAT_MOPS
1	10	1011	CPYPTRN, CPYMTRN, CPYETRN - Epilogue variant	FEAT_MOPS
1	10	1100	CPYPN, CPYMN, CPYEN - Epilogue variant	FEAT_MOPS
1	10	1101	CPYPWTN, CPYMWTN, CPYEWTN - Epilogue variant	FEAT_MOPS

Decode fields			Instruction page	Feature
o0	op1	op2		
1	10	1110	CPYPRTN, CPYMRTN, CPYERTN - Epilogue variant	FEAT_MOPS
1	10	1111	CPYPTN, CPYMTN, CPYETN - Epilogue variant	FEAT_MOPS
1	11	0000	SETGP, SETGM, SETGE - Prologue variant	FEAT_MOPS
1	11	0001	SETGPT, SETGMT, SETGET - Prologue variant	FEAT_MOPS
1	11	0010	SETGPN, SETGMN, SETGEN - Prologue variant	FEAT_MOPS
1	11	0011	SETGPTN, SETGMTN, SETGETN - Prologue variant	FEAT_MOPS
1	11	0100	SETGP, SETGM, SETGE - Main variant	FEAT_MOPS
1	11	0101	SETGPT, SETGMT, SETGET - Main variant	FEAT_MOPS
1	11	0110	SETGPN, SETGMN, SETGEN - Main variant	FEAT_MOPS
1	11	0111	SETGPTN, SETGMTN, SETGETN - Main variant	FEAT_MOPS
1	11	1000	SETGP, SETGM, SETGE - Epilogue variant	FEAT_MOPS
1	11	1001	SETGPT, SETGMT, SETGET - Epilogue variant	FEAT_MOPS
1	11	1010	SETGPN, SETGMN, SETGEN - Epilogue variant	FEAT_MOPS
1	11	1011	SETGPTN, SETGMTN, SETGETN - Epilogue variant	FEAT_MOPS
1	11	11xx	Unallocated.	-

Load/store no-allocate pair (offset)

This section describes the encoding of the Load/store no-allocate pair (offset) instruction class. The encodings in this section are decoded from *Loads and Stores* on page C4-537.

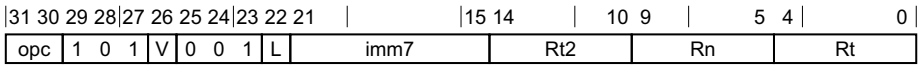


Decode fields			Instruction page
opc	V	L	
00	0	0	STNP - 32-bit variant
00	0	1	LDNP - 32-bit variant
00	1	0	STNP (SIMD&FP) - 32-bit variant
00	1	1	LDNP (SIMD&FP) - 32-bit variant
01	0	-	Unallocated.
01	1	0	STNP (SIMD&FP) - 64-bit variant
01	1	1	LDNP (SIMD&FP) - 64-bit variant
10	0	0	STNP - 64-bit variant

Decode fields			Instruction page
opc	V	L	
10	0	1	LDNP - 64-bit variant
10	1	0	STNP (SIMD&FP) - 128-bit variant
10	1	1	LDNP (SIMD&FP) - 128-bit variant
11	-	-	Unallocated.

Load/store register pair (post-indexed)

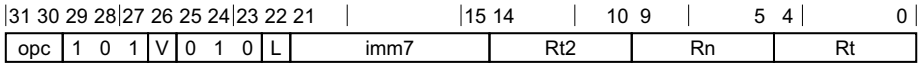
This section describes the encoding of the Load/store register pair (post-indexed) instruction class. The encodings in this section are decoded from *Loads and Stores* on page C4-537.



Decode fields			Instruction page	Feature
opc	V	L		
00	0	0	STP - 32-bit variant	-
00	0	1	LDP - 32-bit variant	-
00	1	0	STP (SIMD&FP) - 32-bit variant	-
00	1	1	LDP (SIMD&FP) - 32-bit variant	-
01	0	0	STGP	FEAT_MTE
01	0	1	LDPSW	-
01	1	0	STP (SIMD&FP) - 64-bit variant	-
01	1	1	LDP (SIMD&FP) - 64-bit variant	-
10	0	0	STP - 64-bit variant	-
10	0	1	LDP - 64-bit variant	-
10	1	0	STP (SIMD&FP) - 128-bit variant	-
10	1	1	LDP (SIMD&FP) - 128-bit variant	-
11	-	-	Unallocated.	-

Load/store register pair (offset)

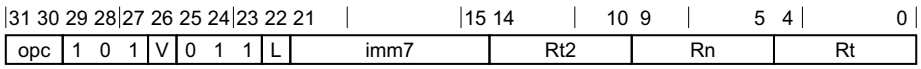
This section describes the encoding of the Load/store register pair (offset) instruction class. The encodings in this section are decoded from *Loads and Stores* on page C4-537.



Decode fields			Instruction page	Feature
opc	V	L		
00	0	0	STP - 32-bit variant	-
00	0	1	LDP - 32-bit variant	-
00	1	0	STP (SIMD&FP) - 32-bit variant	-
00	1	1	LDP (SIMD&FP) - 32-bit variant	-
01	0	0	STGP	FEAT_MTE
01	0	1	LDPSW	-
01	1	0	STP (SIMD&FP) - 64-bit variant	-
01	1	1	LDP (SIMD&FP) - 64-bit variant	-
10	0	0	STP - 64-bit variant	-
10	0	1	LDP - 64-bit variant	-
10	1	0	STP (SIMD&FP) - 128-bit variant	-
10	1	1	LDP (SIMD&FP) - 128-bit variant	-
11	-	-	Unallocated.	-

Load/store register pair (pre-indexed)

This section describes the encoding of the Load/store register pair (pre-indexed) instruction class. The encodings in this section are decoded from *Loads and Stores* on page C4-537.

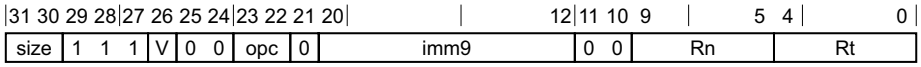


Decode fields			Instruction page	Feature
opc	V	L		
00	0	0	STP - 32-bit variant	-
00	0	1	LDP - 32-bit variant	-
00	1	0	STP (SIMD&FP) - 32-bit variant	-
00	1	1	LDP (SIMD&FP) - 32-bit variant	-
01	0	0	STGP	FEAT_MTE
01	0	1	LDPSW	-

Decode fields			Instruction page	Feature
opc	V	L		
01	1	0	STP (SIMD&FP) - 64-bit variant	-
01	1	1	LDP (SIMD&FP) - 64-bit variant	-
10	0	0	STP - 64-bit variant	-
10	0	1	LDP - 64-bit variant	-
10	1	0	STP (SIMD&FP) - 128-bit variant	-
10	1	1	LDP (SIMD&FP) - 128-bit variant	-
11	-	-	Unallocated.	-

Load/store register (unscaled immediate)

This section describes the encoding of the Load/store register (unscaled immediate) instruction class. The encodings in this section are decoded from *Loads and Stores* on page C4-537.

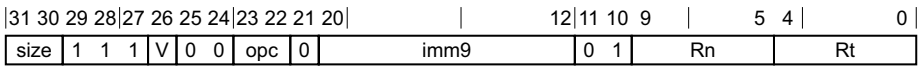


Decode fields			Instruction page
size	V	opc	
x1	1	1x	Unallocated.
00	0	00	STURB
00	0	01	LDURB
00	0	10	LDURSB - 64-bit variant
00	0	11	LDURSB - 32-bit variant
00	1	00	STUR (SIMD&FP) - 8-bit variant
00	1	01	LDUR (SIMD&FP) - 8-bit variant
00	1	10	STUR (SIMD&FP) - 128-bit variant
00	1	11	LDUR (SIMD&FP) - 128-bit variant
01	0	00	STURH
01	0	01	LDURH
01	0	10	LDURSH - 64-bit variant
01	0	11	LDURSH - 32-bit variant
01	1	00	STUR (SIMD&FP) - 16-bit variant
01	1	01	LDUR (SIMD&FP) - 16-bit variant
1x	0	11	Unallocated.

Decode fields			Instruction page
size	V	opc	
1x	1	1x	Unallocated.
10	0	00	STUR - 32-bit variant
10	0	01	LDUR - 32-bit variant
10	0	10	LDURSW
10	1	00	STUR (SIMD&FP) - 32-bit variant
10	1	01	LDUR (SIMD&FP) - 32-bit variant
11	0	00	STUR - 64-bit variant
11	0	01	LDUR - 64-bit variant
11	0	10	PRFUM
11	1	00	STUR (SIMD&FP) - 64-bit variant
11	1	01	LDUR (SIMD&FP) - 64-bit variant

Load/store register (immediate post-indexed)

This section describes the encoding of the Load/store register (immediate post-indexed) instruction class. The encodings in this section are decoded from *Loads and Stores* on page C4-537.

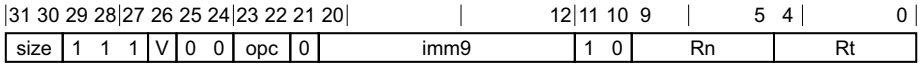


Decode fields			Instruction page
size	V	opc	
x1	1	1x	Unallocated.
00	0	00	STRB (immediate)
00	0	01	LDRB (immediate)
00	0	10	LDRSB (immediate) - 64-bit variant
00	0	11	LDRSB (immediate) - 32-bit variant
00	1	00	STR (immediate, SIMD&FP) - 8-bit variant
00	1	01	LDR (immediate, SIMD&FP) - 8-bit variant
00	1	10	STR (immediate, SIMD&FP) - 128-bit variant
00	1	11	LDR (immediate, SIMD&FP) - 128-bit variant
01	0	00	STRH (immediate)
01	0	01	LDRH (immediate)
01	0	10	LDRSH (immediate) - 64-bit variant

Decode fields			Instruction page
size	V	opc	
01	0	11	LDRSH (immediate) - 32-bit variant
01	1	00	STR (immediate, SIMD&FP) - 16-bit variant
01	1	01	LDR (immediate, SIMD&FP) - 16-bit variant
1x	0	11	Unallocated.
1x	1	1x	Unallocated.
10	0	00	STR (immediate) - 32-bit variant
10	0	01	LDR (immediate) - 32-bit variant
10	0	10	LDRSW (immediate)
10	1	00	STR (immediate, SIMD&FP) - 32-bit variant
10	1	01	LDR (immediate, SIMD&FP) - 32-bit variant
11	0	00	STR (immediate) - 64-bit variant
11	0	01	LDR (immediate) - 64-bit variant
11	0	10	Unallocated.
11	1	00	STR (immediate, SIMD&FP) - 64-bit variant
11	1	01	LDR (immediate, SIMD&FP) - 64-bit variant

Load/store register (unprivileged)

This section describes the encoding of the Load/store register (unprivileged) instruction class. The encodings in this section are decoded from *Loads and Stores* on page C4-537.

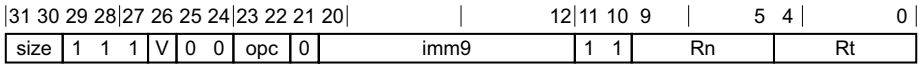


Decode fields			Instruction page
size	V	opc	
-	1	-	Unallocated.
00	0	00	STTRB
00	0	01	LDTRB
00	0	10	LDTRSB - 64-bit variant
00	0	11	LDTRSB - 32-bit variant
01	0	00	STTRH
01	0	01	LDTRH
01	0	10	LDTRSH - 64-bit variant

Decode fields			Instruction page
size	V	opc	
01	0	11	LDTRSH - 32-bit variant
1x	0	11	Unallocated.
10	0	00	STTR - 32-bit variant
10	0	01	LDTR - 32-bit variant
10	0	10	LDRSW
11	0	00	STTR - 64-bit variant
11	0	01	LDTR - 64-bit variant
11	0	10	Unallocated.

Load/store register (immediate pre-indexed)

This section describes the encoding of the Load/store register (immediate pre-indexed) instruction class. The encodings in this section are decoded from *Loads and Stores* on page C4-537.

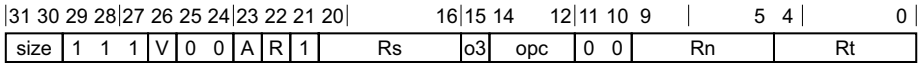


Decode fields			Instruction page
size	V	opc	
x1	1	1x	Unallocated.
00	0	00	STRB (immediate)
00	0	01	LDRB (immediate)
00	0	10	LDRSB (immediate) - 64-bit variant
00	0	11	LDRSB (immediate) - 32-bit variant
00	1	00	STR (immediate, SIMD&FP) - 8-bit variant
00	1	01	LDR (immediate, SIMD&FP) - 8-bit variant
00	1	10	STR (immediate, SIMD&FP) - 128-bit variant
00	1	11	LDR (immediate, SIMD&FP) - 128-bit variant
01	0	00	STRH (immediate)
01	0	01	LDRH (immediate)
01	0	10	LDRSH (immediate) - 64-bit variant
01	0	11	LDRSH (immediate) - 32-bit variant
01	1	00	STR (immediate, SIMD&FP) - 16-bit variant
01	1	01	LDR (immediate, SIMD&FP) - 16-bit variant

Decode fields			Instruction page
size	V	opc	
1x	0	11	Unallocated.
1x	1	1x	Unallocated.
10	0	00	STR (immediate) - 32-bit variant
10	0	01	LDR (immediate) - 32-bit variant
10	0	10	LDRSW (immediate)
10	1	00	STR (immediate, SIMD&FP) - 32-bit variant
10	1	01	LDR (immediate, SIMD&FP) - 32-bit variant
11	0	00	STR (immediate) - 64-bit variant
11	0	01	LDR (immediate) - 64-bit variant
11	0	10	Unallocated.
11	1	00	STR (immediate, SIMD&FP) - 64-bit variant
11	1	01	LDR (immediate, SIMD&FP) - 64-bit variant

Atomic memory operations

This section describes the encoding of the Atomic memory operations instruction class. The encodings in this section are decoded from *Loads and Stores* on page C4-537.



Decode fields							Instruction page	Feature
size	V	A	R	Rs	o3	opc		
-	0	-	-	-	1	11x	Unallocated.	-
-	0	0	-	-	1	100	Unallocated.	-
-	0	0	1	-	1	001	Unallocated.	-
-	0	0	1	-	1	010	Unallocated.	-
-	0	0	1	-	1	011	Unallocated.	-
-	0	0	1	-	1	101	Unallocated.	-
-	0	1	0	-	1	001	Unallocated.	-

Decode fields							Instruction page	Feature
size	V	A	R	Rs	o3	opc		
-	0	1	0	-	1	010	Unallocated.	-
-	0	1	0	-	1	011	Unallocated.	-
-	0	1	0	-	1	101	Unallocated.	-
-	0	1	1	-	1	001	Unallocated.	-
-	0	1	1	-	1	010	Unallocated.	-
-	0	1	1	-	1	011	Unallocated.	-
-	0	1	1	-	1	100	Unallocated.	-
-	0	1	1	-	1	101	Unallocated.	-
-	1	-	-	-	-	-	Unallocated.	-
00	0	0	0	-	0	000	LDADDB, LDADDAB, LDADDALB, LDADDLB - LDADDB variant	FEAT_LSE
00	0	0	0	-	0	001	LDCLRB, LDCLRAB, LDCLRALB, LDCLRLB - LDCLRB variant	FEAT_LSE
00	0	0	0	-	0	010	LDEORB, LDEORAB, LDEORALB, LDEORLB - LDEORB variant	FEAT_LSE
00	0	0	0	-	0	011	LDSETB, LDSETAB, LDSETALB, LDSETLB - LDSETB variant	FEAT_LSE
00	0	0	0	-	0	100	LDSMAXB, LDSMAXAB, LDSMAXALB, LDSMAXLB - LDSMAXB variant	FEAT_LSE
00	0	0	0	-	0	101	LDSMINB, LDSMINAB, LDSMINALB, LDSMINLB - LDSMINB variant	FEAT_LSE
00	0	0	0	-	0	110	LDUMAXB, LDUMAXAB, LDUMAXALB, LDUMAXLB - LDUMAXB variant	FEAT_LSE
00	0	0	0	-	0	111	LDUMINB, LDUMINAB, LDUMINALB, LDUMINLB - LDUMINB variant	FEAT_LSE
00	0	0	0	-	1	000	SWPB, SWPAB, SWPALB, SWPLB - SWPB variant	FEAT_LSE
00	0	0	0	-	1	001	Unallocated.	-
00	0	0	0	-	1	010	Unallocated.	-

Decode fields							Instruction page	Feature
size	V	A	R	Rs	o3	opc		
00	0	0	0	-	1	011	Unallocated.	-
00	0	0	0	-	1	101	Unallocated.	-
00	0	0	1	-	0	000	LDADDB, LDADDAB, LDADDALB, LDADDLB - LDADDLB variant	FEAT_LSE
00	0	0	1	-	0	001	LDCLRB, LDCLRAB, LDCLRALB, LDCLRLB - LDCLRLB variant	FEAT_LSE
00	0	0	1	-	0	010	LDEORB, LDEORAB, LDEORALB, LDEORLB - LDEORLB variant	FEAT_LSE
00	0	0	1	-	0	011	LDSETB, LDSETAB, LDSETALB, LDSETLB - LDSETLB variant	FEAT_LSE
00	0	0	1	-	0	100	LDSMAXB, LDSMAXAB, LDSMAXALB, LDSMAXLB - LDSMAXLB variant	FEAT_LSE
00	0	0	1	-	0	101	LDSMINB, LDSMINAB, LDSMINALB, LDSMINLB - LDSMINLB variant	FEAT_LSE
00	0	0	1	-	0	110	LDUMAXB, LDUMAXAB, LDUMAXALB, LDUMAXLB - LDUMAXLB variant	FEAT_LSE
00	0	0	1	-	0	111	LDUMINB, LDUMINAB, LDUMINALB, LDUMINLB - LDUMINLB variant	FEAT_LSE
00	0	0	1	-	1	000	SWPB, SWPAB, SWPALB, SWPLB - SWPLB variant	FEAT_LSE
00	0	1	0	-	0	000	LDADDB, LDADDAB, LDADDALB, LDADDLB - LDADDAB variant	FEAT_LSE
00	0	1	0	-	0	001	LDCLRB, LDCLRAB, LDCLRALB, LDCLRLB - LDCLRAB variant	FEAT_LSE
00	0	1	0	-	0	010	LDEORB, LDEORAB, LDEORALB, LDEORLB - LDEORAB variant	FEAT_LSE
00	0	1	0	-	0	011	LDSETB, LDSETAB, LDSETALB, LDSETLB - LDSETAB variant	FEAT_LSE
00	0	1	0	-	0	100	LDSMAXB, LDSMAXAB, LDSMAXALB, LDSMAXLB - LDSMAXAB variant	FEAT_LSE
00	0	1	0	-	0	101	LDSMINB, LDSMINAB, LDSMINALB, LDSMINLB - LDSMINAB variant	FEAT_LSE
00	0	1	0	-	0	110	LDUMAXB, LDUMAXAB, LDUMAXALB, LDUMAXLB - LDUMAXAB variant	FEAT_LSE
00	0	1	0	-	0	111	LDUMINB, LDUMINAB, LDUMINALB, LDUMINLB - LDUMINAB variant	FEAT_LSE
00	0	1	0	-	1	000	SWPB, SWPAB, SWPALB, SWPLB - SWPAB variant	FEAT_LSE

Decode fields							Instruction page	Feature
size	V	A	R	Rs	o3	opc		
00	0	1	0	-	1	100	LDAPRB	FEAT_LRCPC
00	0	1	1	-	0	000	LDADDB, LDADDAB, LDADDALB, LDADDLB - LDADDALB variant	FEAT_LSE
00	0	1	1	-	0	001	LDCLRB, LDCLRAB, LDCLRALB, LDCLRLB - LDCLRALB variant	FEAT_LSE
00	0	1	1	-	0	010	LDEORB, LDEORAB, LDEORALB, LDEORLB - LDEORALB variant	FEAT_LSE
00	0	1	1	-	0	011	LDSETB, LDSETAB, LDSETALB, LDSETLB - LDSETALB variant	FEAT_LSE
00	0	1	1	-	0	100	LDSMAXB, LDSMAXAB, LDSMAXALB, LDSMAXLB - LDSMAXALB variant	FEAT_LSE
00	0	1	1	-	0	101	LDSMINB, LDSMINAB, LDSMINALB, LDSMINLB - LDSMINALB variant	FEAT_LSE
00	0	1	1	-	0	110	LDUMAXB, LDUMAXAB, LDUMAXALB, LDUMAXLB - LDUMAXALB variant	FEAT_LSE
00	0	1	1	-	0	111	LDUMINB, LDUMINAB, LDUMINALB, LDUMINLB - LDUMINALB variant	FEAT_LSE
00	0	1	1	-	1	000	SWPB, SWPAB, SWPALB, SWPLB - SWPALB variant	FEAT_LSE
01	0	0	0	-	0	000	LDADDH, LDADDAH, LDADDALH, LDADDLH - LDADDH variant	FEAT_LSE
01	0	0	0	-	0	001	LDCLRH, LDCLRAH, LDCLRALH, LDCLRLH - LDCLRH variant	FEAT_LSE
01	0	0	0	-	0	010	LDEORH, LDEORAH, LDEORALH, LDEORLH - LDEORH variant	FEAT_LSE
01	0	0	0	-	0	011	LDSETH, LDSETAH, LDSETALH, LDSETLH - LDSETH variant	FEAT_LSE
01	0	0	0	-	0	100	LDSMAXH, LDSMAXAH, LDSMAXALH, LDSMAXLH - LDSMAXH variant	FEAT_LSE
01	0	0	0	-	0	101	LDSMINH, LDSMINAH, LDSMINALH, LDSMINLH - LDSMINH variant	FEAT_LSE
01	0	0	0	-	0	110	LDUMAXH, LDUMAXAH, LDUMAXALH, LDUMAXLH - LDUMAXH variant	FEAT_LSE
01	0	0	0	-	0	111	LDUMINH, LDUMINAH, LDUMINALH, LDUMINLH - LDUMINH variant	FEAT_LSE
01	0	0	0	-	1	000	SWPH, SWPAH, SWPALH, SWPLH - SWPH variant	FEAT_LSE
01	0	0	0	-	1	001	Unallocated.	-

Decode fields							Instruction page	Feature
size	V	A	R	Rs	o3	opc		
01	0	0	0	-	1	010	Unallocated.	-
01	0	0	0	-	1	011	Unallocated.	-
01	0	0	0	-	1	101	Unallocated.	-
01	0	0	1	-	0	000	LDADDH, LDADDAH, LDADDALH, LDADDLH - LDADDLH variant	FEAT_LSE
01	0	0	1	-	0	001	LDCLRH, LDCLRAH, LDCLRALH, LDCLRLH - LDCLRLH variant	FEAT_LSE
01	0	0	1	-	0	010	LDEORH, LDEORAH, LDEORALH, LDEORLH - LDEORLH variant	FEAT_LSE
01	0	0	1	-	0	011	LDSETH, LDSETAH, LDSETALH, LDSETLH - LDSETLH variant	FEAT_LSE
01	0	0	1	-	0	100	LDSMAXH, LDSMAXAH, LDSMAXALH, LDSMAXLH - LDSMAXLH variant	FEAT_LSE
01	0	0	1	-	0	101	LDSMINH, LDSMINAH, LDSMINALH, LDSMINLH - LDSMINLH variant	FEAT_LSE
01	0	0	1	-	0	110	LDUMAXH, LDUMAXAH, LDUMAXALH, LDUMAXLH - LDUMAXLH variant	FEAT_LSE
01	0	0	1	-	0	111	LDUMINH, LDUMINAH, LDUMINALH, LDUMINLH - LDUMINLH variant	FEAT_LSE
01	0	0	1	-	1	000	SWPH, SWPAH, SWPALH, SWPLH - SWPLH variant	FEAT_LSE
01	0	1	0	-	0	000	LDADDH, LDADDAH, LDADDALH, LDADDLH - LDADDAH variant	FEAT_LSE
01	0	1	0	-	0	001	LDCLRH, LDCLRAH, LDCLRALH, LDCLRLH - LDCLRAH variant	FEAT_LSE
01	0	1	0	-	0	010	LDEORH, LDEORAH, LDEORALH, LDEORLH - LDEORAH variant	FEAT_LSE
01	0	1	0	-	0	011	LDSETH, LDSETAH, LDSETALH, LDSETLH - LDSETAH variant	FEAT_LSE
01	0	1	0	-	0	100	LDSMAXH, LDSMAXAH, LDSMAXALH, LDSMAXLH - LDSMAXAH variant	FEAT_LSE
01	0	1	0	-	0	101	LDSMINH, LDSMINAH, LDSMINALH, LDSMINLH - LDSMINAH variant	FEAT_LSE
01	0	1	0	-	0	110	LDUMAXH, LDUMAXAH, LDUMAXALH, LDUMAXLH - LDUMAXAH variant	FEAT_LSE
01	0	1	0	-	0	111	LDUMINH, LDUMINAH, LDUMINALH, LDUMINLH - LDUMINAH variant	FEAT_LSE

Decode fields							Instruction page	Feature
size	V	A	R	Rs	o3	opc		
01	0	1	0	-	1	000	SWPH, SWPAH, SWPALH, SWPLH - SWPAH variant	FEAT_LSE
01	0	1	0	-	1	100	LDAPRH	FEAT_LRCPC
01	0	1	1	-	0	000	LDADDH, LDADDAH, LDADDALH, LDADDLH - LDADDALH variant	FEAT_LSE
01	0	1	1	-	0	001	LDCLRH, LDCLRAH, LDCLRALH, LDCLRLH - LDCLRALH variant	FEAT_LSE
01	0	1	1	-	0	010	LDEORH, LDEORAH, LDEORALH, LDEORLH - LDEORALH variant	FEAT_LSE
01	0	1	1	-	0	011	LDSETH, LDSETAH, LDSETALH, LDSETLH - LDSETALH variant	FEAT_LSE
01	0	1	1	-	0	100	LDSMAXH, LDSMAXAH, LDSMAXALH, LDSMAXLH - LDSMAXALH variant	FEAT_LSE
01	0	1	1	-	0	101	LDSMINH, LDSMINAH, LDSMINALH, LDSMINLH - LDSMINALH variant	FEAT_LSE
01	0	1	1	-	0	110	LDUMAXH, LDUMAXAH, LDUMAXALH, LDUMAXLH - LDUMAXALH variant	FEAT_LSE
01	0	1	1	-	0	111	LDUMINH, LDUMINAH, LDUMINALH, LDUMINLH - LDUMINALH variant	FEAT_LSE
01	0	1	1	-	1	000	SWPH, SWPAH, SWPALH, SWPLH - SWPALH variant	FEAT_LSE
10	0	0	0	-	0	000	LDADD, LDADDA, LDADDAL, LDADDL - 32-bit LDADD variant	FEAT_LSE
10	0	0	0	-	0	001	LDCLR, LDCLRA, LDCLRAL, LDCLRL - 32-bit LDCLR variant	FEAT_LSE
10	0	0	0	-	0	010	LDEOR, LDEORA, LDEORAL, LDEORL - 32-bit LDEOR variant	FEAT_LSE
10	0	0	0	-	0	011	LDSET, LDSETA, LDSETAL, LDSETL - 32-bit LDSET variant	FEAT_LSE
10	0	0	0	-	0	100	LDSMAX, LDSMAXA, LDSMAXAL, LDSMAXL - 32-bit LDSMAX variant	FEAT_LSE
10	0	0	0	-	0	101	LDSMIN, LDSMINA, LDSMINAL, LDSMINL - 32-bit LDSMIN variant	FEAT_LSE
10	0	0	0	-	0	110	LDUMAX, LDUMAXA, LDUMAXAL, LDUMAXL - 32-bit LDUMAX variant	FEAT_LSE
10	0	0	0	-	0	111	LDUMIN, LDUMINA, LDUMINAL, LDUMINL - 32-bit LDUMIN variant	FEAT_LSE
10	0	0	0	-	1	000	SWP, SWPA, SWPAL, SWPL - 32-bit SWP variant	FEAT_LSE

Decode fields							Instruction page	Feature
size	V	A	R	Rs	o3	opc		
10	0	0	0	-	1	001	Unallocated.	-
10	0	0	0	-	1	010	Unallocated.	-
10	0	0	0	-	1	011	Unallocated.	-
10	0	0	0	-	1	101	Unallocated.	-
10	0	0	1	-	0	000	LDADD, LDADDA, LDADDAL, LDADDL - 32-bit LDADDL variant	FEAT_LSE
10	0	0	1	-	0	001	LDCLR, LDCLRA, LDCLRAL, LDCLRL - 32-bit LDCLRL variant	FEAT_LSE
10	0	0	1	-	0	010	LDEOR, LDEORA, LDEORAL, LDEORL - 32-bit LDEORL variant	FEAT_LSE
10	0	0	1	-	0	011	LDSET, LDSETA, LDSETAL, LDSETL - 32-bit LDSETL variant	FEAT_LSE
10	0	0	1	-	0	100	LDSMAX, LDSMAXA, LDSMAXAL, LDSMAXL - 32-bit LDSMAXL variant	FEAT_LSE
10	0	0	1	-	0	101	LDSMIN, LDSMINA, LDSMINAL, LDSMINL - 32-bit LDSMINL variant	FEAT_LSE
10	0	0	1	-	0	110	LDUMAX, LDUMAXA, LDUMAXAL, LDUMAXL - 32-bit LDUMAXL variant	FEAT_LSE
10	0	0	1	-	0	111	LDUMIN, LDUMINA, LDUMINAL, LDUMINL - 32-bit LDUMINL variant	FEAT_LSE
10	0	0	1	-	1	000	SWP, SWPA, SWPAL, SWPL - 32-bit SWPL variant	FEAT_LSE
10	0	1	0	-	0	000	LDADD, LDADDA, LDADDAL, LDADDL - 32-bit LDADDA variant	FEAT_LSE
10	0	1	0	-	0	001	LDCLR, LDCLRA, LDCLRAL, LDCLRL - 32-bit LDCLRA variant	FEAT_LSE
10	0	1	0	-	0	010	LDEOR, LDEORA, LDEORAL, LDEORL - 32-bit LDEORA variant	FEAT_LSE
10	0	1	0	-	0	011	LDSET, LDSETA, LDSETAL, LDSETL - 32-bit LDSETA variant	FEAT_LSE
10	0	1	0	-	0	100	LDSMAX, LDSMAXA, LDSMAXAL, LDSMAXL - 32-bit LDSMAXA variant	FEAT_LSE
10	0	1	0	-	0	101	LDSMIN, LDSMINA, LDSMINAL, LDSMINL - 32-bit LDSMINA variant	FEAT_LSE
10	0	1	0	-	0	110	LDUMAX, LDUMAXA, LDUMAXAL, LDUMAXL - 32-bit LDUMAXA variant	FEAT_LSE

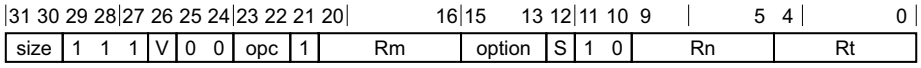
Decode fields							Instruction page	Feature
size	V	A	R	Rs	o3	opc		
10	0	1	0	-	0	111	LDUMIN, LDUMINA, LDUMINAL, LDUMINL - 32-bit LDUMINA variant	FEAT_LSE
10	0	1	0	-	1	000	SWP, SWPA, SWPAL, SWPL - 32-bit SWPA variant	FEAT_LSE
10	0	1	0	-	1	100	LDAPR - 32-bit variant	FEAT_LRCPC
10	0	1	1	-	0	000	LDADD, LDADDA, LDADDAL, LDADDL - 32-bit LDADDAL variant	FEAT_LSE
10	0	1	1	-	0	001	LDCLR, LDCLRA, LDCLRAL, LDCLRL - 32-bit LDCLRAL variant	FEAT_LSE
10	0	1	1	-	0	010	LDEOR, LDEORA, LDEORAL, LDEORL - 32-bit LDEORAL variant	FEAT_LSE
10	0	1	1	-	0	011	LDSET, LDSETA, LDSETAL, LDSETL - 32-bit LDSETAL variant	FEAT_LSE
10	0	1	1	-	0	100	LDSMAX, LDSMAXA, LDSMAXAL, LDSMAXL - 32-bit LDSMAXAL variant	FEAT_LSE
10	0	1	1	-	0	101	LDSMIN, LDSMINA, LDSMINAL, LDSMINL - 32-bit LDSMINAL variant	FEAT_LSE
10	0	1	1	-	0	110	LDUMAX, LDUMAXA, LDUMAXAL, LDUMAXL - 32-bit LDUMAXAL variant	FEAT_LSE
10	0	1	1	-	0	111	LDUMIN, LDUMINA, LDUMINAL, LDUMINL - 32-bit LDUMINAL variant	FEAT_LSE
10	0	1	1	-	1	000	SWP, SWPA, SWPAL, SWPL - 32-bit SWPAL variant	FEAT_LSE
11	0	0	0	-	0	000	LDADD, LDADDA, LDADDAL, LDADDL - 64-bit LDADD variant	FEAT_LSE
11	0	0	0	-	0	001	LDCLR, LDCLRA, LDCLRAL, LDCLRL - 64-bit LDCLR variant	FEAT_LSE
11	0	0	0	-	0	010	LDEOR, LDEORA, LDEORAL, LDEORL - 64-bit LDEOR variant	FEAT_LSE
11	0	0	0	-	0	011	LDSET, LDSETA, LDSETAL, LDSETL - 64-bit LDSET variant	FEAT_LSE
11	0	0	0	-	0	100	LDSMAX, LDSMAXA, LDSMAXAL, LDSMAXL - 64-bit LDSMAX variant	FEAT_LSE
11	0	0	0	-	0	101	LDSMIN, LDSMINA, LDSMINAL, LDSMINL - 64-bit LDSMIN variant	FEAT_LSE
11	0	0	0	-	0	110	LDUMAX, LDUMAXA, LDUMAXAL, LDUMAXL - 64-bit LDUMAX variant	FEAT_LSE
11	0	0	0	-	0	111	LDUMIN, LDUMINA, LDUMINAL, LDUMINL - 64-bit LDUMIN variant	FEAT_LSE

Decode fields							Instruction page	Feature
size	V	A	R	Rs	o3	opc		
11	0	0	0	-	1	000	SWP, SWPA, SWPAL, SWPL - 64-bit SWP variant	FEAT_LSE
11	0	0	0	-	1	010	ST64BV0	FEAT_LS64_ACCDATA
11	0	0	0	-	1	011	ST64BV	FEAT_LS64_V
11	0	0	0	11111	1	001	ST64B	FEAT_LS64
11	0	0	0	11111	1	101	LD64B	FEAT_LS64
11	0	0	1	-	0	000	LDADD, LDADDA, LDADDAL, LDADDL - 64-bit LDADDL variant	FEAT_LSE
11	0	0	1	-	0	001	LDCLR, LDCLRA, LDCLRAL, LDCLRL - 64-bit LDCLRL variant	FEAT_LSE
11	0	0	1	-	0	010	LDEOR, LDEORA, LDEORAL, LDEORL - 64-bit LDEORL variant	FEAT_LSE
11	0	0	1	-	0	011	LDSET, LDSETA, LDSETAL, LDSETL - 64-bit LDSETL variant	FEAT_LSE
11	0	0	1	-	0	100	LDSMAX, LDSMAXA, LDSMAXAL, LDSMAXL - 64-bit LDSMAXL variant	FEAT_LSE
11	0	0	1	-	0	101	LDSMIN, LDSMINA, LDSMINAL, LDSMINL - 64-bit LDSMINL variant	FEAT_LSE
11	0	0	1	-	0	110	LDUMAX, LDUMAXA, LDUMAXAL, LDUMAXL - 64-bit LDUMAXL variant	FEAT_LSE
11	0	0	1	-	0	111	LDUMIN, LDUMINA, LDUMINAL, LDUMINL - 64-bit LDUMINL variant	FEAT_LSE
11	0	0	1	-	1	000	SWP, SWPA, SWPAL, SWPL - 64-bit SWPL variant	FEAT_LSE
11	0	1	0	-	0	000	LDADD, LDADDA, LDADDAL, LDADDL - 64-bit LDADDA variant	FEAT_LSE
11	0	1	0	-	0	001	LDCLR, LDCLRA, LDCLRAL, LDCLRL - 64-bit LDCLRA variant	FEAT_LSE
11	0	1	0	-	0	010	LDEOR, LDEORA, LDEORAL, LDEORL - 64-bit LDEORA variant	FEAT_LSE
11	0	1	0	-	0	011	LDSET, LDSETA, LDSETAL, LDSETL - 64-bit LDSETA variant	FEAT_LSE
11	0	1	0	-	0	100	LDSMAX, LDSMAXA, LDSMAXAL, LDSMAXL - 64-bit LDSMAXA variant	FEAT_LSE

Decode fields							Instruction page	Feature
size	V	A	R	Rs	o3	opc		
11	0	1	0	-	0	101	LDSMIN, LDSMINA, LDSMINAL, LDSMINL - 64-bit LDSMINA variant	FEAT_LSE
11	0	1	0	-	0	110	LDUMAX, LDUMAXA, LDUMAXAL, LDUMAXL - 64-bit LDUMAXA variant	FEAT_LSE
11	0	1	0	-	0	111	LDUMIN, LDUMINA, LDUMINAL, LDUMINL - 64-bit LDUMINA variant	FEAT_LSE
11	0	1	0	-	1	000	SWP, SWPA, SWPAL, SWPL - 64-bit SWPA variant	FEAT_LSE
11	0	1	0	-	1	100	LDAPR - 64-bit variant	FEAT_LRCPC
11	0	1	1	-	0	000	LDADD, LDADDA, LDADDAL, LDADDL - 64-bit LDADDAL variant	FEAT_LSE
11	0	1	1	-	0	001	LDCLR, LDCLRA, LDCLRAL, LDCLRL - 64-bit LDCLRAL variant	FEAT_LSE
11	0	1	1	-	0	010	LDEOR, LDEORA, LDEORAL, LDEORL - 64-bit LDEORAL variant	FEAT_LSE
11	0	1	1	-	0	011	LDSET, LDSETA, LDSETAL, LDSETL - 64-bit LDSETAL variant	FEAT_LSE
11	0	1	1	-	0	100	LDSMAX, LDSMAXA, LDSMAXAL, LDSMAXL - 64-bit LDSMAXAL variant	FEAT_LSE
11	0	1	1	-	0	101	LDSMIN, LDSMINA, LDSMINAL, LDSMINL - 64-bit LDSMINAL variant	FEAT_LSE
11	0	1	1	-	0	110	LDUMAX, LDUMAXA, LDUMAXAL, LDUMAXL - 64-bit LDUMAXAL variant	FEAT_LSE
11	0	1	1	-	0	111	LDUMIN, LDUMINA, LDUMINAL, LDUMINL - 64-bit LDUMINAL variant	FEAT_LSE
11	0	1	1	-	1	000	SWP, SWPA, SWPAL, SWPL - 64-bit SWPAL variant	FEAT_LSE

Load/store register (register offset)

This section describes the encoding of the Load/store register (register offset) instruction class. The encodings in this section are decoded from *Loads and Stores* on page C4-537.

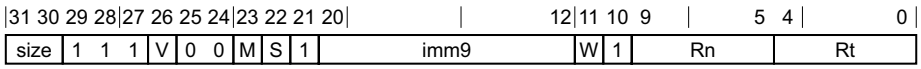


Decode fields				Instruction page
size	V	opc	option	
x1	1	1x	-	Unallocated.
00	0	00	!= 011	STRB (register) - Extended register variant
00	0	00	011	STRB (register) - Shifted register variant
00	0	01	!= 011	LDRB (register) - Extended register variant
00	0	01	011	LDRB (register) - Shifted register variant
00	0	10	!= 011	LDRSB (register) - 64-bit with extended register offset variant
00	0	10	011	LDRSB (register) - 64-bit with shifted register offset variant
00	0	11	!= 011	LDRSB (register) - 32-bit with extended register offset variant
00	0	11	011	LDRSB (register) - 32-bit with shifted register offset variant
00	1	00	!= 011	STR (register, SIMD&FP)
00	1	00	011	STR (register, SIMD&FP)
00	1	01	!= 011	LDR (register, SIMD&FP)
00	1	01	011	LDR (register, SIMD&FP)
00	1	10	-	STR (register, SIMD&FP)
00	1	11	-	LDR (register, SIMD&FP)
01	0	00	-	STRH (register)
01	0	01	-	LDRH (register)
01	0	10	-	LDRSH (register) - 64-bit variant
01	0	11	-	LDRSH (register) - 32-bit variant
01	1	00	-	STR (register, SIMD&FP)
01	1	01	-	LDR (register, SIMD&FP)
1x	0	11	-	Unallocated.
1x	1	1x	-	Unallocated.
10	0	00	-	STR (register) - 32-bit variant
10	0	01	-	LDR (register) - 32-bit variant
10	0	10	-	LDRSW (register)
10	1	00	-	STR (register, SIMD&FP)
10	1	01	-	LDR (register, SIMD&FP)

Decode fields				Instruction page
size	V	opc	option	
11	0	00	-	STR (register) - 64-bit variant
11	0	01	-	LDR (register) - 64-bit variant
11	0	10	-	PRFM (register)
11	1	00	-	STR (register, SIMD&FP)
11	1	01	-	LDR (register, SIMD&FP)

Load/store register (pac)

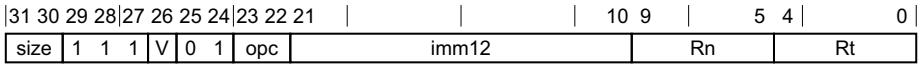
This section describes the encoding of the Load/store register (pac) instruction class. The encodings in this section are decoded from *Loads and Stores* on page C4-537.



Decode fields				Instruction page	Feature
size	V	M	W		
!= 11	-	-	-	Unallocated.	-
11	0	0	0	LDRAA, LDRAB - Key A, offset variant	FEAT_PAuth
11	0	0	1	LDRAA, LDRAB - Key A, pre-indexed variant	FEAT_PAuth
11	0	1	0	LDRAA, LDRAB - Key B, offset variant	FEAT_PAuth
11	0	1	1	LDRAA, LDRAB - Key B, pre-indexed variant	FEAT_PAuth
11	1	-	-	Unallocated.	-

Load/store register (unsigned immediate)

This section describes the encoding of the Load/store register (unsigned immediate) instruction class. The encodings in this section are decoded from *Loads and Stores* on page C4-537.



Decode fields			Instruction page
size	V	opc	
x1	1	1x	Unallocated.
00	0	00	STRB (immediate)
00	0	01	LDRB (immediate)

Decode fields			Instruction page
size	V	opc	
00	0	10	LDRSB (immediate) - 64-bit variant
00	0	11	LDRSB (immediate) - 32-bit variant
00	1	00	STR (immediate, SIMD&FP) - 8-bit variant
00	1	01	LDR (immediate, SIMD&FP) - 8-bit variant
00	1	10	STR (immediate, SIMD&FP) - 128-bit variant
00	1	11	LDR (immediate, SIMD&FP) - 128-bit variant
01	0	00	STRH (immediate)
01	0	01	LDRH (immediate)
01	0	10	LDRSH (immediate) - 64-bit variant
01	0	11	LDRSH (immediate) - 32-bit variant
01	1	00	STR (immediate, SIMD&FP) - 16-bit variant
01	1	01	LDR (immediate, SIMD&FP) - 16-bit variant
1x	0	11	Unallocated.
1x	1	1x	Unallocated.
10	0	00	STR (immediate) - 32-bit variant
10	0	01	LDR (immediate) - 32-bit variant
10	0	10	LDRSW (immediate)
10	1	00	STR (immediate, SIMD&FP) - 32-bit variant
10	1	01	LDR (immediate, SIMD&FP) - 32-bit variant
11	0	00	STR (immediate) - 64-bit variant
11	0	01	LDR (immediate) - 64-bit variant
11	0	10	PRFM (immediate)
11	1	00	STR (immediate, SIMD&FP) - 64-bit variant
11	1	01	LDR (immediate, SIMD&FP) - 64-bit variant

C4.1.67 Data Processing -- Register

This section describes the encoding of the Data Processing -- Register group. The encodings in this section are decoded from *A64 instruction set encoding* on page C4-380.

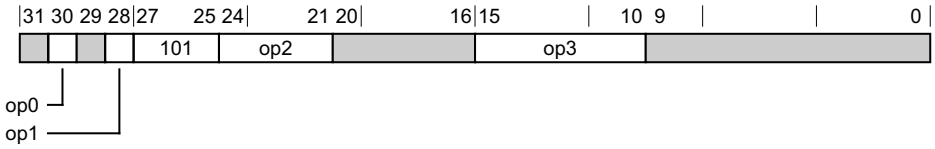
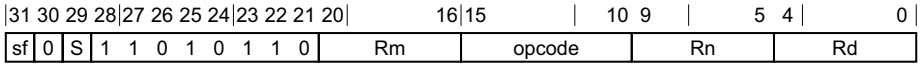


Table C4-68 Encoding table for the Data Processing -- Register group

Decode fields				Decode group or instruction page
op0	op1	op2	op3	
0	1	0110	-	*Data-processing (2 source)*
1	1	0110	-	*Data-processing (1 source)* on page C4-579
-	0	0xxx	-	*Logical (shifted register)* on page C4-580
-	0	1xx0	-	*Add/subtract (shifted register)* on page C4-581
-	0	1xx1	-	*Add/subtract (extended register)* on page C4-582
-	1	0000	000000	*Add/subtract (with carry)* on page C4-583
-	1	0000	x00001	*Rotate right into flags* on page C4-583
-	1	0000	xx0010	*Evaluate into flags* on page C4-584
-	1	0010	xxxx0x	*Conditional compare (register)* on page C4-584
-	1	0010	xxxx1x	*Conditional compare (immediate)* on page C4-585
-	1	0100	-	*Conditional select* on page C4-585
-	1	1xxx	-	*Data-processing (3 source)* on page C4-586

Data-processing (2 source)

This section describes the encoding of the Data-processing (2 source) instruction class. The encodings in this section are decoded from *Data Processing -- Register* on page C4-576.



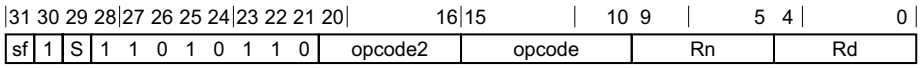
Decode fields			Instruction page	Feature
sf	S	opcode		
-	-	000001	Unallocated.	-
-	-	011xxx	Unallocated.	-
-	-	1xxxxx	Unallocated.	-
-	0	00011x	Unallocated.	-
-	0	001101	Unallocated.	-

Decode fields			Instruction page	Feature
sf	S	opcode		
-	0	00111x	Unallocated.	-
-	1	00001x	Unallocated.	-
-	1	0001xx	Unallocated.	-
-	1	001xxx	Unallocated.	-
-	1	01xxxx	Unallocated.	-
0	-	000000	Unallocated.	-
0	0	000010	UDIV - 32-bit variant	-
0	0	000011	SDIV - 32-bit variant	-
0	0	00010x	Unallocated.	-
0	0	001000	LSLV - 32-bit variant	-
0	0	001001	LSRV - 32-bit variant	-
0	0	001010	ASRV - 32-bit variant	-
0	0	001011	RORV - 32-bit variant	-
0	0	001100	Unallocated.	-
0	0	010x11	Unallocated.	-
0	0	010000	CRC32B, CRC32H, CRC32W, CRC32X - CRC32B variant	-
0	0	010001	CRC32B, CRC32H, CRC32W, CRC32X - CRC32H variant	-
0	0	010010	CRC32B, CRC32H, CRC32W, CRC32X - CRC32W variant	-
0	0	010100	CRC32CB, CRC32CH, CRC32CW, CRC32CX - CRC32CB variant	-
0	0	010101	CRC32CB, CRC32CH, CRC32CW, CRC32CX - CRC32CH variant	-
0	0	010110	CRC32CB, CRC32CH, CRC32CW, CRC32CX - CRC32CW variant	-
1	0	000000	SUBP	FEAT_MTE
1	0	000010	UDIV - 64-bit variant	-
1	0	000011	SDIV - 64-bit variant	-
1	0	000100	IRG	FEAT_MTE
1	0	000101	GMI	FEAT_MTE
1	0	001000	LSLV - 64-bit variant	-
1	0	001001	LSRV - 64-bit variant	-
1	0	001010	ASRV - 64-bit variant	-
1	0	001011	RORV - 64-bit variant	-
1	0	001100	PACGA	FEAT_PAuth
1	0	010xx0	Unallocated.	-

Decode fields			Instruction page	Feature
sf	S	opcode		
1	0	010x0x	Unallocated.	-
1	0	010011	CRC32B, CRC32H, CRC32W, CRC32X - CRC32X variant	-
1	0	010111	CRC32CB, CRC32CH, CRC32CW, CRC32CX - CRC32CX variant	-
1	1	000000	SUBPS	FEAT_MTE

Data-processing (1 source)

This section describes the encoding of the Data-processing (1 source) instruction class. The encodings in this section are decoded from *Data Processing -- Register* on page C4-576.

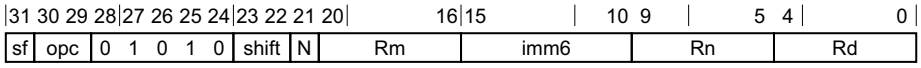


Decode fields					Instruction page	Feature
sf	S	opcode2	opcode	Rn		
-	-	-	1xxxxx	-	Unallocated.	-
-	-	xxx1x	-	-	Unallocated.	-
-	-	xx1xx	-	-	Unallocated.	-
-	-	x1xxx	-	-	Unallocated.	-
-	-	1xxxx	-	-	Unallocated.	-
-	0	00000	00011x	-	Unallocated.	-
-	0	00000	001xxx	-	Unallocated.	-
-	0	00000	01xxxx	-	Unallocated.	-
-	1	-	-	-	Unallocated.	-
0	-	00001	-	-	Unallocated.	-
0	0	00000	000000	-	RBIT - 32-bit variant	-
0	0	00000	000001	-	REV16 - 32-bit variant	-
0	0	00000	000010	-	REV - 32-bit variant	-
0	0	00000	000011	-	Unallocated.	-
0	0	00000	000100	-	CLZ - 32-bit variant	-
0	0	00000	000101	-	CLS - 32-bit variant	-
1	0	00000	000000	-	RBIT - 64-bit variant	-
1	0	00000	000001	-	REV16 - 64-bit variant	-
1	0	00000	000010	-	REV32	-

Decode fields					Instruction page	Feature
sf	S	opcode2	opcode	Rn		
1	0	00000	000011	-	REV - 64-bit variant	-
1	0	00000	000100	-	CLZ - 64-bit variant	-
1	0	00000	000101	-	CLS - 64-bit variant	-
1	0	00001	000000	-	PACIA, PACIA1716, PACIASP, PACIAZ, PACIZA - PACIA variant	FEAT_PAuth
1	0	00001	000001	-	PACIB, PACIB1716, PACIBSP, PACIBZ, PACIZB - PACIB variant	FEAT_PAuth
1	0	00001	000010	-	PACDA, PACDZA - PACDA variant	FEAT_PAuth
1	0	00001	000011	-	PACDB, PACDZB - PACDB variant	FEAT_PAuth
1	0	00001	000100	-	AUTIA, AUTIA1716, AUTIASP, AUTIAZ, AUTIZA - AUTIA variant	FEAT_PAuth
1	0	00001	000101	-	AUTIB, AUTIB1716, AUTIBSP, AUTIBZ, AUTIZB - AUTIB variant	FEAT_PAuth
1	0	00001	000110	-	AUTDA, AUTDZA - AUTDA variant	FEAT_PAuth
1	0	00001	000111	-	AUTDB, AUTDZB - AUTDB variant	FEAT_PAuth
1	0	00001	001000	11111	PACIA, PACIA1716, PACIASP, PACIAZ, PACIZA - PACIZA variant	FEAT_PAuth
1	0	00001	001001	11111	PACIB, PACIB1716, PACIBSP, PACIBZ, PACIZB - PACIZB variant	FEAT_PAuth
1	0	00001	001010	11111	PACDA, PACDZA - PACDZA variant	FEAT_PAuth
1	0	00001	001011	11111	PACDB, PACDZB - PACDZB variant	FEAT_PAuth
1	0	00001	001100	11111	AUTIA, AUTIA1716, AUTIASP, AUTIAZ, AUTIZA - AUTIZA variant	FEAT_PAuth
1	0	00001	001101	11111	AUTIB, AUTIB1716, AUTIBSP, AUTIBZ, AUTIZB - AUTIZB variant	FEAT_PAuth
1	0	00001	001110	11111	AUTDA, AUTDZA - AUTDZA variant	FEAT_PAuth
1	0	00001	001111	11111	AUTDB, AUTDZB - AUTDZB variant	FEAT_PAuth
1	0	00001	010000	11111	XPACD, XPACI, XPACLRI - XPACI variant	FEAT_PAuth
1	0	00001	010001	11111	XPACD, XPACI, XPACLRI - XPACD variant	FEAT_PAuth
1	0	00001	01001x	-	Unallocated.	-
1	0	00001	0101xx	-	Unallocated.	-
1	0	00001	011xxx	-	Unallocated.	-

Logical (shifted register)

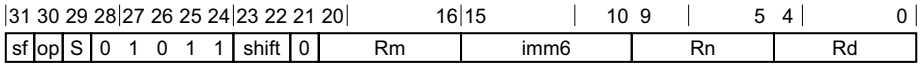
This section describes the encoding of the Logical (shifted register) instruction class. The encodings in this section are decoded from *Data Processing -- Register* on page C4-576.



Decode fields				Instruction page
sf	opc	N	imm6	
0	-	-	1xxxxx	Unallocated.
0	00	0	-	AND (shifted register) - 32-bit variant
0	00	1	-	BIC (shifted register) - 32-bit variant
0	01	0	-	ORR (shifted register) - 32-bit variant
0	01	1	-	ORN (shifted register) - 32-bit variant
0	10	0	-	EOR (shifted register) - 32-bit variant
0	10	1	-	EON (shifted register) - 32-bit variant
0	11	0	-	ANDS (shifted register) - 32-bit variant
0	11	1	-	BICS (shifted register) - 32-bit variant
1	00	0	-	AND (shifted register) - 64-bit variant
1	00	1	-	BIC (shifted register) - 64-bit variant
1	01	0	-	ORR (shifted register) - 64-bit variant
1	01	1	-	ORN (shifted register) - 64-bit variant
1	10	0	-	EOR (shifted register) - 64-bit variant
1	10	1	-	EON (shifted register) - 64-bit variant
1	11	0	-	ANDS (shifted register) - 64-bit variant
1	11	1	-	BICS (shifted register) - 64-bit variant

Add/subtract (shifted register)

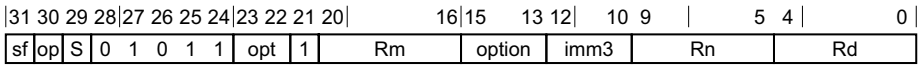
This section describes the encoding of the Add/subtract (shifted register) instruction class. The encodings in this section are decoded from *Data Processing -- Register* on page C4-576.



Decode fields					Instruction page
sf	op	S	shift	imm6	
-	-	-	11	-	Unallocated.
0	-	-	-	1xxxxx	Unallocated.
0	0	0	-	-	ADD (shifted register) - 32-bit variant
0	0	1	-	-	ADDS (shifted register) - 32-bit variant
0	1	0	-	-	SUB (shifted register) - 32-bit variant
0	1	1	-	-	SUBS (shifted register) - 32-bit variant
1	0	0	-	-	ADD (shifted register) - 64-bit variant
1	0	1	-	-	ADDS (shifted register) - 64-bit variant
1	1	0	-	-	SUB (shifted register) - 64-bit variant
1	1	1	-	-	SUBS (shifted register) - 64-bit variant

Add/subtract (extended register)

This section describes the encoding of the Add/subtract (extended register) instruction class. The encodings in this section are decoded from *Data Processing -- Register* on page C4-576.

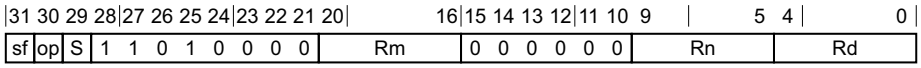


Decode fields					Instruction page
sf	op	S	opt	imm3	
-	-	-	-	1x1	Unallocated.
-	-	-	-	11x	Unallocated.
-	-	-	x1	-	Unallocated.
-	-	-	1x	-	Unallocated.
0	0	0	00	-	ADD (extended register) - 32-bit variant
0	0	1	00	-	ADDS (extended register) - 32-bit variant
0	1	0	00	-	SUB (extended register) - 32-bit variant
0	1	1	00	-	SUBS (extended register) - 32-bit variant
1	0	0	00	-	ADD (extended register) - 64-bit variant

Decode fields					Instruction page
sf	op	S	opt	imm3	
1	0	1	00	-	ADDS (extended register) - 64-bit variant
1	1	0	00	-	SUB (extended register) - 64-bit variant
1	1	1	00	-	SUBS (extended register) - 64-bit variant

Add/subtract (with carry)

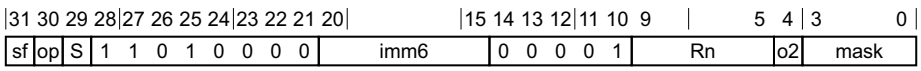
This section describes the encoding of the Add/subtract (with carry) instruction class. The encodings in this section are decoded from *Data Processing -- Register* on page C4-576.



Decode fields			Instruction page
sf	op	S	
0	0	0	ADC - 32-bit variant
0	0	1	ADCS - 32-bit variant
0	1	0	SBC - 32-bit variant
0	1	1	SBCS - 32-bit variant
1	0	0	ADC - 64-bit variant
1	0	1	ADCS - 64-bit variant
1	1	0	SBC - 64-bit variant
1	1	1	SBCS - 64-bit variant

Rotate right into flags

This section describes the encoding of the Rotate right into flags instruction class. The encodings in this section are decoded from *Data Processing -- Register* on page C4-576.

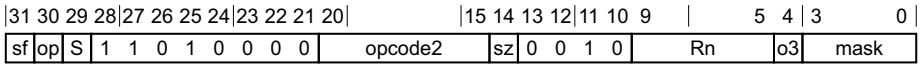


Decode fields				Instruction page	Feature
sf	op	S	o2		
0	-	-	-	Unallocated.	-
1	0	0	-	Unallocated.	-

Decode fields				Instruction page	Feature
sf	op	S	o2		
1	0	1	0	RMIF	FEAT_FlagM
1	0	1	1	Unallocated.	-
1	1	-	-	Unallocated.	-

Evaluate into flags

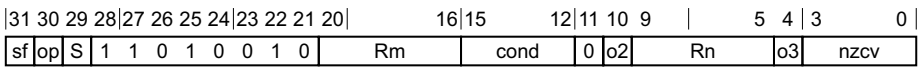
This section describes the encoding of the Evaluate into flags instruction class. The encodings in this section are decoded from *Data Processing -- Register* on page C4-576.



Decode fields							Instruction page	Feature
sf	op	S	opcode2	sz	o3	mask		
0	0	0	-	-	-	-	Unallocated.	-
0	0	1	!= 000000	-	-	-	Unallocated.	-
0	0	1	000000	-	0	!= 1101	Unallocated.	-
0	0	1	000000	-	1	-	Unallocated.	-
0	0	1	000000	0	0	1101	SETF8, SETF16 - SETF8 variant	FEAT_FlagM
0	0	1	000000	1	0	1101	SETF8, SETF16 - SETF16 variant	FEAT_FlagM
0	1	-	-	-	-	-	Unallocated.	-
1	-	-	-	-	-	-	Unallocated.	-

Conditional compare (register)

This section describes the encoding of the Conditional compare (register) instruction class. The encodings in this section are decoded from *Data Processing -- Register* on page C4-576.

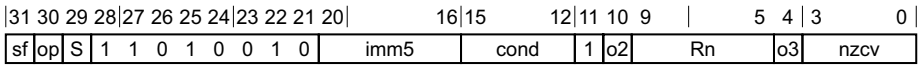


Decode fields					Instruction page
sf	op	S	o2	o3	
-	-	-	-	1	Unallocated.
-	-	-	1	-	Unallocated.
-	-	0	-	-	Unallocated.

Decode fields					Instruction page
sf	op	S	o2	o3	
0	0	1	0	0	CCMN (register) - 32-bit variant
0	1	1	0	0	CCMP (register) - 32-bit variant
1	0	1	0	0	CCMN (register) - 64-bit variant
1	1	1	0	0	CCMP (register) - 64-bit variant

Conditional compare (immediate)

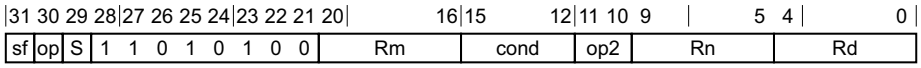
This section describes the encoding of the Conditional compare (immediate) instruction class. The encodings in this section are decoded from *Data Processing -- Register* on page C4-576.



Decode fields					Instruction page
sf	op	S	o2	o3	
-	-	-	-	1	Unallocated.
-	-	-	1	-	Unallocated.
-	-	0	-	-	Unallocated.
0	0	1	0	0	CCMN (immediate) - 32-bit variant
0	1	1	0	0	CCMP (immediate) - 32-bit variant
1	0	1	0	0	CCMN (immediate) - 64-bit variant
1	1	1	0	0	CCMP (immediate) - 64-bit variant

Conditional select

This section describes the encoding of the Conditional select instruction class. The encodings in this section are decoded from *Data Processing -- Register* on page C4-576.

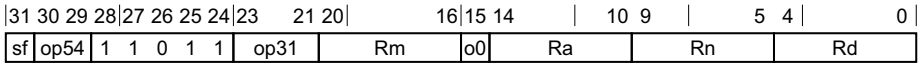


Decode fields				Instruction page
sf	op	S	op2	
-	-	-	1x	Unallocated.
-	-	1	-	Unallocated.
0	0	0	00	CSEL - 32-bit variant

Decode fields				Instruction page
sf	op	S	op2	
0	0	0	01	CSINC - 32-bit variant
0	1	0	00	CSINV - 32-bit variant
0	1	0	01	CSNEG - 32-bit variant
1	0	0	00	CSEL - 64-bit variant
1	0	0	01	CSINC - 64-bit variant
1	1	0	00	CSINV - 64-bit variant
1	1	0	01	CSNEG - 64-bit variant

Data-processing (3 source)

This section describes the encoding of the Data-processing (3 source) instruction class. The encodings in this section are decoded from *Data Processing -- Register* on page C4-576.



Decode fields				Instruction page
sf	op54	op31	o0	
-	00	010	1	Unallocated.
-	00	011	-	Unallocated.
-	00	100	-	Unallocated.
-	00	110	1	Unallocated.
-	00	111	-	Unallocated.
-	01	-	-	Unallocated.
-	1x	-	-	Unallocated.
0	00	000	0	MADD - 32-bit variant
0	00	000	1	MSUB - 32-bit variant
0	00	001	0	Unallocated.
0	00	001	1	Unallocated.
0	00	010	0	Unallocated.
0	00	101	0	Unallocated.
0	00	101	1	Unallocated.
0	00	110	0	Unallocated.
1	00	000	0	MADD - 64-bit variant

Decode fields				Instruction page
sf	op54	op31	o0	
1	00	000	1	MSUB - 64-bit variant
1	00	001	0	SMADDL
1	00	001	1	SMSUBL
1	00	010	0	SMULH
1	00	101	0	UMADDL
1	00	101	1	UMSUBL
1	00	110	0	UMULH

C4.1.68 Data Processing -- Scalar Floating-Point and Advanced SIMD

This section describes the encoding of the Data Processing -- Scalar Floating-Point and Advanced SIMD group. The encodings in this section are decoded from *A64 instruction set encoding* on page C4-380.

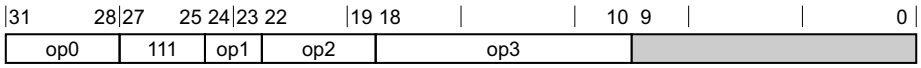


Table C4-69 Encoding table for the Data Processing -- Scalar Floating-Point and Advanced SIMD group

Decode fields				Decode group or instruction page	Feature
op0	op1	op2	op3		
0000	0x	x101	00xxxxx10	Unallocated.	-
0010	0x	x101	00xxxxx10	Unallocated.	-
0100	0x	x101	00xxxxx10	*Cryptographic AES* on page C4-589	-
0101	0x	x0xx	xxx0xxx00	*Cryptographic three-register SHA* on page C4-590	-
0101	0x	x0xx	xxx0xxx10	Unallocated.	-
0101	0x	x101	00xxxxx10	*Cryptographic two-register SHA* on page C4-590	-
0110	0x	x101	00xxxxx10	Unallocated.	-
0111	0x	x0xx	xxx0xxxx0	Unallocated.	-
0111	0x	x101	00xxxxx10	Unallocated.	-
01x1	00	00xx	xxx0xxxx1	*Advanced SIMD scalar copy* on page C4-591	-
01x1	01	00xx	xxx0xxxx1	Unallocated.	-
01x1	0x	0111	00xxxxx10	Unallocated.	-
01x1	0x	10xx	xxx00xxx1	*Advanced SIMD scalar three same FP16* on page C4-591	-
01x1	0x	10xx	xxx01xxx1	Unallocated.	-
01x1	0x	1111	00xxxxx10	*Advanced SIMD scalar two-register miscellaneous FP16* on page C4-592	-

Table C4-69 Encoding table for the Data Processing -- Scalar Floating-Point and Advanced SIMD group (continued)

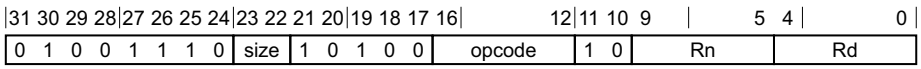
Decode fields				Decode group or instruction page	Feature
op0	op1	op2	op3		
01x1	0x	x0xx	xxx1xxxx0	Unallocated.	-
01x1	0x	x0xx	xxx1xxxx1	*Advanced SIMD scalar three same extra* on page C4-594	-
01x1	0x	x100	00xxxxx10	*Advanced SIMD scalar two-register miscellaneous* on page C4-594	-
01x1	0x	x110	00xxxxx10	*Advanced SIMD scalar pairwise* on page C4-596	-
01x1	0x	x1xx	1xxxxxx10	Unallocated.	-
01x1	0x	x1xx	x1xxxxx10	Unallocated.	-
01x1	0x	x1xx	xxxxxxx00	*Advanced SIMD scalar three different* on page C4-597	-
01x1	0x	x1xx	xxxxxxxx1	*Advanced SIMD scalar three same* on page C4-598	-
01x1	10	-	xxxxxxxx1	*Advanced SIMD scalar shift by immediate* on page C4-600	-
01x1	11	-	xxxxxxxx1	Unallocated.	-
01x1	1x	-	xxxxxxxx0	*Advanced SIMD scalar x indexed element* on page C4-602	-
0x00	0x	x0xx	xxx0xxx00	*Advanced SIMD table lookup* on page C4-603	-
0x00	0x	x0xx	xxx0xxx10	*Advanced SIMD permute* on page C4-604	-
0x10	0x	x0xx	xxx0xxxx0	*Advanced SIMD extract* on page C4-604	-
0xx0	00	00xx	xxx0xxxx1	*Advanced SIMD copy* on page C4-605	-
0xx0	01	00xx	xxx0xxxx1	Unallocated.	-
0xx0	0x	0111	00xxxxx10	Unallocated.	-
0xx0	0x	10xx	xxx00xxx1	*Advanced SIMD three same (FP16)* on page C4-605	-
0xx0	0x	10xx	xxx01xxx1	Unallocated.	-
0xx0	0x	1111	00xxxxx10	*Advanced SIMD two-register miscellaneous (FP16)* on page C4-607	-
0xx0	0x	x0xx	xxx1xxxx0	Unallocated.	-
0xx0	0x	x0xx	xxx1xxxx1	*Advanced SIMD three-register extension* on page C4-608	-
0xx0	0x	x100	00xxxxx10	*Advanced SIMD two-register miscellaneous* on page C4-610	-
0xx0	0x	x110	00xxxxx10	*Advanced SIMD across lanes* on page C4-612	-
0xx0	0x	x1xx	1xxxxxx10	Unallocated.	-
0xx0	0x	x1xx	x1xxxxx10	Unallocated.	-
0xx0	0x	x1xx	xxxxxxx00	*Advanced SIMD three different* on page C4-614	-
0xx0	0x	x1xx	xxxxxxxx1	*Advanced SIMD three same* on page C4-615	-
0xx0	10	0000	xxxxxxxx1	*Advanced SIMD modified immediate* on page C4-618	-
0xx0	10	!= 0000	xxxxxxxx1	*Advanced SIMD shift by immediate* on page C4-619	-
0xx0	11	-	xxxxxxxx1	Unallocated.	-

Table C4-69 Encoding table for the Data Processing -- Scalar Floating-Point and Advanced SIMD group (continued)

Decode fields				Decode group or instruction page	Feature
op0	op1	op2	op3		
0xx0	1x	-	xxxxxxxx0	*Advanced SIMD vector x indexed element* on page C4-621	-
1100	00	10xx	xxx10xxxx	*Cryptographic three-register, imm2* on page C4-623	-
1100	00	11xx	xxx1x00xx	*Cryptographic three-register SHA 512* on page C4-623	-
1100	00	-	xxx0xxxxx	*Cryptographic four-register* on page C4-624	-
1100	01	00xx	-	XAR	FEAT_SHA3
1100	01	1000	0001000xx	*Cryptographic two-register SHA 512* on page C4-624	-
1xx0	1x	-	-	Unallocated.	-
x0x1	0x	x0xx	-	*Conversion between floating-point and fixed-point* on page C4-625	-
x0x1	0x	x1xx	xxx000000	*Conversion between floating-point and integer* on page C4-626	-
x0x1	0x	x1xx	xxxx10000	*Floating-point data-processing (1 source)* on page C4-630	-
x0x1	0x	x1xx	xxxxx1000	*Floating-point compare* on page C4-632	-
x0x1	0x	x1xx	xxxxxx100	*Floating-point immediate* on page C4-633	-
x0x1	0x	x1xx	xxxxxxx01	*Floating-point conditional compare* on page C4-634	-
x0x1	0x	x1xx	xxxxxxx10	*Floating-point data-processing (2 source)* on page C4-634	-
x0x1	0x	x1xx	xxxxxxx11	*Floating-point conditional select* on page C4-636	-
x0x1	1x	-	-	*Floating-point data-processing (3 source)* on page C4-636	-

Cryptographic AES

This section describes the encoding of the Cryptographic AES instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.

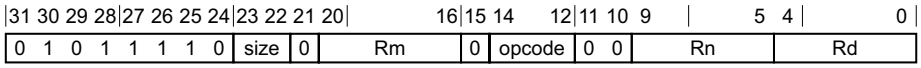


Decode fields		Instruction page
size	opcode	
-	x1xxx	Unallocated.
-	000xx	Unallocated.
-	1xxxx	Unallocated.
x1	-	Unallocated.
00	00100	AESE
00	00101	AESD

Decode fields		Instruction page
size	opcode	
00	00110	AESMC
00	00111	AESIMC
1x	-	Unallocated.

Cryptographic three-register SHA

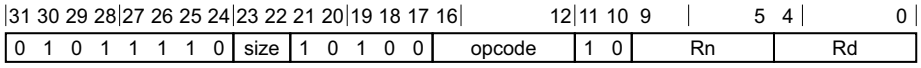
This section describes the encoding of the Cryptographic three-register SHA instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.



Decode fields		Instruction page
size	opcode	
-	111	Unallocated.
x1	-	Unallocated.
00	000	SHA1C
00	001	SHA1P
00	010	SHA1M
00	011	SHA1SU0
00	100	SHA256H
00	101	SHA256H2
00	110	SHA256SU1
1x	-	Unallocated.

Cryptographic two-register SHA

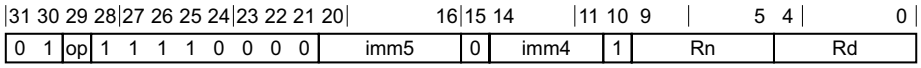
This section describes the encoding of the Cryptographic two-register SHA instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.



Decode fields		Instruction page
size	opcode	
-	xx1xx	Unallocated.
-	x1xxx	Unallocated.
-	1xxxx	Unallocated.
x1	-	Unallocated.
00	00000	SHA1H
00	00001	SHA1SU1
00	00010	SHA256SU0
00	00011	Unallocated.
1x	-	Unallocated.

Advanced SIMD scalar copy

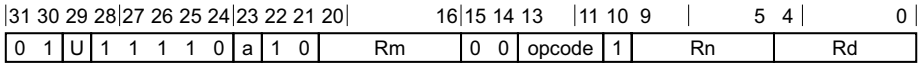
This section describes the encoding of the Advanced SIMD scalar copy instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.



Decode fields		Instruction page
op	imm4	
0	xxx1	Unallocated.
0	xx1x	Unallocated.
0	x1xx	Unallocated.
0	0000	DUP (element)
0	1xxx	Unallocated.
1	-	Unallocated.

Advanced SIMD scalar three same FP16

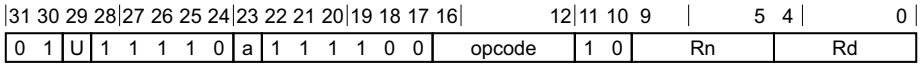
This section describes the encoding of the Advanced SIMD scalar three same FP16 instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.



Decode fields			Instruction page	Feature
U	a	opcode		
-	-	110	Unallocated.	-
-	1	011	Unallocated.	-
0	0	011	FMULX	FEAT_FP16
0	0	100	FCMEQ (register)	FEAT_FP16
0	0	101	Unallocated.	-
0	0	111	FRECPS	FEAT_FP16
0	1	100	Unallocated.	-
0	1	101	Unallocated.	-
0	1	111	FRSQRTS	FEAT_FP16
1	0	011	Unallocated.	-
1	0	100	FCMGE (register)	FEAT_FP16
1	0	101	FACGE	FEAT_FP16
1	0	111	Unallocated.	-
1	1	010	FABD	FEAT_FP16
1	1	100	FCMGT (register)	FEAT_FP16
1	1	101	FACGT	FEAT_FP16
1	1	111	Unallocated.	-

Advanced SIMD scalar two-register miscellaneous FP16

This section describes the encoding of the Advanced SIMD scalar two-register miscellaneous FP16 instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.

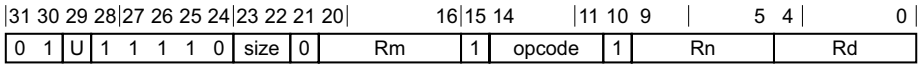


Decode fields			Instruction page	Feature
U	a	opcode		
-	-	00xxx	Unallocated.	-
-	-	010xx	Unallocated.	-
-	-	10xxx	Unallocated.	-
-	-	1100x	Unallocated.	-
-	-	11110	Unallocated.	-
-	0	011xx	Unallocated.	-
-	0	11111	Unallocated.	-
-	1	01111	Unallocated.	-
-	1	11100	Unallocated.	-
0	0	11010	FCVTNS (vector)	FEAT_FP16
0	0	11011	FCVTMS (vector)	FEAT_FP16
0	0	11100	FCVTAS (vector)	FEAT_FP16
0	0	11101	SCVTF (vector, integer)	FEAT_FP16
0	1	01100	FCMGT (zero)	FEAT_FP16
0	1	01101	FCMEQ (zero)	FEAT_FP16
0	1	01110	FCMLT (zero)	FEAT_FP16
0	1	11010	FCVTPS (vector)	FEAT_FP16
0	1	11011	FCVTZS (vector, integer)	FEAT_FP16
0	1	11101	FRECPE	FEAT_FP16
0	1	11111	FRECPX	FEAT_FP16
1	0	11010	FCVTNU (vector)	FEAT_FP16
1	0	11011	FCVTMU (vector)	FEAT_FP16
1	0	11100	FCVTAU (vector)	FEAT_FP16
1	0	11101	UCVTF (vector, integer)	FEAT_FP16
1	1	01100	FCMGE (zero)	FEAT_FP16
1	1	01101	FCMLE (zero)	FEAT_FP16
1	1	01110	Unallocated.	-
1	1	11010	FCVTPU (vector)	FEAT_FP16

Decode fields			Instruction page	Feature
U	a	opcode		
1	1	11011	FCVTZU (vector, integer)	FEAT_FP16
1	1	11101	FRSQRTE	FEAT_FP16
1	1	11111	Unallocated.	-

Advanced SIMD scalar three same extra

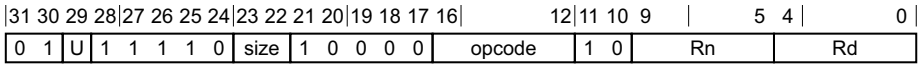
This section describes the encoding of the Advanced SIMD scalar three same extra instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.



Decode fields		Instruction page	Feature
U	opcode		
-	001x	Unallocated.	-
-	01xx	Unallocated.	-
-	1xxx	Unallocated.	-
0	0000	Unallocated.	-
0	0001	Unallocated.	-
1	0000	SQRDMLAH (vector)	FEAT_RDM
1	0001	SQRDMLSH (vector)	FEAT_RDM

Advanced SIMD scalar two-register miscellaneous

This section describes the encoding of the Advanced SIMD scalar two-register miscellaneous instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.



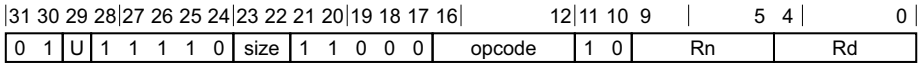
Decode fields			Instruction page
U	size	opcode	
-	-	0000x	Unallocated.
-	-	00010	Unallocated.
-	-	0010x	Unallocated.

Decode fields			Instruction page
U	size	opcode	
-	-	00110	Unallocated.
-	-	01111	Unallocated.
-	-	1000x	Unallocated.
-	-	10011	Unallocated.
-	-	10101	Unallocated.
-	-	10111	Unallocated.
-	-	1100x	Unallocated.
-	-	11110	Unallocated.
-	0x	011xx	Unallocated.
-	0x	11111	Unallocated.
-	1x	10110	Unallocated.
-	1x	11100	Unallocated.
0	-	00011	SUQADD
0	-	00111	SQABS
0	-	01000	CMGT (zero)
0	-	01001	CMEQ (zero)
0	-	01010	CMLT (zero)
0	-	01011	ABS
0	-	10010	Unallocated.
0	-	10100	SQXTN, SQXTN2
0	0x	10110	Unallocated.
0	0x	11010	FCVTNS (vector)
0	0x	11011	FCVTMS (vector)
0	0x	11100	FCVTAS (vector)
0	0x	11101	SCVTF (vector, integer)
0	1x	01100	FCMGT (zero)
0	1x	01101	FCMEQ (zero)
0	1x	01110	FCMLT (zero)
0	1x	11010	FCVTPS (vector)
0	1x	11011	FCVTZS (vector, integer)
0	1x	11101	FRECPE
0	1x	11111	FRECPX

Decode fields			Instruction page
U	size	opcode	
1	-	00011	USQADD
1	-	00111	SQNEG
1	-	01000	CMGE (zero)
1	-	01001	CMLE (zero)
1	-	01010	Unallocated.
1	-	01011	NEG (vector)
1	-	10010	SQXTUN, SQXTUN2
1	-	10100	UQXTN, UQXTN2
1	0x	10110	FCVTXN, FCVTXN2
1	0x	11010	FCVTNU (vector)
1	0x	11011	FCVTMU (vector)
1	0x	11100	FCVTAU (vector)
1	0x	11101	UCVTF (vector, integer)
1	1x	01100	FCMGE (zero)
1	1x	01101	FCMLE (zero)
1	1x	01110	Unallocated.
1	1x	11010	FCVTPU (vector)
1	1x	11011	FCVTZU (vector, integer)
1	1x	11101	FRSQRTE
1	1x	11111	Unallocated.

Advanced SIMD scalar pairwise

This section describes the encoding of the Advanced SIMD scalar pairwise instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.

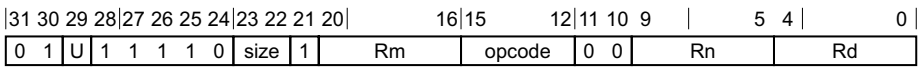


Decode fields			Instruction page	Feature
U	size	opcode		
-	-	00xxx	Unallocated.	-
-	-	010xx	Unallocated.	-
-	-	01110	Unallocated.	-

Decode fields			Instruction page	Feature
U	size	opcode		
-	-	10xxx	Unallocated.	-
-	-	1100x	Unallocated.	-
-	-	11010	Unallocated.	-
-	-	111xx	Unallocated.	-
-	1x	01101	Unallocated.	-
0	-	11011	ADDP (scalar)	-
0	0x	01100	FMAXNMP (scalar) - Encoding	FEAT_FP16
0	0x	01101	FADDP (scalar) - Encoding	FEAT_FP16
0	0x	01111	FMAXP (scalar) - Encoding	FEAT_FP16
0	1x	01100	FMINNMP (scalar) - Encoding	FEAT_FP16
0	1x	01111	FMINP (scalar) - Encoding	FEAT_FP16
1	-	11011	Unallocated.	-
1	0x	01100	FMAXNMP (scalar) - Encoding	-
1	0x	01101	FADDP (scalar) - Encoding	-
1	0x	01111	FMAXP (scalar) - Encoding	-
1	1x	01100	FMINNMP (scalar) - Encoding	-
1	1x	01111	FMINP (scalar) - Encoding	-

Advanced SIMD scalar three different

This section describes the encoding of the Advanced SIMD scalar three different instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.

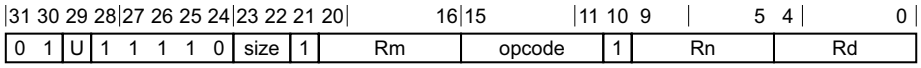


Decode fields		Instruction page
U	opcode	
-	00xx	Unallocated.
-	01xx	Unallocated.
-	1000	Unallocated.
-	1010	Unallocated.
-	1100	Unallocated.
-	111x	Unallocated.

Decode fields		Instruction page
U	opcode	
0	1001	SQDMLAL, SQDMLAL2 (vector)
0	1011	SQDMLSL, SQDMLSL2 (vector)
0	1101	SQDMULL, SQDMULL2 (vector)
1	1001	Unallocated.
1	1011	Unallocated.
1	1101	Unallocated.

Advanced SIMD scalar three same

This section describes the encoding of the Advanced SIMD scalar three same instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.



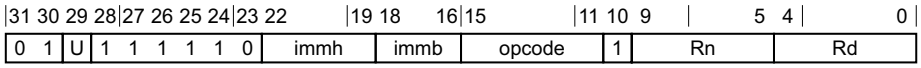
Decode fields			Instruction page
U	size	opcode	
-	-	00000	Unallocated.
-	-	0001x	Unallocated.
-	-	00100	Unallocated.
-	-	011xx	Unallocated.
-	-	1001x	Unallocated.
-	1x	11011	Unallocated.
0	-	00001	SQADD
0	-	00101	SQSUB
0	-	00110	CMGT (register)
0	-	00111	CMGE (register)
0	-	01000	SSHL
0	-	01001	SQSHL (register)
0	-	01010	SRSHL
0	-	01011	SQRSHL
0	-	10000	ADD (vector)
0	-	10001	CMTST
0	-	10100	Unallocated.

Decode fields			Instruction page
U	size	opcode	
0	-	10101	Unallocated.
0	-	10110	SQDMULH (vector)
0	-	10111	Unallocated.
0	0x	11000	Unallocated.
0	0x	11001	Unallocated.
0	0x	11010	Unallocated.
0	0x	11011	FMULX
0	0x	11100	FCMEQ (register)
0	0x	11101	Unallocated.
0	0x	11110	Unallocated.
0	0x	11111	FRECPS
0	1x	11000	Unallocated.
0	1x	11001	Unallocated.
0	1x	11010	Unallocated.
0	1x	11100	Unallocated.
0	1x	11101	Unallocated.
0	1x	11110	Unallocated.
0	1x	11111	FRSQRTS
1	-	00001	UQADD
1	-	00101	UQSUB
1	-	00110	CMHI (register)
1	-	00111	CMHS (register)
1	-	01000	USHL
1	-	01001	UQSHL (register)
1	-	01010	URSHL
1	-	01011	UQRSHL
1	-	10000	SUB (vector)
1	-	10001	CMEQ (register)
1	-	10100	Unallocated.
1	-	10101	Unallocated.
1	-	10110	SQRDMULH (vector)
1	-	10111	Unallocated.

Decode fields			Instruction page
U	size	opcode	
1	0x	11000	Unallocated.
1	0x	11001	Unallocated.
1	0x	11010	Unallocated.
1	0x	11011	Unallocated.
1	0x	11100	FCMGE (register)
1	0x	11101	FACGE
1	0x	11110	Unallocated.
1	0x	11111	Unallocated.
1	1x	11000	Unallocated.
1	1x	11001	Unallocated.
1	1x	11010	FABD
1	1x	11100	FCMGT (register)
1	1x	11101	FACGT
1	1x	11110	Unallocated.
1	1x	11111	Unallocated.

Advanced SIMD scalar shift by immediate

This section describes the encoding of the Advanced SIMD scalar shift by immediate instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.



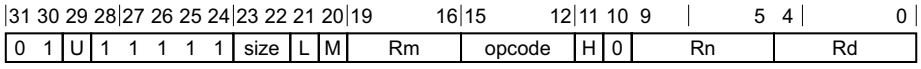
Decode fields			Instruction page
U	immh	opcode	
-	!= 0000	00001	Unallocated.
-	!= 0000	00011	Unallocated.
-	!= 0000	00101	Unallocated.
-	!= 0000	00111	Unallocated.
-	!= 0000	01001	Unallocated.
-	!= 0000	01011	Unallocated.
-	!= 0000	01101	Unallocated.

Decode fields			Instruction page
U	immh	opcode	
-	!= 0000	01111	Unallocated.
-	!= 0000	101xx	Unallocated.
-	!= 0000	110xx	Unallocated.
-	!= 0000	11101	Unallocated.
-	!= 0000	11110	Unallocated.
-	0000	-	Unallocated.
0	!= 0000	00000	SSHR
0	!= 0000	00010	SSRA
0	!= 0000	00100	SRSHR
0	!= 0000	00110	SRSRA
0	!= 0000	01000	Unallocated.
0	!= 0000	01010	SHL
0	!= 0000	01100	Unallocated.
0	!= 0000	01110	SQSHL (immediate)
0	!= 0000	10000	Unallocated.
0	!= 0000	10001	Unallocated.
0	!= 0000	10010	SQSHRN, SQSHRN2
0	!= 0000	10011	SQRSHRN, SQRSHRN2
0	!= 0000	11100	SCVTF (vector, fixed-point)
0	!= 0000	11111	FCVTZS (vector, fixed-point)
1	!= 0000	00000	USHR
1	!= 0000	00010	USRA
1	!= 0000	00100	URSHR
1	!= 0000	00110	URSRA
1	!= 0000	01000	SRI
1	!= 0000	01010	SLI
1	!= 0000	01100	SQSHLU
1	!= 0000	01110	UQSHL (immediate)
1	!= 0000	10000	SQSHRUN, SQSHRUN2
1	!= 0000	10001	SQRSHRUN, SQRSHRUN2
1	!= 0000	10010	UQSHRN, UQSHRN2

Decode fields			Instruction page
U	immh	opcode	
1	!= 0000	10011	UQRSHRN, UQRSHRN2
1	!= 0000	11100	UCVTF (vector, fixed-point)
1	!= 0000	11111	FCVTZU (vector, fixed-point)

Advanced SIMD scalar x indexed element

This section describes the encoding of the Advanced SIMD scalar x indexed element instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.

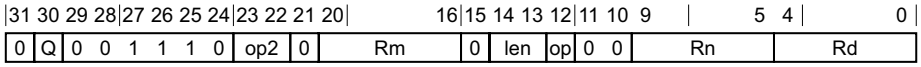


Decode fields			Instruction page	Feature
U	size	opcode		
-	-	0000	Unallocated.	-
-	-	0010	Unallocated.	-
-	-	0100	Unallocated.	-
-	-	0110	Unallocated.	-
-	-	1000	Unallocated.	-
-	-	1010	Unallocated.	-
-	-	1110	Unallocated.	-
-	01	0001	Unallocated.	-
-	01	0101	Unallocated.	-
-	01	1001	Unallocated.	-
0	-	0011	SQDMLAL, SQDMLAL2 (by element)	-
0	-	0111	SQDMLSL, SQDMLSL2 (by element)	-
0	-	1011	SQDMULL, SQDMULL2 (by element)	-
0	-	1100	SQDMULH (by element)	-
0	-	1101	SQRDMULH (by element)	-
0	-	1111	Unallocated.	-
0	00	0001	FMLA (by element) - Encoding	FEAT_FP16
0	00	0101	FMLS (by element) - Encoding	FEAT_FP16
0	00	1001	FMUL (by element) - Encoding	FEAT_FP16

Decode fields			Instruction page	Feature
U	size	opcode		
0	1x	0001	FMLA (by element) - Encoding	-
0	1x	0101	FMLS (by element) - Encoding	-
0	1x	1001	FMUL (by element) - Encoding	-
1	-	0011	Unallocated.	-
1	-	0111	Unallocated.	-
1	-	1011	Unallocated.	-
1	-	1100	Unallocated.	-
1	-	1101	SQRDMLAH (by element)	FEAT_RDM
1	-	1111	SQRDMLSH (by element)	FEAT_RDM
1	00	0001	Unallocated.	-
1	00	0101	Unallocated.	-
1	00	1001	FMULX (by element) - Encoding	FEAT_FP16
1	1x	0001	Unallocated.	-
1	1x	0101	Unallocated.	-
1	1x	1001	FMULX (by element) - Encoding	-

Advanced SIMD table lookup

This section describes the encoding of the Advanced SIMD table lookup instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.

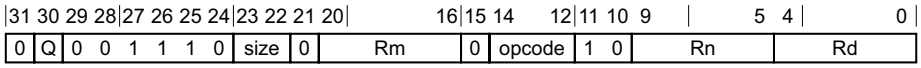


Decode fields			Instruction page
op2	len	op	
x1	-	-	Unallocated.
00	00	0	TBL - Single register table variant
00	00	1	TBX - Single register table variant
00	01	0	TBL - Two register table variant
00	01	1	TBX - Two register table variant
00	10	0	TBL - Three register table variant
00	10	1	TBX - Three register table variant

Decode fields			Instruction page
op2	len	op	
00	11	0	TBL - Four register table variant
00	11	1	TBX - Four register table variant
1x	-	-	Unallocated.

Advanced SIMD permute

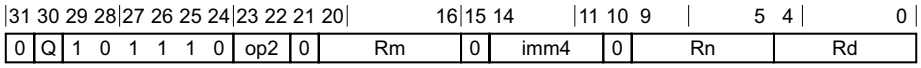
This section describes the encoding of the Advanced SIMD permute instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.



Decode fields	Instruction page
opcode	
000	Unallocated.
001	UZP1
010	TRN1
011	ZIP1
100	Unallocated.
101	UZP2
110	TRN2
111	ZIP2

Advanced SIMD extract

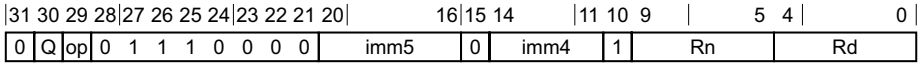
This section describes the encoding of the Advanced SIMD extract instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.



Decode fields	Instruction page
op2	
x1	Unallocated.
00	EXT
1x	Unallocated.

Advanced SIMD copy

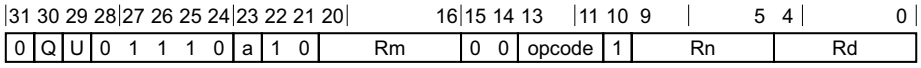
This section describes the encoding of the Advanced SIMD copy instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.



Decode fields				Instruction page
Q	op	imm5	imm4	
-	-	x0000	-	Unallocated.
-	0	-	0000	DUP (element)
-	0	-	0001	DUP (general)
-	0	-	0010	Unallocated.
-	0	-	0100	Unallocated.
-	0	-	0110	Unallocated.
-	0	-	1xxx	Unallocated.
0	0	-	0011	Unallocated.
0	0	-	0101	SMOV
0	0	-	0111	UMOV
0	1	-	-	Unallocated.
1	0	-	0011	INS (general)
1	0	-	0101	SMOV
1	0	x1000	0111	UMOV
1	1	-	-	INS (element)

Advanced SIMD three same (FP16)

This section describes the encoding of the Advanced SIMD three same (FP16) instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.

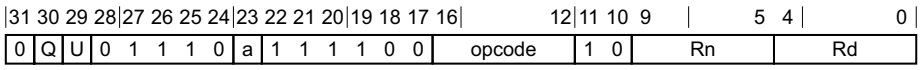


Decode fields			Instruction page	Feature
U	a	opcode		
0	0	000	FMAXNM (vector)	FEAT_FP16
0	0	001	FMLA (vector)	FEAT_FP16
0	0	010	FADD (vector)	FEAT_FP16
0	0	011	FMULX	FEAT_FP16
0	0	100	FCMEQ (register)	FEAT_FP16
0	0	101	Unallocated.	-
0	0	110	FMAX (vector)	FEAT_FP16
0	0	111	FRECPS	FEAT_FP16
0	1	000	FMINNM (vector)	FEAT_FP16
0	1	001	FMLS (vector)	FEAT_FP16
0	1	010	FSUB (vector)	FEAT_FP16
0	1	011	Unallocated.	-
0	1	100	Unallocated.	-
0	1	101	Unallocated.	-
0	1	110	FMIN (vector)	FEAT_FP16
0	1	111	FRSQRTS	FEAT_FP16
1	0	000	FMAXNMP (vector)	FEAT_FP16
1	0	001	Unallocated.	-
1	0	010	FADDP (vector)	FEAT_FP16
1	0	011	FMUL (vector)	FEAT_FP16
1	0	100	FCMGE (register)	FEAT_FP16
1	0	101	FACGE	FEAT_FP16
1	0	110	FMAXP (vector)	FEAT_FP16
1	0	111	FDIV (vector)	FEAT_FP16
1	1	000	FMINNMP (vector)	FEAT_FP16
1	1	001	Unallocated.	-
1	1	010	FABD	FEAT_FP16
1	1	011	Unallocated.	-

Decode fields			Instruction page	Feature
U	a	opcode		
1	1	100	FCMGT (register)	FEAT_FP16
1	1	101	FACGT	FEAT_FP16
1	1	110	FMINP (vector)	FEAT_FP16
1	1	111	Unallocated.	-

Advanced SIMD two-register miscellaneous (FP16)

This section describes the encoding of the Advanced SIMD two-register miscellaneous (FP16) instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.

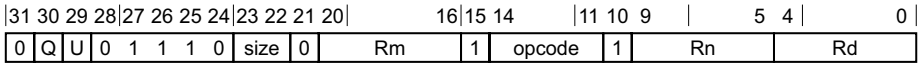


Decode fields			Instruction page	Feature
U	a	opcode		
-	-	00xxx	Unallocated.	-
-	-	010xx	Unallocated.	-
-	-	10xxx	Unallocated.	-
-	-	11110	Unallocated.	-
-	0	011xx	Unallocated.	-
-	0	11111	Unallocated.	-
-	1	11100	Unallocated.	-
0	0	11000	FRINTN (vector)	FEAT_FP16
0	0	11001	FRINTM (vector)	FEAT_FP16
0	0	11010	FCVTNS (vector)	FEAT_FP16
0	0	11011	FCVTMS (vector)	FEAT_FP16
0	0	11100	FCVTAS (vector)	FEAT_FP16
0	0	11101	SCVTF (vector, integer)	FEAT_FP16
0	1	01100	FCMGT (zero)	FEAT_FP16
0	1	01101	FCMEQ (zero)	FEAT_FP16
0	1	01110	FCMLT (zero)	FEAT_FP16
0	1	01111	FABS (vector)	FEAT_FP16
0	1	11000	FRINTP (vector)	FEAT_FP16

Decode fields			Instruction page	Feature
U	a	opcode		
0	1	11001	FRINTZ (vector)	FEAT_FP16
0	1	11010	FCVTPS (vector)	FEAT_FP16
0	1	11011	FCVTZS (vector, integer)	FEAT_FP16
0	1	11101	FRECPE	FEAT_FP16
0	1	11111	Unallocated.	-
1	0	11000	FRINTA (vector)	FEAT_FP16
1	0	11001	FRINTX (vector)	FEAT_FP16
1	0	11010	FCVTNU (vector)	FEAT_FP16
1	0	11011	FCVTMU (vector)	FEAT_FP16
1	0	11100	FCVTAU (vector)	FEAT_FP16
1	0	11101	UCVTF (vector, integer)	FEAT_FP16
1	1	01100	FCMGE (zero)	FEAT_FP16
1	1	01101	FCMLE (zero)	FEAT_FP16
1	1	01110	Unallocated.	-
1	1	01111	FNEG (vector)	FEAT_FP16
1	1	11000	Unallocated.	-
1	1	11001	FRINTI (vector)	FEAT_FP16
1	1	11010	FCVTPU (vector)	FEAT_FP16
1	1	11011	FCVTZU (vector, integer)	FEAT_FP16
1	1	11101	FRSQRTE	FEAT_FP16
1	1	11111	FSQRT (vector)	FEAT_FP16

Advanced SIMD three-register extension

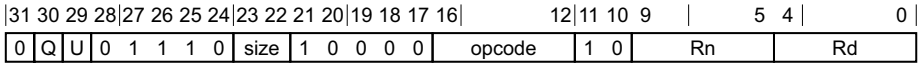
This section describes the encoding of the Advanced SIMD three-register extension instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.



Decode fields				Instruction page	Feature
Q	U	size	opcode		
-	-	0x	0011	Unallocated.	-
-	-	11	0011	Unallocated.	-
-	0	-	0000	Unallocated.	-
-	0	-	0001	Unallocated.	-
-	0	-	0010	SDOT (vector)	FEAT_DotProd
-	0	-	1xxx	Unallocated.	-
-	0	10	0011	USDOT (vector)	FEAT_I8MM
-	1	-	0000	SQRDMLAH (vector)	FEAT_RDM
-	1	-	0001	SQRDMLSH (vector)	FEAT_RDM
-	1	-	0010	UDOT (vector)	FEAT_DotProd
-	1	-	10xx	FCMLA	FEAT_FCMA
-	1	-	11x0	FCADD	FEAT_FCMA
-	1	00	1101	Unallocated.	-
-	1	00	1111	Unallocated.	-
-	1	01	1111	BFDOT (vector)	FEAT_BF16
-	1	1x	1101	Unallocated.	-
-	1	10	0011	Unallocated.	-
-	1	10	1111	Unallocated.	-
-	1	11	1111	BFMLALB, BFMLALT (vector)	FEAT_BF16
0	-	-	01xx	Unallocated.	-
0	1	01	1101	Unallocated.	-
1	-	0x	01xx	Unallocated.	-
1	-	1x	011x	Unallocated.	-
1	0	10	0100	SMMLA (vector)	FEAT_I8MM
1	0	10	0101	USMMLA (vector)	FEAT_I8MM
1	1	01	1101	BFMMLA	FEAT_BF16
1	1	10	0100	UMMLA (vector)	FEAT_I8MM
1	1	10	0101	Unallocated.	-

Advanced SIMD two-register miscellaneous

This section describes the encoding of the Advanced SIMD two-register miscellaneous instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.



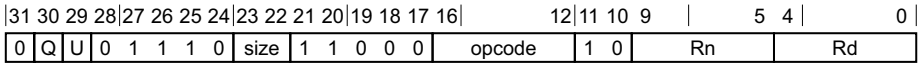
Decode fields			Instruction page	Feature
U	size	opcode		
-	-	1000x	Unallocated.	-
-	-	10101	Unallocated.	-
-	0x	011xx	Unallocated.	-
-	1x	10111	Unallocated.	-
-	1x	11110	Unallocated.	-
-	11	10110	Unallocated.	-
0	-	00000	REV64	-
0	-	00001	REV16 (vector)	-
0	-	00010	SADDLP	-
0	-	00011	SUQADD	-
0	-	00100	CLS (vector)	-
0	-	00101	CNT	-
0	-	00110	SADALP	-
0	-	00111	SQABS	-
0	-	01000	CMGT (zero)	-
0	-	01001	CMEQ (zero)	-
0	-	01010	CMLT (zero)	-
0	-	01011	ABS	-
0	-	10010	XTN, XTN2	-
0	-	10011	Unallocated.	-
0	-	10100	SQXTN, SQXTN2	-
0	0x	10110	FCVTN, FCVTN2	-
0	0x	10111	FCVTL, FCVTL2	-
0	0x	11000	FRINTN (vector)	-
0	0x	11001	FRINTM (vector)	-

Decode fields			Instruction page	Feature
U	size	opcode		
0	0x	11010	FCVTNS (vector)	-
0	0x	11011	FCVTMS (vector)	-
0	0x	11100	FCVTAS (vector)	-
0	0x	11101	SCVTF (vector, integer)	-
0	0x	11110	FRINT32Z (vector)	FEAT_FRINTTS
0	0x	11111	FRINT64Z (vector)	FEAT_FRINTTS
0	1x	01100	FCMGT (zero)	-
0	1x	01101	FCMEQ (zero)	-
0	1x	01110	FCMLT (zero)	-
0	1x	01111	FABS (vector)	-
0	1x	11000	FRINTP (vector)	-
0	1x	11001	FRINTZ (vector)	-
0	1x	11010	FCVTPS (vector)	-
0	1x	11011	FCVTZS (vector, integer)	-
0	1x	11100	URECPE	-
0	1x	11101	FRECPE	-
0	1x	11111	Unallocated.	-
0	10	10110	BFCVTN, BFCVTN2	FEAT_BF16
1	-	00000	REV32 (vector)	-
1	-	00001	Unallocated.	-
1	-	00010	UADDLP	-
1	-	00011	USQADD	-
1	-	00100	CLZ (vector)	-
1	-	00110	UADALP	-
1	-	00111	SQNEG	-
1	-	01000	CMGE (zero)	-
1	-	01001	CMLE (zero)	-
1	-	01010	Unallocated.	-
1	-	01011	NEG (vector)	-
1	-	10010	SQXTUN, SQXTUN2	-
1	-	10011	SHLL, SHLL2	-
1	-	10100	UQXTN, UQXTN2	-

Decode fields			Instruction page	Feature
U	size	opcode		
1	0x	10110	FCVTXN, FCVTXN2	-
1	0x	10111	Unallocated.	-
1	0x	11000	FRINTA (vector)	-
1	0x	11001	FRINTX (vector)	-
1	0x	11010	FCVTNU (vector)	-
1	0x	11011	FCVTMU (vector)	-
1	0x	11100	FCVTAU (vector)	-
1	0x	11101	UCVTF (vector, integer)	-
1	0x	11110	FRINT32X (vector)	FEAT_FRINTTS
1	0x	11111	FRINT64X (vector)	FEAT_FRINTTS
1	00	00101	NOT	-
1	01	00101	RBIT (vector)	-
1	1x	00101	Unallocated.	-
1	1x	01100	FCMGE (zero)	-
1	1x	01101	FCMLE (zero)	-
1	1x	01110	Unallocated.	-
1	1x	01111	FNEG (vector)	-
1	1x	11000	Unallocated.	-
1	1x	11001	FRINTI (vector)	-
1	1x	11010	FCVTPU (vector)	-
1	1x	11011	FCVTZU (vector, integer)	-
1	1x	11100	URSQRTE	-
1	1x	11101	FRSQRTE	-
1	1x	11111	FSQRT (vector)	-
1	10	10110	Unallocated.	-

Advanced SIMD across lanes

This section describes the encoding of the Advanced SIMD across lanes instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.

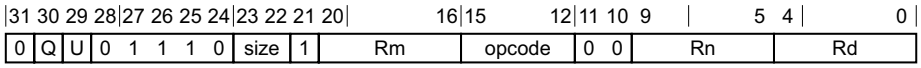


Decode fields			Instruction page	Feature
U	size	opcode		
-	-	0000x	Unallocated.	-
-	-	00010	Unallocated.	-
-	-	001xx	Unallocated.	-
-	-	0100x	Unallocated.	-
-	-	01011	Unallocated.	-
-	-	01101	Unallocated.	-
-	-	01110	Unallocated.	-
-	-	10xxx	Unallocated.	-
-	-	1100x	Unallocated.	-
-	-	111xx	Unallocated.	-
0	-	00011	SADDLV	-
0	-	01010	SMAXV	-
0	-	11010	SMINV	-
0	-	11011	ADDV	-
0	00	01100	FMAXNMV - Encoding	FEAT_FP16
0	00	01111	FMAXV - Encoding	FEAT_FP16
0	01	01100	Unallocated.	-
0	01	01111	Unallocated.	-
0	10	01100	FMINNMV - Encoding	FEAT_FP16
0	10	01111	FMINV - Encoding	FEAT_FP16
0	11	01100	Unallocated.	-
0	11	01111	Unallocated.	-
1	-	00011	UADDLV	-
1	-	01010	UMAXV	-
1	-	11010	UMINV	-
1	-	11011	Unallocated.	-
1	0x	01100	FMAXNMV - Encoding	-

Decode fields			Instruction page	Feature
U	size	opcode		
1	0x	01111	FMAXV - Encoding	-
1	1x	01100	FMINNMV - Encoding	-
1	1x	01111	FMINV - Encoding	-

Advanced SIMD three different

This section describes the encoding of the Advanced SIMD three different instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.

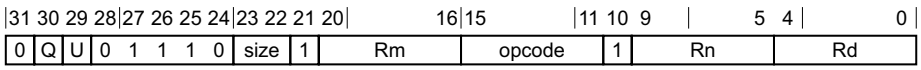


Decode fields		Instruction page
U	opcode	
-	1111	Unallocated.
0	0000	SADDL, SADDL2
0	0001	SADDW, SADDW2
0	0010	SSUBL, SSUBL2
0	0011	SSUBW, SSUBW2
0	0100	ADDHN, ADDHN2
0	0101	SABAL, SABAL2
0	0110	SUBHN, SUBHN2
0	0111	SABDL, SABDL2
0	1000	SMLAL, SMLAL2 (vector)
0	1001	SQDMLAL, SQDMLAL2 (vector)
0	1010	SMLSL, SMLSL2 (vector)
0	1011	SQDMLSL, SQDMLSL2 (vector)
0	1100	SMULL, SMULL2 (vector)
0	1101	SQDMULL, SQDMULL2 (vector)
0	1110	PMULL, PMULL2
1	0000	UADDL, UADDL2
1	0001	UADDW, UADDW2
1	0010	USUBL, USUBL2
1	0011	USUBW, USUBW2

Decode fields		Instruction page
U	opcode	
1	0100	RADDHN, RADDHN2
1	0101	UABAL, UABAL2
1	0110	RSUBHN, RSUBHN2
1	0111	UABDL, UABDL2
1	1000	UMLAL, UMLAL2 (vector)
1	1001	Unallocated.
1	1010	UMLSL, UMLSL2 (vector)
1	1011	Unallocated.
1	1100	UMULL, UMULL2 (vector)
1	1101	Unallocated.
1	1110	Unallocated.

Advanced SIMD three same

This section describes the encoding of the Advanced SIMD three same instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.



Decode fields			Instruction page	Feature
U	size	opcode		
0	-	00000	SHADD	-
0	-	00001	SQADD	-
0	-	00010	SRHADD	-
0	-	00100	SHSUB	-
0	-	00101	SQSUB	-
0	-	00110	CMGT (register)	-
0	-	00111	CMGE (register)	-
0	-	01000	SSHL	-
0	-	01001	SQSHL (register)	-
0	-	01010	SRSHL	-
0	-	01011	SQRSHL	-
0	-	01100	SMAX	-

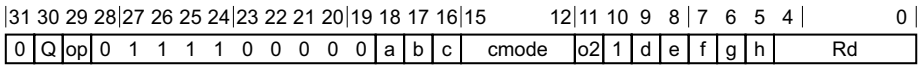
Decode fields			Instruction page	Feature
U	size	opcode		
0	-	01101	SMIN	-
0	-	01110	SABD	-
0	-	01111	SABA	-
0	-	10000	ADD (vector)	-
0	-	10001	CMTST	-
0	-	10010	MLA (vector)	-
0	-	10011	MUL (vector)	-
0	-	10100	SMAXP	-
0	-	10101	SMINP	-
0	-	10110	SQDMULH (vector)	-
0	-	10111	ADDP (vector)	-
0	0x	11000	FMAXNM (vector)	-
0	0x	11001	FMLA (vector)	-
0	0x	11010	FADD (vector)	-
0	0x	11011	FMULX	-
0	0x	11100	FCMEQ (register)	-
0	0x	11110	FMAX (vector)	-
0	0x	11111	FRECPS	-
0	00	00011	AND (vector)	-
0	00	11101	FMLAL, FMLAL2 (vector) - Encoding	FEAT_FHM
0	01	00011	BIC (vector, register)	-
0	01	11101	Unallocated.	-
0	1x	11000	FMINNM (vector)	-
0	1x	11001	FMLS (vector)	-
0	1x	11010	FSUB (vector)	-
0	1x	11011	Unallocated.	-
0	1x	11100	Unallocated.	-
0	1x	11110	FMIN (vector)	-
0	1x	11111	FRSQRTS	-
0	10	00011	ORR (vector, register)	-
0	10	11101	FMLSL, FMLSL2 (vector) - Encoding	FEAT_FHM
0	11	00011	ORN (vector)	-

Decode fields			Instruction page	Feature
U	size	opcode		
0	11	11101	Unallocated.	-
1	-	00000	UHADD	-
1	-	00001	UQADD	-
1	-	00010	URHADD	-
1	-	00100	UHSUB	-
1	-	00101	UQSUB	-
1	-	00110	CMHI (register)	-
1	-	00111	CMHS (register)	-
1	-	01000	USHL	-
1	-	01001	UQSHL (register)	-
1	-	01010	URSHL	-
1	-	01011	UQRSHL	-
1	-	01100	UMAX	-
1	-	01101	UMIN	-
1	-	01110	UABD	-
1	-	01111	UABA	-
1	-	10000	SUB (vector)	-
1	-	10001	CMEQ (register)	-
1	-	10010	MLS (vector)	-
1	-	10011	PMUL	-
1	-	10100	UMAXP	-
1	-	10101	UMINP	-
1	-	10110	SQRDMULH (vector)	-
1	-	10111	Unallocated.	-
1	0x	11000	FMAXNMP (vector)	-
1	0x	11010	FADDP (vector)	-
1	0x	11011	FMUL (vector)	-
1	0x	11100	FCMGE (register)	-
1	0x	11101	FACGE	-
1	0x	11110	FMAXP (vector)	-
1	0x	11111	FDIV (vector)	-
1	00	00011	EOR (vector)	-

Decode fields			Instruction page	Feature
U	size	opcode		
1	00	11001	FMLAL, FMLAL2 (vector) - Encoding	FEAT_FHM
1	01	00011	BSL	-
1	01	11001	Unallocated.	-
1	1x	11000	FMINNMP (vector)	-
1	1x	11010	FABD	-
1	1x	11011	Unallocated.	-
1	1x	11100	FCMGT (register)	-
1	1x	11101	FACGT	-
1	1x	11110	FMINP (vector)	-
1	1x	11111	Unallocated.	-
1	10	00011	BIT	-
1	10	11001	FMLSL, FMLSL2 (vector) - Encoding	FEAT_FHM
1	11	00011	BIF	-
1	11	11001	Unallocated.	-

Advanced SIMD modified immediate

This section describes the encoding of the Advanced SIMD modified immediate instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.

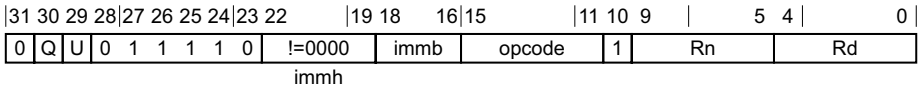


Decode fields				Instruction page	Feature
Q	op	cmode	o2		
-	0	0xxx	1	Unallocated.	-
-	0	0xx0	0	MOVI - 32-bit shifted immediate variant	-
-	0	0xx1	0	ORR (vector, immediate) - 32-bit variant	-
-	0	10xx	1	Unallocated.	-
-	0	10x0	0	MOVI - 16-bit shifted immediate variant	-
-	0	10x1	0	ORR (vector, immediate) - 16-bit variant	-
-	0	110x	0	MOVI - 32-bit shifting ones variant	-
-	0	110x	1	Unallocated.	-
-	0	1110	0	MOVI - 8-bit variant	-

Decode fields				Instruction page	Feature
Q	op	cmode	o2		
-	0	1110	1	Unallocated.	-
-	0	1111	0	FMOV (vector, immediate) - Single-precision variant	-
-	0	1111	1	FMOV (vector, immediate) - Encoding	FEAT_FP16
-	1	-	1	Unallocated.	-
-	1	0xx0	0	MVNI - 32-bit shifted immediate variant	-
-	1	0xx1	0	BIC (vector, immediate) - 32-bit variant	-
-	1	10x0	0	MVNI - 16-bit shifted immediate variant	-
-	1	10x1	0	BIC (vector, immediate) - 16-bit variant	-
-	1	110x	0	MVNI - 32-bit shifting ones variant	-
0	1	1110	0	MOVI - 64-bit scalar variant	-
0	1	1111	0	Unallocated.	-
1	1	1110	0	MOVI - 64-bit vector variant	-
1	1	1111	0	FMOV (vector, immediate) - Double-precision variant	-

Advanced SIMD shift by immediate

This section describes the encoding of the Advanced SIMD shift by immediate instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.



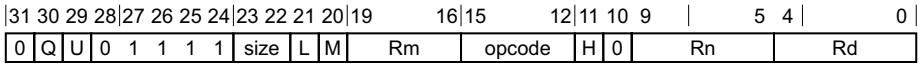
Decode fields		Instruction page
U	opcode	
-	00001	Unallocated.
-	00011	Unallocated.
-	00101	Unallocated.
-	00111	Unallocated.
-	01001	Unallocated.
-	01011	Unallocated.
-	01101	Unallocated.
-	01111	Unallocated.
-	10101	Unallocated.
-	1011x	Unallocated.

Decode fields		Instruction page
U	opcode	
-	110xx	Unallocated.
-	11101	Unallocated.
-	11110	Unallocated.
0	00000	SSHR
0	00010	SSRA
0	00100	SRSHR
0	00110	SRSRA
0	01000	Unallocated.
0	01010	SHL
0	01100	Unallocated.
0	01110	SQSHL (immediate)
0	10000	SHRN, SHRN2
0	10001	RSHRN, RSHRN2
0	10010	SQSHRN, SQSHRN2
0	10011	SQRSHRN, SQRSHRN2
0	10100	SSHLL, SSHLL2
0	11100	SCVTF (vector, fixed-point)
0	11111	FCVTZS (vector, fixed-point)
1	00000	USHR
1	00010	USRA
1	00100	URSHR
1	00110	URSRA
1	01000	SRI
1	01010	SLI
1	01100	SQSHLU
1	01110	UQSHL (immediate)
1	10000	SQSHRUN, SQSHRUN2
1	10001	SQRSHRUN, SQRSHRUN2
1	10010	UQSHRN, UQSHRN2
1	10011	UQRSHRN, UQRSHRN2

Decode fields		Instruction page
U	opcode	
1	10100	USHLL, USHLL2
1	11100	UCVTF (vector, fixed-point)
1	11111	FCVTZU (vector, fixed-point)

Advanced SIMD vector x indexed element

This section describes the encoding of the Advanced SIMD vector x indexed element instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.



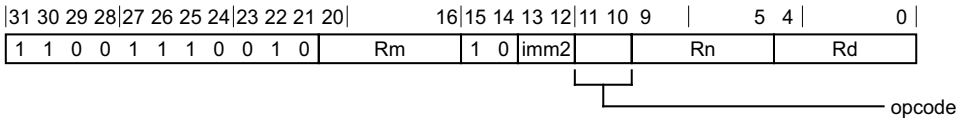
Decode fields			Instruction page	Feature
U	size	opcode		
-	01	1001	Unallocated.	-
0	-	0010	SMLAL, SMLAL2 (by element)	-
0	-	0011	SQDMLAL, SQDMLAL2 (by element)	-
0	-	0110	SMLSL, SMLSL2 (by element)	-
0	-	0111	SQDMLSL, SQDMLSL2 (by element)	-
0	-	1000	MUL (by element)	-
0	-	1010	SMULL, SMULL2 (by element)	-
0	-	1011	SQDMULL, SQDMULL2 (by element)	-
0	-	1100	SQDMULH (by element)	-
0	-	1101	SQRDMULH (by element)	-
0	-	1110	SDOT (by element)	FEAT_DotProd
0	0x	0000	Unallocated.	-
0	0x	0100	Unallocated.	-
0	00	0001	FMLA (by element) - Encoding	FEAT_FP16
0	00	0101	FMLS (by element) - Encoding	FEAT_FP16
0	00	1001	FMUL (by element) - Encoding	FEAT_FP16
0	00	1111	SUDOT (by element)	FEAT_I8MM
0	01	0001	Unallocated.	-
0	01	0101	Unallocated.	-

Decode fields			Instruction page	Feature
U	size	opcode		
0	01	1111	BFDOT (by element)	FEAT_BF16
0	1x	0001	FMLA (by element) - Encoding	-
0	1x	0101	FMLS (by element) - Encoding	-
0	1x	1001	FMUL (by element) - Encoding	-
0	10	0000	FMLAL, FMLAL2 (by element) - Encoding	FEAT_FHM
0	10	0100	FMLSL, FMLSL2 (by element) - Encoding	FEAT_FHM
0	10	1111	USDOT (by element)	FEAT_I8MM
0	11	0000	Unallocated.	-
0	11	0100	Unallocated.	-
0	11	1111	BFMLALB, BFMLALT (by element)	FEAT_BF16
1	-	0000	MLA (by element)	-
1	-	0010	UMLAL, UMLAL2 (by element)	-
1	-	0100	MLS (by element)	-
1	-	0110	UMLSL, UMLSL2 (by element)	-
1	-	1010	UMULL, UMULL2 (by element)	-
1	-	1011	Unallocated.	-
1	-	1101	SQRDMLAH (by element)	FEAT_RDM
1	-	1110	UDOT (by element)	FEAT_DotProd
1	-	1111	SQRDMLSH (by element)	FEAT_RDM
1	0x	1000	Unallocated.	-
1	0x	1100	Unallocated.	-
1	00	0001	Unallocated.	-
1	00	0011	Unallocated.	-
1	00	0101	Unallocated.	-
1	00	0111	Unallocated.	-
1	00	1001	FMULX (by element) - Encoding	FEAT_FP16
1	01	0xx1	FCMLA (by element)	FEAT_FCMA
1	1x	1001	FMULX (by element) - Encoding	-
1	10	0xx1	FCMLA (by element)	FEAT_FCMA
1	10	1000	FMLAL, FMLAL2 (by element) - Encoding	FEAT_FHM
1	10	1100	FMLSL, FMLSL2 (by element) - Encoding	FEAT_FHM
1	11	0001	Unallocated.	-

Decode fields			Instruction page	Feature
U	size	opcode		
1	11	0011	Unallocated.	-
1	11	0101	Unallocated.	-
1	11	0111	Unallocated.	-
1	11	1000	Unallocated.	-
1	11	1100	Unallocated.	-

Cryptographic three-register, imm2

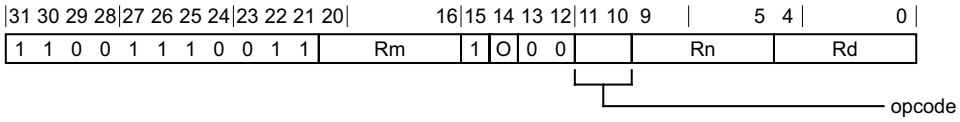
This section describes the encoding of the Cryptographic three-register, imm2 instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.



Decode fields	Instruction page	Feature
opcode		
00	SM3TT1A	FEAT_SM3
01	SM3TT1B	FEAT_SM3
10	SM3TT2A	FEAT_SM3
11	SM3TT2B	FEAT_SM3

Cryptographic three-register SHA 512

This section describes the encoding of the Cryptographic three-register SHA 512 instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.

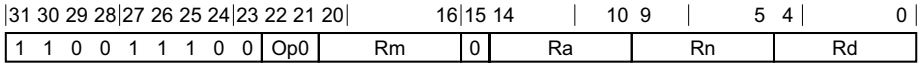


Decode fields		Instruction page	Feature
O	opcode		
0	00	SHA512H	FEAT_SHA512
0	01	SHA512H2	FEAT_SHA512
0	10	SHA512SU1	FEAT_SHA512

Decode fields		Instruction page	Feature
O	opcode		
0	11	RAX1	FEAT_SHA3
1	00	SM3PARTW1	FEAT_SM3
1	01	SM3PARTW2	FEAT_SM3
1	10	SM4EKEY	FEAT_SM4
1	11	Unallocated.	-

Cryptographic four-register

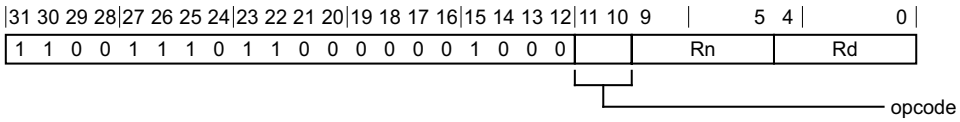
This section describes the encoding of the Cryptographic four-register instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.



Decode fields	Instruction page	Feature
Op0		
00	EOR3	FEAT_SHA3
01	BCAX	FEAT_SHA3
10	SM3SS1	FEAT_SM3
11	Unallocated.	-

Cryptographic two-register SHA 512

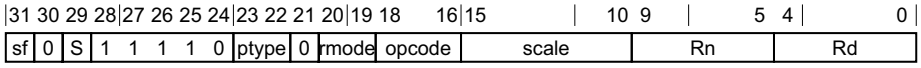
This section describes the encoding of the Cryptographic two-register SHA 512 instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.



Decode fields	Instruction page	Feature
opcode		
00	SHA512SU0	FEAT_SHA512
01	SM4E	FEAT_SM4
1x	Unallocated.	-

Conversion between floating-point and fixed-point

This section describes the encoding of the Conversion between floating-point and fixed-point instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.

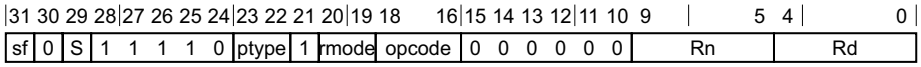


Decode fields						Instruction page	Feature
sf	S	ptype	rmode	opcode	scale		
-	-	-	-	1xx	-	Unallocated.	-
-	-	-	x0	00x	-	Unallocated.	-
-	-	-	x1	01x	-	Unallocated.	-
-	-	-	0x	00x	-	Unallocated.	-
-	-	-	1x	01x	-	Unallocated.	-
-	-	10	-	-	-	Unallocated.	-
-	1	-	-	-	-	Unallocated.	-
0	-	-	-	-	0xxxxx	Unallocated.	-
0	0	00	00	010	-	SCVTF (scalar, fixed-point) - 32-bit to single-precision variant	-
0	0	00	00	011	-	UCVTF (scalar, fixed-point) - 32-bit to single-precision variant	-
0	0	00	11	000	-	FCVTZS (scalar, fixed-point) - Single-precision to 32-bit variant	-
0	0	00	11	001	-	FCVTZU (scalar, fixed-point) - Single-precision to 32-bit variant	-
0	0	01	00	010	-	SCVTF (scalar, fixed-point) - 32-bit to double-precision variant	-
0	0	01	00	011	-	UCVTF (scalar, fixed-point) - 32-bit to double-precision variant	-
0	0	01	11	000	-	FCVTZS (scalar, fixed-point) - Double-precision to 32-bit variant	-
0	0	01	11	001	-	FCVTZU (scalar, fixed-point) - Double-precision to 32-bit variant	-
0	0	11	00	010	-	SCVTF (scalar, fixed-point) - 32-bit to half-precision variant	FEAT_FP16
0	0	11	00	011	-	UCVTF (scalar, fixed-point) - 32-bit to half-precision variant	FEAT_FP16

Decode fields						Instruction page	Feature
sf	S	ptype	rmode	opcode	scale		
0	0	11	11	000	-	FCVTZS (scalar, fixed-point) - Half-precision to 32-bit variant	FEAT_FP16
0	0	11	11	001	-	FCVTZU (scalar, fixed-point) - Half-precision to 32-bit variant	FEAT_FP16
1	0	00	00	010	-	SCVTF (scalar, fixed-point) - 64-bit to single-precision variant	-
1	0	00	00	011	-	UCVTF (scalar, fixed-point) - 64-bit to single-precision variant	-
1	0	00	11	000	-	FCVTZS (scalar, fixed-point) - Single-precision to 64-bit variant	-
1	0	00	11	001	-	FCVTZU (scalar, fixed-point) - Single-precision to 64-bit variant	-
1	0	01	00	010	-	SCVTF (scalar, fixed-point) - 64-bit to double-precision variant	-
1	0	01	00	011	-	UCVTF (scalar, fixed-point) - 64-bit to double-precision variant	-
1	0	01	11	000	-	FCVTZS (scalar, fixed-point) - Double-precision to 64-bit variant	-
1	0	01	11	001	-	FCVTZU (scalar, fixed-point) - Double-precision to 64-bit variant	-
1	0	11	00	010	-	SCVTF (scalar, fixed-point) - 64-bit to half-precision variant	FEAT_FP16
1	0	11	00	011	-	UCVTF (scalar, fixed-point) - 64-bit to half-precision variant	FEAT_FP16
1	0	11	11	000	-	FCVTZS (scalar, fixed-point) - Half-precision to 64-bit variant	FEAT_FP16
1	0	11	11	001	-	FCVTZU (scalar, fixed-point) - Half-precision to 64-bit variant	FEAT_FP16

Conversion between floating-point and integer

This section describes the encoding of the Conversion between floating-point and integer instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.



Decode fields					Instruction page	Feature
sf	S	ptype	rmode	opcode		
-	-	-	x1	01x	Unallocated.	-
-	-	-	x1	10x	Unallocated.	-
-	-	-	1x	01x	Unallocated.	-
-	-	-	1x	10x	Unallocated.	-
-	0	10	-	0xx	Unallocated.	-
-	0	10	-	10x	Unallocated.	-
-	1	-	-	-	Unallocated.	-
0	0	00	x1	11x	Unallocated.	-
0	0	00	00	000	FCVTNS (scalar) - Single-precision to 32-bit variant	-
0	0	00	00	001	FCVTNU (scalar) - Single-precision to 32-bit variant	-
0	0	00	00	010	SCVTF (scalar, integer) - 32-bit to single-precision variant	-
0	0	00	00	011	UCVTF (scalar, integer) - 32-bit to single-precision variant	-
0	0	00	00	100	FCVTAS (scalar) - Single-precision to 32-bit variant	-
0	0	00	00	101	FCVTAU (scalar) - Single-precision to 32-bit variant	-
0	0	00	00	110	FMOV (general) - Single-precision to 32-bit variant	-
0	0	00	00	111	FMOV (general) - 32-bit to single-precision variant	-
0	0	00	01	000	FCVTPS (scalar) - Single-precision to 32-bit variant	-
0	0	00	01	001	FCVTPU (scalar) - Single-precision to 32-bit variant	-
0	0	00	1x	11x	Unallocated.	-
0	0	00	10	000	FCVTMS (scalar) - Single-precision to 32-bit variant	-
0	0	00	10	001	FCVTMU (scalar) - Single-precision to 32-bit variant	-
0	0	00	11	000	FCVTZS (scalar, integer) - Single-precision to 32-bit variant	-
0	0	00	11	001	FCVTZU (scalar, integer) - Single-precision to 32-bit variant	-
0	0	01	0x	11x	Unallocated.	-
0	0	01	00	000	FCVTNS (scalar) - Double-precision to 32-bit variant	-
0	0	01	00	001	FCVTNU (scalar) - Double-precision to 32-bit variant	-
0	0	01	00	010	SCVTF (scalar, integer) - 32-bit to double-precision variant	-
0	0	01	00	011	UCVTF (scalar, integer) - 32-bit to double-precision variant	-

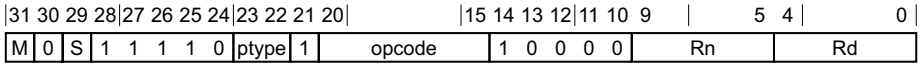
Decode fields					Instruction page	Feature
sf	S	ptype	rmode	opcode		
0	0	01	00	100	FCVTAS (scalar) - Double-precision to 32-bit variant	-
0	0	01	00	101	FCVTAU (scalar) - Double-precision to 32-bit variant	-
0	0	01	01	000	FCVTPS (scalar) - Double-precision to 32-bit variant	-
0	0	01	01	001	FCVTPU (scalar) - Double-precision to 32-bit variant	-
0	0	01	10	000	FCVTMS (scalar) - Double-precision to 32-bit variant	-
0	0	01	10	001	FCVTMU (scalar) - Double-precision to 32-bit variant	-
0	0	01	10	11x	Unallocated.	-
0	0	01	11	000	FCVTZS (scalar, integer) - Double-precision to 32-bit variant	-
0	0	01	11	001	FCVTZU (scalar, integer) - Double-precision to 32-bit variant	-
0	0	01	11	110	FJCVTZS	FEAT_JSCVT
0	0	01	11	111	Unallocated.	-
0	0	10	-	11x	Unallocated.	-
0	0	11	00	000	FCVTNS (scalar) - Half-precision to 32-bit variant	FEAT_FP16
0	0	11	00	001	FCVTNU (scalar) - Half-precision to 32-bit variant	FEAT_FP16
0	0	11	00	010	SCVTF (scalar, integer) - 32-bit to half-precision variant	FEAT_FP16
0	0	11	00	011	UCVTF (scalar, integer) - 32-bit to half-precision variant	FEAT_FP16
0	0	11	00	100	FCVTAS (scalar) - Half-precision to 32-bit variant	FEAT_FP16
0	0	11	00	101	FCVTAU (scalar) - Half-precision to 32-bit variant	FEAT_FP16
0	0	11	00	110	FMOV (general) - Half-precision to 32-bit variant	FEAT_FP16
0	0	11	00	111	FMOV (general) - 32-bit to half-precision variant	FEAT_FP16
0	0	11	01	000	FCVTPS (scalar) - Half-precision to 32-bit variant	FEAT_FP16
0	0	11	01	001	FCVTPU (scalar) - Half-precision to 32-bit variant	FEAT_FP16
0	0	11	10	000	FCVTMS (scalar) - Half-precision to 32-bit variant	FEAT_FP16
0	0	11	10	001	FCVTMU (scalar) - Half-precision to 32-bit variant	FEAT_FP16
0	0	11	11	000	FCVTZS (scalar, integer) - Half-precision to 32-bit variant	FEAT_FP16
0	0	11	11	001	FCVTZU (scalar, integer) - Half-precision to 32-bit variant	FEAT_FP16
1	0	00	-	11x	Unallocated.	-
1	0	00	00	000	FCVTNS (scalar) - Single-precision to 64-bit variant	-
1	0	00	00	001	FCVTNU (scalar) - Single-precision to 64-bit variant	-
1	0	00	00	010	SCVTF (scalar, integer) - 64-bit to single-precision variant	-
1	0	00	00	011	UCVTF (scalar, integer) - 64-bit to single-precision variant	-
1	0	00	00	100	FCVTAS (scalar) - Single-precision to 64-bit variant	-

Decode fields					Instruction page	Feature
sf	S	ptype	rmode	opcode		
1	0	00	00	101	FCVTAU (scalar) - Single-precision to 64-bit variant	-
1	0	00	01	000	FCVTPS (scalar) - Single-precision to 64-bit variant	-
1	0	00	01	001	FCVTPU (scalar) - Single-precision to 64-bit variant	-
1	0	00	10	000	FCVTMS (scalar) - Single-precision to 64-bit variant	-
1	0	00	10	001	FCVTMU (scalar) - Single-precision to 64-bit variant	-
1	0	00	11	000	FCVTZS (scalar, integer) - Single-precision to 64-bit variant	-
1	0	00	11	001	FCVTZU (scalar, integer) - Single-precision to 64-bit variant	-
1	0	01	x1	11x	Unallocated.	-
1	0	01	00	000	FCVTNS (scalar) - Double-precision to 64-bit variant	-
1	0	01	00	001	FCVTNU (scalar) - Double-precision to 64-bit variant	-
1	0	01	00	010	SCVTF (scalar, integer) - 64-bit to double-precision variant	-
1	0	01	00	011	UCVTF (scalar, integer) - 64-bit to double-precision variant	-
1	0	01	00	100	FCVTAS (scalar) - Double-precision to 64-bit variant	-
1	0	01	00	101	FCVTAU (scalar) - Double-precision to 64-bit variant	-
1	0	01	00	110	FMOV (general) - Double-precision to 64-bit variant	-
1	0	01	00	111	FMOV (general) - 64-bit to double-precision variant	-
1	0	01	01	000	FCVTPS (scalar) - Double-precision to 64-bit variant	-
1	0	01	01	001	FCVTPU (scalar) - Double-precision to 64-bit variant	-
1	0	01	1x	11x	Unallocated.	-
1	0	01	10	000	FCVTMS (scalar) - Double-precision to 64-bit variant	-
1	0	01	10	001	FCVTMU (scalar) - Double-precision to 64-bit variant	-
1	0	01	11	000	FCVTZS (scalar, integer) - Double-precision to 64-bit variant	-
1	0	01	11	001	FCVTZU (scalar, integer) - Double-precision to 64-bit variant	-
1	0	10	x0	11x	Unallocated.	-
1	0	10	01	110	FMOV (general) - Top half of 128-bit to 64-bit variant	-
1	0	10	01	111	FMOV (general) - 64-bit to top half of 128-bit variant	-
1	0	10	1x	11x	Unallocated.	-
1	0	11	00	000	FCVTNS (scalar) - Half-precision to 64-bit variant	FEAT_FP16
1	0	11	00	001	FCVTNU (scalar) - Half-precision to 64-bit variant	FEAT_FP16
1	0	11	00	010	SCVTF (scalar, integer) - 64-bit to half-precision variant	FEAT_FP16
1	0	11	00	011	UCVTF (scalar, integer) - 64-bit to half-precision variant	FEAT_FP16
1	0	11	00	100	FCVTAS (scalar) - Half-precision to 64-bit variant	FEAT_FP16

Decode fields					Instruction page	Feature
sf	S	ptype	rmode	opcode		
1	0	11	00	101	FCVTAU (scalar) - Half-precision to 64-bit variant	FEAT_FP16
1	0	11	00	110	FMOV (general) - Half-precision to 64-bit variant	FEAT_FP16
1	0	11	00	111	FMOV (general) - 64-bit to half-precision variant	FEAT_FP16
1	0	11	01	000	FCVTPS (scalar) - Half-precision to 64-bit variant	FEAT_FP16
1	0	11	01	001	FCVTPU (scalar) - Half-precision to 64-bit variant	FEAT_FP16
1	0	11	10	000	FCVTMS (scalar) - Half-precision to 64-bit variant	FEAT_FP16
1	0	11	10	001	FCVTMU (scalar) - Half-precision to 64-bit variant	FEAT_FP16
1	0	11	11	000	FCVTZS (scalar, integer) - Half-precision to 64-bit variant	FEAT_FP16
1	0	11	11	001	FCVTZU (scalar, integer) - Half-precision to 64-bit variant	FEAT_FP16

Floating-point data-processing (1 source)

This section describes the encoding of the Floating-point data-processing (1 source) instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.



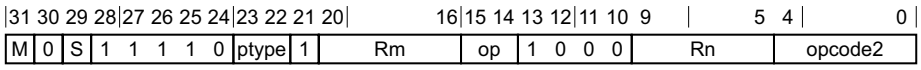
Decode fields				Instruction page	Feature
M	S	ptype	opcode		
-	-	-	1xxxxx	Unallocated.	-
-	1	-	-	Unallocated.	-
0	0	00	000000	FMOV (register) - Single-precision variant	-
0	0	00	000001	FABS (scalar) - Single-precision variant	-
0	0	00	000010	FNEG (scalar) - Single-precision variant	-
0	0	00	000011	FSQRT (scalar) - Single-precision variant	-
0	0	00	000100	Unallocated.	-
0	0	00	000101	FCVT - Single-precision to double-precision variant	-
0	0	00	000110	Unallocated.	-
0	0	00	000111	FCVT - Single-precision to half-precision variant	-
0	0	00	001000	FRINTN (scalar) - Single-precision variant	-
0	0	00	001001	FRINTP (scalar) - Single-precision variant	-
0	0	00	001010	FRINTM (scalar) - Single-precision variant	-

Decode fields				Instruction page	Feature
M	S	ptype	opcode		
0	0	00	001011	FRINTZ (scalar) - Single-precision variant	-
0	0	00	001100	FRINTA (scalar) - Single-precision variant	-
0	0	00	001101	Unallocated.	-
0	0	00	001110	FRINTX (scalar) - Single-precision variant	-
0	0	00	001111	FRINTI (scalar) - Single-precision variant	-
0	0	00	010000	FRINT32Z (scalar) - Single-precision variant	FEAT_FRINTTS
0	0	00	010001	FRINT32X (scalar) - Single-precision variant	FEAT_FRINTTS
0	0	00	010010	FRINT64Z (scalar) - Single-precision variant	FEAT_FRINTTS
0	0	00	010011	FRINT64X (scalar) - Single-precision variant	FEAT_FRINTTS
0	0	00	0101xx	Unallocated.	-
0	0	00	011xxx	Unallocated.	-
0	0	01	000000	FMOV (register) - Double-precision variant	-
0	0	01	000001	FABS (scalar) - Double-precision variant	-
0	0	01	000010	FNEG (scalar) - Double-precision variant	-
0	0	01	000011	FSQRT (scalar) - Double-precision variant	-
0	0	01	000100	FCVT - Double-precision to single-precision variant	-
0	0	01	000101	Unallocated.	-
0	0	01	000110	BFCVT	FEAT_BF16
0	0	01	000111	FCVT - Double-precision to half-precision variant	-
0	0	01	001000	FRINTN (scalar) - Double-precision variant	-
0	0	01	001001	FRINTP (scalar) - Double-precision variant	-
0	0	01	001010	FRINTM (scalar) - Double-precision variant	-
0	0	01	001011	FRINTZ (scalar) - Double-precision variant	-
0	0	01	001100	FRINTA (scalar) - Double-precision variant	-
0	0	01	001101	Unallocated.	-
0	0	01	001110	FRINTX (scalar) - Double-precision variant	-
0	0	01	001111	FRINTI (scalar) - Double-precision variant	-
0	0	01	010000	FRINT32Z (scalar) - Double-precision variant	FEAT_FRINTTS
0	0	01	010001	FRINT32X (scalar) - Double-precision variant	FEAT_FRINTTS
0	0	01	010010	FRINT64Z (scalar) - Double-precision variant	FEAT_FRINTTS
0	0	01	010011	FRINT64X (scalar) - Double-precision variant	FEAT_FRINTTS
0	0	01	0101xx	Unallocated.	-

Decode fields				Instruction page	Feature
M	S	ptype	opcode		
0	0	01	011xxx	Unallocated.	-
0	0	10	0xxxxx	Unallocated.	-
0	0	11	000000	FMOV (register) - Half-precision variant	FEAT_FP16
0	0	11	000001	FABS (scalar) - Half-precision variant	FEAT_FP16
0	0	11	000010	FNEG (scalar) - Half-precision variant	FEAT_FP16
0	0	11	000011	FSQRT (scalar) - Half-precision variant	FEAT_FP16
0	0	11	000100	FCVT - Half-precision to single-precision variant	-
0	0	11	000101	FCVT - Half-precision to double-precision variant	-
0	0	11	00011x	Unallocated.	-
0	0	11	001000	FRINTN (scalar) - Half-precision variant	FEAT_FP16
0	0	11	001001	FRINTP (scalar) - Half-precision variant	FEAT_FP16
0	0	11	001010	FRINTM (scalar) - Half-precision variant	FEAT_FP16
0	0	11	001011	FRINTZ (scalar) - Half-precision variant	FEAT_FP16
0	0	11	001100	FRINTA (scalar) - Half-precision variant	FEAT_FP16
0	0	11	001101	Unallocated.	-
0	0	11	001110	FRINTX (scalar) - Half-precision variant	FEAT_FP16
0	0	11	001111	FRINTI (scalar) - Half-precision variant	FEAT_FP16
0	0	11	01xxxx	Unallocated.	-
1	-	-	-	Unallocated.	-

Floating-point compare

This section describes the encoding of the Floating-point compare instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.

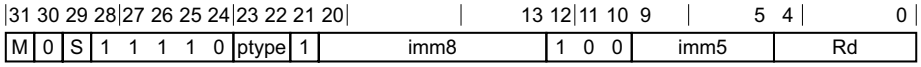


Decode fields					Instruction page	Feature
M	S	ptype	op	opcode2		
-	-	-	-	xxxx1	Unallocated.	-
-	-	-	-	xxx1x	Unallocated.	-
-	-	-	-	xx1xx	Unallocated.	-
-	-	-	x1	-	Unallocated.	-

Decode fields					Instruction page	Feature
M	S	ptype	op	opcode2		
-	-	-	1x	-	Unallocated.	-
-	-	10	-	-	Unallocated.	-
-	1	-	-	-	Unallocated.	-
0	0	00	00	00000	FCMP	-
0	0	00	00	01000	FCMP	-
0	0	00	00	10000	FCMPE	-
0	0	00	00	11000	FCMPE	-
0	0	01	00	00000	FCMP	-
0	0	01	00	01000	FCMP	-
0	0	01	00	10000	FCMPE	-
0	0	01	00	11000	FCMPE	-
0	0	11	00	00000	FCMP	FEAT_FP16
0	0	11	00	01000	FCMP	FEAT_FP16
0	0	11	00	10000	FCMPE	FEAT_FP16
0	0	11	00	11000	FCMPE	FEAT_FP16
1	-	-	-	-	Unallocated.	-

Floating-point immediate

This section describes the encoding of the Floating-point immediate instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.

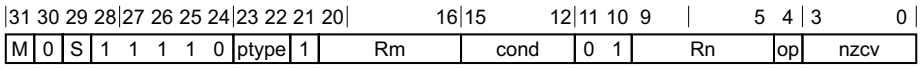


Decode fields				Instruction page	Feature
M	S	ptype	imm5		
-	-	-	xxxx1	Unallocated.	-
-	-	-	xxx1x	Unallocated.	-
-	-	-	xx1xx	Unallocated.	-
-	-	-	x1xxx	Unallocated.	-
-	-	-	1xxxx	Unallocated.	-
-	-	10	-	Unallocated.	-
-	1	-	-	Unallocated.	-

Decode fields				Instruction page	Feature
M	S	ptype	imm5		
0	0	00	00000	FMOV (scalar, immediate) - Single-precision variant	-
0	0	01	00000	FMOV (scalar, immediate) - Double-precision variant	-
0	0	11	00000	FMOV (scalar, immediate) - Half-precision variant	FEAT_FP16
1	-	-	-	Unallocated.	-

Floating-point conditional compare

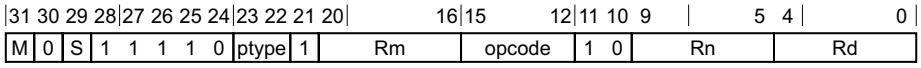
This section describes the encoding of the Floating-point conditional compare instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.



Decode fields				Instruction page	Feature
M	S	ptype	op		
-	-	10	-	Unallocated.	-
-	1	-	-	Unallocated.	-
0	0	00	0	FCCMP - Single-precision variant	-
0	0	00	1	FCCMPE - Single-precision variant	-
0	0	01	0	FCCMP - Double-precision variant	-
0	0	01	1	FCCMPE - Double-precision variant	-
0	0	11	0	FCCMP - Half-precision variant	FEAT_FP16
0	0	11	1	FCCMPE - Half-precision variant	FEAT_FP16
1	-	-	-	Unallocated.	-

Floating-point data-processing (2 source)

This section describes the encoding of the Floating-point data-processing (2 source) instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.

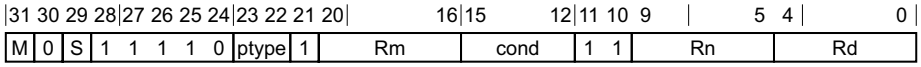


Decode fields				Instruction page	Feature
M	S	ptype	opcode		
-	-	-	1xx1	Unallocated.	-
-	-	-	1x1x	Unallocated.	-
-	-	-	11xx	Unallocated.	-
-	-	10	-	Unallocated.	-
-	1	-	-	Unallocated.	-
0	0	00	0000	FMUL (scalar) - Single-precision variant	-
0	0	00	0001	FDIV (scalar) - Single-precision variant	-
0	0	00	0010	FADD (scalar) - Single-precision variant	-
0	0	00	0011	FSUB (scalar) - Single-precision variant	-
0	0	00	0100	FMAX (scalar) - Single-precision variant	-
0	0	00	0101	FMIN (scalar) - Single-precision variant	-
0	0	00	0110	FMAXNM (scalar) - Single-precision variant	-
0	0	00	0111	FMINNM (scalar) - Single-precision variant	-
0	0	00	1000	FNMUL (scalar) - Single-precision variant	-
0	0	01	0000	FMUL (scalar) - Double-precision variant	-
0	0	01	0001	FDIV (scalar) - Double-precision variant	-
0	0	01	0010	FADD (scalar) - Double-precision variant	-
0	0	01	0011	FSUB (scalar) - Double-precision variant	-
0	0	01	0100	FMAX (scalar) - Double-precision variant	-
0	0	01	0101	FMIN (scalar) - Double-precision variant	-
0	0	01	0110	FMAXNM (scalar) - Double-precision variant	-
0	0	01	0111	FMINNM (scalar) - Double-precision variant	-
0	0	01	1000	FNMUL (scalar) - Double-precision variant	-
0	0	11	0000	FMUL (scalar) - Half-precision variant	FEAT_FP16
0	0	11	0001	FDIV (scalar) - Half-precision variant	FEAT_FP16
0	0	11	0010	FADD (scalar) - Half-precision variant	FEAT_FP16
0	0	11	0011	FSUB (scalar) - Half-precision variant	FEAT_FP16
0	0	11	0100	FMAX (scalar) - Half-precision variant	FEAT_FP16

Decode fields				Instruction page	Feature
M	S	ptype	opcode		
0	0	11	0101	FMIN (scalar) - Half-precision variant	FEAT_FP16
0	0	11	0110	FMAXNM (scalar) - Half-precision variant	FEAT_FP16
0	0	11	0111	FMINNM (scalar) - Half-precision variant	FEAT_FP16
0	0	11	1000	FNMUL (scalar) - Half-precision variant	FEAT_FP16
1	-	-	-	Unallocated.	-

Floating-point conditional select

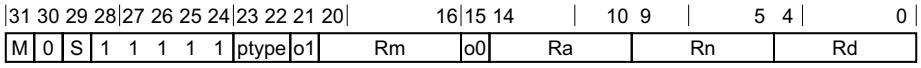
This section describes the encoding of the Floating-point conditional select instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.



Decode fields			Instruction page	Feature
M	S	ptype		
-	-	10	Unallocated.	-
-	1	-	Unallocated.	-
0	0	00	FCSEL - Single-precision variant	-
0	0	01	FCSEL - Double-precision variant	-
0	0	11	FCSEL - Half-precision variant	FEAT_FP16
1	-	-	Unallocated.	-

Floating-point data-processing (3 source)

This section describes the encoding of the Floating-point data-processing (3 source) instruction class. The encodings in this section are decoded from *Data Processing -- Scalar Floating-Point and Advanced SIMD* on page C4-587.



Decode fields					Instruction page	Feature
M	S	ptype	o1	o0		
-	-	10	-	-	Unallocated.	-
-	1	-	-	-	Unallocated.	-
0	0	00	0	0	FMADD - Single-precision variant	-
0	0	00	0	1	FMSUB - Single-precision variant	-
0	0	00	1	0	FNMADD - Single-precision variant	-
0	0	00	1	1	FNMSUB - Single-precision variant	-
0	0	01	0	0	FMADD - Double-precision variant	-
0	0	01	0	1	FMSUB - Double-precision variant	-
0	0	01	1	0	FNMADD - Double-precision variant	-
0	0	01	1	1	FNMSUB - Double-precision variant	-
0	0	11	0	0	FMADD - Half-precision variant	FEAT_FP16
0	0	11	0	1	FMSUB - Half-precision variant	FEAT_FP16
0	0	11	1	0	FNMADD - Half-precision variant	FEAT_FP16
0	0	11	1	1	FNMSUB - Half-precision variant	FEAT_FP16
1	-	-	-	-	Unallocated.	-