Ryerson University

Department of Electrical, Computer, & Biomedical Engineering
Faculty of Engineering & Architectural Science

Course Title:	Low-Power Digital Integrated Circuits
Course Number:	ELE 734
Semester/Year (e.g.F2016)	F2022

Instructor:	Dr. Andy Ye

Assignment/Lab Number:	3
Assignment/Lab Title:	CMOS Logic Families

Submission Date:	November 15, 2022
Due Date:	November 16, 2022

Student LAST Name	Student FIRST Name	Student Number	Section	Signature*
Youssef	Helana	500766171	1	H.Y.

*By signing above you attest that you have contributed to this written lab report and confirm that all work you have contributed to this lab report is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a "0" on the work, an "F" in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at: http://www.ryerson.ca/senate/current/pol60.pdf

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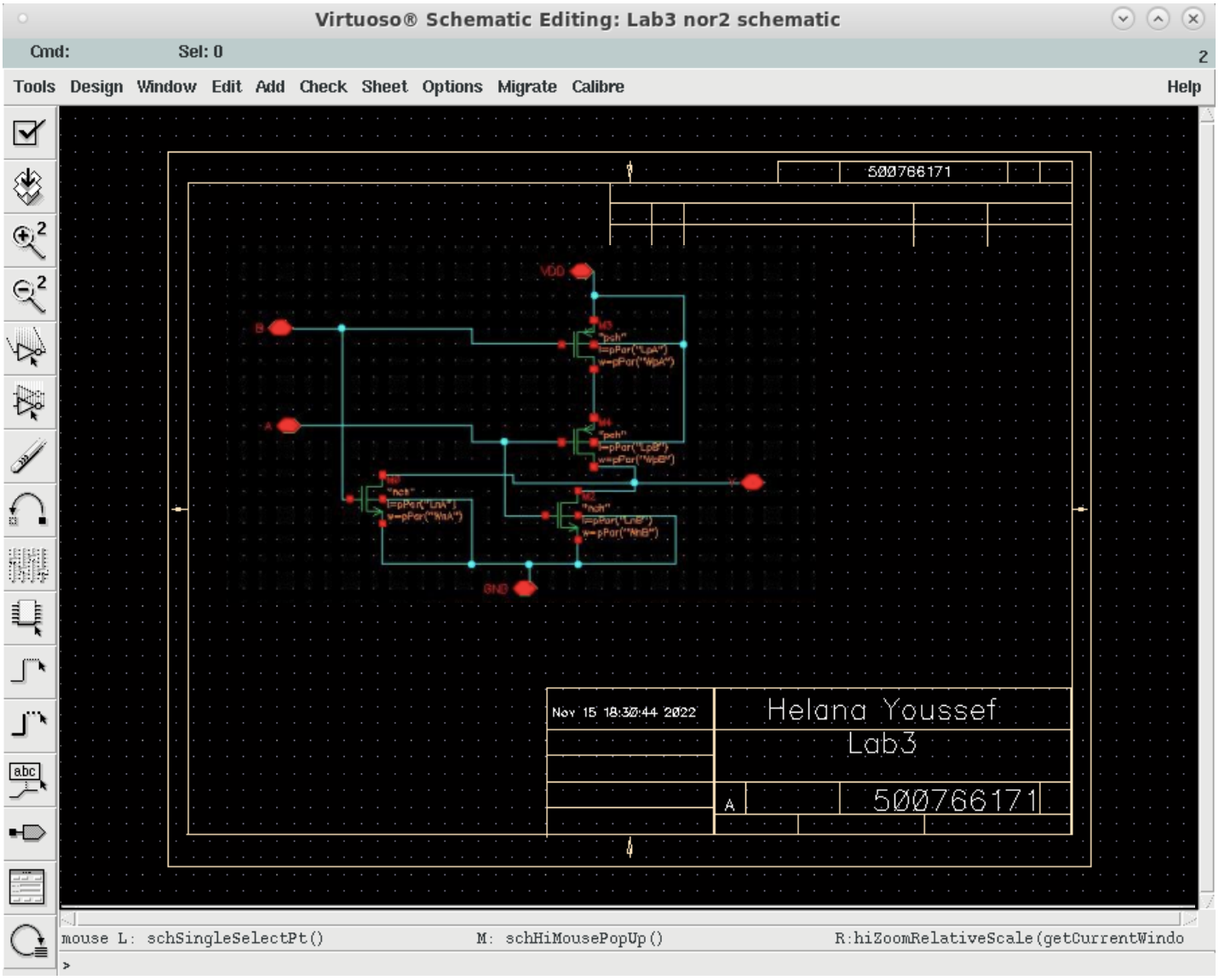
Introduction:

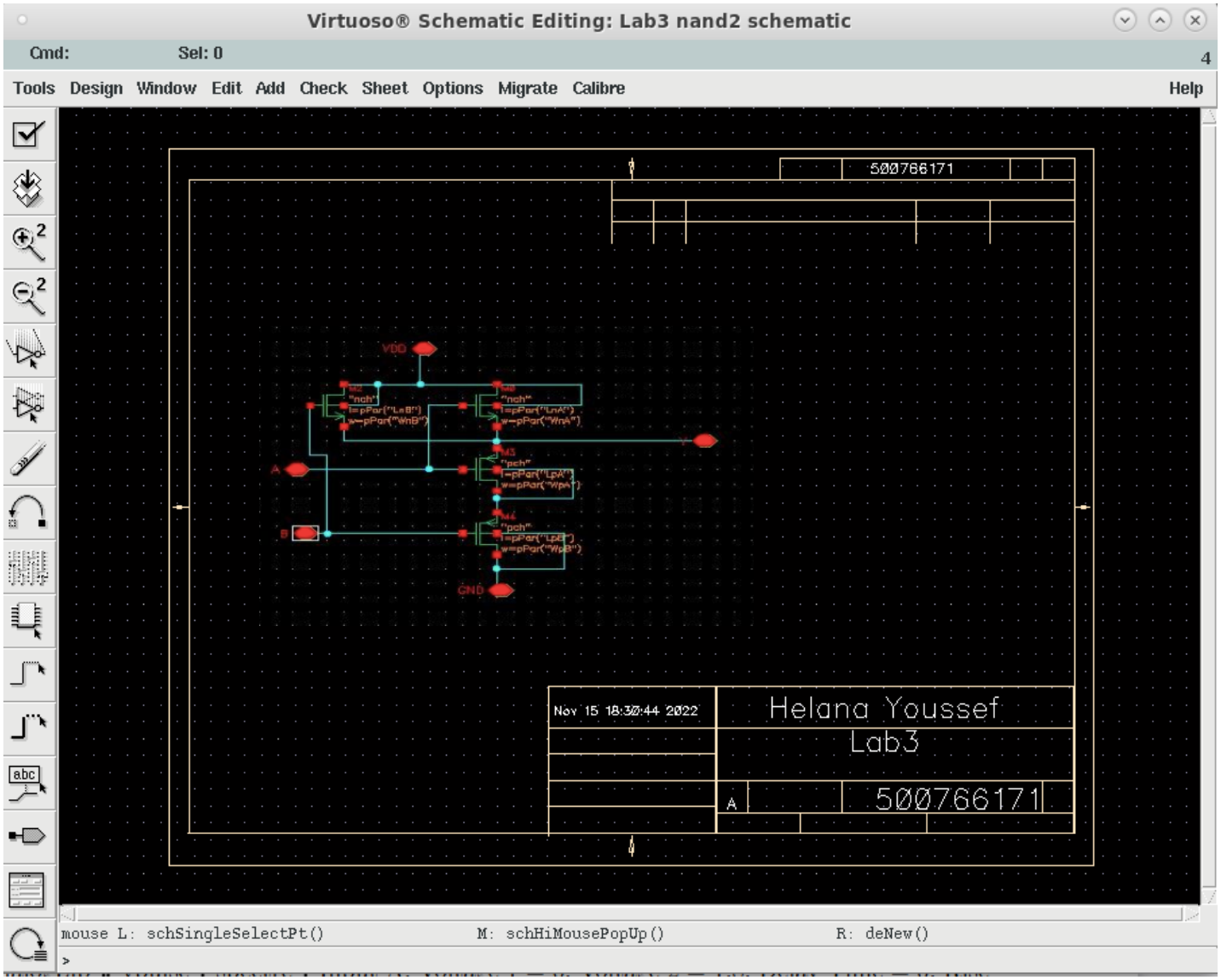
Investigating the dynamic behavior of unskewed, high-skewed, and low-skewed NOR2 and NAND2 gates is the goal of the lab. The same circuit design as static CMOS gates are used by skewed logic gates; however, one transition is favoured over the other due to the ratio between NMOS and PMOS. A high-skewed gate favors a rising transition over a falling transition, and vice versa.

Schematic of the NOR2 and NAND2 gates:

NOR2:

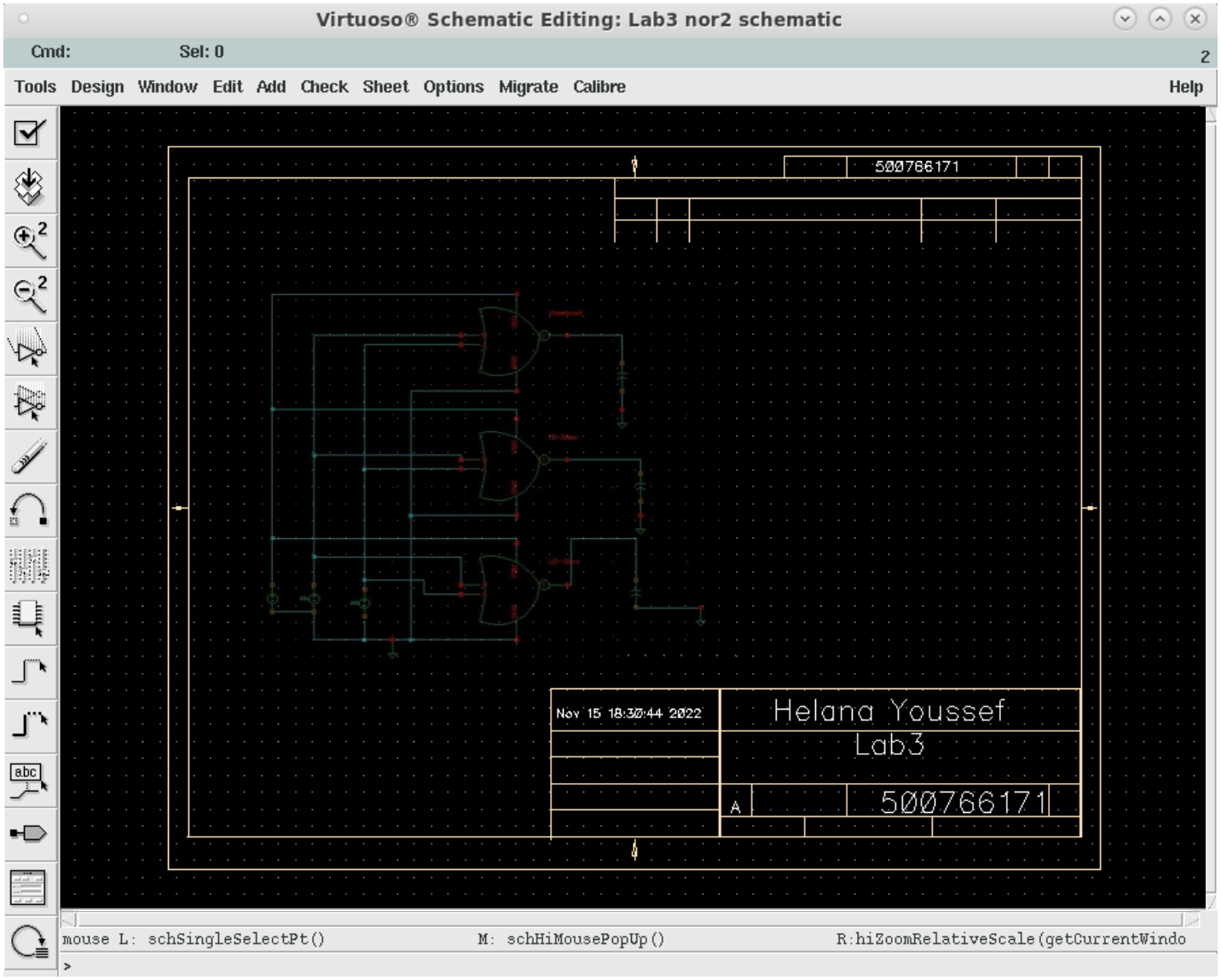


NAND2:

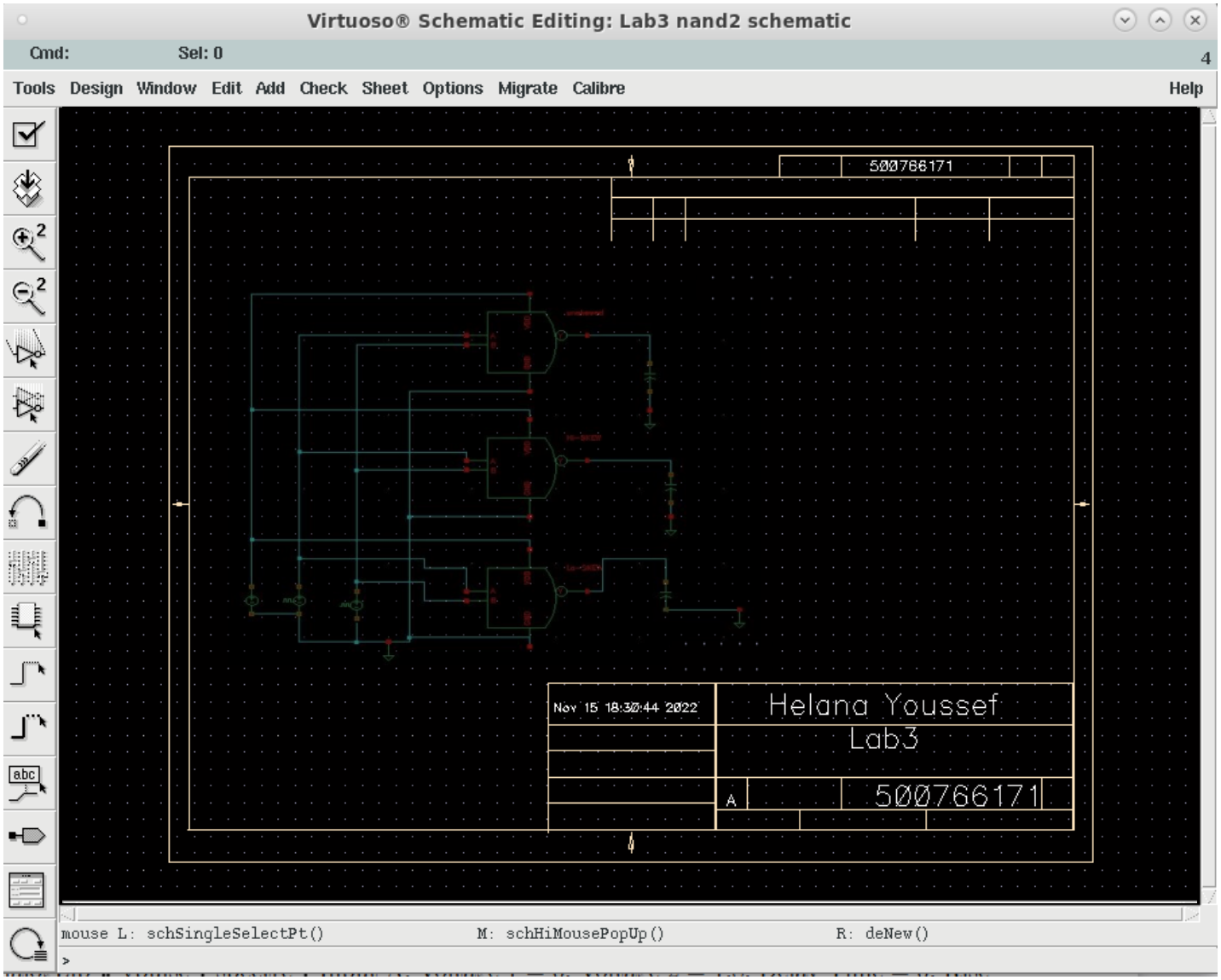

Virtuoso® Schematic Editing: Lab3 nand2 schematic
Cmd:
Sel: 0
Tools Design Window Edit Add Check Sheet Options Migrate Calibre Help
500766171
VDD
GND
A
B
M1
"nch"
l=pPar("LnB")
w=pPar("WnB")
M2
"nch"
l=pPar("LnA")
w=pPar("WnA")
M3
"pch"
l=pPar("LpA")
w=pPar("WpA")
M4
"pch"
l=pPar("LpB")
w=pPar("WpB")
Nov 15 18:30:44 2022
Helana Youssef
Lab3
A
500766171
mouse L: schSingleSelectPt()
M: schHiMousePopUp()
R: deNew()

Schematic of the textbench for the NOR2 and NAND2 gates:

NOR2 Textbench:

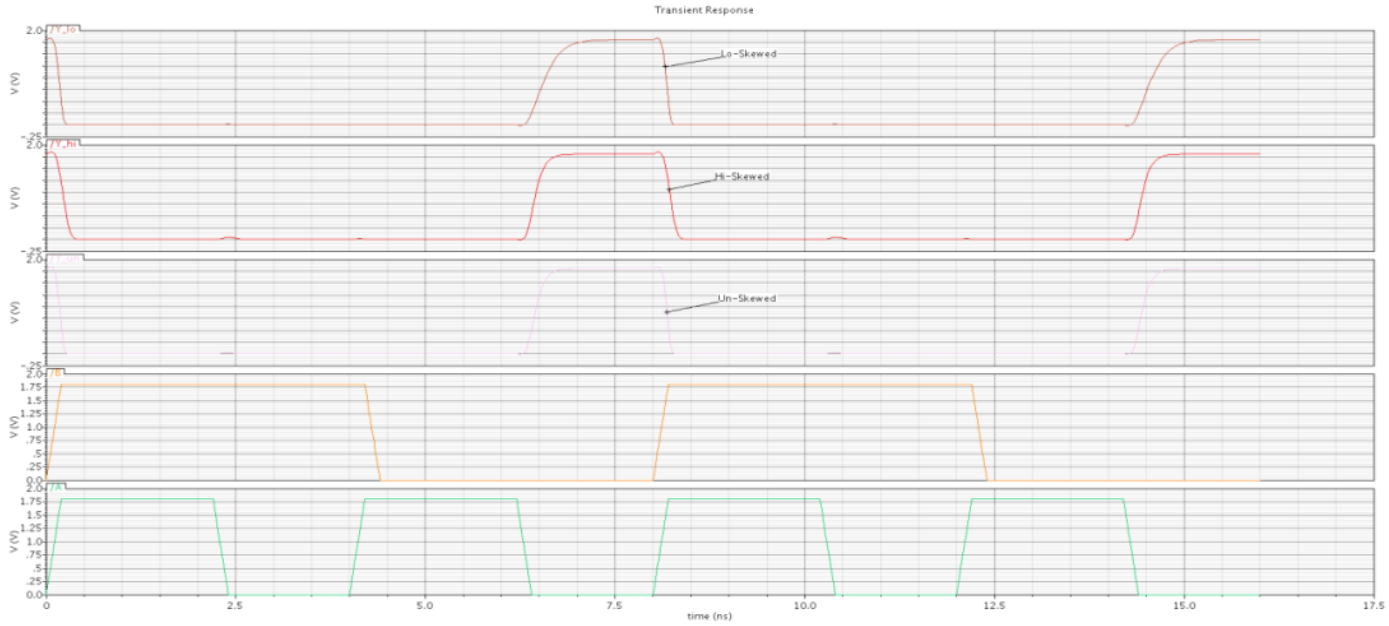


NAND2 Textbench:



Delay measurement for unskewed, high-skewed and low-skewed NOR2 and NAND2 gates:

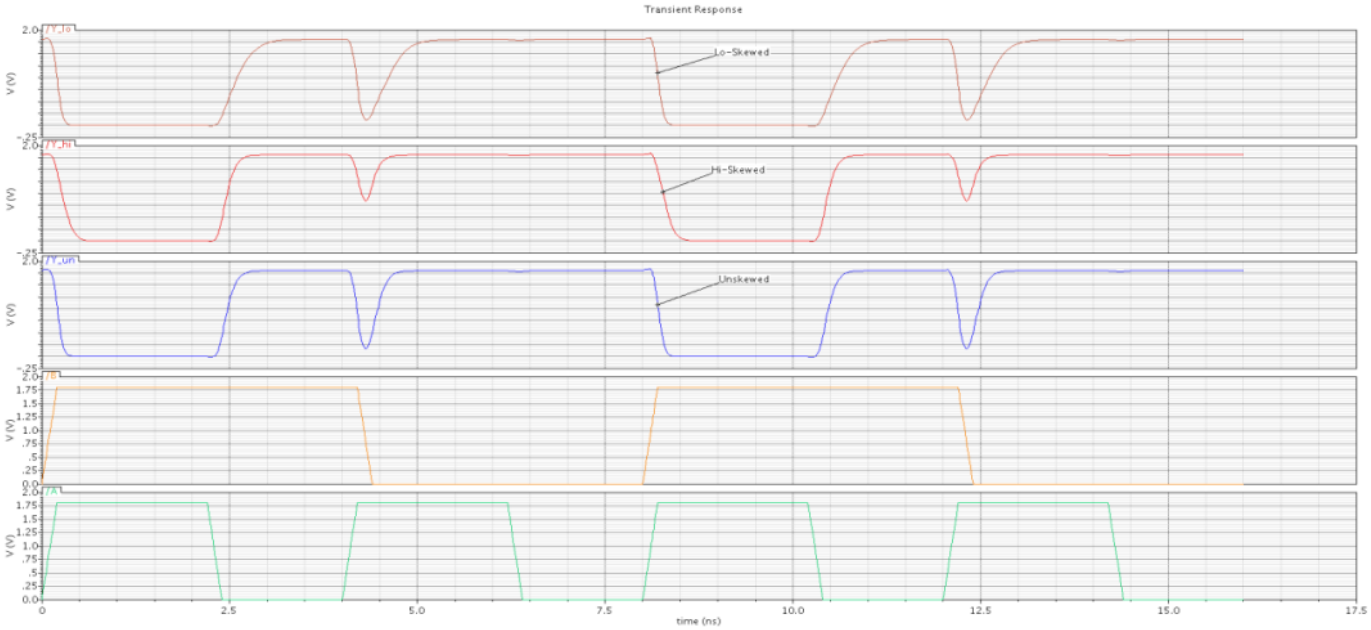
NOR2 Measurement of Unskewed, High-Skewed, and Low-Skewed:



NOR2 Overall Propagation Delay for Unskewed, High-Skewed, and Low-Skewed:

	Output Rising Delay	Output Falling Delay
Unskewed	4.145nF	83.82pF
High-Skewed	4.141nF	127.1pF
Low-Skewed	4.251nF	77.58pF

NAND2 Unskewed, High-Skewed, and Low-Skewed Delay Measurement:

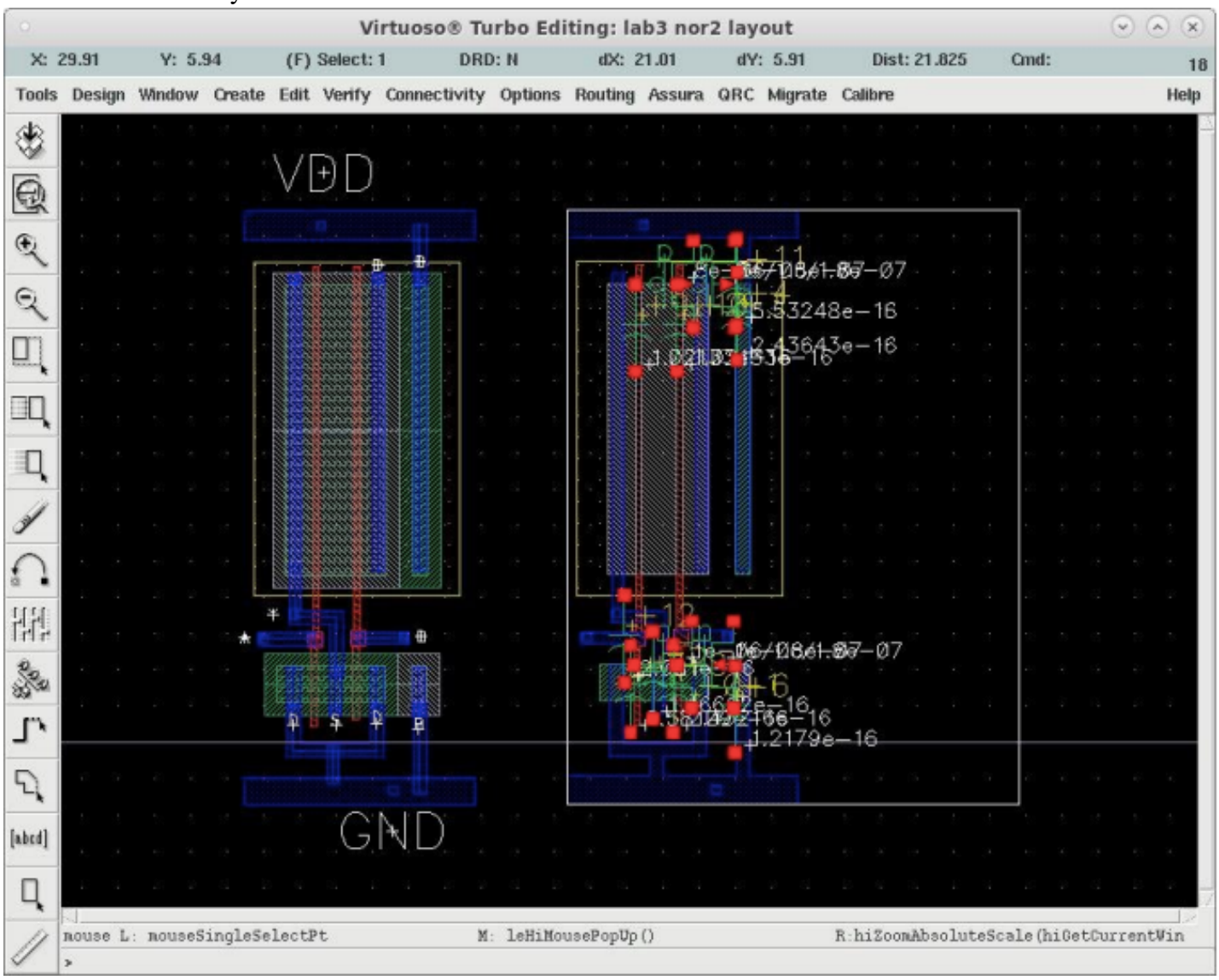


NAND2 Overall Propagation Delay for Unskewed, High-Skewed, and Low-Skewed:

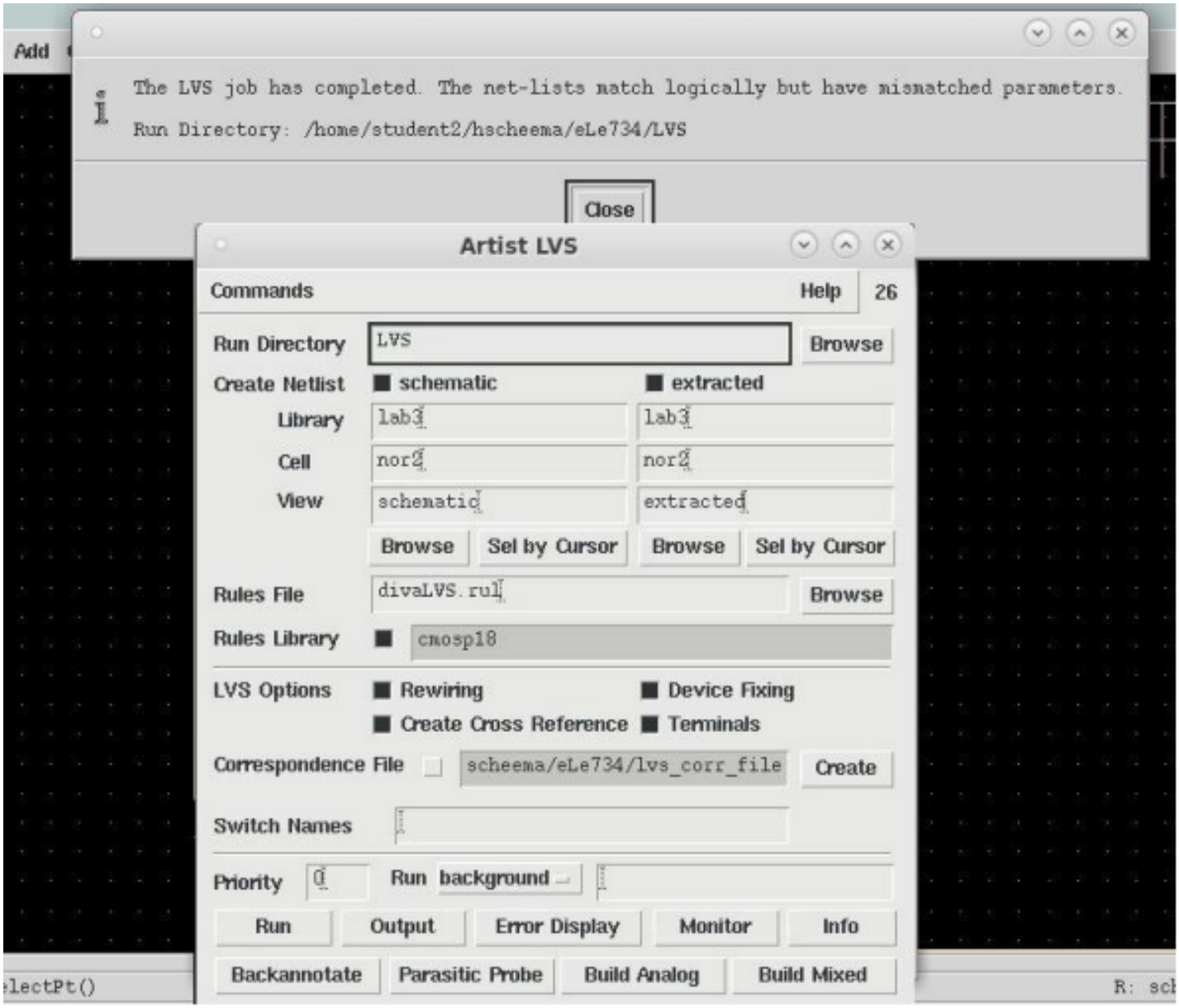
	Output Rising Delay	Output Falling Delay
Unskewed	159pF	114.5pF
High-Skewed	154.3pF	182.4pF
Low-Skewed	275.8pF	109.2pF

The layout and extracted views of the unskewed NOR2 and NAND2 gates:

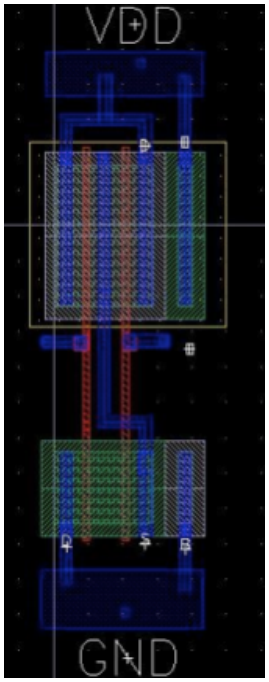
NOR2 Unskewed Layout and Extracted views:

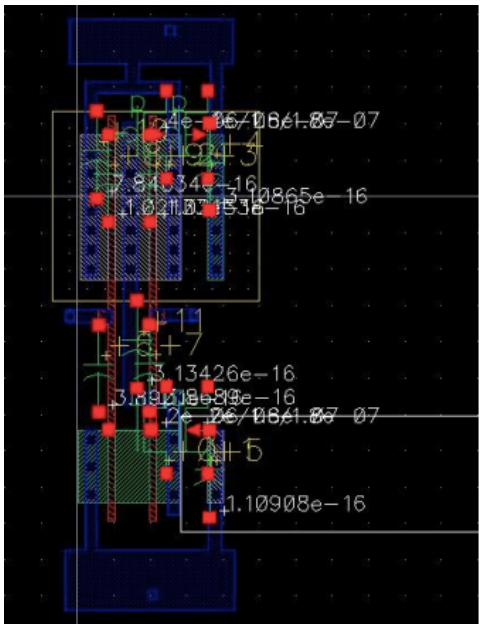


NOR2 LVS:

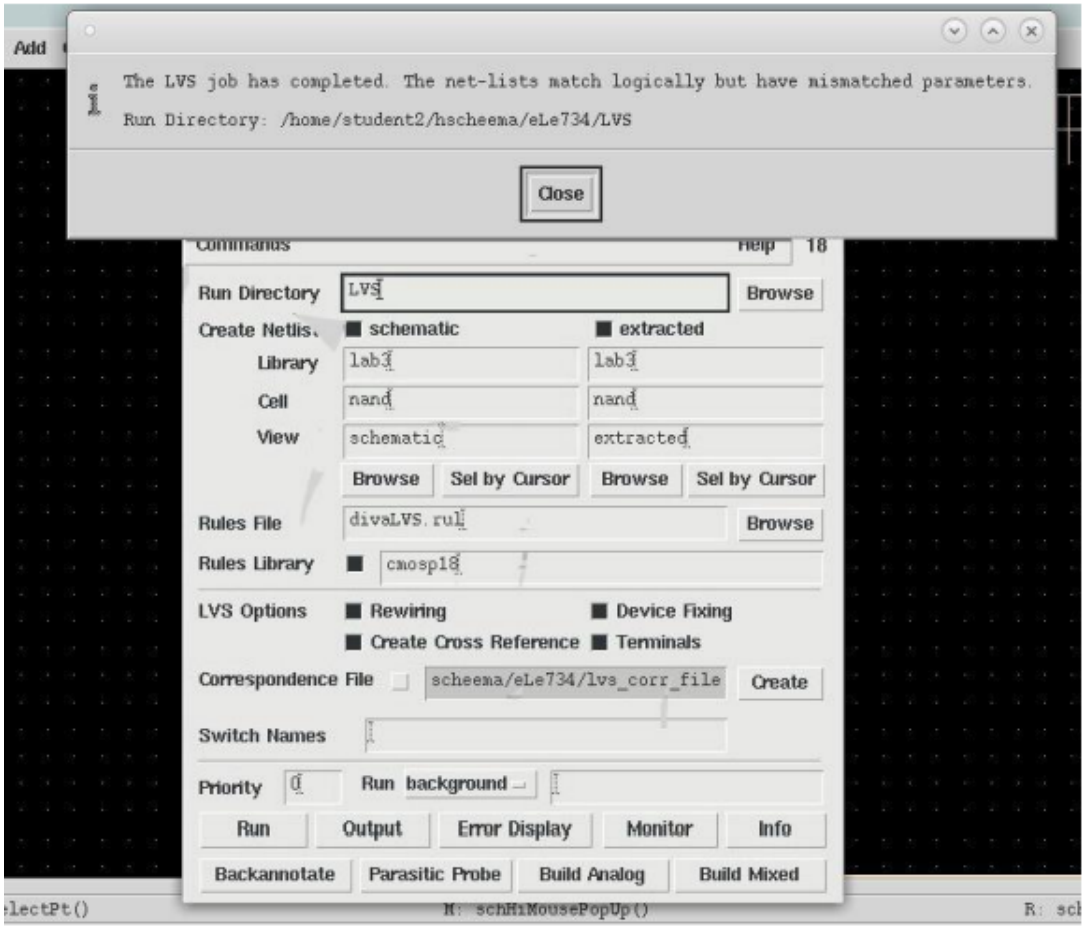

The LVS job has completed. The net-lists match logically but have mismatched parameters.
Run Directory: /home/student2/hscheema/eLe734/LVS
Close
Artist LVS
Commands
Help
26
Run Directory
LVS
Browse
Create Netlist
schematic
extracted
Library
lab3
lab3
Cell
nor2
nor2
View
schematic
extracted
Browse
Sel by Cursor
Browse
Sel by Cursor
Rules File
divaLVS.rul
Browse
Rules Library
cmosp18
LVS Options
Rewiring
Device Fixing
Create Cross Reference
Terminals
Correspondence File
scheema/eLe734/lvs_corr_file
Create
Switch Names
Priority
0
Run
background
Run
Output
Error Display
Monitor
Info
Backannotate
Parasitic Probe
Build Analog
Build Mixed

NAND2 Unskewed Layout and Extracted Views:



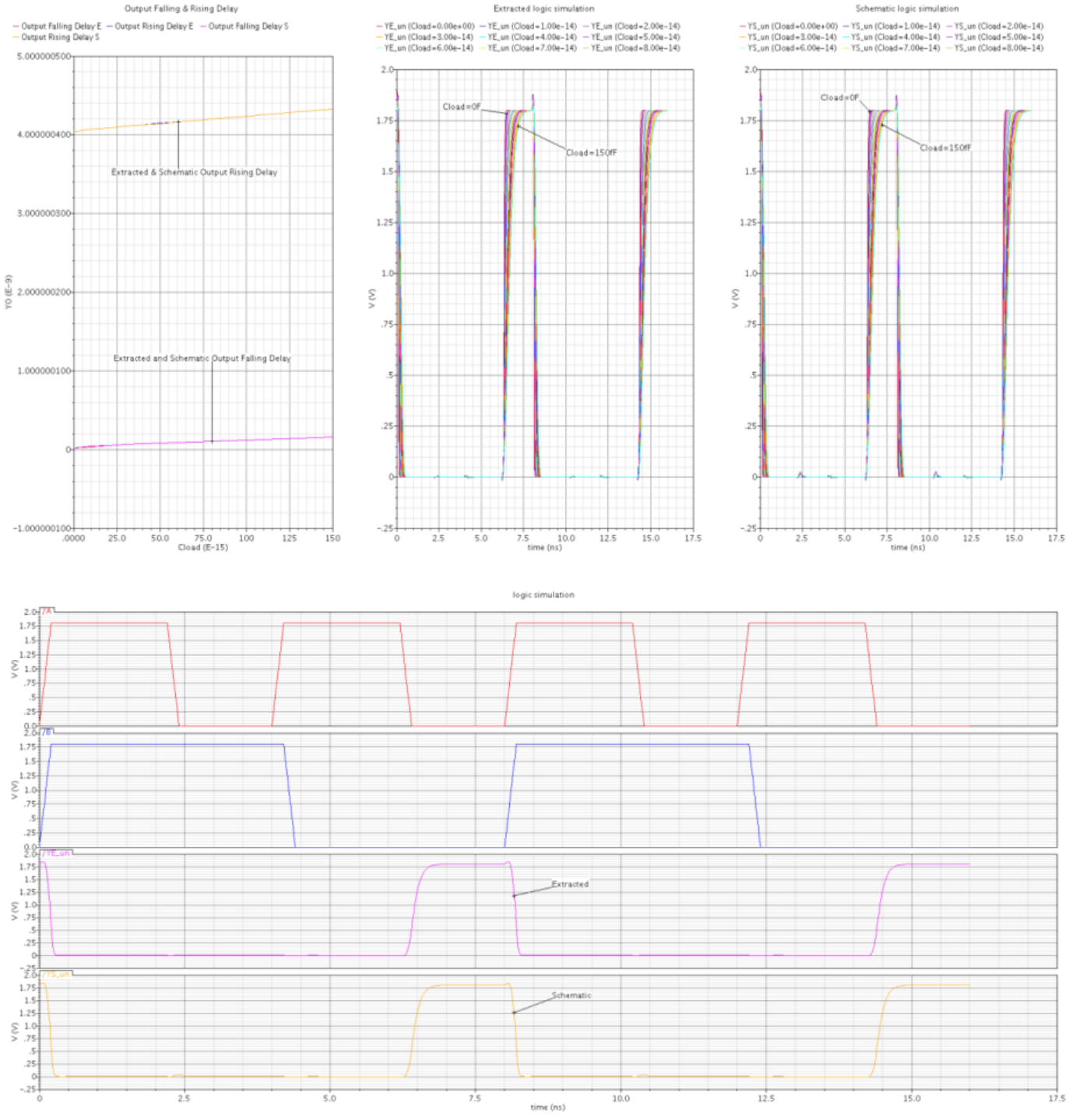


NAND2 LVS:



Post-layout simulation comparing delay measurement for unskewed NAND2 and NOR2 gates:

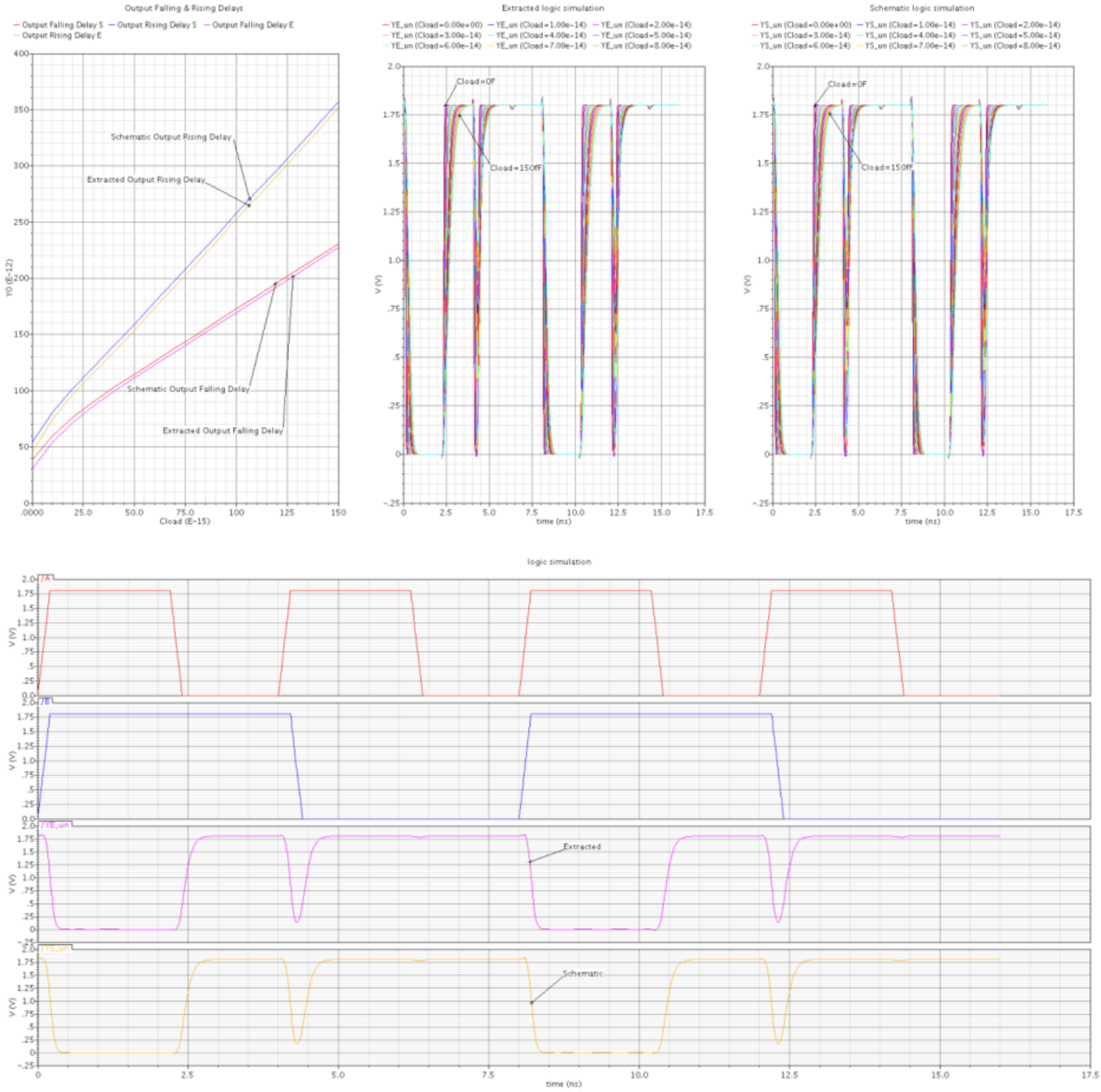
NOR2 post Simulation comparing delay measurements:



NOR2 Overall Propagation Delay for Unskewed (Schematic Vs Extracted):

	Output Rising Delay	Output Falling Delay
Unskewed Schematic	4.145nF	83.77pF
Unskewed Extracted	4.146nF	83.57pF

NAND2 post Simulation comparing delay measurements:



NAND2 Overall Propagation Delay for Unskewed (Schematic Vs Extracted):

	Output Rising Delay	Output Falling Delay
Unskewed Schematic	158.6pF	114.5pF
Unskewed Extracted	153.5pF	111.1pF

Conclusion:

The lab evaluated the dynamic behaviour of the unskewed, high-skewed, and low-skewed NAND2 and NOR2 gates. It is clear from the figures as well as the Tables that the high-skewed gate favours the rising transition over the falling transition and the low-skewed gate favours the rising transition over the falling transition by having the lowest output rising delay. By making the layout for the NOR2 and NAND2 with no skew. The default sizes specified in the CDF parameters are the reason why the netlist matches but the parameters don't. The schematic was then compared to both extracted gates, and they virtually had a perfect match with a close match on both the output falling and rising delays. A parametric analysis was conducted to see how the unskewed gates were affected when the Cload was swept from 0F to 150fF, and by looking at the figures, as Cload increases, the Delay also increases.

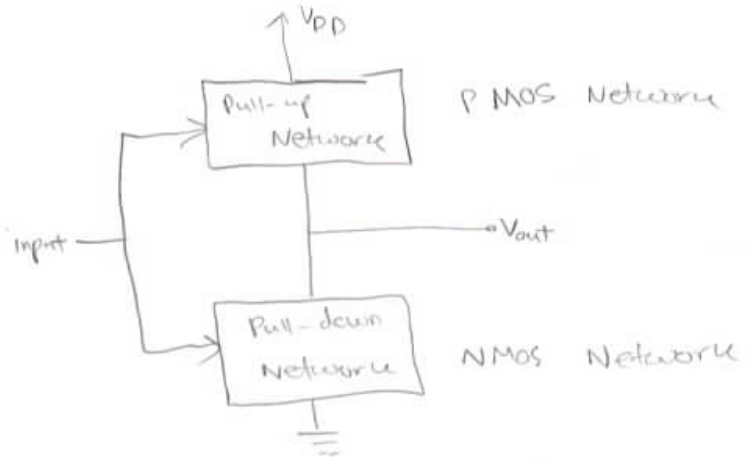
ECE 734 : Pre-Lab 3

1- Normal Skewed : This means that Fall Time (for o/p going from high low) is roughly EQUAL to RISE Time (For o/p going from low to high) for a digital logic gate.

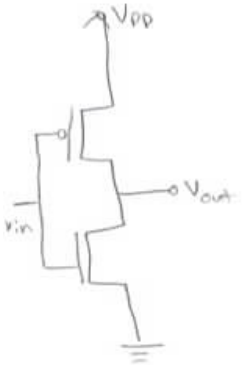
High Skewed : This means that FALL TIME (for o/p going from high to low) is greater than to the rise time (for o/p going from low to high) for a digital logic gate.

Low Skewed : This means that FALL TIME (for o/p going from high to low) is less than to the rise time (for o/p going from low to high) for a digital logic gate.

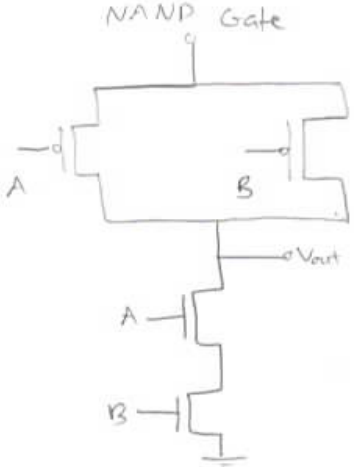
A general CMOS logic realization is shown below:



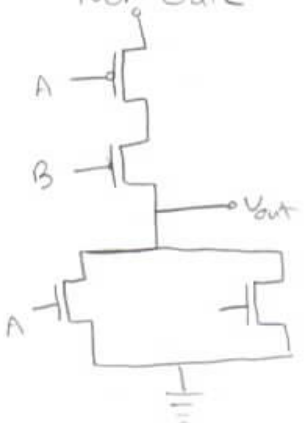
INVERTER



NAND Gate



NOR Gate



- If PMOS & NMOS have same size, then PMOS will have an ON state resistance equal to 2 times that of NMOS
- Fall time is directly proportional to resistance offered by NMOS network
- The rise time is directly proportional to resistance offered by PMOS network
- So ratio is equal to R_N/R_p
  - R_p → resistance by PMOS
  - R_N → resistance by NMOS
- P/N ratio : size of PMOS / size of NMOS.

Unskewed CMOS inverter, NAND-2 Gate, NOR-2 Gate
Resistances of PMOS & NMOS are equal

P/N = 2 → CMOS inverter
P/N = 1 → NAND
P/N = 4 → NOR

Sizing CMOS inverter to achieve 1.5 (high skewed)
↳ P/N ration of 3 → $R_p = 2/3 * R_N$

Sizing CMOS inverter to achieve 1.5 (low skewed)
↳ P/N ratio of 4/3 → $R_p = 3/2 * R_n$

Sizing CMOS NAND to achieve = 1.5 (high skewed)
unskewed CMOS NAND-2 : P/N = 1, Therefore P/N = 3/2

sizing CMOS NAND to achieve = 1.5 (low skewed)
unskewed CMOS NAND-2: P/N = 1, Therefore P/N = 2/3

Sizing CMOS NOR to achieve = 1.5 (high skewed)
unskewed CMOS NOR-2 · P/N = 4, Therefore P/N = 6

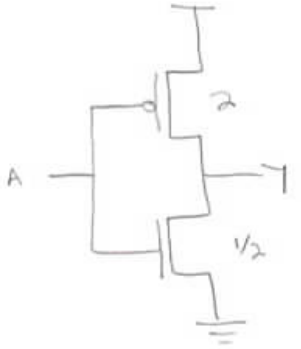
sizing CMOS NOR to achieve = 1.5 (low skewed)
unskewed CMOS NOR-2 · P/N = 4, Therefore P/N = 8/3

2- Skewed gates:

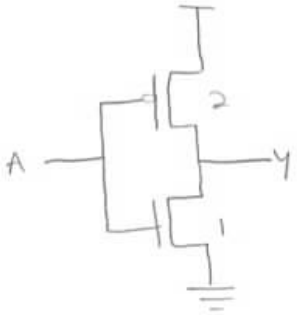
→ Skewed gates favour one edge over another

→ Downsize non-critical nmos transistor

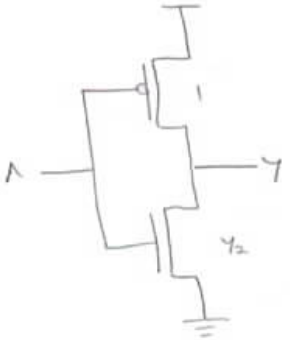
high skewed inverter



unskewed inverter (equal rise resistance)

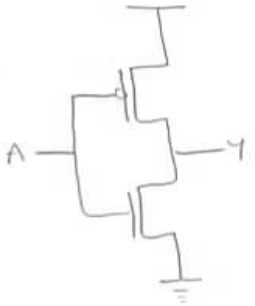


unskewed inverter (equal fall resistance)



NOR-2 & NAND-2

unskewed inverter



$g_0 = 1$

$g_1 = 1$

$g_{avg} = 1$

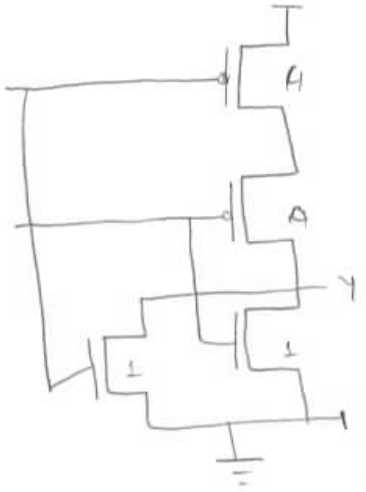
NAND-2

$g_A = 4/3$

$g_B = 4/3$

$g_{A-g} = 4/3$

NOR - 2



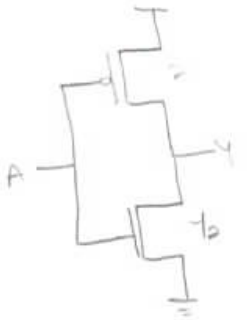
$g_u = 5/3$

$g_d = 5/3$

$g_{avg} = 5/3$

high skew :

Inverter :

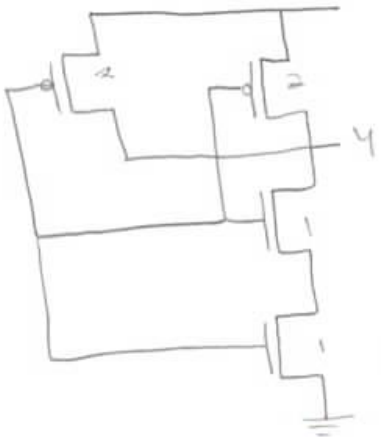


$g_u = 5/6$

$g_d = 5/3$

$g_{avg} = 5/4$

NAND - 2 :

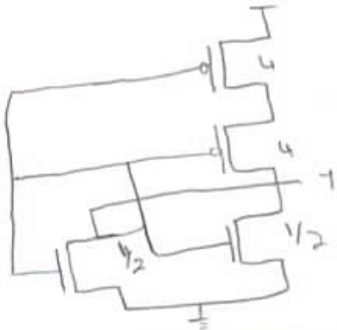


$g_u = 1$

$g_d = 2$

$g_{avg} = 5/3$

NOR 2 :



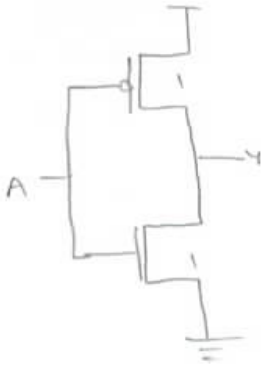
$g_u = 3/2$

$g_d = 3$

$g_{avg} = 9/4$

Low-Skewed:

Inverter:

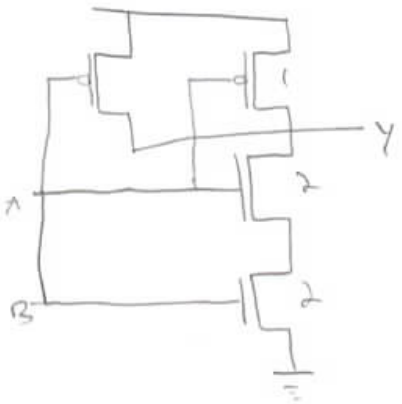


$g_u = 4/3$

$g_d = 2/3$

$g_{avg} = 1$

NAND-2

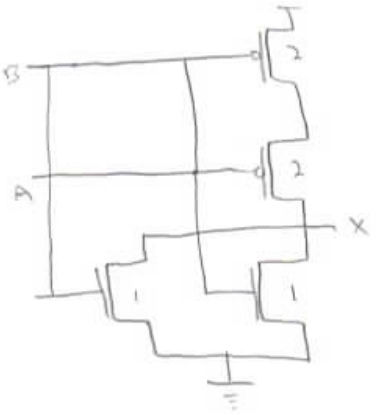


$g_u = 2$

$g_d = 1$

$g_{avg} = 3/2$

NOR-2



$g_{ud} = 2$

$g_d = 1$

$g_{avg} = 3/2$

Logical effort for skew gate:

b) Logical effort of a skewed gate for a particular transition is ratio of input capacitance of that gate to input capacitance of an unskewed inverter delivering the same output for the same transition

* Logical effort is smaller for favoured directions but larger for other direction.