Ryerson University

Department of Electrical, Computer, & Biomedical Engineering
Faculty of Engineering & Architectural Science

Course Title:	Low Power Digital Integrated Circuits
Course Number:	ELE 734
Semester/Year (e.g.F2016)	F2022

Instructor:	Dr. Andy Ye

Assignment/Lab Number:	4
Assignment/Lab Title:	CMOS 1-bit full adder

Submission Date:	November 30, 2022
Due Date:	November 30, 2022

Student LAST Name	Student FIRST Name	Student Number	Section	Signature*
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*By signing above you attest that you have contributed to this written lab report and confirm that all work you have contributed to this lab report is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a "0" on the work, an "F" in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at: http://www.ryerson.ca/senate/current/pol60.pdf

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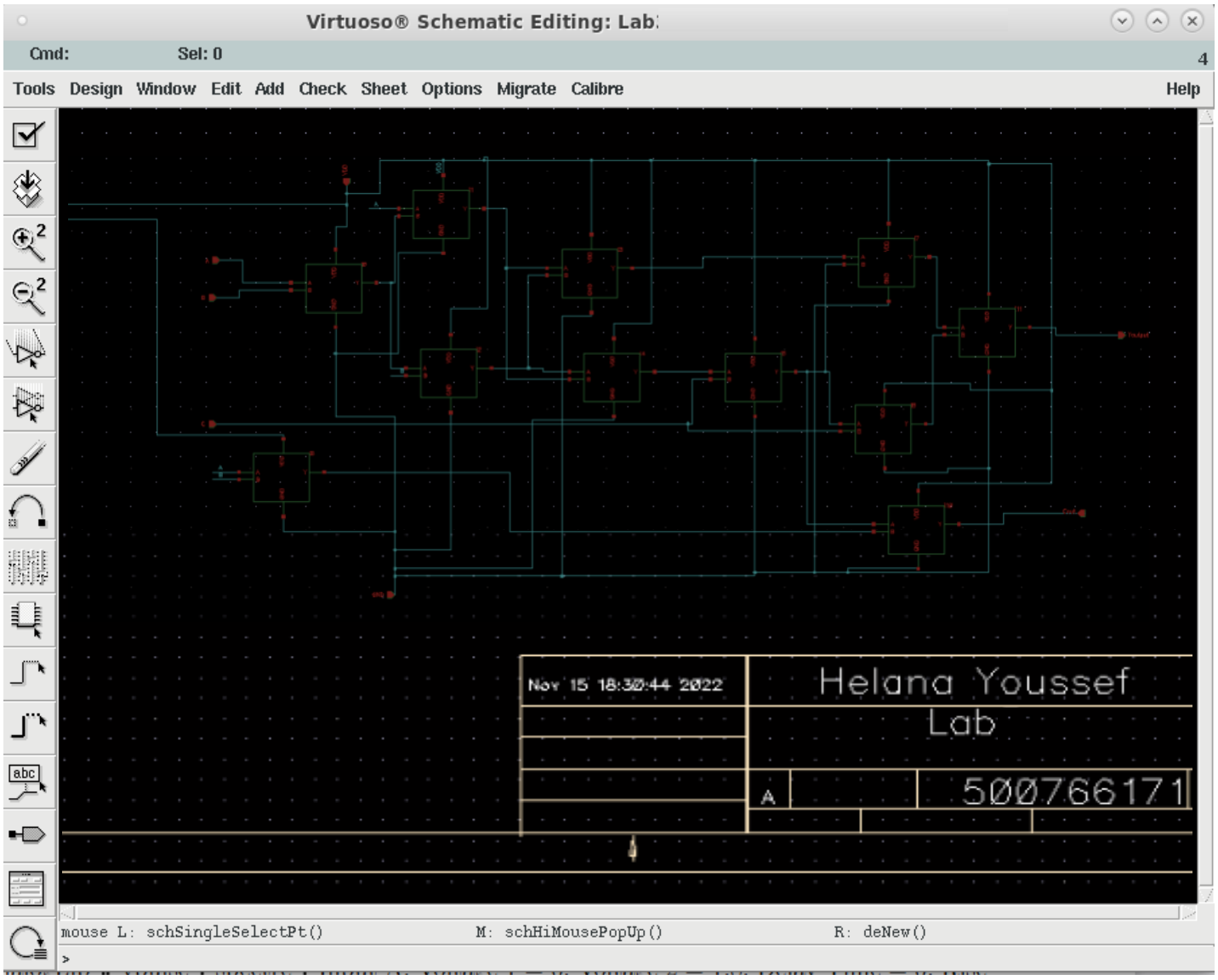
Introduction:

The objective of this lab was to put in place a 1-bit full adder. The logical effort method will be used to size the complete adder to drive a big output capacitance at its sum output. A random stream of bits will be used as input to test the adder's performance, and the worst-case delay will be simulated. Unfortunately, due to some time constraints on my end I was not able to complete this lab. Below id what I have been able to do for this lab. I am hoping for any marks that can be given here.

Schematic of Adder:



Conclusion:

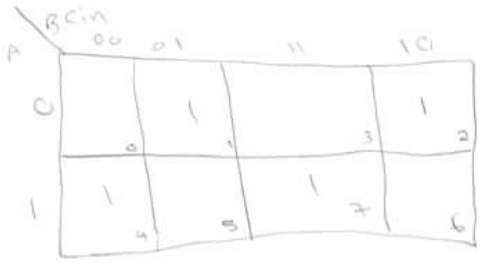
The lab was not completed, I am just hoping for any part marks that can be given here.

Pre-Lab:

TLE 734 : Pre-Lab 4

1- 1 bit full adder

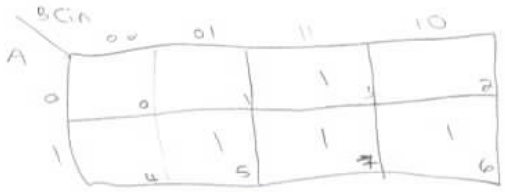
A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



$S = \bar{A}\bar{B}Cin + \bar{A}B\bar{Cin} + A\bar{B}\bar{Cin} + ABCin$

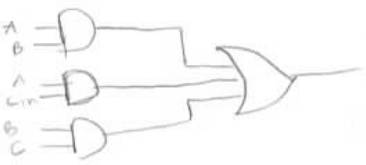
$= Cin(A\bar{B} + AB) + \bar{Cin}(\bar{A}B + A\bar{B})$

$S = (A \oplus B) \oplus Cin$



$Cout = AB + ACin + BC$

$S = (A \oplus B) \oplus Cin$



*Still working on understanding question 2

2- Logic effort method :

$$C_{in,j} = \frac{g_i C_{out,i}}{\hat{f}} \qquad D = NF^{\frac{1}{N}} + P$$

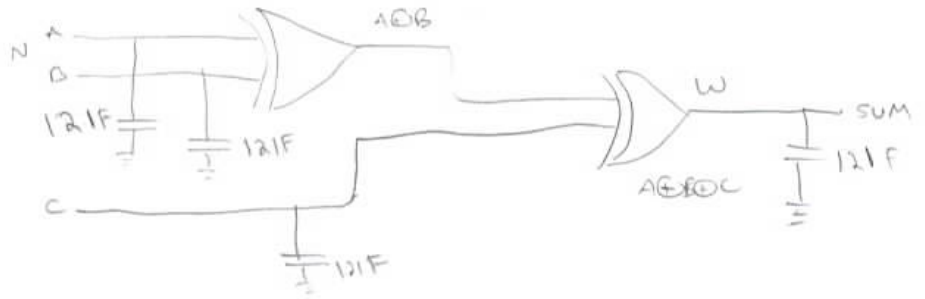
$$\hat{f} = F^{\frac{1}{N}}$$

$$N = \log_4 F$$

$$F = GBH$$

* Student number ends in 71

Therefore 5c + 71 = 121F



Logical effort method in full adder :

i) Number of stages = 2

N = 2

ii) Path logical effort, $G = \Pi g_1 * g_2$

$= 4 \times 4 = 16$ [logical effort of xor gate is 4]

iii) Parasitic delay along Path (N-W), $P = 4 + 4 = 8$ [Parasitic delay of xor gate is 4]

iv) The Branching effort, $B = 1$ [since fan out of all gates = 1]

Since delay D, is not given, so assuming a delay of 1Cs

$D = N \cdot F^{1/N} + P$

$(F)^{1/N} = \frac{D-P}{N} = \frac{16-8}{2} = 4$

$F^{1/2} = 4$

$\Rightarrow F = 16$

if $f = GBH$

Then electrical effort, $H = \frac{f}{GB}$

$= \frac{16}{16 \times 1} = 1$

Then gate size $C_{in} = \frac{C_{out}}{H}$

$= \frac{121f}{1}$

$= 121f$