Wang-LeGrand-Lab1-326

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We both contributed equally when performing both parts of the regular assignment, the extra credit assignment, and the lab report.

High Level Circuit

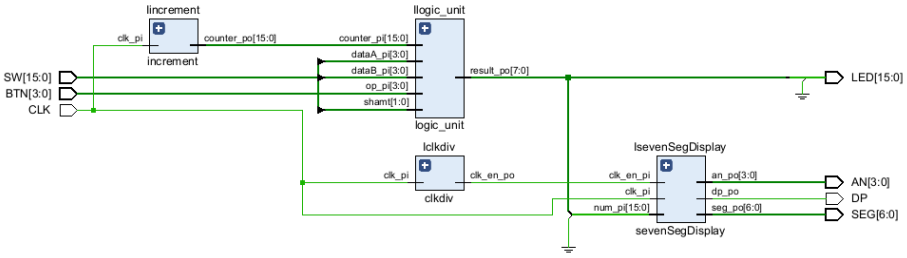

Figure 1: High Level Circuit Schematic

On a high level the switch and button inputs enter the logic unit. The logic unit decides what operation what must be performed and outputs the result to result-po[7:0]. This signal travels the IsevenSegDisplay module and where the result is interpreted and displayed via interfacing with the display pins. In addition result-po[7:0] drives controls the LEDs. The clkdiv module provides a slower clock to the seven segment display and the increment module assists the logic unit in its increment function.

Logic Unit

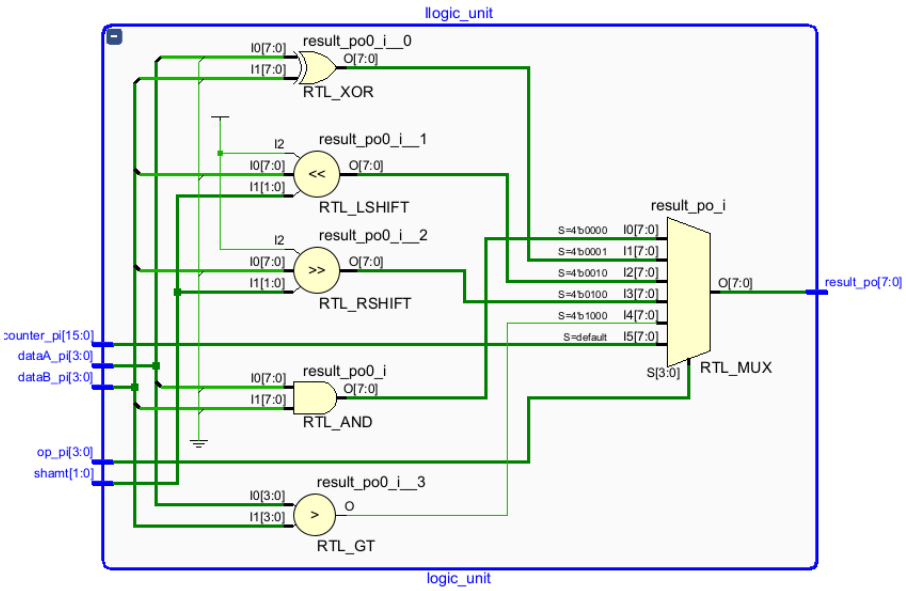

Figure 2: Logic Unit Schematic

Signals from the clock counter, switch, and buttons flow into the Logic Unit. op_pi[3:] is determined by single button presses and decides the operation performed with dataA_pi[3:0] and/or dataB_pi[3:0]. The output is stored in result_po[7:0], which holds the values to be displayed before before being interpreted by the seven segment display.

Extra Credit [10 points]: Parity Checker

To implement the parity checker, we computed p_en and p_val in logic_unit.v. p_en is an enable signal representing whether or not we want to display the parity, and p_val stores the actual parity. In top, we passed these values to the sevenSegDisplay module called IsevenSegDisplay. Then in sevenSegDisplay, we passed p_en and p_val to the segmentFormatter modules along with a bus to specify the relative position of each formatter in order to correctly display the EVEN or ODD text.