Laboratório de Arquitetura de Computadores

Relatório 03

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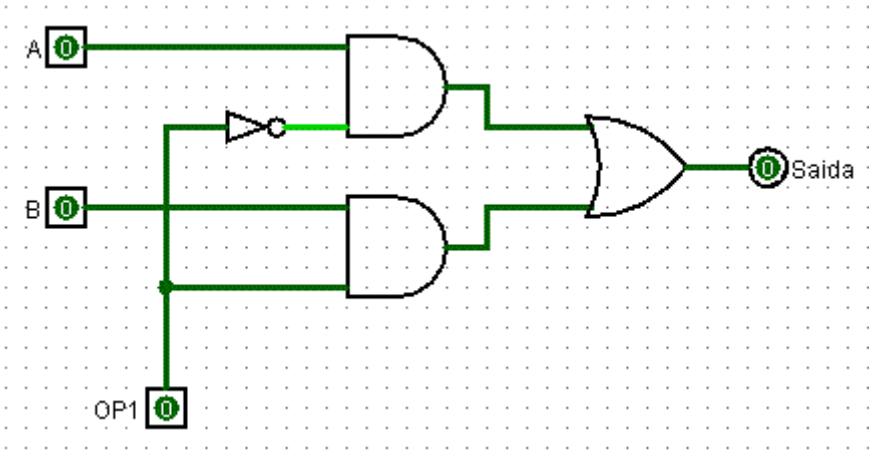
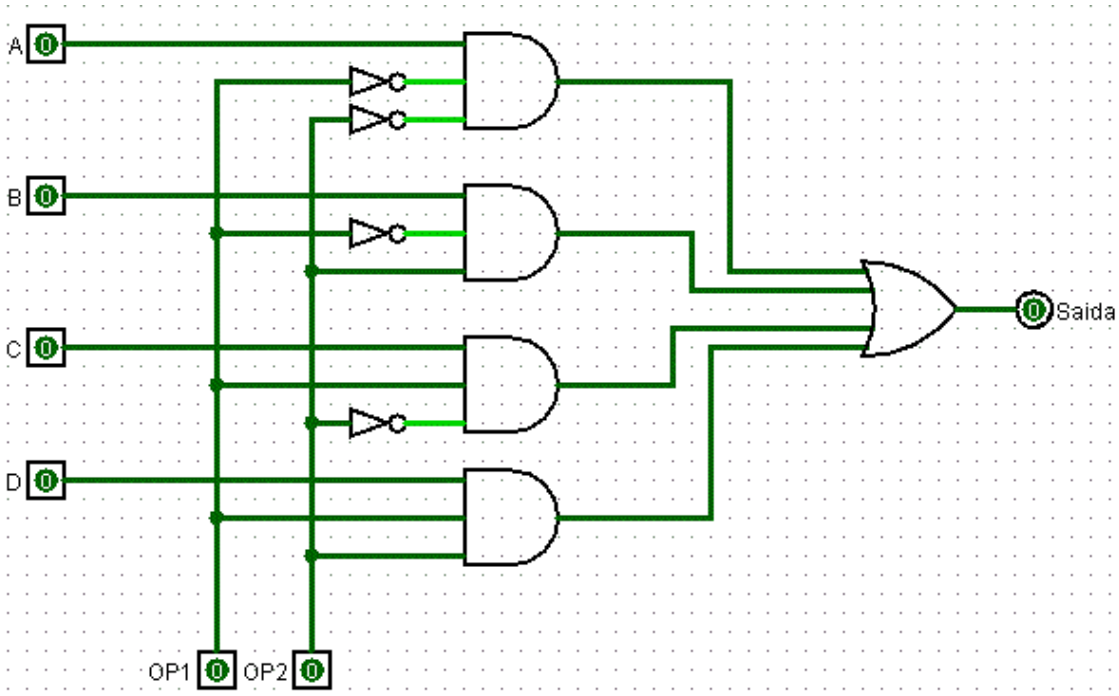
Prof. Romanelli

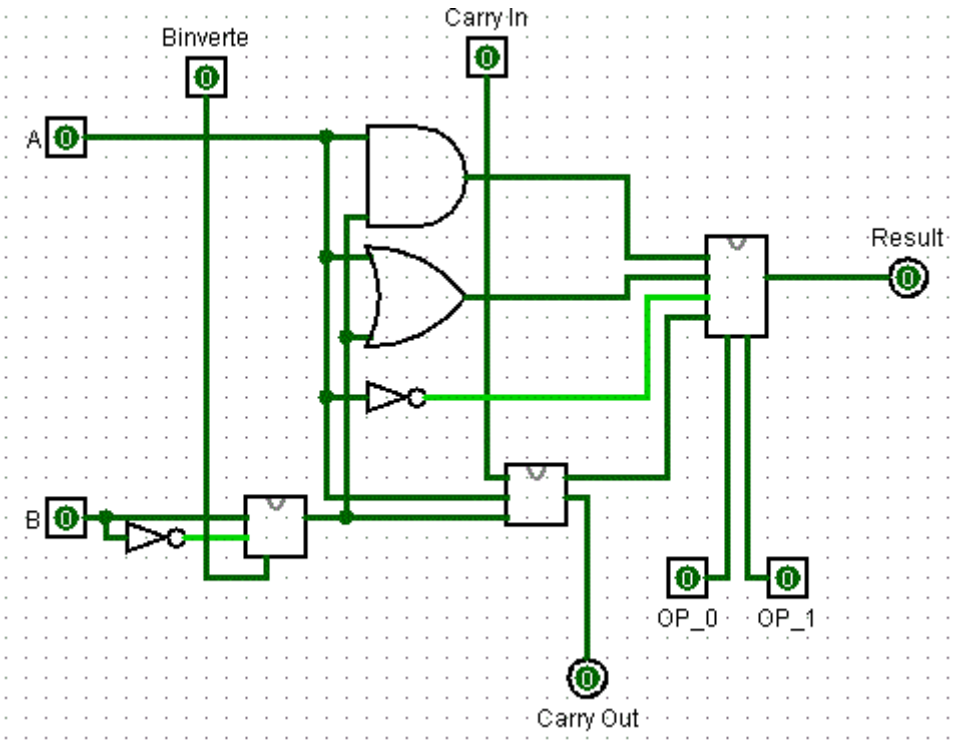
Parte 1



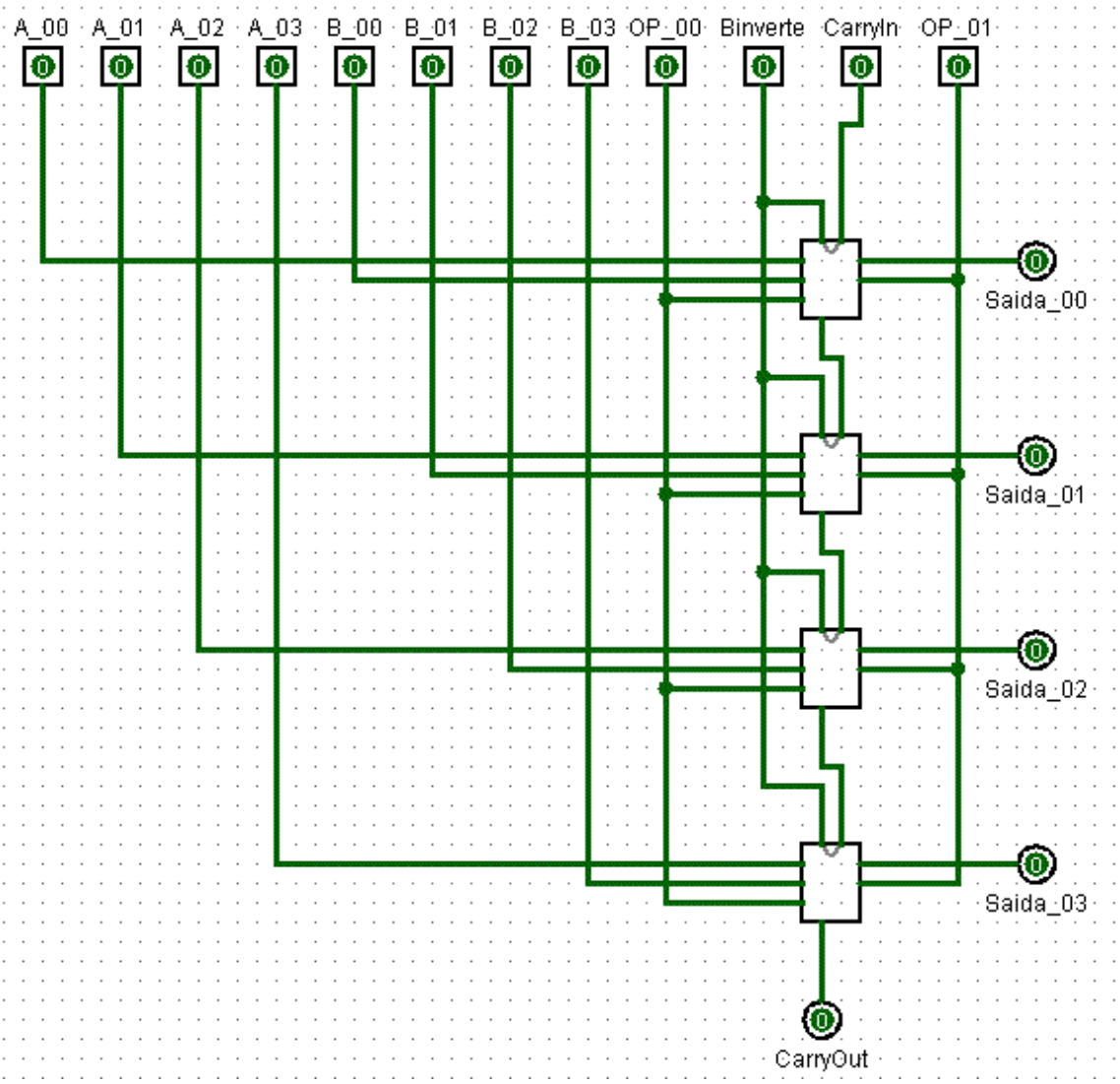
Multiplexador para B Inverte



Determina a saída da ALU dependendo das operações

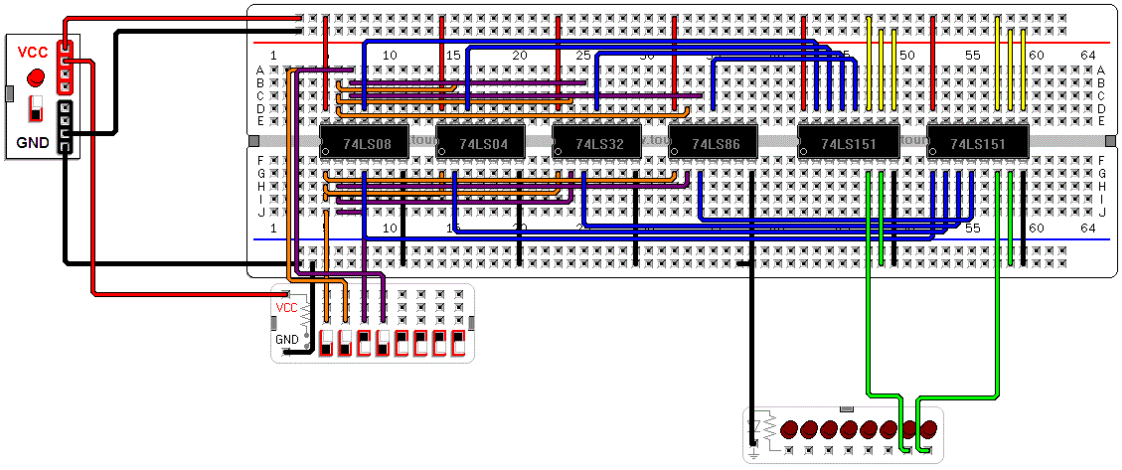


ALU de 1 bit

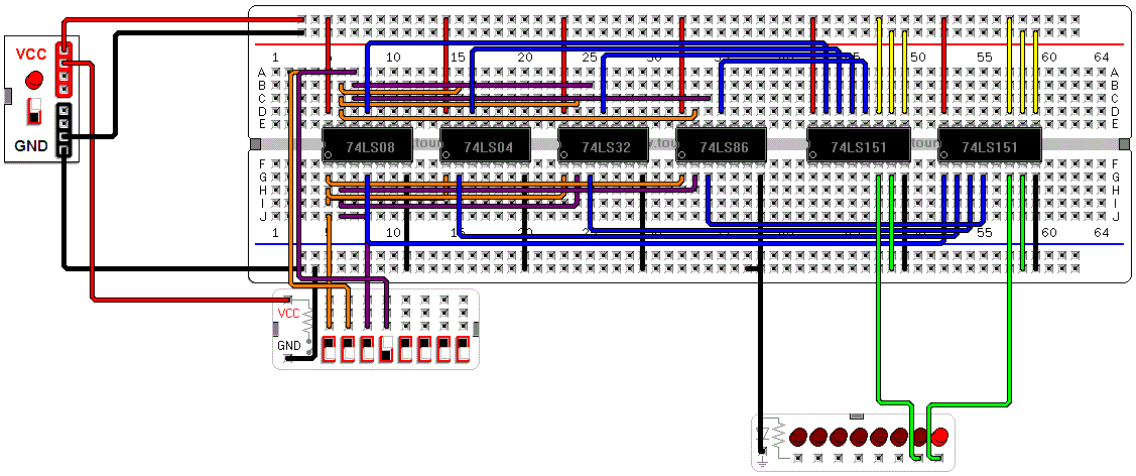


ALU de 4 bits

Parte 2



Saida 00 – AND



Saída 01 – OR

Instrução Realizada	Binário (A, B, Op.Code)	Valor em Hexa	Resultado em Binário
AND (a , b)	10 01 00	24	00
0R (a , b)	00 01 01		
SOMA (a , b)	00 01 11		
NOT (a)	11 00 10		
AND(b , a)	00 01 00		