NTNU – Trondheim
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Department of Electronics and Telecommunications

TTT4212 RF/Microwave Design and Measurement Techniques

Term Project Fall 2014

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1 Abstract

This report describes the process of designing, building and verifying an RF power amplifier for the 2.4 GHz±50MHz frequency band. The Cree CGH40010F GaN transistor is used as the active device. The circuit is built on standard FR-4 substrate. The circuit is designed and simulated in the Keysight ADS software suite, then built up and measured using standard RF measurement instruments such as a network analyzer and spectrum analyzer.

The resulting amplifier was measured to have a small-signal gain of 14dB at the center frequency of 2.4 GHz, however, the gain diminished rapidly towards the lower end of the operating band at 2.35 GHz. Also the large-signal power gain and power added efficiency showed poorer performance at the lower end of the operating band. At 2.4 GHz, the large-signal gain with an input signal of 27dBm was measured to 10dB with a power-added efficiency of 35% . Third-order intermodulation distortion was measured to -22dBc at a peak output power of 38dBm with a two-tone input signal with 5Mhz spacing.

Contents

2 Introduction

In the course TTT4212 RF/Microwave design and measurement techniques at NTNU, the students are given the task of designing, building and verifying the performance parameters of an RF power amplifier. The amplifier should fulfill the following requirements and design restrictions:

- Center operating frequency of 2.4 GHz
- Based on the Cree CGH40010F GaN transistor
- Drain voltage biased at 28V
- Gate voltage biased at -3.0V or higher
- The amplifier should be unconditionally stable
- Small-signal bandwidth of at least 100 Mhz
- Small-signal gain of at least 13dB throughout the bandwidth
- Output power of at least 39dBm with a single-tone input power of 27dBm
- Some geometrical restrictions for the board layout are given to make the amplifier fit on a standardized heatsink, to avoid the added time, cost and complications of manufacturing customized heatsinks for each group of students.

The power added efficiency (with a single-tone input signal at 27dBm) and intermodulation distortion (for a two-tone signal with 5 Mhz spacing and a peak output power of 38 dBm) should also be measured, however, no requirements for these performance parameters are given, and it will be up to the group members' to decide which parameters to focus on optimizing (as long as the requirement specification is fulfilled.

The circuit shall be designed and simulated in the Keysight Advanced Design System (ADS) software suite for computer-aided design (CAD) and simulation of microwave circuits, and all performance parameters shall be verified to be within the requirement specification before proceeding to making a board layout (also in ADS), generating the Gerber production files for having the printed circuit board manufactured, and then building the amplifier and doing real world measurements at the lab.

3 Theory

3.1 Amplifier classes

3.2 Efficiency

3.3 Linearity

3.4 Distortion

4 Method of design

In this chapter, the design procedure will be described, and the choices we made will be clarified. Then the test-measurements is explained in detail. During the design process, we will use the models given for inductors and capacitors. We will use ideal resistors from the libraries in ADS.

4.1 DC Bias point at gate

The first step in designing a power amplifier is to choose the DC bias point, which will define the amplifier's class of operation.We will be aiming for a deep AB class design, because this gives a good compromise between gain, linearity and efficiency, which enables us to meet the required specifications as well as obtain good results with respect to the other performance parameters with no set requirements. We are using the ADS Design Guide called FET_ IV_ Gm_ PowerCalcs, where we inserted the transistor as shown in figure. From the design guide we used the I/V-plot to find the gate bias voltage that gives the desired quiescent drain current of 300mA, which will be used as a starting point as this will be low in the class AB range ($0 < Ids < Imax/2$). We may need to tweak the quiescent current when testing on the real amplifier. The gate bias voltage that gives this quiescent current was found to be -2.6V.

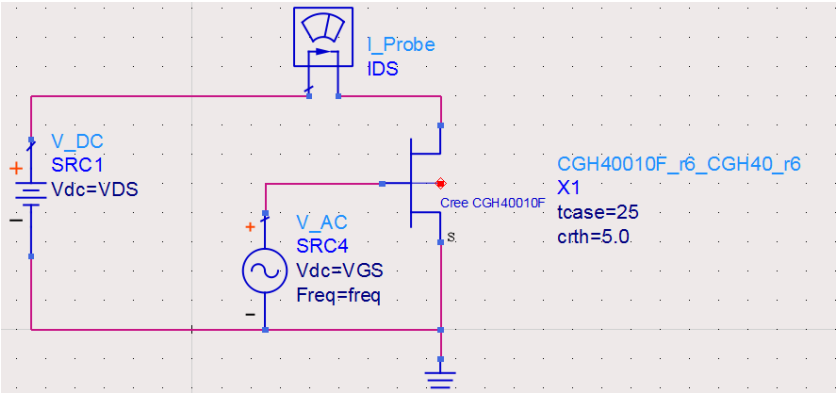

Figure 4.1: Setup for bias-measurements

4.2 Bias network

To ensure that the RF input does not affect the DC power supply, a quarter-wave transformer was used to present an infinite impedance in the 2.4GHz band when looking towards the DC power supplies from the RF signal pathways. The values were tuned to obtain optimal ac-block as seen from the transistor gate. In addition, a bank of lumped capacitors was used to suppress noise from the DC power supplies from entering the RF signal pathway. The same DC bias network was used for both the gate and drain DC bias voltage connections.

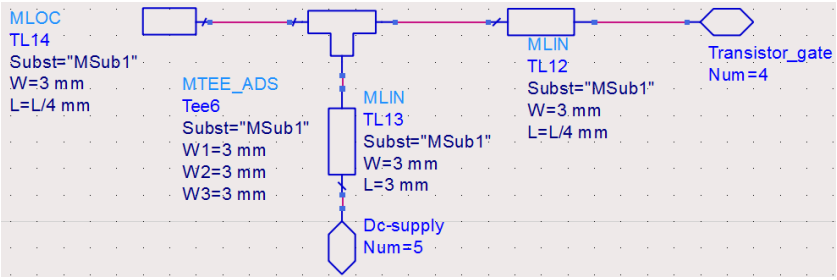

Figure 4.2: Setup for bias-network

4.3 Stability

To check if the amplifier is stable, we used the small-signal S-parameter simulations in ADS with added blocks for measuring the stability factors (mu and muprime) on the input and output. According to the measurements, the amplifier is stable at higher frequencies, but at lower frequencies it is unstable. To remove the instabilities we will introduce losses at the lower frequencies, by adding a series RC element at the input, and a resistor at the DC bias feed point as shown in figure 4.3. The capacitor C and

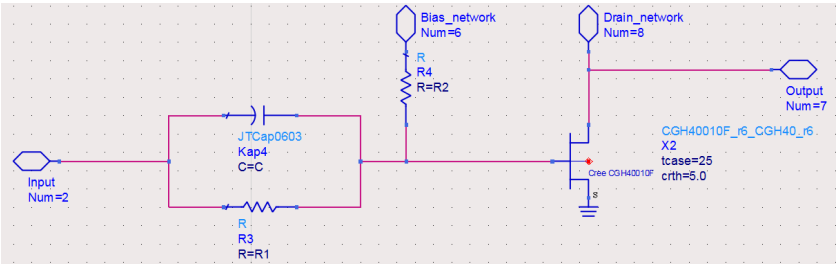

Figure 4.3: Stability-network

Resistor R1 presents a high impedance for lower frequencies, but for higher the capacitor is an effective short. The resistor R2 is introduced as a loss for all frequencies.

The values C,R1 and R2 were found by using ADS' optimization feature, with optimization goals for the stability factors (mu and muprime) and the maximum available gain. The lowest value for the stability factors across the simulated frequency range from 0Hz to 6GHz was 1.05.

4.4 Matching

When stabilizing the amplifier, one of the goals for optimization was maximum available gain. to achieve this gain, one must match the input and output to 50 Ohm. To realise this without having to mount more components, we added an open-circuit stub of microstrip line as shown in figure 4.4. The setup was used both on the input and

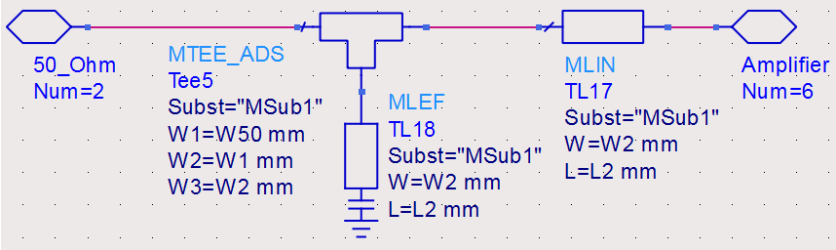

Figure 4.4: Setup for matching the amplifier with 50Ω

output of the amplifier, and optimized the values for max S21 within the band.

4.5 Large signal simulation, one tone input signal

To run large signal simulation, a design guide called HB1TonePAE_ Pswp was used. In the design guide, we checked the power added efficiency, the interpolated output spectrum and fundamental output power. We saw that power added efficiency was low, so we ran an optimization with increased power added efficiency and output power with 27dBm input as goals.

4.6 Large signal simulation, two tone input signal

To run large signal simulation two tone, a design guide called HB2TonePAE_ Pswp was used. In the design guide we checked the Power added efficiency, interpolated output spectrum and the output power with 27dBm as input.

4.7 Layout and conversion to real components

Now that the design is complete, all components that are related to the layout will be added. This is done to make sure that the layout will fit within the predefined board

size and that there is as few as possible steep transitions between different widths of microstrip line. At the same time, the transistor was placed in the center of the board with its borders to cut out from the PCB. With the restriction, the lines on the output was too long, added bends to make it fit.

4.8 Tests with complete layout

All the above simulations was done again since the changes done may change for instance the stability of the amplifier. All new simulations are done with the whole design. A few tweaks with respect to line geometry was needed to obtain similar responses but the design passed the requirements given by the task.

4.9 Laboratory measurements

The goal for the measurements is to determine if the amplifier (DUT) passes the requirements given by the task or not. To do this we need to perform a small signal gain test, one-tone large signal test and a two-tone large signal test.

4.9.1 Small-signal s-parameters

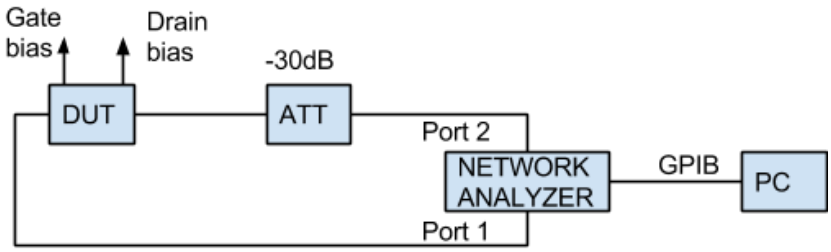

Figure 4.5: Small-signal measurements setup

As shown in figure 4.5, there will be an attenuator connected to the output of the amplifier to protect the network analyzer ports from excessive input voltages that could damage the instrument. The network analyzer was calibrated using a TOLS (through-open-load-short) calibration sequence.

4.9.2 Large signal one- and two-tone

We were at liberty to choose three set frequencies to perform the large-signal testing at. We chose the frequencies of 2.35 GHz, 2.40 GHz and 2.45 GHz, because testing at these frequencies would give us the best prerequisites for determining if we had met the requirement specifications within the band of operation. As shown in figure 4.6 there

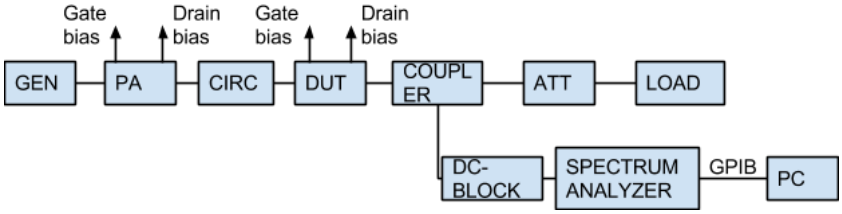

Figure 4.6: Large-signal measurements setup

are several items that will introduce losses in the signal pathway, all of those must be subtracted from the measured power levels when analyzing the results in Matlab.

4.9.3 Calculations

Table 4.1 lists the S-Parameters for the transistor as given in [3]. Using these, we can calculate the K and $|\Delta|$ factors to determine the stability using equations (6.31) and (6.32) in [2].

S_{11}	$0.9\angle 165°$	S_{12}	$0.019\angle -17.6°$
S_{21}	$4.21\angle 46.9°$	S_{22}	$0.39\angle -162°$

Table 4.1: S-parameters for Cree CGH40010

Using these values we find $K = 0.732$ and $|\Delta| = 0.282$. *Rollet's condition* specifies that an amplifier will be unconditionally stable if $K > 1$ and $|\Delta| < 1$. Since only the latter condition is fulfilled in our case, the transistor will not be unconditionally stable by itself.

4.9.4 Stabilization circuit

4.10 Bias network

4.11 Matching network

5 Results

5.1 Simulated results

This section lists the results from the simulation done in the Keysight Advanced Design System (ADS) software suite.

5.1.1 Transistor I-V curve

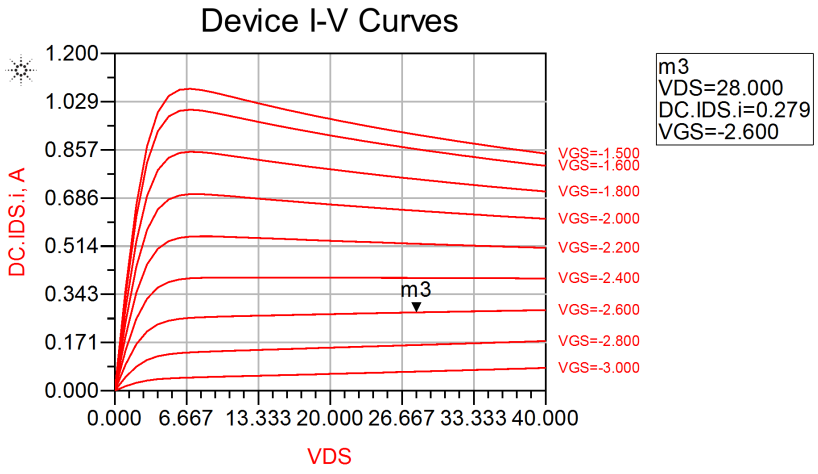

Figure 5.1: Simulated drain current for different drain and gate bias voltages with a load-line

Note that the transistor model used is only valid for VDS voltages between 28 and 48 volts, meaning that the I-V-curves are at best approximate below 28 volts.

5.1.2 Stability simulations

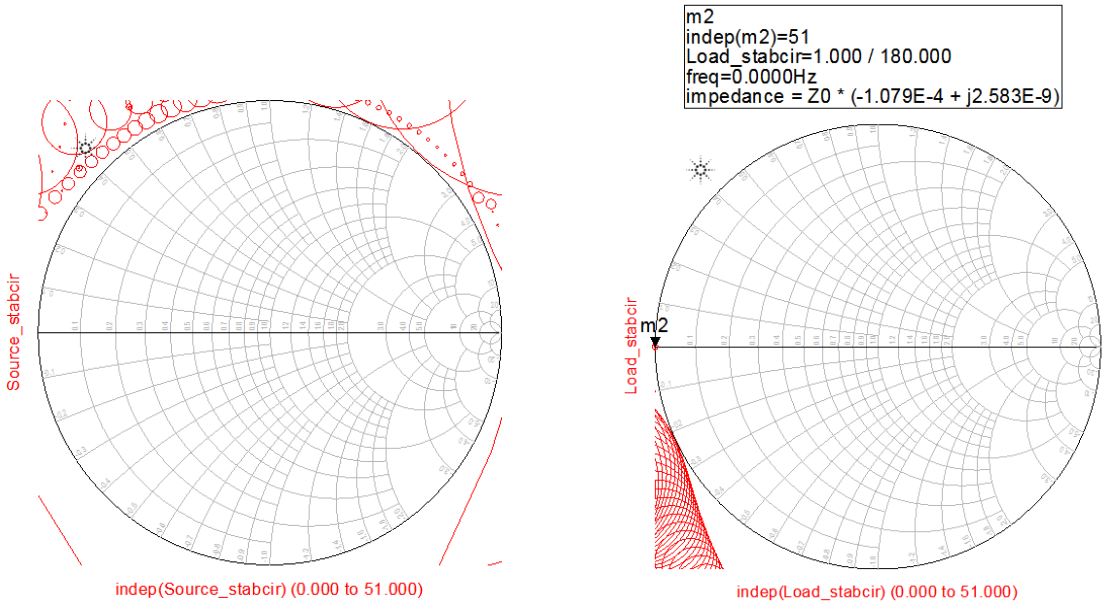

Figure 5.2: Smith-chart representation of the stability circles for source (left) and load (right) for frequencies between 0Hz and 6GHz

5.1.3 Small-signal gain

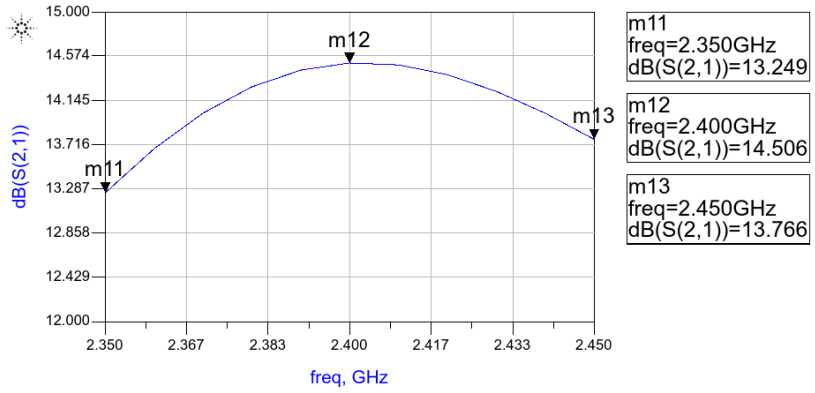

Figure 5.3: Simulated small-signal gain within the band of operation

The small-signal gain (S_{21}) has a peak value of 14.506 dB at 2.4GHz, and a minimum value within the band of operations of 13.287 dB, giving a maximum variation of 1.257

dB within the 100MHz band of operation.

5.1.4 Large-signal gain

Frequency	Output power	gain
2.35 GHz	38.71dBm	11.71dB
2.40 GHz	39.26dBm	12.26dB
2.45 GHz	38.87dBm	11.87dB

Table 5.1: Simulated output power with input power of 27dBm

5.1.5 Power added efficiency (PAE)

Frequency	PAE
2.35 GHz	40.30%
2.40 GHz	41.79%
2.45 GHz	42.59%

Table 5.2: Simulated power added efficiency with output power of 38dBm

5.1.6 Third-order intermodulation distortion (TOIMD)

TOIMD high	-15.35dBc
TOIMD low	-15.62dBc

Table 5.3: Simulated third-order intermodulation distortion with output power of 38dBm

5.2 Measured results

This section lists the results from the measurements done on the real circuit in the laboratory.

5.2.1 Small-signal gain

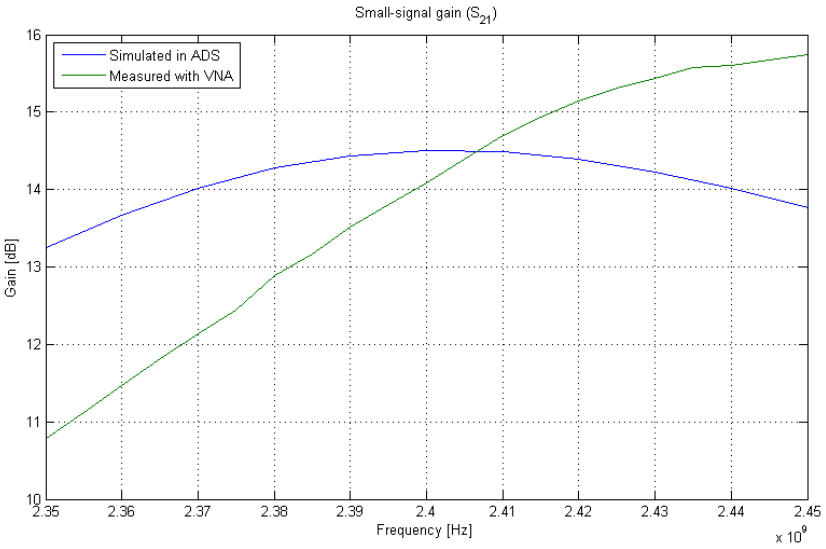

Figure 5.4: Measured small-signal gain (green) compared to simulated small-signal gain (blue) within the band of operation

Minimum measured gain was 10.79dB at 2.35 GHz, while the maximum was measured to 15.74dB at 2.45 GHz. At the center frequency of 2.40 GHz the small-signal gain was 14.08dB

5.2.2 Large-signal gain

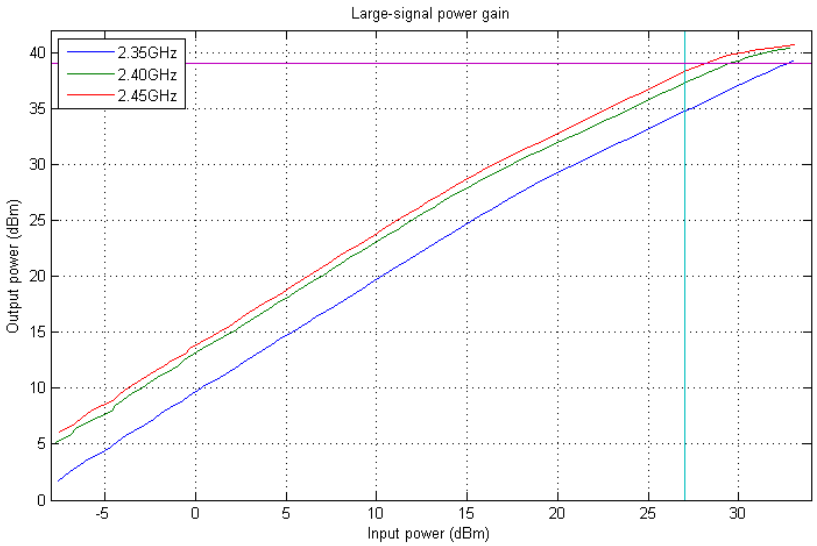

Figure 5.5: Measured output power at three different frequencies

Frequency	Output power
2.35 GHz	34.73dBm
2.40 GHz	37.17dBm
2.45 GHz	38.37dBm

Table 5.4: Measured power output with an input power of 27dBm

5.2.3 Power added efficiency (PAE)

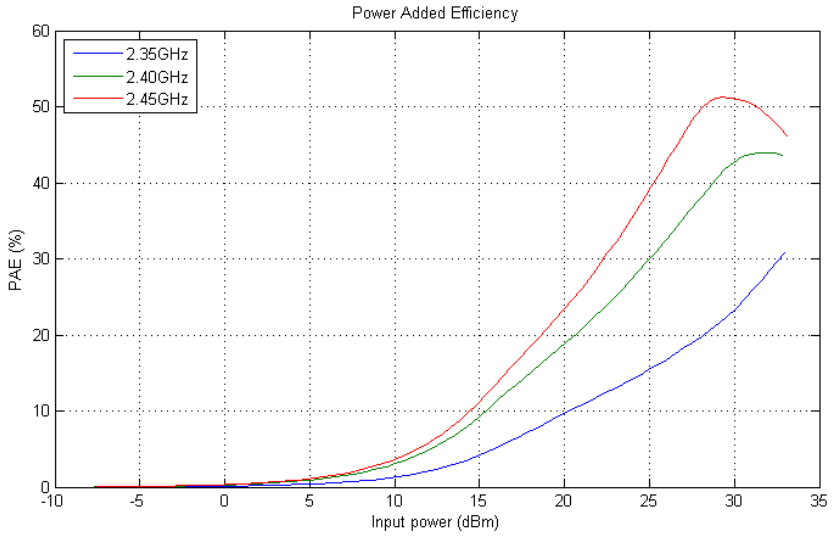

Figure 5.6: Measured power added efficiency at three different frequencies

Frequency	PAE
2.35 GHz	18.26%
2.40 GHz	35.02%
2.45 GHz	46.99%

Table 5.5: Measured power added efficiency with output power of 38dBm

5.2.4 Third-order intermodulation distortion

TOIMD high	-22.41dBc
TOIMD low	-22.45dBc

Table 5.6: Measured third-order intermodulation distortion with output power of 38dBm

5.2.5 Summary of measured results

Parameter	2.35 GHz	2.40 GHz	2.45 GHz	Requirement
Small-signal gain	10.79dB	14.08dB	15.74dB	$> 13dB$
Output power with 27dBm input	34.73dBm	37.17dBm	38.37dBm	$> 39dBm$
Power added efficiency	18.26%	35.02%	46.99%	-
Third-order intermodulation distortion		high: -22.41dBc low: -22.45dBc		-

Table 5.7: Summary of measured results

6 Discussion

6.1 Fulfillment of requirements

6.1.1 Stability

The amplifier was simulated to be unconditionally stable for all frequencies at all source and load impedances except for when the output was presented with a short-circuit to ground. In real life, it was only tested with a 50Ω termination on the input and a 50Ω dummy load, for which it proved not to oscillate at any frequency seen on the spectrum analyzer. No tendencies to start oscillating was seen when doing both small- and large-signal testing. To our best knowledge, the requirement of stability was fulfilled.

6.1.2 Small-signal gain and bandwidth

The simulated gain was within the requirement specification with a minimum value of 13.287dBm across the 100 MHz bandwidth. The measured gain was below the required minimum of 13dBm for the frequency range of 2.35 - 2.38 GHz, while it was above the 13dBm limit for the rest of the band of operation. This requirement was hence not fulfilled.

6.1.3 Large-signal gain

For an input power of 27dBm, the required output power of 39dBm was not achieved at any of the tested frequencies of 2.35 GHz, 2.40 GHz and 2.45 GHz. This requirement was then not fulfilled.

6.2 Other results

6.2.1 Power added efficiency

The power added efficiency exhibits the same shift in frequency as the gain, with the best performance at 2.45 GHz, while the results at 2.35 GHz and 2.40 GHz are below the results from the simulations in ADS.

6.2.2 Third-order intermodulation distortion

The third-order intermodulation distortion (TOIMD) was measured to be below -22dBc for all output power levels up to 38dBm. This level of TOIMD is similar to what was

achieved in a comparable amplifier design described in [4], which should mean that this is an acceptable TOIMD level, meaning the amplifier shows good linearity.

6.3 What happened

The shape of the measured small-signal gain curve shows that the maximum gain is not at our center frequency of 2.40 GHz where it was designed to be, but probably at or above 2.45GHz. This is most probably due to incorrect matching at the input or output. Since the center frequency was shifted upwards, this indicates that the electrical length of the matching network stubs is shorter than expected. This again leads to the observation that the propagation speed in the substrate is higher than expected, which must mean that the permittivity of the substrate is lower than expected.

Variations in the relative permittivity of the substrate is not uncommon when using standard FR-4 substrate, as this type of substrate by nature has a highly variable permittivity. If absolute control of the permittivity of the substrate is required, special, more expensive RF substrate should be used.

Since the small-signal gain at 2.45 GHz was well above the requirements, it is highly probable that the amplifier would meet the requirement specifications if some effort was put into tuning the input and output matching networks to have the input and output impedances matched as closely as possible to 50 Ohms.

6.4 Conclusion

The project was successful in designing an RF power amplifier that is unconditionally stable, shows quite good efficiency and linearity characteristics and is functional in amplifying RF frequency signals.

The project was not able to meet all point of the requirement specifications, however, having identified the most probable reasons for not fulfilling the required performance characteristics, it is believed that only a minor redesign should be needed to be able to reach the given performance criterions.

The project was successful in teaching the students participating in the group the techniques for designing, simulating, building and measuring an RF power amplifier.

7 Bibliography

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[3] *Cree CGH40010 Datasheet*. Cree, Inc. Rev 3.2, April 2012

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