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TTT4212 RF/Microwave Design and Measurement Techniques

Term Project Fall 2014

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1 Introduction

This report serves as the documentation of the work done in conjunction with the term project done in the course TTT4212 RF/Microwave design and measurement techniques. The goal of the project is to design an RF power amplifier using a single active device, the Cree CHG40010 GaN transistor, to simulate the performance parameters of the amplifier using the Keysight ADS software suite, and to verify the performance of the amplifier by building it and performing the required measurements.

2 Design of circuit

2.1 DC Bias point at gate

We are using ADS to simulate the I-V characteristics of the CGH40010 transistor. ADS is providing a built-in design guide for this purpose. Figure 2.1 shows the I-V characteristics, with drain current on the y-axis, drain voltage on the x-axis and curves for various gate voltages from -5 to -1 volts in 0.2 volts increments. Refering to figure 5.12 in [1, p. 200], we choose to set a bias point at approximately 70% of the maximum saturated drain current IDS, to achieve a compromise between good linearity and high gain. We find this to be a gate voltage of about -1 volts.

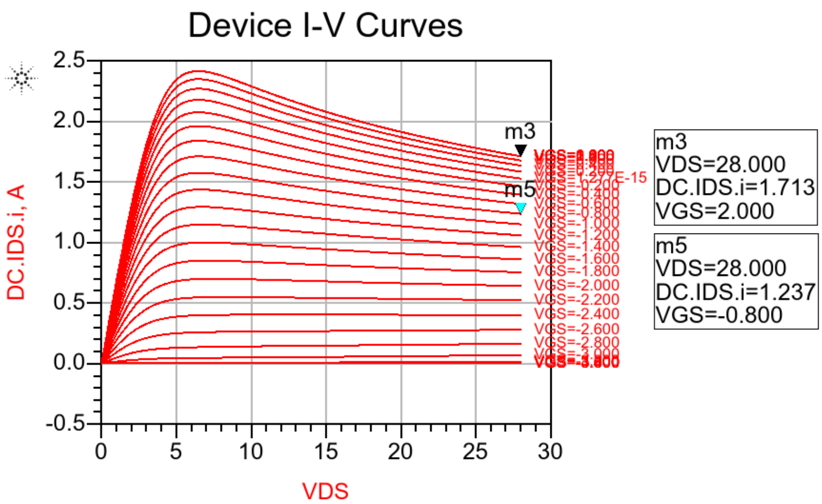

Figure 2.1: I-V curve characteristics for CGH40010

2.2 Gate bias network

The purpose of a bias network is to filter unwanted noise from the bias voltage source to prevent it from reaching the gate, and to prevent RF signal from the amplifier input from reaching the bias voltage source. Our gate bias network is composed of a microstrip quarter-wave transformer which blocks the input signal from reaching the bias source, and a capacitor bank that filters out noise from the bias voltage source.

Figure 2.2 shows the bias network we are using, with the probes used for measuring S-parameter characteristics. We have first simulated the two-port characteristics with terminal 1 at the input and terminal 2 at the point that will be connected to the transistor's gate. Figure 2.2 shows two-port parameters S_{12} and S_{22}, which shows that within our designated frequency band from 2.35 to 2.45 GHz, only between -42 and -50 dB of the input signal gets transmitted to the bias voltage source.

We have also simulated one-port S-parameters by grounding the input of the circuit and measuring the reflection coefficient at the output (S_{11}). This is more relevant to real-world conditions as the DC voltage source providing the bias voltage will act as an AC ground. The results of this simulation is shown in figure 2.2. The simulation shows that within the 2.35-2.45 GHz band almost all of the incident wave is reflected, while we have a -6dB attenuation of the reflected incident wave at approx. 1.8 GHz.

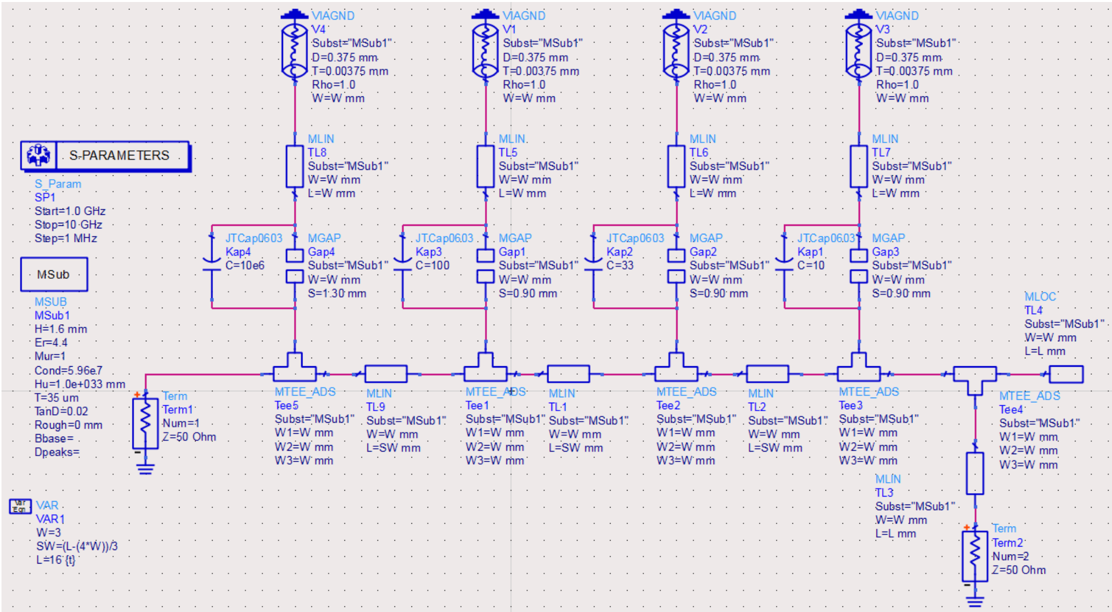

Figure 2.2: Gate bias network schematics

2.3 Matching network

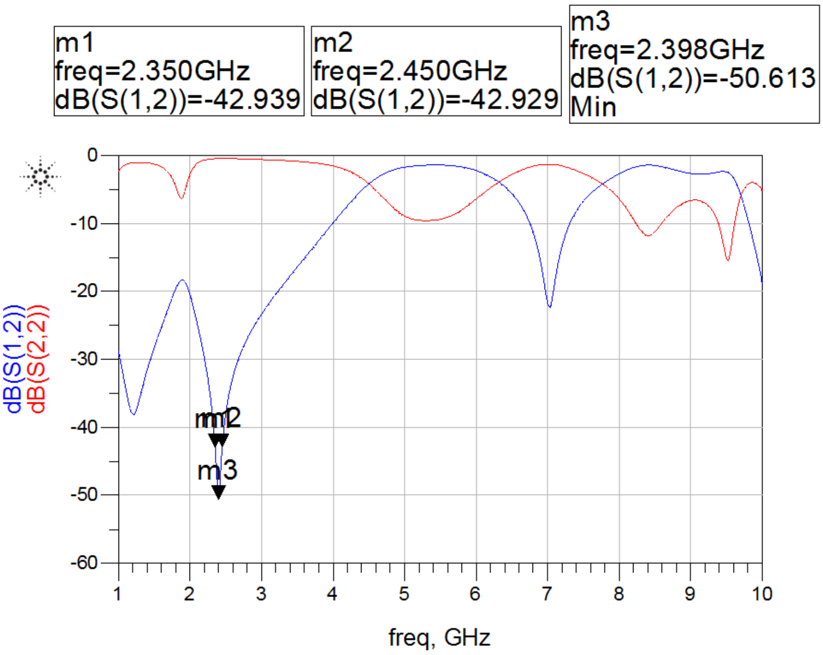

Figure 2.3: Bias network two-port S-parameter

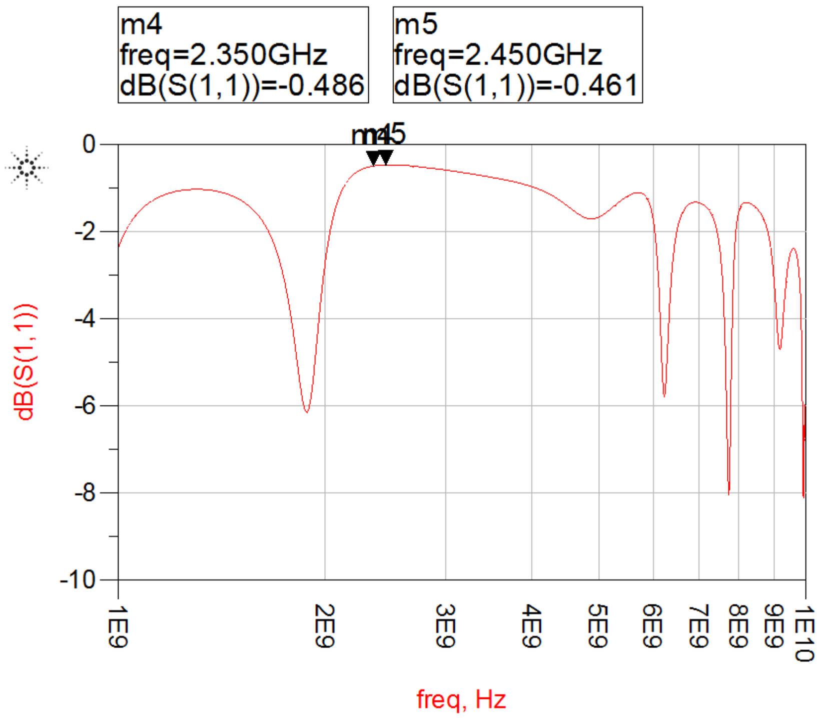

Figure 2.4: Bias network one-port S-parameter

3 Circuit Simulation

3.1 DC Bias point simulation

3.2 Linear S-parameter simulations

3.3 Nonlinear Harmonic balance simulation

4 Real-World Measurements

4.1 Gain

4.2 Power output

4.3 Stability

4.4 Linearity

5 Bibliography

[1] I.D. Robertson, *RFIC and MMIC Design and Technology*. The Institution of Engineering and Technology, 2nd edition, 2001