

HARDWARE SECURITY

101

DEEP DIVE INTO HARDWARE

ABOUT ME

”

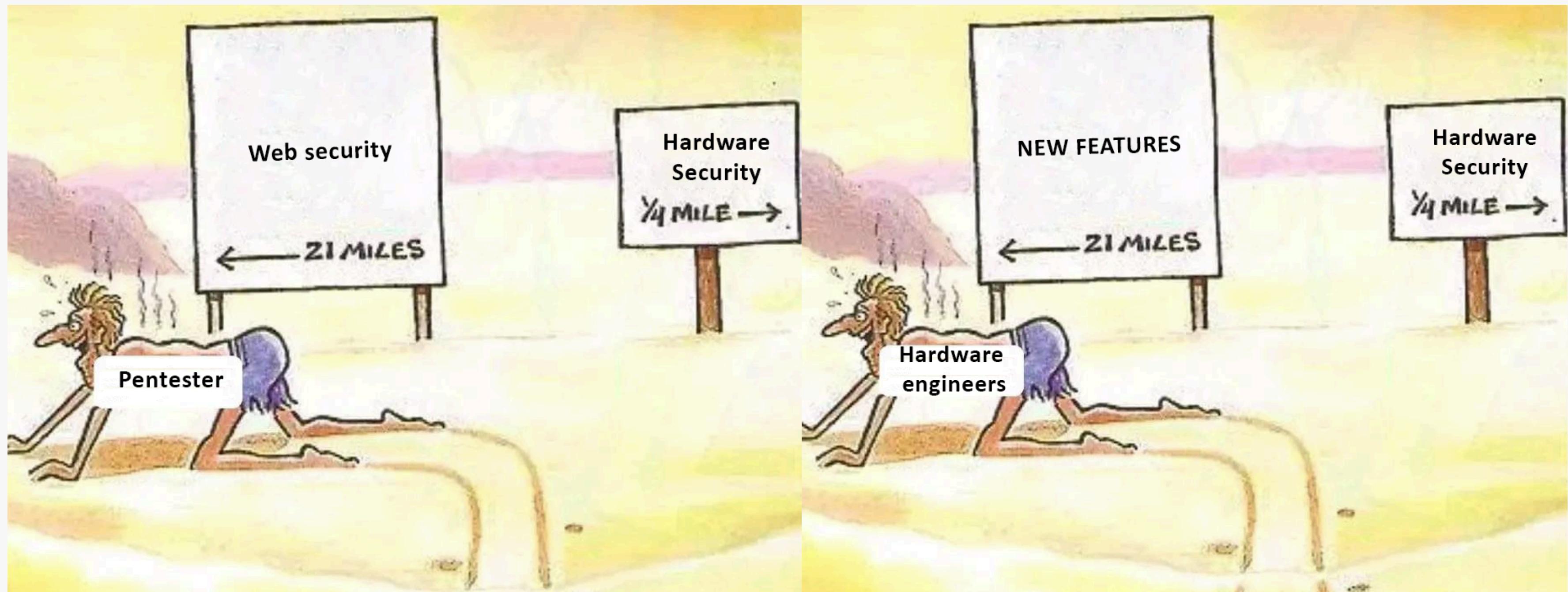
**Computer hardware
engineering**

Founder of Beelog Tech
Inventor, IoT developer



Davgasuren

PROBLEM



REAL LIFE PROBLEMS



REAL LIFE PROBLEMS



REAL LIFE PROBLEMS



REAL LIFE PROBLEMS



REAL LIFE PROBLEMS



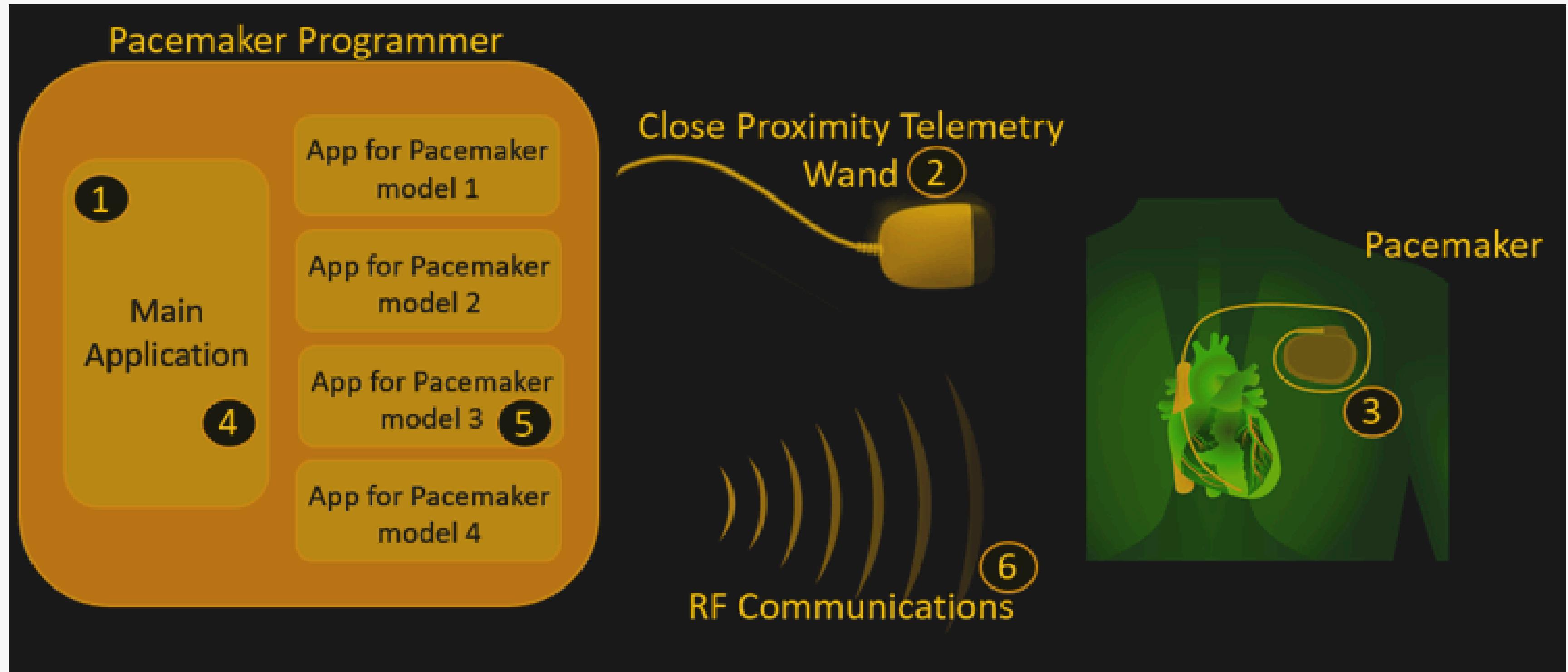
REAL LIFE PROBLEMS



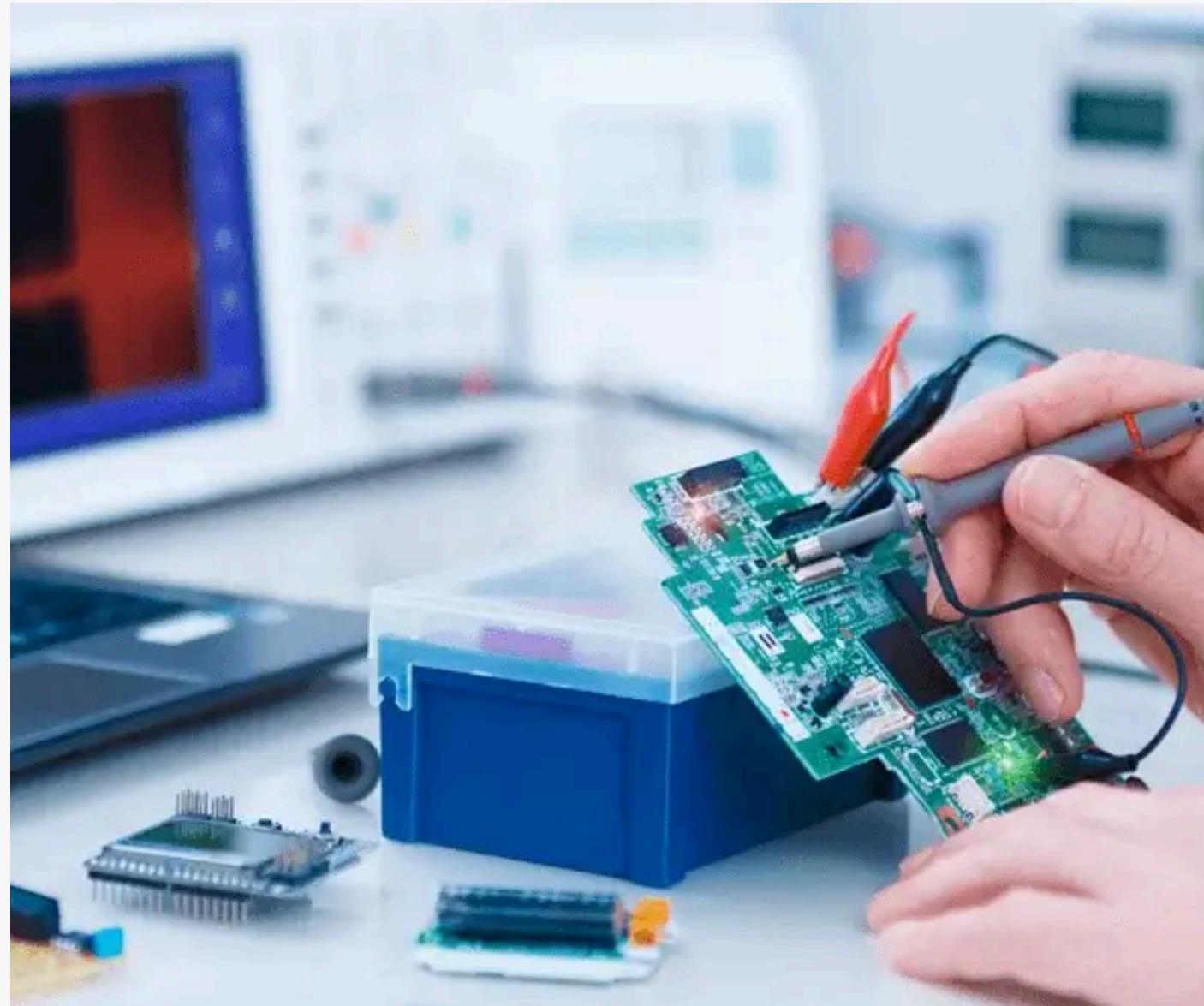
REAL LIFE PROBLEMS



REAL LIFE PROBLEMS



HARDWARE IS HARD

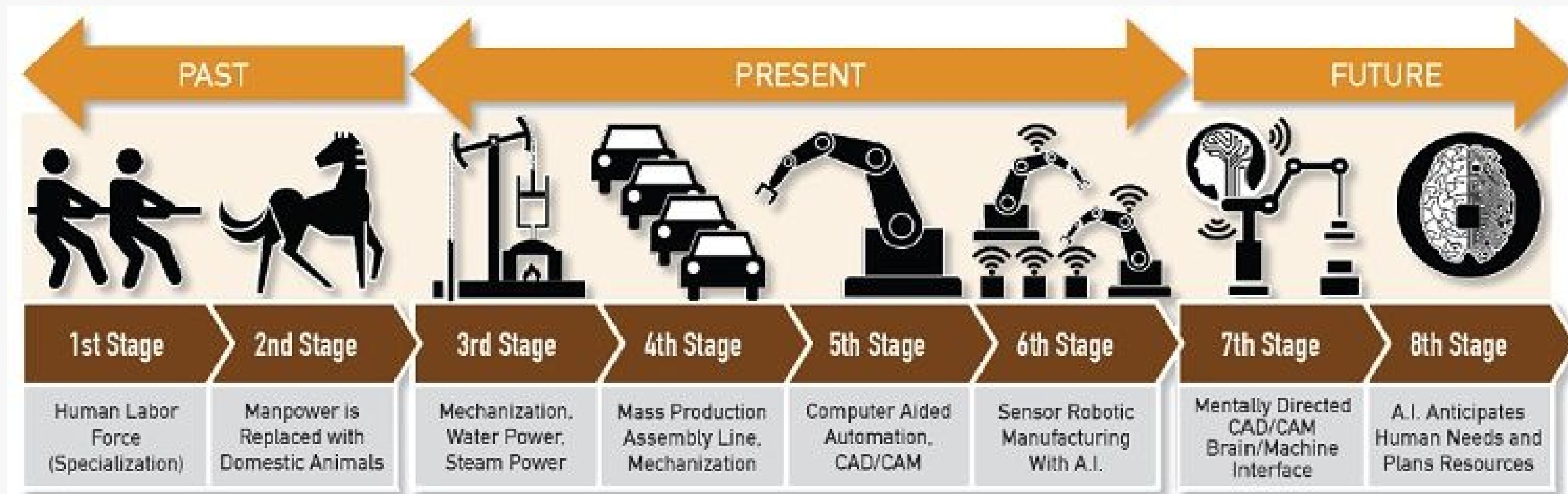


More moving parts

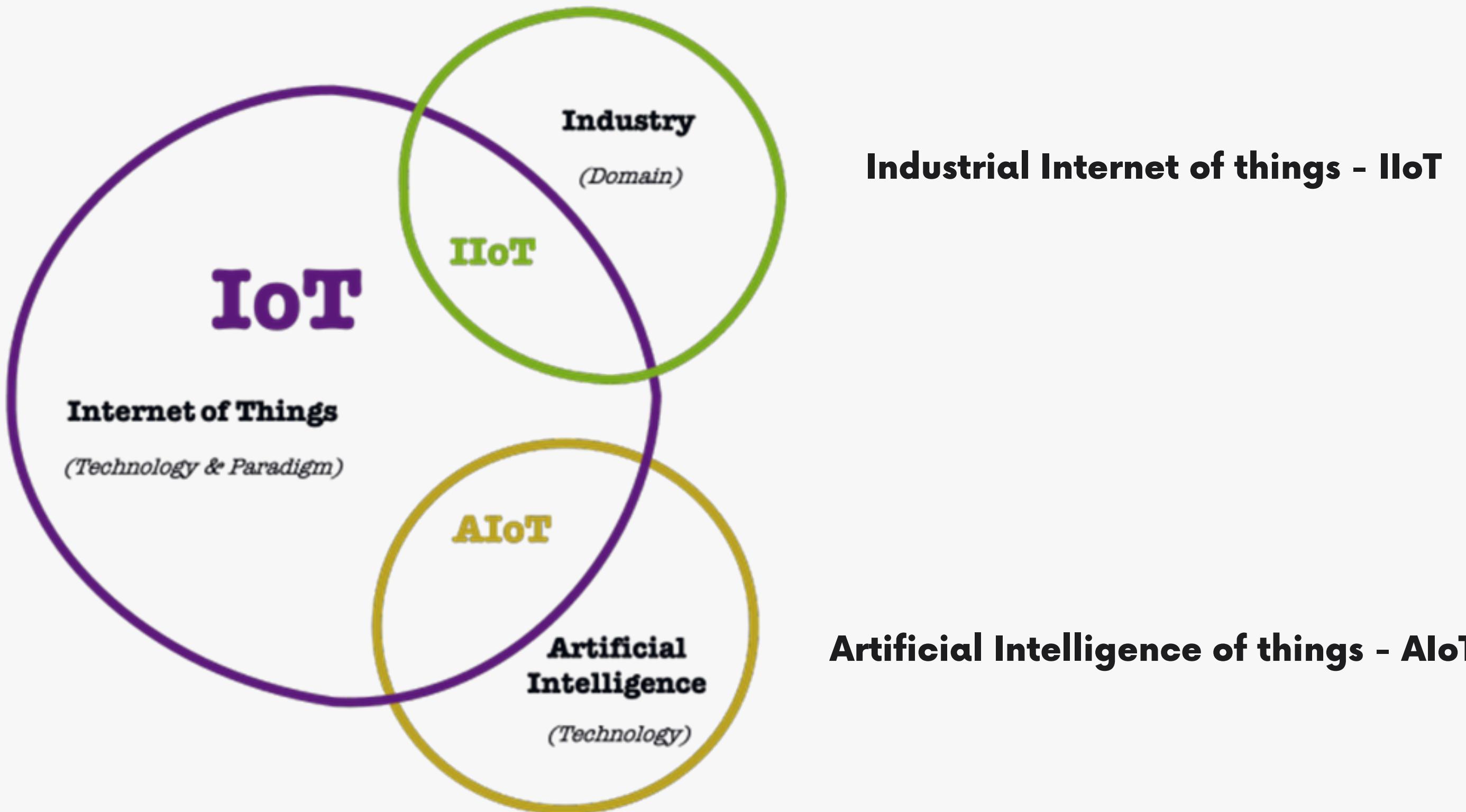
Need diverse skills

Requires longer lead times

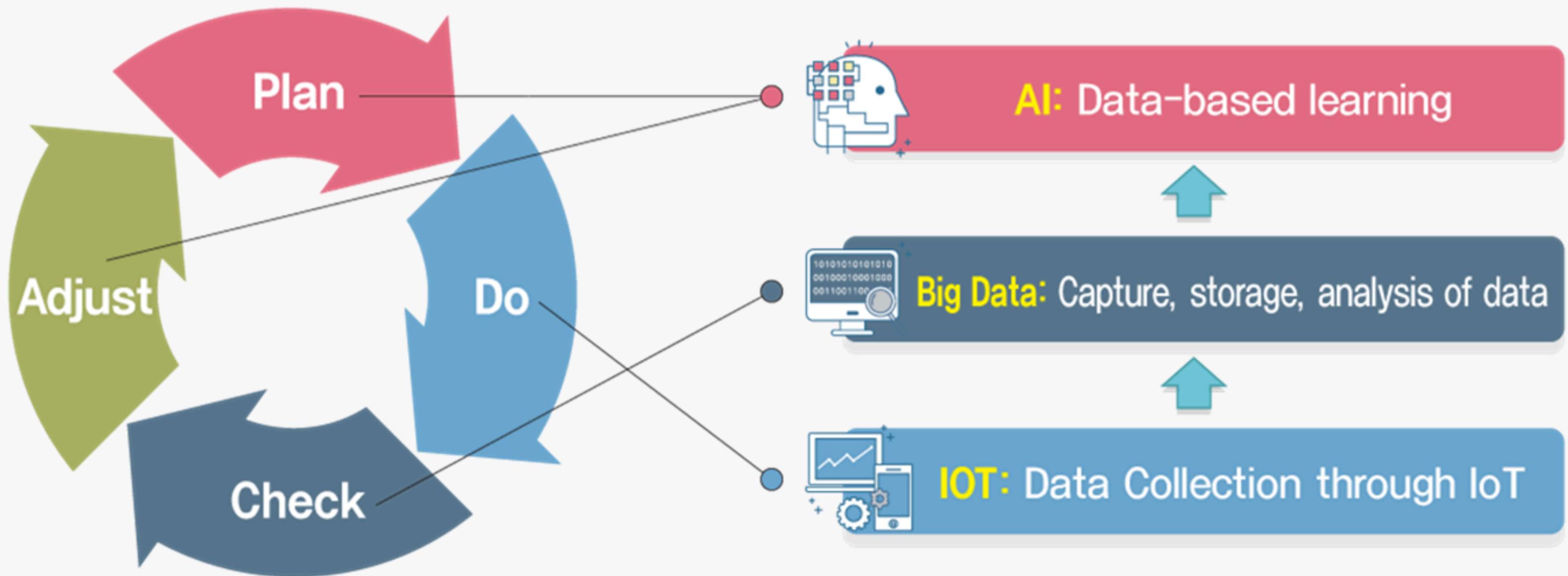
INDUSTRIAL REVOLUTION



INDUSTRIAL REVOLUTION

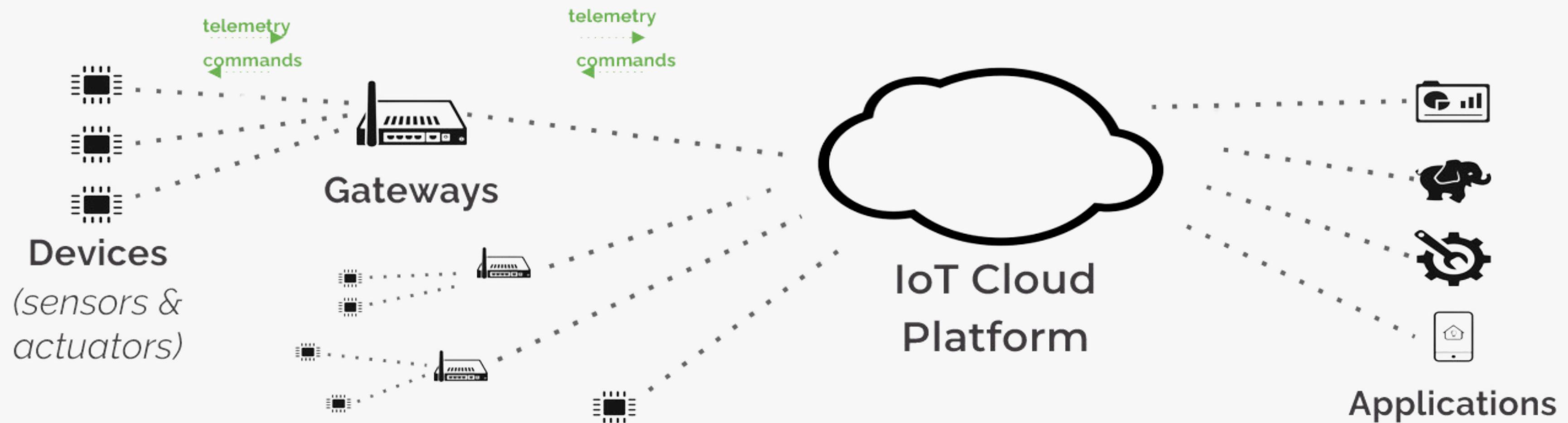


VENDOR LOCK



DEEP DIVE INTO HARDWARE DEVELOPMENT

TYPICAL IOT ARCHITECTURE



IOT STACKS



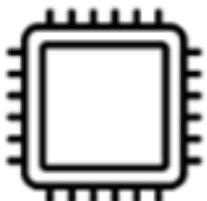
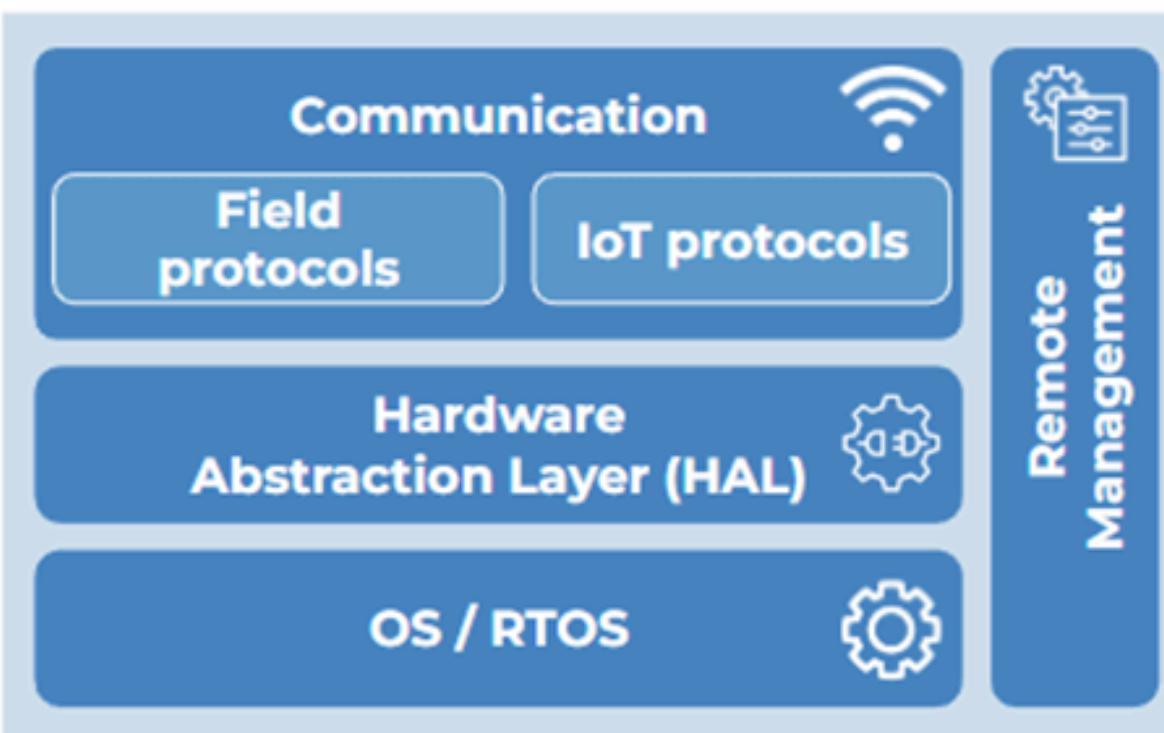
SECURITY



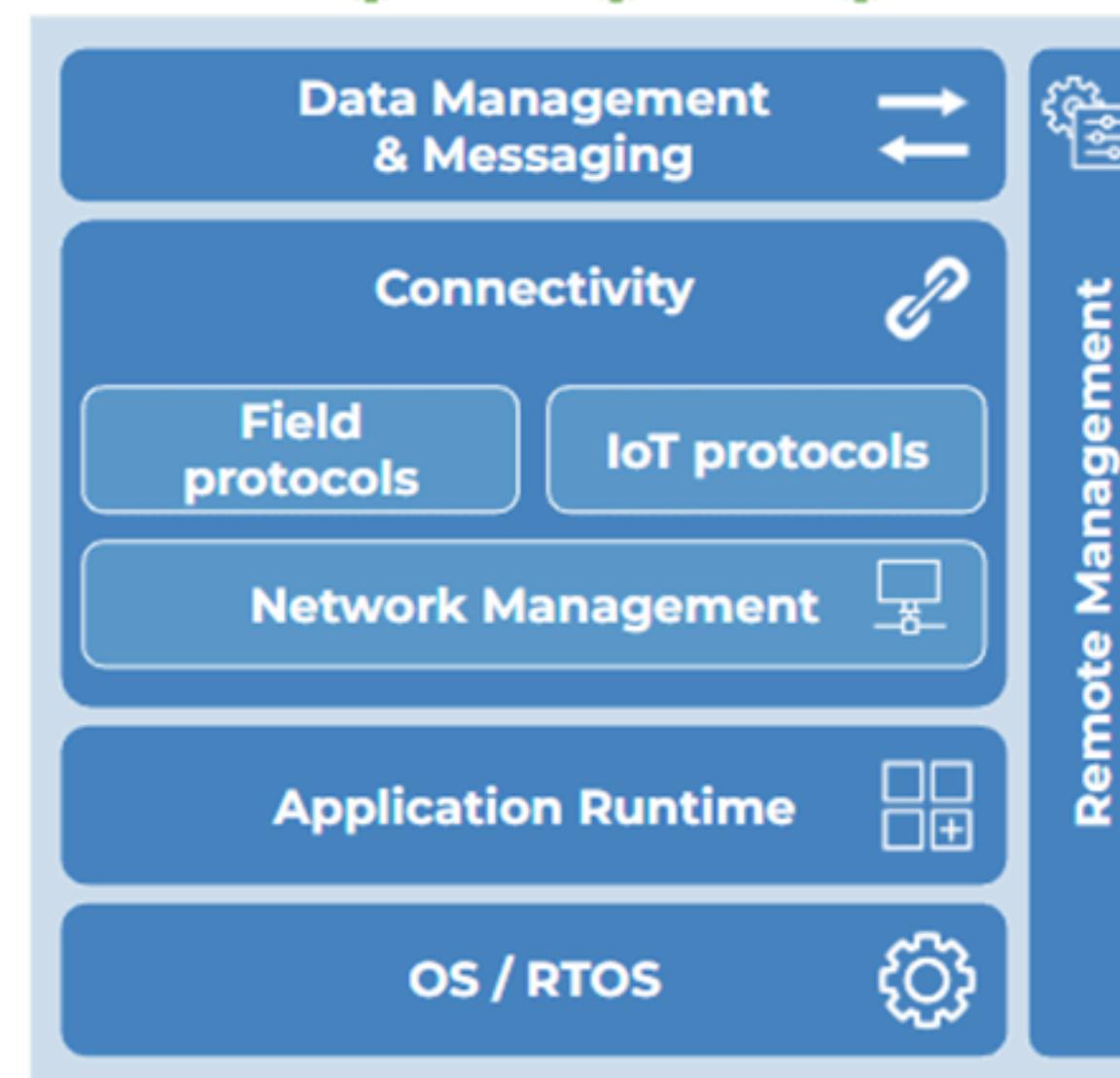
ONTOLOGIES



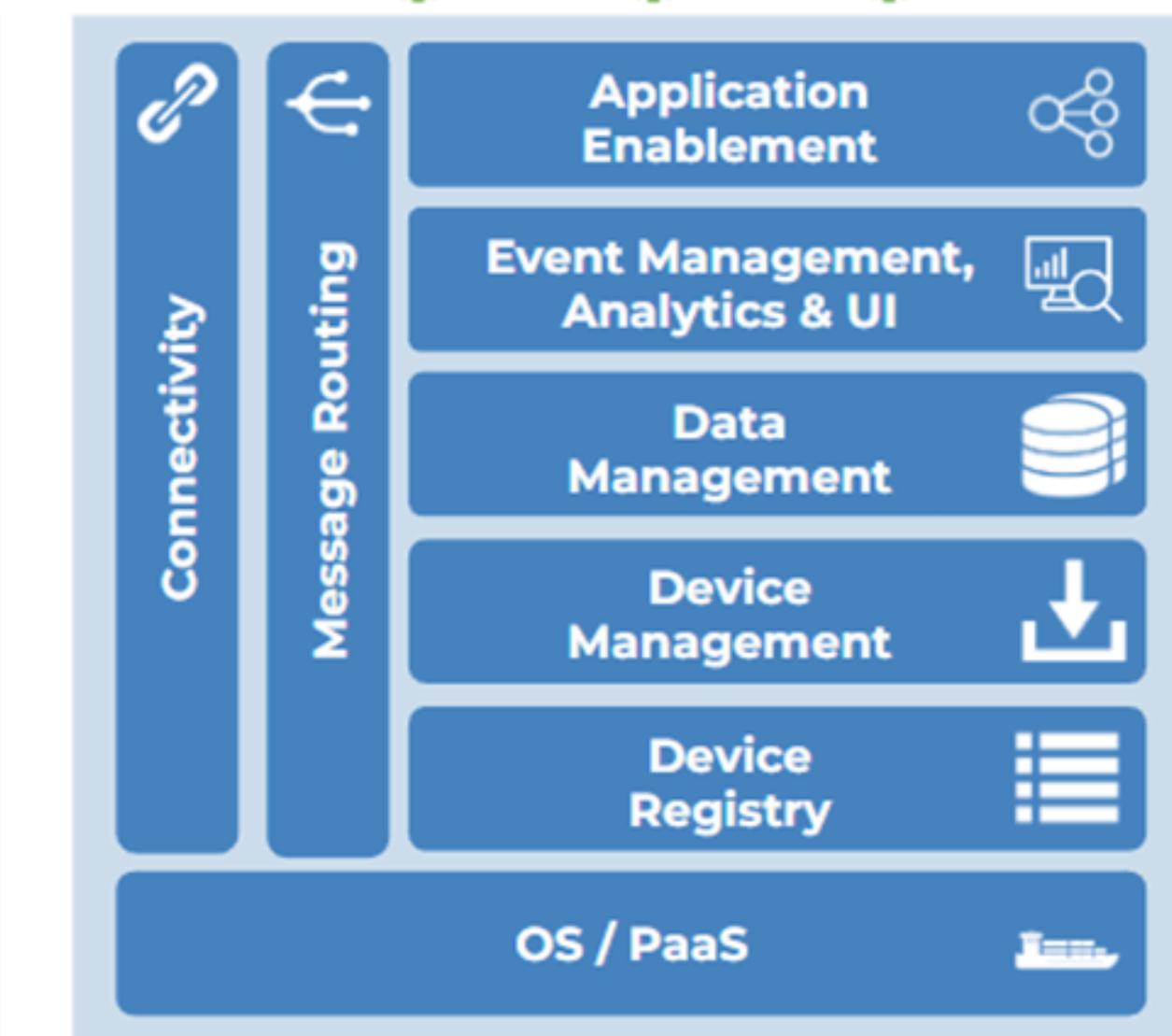
TOOLS & SDKs



CONSTRAINED DEVICES

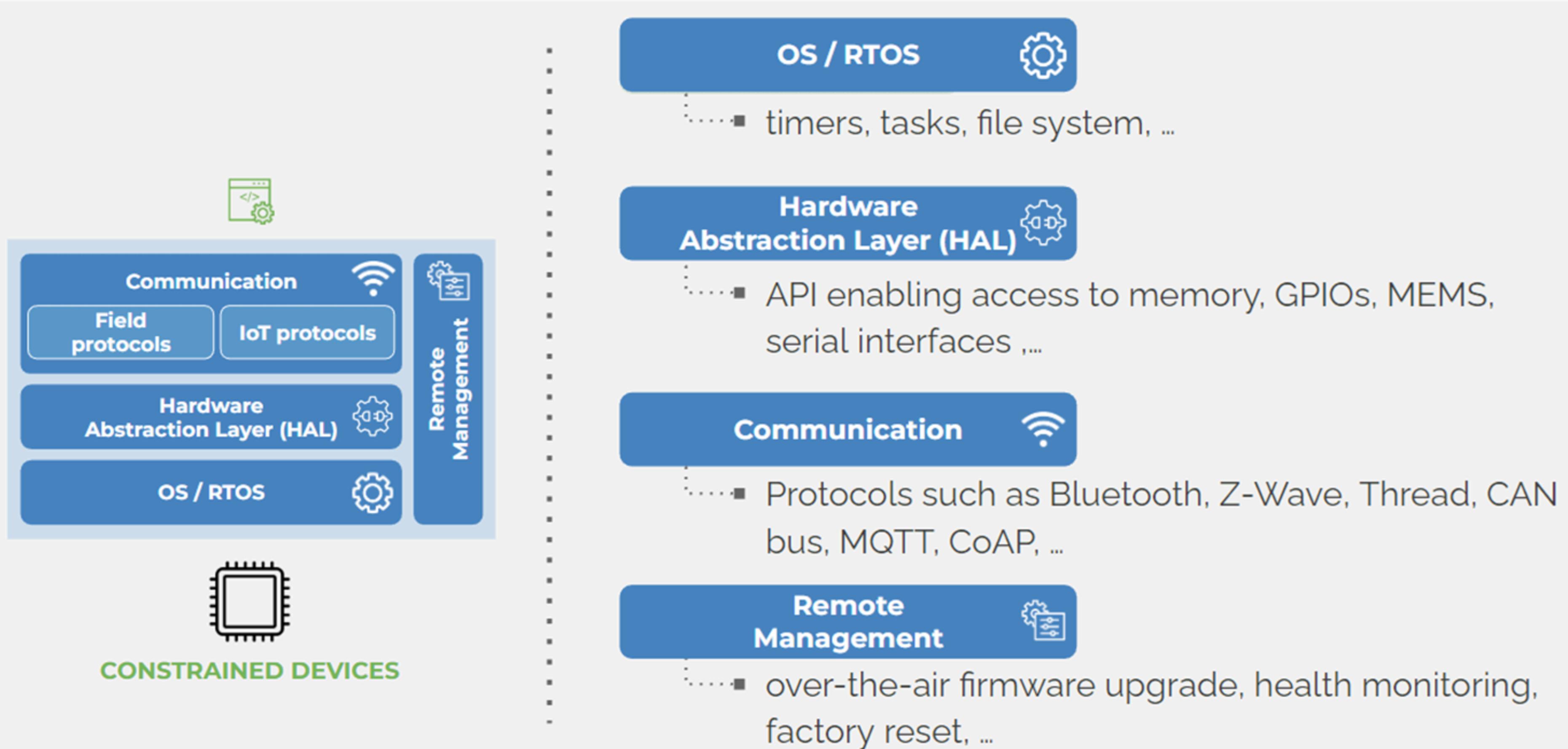


GATEWAYS AND SMART DEVICES

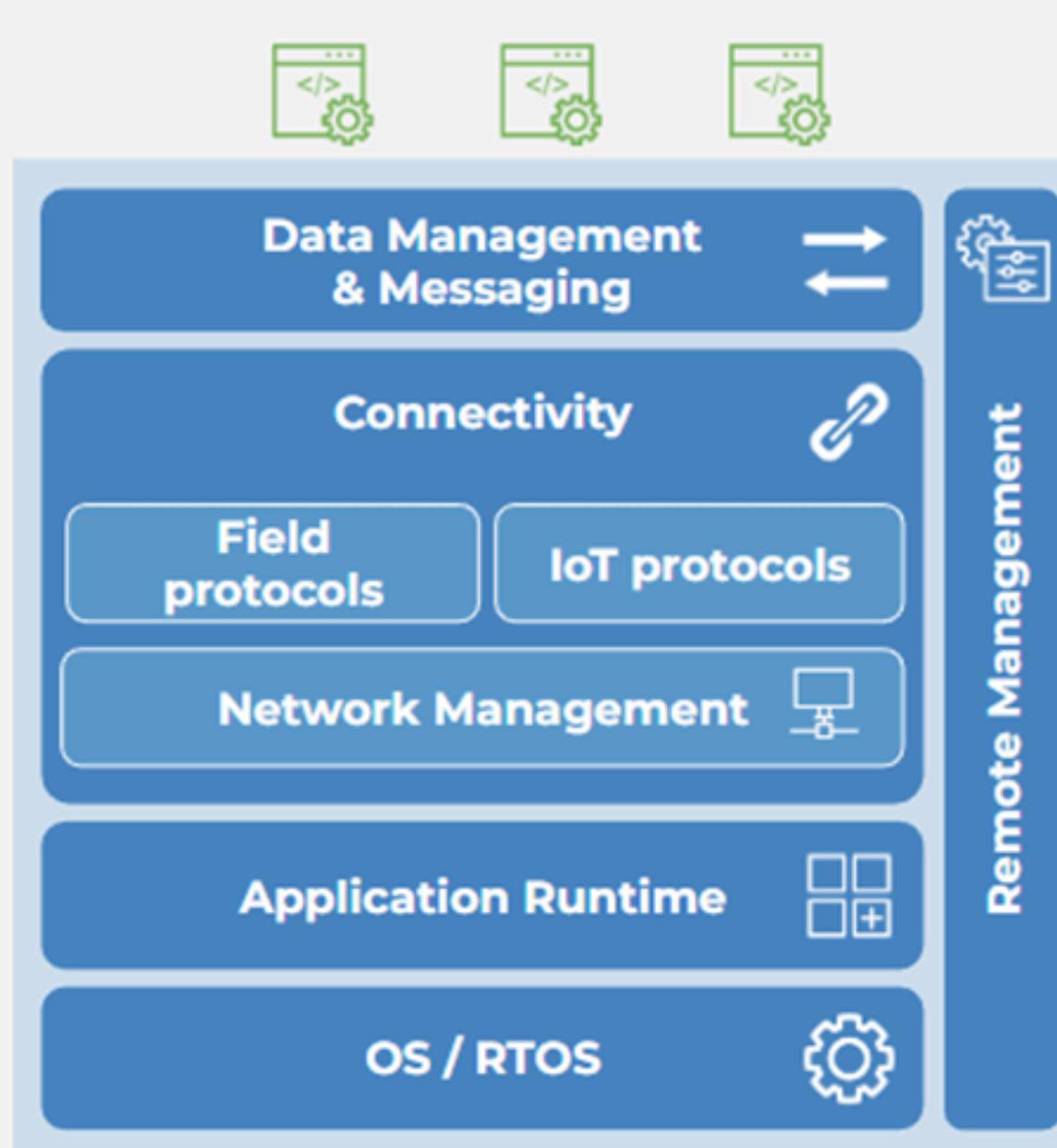


IOT CLOUD PLATFORM

IOT DEVICE STACK



IOT GATEWAY STACK



GATEWAYS AND SMART DEVICES



Application Runtime

- Virtual Machine / Application container

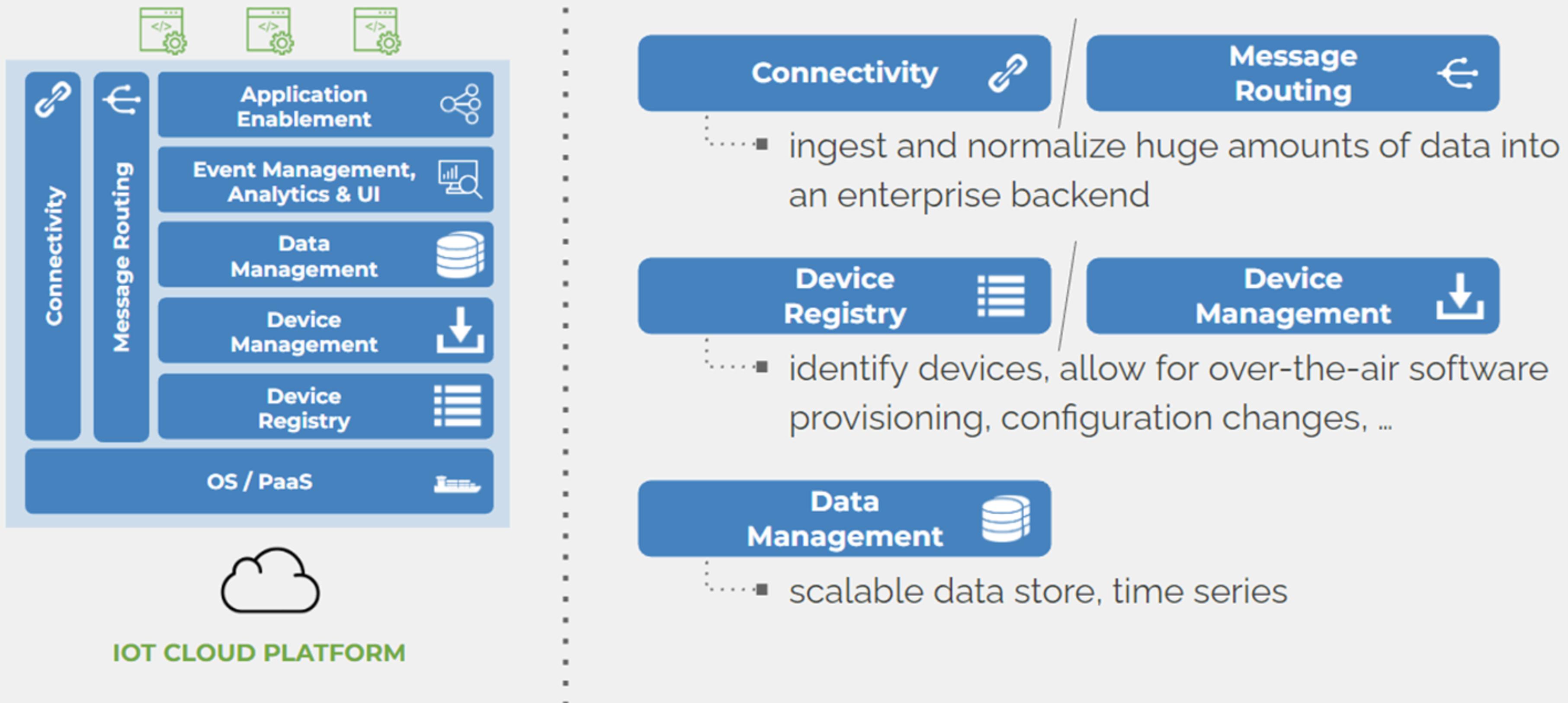
Network Management

- connect to different types of networks
- ensure reliability, security (VPN, firewall, ...)

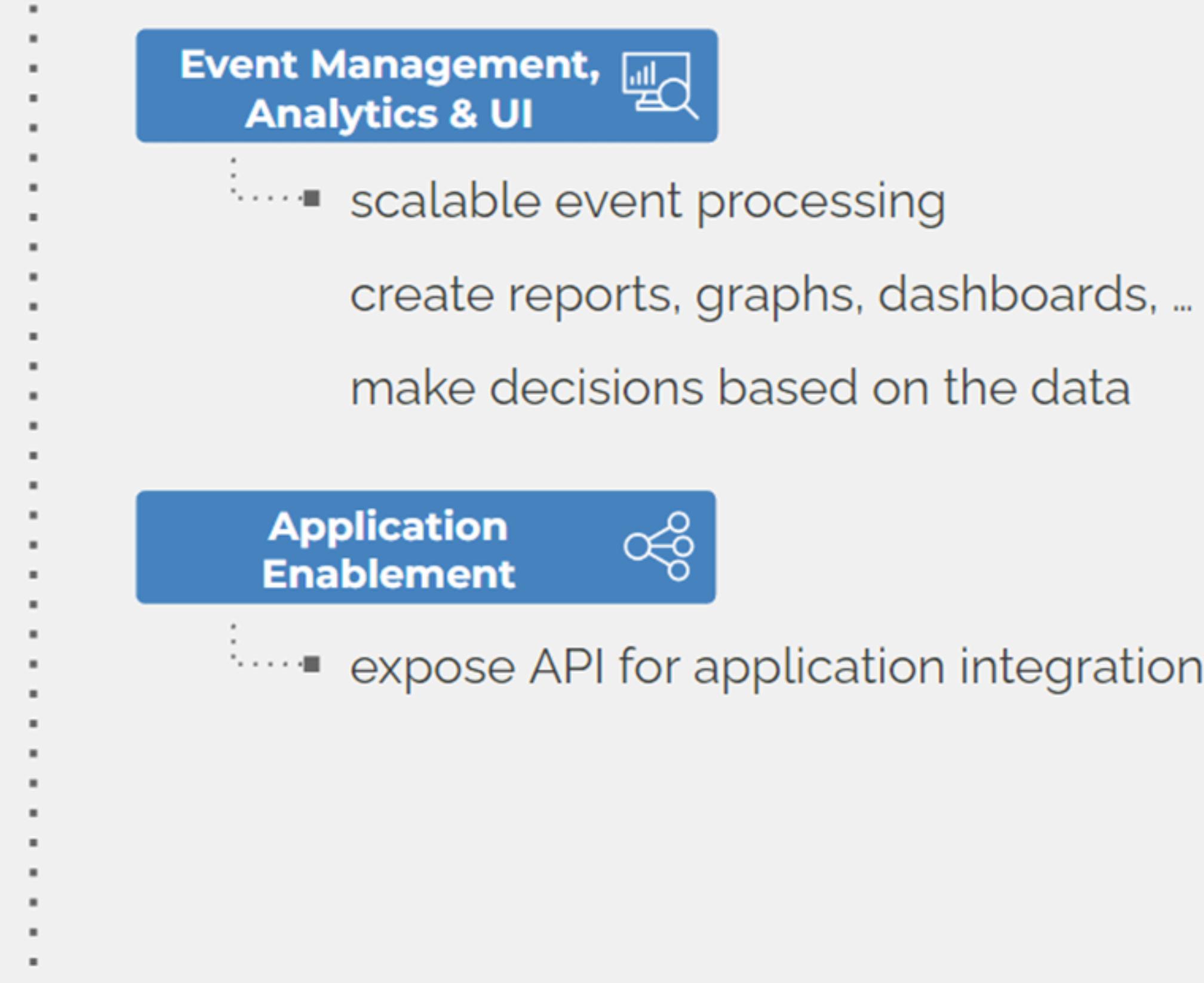
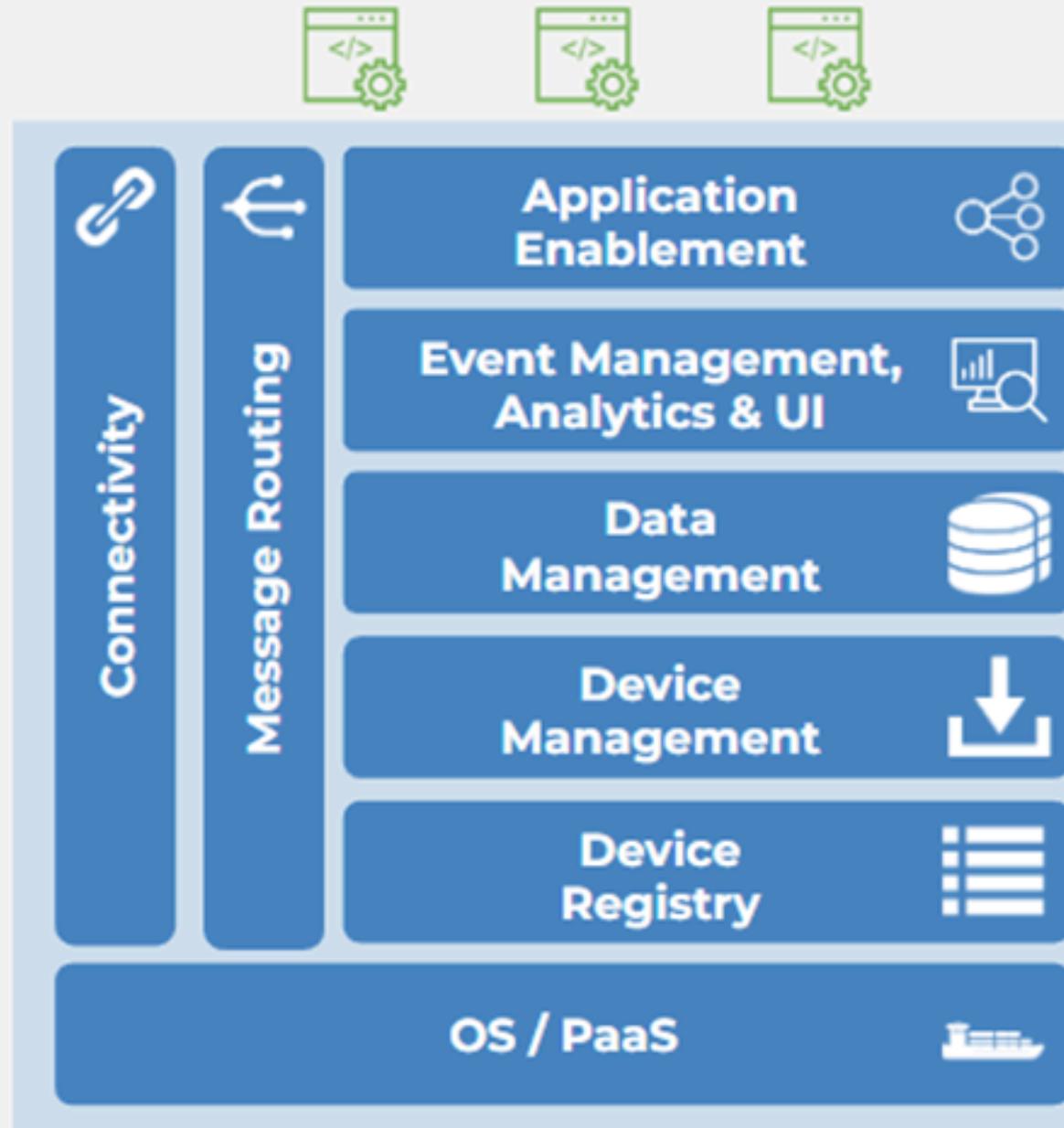
Data Management & Messaging

- local persistence (network latency)
- offline mode
- data analytics at the edge

IOT CLOUD PLATFORM STACK

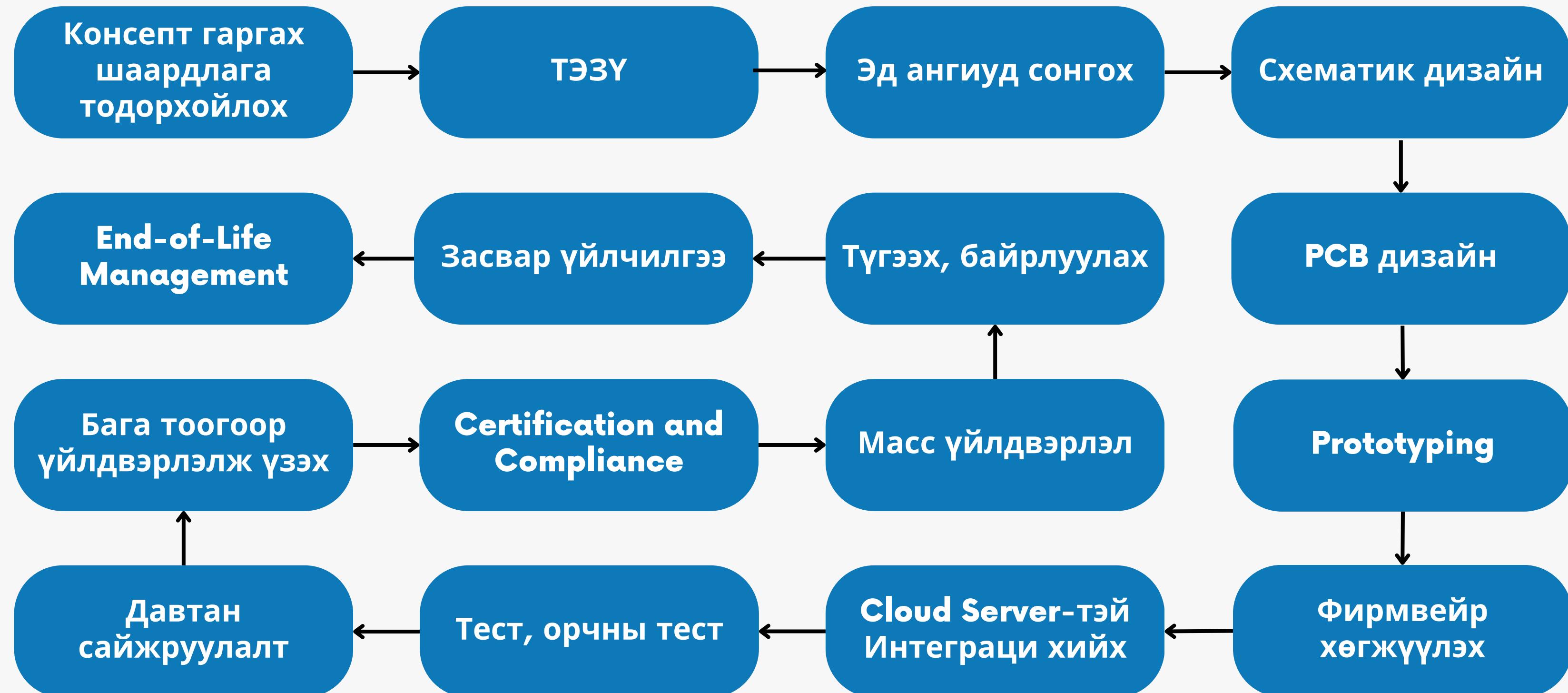


IOT CLOUD PLATFORM STACK

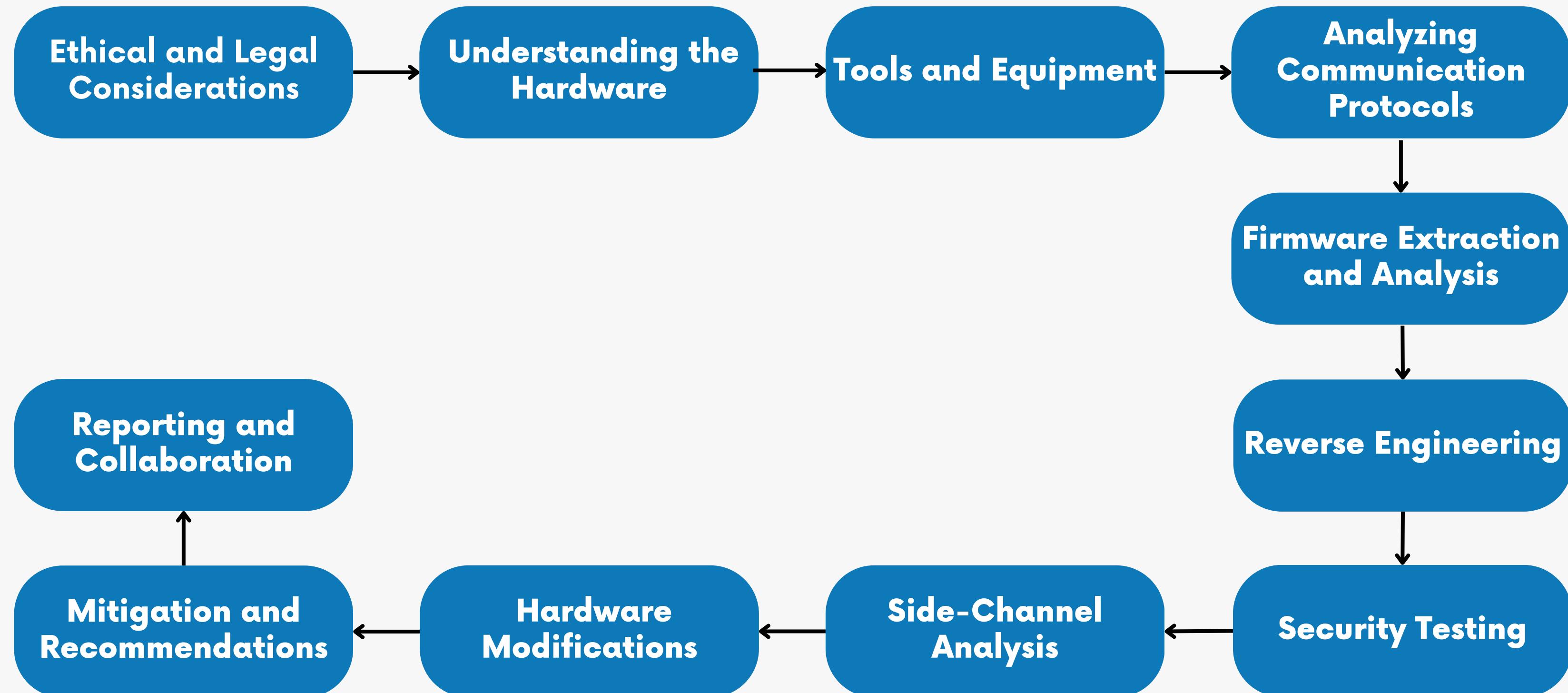


IOT CLOUD PLATFORM

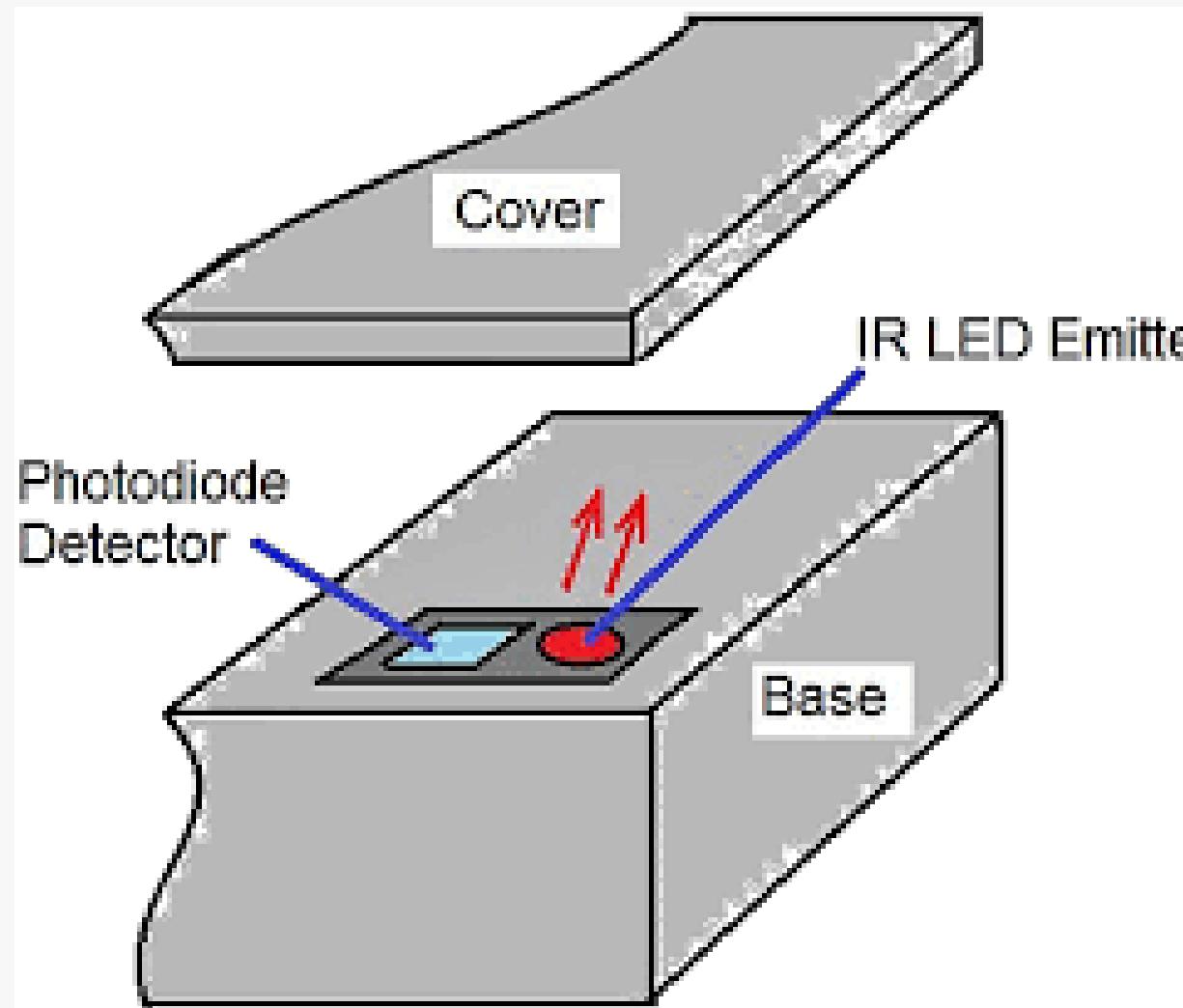
IOT HARDWARE DEVELOPMENT PROCESS



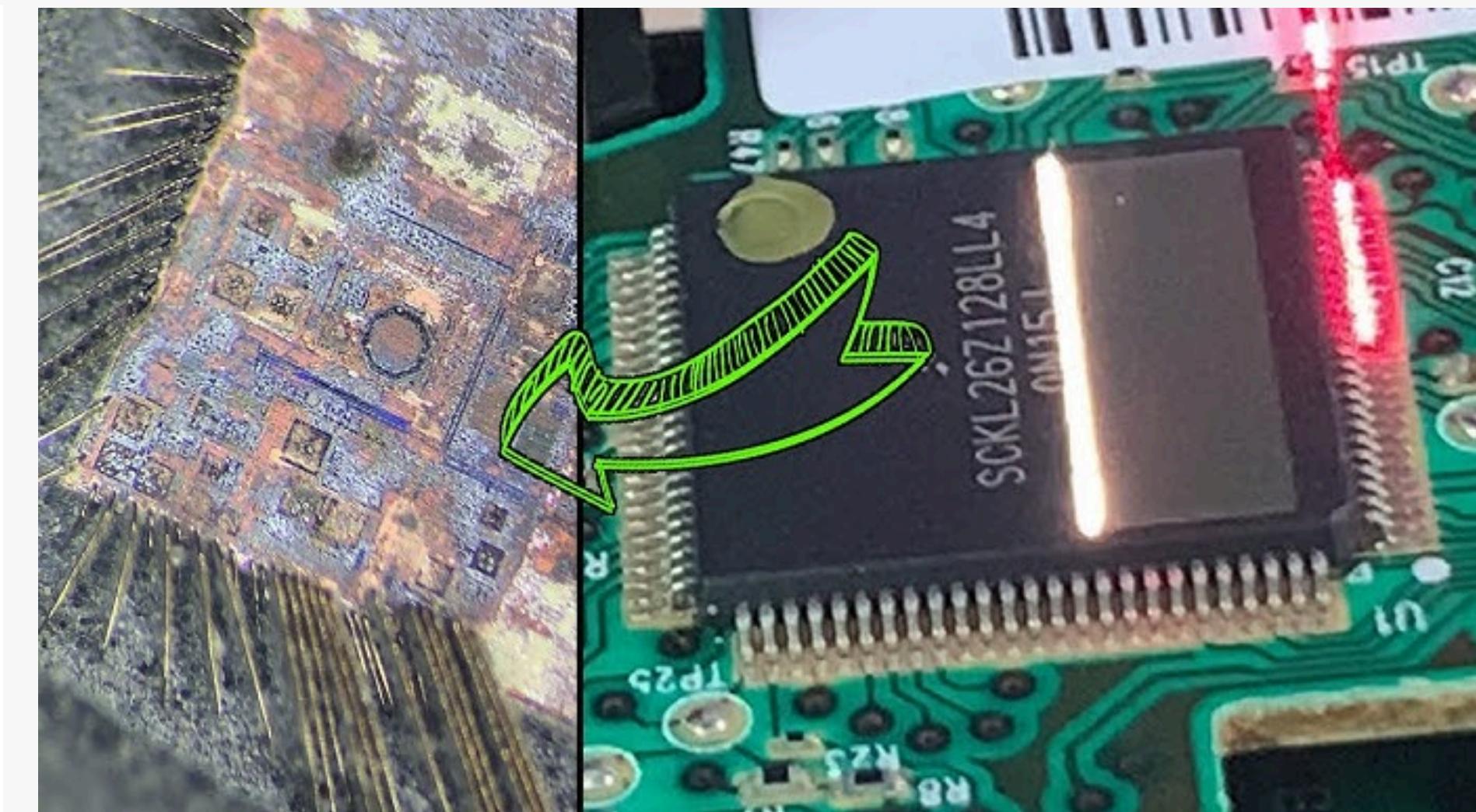
HOW TO HACK A HARDWARE - HANDS ON GUIDE



BEST PRACTICES

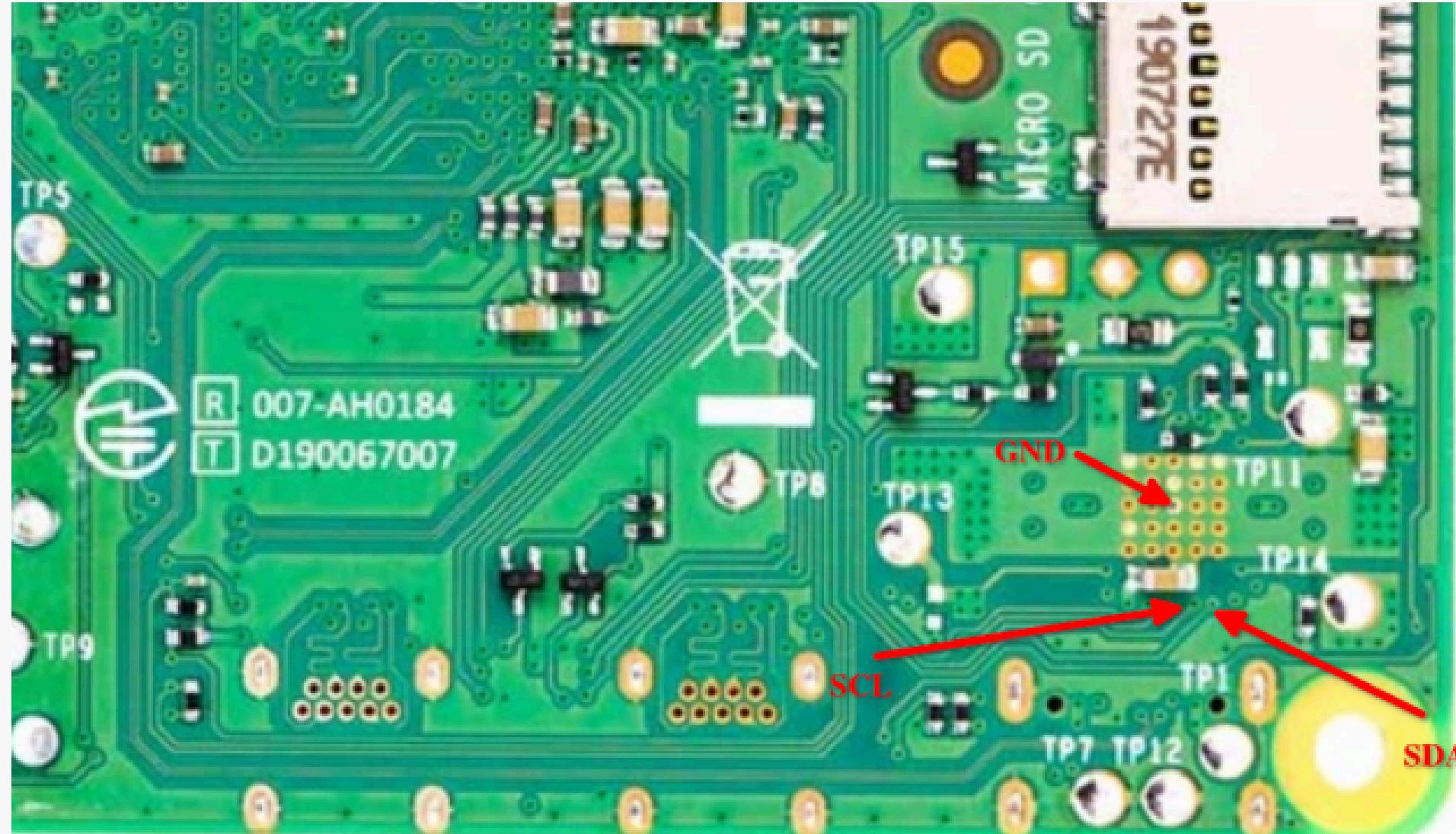


Tamper detection



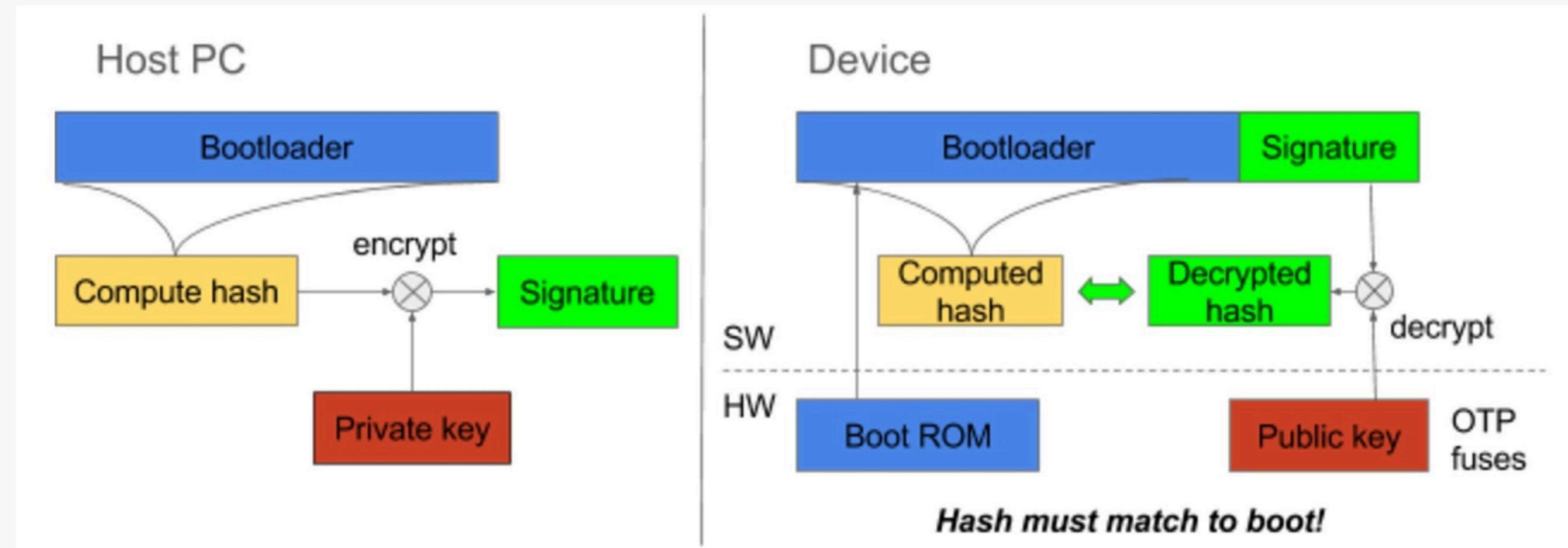
Remove chip mark

BEST PRACTICES



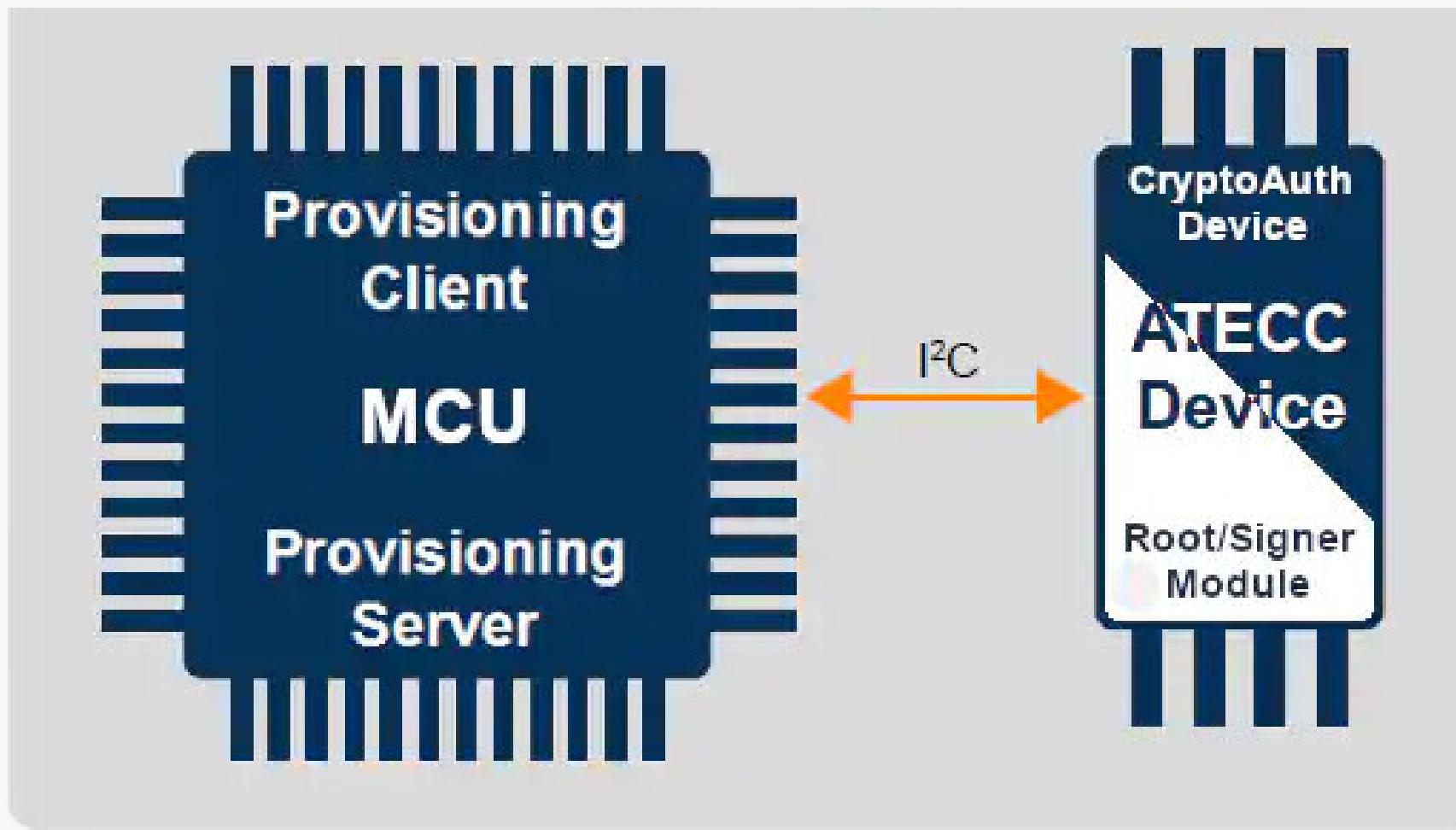
Remove silk screen and test point from PCB Board

BEST PRACTICES



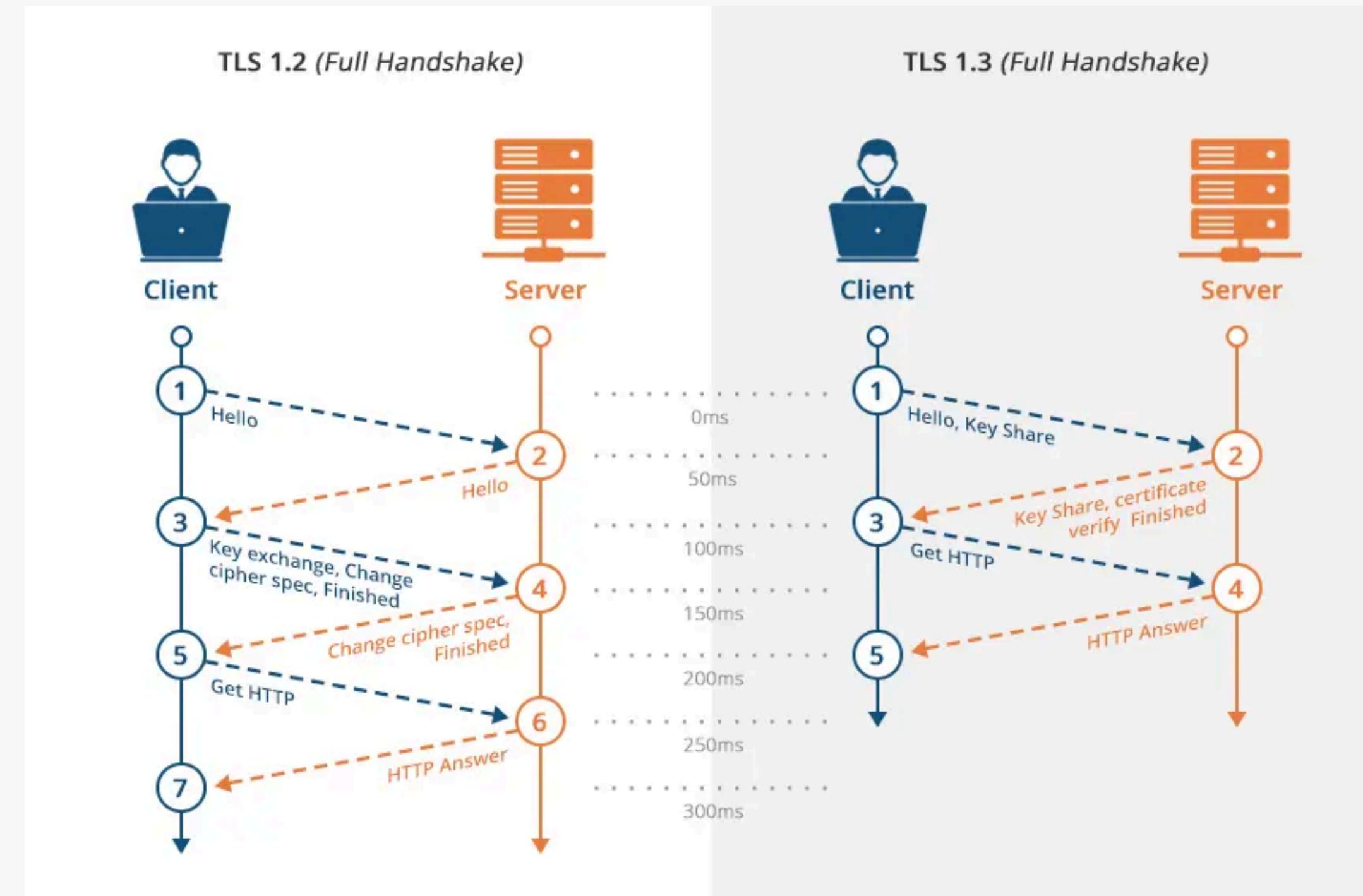
Secure boot and encrypt data storage

BEST PRACTICES



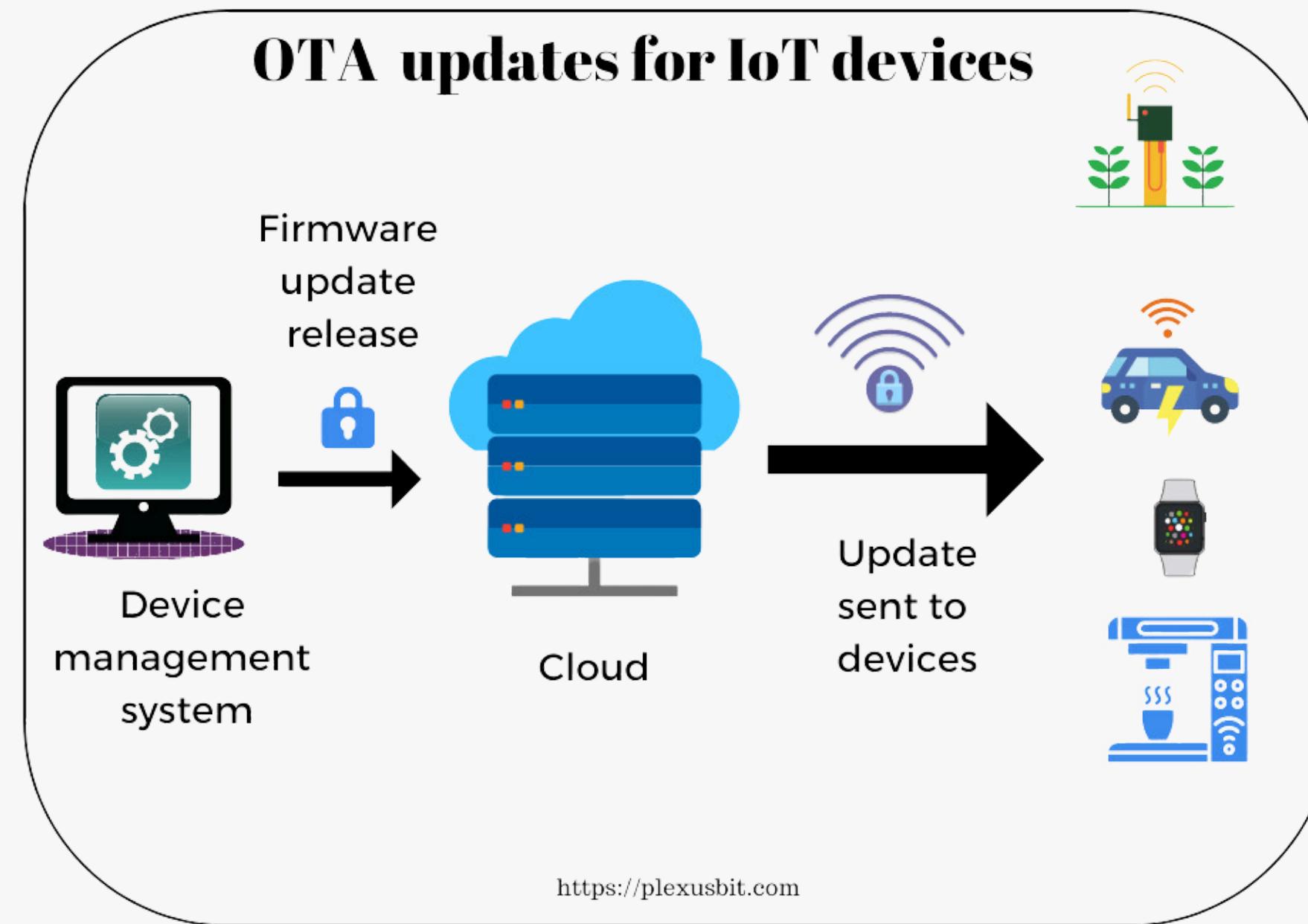
Using crypto Authentication chip

BEST PRACTICES



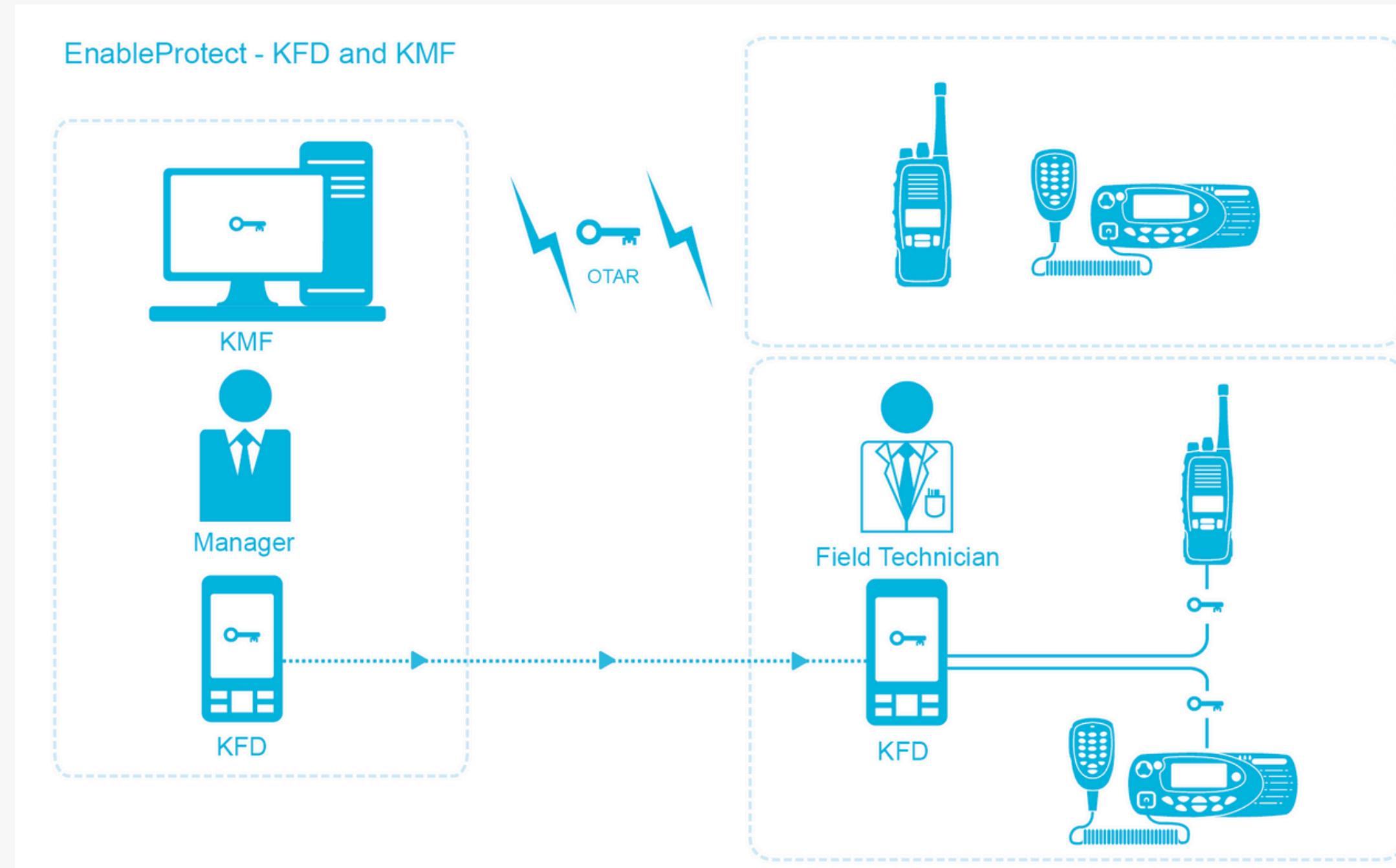
Using secure messaging protocol

BEST PRACTICES



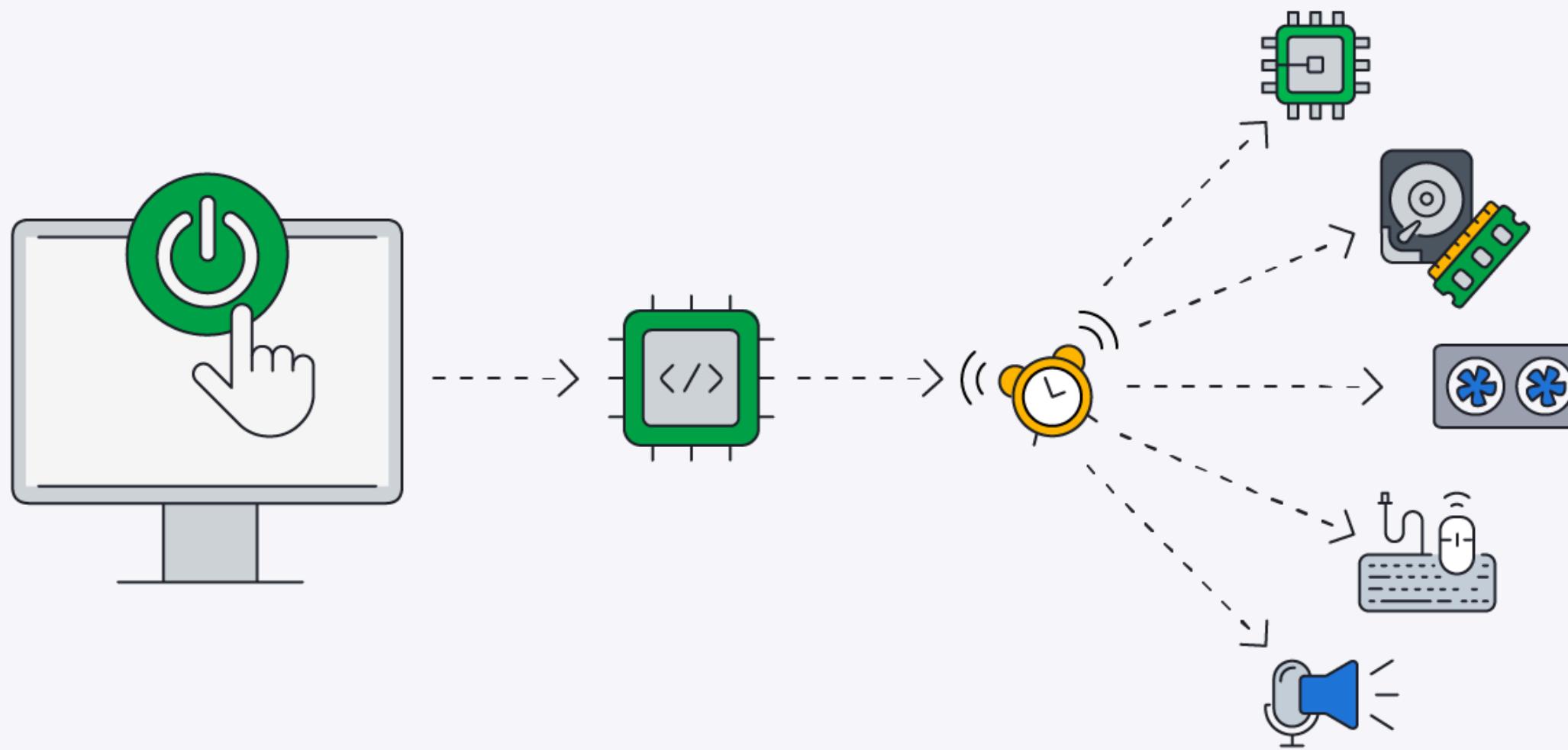
Secure OTA update

BEST PRACTICES



Encrypted Radio Communication Protocol

BEST PRACTICES



**Chip architecture
Peripherals
Interrupts
RTOS
Memory Management
Test & Debug**

THANK YOU

FOR COMING