Introduction to VLSI Design

October 31, 2020

1 Spice Analysis

1.1 DC Operating point

- Netlist for calculating the DC operating point for the given filter.

```
* C:\Users\SAI ASHOK\q1_vlsi1.cir
R1 Vout N001 1000
C1 Vout N002 0.000001
R2 N002 0 100
V1 N001 0 2.5
*control commands
.control
op
print v(vout)
.endc
.end
```

Listing 1: Q1-a.cir

- The Simulated value of V_{out} is 2.5V.

1.2 Phase Differnce using Transient Analysis

- Phase lag introduced at f = 100Hz as observed from simulations is -31.3216°.

- Netlist for calculating the phase lag between input and output at f = 100Hz.

```
* C:\Users\SAI ASHOK\q1_vlsi2.cir
R1 Vout Vin 1000
C1 Vout N001 0.000001
R2 N001 0 100
V1 Vin 0 SINE(0 1 100)
*control commands
.control
tran 0.02 20ms
meas TRAN TIME_1 TRIG V(Vin) VAL=0 CROSS=2 TARG V(Vin) VAL=0 CROSS=4
meas TRAN TIME_2 TRIG V(Vin) VAL=0 CROSS=2 TARG V(Vout) VAL=0 CROSS=2
print 360*(time_2/time_1)
*plot vout vin
wrdata plot1.dat V(Vout)
wrdata plot2.dat V(Vin)
.endc
.end
```

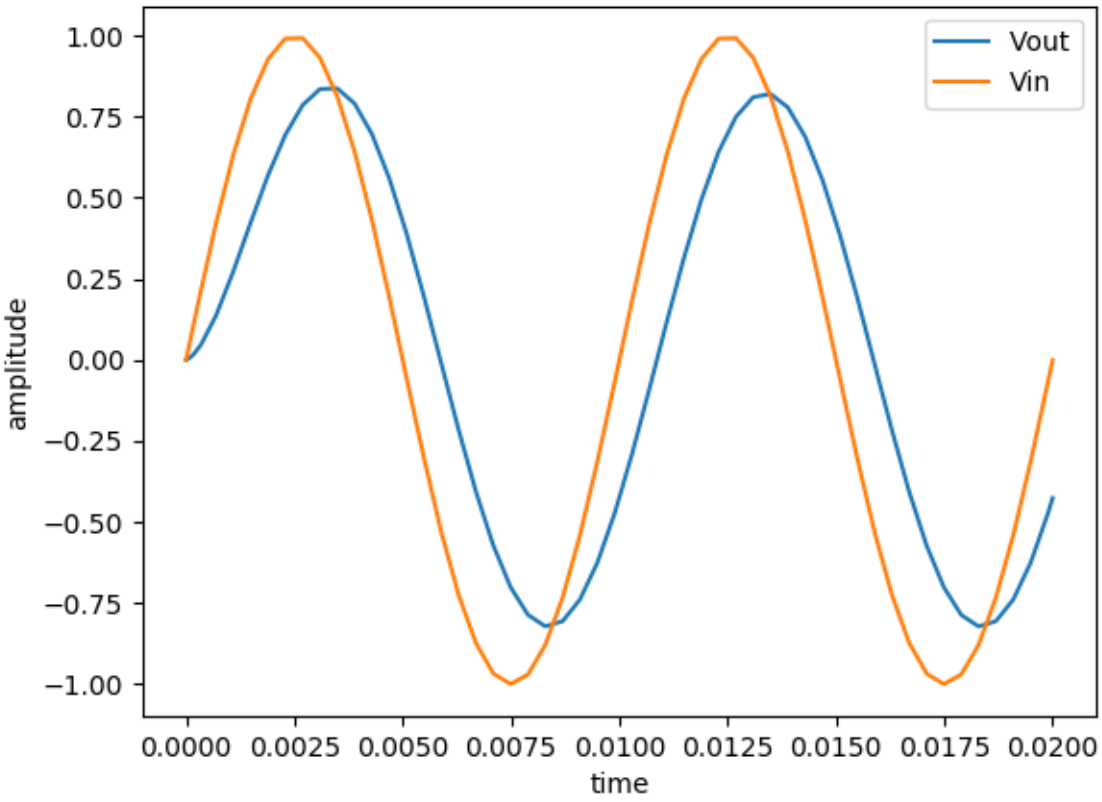

Figure 1: Phase Difference at f=100Hz

Listing 2: Q1-a.cir

- Please refer Figure-1 for the output generated by SPICE simulator.
- Phase lag introduced at f = 1MHz as observed from simulations is -0.165°.
- Netlist for calculating the phase lag between input and output at f = 1MHz.

```
* C:\Users\SAI ASHOK\q1_vlsi2.cir
R1 Vout Vin 1000
C1 Vout N001 0.000001
R2 N001 0 100
V1 Vin 0 SINE(0 1 1000000)
*control commands
.control
tran 2n 0.000002
meas TRAN TIME_1 TRIG V(Vin) VAL=0 CROSS=2 TARG V(Vin) VAL=0 CROSS=4
meas TRAN TIME_2 TRIG V(Vin) VAL=0 CROSS=2 TARG V(Vout) VAL=0 CROSS=2
print 360*(time_2/time_1)
*plot vout vin
wrdata plot1.dat V(Vout)
```

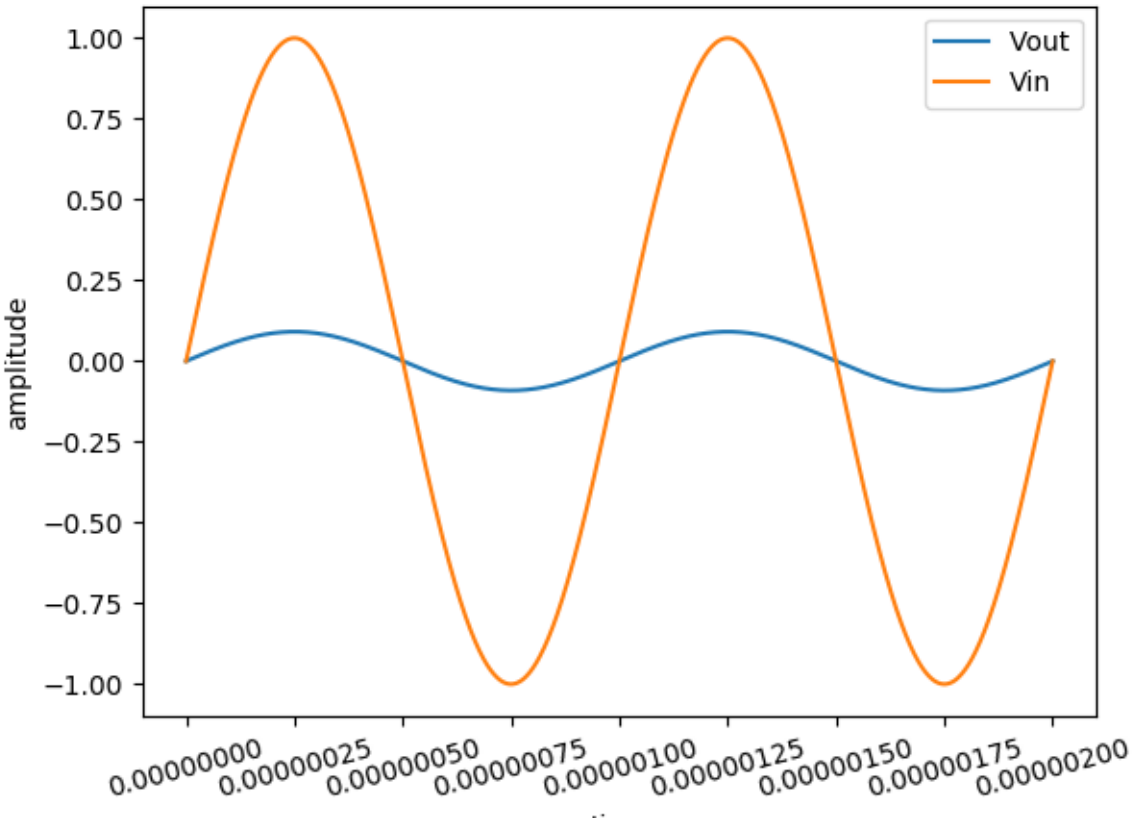

Figure 2: Phase Difference at f=1MHz

```
wrdata plot2.dat V(Vin)
.endc
.end
```

Listing 3: Q1-a.cir

- Please refer Figure-2 for the output generated by SPICE simulator.

1.3 Characteristics of Transfer Function

- Netlist used for simulating Amplitude and Phase characteristics of the given RC circuit.

```
* C:\Users\SAI ASHOK\q1_vlsi3.cir
R1 Vout Vin 1000
C1 Vout N001 0.000001
R2 N001 0 100
V1 Vin 0 dc 0 ac 1
.control
ac dec 10 0.1 1000000
run
*Magnitude of output on log scale
wrdata plot1.dat db(vout/vin) xlog
*plot db(vout/vin) xlog
```

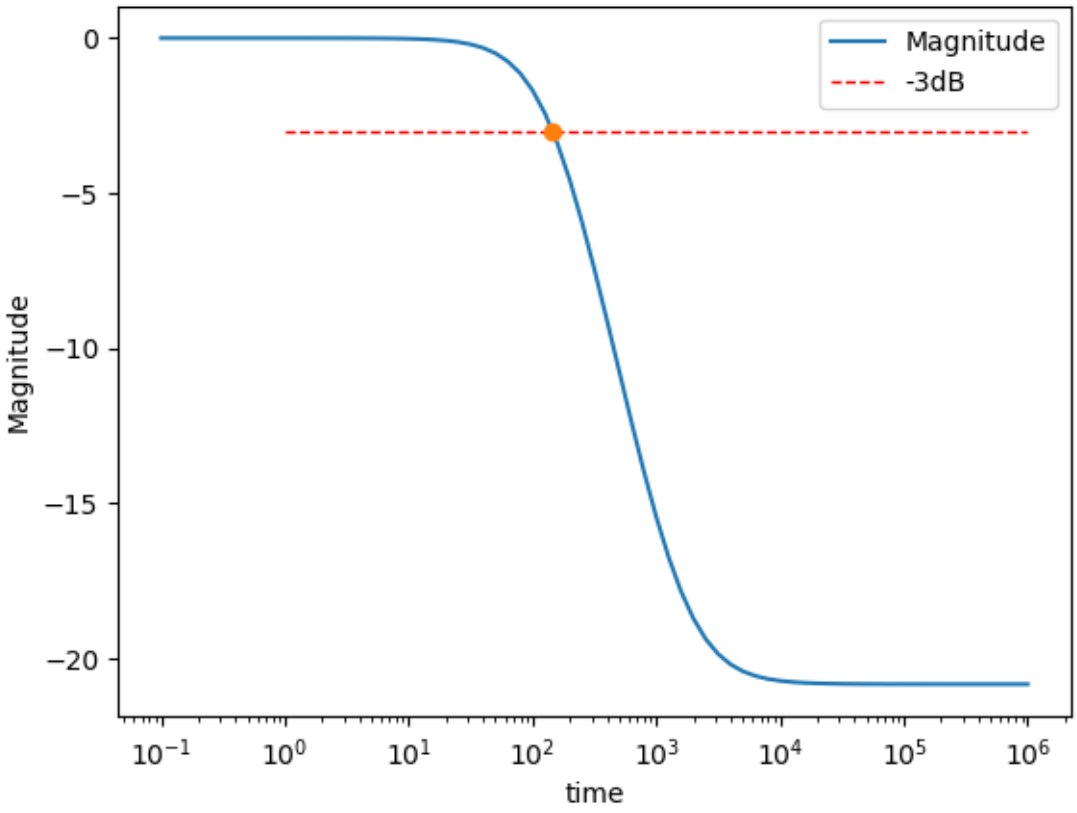

Figure 3: Magnitude Response

```
*Phase of output on log scale
wrdata plot2.dat {180/3.14*phase(vout/vin)} xlog
*plot {180/3.14*phase(vout/vin)} xlog
.endc
.end
```

Listing 4: Q1-a.cir

- The phase corresponding to -3dB is -40°(approx) as observed from simulations.
- Please refer Figure-3 and Figure-4 for Magnitude and Phase plots of Transfer function.

2 SPICE simulation for diode circuit

2.1 Simulation

- Netlist for simulating the diode taking $I_s = 10^{-14}$.

```
* C:\Users\SAI ASHOK\q2_vlsi1.cir
.model DMOD D
D1 N002 P001 DMOD
R1 N001 N002 2000
V1 N001 0 2.5
```

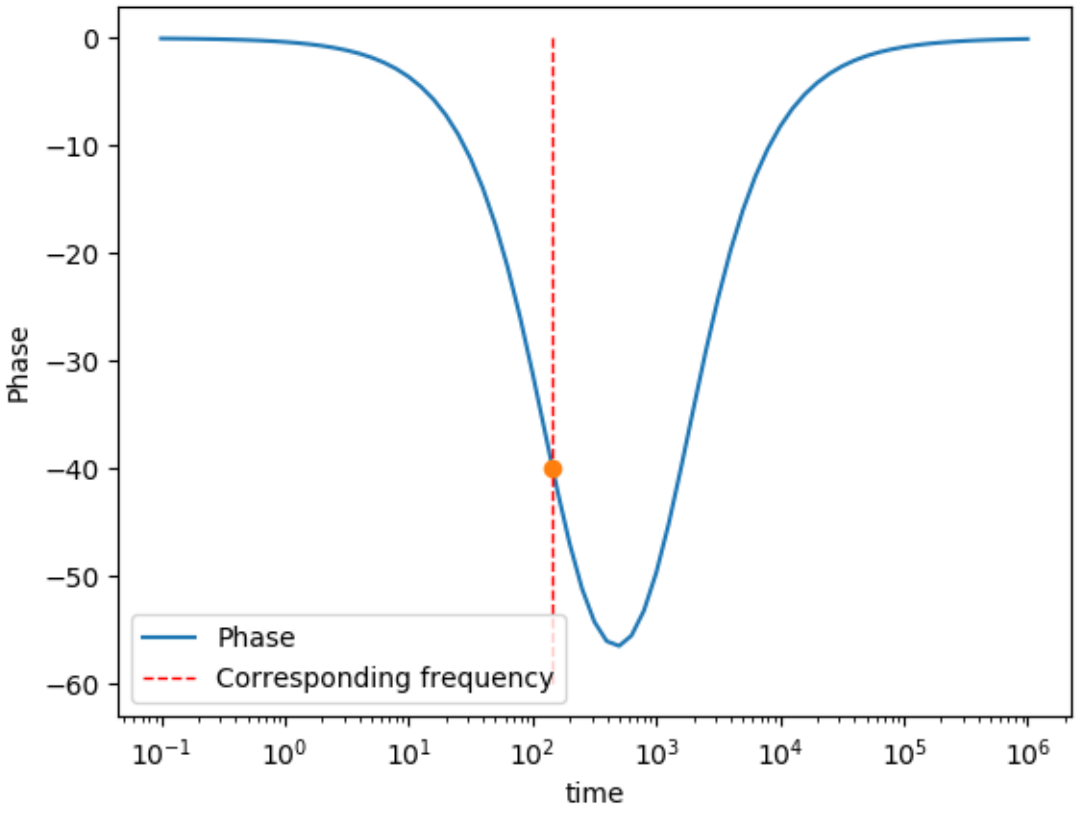

Figure 4: Phase Response

```
R2 P001 N003 2000
D2 N003 0 DMOD
.op
.control
run
*display
print i(v1)
.endc
.end
```

Listing 5: Q1-a.cir

- Value of I_d from simulations is -3.12e-04 and voltage across diode comes out to be 0.625V.

3 Controlled Sources

- Netlist for simulating the given circuit consisting of a VCCS.

```
* C:\Users\SAI ASHOK\q3_vlsi1.cir
G1 0 Vout N001 0 1000000
R1 Vin N001 1000
R2 Vout N001 3000
V1 0 Vin SINE(0 0.5 1000)
R3 Vout 0 1
.control
tran 50u 5m
run
*plot Vout Vin
wrdata plot1.dat Vout
wrdata plot2.dat Vin
.endc
.end
```

Listing 6: Q1-a.cir

- Gain is observed to be -3 from the simulations.
- Please refer Figure-5 for the simulated output.

4 MOSFET characteristics

4.1 I_d vs V_{ds}

- Netlist for simulating a Short Channel nmos.

```
* C:\Users\SAI ASHOK\q4_vlsi1.cir
.include "C:\Users\SAI ASHOK\TSMC180.lib"
.model nch_tt nmos

```

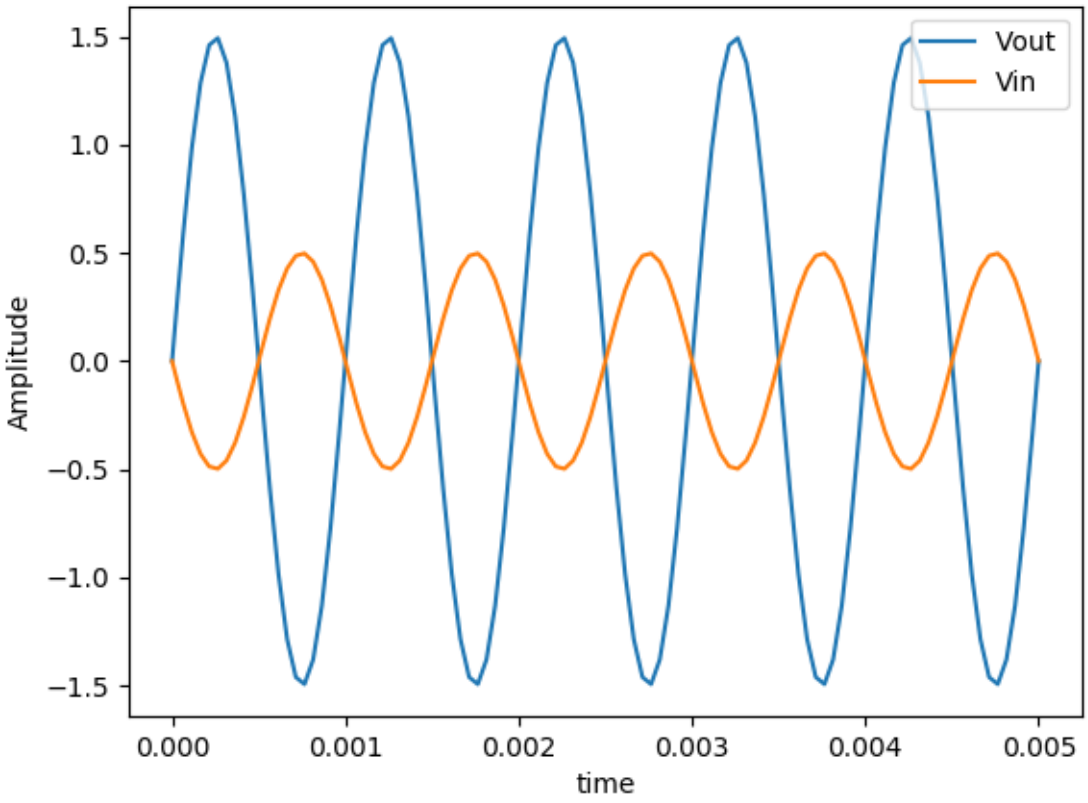

Figure 5: VCCS

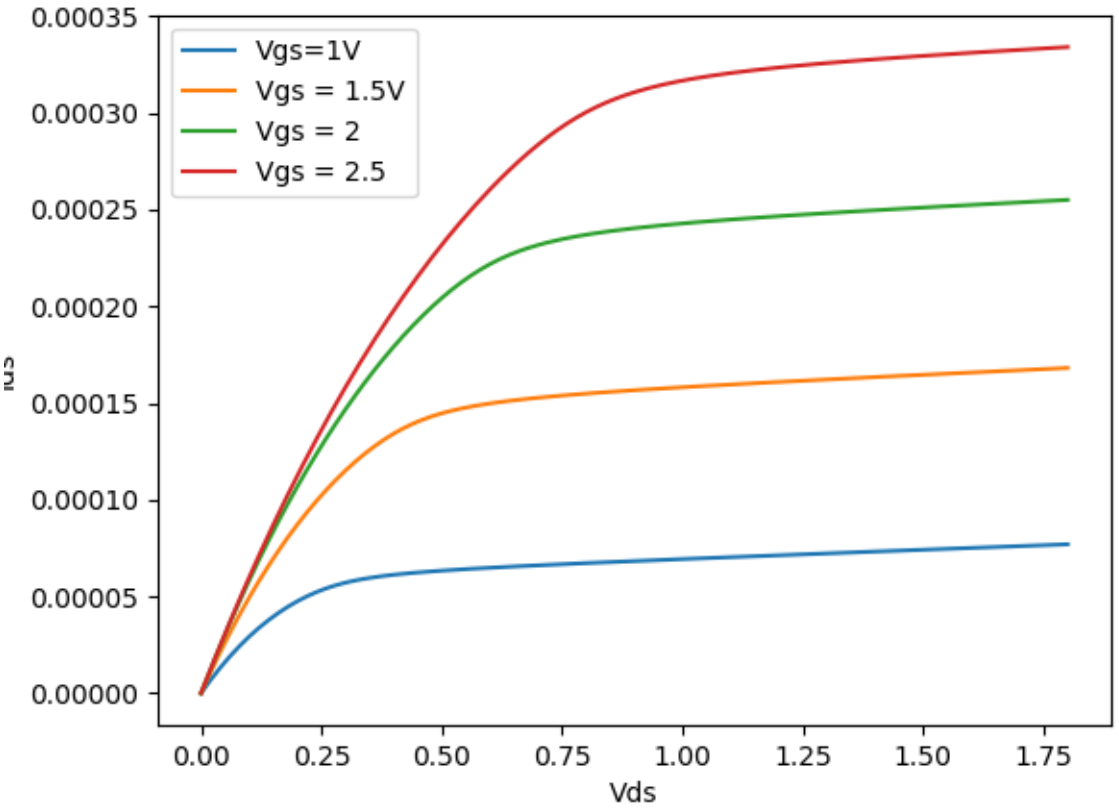

Figure 6: Short Channel nmos characteristics

```
*M1 ds gs 0 0 nch_tt W=15u L=10u
M1 ds gs 0 0 nch_tt W=0.27u L=0.18u
V1 ds 0 DC 0
V2 gs 0 DC 1
.dc V1 0 1.8 0.01
.control
run
*plot -i(v1) vs v(ds)
wrdata plot1.dat -i(v1) vs v(ds)
.endc
.end
```

Listing 7: Q1-a.cir

- Please refer Figure-6 for simulated output.
- Netlist for simulating a Long Channel nmos.

```
* C:\Users\SAI ASHOK\q4_vlsi1.cir
.include "C:\Users\SAI ASHOK\TSMC180.lib"
.model nch_tt nmos

M1 ds gs 0 0 nch_tt W=15u L=10u
*M1 ds gs 0 0 nch_tt W=0.27u L=0.18u
```

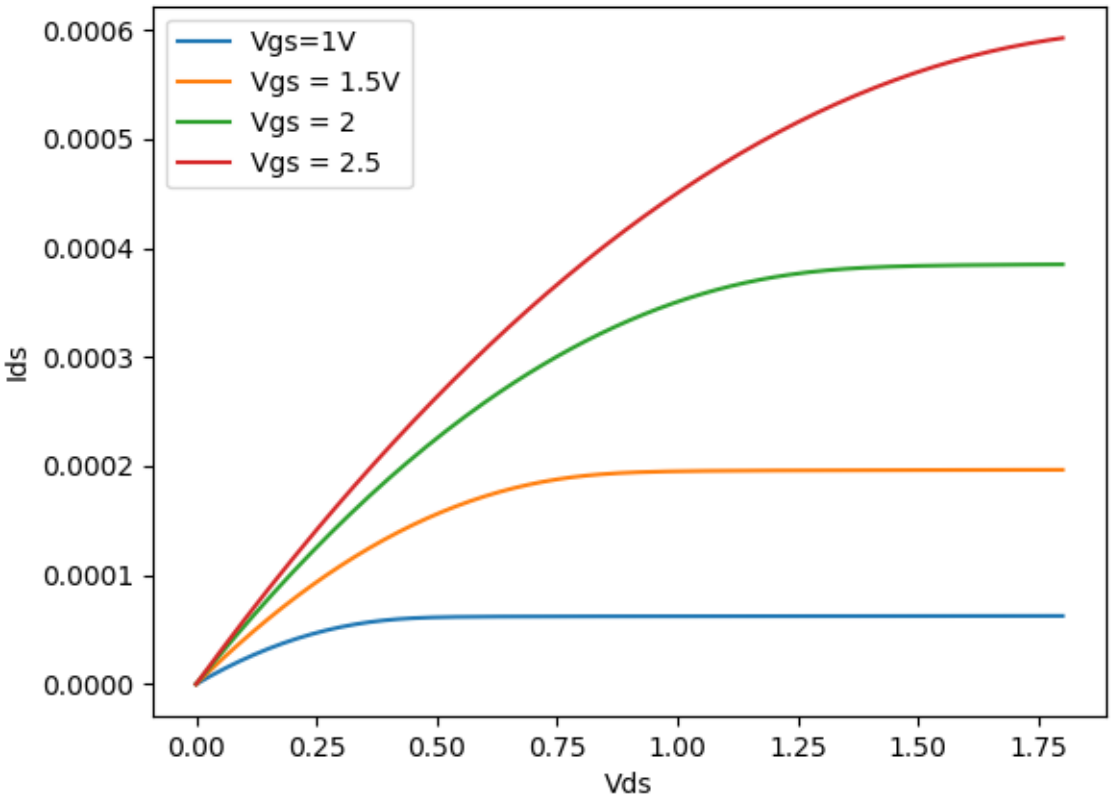

Figure 7: Long Channel nmos characteristics

```
V1 ds 0 DC 0
V2 gs 0 DC 1
.dc V1 0 1.8 0.01
.control
run
*plot -i(v1) vs v(ds)
wrdata plot1.dat -i(v1) vs v(ds)
.endc
.end
```

Listing 8: Q1-a.cir

- Please refer Figure-7 for simulated output.
- Netlist for simulating a Short Channel pmos.

```
* C:\Users\SAI ASHOK\q4_vlsi1.cir
.include "C:\Users\SAI ASHOK\TSMC180.lib"
.model pch_tt pmos

*M1 ds gs 0 0 nch_tt W=15u L=10u
M1 ds gs 0 0 nch_tt W=0.27u L=0.18u
V1 ds 0 DC 0
V2 gs 0 DC -1
```

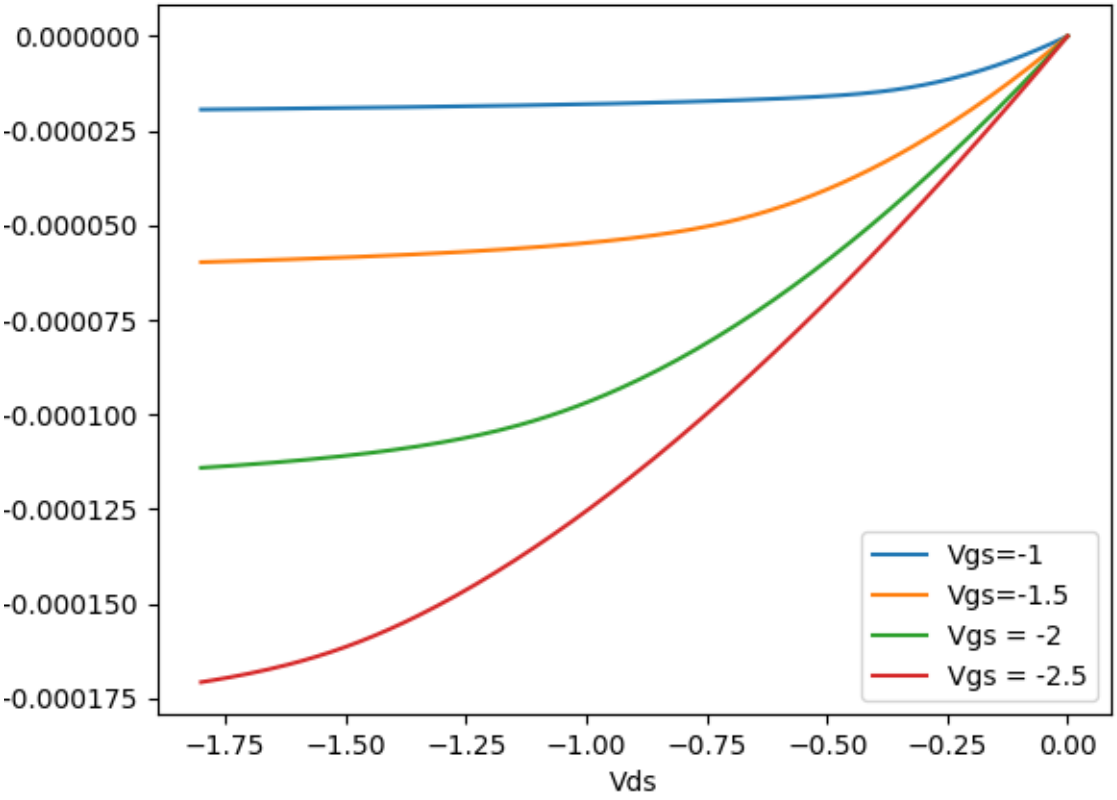

Figure 8: Short Channel pmos characteristics

```
.dc V1 0 -1.8 -0.01
.control
run
*plot -i(v1) vs v(ds)
wrdata plot1.dat -i(v1) vs v(ds)
.endc
.end
```

Listing 9: Q1-a.cir

- Please refer Figure-8 for simulated output.
- Netlist for simulating a Long Channel pmos.

```
* C:\Users\SAI ASHOK\q4_vlsi1.cir
.include "C:\Users\SAI ASHOK\TSMC180.lib"
.model pch_tt pmos

M1 ds gs 0 0 pch_tt W=15u L=10u
*M1 ds gs 0 0 pch_tt W=0.27u L=0.18u
V1 ds 0 DC 0
V2 gs 0 DC -1
.dc V1 0 -1.8 -0.01
.control
```

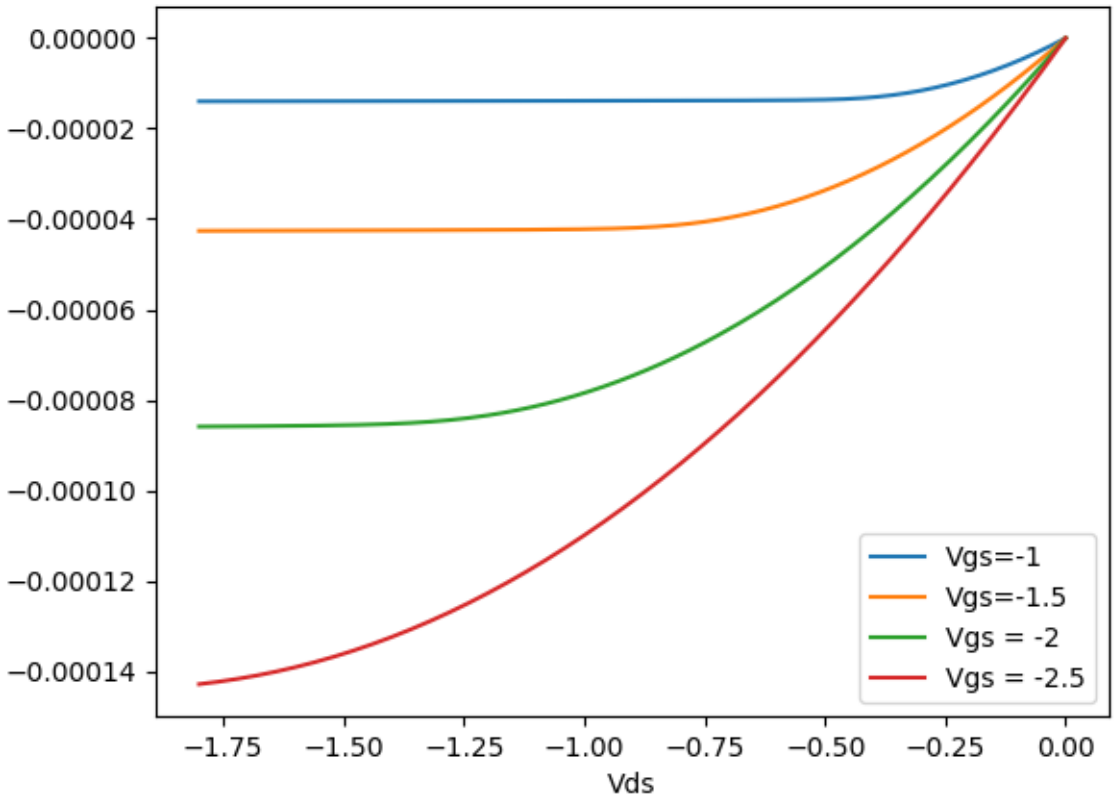

Figure 9: Long Channel pmos characteristics

```
run
*plot -i(v1) vs v(ds)
wrdata plot1.dat -i(v1) vs v(ds)
.endc
.end
```

Listing 10: Q1-a.cir

- Please refer Figure-9 for simulated output.

4.2 Saturation and Linear Regions

- Saturation and Linear Regions have been identified using I_d vs $V_{gs} - V_{th}$ plot.
- Netlist used for simulating the I_d vs V_{gs} plot for MOS devices.(Please note that the same netlist can be used for nmos short and long channel, pmos short and long channel with minor modifications)

```
* C:\Users\SAI ASHOK\q4_vlsi1.cir
.include "C:\Users\SAI ASHOK\TSMC180.lib"
.model pch_tt pmos

*M1 ds gs 0 0 pch_tt W=15u L=10u
```

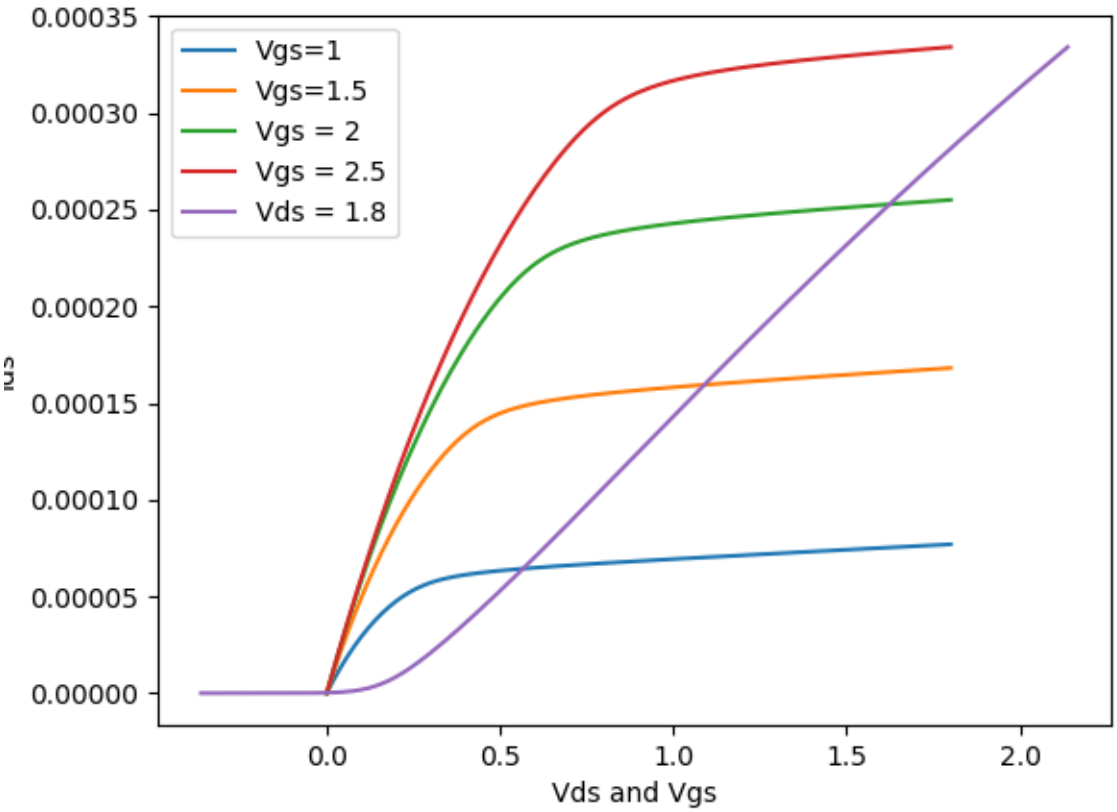

Figure 10: Short Channel nmos

```
M1 ds gs 0 0 pch_tt W=0.27u L=0.18u
V1 ds 0 DC -1.8
V2 gs 0 DC 0
.dc V2 0 -2.5 -0.01
.control
run
plot -i(v1) vs v(gs)
wrdata plot1.dat -i(v1) vs v(gs)
.endc
.end
```

Listing 11: Q1-a.cir

- Please refer Figure-10 for Short channel nmos.
- Please refer Figure-11 for Long Channel nmos.
- Please refer Figure-12 for Short channel pmos.
- Please refer Figure-13 for Long Channel pmos.
- **Please note that the region to the right of I_d vs $V_{gs} - V_{th}$ graph is saturation region and on the left would be Linear Region.**

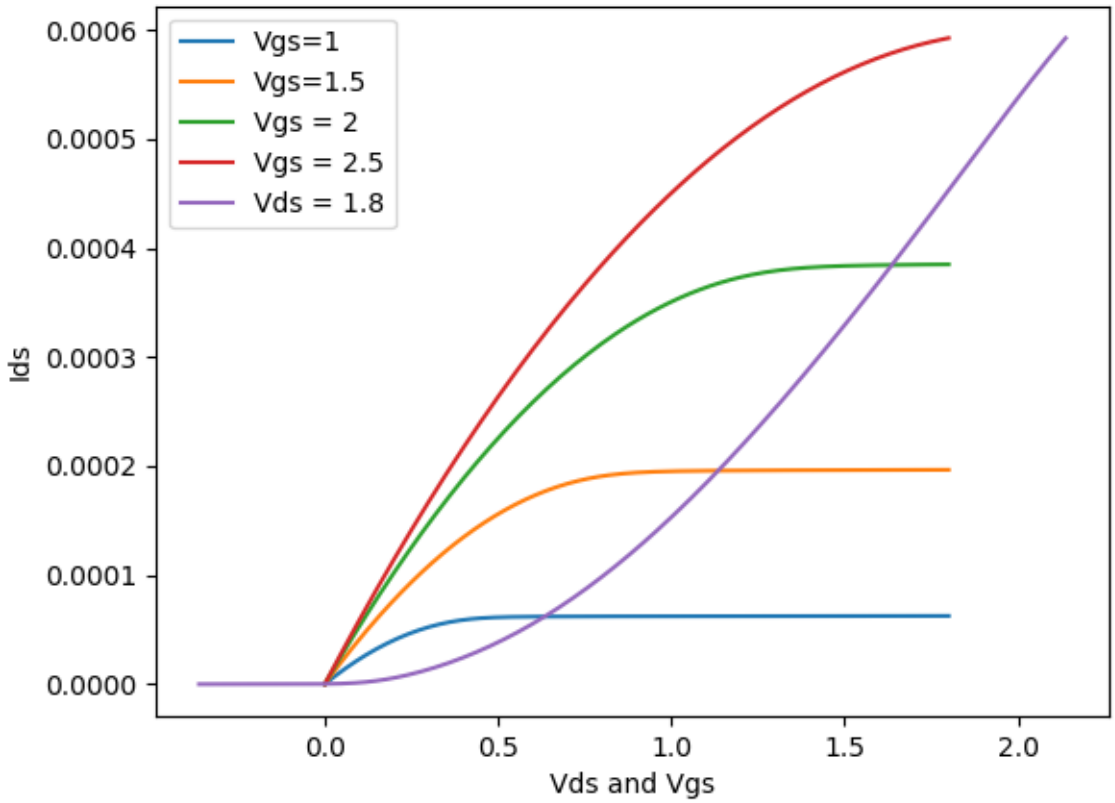

Figure 11: Long Channel nmos

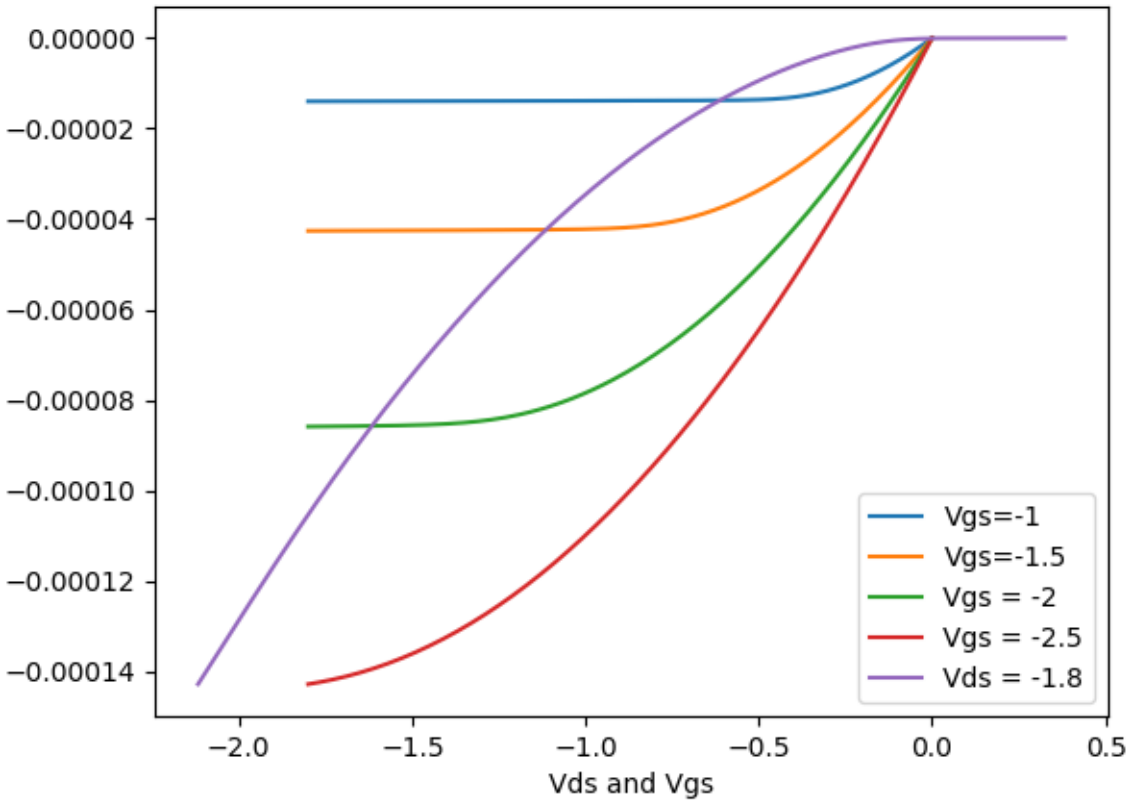

Figure 12: Short Channel pmos

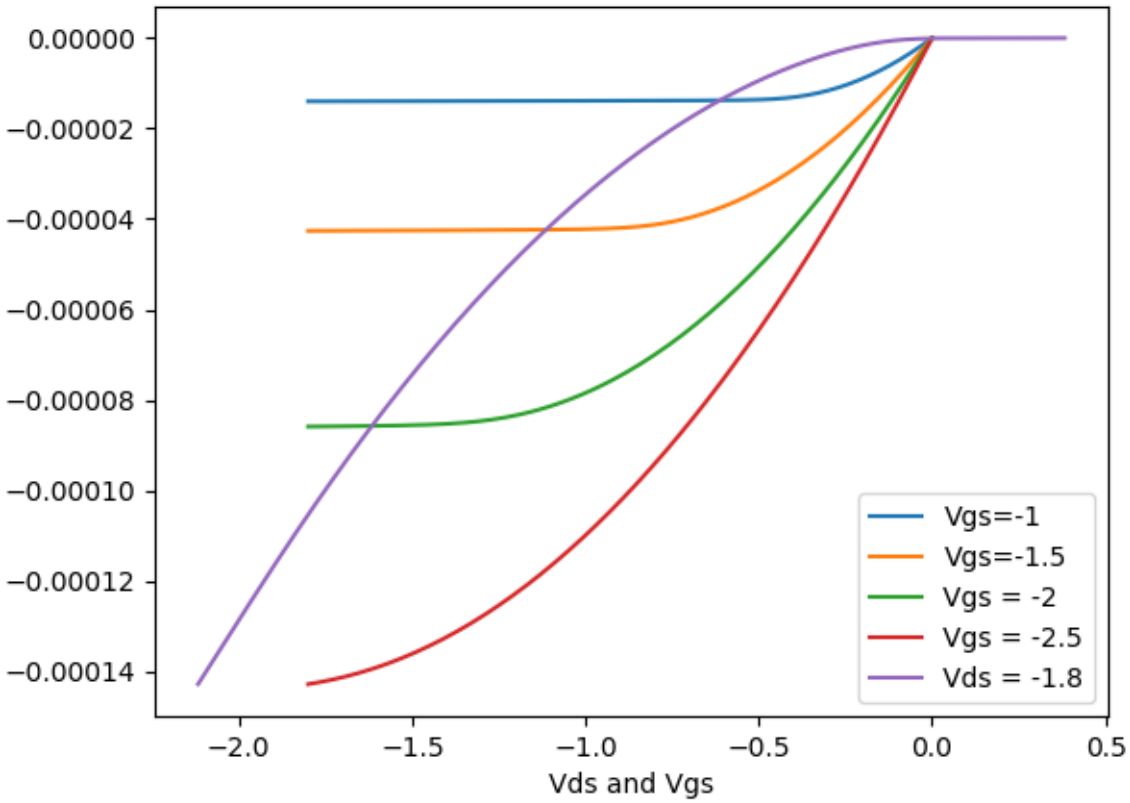

Figure 13: Long Channel pmos

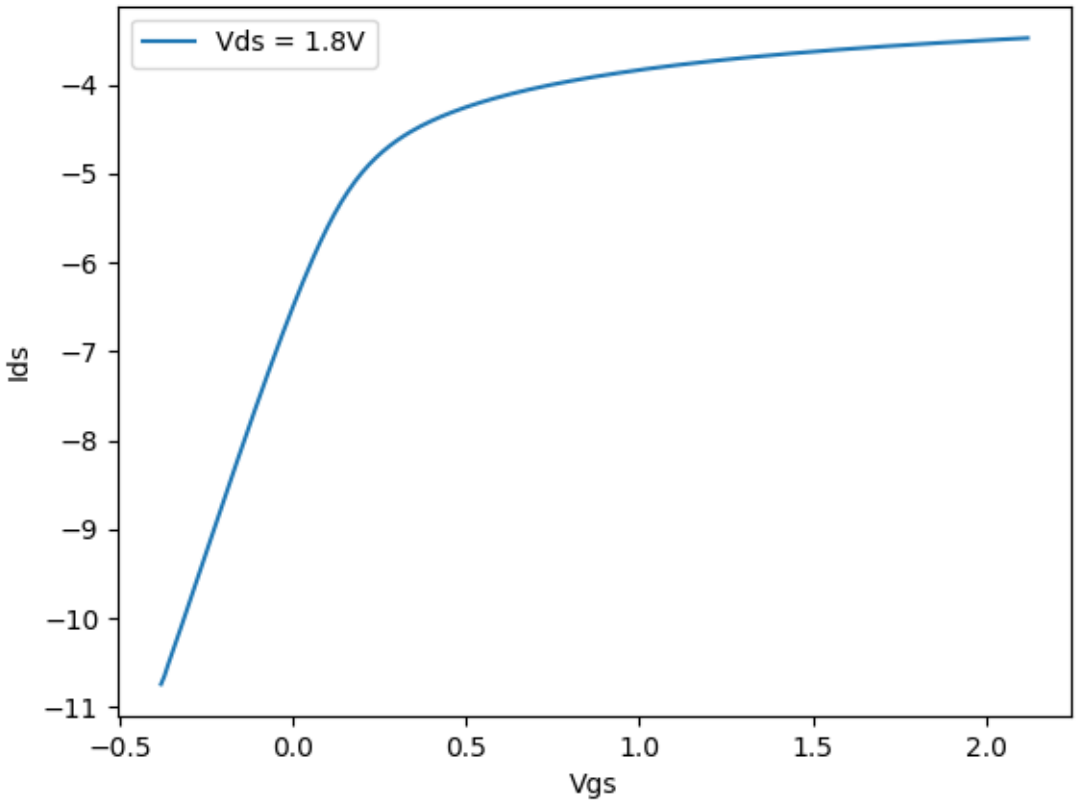

Figure 14: NMOS SC

4.3 Small Signal Resistance

- Small Signal Resistance is 1 over slope of I_d vs V_{ds} curve in saturation region.

MOS device	Slope	Small Signal Resistance
NMOS Short Channel	1.19e-05	84033Ω
NMOS Long Channel	1.18e-05	84745Ω
PMOS Short Channel	2.81e-06	355871Ω
PMOS Long Channel	5.13e-07	1960784Ω

4.4 Sub Threshold Slope

- Previously generated plots of I_d vs $V_{gs} - V_{th}$ for nmos short channel device in Log-Lin scale. (Please refer Figure-14)
- Slope of Sub-Threshold region = 11.40
- Value of n = 190

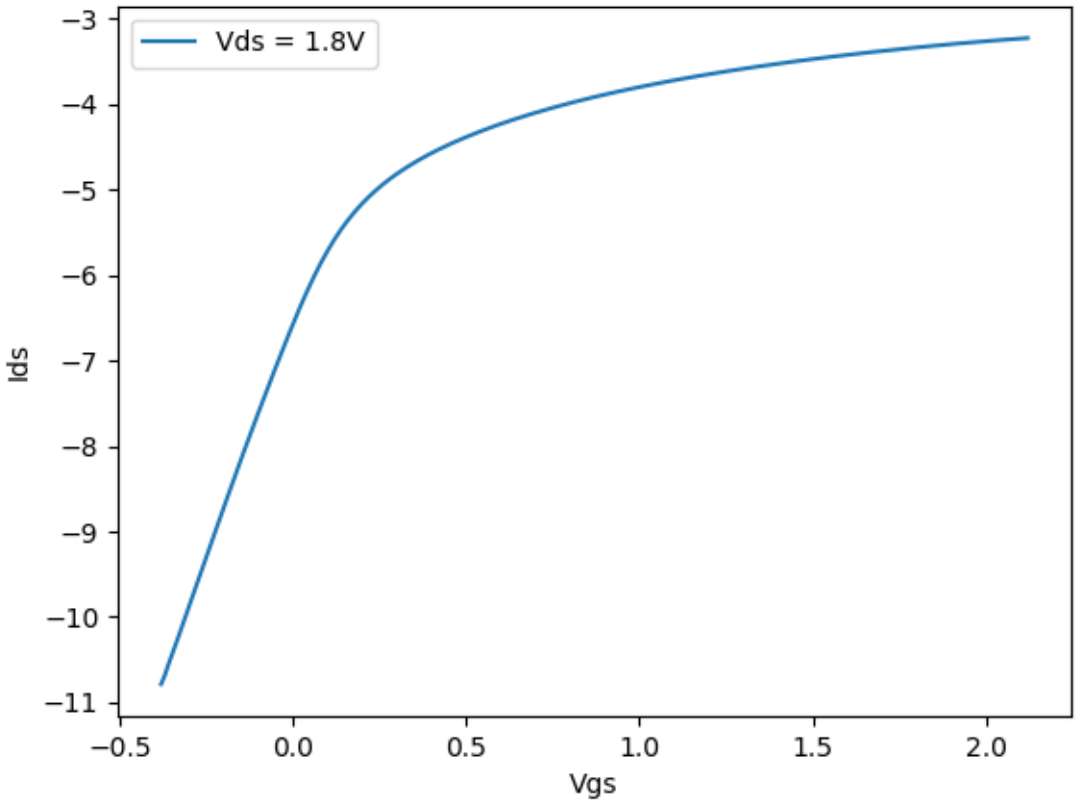

Figure 15: NMOS LC

- Previously generated plots of I_d vs $V_{gs} - V_{th}$ for nmos long channel device in Log-Lin scale. (Please refer Figure-15)
- Slope of Sub-Threshold region = 10.436
- Value of n = 174
- Previously generated plots of I_d vs $V_{gs} - V_{th}$ for pmos short channel device in Log-Lin scale. (Please refer Figure-16)
- Slope of Sub-Threshold region = -10.427
- Value of n = -174
- Previously generated plots of I_d vs $V_{gs} - V_{th}$ for pmos long channel device in Log-Lin scale. (Please refer Figure-17)
- Slope of Sub-Threshold region = -9.994
- Value of n = -166.5

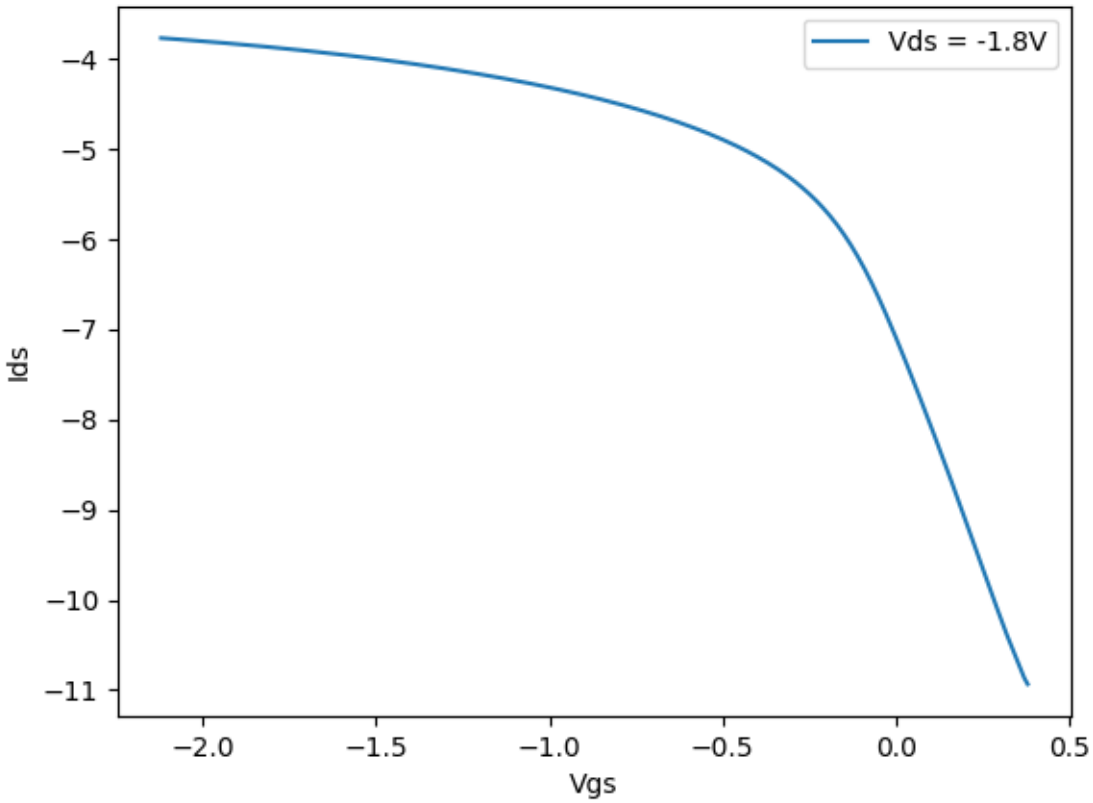

Figure 16: PMOS SC

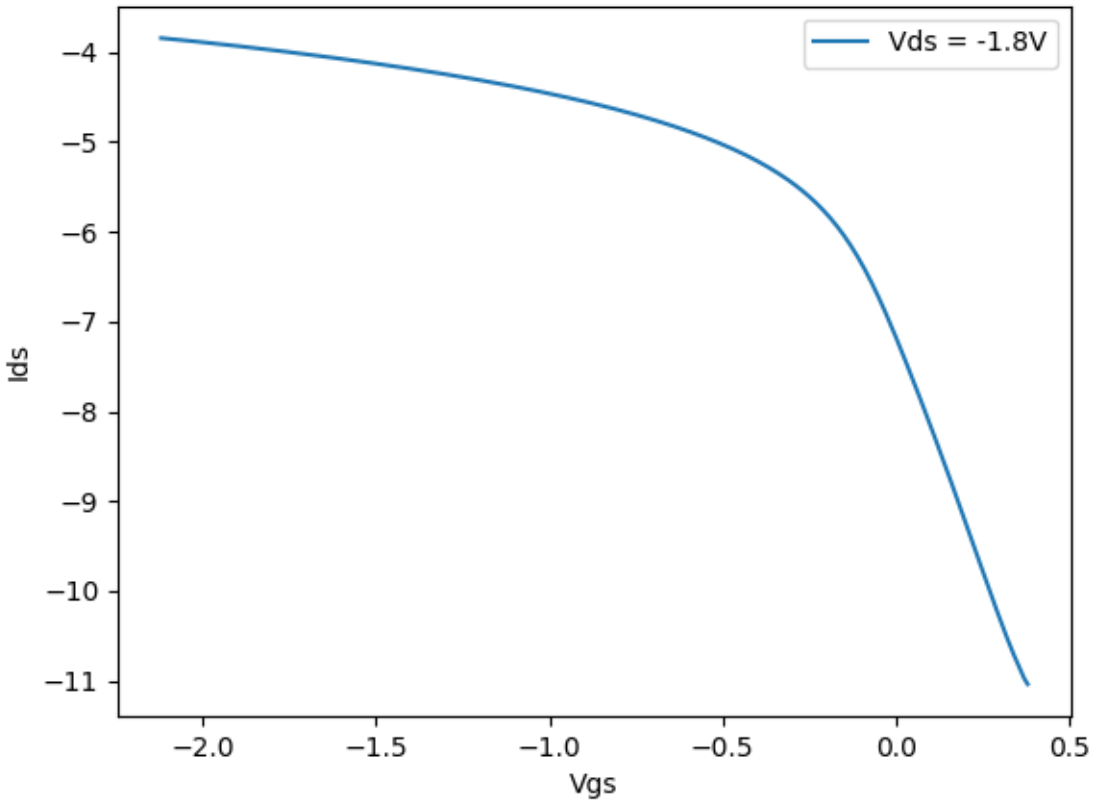

Figure 17: PMOS LC

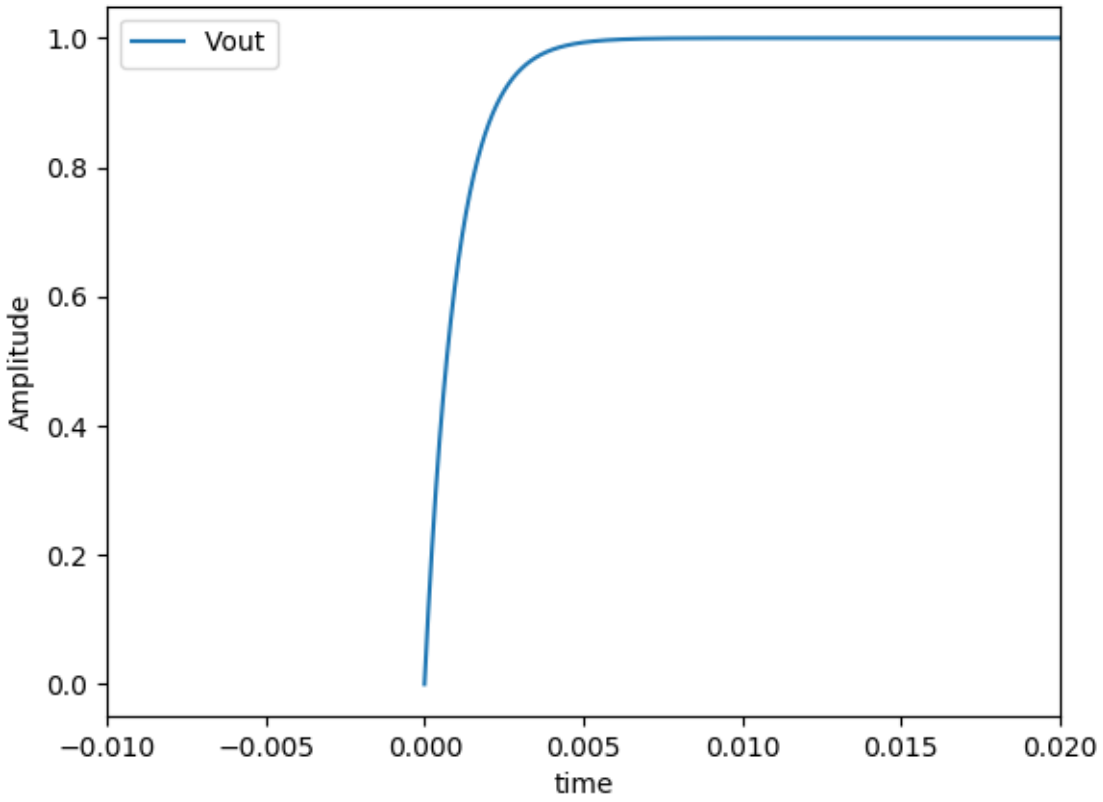

Figure 18: Propagation delay

5 Propagation Delay

5.1 Rise time and Propagation delay

- Netlist used to simulate the circuit with step input. Value of **R = 1000Ω , C = 1μF , RC = 1ms**.

```
* C:\Users\SAI ASHOK\q5_vlsi1.cir
V1 N001 0 PULSE(0 1 0 0 0 5 5 0)
R1 Vout N001 1000
C1 Vout 0 0.000001
*control commands
.control
tran 0.1u 40ms
plot vout
.endc
.end
```

Listing 12: Q1-a.cir

- Please refer Figure-18 for the output of simulation.
- As we can observe from the graph t_p is 0.000649351, which is aproximately equal to 0.69RC (0.00069).

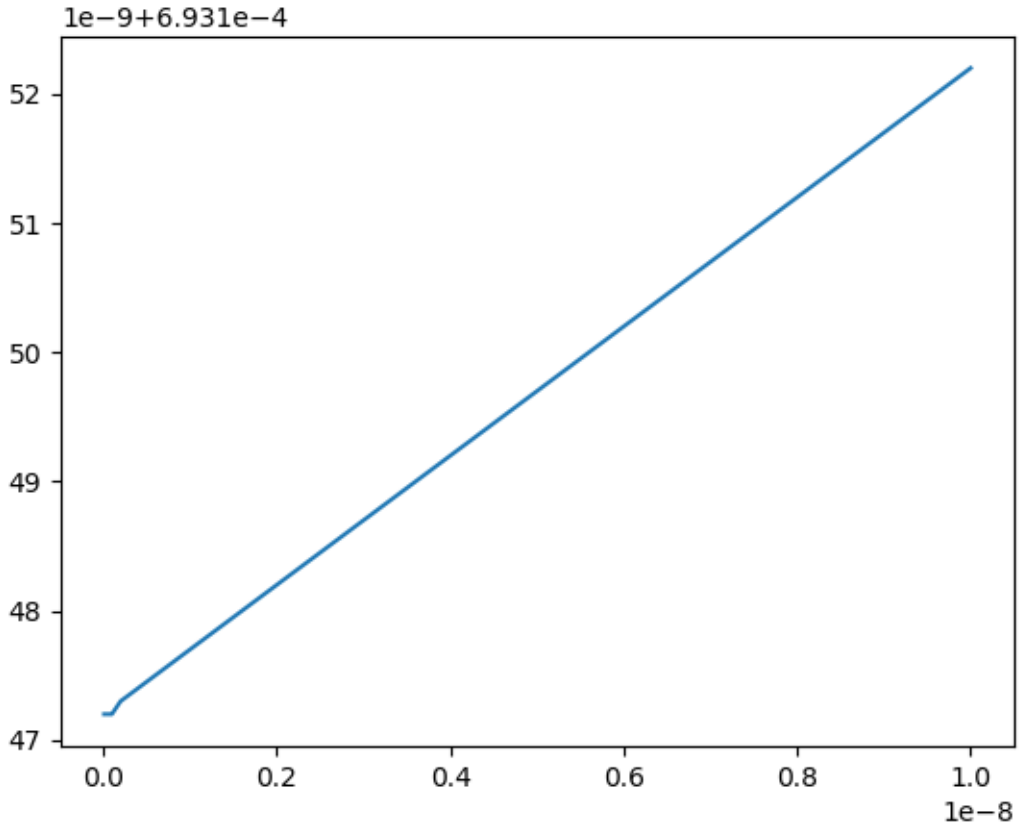

Figure 19: t_p vs $t_{r,in}$

- As we can observe from the graph t_r is 0.00233766 - 0.00012987 = 0.0022077 , which is approximately equal to 2.2RC (0.002200).

5.2 Non-Ideal Step Input

- Netlist to simulating for Non-Ideal Step Input and then to calculate Propagation Delay.

```
* C:\Users\SAI ASHOK\q5_vlsi1.cir
V1 N001 0 PULSE(0 1 0 0.01n 0 5 5 0)
R1 Vout N001 1000
C1 Vout 0 0.000001
*control commands
.control
tran 0.1u 1ms
meas TRAN TIME_1 TRIG V(Vout) VAL=0 CROSS=1 TARG V(Vout) VAL=0.5 CROSS=1
plot vout
.endc
.end
```

Listing 13: Q1-a.cir

- Please refer Figure-19 for the plot Propagation delay vs Rise time of Input

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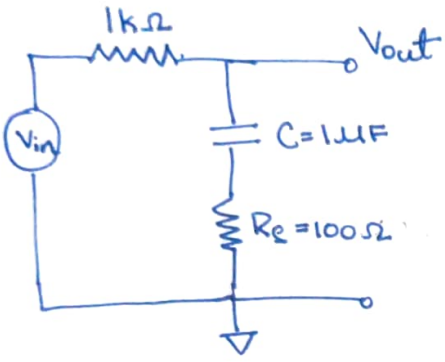
1)

b) phase lag estimation.



$$V_{in} - iR - iR_S - V_c = 0$$

$$V_{in} - RC\frac{dV_c}{dt} - R_S C\frac{dV_c}{dt} - V_c = 0 \quad \text{let } R + R_S = R'$$

$$V_{in} = R'C\frac{dV_c}{dt} + V_c \quad \text{(applying laplace transforms)}$$

$$V_{in}(s) = V_c(1 + R'Cs)$$

$$V_c = \frac{V_{in}(s)}{1 + R'Cs}$$

W.K.T $$i = C\frac{dV_c}{dt}$$

$$I(s) = Cs\,V_c(s)$$

$$I(s) = \frac{Cs\,V_{in}(s)}{1 + R'Cs}$$

$$V_{out} = I(s)R_s + V_c(s)$$

$$V_{out}(s) = \frac{R_s C s\, V_{in}(s)}{1 + R'Cs} + \frac{V_{in}(s)}{1 + R'Cs}$$

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1 + R_s Cs}{1 + R'Cs}$$ } transfer function.

phase lag introduced = $\underbrace{\tan^{-1}\left(\frac{R_s(\omega)}{1}\right)}_{\text{numerator}} - \underbrace{\tan^{-1}\left(\frac{R'C\omega}{1}\right)}_{\text{denominator}}$

for f = 100Hz $\Rightarrow \tan^{-1}(100 \times 10^{-6} \times 2\pi \times 100) - \tan^{-1}(1100 \times 10^{-6} \times 2\pi \times 100)$

$= 3.5952^\circ - 34.650^\circ$

$= -31.055^\circ$

for f = 1000000Hz $\Rightarrow \tan^{-1}(100 \times 10^{-6} \times 2\pi \times 10^{6}) - \tan^{-1}(1100 \times 10^{-6} \times 2\pi \times 10^{6})$

$= -0.08289^\circ$

c) phase lag introduced at 3dB point.

→ in the (b) part we have calculated Transfer function.

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{1+R_sCs}{1+R'Cs} = \frac{1+R_sC\omega_1^\circ}{1+R'C\omega_1^\circ}$$

* 3dB point

$$\frac{\sqrt{1+(R_sC\omega)^2}}{\sqrt{1+(R'C\omega)^2}} = \frac{1}{\sqrt{2}}$$

$$1 = \left((R')^2 - 2R_s^2\right) C^2\omega^2$$

$$\omega^2 = 840336.134$$

$$\omega_1 = 916.698$$

* Corresponding phase lag:

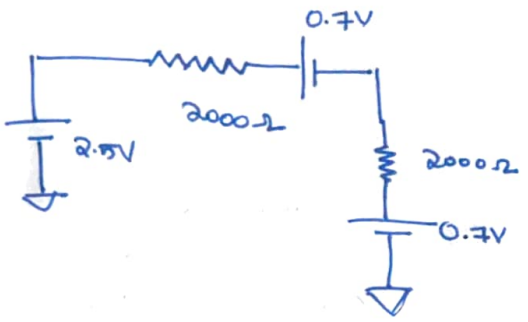
→ $\tan^{-1}(R_sC\omega_1) - \tan^{-1}(R'C\omega_1)$

⇒ $(-0.6981)^c \times 1 \cdot \because (180/\pi) = -40.001^\circ$

2)

a) Replacing diode with a voltage source

$V_{Don} = 0.7V$



Equation:

$$0 + 2.5 - i^{0}(2000) - 0.7 - i^{0}(2000) - 0.7 = 0$$

$$2.5 - 1.4 = i^{0}(4000)$$

$$\frac{1.1}{4000} = i^{0}$$

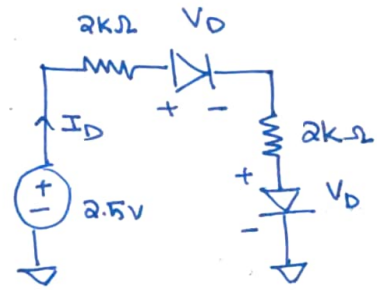
$$i^{0} = 0.000275$$

b) Solving for I_D & V_D using Ideal Diode equation

Ideal diode Equation:

$$I_D = I_s\left(e^{qV_D/nKT} - 1\right) \quad -①$$

Loop Equation:



$$2.5 - I_D(4000) - 2V_D = 0$$

$$I_D = \frac{2.5 - 2V_D}{4000} \quad -②$$

using eqn ② in ①:

$$e^{V_D/0.026} = 1 + \frac{10^{11}(2.5 - 2V_D)}{4}$$

$$V_D = 0.638V$$

$$I_D = 0.000306 \text{ Amps.}$$

4)

b) differences between short & long channel MOSFET

* Long channel transistor has squared dependence of I_D as a function of V_{GS} in the saturation region. (clearly observable from the spacing between different curves).

* Short channel MOSFET has a linear dependence of saturation current w.r.t V_{GS} which is also apparent in the graph.

* Short channel Transistors also saturate at a lower voltage than (V_{DS}) (in case of nmos) long channel transistors

* The above stated velocity saturation is less prominent in pmos.