Introduction to VLSI Design

November 14, 2020

1 MOSFET Resistance

1.1 Transient Simulation

- Netlist for calculating the R_{eq} as a function of V_{DD} for an NMOS device.

```
* C:\Users\SAI ASHOK\hw2_vlsi_q1.cir
.include "C:\Users\SAI ASHOK\TSMC180.lib"
.model nch_tt nmos
V1 gs 0 DC 1.8
M1 ds gs 0 0 nch_tt W=0.24u L=0.18u
C c1 0 1pF ic=1.8V
V2 c1 ds DC 0
*.IC V(C1)=1.8
.control
let vdd = 1.8V
let Req = vector(17)
let Vval = vector(17)
let loop = 0
print Req[0]
while loop<17
  alter @V1=vdd
  alter @C ic=vdd
  let vdd2 = vdd/2
  run
  tran 0.05u 500u uic
  let t_vdd = 0
  let v3 = v(ds)/i(v2)
  meas tran t_vdd2 when v(ds)=vdd2 cross=1
  meas tran r_eq avg v3 from=t_vdd to=t_vdd2
  let Req[loop] = r_eq
  let Vval[loop] = vdd
  let loop=loop+1
  let vdd=vdd-0.1
end
plot req vs vval
wrdata plot_1.dat req vs vval
.endc
.end
```

Listing 1: Q1-a.cir

- The value of R_{eq} at V_{dd} = 1.8V is 6.706644e+03Ω.

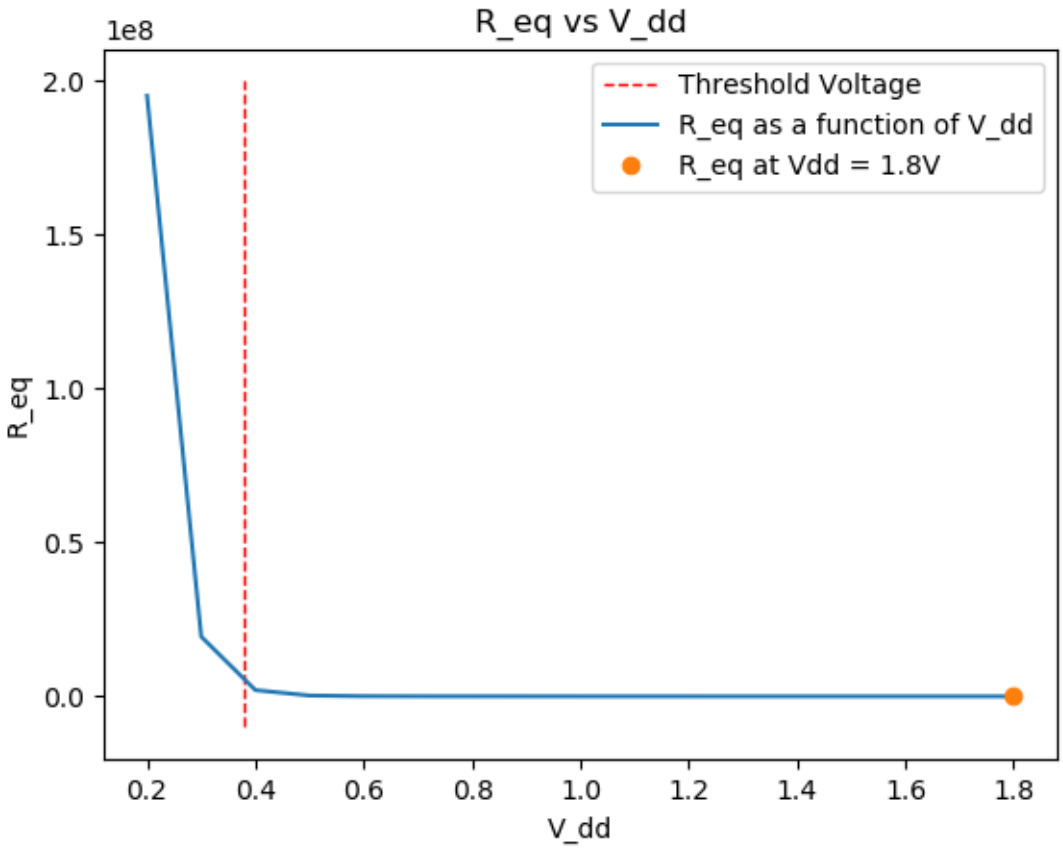

Figure 1: nmos

- Please refer Figure 1 for the plot of R_{eq} vs V_{DD} for an NMOS device.
- Netlist for calculating the R_{eq} as a function of V_{DD} for a PMOS device.

```
* C:\Users\SAI ASHOK\hw2_vlsi_q1.cir
.include "C:\Users\SAI ASHOK\TSMC180.lib"
.model pch_tt pmos
V1 gs 0 DC -1.8
M1 ds gs 0 0 pch_tt W=0.24u L=0.18u
C c1 0 1pF ic=-1.8V
V2 c1 ds DC 0
*.IC V(C1)=1.8
.control
let vdd = -1.8V
let Req = vector(17)
let Vval = vector(17)
let loop = 0
print Req[0]
while loop<17
  alter @V1=vdd
  alter @C ic=vdd
  let vdd2 = vdd/2
  run
  tran 0.05u 500u uic
```

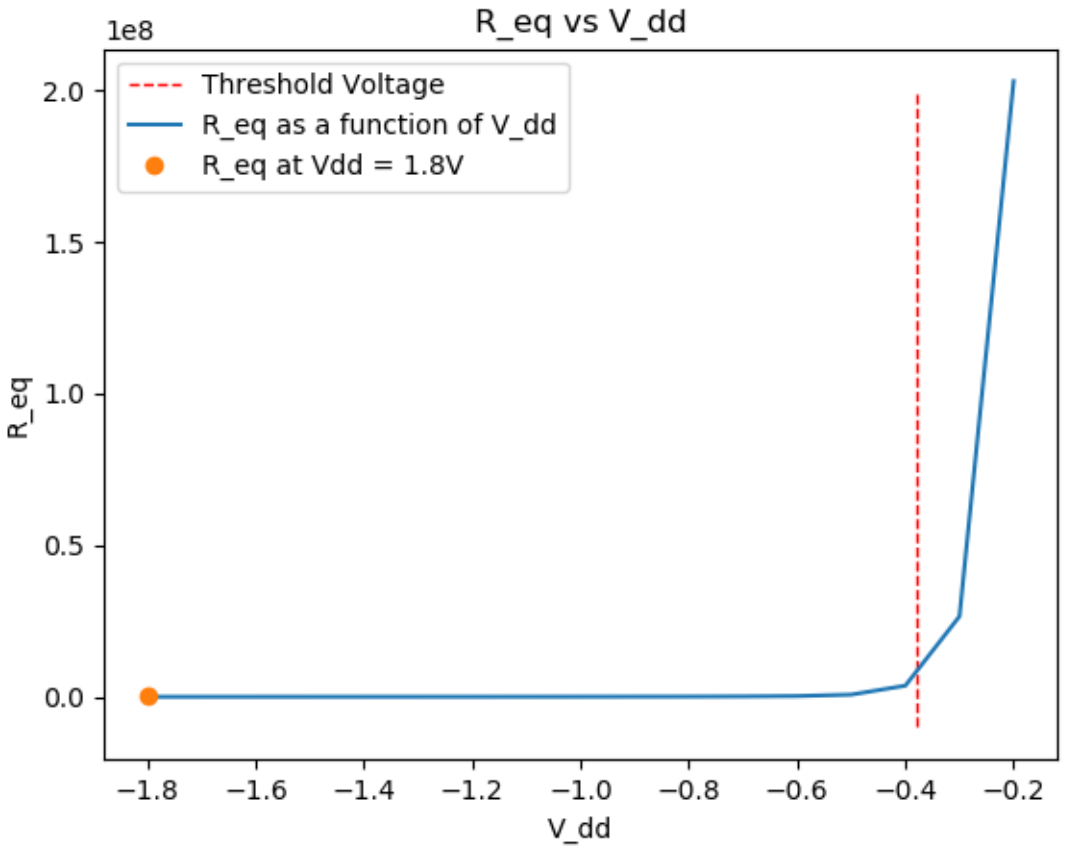

Figure 2: pmos

```
  let t_vdd = 0
  let v3 = v(ds)/i(v2)
  meas tran t_vdd2 when v(ds)=vdd2 cross=1
  meas tran r_eq avg v3 from=t_vdd to=t_vdd2
  let Req[loop] = r_eq
  let Vval[loop] = vdd
  let loop=loop+1
  let vdd=vdd+0.1
end
plot req vs vval
wrdata plot_2.dat req vs vval
.endc
.end
```

Listing 2: Q1-a.cir

- The value of R_{eq} at V_{dd} = -1.8V is 17692Ω.
- Please refer Figure 2 for the plot of R_{eq} vs V_{DD} for a PMOS device.

1.2 Comparing with Table 3.3

- The values of R_{eq} for 0.18µm process as calculated from simulations are given in the table below.

$\|V_{DD}\|$	R_{eq} **NMOS**	R_{eq} **for PMOS**
2V	6477Ω	15454.38Ω
1.8V	6706.644Ω	17692.76Ω
1.5V	7401.839Ω	23740.9Ω
1V	12178.95Ω	50710.38Ω
0.5V	275508.9Ω	726286.9Ω

- We can clearly observe that these values are less than their counterparts for 0.25µm process given in the table.
- It is because of the ratio $\frac{\omega}{L}$ which is inversely proportional to R_{eq}.
- It can also be seen from the table that R_{eq} for PMOS devices are much higher than R_{eq} for NMOS devices for the same V_{DD}. This can be attributed to the fact that mobility of holes are less than mobility of electrons.

2 Capacitance

2.1 Long Channel, f=100Hz

- Netlist for simulating capacitance of Long Channel MOS at 100Hz.

```
* C:\Users\SAI ASHOK\hw2_vlsi_q2.cir
.include "C:\Users\SAI ASHOK\TSMC180.lib"
.model nch_tt nmos
V1 N002 0 SINE(0 1.59e-3 10e1)
M1 0 N001 0 0 nch_tt W=25u L=10u
*M1 0 N001 0 0 nch_tt W=0.45u L=0.18u
V2 N001 N002 DC -1.8
.control
let Vg = -1.8
let x = unitvec(72)
let y = unitvec(72)
while Vg < 1.81
  alter V2=Vg
  tran 1u 1m
  *tran 1n 100n
  *tran 10p 1n
  run
  meas tran i_max FIND i(v1) at=0.5m
  *meas tran i_max MAX i(v1) from=0 to=1n
  let x[20*(Vg+1.8)] = Vg
  let y[20*(Vg+1.8)] = i_max
  let Vg = Vg + 0.05
end
```

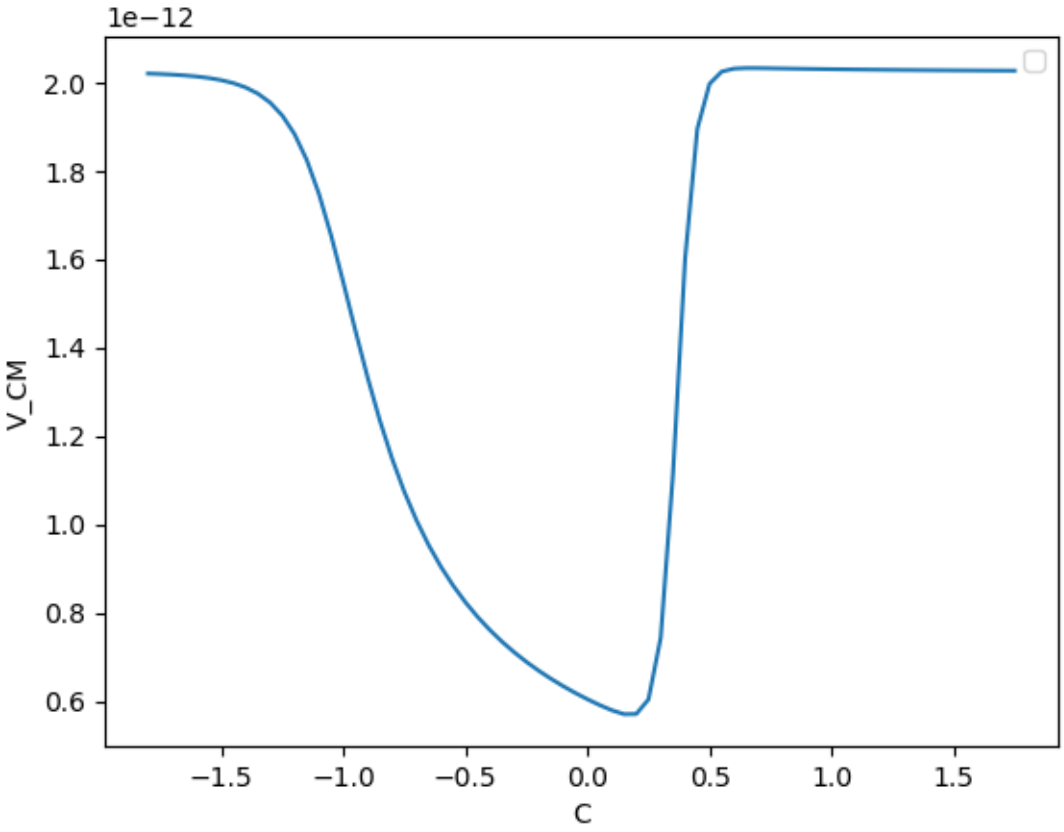

Figure 3: Long Channel, f=100Hz

```
plot y vs x
wrdata plot_3.dat y vs x
.endc
.end
```

Listing 3: Q1-a.cir

- Please refer Figure 3 for the plot.

2.2 Long Channel, f=10MHz

- Netlist for simulating capacitance of Long Channel MOS at 10MHz.

```
* C:\Users\SAI ASHOK\hw2_vlsi_q2.cir
.include "C:\Users\SAI ASHOK\TSMC180.lib"
.model nch_tt nmos
V1 N002 0 SINE(0 1.59e-8 10e6)
M1 0 N001 0 0 nch_tt W=25u L=10u
*M1 0 N001 0 0 nch_tt W=0.45u L=0.18u
V2 N001 N002 DC -1.8
.control
let Vg = -1.8
let x = unitvec(72)
```

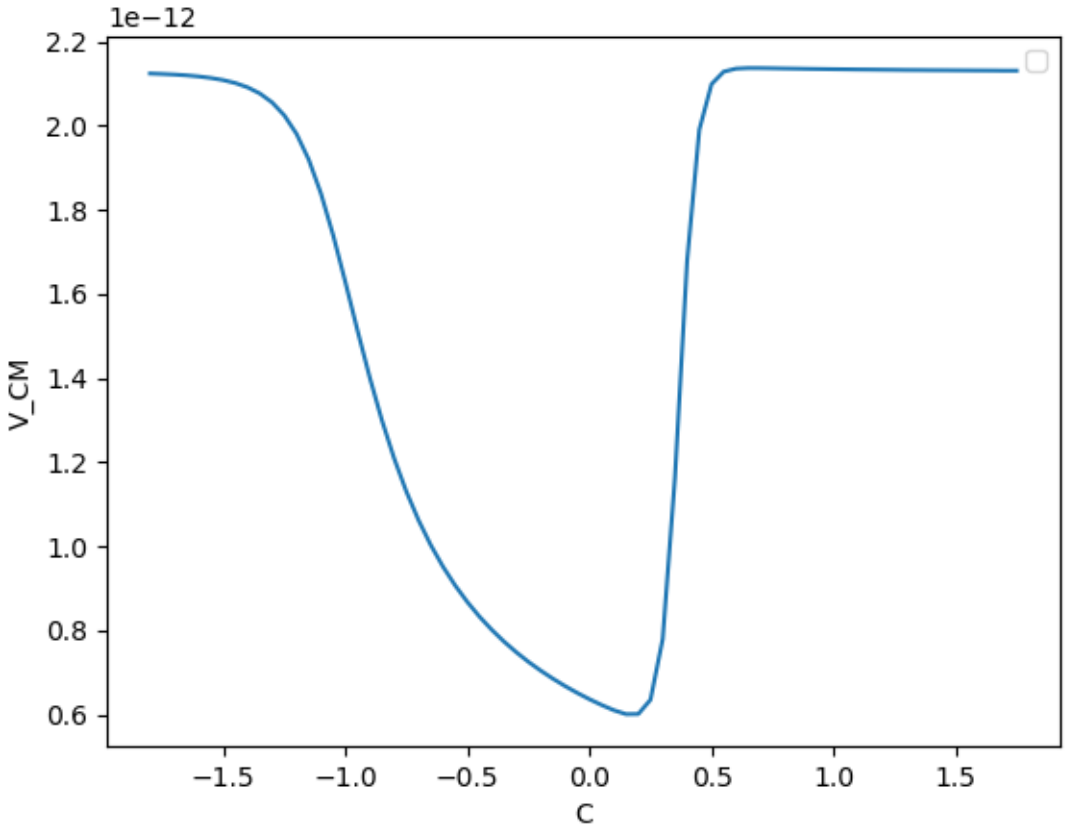

Figure 4: Long Channel, f=10MHz

```
let y = unitvec(72)
while Vg < 1.81
  alter V2=Vg
  *tran 1u 1m
  tran 1n 100n
  *tran 10p 1n
  run
  meas tran i_max FIND i(v1) at=50n
  *meas tran i_max MAX i(v1) from=0 to=1n
  let x[20*(Vg+1.8)] = Vg
  let y[20*(Vg+1.8)] = i_max
  let Vg = Vg + 0.05
end
plot y vs x
wrdata plot_4.dat y vs x
.endc
.end
```

Listing 4: Q1-a.cir

- Please refer Figure 4 for the plot.

2.3 Long Channel, f=10GHz

- Netlist for simulating capacitance of Long Channel MOS at 10GHz.

```
* C:\Users\SAI ASHOK\hw2_vlsi_q2.cir
.include "C:\Users\SAI ASHOK\TSMC180.lib"
.model nch_tt nmos
V1 N002 0 SINE(0 1.59e-11 10e9)
M1 0 N001 0 0 nch_tt W=25u L=10u
*M1 0 N001 0 0 nch_tt W=0.45u L=0.18u
V2 N001 N002 DC -1.8
.control
let Vg = -1.8
let x = unitvec(72)
let y = unitvec(72)
while Vg < 1.81
  alter V2=Vg
  *tran 1u 1m
  *tran 1n 100n
  tran 10p 1n
  run
  *meas tran i_max FIND i(v1) at=50n
  meas tran i_max MAX i(v1) from=0 to=1n
  let x[20*(Vg+1.8)] = Vg
  let y[20*(Vg+1.8)] = i_max
  let Vg = Vg + 0.05
end
plot y vs x
wrdata plot_5.dat y vs x
.endc
.end
```

Listing 5: Q1-a.cir

- Please refer Figure 5 for the plot.

2.4 Short Channel, f=100Hz

- Netlist for simulating capacitance of Short Channel MOS at 100Hz.

```
* C:\Users\SAI ASHOK\hw2_vlsi_q2.cir
.include "C:\Users\SAI ASHOK\TSMC180.lib"
.model nch_tt nmos
V1 N002 0 SINE(0 1.59e-3 10e1)
*M1 0 N001 0 0 nch_tt W=25u L=10u
M1 0 N001 0 0 nch_tt W=0.45u L=0.18u
V2 N001 N002 DC -1.8
.control
let Vg = -1.8
let x = unitvec(72)
let y = unitvec(72)
while Vg < 1.81
```

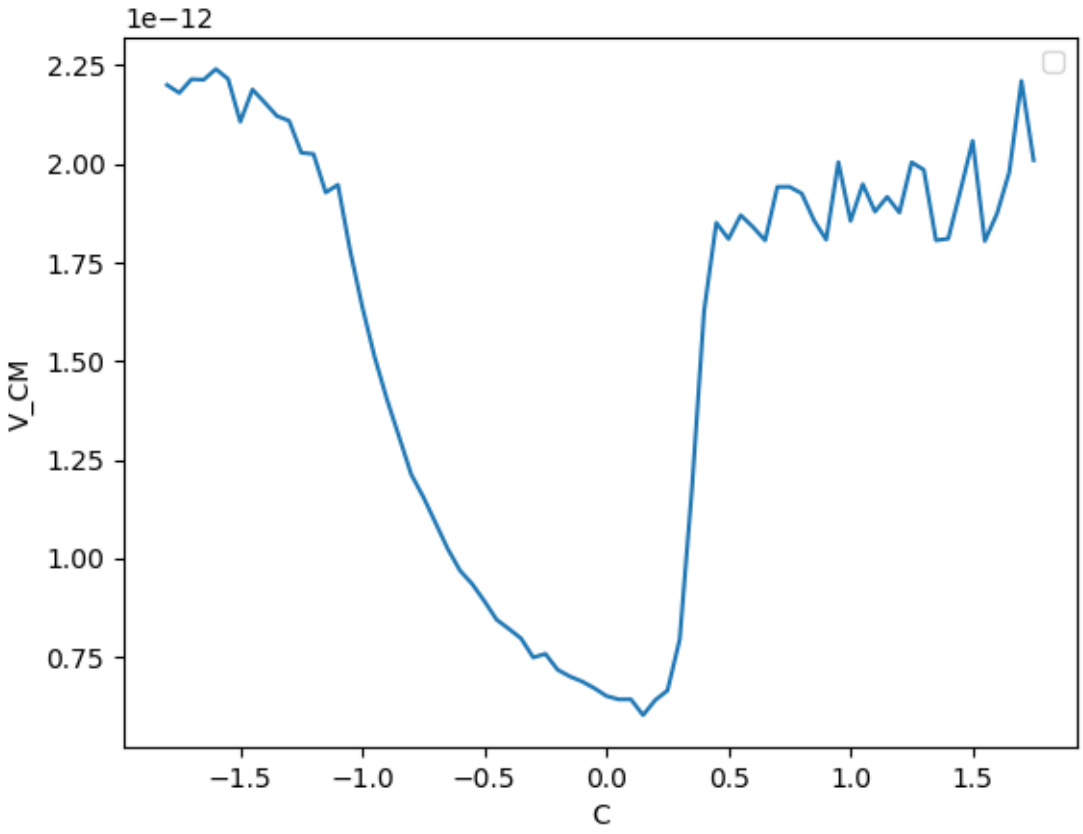

Figure 5: Long Channel, f=10GHz

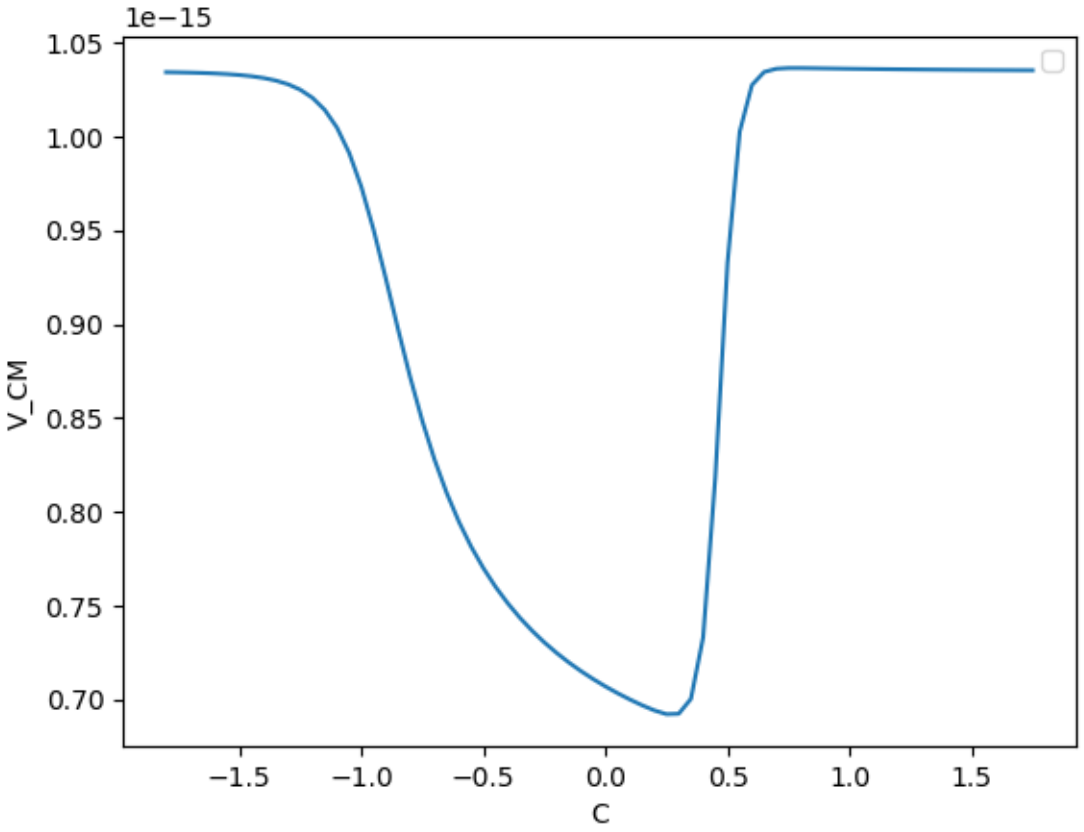

Figure 6: Short Channel, f=100Hz

```
  alter V2=Vg
  tran 1u 1m
  *tran 1n 100n
  *tran 10p 1n
  run
  meas tran i_max FIND i(v1) at=0.5m
  *meas tran i_max MAX i(v1) from=0 to=1n
  let x[20*(Vg+1.8)] = Vg
  let y[20*(Vg+1.8)] = i_max
  let Vg = Vg + 0.05
end
plot y vs x
wrdata plot_6.dat y vs x
.endc
.end
```

Listing 6: Q1-a.cir

- Please refer Figure 6 for the plot.

2.5 Short Channel, f=10MHz

- Netlist for simulating capacitance of Short Channel MOS at 10MHz.

```
* C:\Users\SAI ASHOK\hw2_vlsi_q2.cir
.include "C:\Users\SAI ASHOK\TSMC180.lib"
.model nch_tt nmos
V1 N002 0 SINE(0 1.59e-8 10e6)
*M1 0 N001 0 0 nch_tt W=25u L=10u
M1 0 N001 0 0 nch_tt W=0.45u L=0.18u
V2 N001 N002 DC -1.8
.control
let Vg = -1.8
let x = unitvec(72)
let y = unitvec(72)
while Vg < 1.81
  alter V2=Vg
  *tran 1u 1m
  tran 1n 100n
  *tran 10p 1n
  run
  meas tran i_max FIND i(v1) at=50n
  *meas tran i_max MAX i(v1) from=0 to=1n
  let x[20*(Vg+1.8)] = Vg
  let y[20*(Vg+1.8)] = i_max
  let Vg = Vg + 0.05
end
plot y vs x
wrdata plot_7.dat y vs x
.endc
.end
```

Listing 7: Q1-a.cir

- Please refer Figure 7 for the plot.

2.6 Long Channel, f=10GHz

- Netlist for simulating capacitance of Short Channel MOS at 10GHz.

```
* C:\Users\SAI ASHOK\hw2_vlsi_q2.cir
.include "C:\Users\SAI ASHOK\TSMC180.lib"
.model nch_tt nmos
V1 N002 0 SINE(0 1.59e-11 10e9)
*M1 0 N001 0 0 nch_tt W=25u L=10u
M1 0 N001 0 0 nch_tt W=0.45u L=0.18u
V2 N001 N002 DC -1.8
.control
let Vg = -1.8
let x = unitvec(72)
let y = unitvec(72)
while Vg < 1.81
  alter V2=Vg
  *tran 1u 1m
```

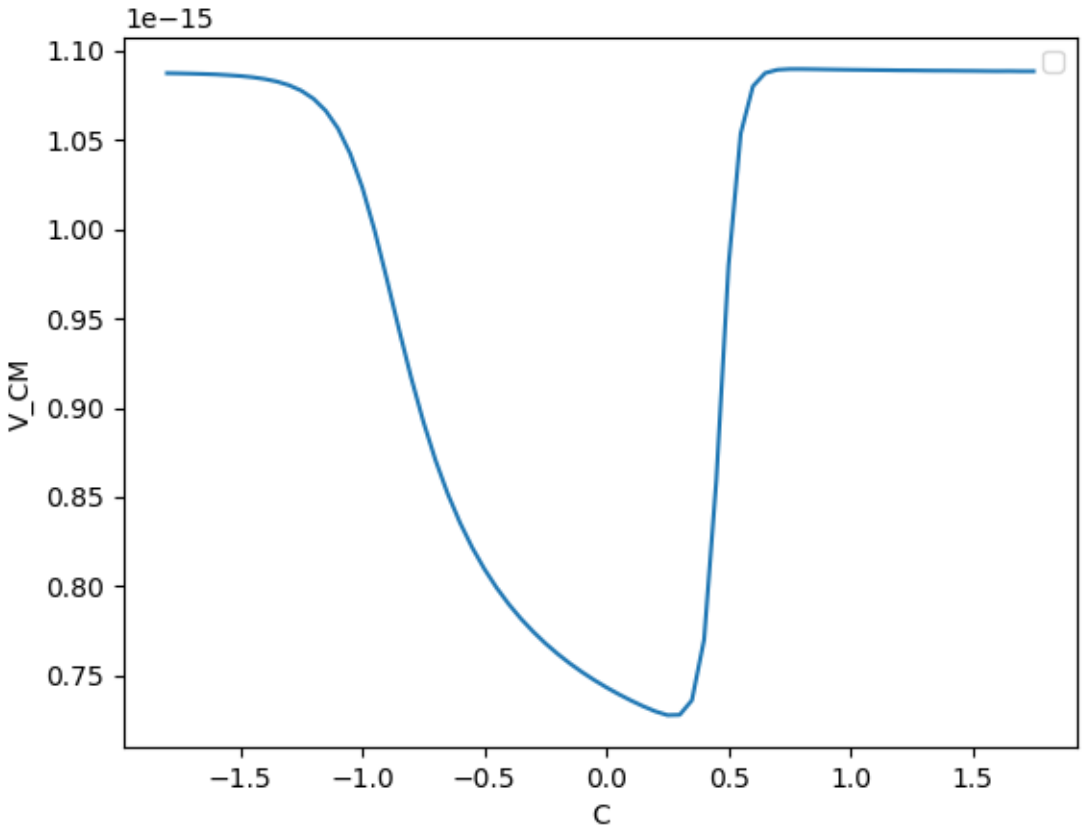

Figure 7: Short Channel, f=10MHz

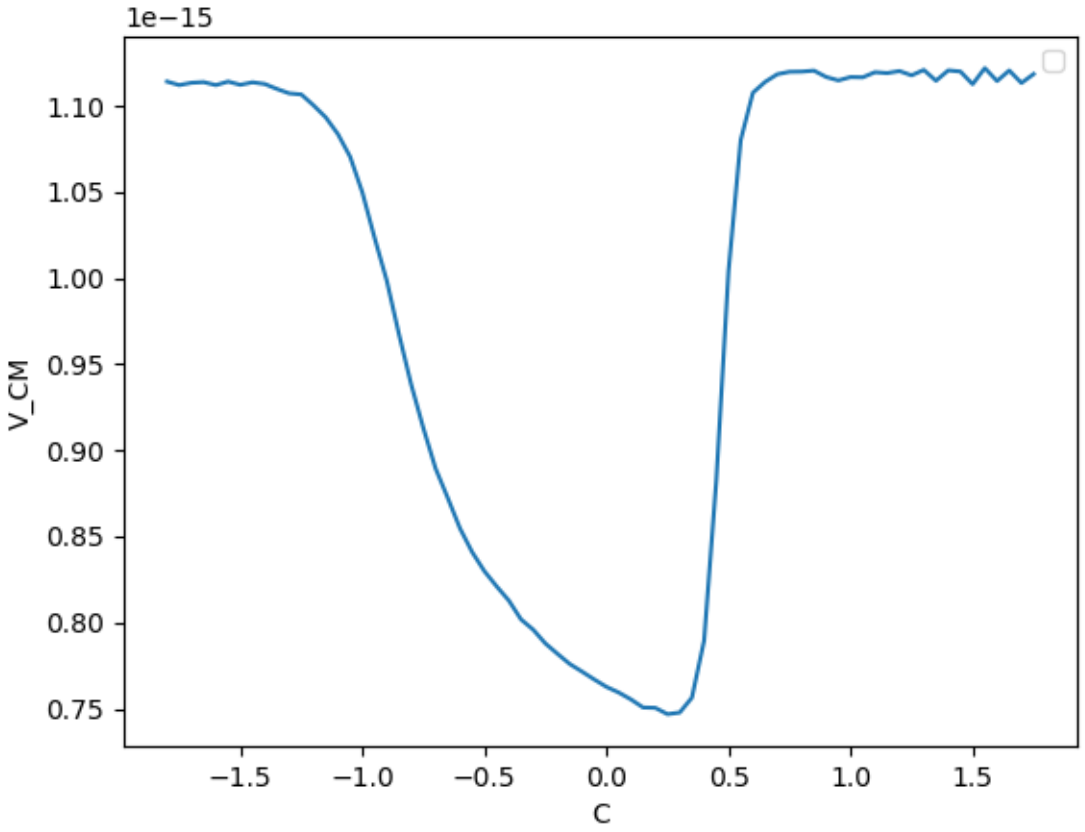

Figure 8: Short Channel, f=10GHz

```
  *tran 1n 100n
  tran 10p 1n
  run
  *meas tran i_max FIND i(v1) at=50n
  meas tran i_max MAX i(v1) from=0 to=1n
  let x[20*(Vg+1.8)] = Vg
  let y[20*(Vg+1.8)] = i_max
  let Vg = Vg + 0.05
end
plot y vs x
wrdata plot_8.dat y vs x
.endc
.end
```

Listing 8: Q1-a.cir

- Please refer Figure 8 for the plot.

2.7 Observation

- We can clearly observer that the shape of Graph is not changing in all the cases including short channel, long channel, low frequency and high frequency.

- For the high frequency we can see some distortions because of the sensitivity that lies in calculating for such small step sizes.
- The Peak Capacitance is higher in Long Channel than Short Channel which can be attributed to the fact that w*L of long channel is higher than W*L of short channel as Gate Capacitance is directly proportional to W*L.
- Also the Capacitance does not vary for high frequency and low frequency case because of abundance of inversion charges.

3 Simulating NMOS inverter R load

3.1 VTC and Gain of Inverter

- Netlist for simulating Gain and VTC of Inverter.

```
* C:\Users\SAI ASHOK\hw2_vlsi_q2.cir
.include "C:\Users\SAI ASHOK\TSMC180.lib"
.model nch_tt nmosV1
V1 n1 0 2.5
R1 n1 Vout 75000
M1 Vout Vin 0 0 nch_tt W=30u L=10u
V2 Vin 0 dc
.control
dc v2 -0.01 2.6 0.01
run
plot vout vs vin
let gain = deriv(v(vout))
let dgain = deriv(gain)
plot gain vs vin
meas dc vil find vin when gain=-1 cross=1
meas dc vih find vin when gain=-1 cross=2
meas dc voh find vout when vin=0 cross=1
meas dc vol find vout when vin=2.5 cross=1
meas dc vm find vout when vin=vout cross=1
meas dc pg find gain when dgain=0
wrdata plot_9.dat vout vs vin
wrdata plot_10.dat gain vs vin
.endc
.end
```

Listing 9: Q1-a.cir

- Please refer Figure 9 for the plot of VTC.
- Please refer Figure 10 for the plot of Gain.
- Please find the following observations from the simulation.

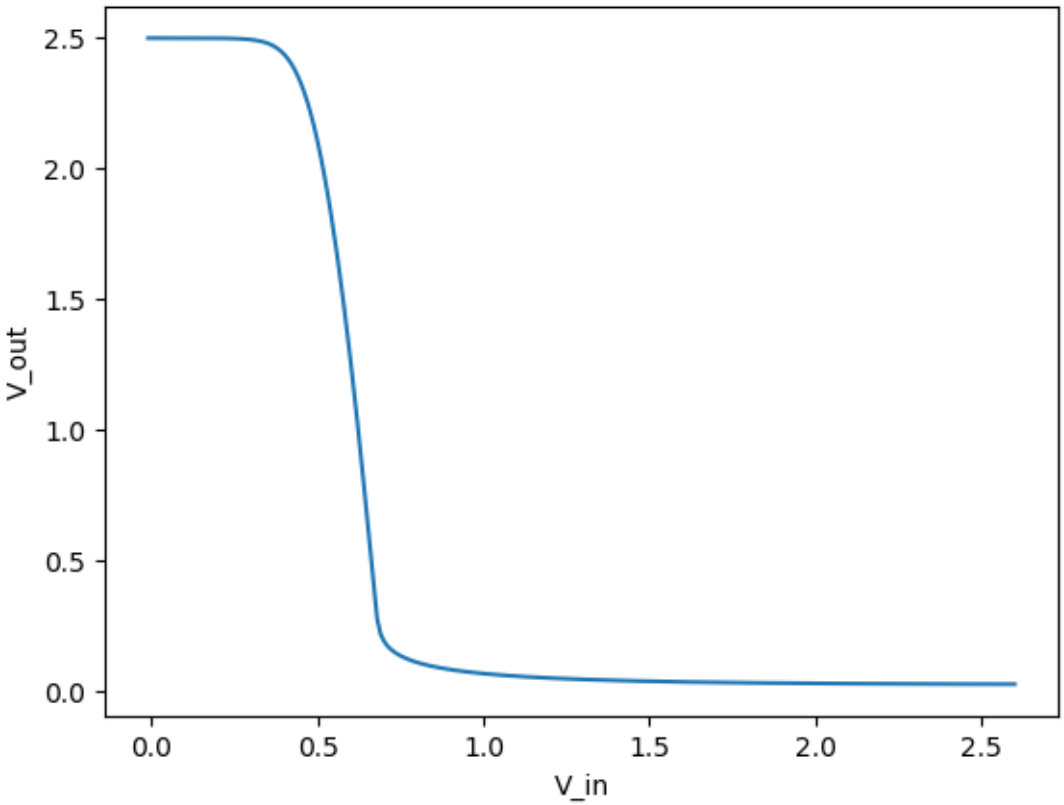

Figure 9: VTC

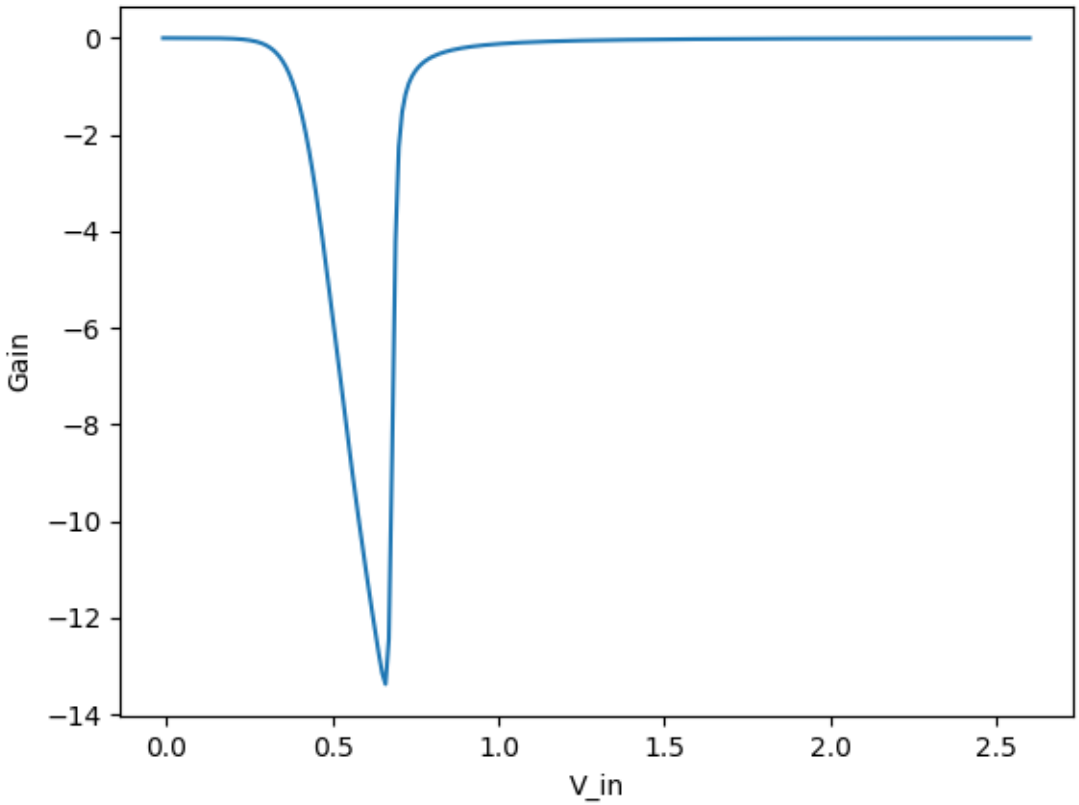

Figure 10: Gain of Inverter

Parameters	Value
V_{IL}	3.871599e-01
V_{IH}	7.738449e-01
V_{OH}	2.499998e+00
V_{OL}	3.174192e-02
V_m	6.731995e-01
$PeakGain$	-9.514598e+01

3.2 Impct of R_L on PeakGain

- Please find the Netlist for simulating Peakgain for various Resistive Loads.

```
* C:\Users\SAI ASHOK\hw2_vlsi_q2.cir
.include "C:\Users\SAI ASHOK\TSMC180.lib"
.model nch_tt nmosV1
V1 n1 0 2.5
R1 n1 Vout 75000
M1 Vout Vin 0 0 nch_tt W=30u L=10u
V2 Vin 0 dc
.control
dc v2 -0.01 2.6 0.01 r1 10k 100k 10k
run
plot vout vs vin
let gain = deriv(v(vout))
let dgain = deriv(gain)
plot gain vs vin
wrdata plot_11.dat gain vs vin
.endc
.end
```

Listing 10: Q1-a.cir

- Please refer Figure 11 for the plot generated.
- It is clear that as R_L increases Peakgain increases and V_M shifts to the left, which is also supported by the formula in which R_L is directly proportional to Peakgain.
- So as R_L increases the pull down circuit becomes stronger and V_M shifts to the left.

3.3 Transient Analysis for Square Pulse

- Netlist for simulating the output for a square pulse with 50% duty cycle.

```
* C:\Users\SAI ASHOK\hw2_vlsi_q5.cir
.include "C:\Users\SAI ASHOK\TSMC180.lib"
.model nch_tt nmos
V1 n1 0 2.5
R1 n1 Vout 75k
C1 Vout 0 3p
M1 Vout Vin 0 0 nch_tt W=0.54u L=0.18u
```

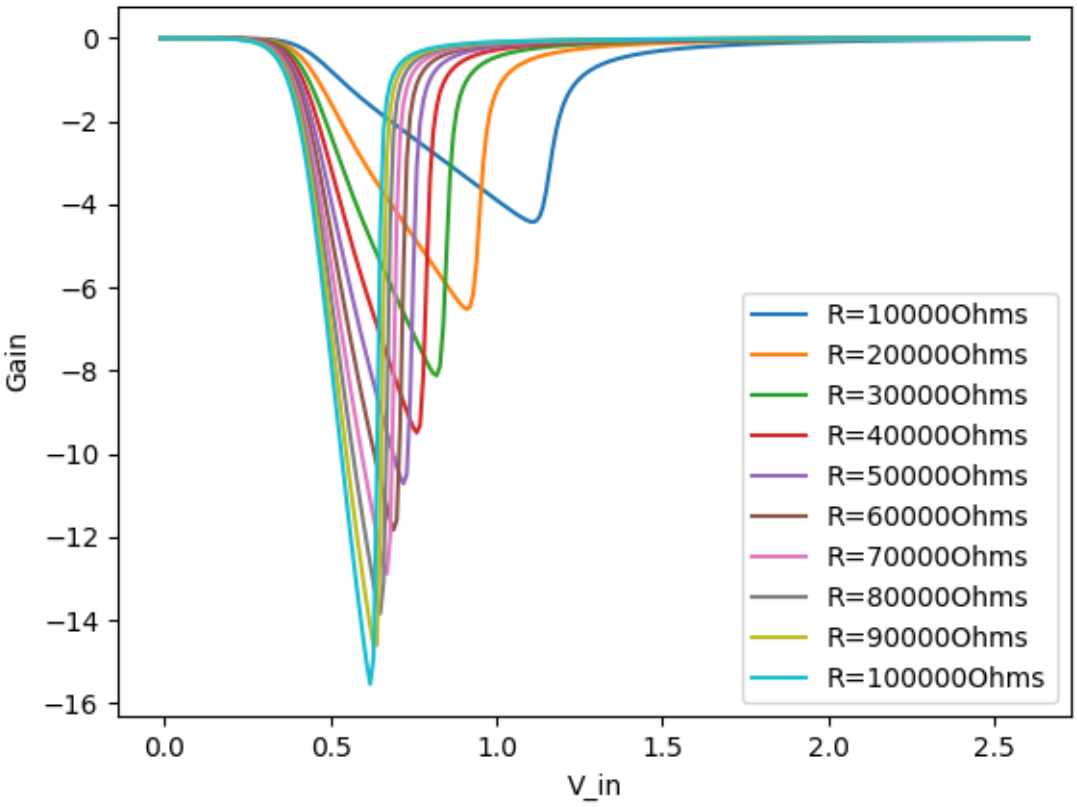

Figure 11: Impact of R_L on PG

```
V2 Vin 0 PULSE(0 2.5 0 0 0 2u 4u)
.control
tran 0.01u 10u 6u
meas tran OP max Vout
meas tran IP max Vin
let va = 0.1*OP
let vb = 0.9*OP
let vc = 0.5*IP
let vd = 0.5*OP
meas TRAN Tr TRIG V(Vout) VAL=va CROSS=1 TARG V(Vout) VAL=vb CROSS=1
meas TRAN Tf TRIG V(Vout) VAL=vb CROSS=2 TARG V(Vout) VAL=va CROSS=2
meas TRAN Tpl TRIG V(Vin) VAL=vc CROSS=1 TARG V(Vout) VAL=vd CROSS=1
meas TRAN Tph TRIG V(Vin) VAL=vc CROSS=2 TARG V(Vout) VAL=vd CROSS=2
.endc
.end
```

Listing 11: Q1-a.cir

- Please find the following observations from the simulations.

Parameters	**Value**
t_r	4.940419e-07
t_f	1.437981e-08
t_{plh}	1.543478e-07
t_{phl}	7.799387e-09
t_{pd}	8.107350e-08

- As the charging and discharging path of capacitor are different(because R_L is much higher than effective linearized on-resistance of MOSFET) we have different Rise and Fall times for V_{out}.
- **Geometric Parameters**:Calculating maximum operating frequency depends on t_p, which in turn depends on t_{phl} and t_{plh}. Calculating t_{phl} depends on R_{eq} of MOSFET. For calculating R_{eq} we need I_{dsat} which also depends on W and L of MOSFET which are geometric parameters.
- **Maximum Operating Frequency**: It depends on propagation delay and from the simulated value of propagation delay, we get maximum frequency to be

$$f_{max} = 1/t_p \tag{1}$$

$$f_{max} = 1/81.07ns \tag{2}$$

$$f_{max} = 12.33MHz \tag{3}$$

- **Dynamic Power Disspation**: It is given by the formulae

$$P_{dyn} = C_L * \Delta V * V_{DD} * f_{max} \tag{4}$$

$$P_{dyn} = 3 * 10^{-12} * (2.5 - 0.463) * 2.5 * 12.33 * 10^6 \tag{5}$$

$$P_{dyn} = 0.225mW \tag{6}$$

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3) $V_{DD} = 1.2V$, $|V_{Tp}| = V_{TN} = 0.3V$, C_L initially discharged.

a) Static power when $V_{IN} = 1.2V$? ✓ ✓ ✓ ✗

→ CMOS inverter does not have a path for current to flow as PMOS is OFF. For the remaining ckts, as all the MOS devices are ON, there is a path for current to flow (so they consume static power)

b) Static power when $V_{IN} = 0V$? ✗ ✗ ✗ ✗

→ None of Inverters consume static power as the MOSFET whose $V_{GS} = V_{in}$ is OFF.

c) V_{OH} of which circuits is 1.2V? ✓ ✗ ✓ ✓

* i) → As the MOS is open $V_{out} = 1.2V$

ii) → As there is no current because of MOSFET whose $V_{GS} = V_{in}$, V_{GT} of upper MOSFET should be zero. $V_{out} = 0.9V$.

iii) → As there is no current because below MOSFET is open, upper MOSFET should have $V_{GT} = 0$, $V_{out} = 1.2V$

iv) → As the lower MOS is open, $V_{out} = 1.2V$.

d) V_{OL} of which circuits is 0V? X X X ✓

First three circuits are closed & hence V_{out} cannot be zero.

But the CMOS circuit is open, because of PMOS. $\therefore V_{out} = 0V$.

e) (-) All the circuits except the CMOS circuit are dependent on relative sizes of transistors. ✓ ✓ ✓ X

4) NMOS Inverter

a) * V_{OH} ⟶ When $V_{in} = 0V$.

⇓

No current in circuit

$$V_{OH} = 2.5V$$

* V_{OL} ⟶ when $V_{in} = 2.5V$ (NMOS in Linear Region)

$$\frac{k'_n}{L}\left((V_{GS} - V_T)V_{OL} - \frac{V_{OL}^2}{2}\right) = \frac{V_{DD} - V_{OL}}{R_L}$$

$$345 \times 10^{-6}\,(75000)\left(2.07\,V_{OL} - \frac{V_{OL}^2}{2}\right) = \frac{2.5V - V_{OL}}{1}$$

$$25.875\left(2.07V_{OL} - \frac{V_{OL}^2}{2}\right) = 2.5 - V_{OL}$$

$$V_{OL} = 46.329mV$$

* V_m → when $V_{in} = V_{out}$ (NMOS in Saturation Region)

$$\frac{k'_n}{2L}(V_m - V_T)^2 = \frac{V_{DD} - V_m}{R_L}$$

$$12.937\,(V_m - 0.43)^2 = 2.5 - V_m$$

$$V_m = 0.7932V$$

b) Expressions for V_{IL}, V_{IH}

$$\frac{dV_{out}}{dV_{in}} = -1 \text{ at } V_{IL} \text{ \& } V_{IH}$$

* V_{IL} (Saturation Region)

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k'_n}{2L}(V_{in} - V_T)^2$$

$$\frac{-1}{R_L}\frac{dV_{out}}{dV_{in}} = \frac{k'_n}{2L}(2)(V_{in} - V_T)$$

$$\frac{1}{R_L} = \frac{k'_n}{L}(V_{in} - V_T)$$

$$V_{in} = V_{IL} = \frac{L}{k'_n R_L} + V_T$$

$$= \frac{1}{345 \times 10^{-6} \times 75000} + V_T$$

$$V_{IL} = 0.468V$$

* V_{IH} (Linear Region)

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k'_n}{L}\left[(V_{in} - V_T)V_{out} - \frac{V_{out}^2}{2}\right] - ①$$

$$\frac{-1}{R_L}\frac{dV_{out}}{dV_{in}} = \frac{k'_n}{L}\left[(V_{in} - V_T)\frac{dV_{out}}{dV_{in}} + V_{out} - \cancel{2}\frac{V_{out}}{\cancel{2}}\frac{dV_{out}}{dV_{in}}\right]$$

$$\frac{1}{R_L} = \frac{k'w}{L}\left[V_T - V_{in} + 2V_{out}\right]$$

$$\frac{L}{R_L k'W} = V_T - V_{in} + 2V_{out}$$

$$V_{in} = V_T + 2V_{out} - \frac{L}{R_L k'W} \quad \text{—(2)}$$

using (2) in (1)

$$2.5 - V_{out} = \underbrace{\frac{R_L k'W}{L}}_{25.875}\left[\left(2V_{out} - \underbrace{\frac{L}{R_L k'W}}_{0.0386}\right)V_{out} - \frac{V_{out}^2}{2}\right]$$

$$V_{out} = 0.25378$$

$$\Downarrow$$

$$V_{IH} = V_{in} = 2 \times 0.25378 + 0.43 - 0.0378$$

$$V_{IH} = 0.89976$$

c) peak gain occurs at V_M

($V_{in} = V_{out}$, Saturation Region)

$$\frac{k'W}{2L}(V_M - V_T)^2 = \frac{V_{DD} - V_{out}}{R_L}$$

$$\left(\frac{k'W}{2L}\right) 2(V_M - V_T) = \frac{-1}{R_L} \left.\frac{dV_{out}}{dV_{in}}\right|_{V_{in}=V_M}$$

$$-\frac{R_L k'W}{L}(V_M - V_T) = \text{peak gain}$$

$\therefore$ peak gain $= 25.875(0.7932 - 0.43)$

$= 9.38V.$