VLSI Design - Assignment-3

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1 Impact of Sizing on Perfomance

1.1 Value of β for $V_M = \frac{V_{DD}}{2}$

- Calculating the appropriate β by trial and error method by simulating the circuit for various values of βs.

```
 * C:\Users\SAI ASHOK\a3_test_3.cir
.include "C:\Users\SAI ASHOK\TSMC180.lib"
.model pch_tt pmos
.model nch_tt nmos
V1 Vin 0 PULSE(1.8 0 0 0 0 1u 2u 0)
M2 Vout Vin 0 0 nch_tt W=0.18u L=0.18u
M1 Vout Vin Vdd Vdd pch_tt W=1.2u L=0.18u
V2 Vdd 0 dc 1.8V
.control
dc v1 0.01 1.8 0.01
run
meas dc vm find vout when vin=vout cross=1
plot vout vs vin
.endc
.end
```

- I have chosen the value of β to be 6.67 to continue with further simulations in this question.

1.2 No External Load

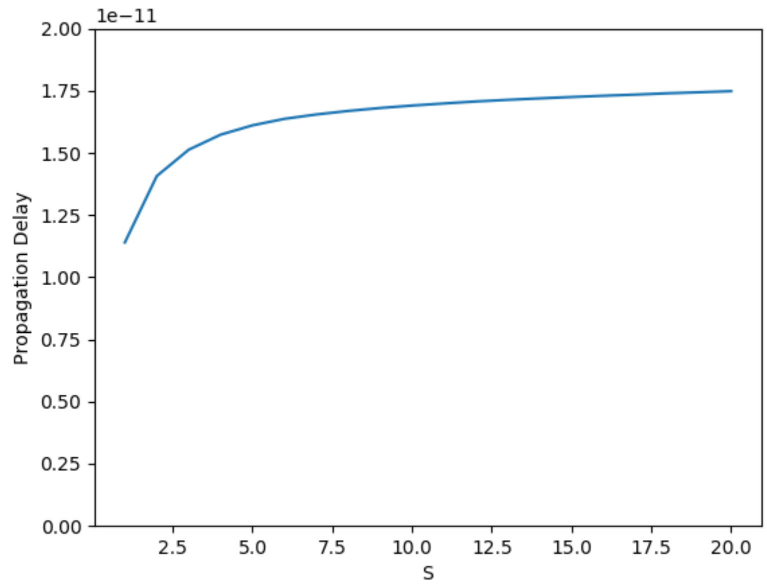
- Simulating the variation of propagation delay with scaling for no external load.

```
* C:\Users\SAI ASHOK\a3_1b.cir
.include "C:\Users\SAI ASHOK\TSMC180.lib"
.model pch_tt pmos
```

```
.model nch_tt nmos
V1 Vin 0 PULSE(1.8 0 0 0 0 1n 2n 0)
M2 Vout Vin 0 0 nch_tt W=0.18u L=0.18u
M1 Vout Vin Vdd Vdd pch_tt W=1.2u L=0.18u
V2 Vdd 0 dc 1.8V
.control
let lh = vector(20)
let hl = vector(20)
let delay = vector(20)
let s = vector(20)
let loop = 0
while loop<20
  let loop = loop + 1
  alter @M1 W=1.2u*loop
  alter @M2 W=0.18u*loop
  tran 1p 5n uic
  run
  *plot vout
  meas tran OP max Vout
  meas tran IP max Vin
  let vc = 0.5*IP
  let vd = 0.5*1.8
  meas TRAN Tlh TRIG V(Vin) VAL=vc CROSS=1 TARG V(Vout) VAL=vd
     CROSS=2
  meas TRAN Thl TRIG V(Vin) VAL=vc CROSS=2 TARG V(Vout) VAL=vd
     CROSS=3
  print loop
  let lh[loop-1] = Tlh
  let hl[loop-1] = Thl
  let delay[loop-1] = (Tlh+Thl)/2
  let s[loop-1] = loop
end
plot delay vs s
wrdata fig2.dat delay vs s
.endc
.end
```

- The graph obtained from simulations suggests that propagation delay is almost constant(variations of the order picoseconds) with scaling.

Scaling Factor	**Propagation Delay**
1	1.13980915e-11
2	1.40667000e-11
3	1.51252790e-11
4	1.57304455e-11
5	1.61057270e-11
6	1.63668215e-11
7	1.65432560e-11
8	1.66849085e-11
9	1.68030630e-11
10	1.69013220e-11
11	1.69855645e-11
12	1.70659515e-11
13	1.71312880e-11
14	1.71900750e-11
15	1.72455125e-11
16	1.72960025e-11
17	1.73413895e-11
18	1.73947970e-11
19	1.74360210e-11
20	1.74799015e-11



1.3 External Load of 20pF

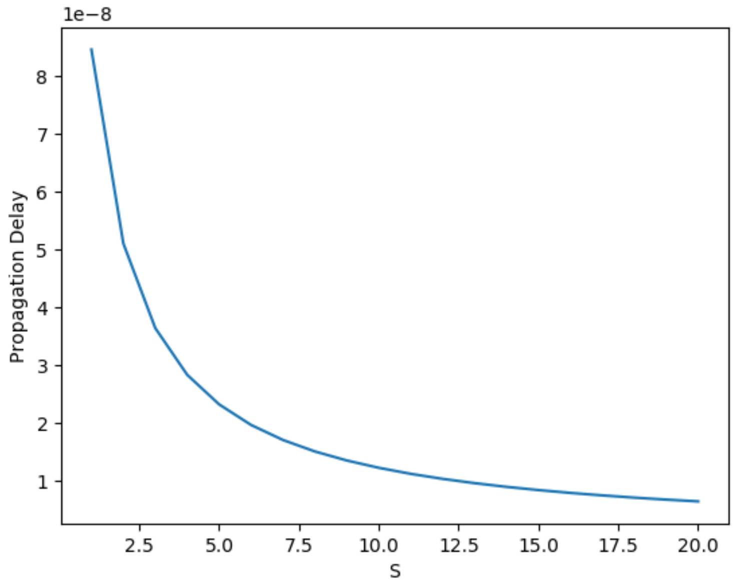
- Simulating the variation of propagation delay with scaling for an external load of 20pF.

```
* C:\Users\SAI ASHOK\a3_1a.cir
.include "C:\Users\SAI ASHOK\TSMC180.lib"
.model pch_tt pmos
.model nch_tt nmos
V1 Vin 0 PULSE(1.8 0 0 0 0 1u 2u 0)
M2 Vout Vin 0 0 nch_tt W=0.18u L=0.18u
M1 Vout Vin Vdd Vdd pch_tt W=1.2u L=0.18u
V2 Vdd 0 dc 1.8V
C Vout 0 20p
.control
let lh = vector(20)
let hl = vector(20)
let delay = vector(20)
let s = vector(20)
let loop = 0
while loop<20
  let loop = loop + 1
  alter @M1 W=1.2u*loop
```

```
  alter @M2 W=0.18u*loop
  tran 1n 5u uic
  run
  *plot vout
  meas tran OP max Vout
  meas tran IP max Vin
  let vc = 0.5*IP
  let vd = 0.5*OP
  meas TRAN Tlh TRIG V(Vin) VAL=vc CROSS=1 TARG V(Vout) VAL=vd
     CROSS=1
  meas TRAN Thl TRIG V(Vin) VAL=vc CROSS=2 TARG V(Vout) VAL=vd
     CROSS=2
  print loop
  let lh[loop-1] = Tlh
  let hl[loop-1] = Thl
  let delay[loop-1] = (Tlh+Thl)/2
  let s[loop-1] = loop
end
plot delay vs s
wrdata fig1.dat delay vs s
.endc
.end
```

- The graph obtained from simulations suggests that propagation delay decreases with scaling(variations of the order nanoseconds).

Scaling Factor	**Propagation Delay**
1	8.46420350e-08
2	5.10769100e-08
3	3.64366550e-08
4	2.83513600e-08
5	2.32364750e-08
6	1.96766550e-08
7	1.70734100e-08
8	1.50893990e-08
9	1.35262940e-08
10	1.22633740e-08
11	1.12196165e-08
12	1.03492665e-08
13	9.60793300e-09
14	8.96657450e-09
15	8.41090650e-09
16	7.91747000e-09
17	7.49028200e-09
18	7.10262400e-09
19	6.75987900e-09
20	6.44903150e-09



1.4 Variation of t_{plh} with W_p

- As we increase W_p the pull up network becomes stronger and t_{lh} decreases. Variation of W_p will have no effect on t_{hl}.

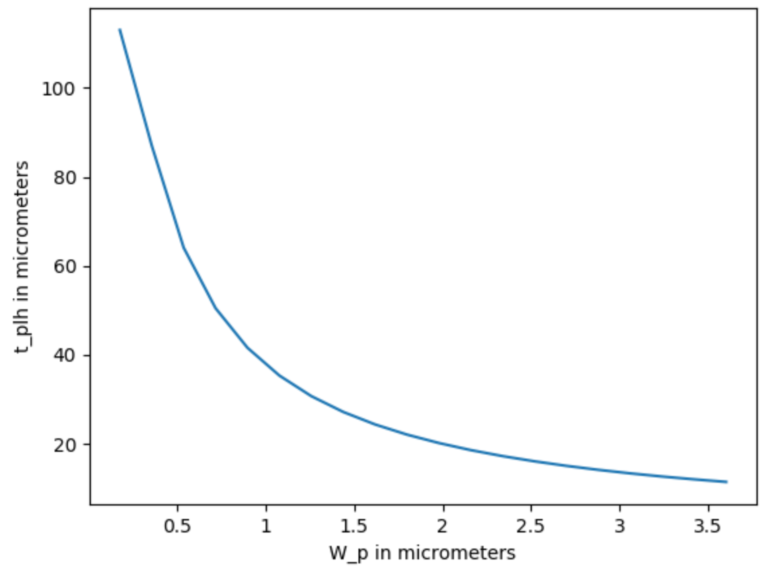
```
* C:\Users\SAI ASHOK\a3_wp.cir
.include "C:\Users\SAI ASHOK\TSMC180.lib"
.model pch_tt pmos
.model nch_tt nmos
V1 Vin 0 PULSE(1.8 0 0 0 0 1m 2m 0)
M2 Vout Vin 0 0 nch_tt W=0.18u L=0.18u
M1 Vout Vin Vdd Vdd pch_tt W=0.18u L=0.18u
C Vout 0 10n
V2 Vdd 0 dc 1.8V
.control
let lh = vector(20)
let hl = vector(20)
let delay = vector(20)
let wp = vector(20)
let loop = 0
while loop<20
  let loop = loop+1
  alter @M1 W=0.18u*loop
```

```
  tran 1u 5m
  run
  *plot vout
  meas tran OP max Vout
  meas tran IP max Vin
  let vc = 0.5*IP
  let vd = 0.5*OP
  meas TRAN Tlh TRIG V(Vin) VAL=vc CROSS=1 TARG V(Vout) VAL=vd
     CROSS=1
  meas TRAN Thl TRIG V(Vin) VAL=vc CROSS=2 TARG V(Vout) VAL=vd
     CROSS=2
  let lh[loop-1] = Tlh
  let hl[loop-1] = Thl
  let delay[loop-1] = (Tlh+Thl)/2
  let wp[loop-1] = loop*0.18u

end
plot lh vs wp
wrdata fig4.dat lh vs wp
.endc
.end
```

- The graph obtained from simulations suggests that t_{plh} decreases with increase in W_p supporting the theory discussed in class.

W_p	t_{plh}
1.80e-07	1.130081e-04
3.60e-07	8.702253e-05
5.40e-07	6.407451e-05
7.20e-07	5.046961e-05
9.00e-07	4.157633e-05
1.08e-06	3.533057e-05
1.26e-06	3.070895e-05
1.44e-06	2.715692e-05
1.62e-06	2.434122e-05
1.80e-06	2.205642e-05
1.98e-06	2.016575e-05
2.16e-06	1.857430e-05
2.34e-06	1.722012e-05
2.52e-06	1.605093e-05
2.70e-06	1.503236e-05
2.88e-06	1.413729e-05
3.06e-06	1.334381e-05
3.24e-06	1.263423e-05
3.42e-06	1.200261e-05
3.60e-06	1.142871e-05



1.5 Variation of t_{phl} with W_n

- As we increase W_n the pull down network becomes stronger and t_{hl} decreases. Variation of W_n will have no effect on t_{lh}.

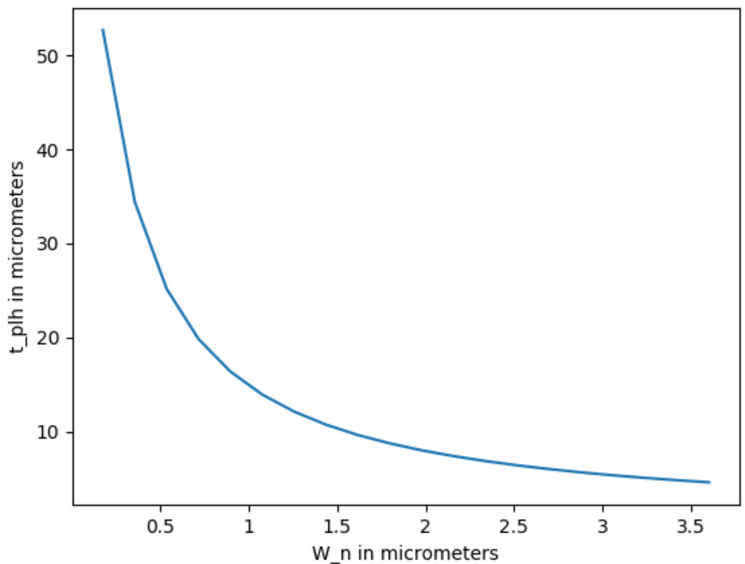
```
* C:\Users\SAI ASHOK\a3_wn.cir
.include "C:\Users\SAI ASHOK\TSMC180.lib"
.model pch_tt pmos
.model nch_tt nmos
V1 Vin 0 PULSE(1.8 0 0 0 0 1m 2m 0)
M2 Vout Vin 0 0 nch_tt W=0.18u L=0.18u
M1 Vout Vin Vdd Vdd pch_tt W=0.18u L=0.18u
C Vout 0 10n
V2 Vdd 0 dc 1.8V
.control
let lh = vector(20)
let hl = vector(20)
let delay = vector(20)
let wn = vector(20)
let loop = 0
while loop<20
  let loop = loop+1
  alter @M2 W=0.18u*loop
```

```
  tran 1u 5m
  run
  *plot vout
  meas tran OP max Vout
  meas tran IP max Vin
  let vc = 0.5*IP
  let vd = 0.5*OP
  meas TRAN Tlh TRIG V(Vin) VAL=vc CROSS=1 TARG V(Vout) VAL=vd
     CROSS=1
  meas TRAN Thl TRIG V(Vin) VAL=vc CROSS=2 TARG V(Vout) VAL=vd
     CROSS=2
  let lh[loop-1] = Tlh
  let hl[loop-1] = Thl
  let delay[loop-1] = (Tlh+Thl)/2
  let wn[loop-1] = loop*0.18u

end
plot hl vs wn
wrdata fig5.dat hl vs wn
.endc
.end
```

- The graph obtained from simulations suggests that t_{phl} decreases with increase in W_n supporting the theory discussed in class.

W_n	$t_{phl}\}$
1.80e-07	5.269339e-05
3.60e-07	3.442960e-05
5.40e-07	2.517161e-05
7.20e-07	1.982556e-05
9.00e-07	1.636824e-05
1.08e-06	1.391895e-05
1.26e-06	1.210850e-05
1.44e-06	1.071959e-05
1.62e-06	9.621842e-06
1.80e-06	8.731455e-06
1.98e-06	7.994882e-06
2.16e-06	7.377894e-06
2.34e-06	6.851755e-06
2.52e-06	6.395959e-06
2.70e-06	6.001310e-06
2.88e-06	5.651744e-06
3.06e-06	5.341441e-06
3.24e-06	5.065535e-06
3.42e-06	4.820585e-06
3.60e-06	4.596671e-06



2 Ring Oscillator

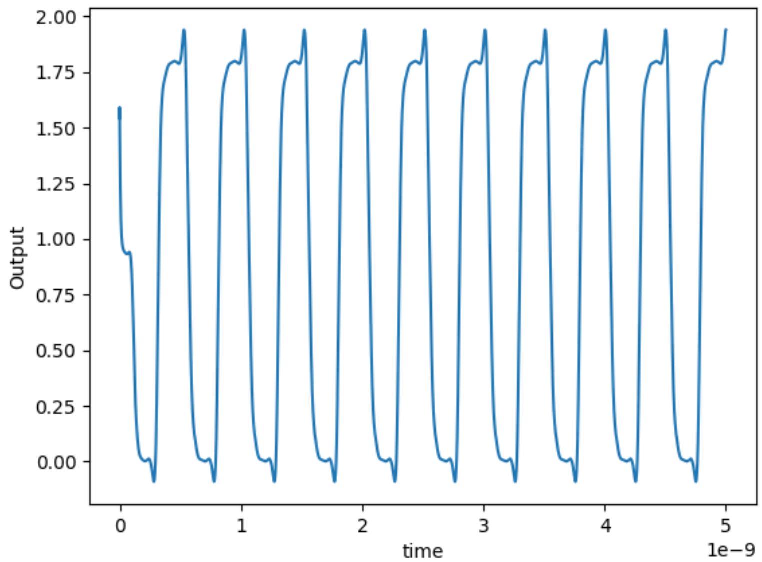
2.1 Time Response over ten periods

- Ring Oscillators are used to calculate propagation delay of inverters in real life.
- The values of parameters have been chosen in such a way that the results of this simulation can be compared with the propagation delay of inverter simulated in the first question.
- The following netlist has been used to simulate the circuit of a ring oscillator.

```
* C:\Users\SAI ASHOK\a3_q2.cir
.include "C:\Users\SAI ASHOK\TSMC180.lib"
.model pch_tt pmos
.model nch_tt nmos
M1 s1 s7 0 0 nch_tt W=0.18u L=0.18u
M2 s2 s1 0 0 nch_tt W=0.18u L=0.18u
M3 s3 s2 0 0 nch_tt W=0.18u L=0.18u
M4 s4 s3 0 0 nch_tt W=0.18u L=0.18u
```

```
M5 s5 s4 0 0 nch_tt W=0.18u L=0.18u
M6 s6 s5 0 0 nch_tt W=0.18u L=0.18u
M7 s7 s6 0 0 nch_tt W=0.18u L=0.18u
M8 s1 s7 Vdd Vdd pch_tt W=1.2u L=0.18u
M9 s2 s1 Vdd Vdd pch_tt W=1.2u L=0.18u
M10 s3 s2 Vdd Vdd pch_tt W=1.2u L=0.18u
M11 s4 s3 Vdd Vdd pch_tt W=1.2u L=0.18u
M12 s5 s4 Vdd Vdd pch_tt W=1.2u L=0.18u
M13 s6 s5 Vdd Vdd pch_tt W=1.2u L=0.18u
M14 s7 s6 Vdd Vdd pch_tt W=1.2u L=0.18u
V1 Vdd 0 1.8
.control
tran 1p 5n uic
run
meas TRAN T1 TRIG V(s7) VAL=1 CROSS=3 TARG V(s7) VAL=1 CROSS=5
let f = 1/T1
let t_p = T1/14
print t_p
plot s7
wrdata fig3.dat s7
.endc
.end
```

- The time response of the ring oscillator for 10 periods is given below.



- The frequency of the output as observed from simulation is 2.0134GHz.

2.2 Propagation Delay from Ring Oscillator

- Propgation delay can be calculated from the frequency of output obtained from ring oscillator using the formula

$$t_p = \frac{1}{2Nf}. \tag{1}$$

- The value of propagation delay obtained from the simulation of ring oscillator is 3.5476 x 10^{-11}.
- The value of propagation delay observed in the simulations of first question for S = 1 is equal to 1.1398 x 10^{-11} which is slightly lower than the value obtained from Ring Oscillator(because of overhead capacitances in Ring Oscillator).

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2)

c) o frequency of oscillations when all the inverters are sized up by S.

(No external Capacitor has been considered in Ring oscillator)

$$* \; t_p = t_{p_0}\left(1+\frac{C_{g,j+1}^{\circ}}{C_{g,j}^{\circ}}\right)\Bigg|_{j=1,2,3,4,5,6,7}$$

$$= 2N t_{p_0} \quad \text{(before sizing)}$$

* After sizing

$$t_p = 0.69\, \frac{R_{eq,j}^{\circ}}{\cancel{S}} \times C_{g,j}^{\circ} \times \cancel{S}\left(1+\frac{C_{g,j+1}^{\circ}\times \cancel{S}}{C_{g,j}^{\circ}\times \cancel{S}}\right)\Bigg|_{j=1,2,3,4,5,6,7}$$

$$t_p = t_{p_0}(2N)$$

↳ (of the whole Ring oscillator)

As t_p does not change, f does not change.

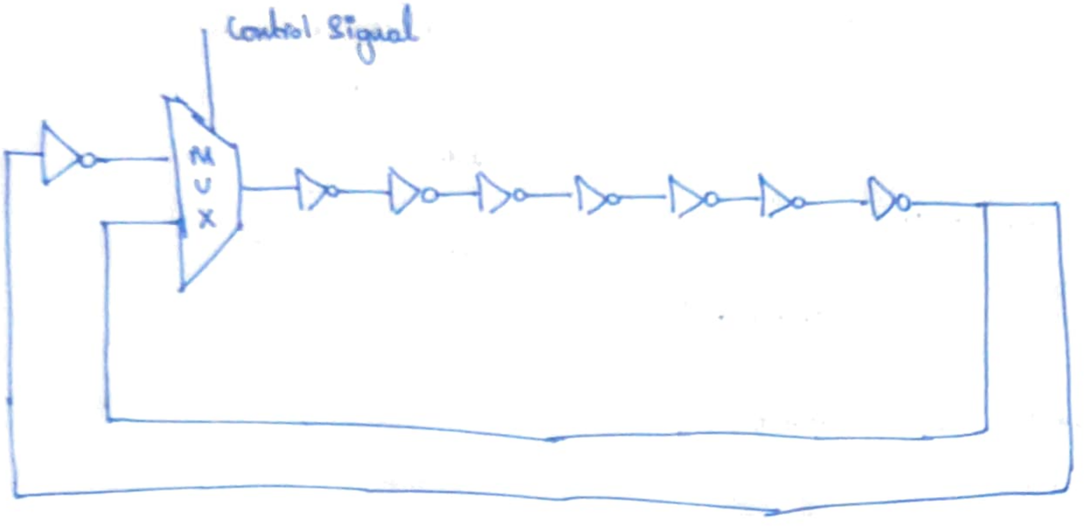
o power consumption when all inverters are sized up by S.

$$P = N C_g V_{dd}^2 f \quad \text{(before sizing)}$$

$$P = N(S C_g) V_{dd}^2 f \quad \text{(after sizing)}$$

does not change.

d) Modification to ring oscillator circuit.

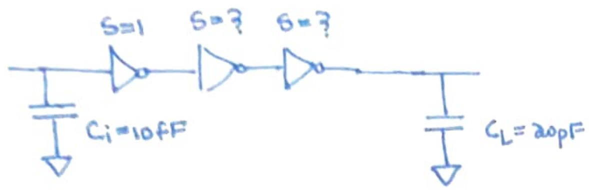


- when control signal is 1, Ring oscillator will be in OFF mode
- when control signal is 0, Ring oscillator will be in ON mode.

3) Sizing of Inverters

driving a load of 20pF with two staged buffer. tp of minimum sized inverter is 70ps

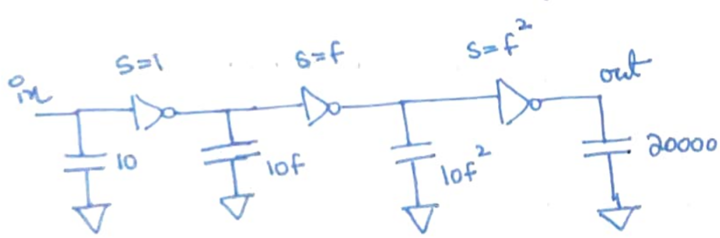
input capacitance = 10fF.



a) determine sizing of the two additional buffer stages

sizing of inverters must be in G.P

1, f, f^2 respectively. (considering $\gamma=1$)



* $10f^3 = 20000$

$f = \sqrt[3]{2000}$

$f = 12.6$

* sizing of the inverters are

1, 12.6, 158.76.

* delay with this sizing

$tp = 3 \times 70ps \left(1 + \frac{12.6}{1}\right) = 2.8ns$

b) No. of stages to achieve minimum delay. What is tp in this case.

* for $\gamma = 1$, f_{opt} would be 3.6.

$$N = \frac{\ln(2000)}{\ln(3.6)} = 5.93 \sim \underline{\underline{6}}$$

* tp in this case $= N t_{p_0} \left(1 + \frac{f}{\gamma}\right)$

$= 6\,(70ps)\,(4.6)$

$= 1.932 ns.$

c) Advantages & Disadvantages of methos mentioned above.

v

* for a fixed, fan out at each stage should be in GP to get min delay.

* for a fixed F, we can determine N_{opt} to obtain minimum delay

for a fixed γ.

* there is a trade off between delay & the area occupied by the inverters, while sizing up & increasing No. of inverters.

d) Closed form expression for the power consumption in the circuit.

In this circuit we can ignore static power consumption, direct current leakage as N is small.

$$P_{dyn} = f C_i V_{DD}^2 \left(\frac{1}{T}\right) + f^2 C_i V_{DD}^2 \left(\frac{1}{T}\right) + f^3 C_i V_{DD}^2 \left(\frac{1}{T}\right)$$

$$= C_i V_{DD}^2 \left(\frac{1}{T}\right) \sum_{j=0}^{3} f^j$$

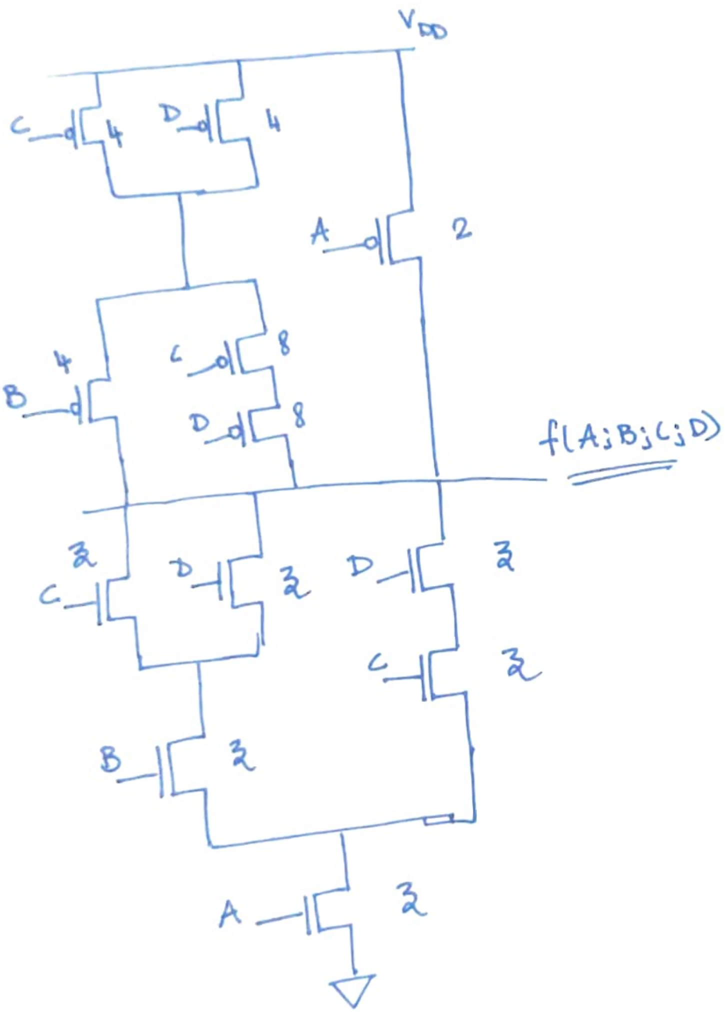
$$= 10 \times 10^{-15} (2.5)(2.5) \left(\frac{1}{T}\right) \left[f + f^2 + f^3\right]$$

$$= 135.796 \times 10^{-12} \left(\frac{1}{T}\right) W$$

$$= 135.796 \left(\frac{1}{T}\right) pW.$$

4) Complex CMOS logic gate implementing

$$f(A;B;C;D) = \overline{A\cdot(B\cdot(C+D)+C\cdot D)}$$



* Assumption $R_p = 2R_n$

5) parameters of given technology:

$V_{Tn} = 0.2V$ $|V_{Tp}| = 0.3V$ $R_n = 2k\Omega * \mu m$ $R_p = 3k\Omega * \mu m$ $V_{DD} = 1V$

$w_p = w_n = 1\mu m$

Draw VTC.

Sol:

given that R_{on} (NMOS) = $2k\Omega$ (at $w_n = 1\mu m$)

R_{on} (PMOS) = $3k\Omega$ (at $w_p = 1\mu m$)

* initially $V_{DD} = 1V$; $V_{in} = 0V$ PMOS is ON & NMOS is OFF. As the circuit is not complete $V_{out} = 1V$

* when V_{in} reaches 0.2V, NMOS turns on & the circuit will be equivalent to a simple voltage divider circuit & $V_{out} = 1 \times \frac{2}{5} = 0.4V$

* when V_{in} becomes greater than 0.7V, PMOS turns off, $V_{out} = 0V$