

Diving Deep into Neuromorphic Computing with Intel's Loihi

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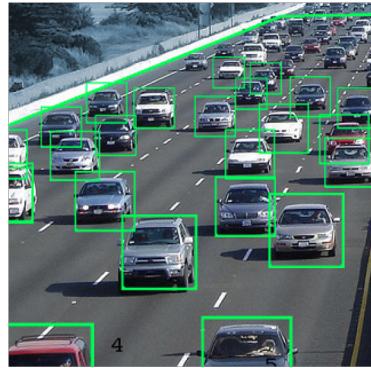
Computational needs of massive data



Automatic Driving



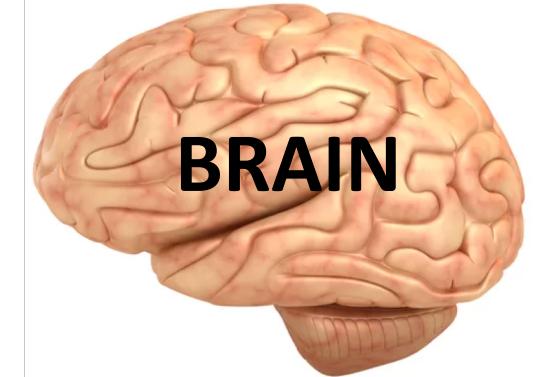
Robotics



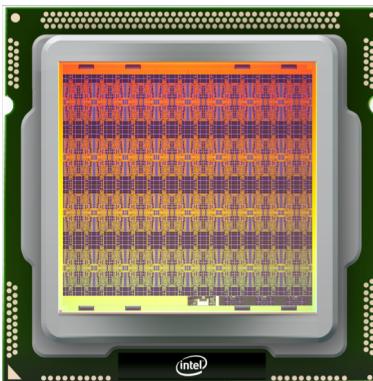
Computer Vision



Nature has already come up with something amazing.

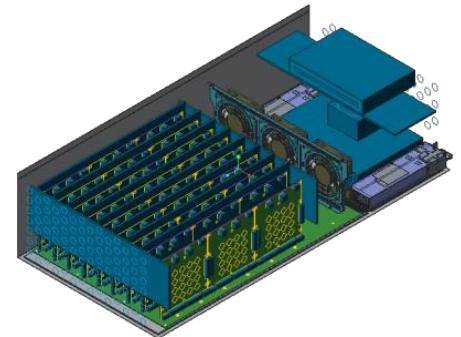


Neuromorphic Hardware: Spiking Neural Network in Silicon



Intel's Loihi

- Energy Minimization
- Asynchronized Parallelism
- Fully distributed memory
- Fast Response Time

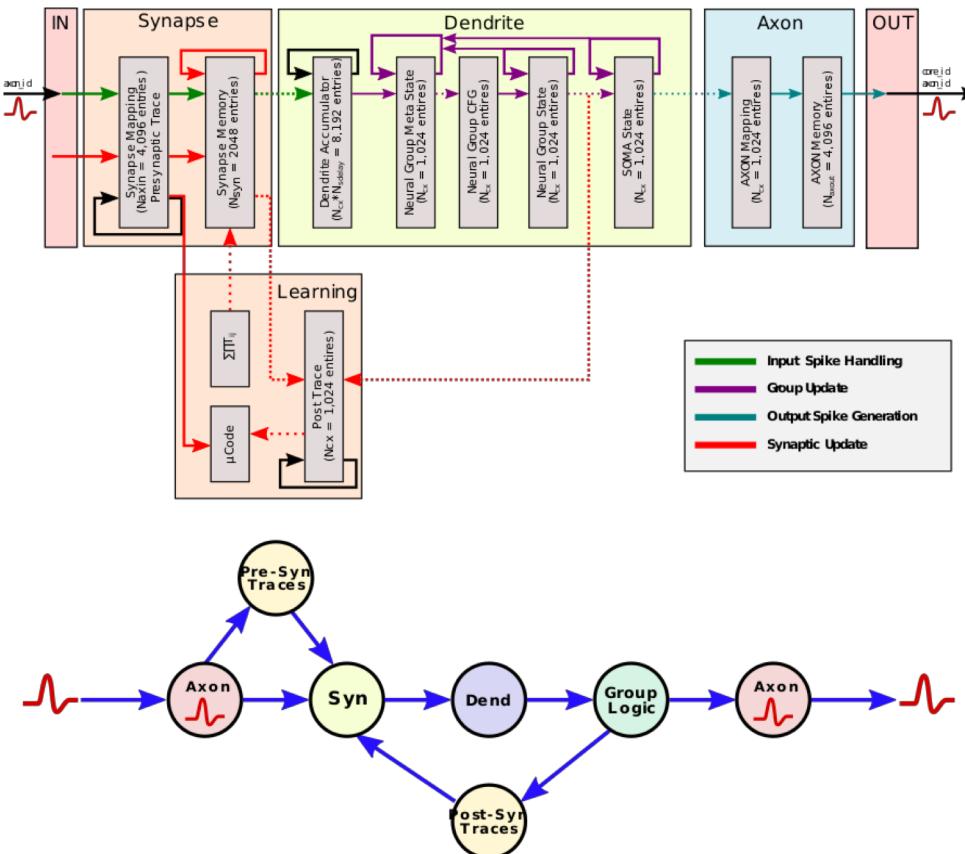


Large Scale Brain Simulation

400 Million Spiking Neurons
100 Billion Synapses

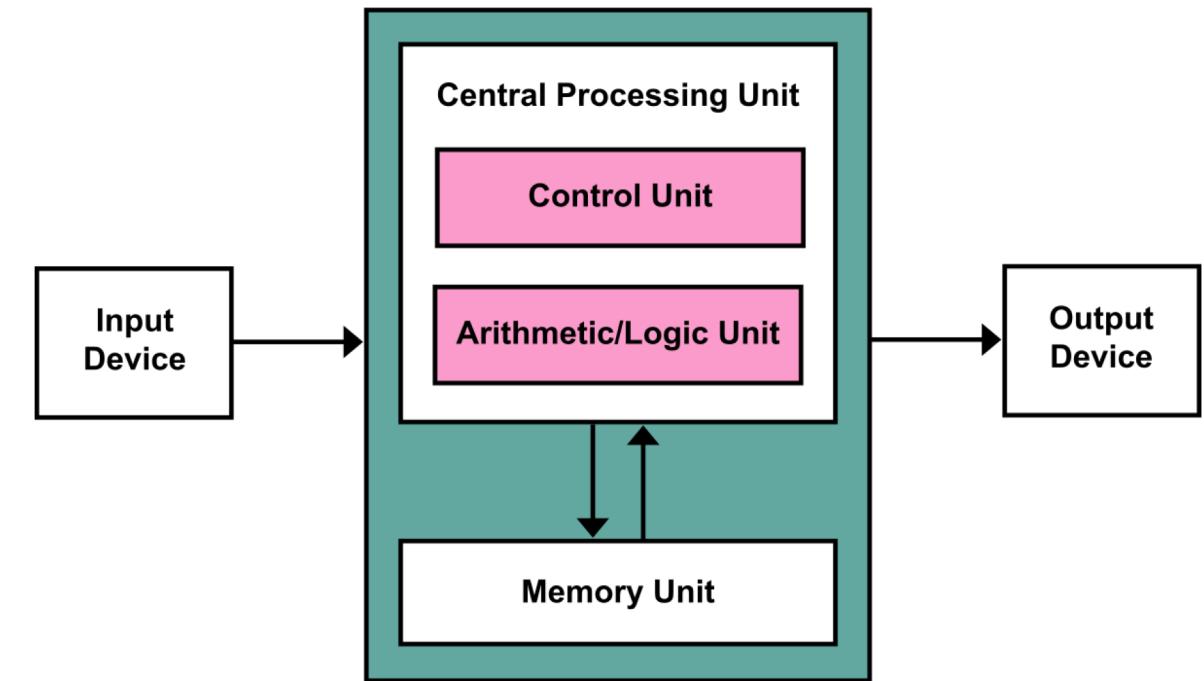


Neuromorphic Processor



Distributed Memory with Asynchronous Parallelism

Von Neumann Architecture

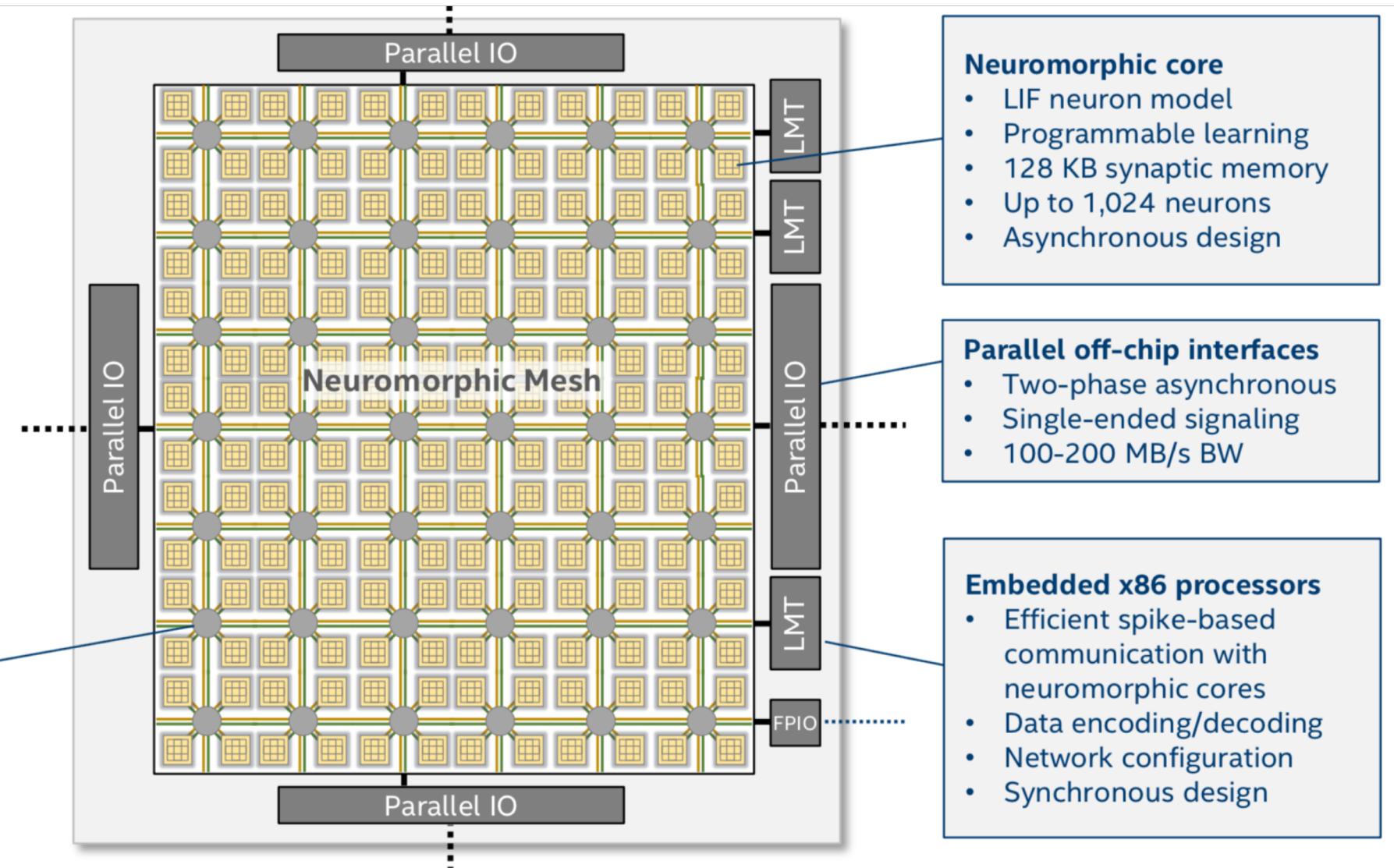


Central Memory with Blocking Parallelism



Intel's Loihi Neuromorphic Processor

Technology:	14nm
Die Area:	60 mm ²
Core area:	0.41 mm ²
NmC cores:	128 cores
x86 cores:	3 LMT cores
Max # neurons:	128K neurons
Max # synapses:	128M synapses
Transistors:	2.07 billion



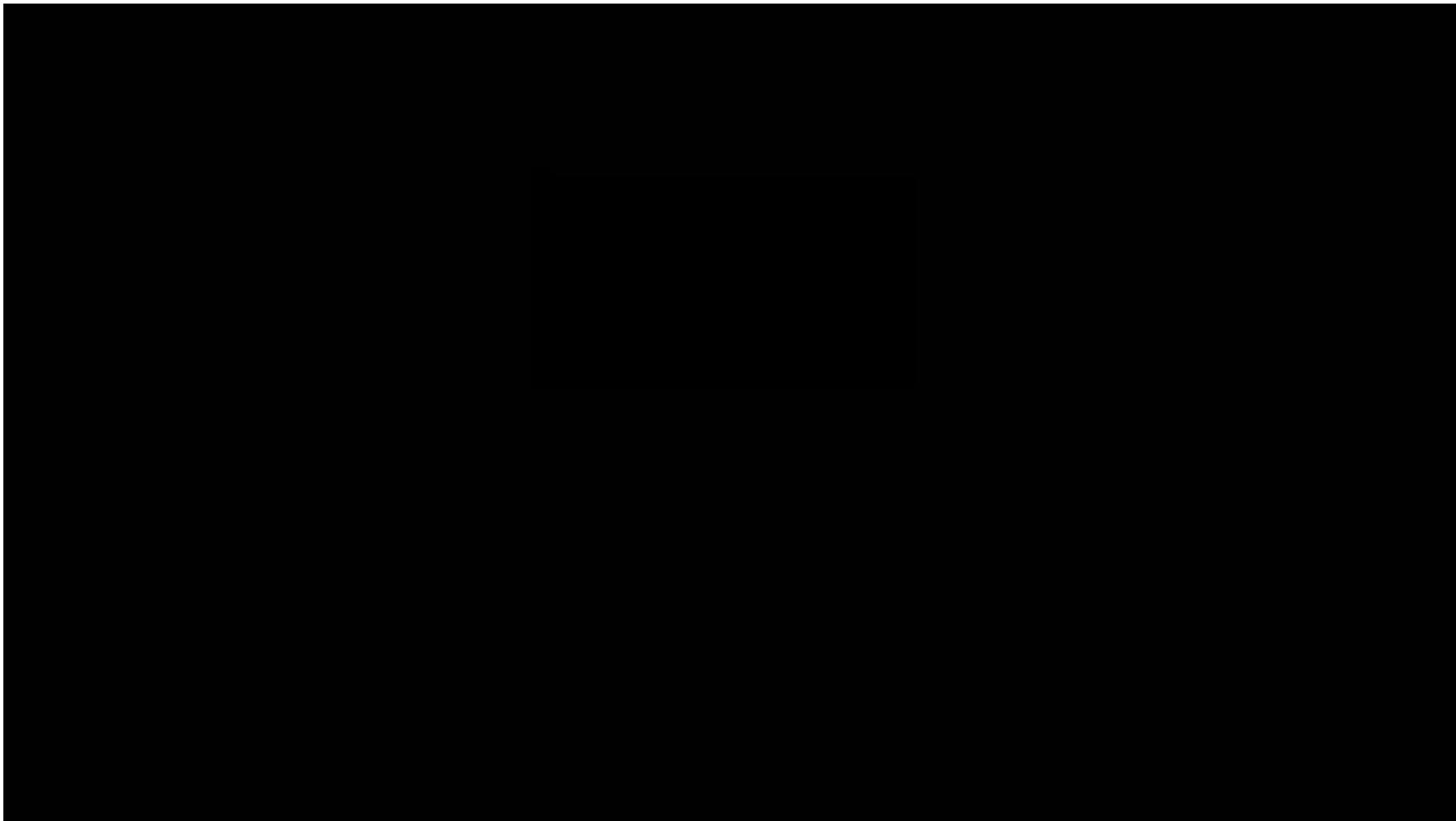


Intel's Loihi Neuromorphic Processor

	Bare Loihi Chip	Kapoho Bay	Oheo Gulch	Nahuku	Pohoiki Springs
Loihi	1	2	Up to 5	Up to 32	Up to 768
Neurons	128k	256k	640k	4M	100M
Synapses	100M	200M	500M	4B	100B
Interface	Async	USB	Async	Async	Ethernet



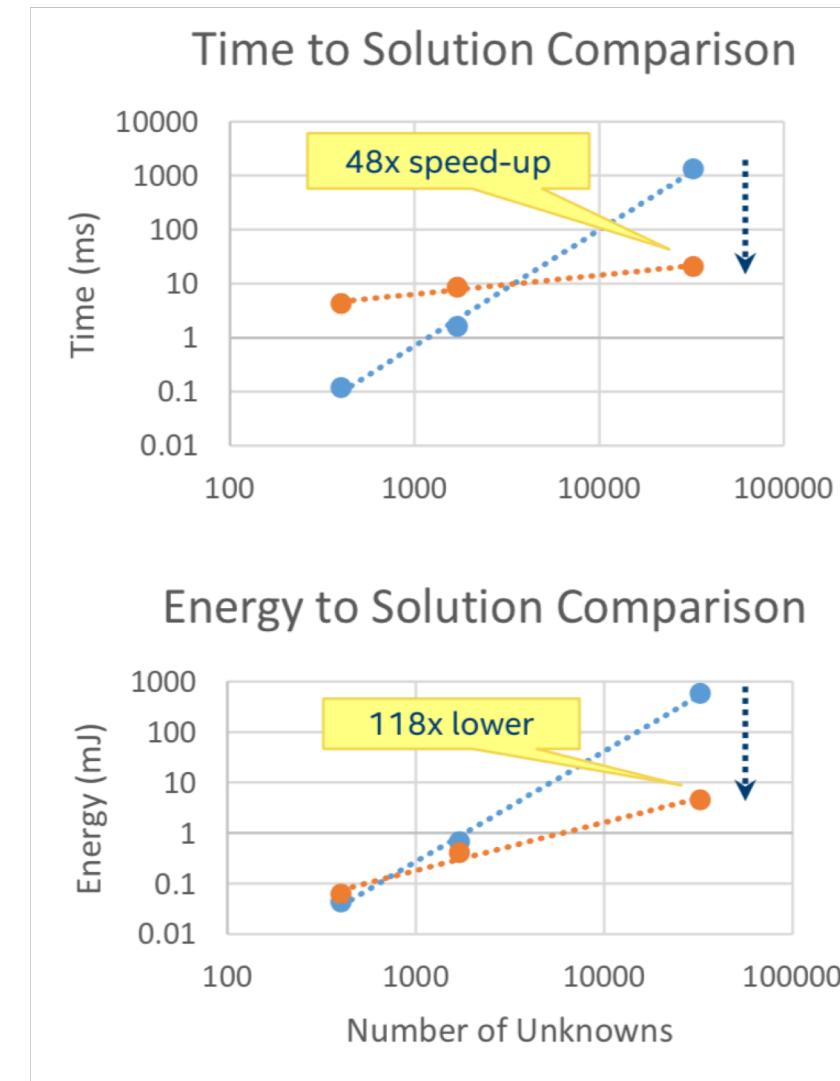
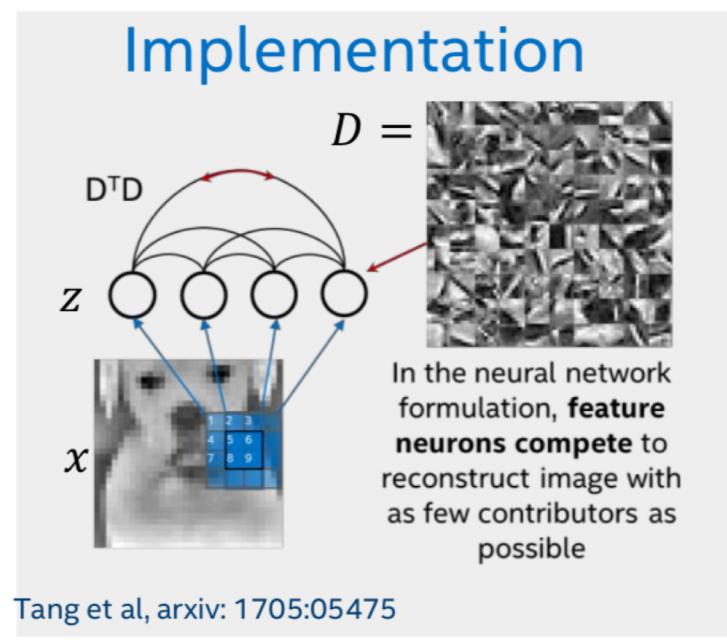
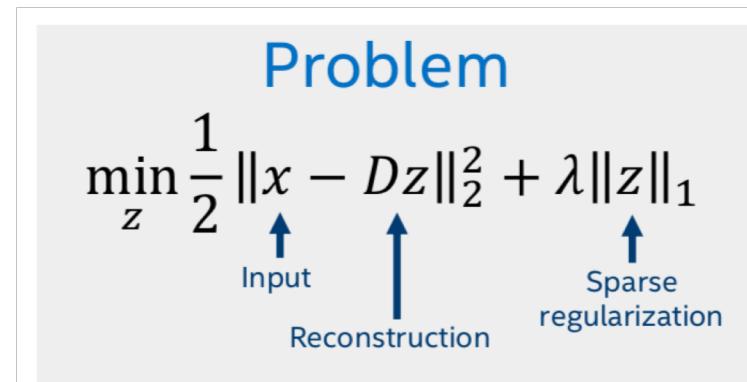
Demo 1: Adaptive Robotic Control on Nengo



(<https://appliedbrainresearch.com/research/#adaptive-manipulators>)



Demo 2: Sparse Coding for Image Processing



(Davies, et al. IEEE Micro, 2018)

Loihi Computation

Level 1: Phase Level



Level 2: Neuron Level



Level 3: Learning Level



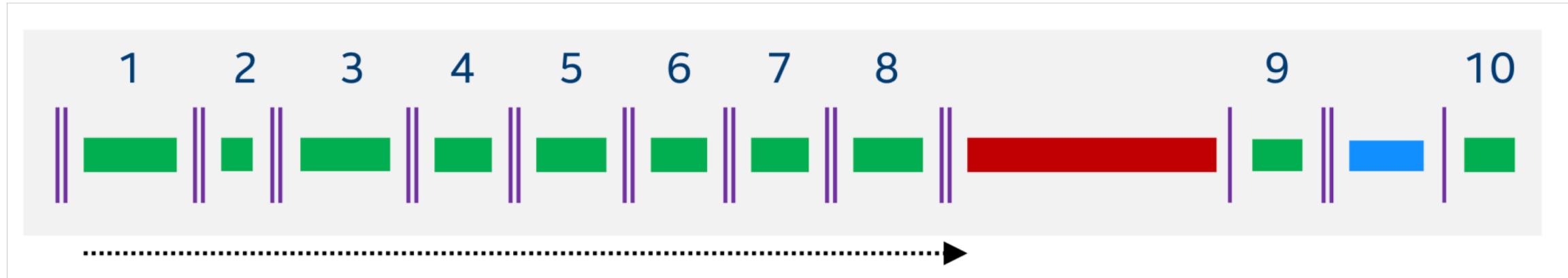
Level 4: SNIPs Level



Loihi Computation 1: Phase Level



- Check Input Spikes
 - Update Neurons
 - Transfer Spikes
 - ...
- Update Trace
 - Update Weight
 - Update Delay and Trace
 - ...
- Run custom SNIPs
 - Change Parameters
 - Monitor Probes
 - ...



Loihi Computation 2: Neuron Level

Neuron Level 1: Compartments



Neuron Level 2: Dendritic Tree



Neuron Level 3: Synapses and Spikes



Neuron Level 1: Compartments (LIF)

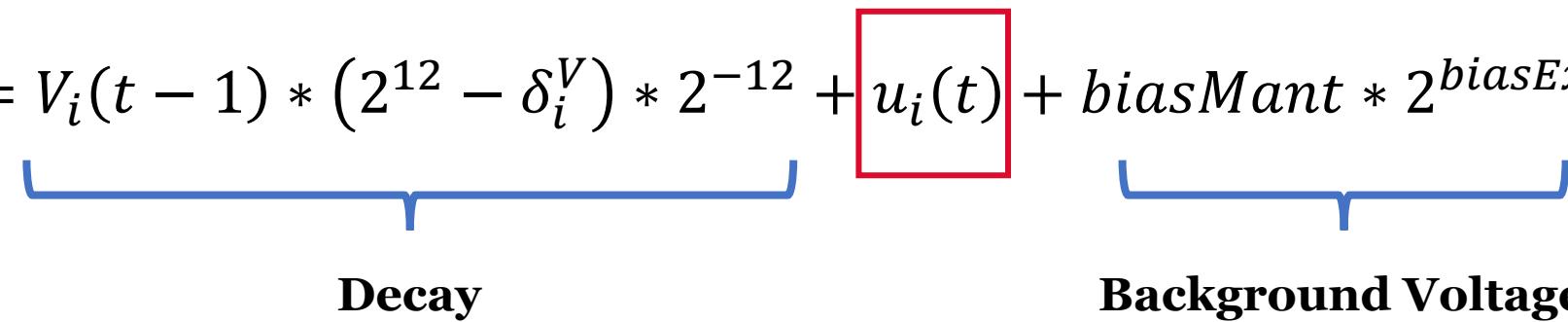
Compartment Current

$$u_i(t) = u_i(t - 1) * (2^{12} - \delta_i^u) * 2^{-12} + 2^6 \sum_j w_{ij} * s_j(t)$$



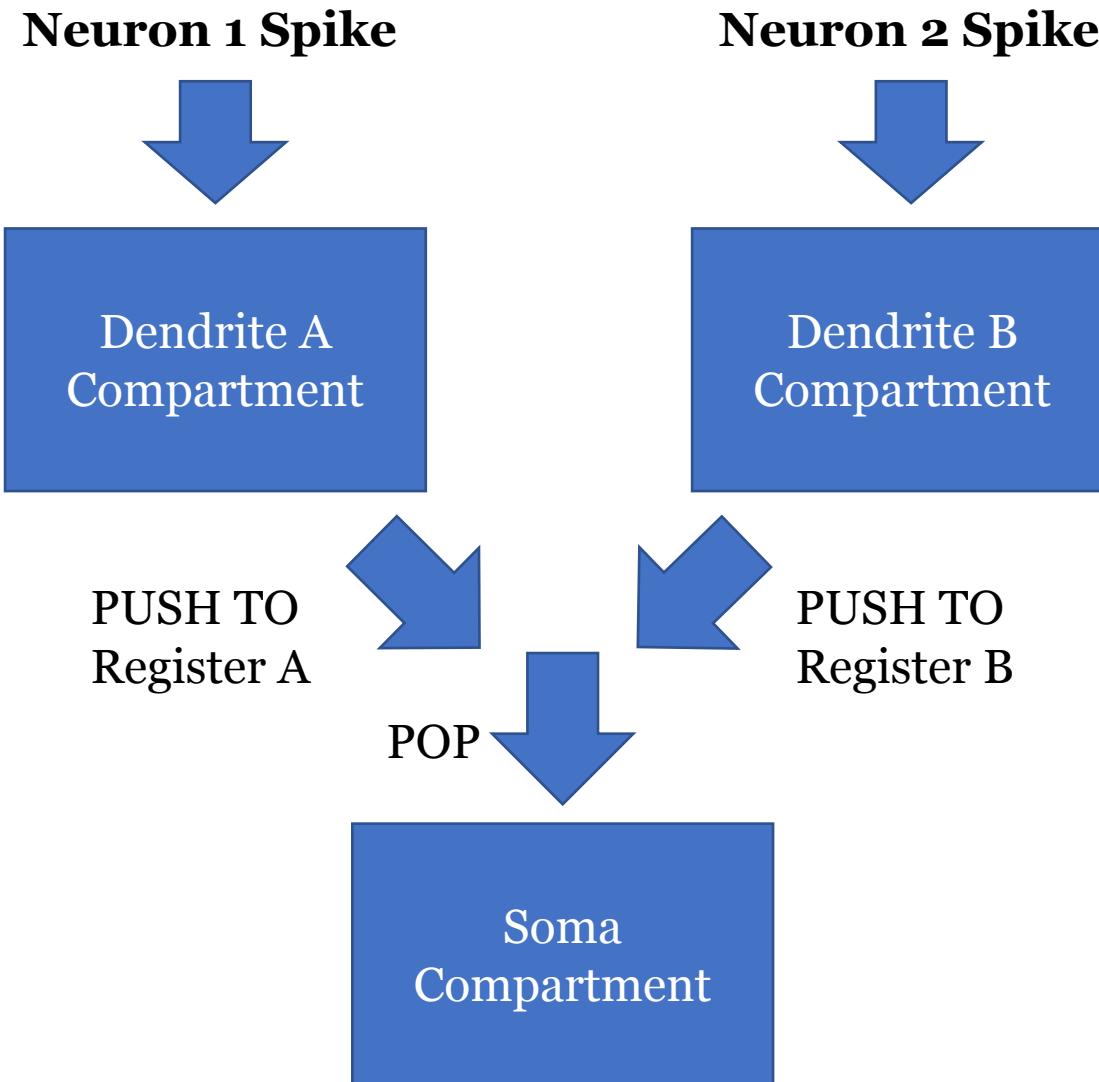
Compartment Voltage

$$V_i(t) = V_i(t - 1) * (2^{12} - \delta_i^V) * 2^{-12} + u_i(t) + biasMant * 2^{biasExp}$$





Neuron Level 2: Dendrite Tree



ADD: $C.dV = C.U + A.V + B.V$

MAX: $C.dV = \max(C.U, A.V, B.V)$

MIN: $C.dV = \min(C.U, A.V, B.V)$

PASS: $C.dV = A.S? C.U + B.V : 0$

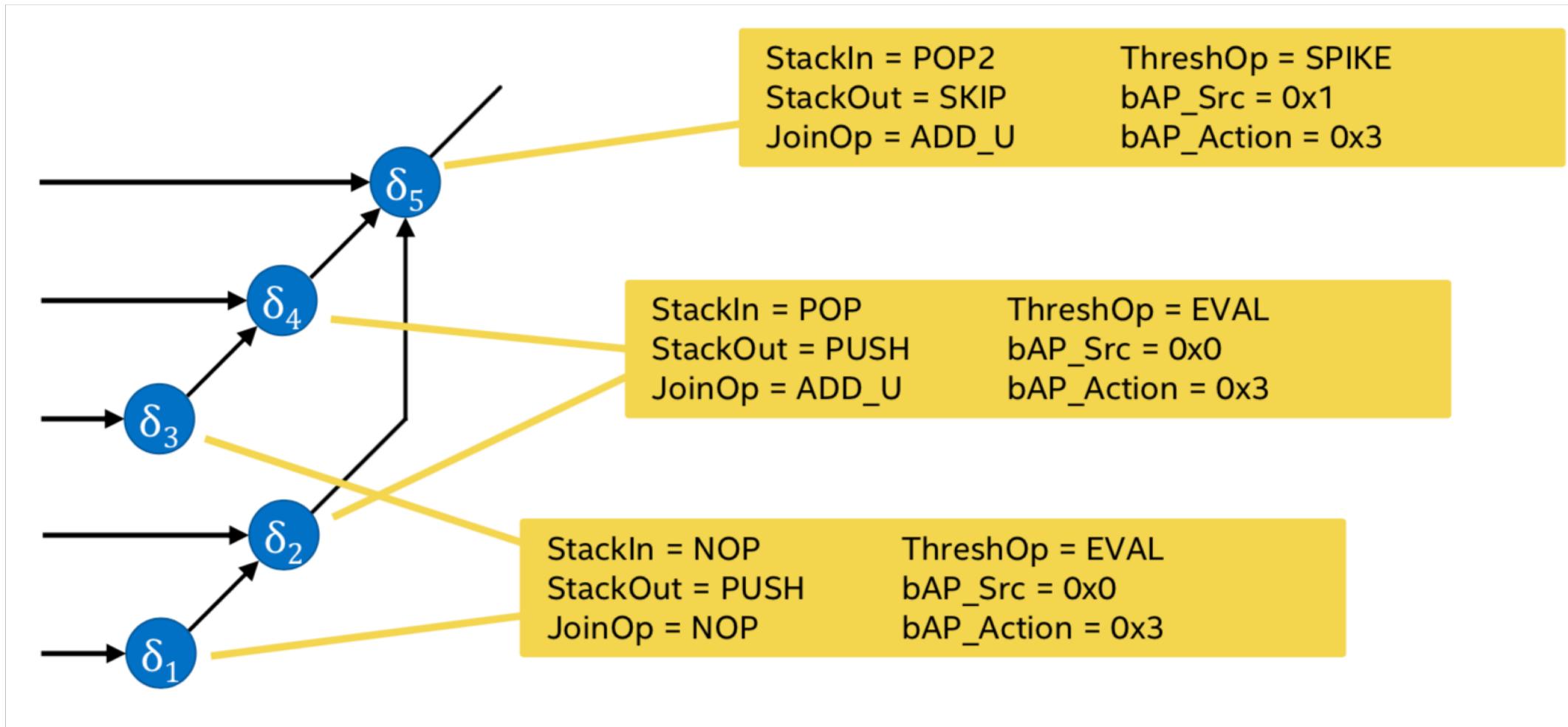
BLOCK: $C.dV = A.S? 0 : C.U + B.V$

OR: $C.dS = A.S | B.S | C.S$

AND: $C.dS = A.S \& B.S \& C.S$



Neuron Level 2: Dendrite Tree

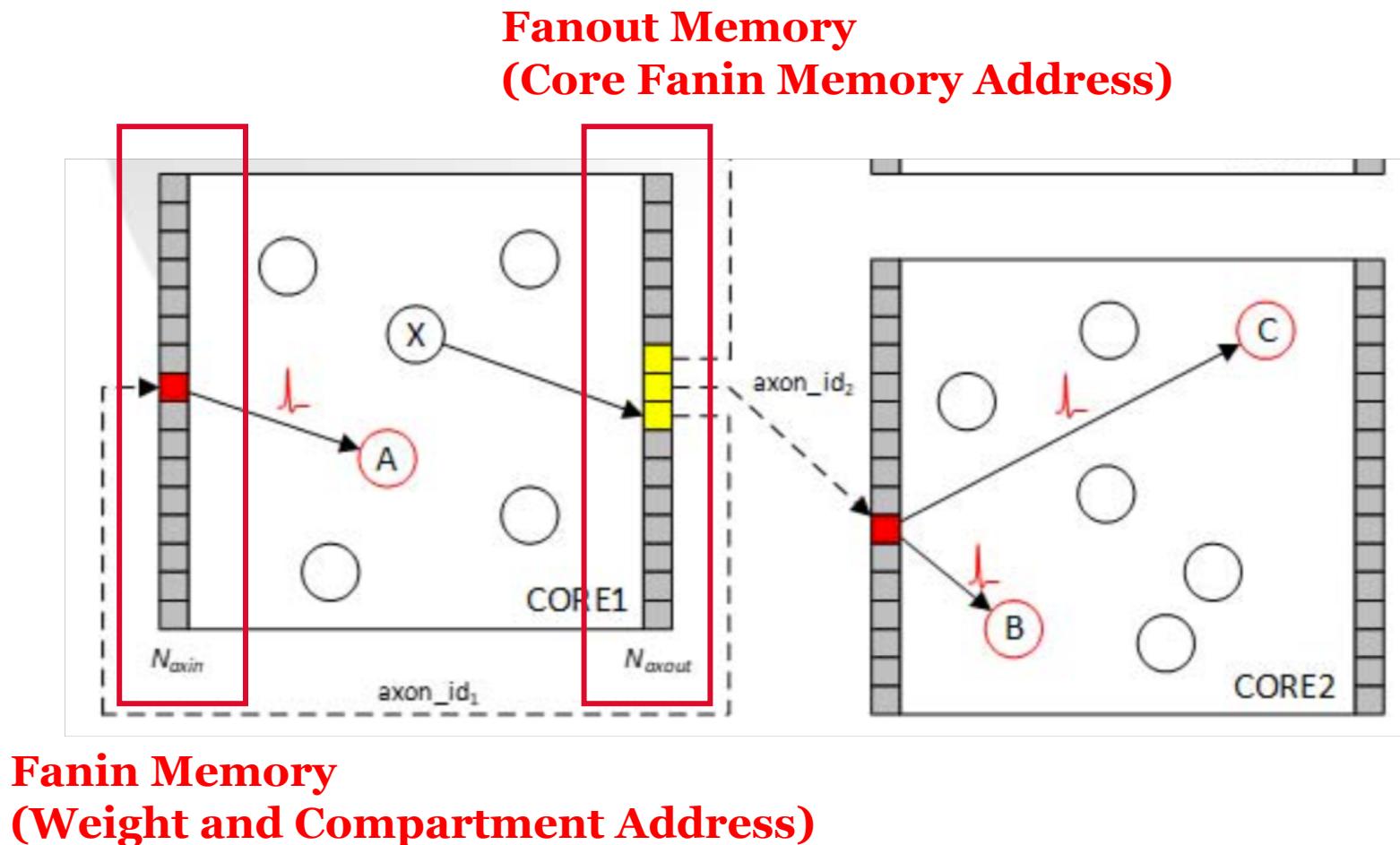
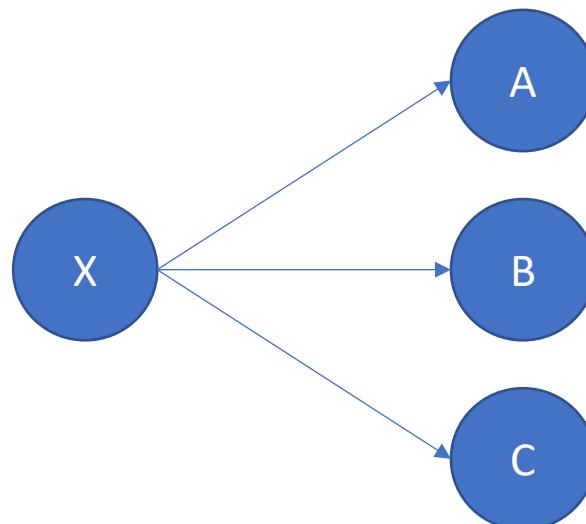


Partial Binary Tree

(Intel INRC Iceland Workshop, 2018)

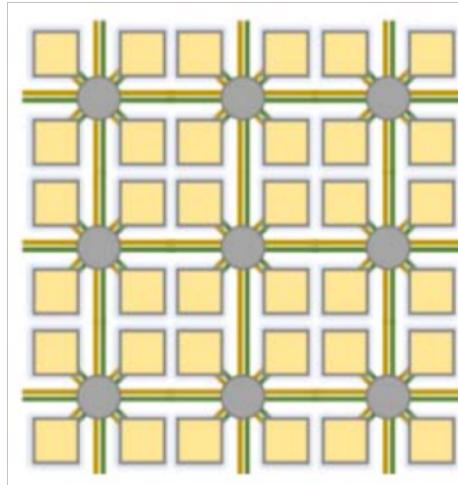


Neuron Level 3: Synapses and Spikes

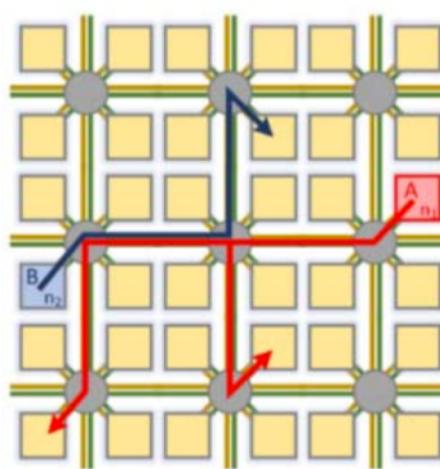




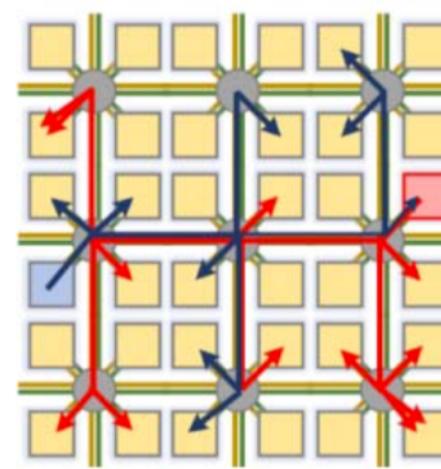
Neuron Level 3: Synapses and Spikes



Timestep T Begins
Update LIF Neurons



Send Spikes to Fanout Cores



Barrier Synchronization
Flush Spikes in Flight

Go to Timestep T+1

Loihi Computation 3: Learning Level

Learning Level 1: Vanilla STDP



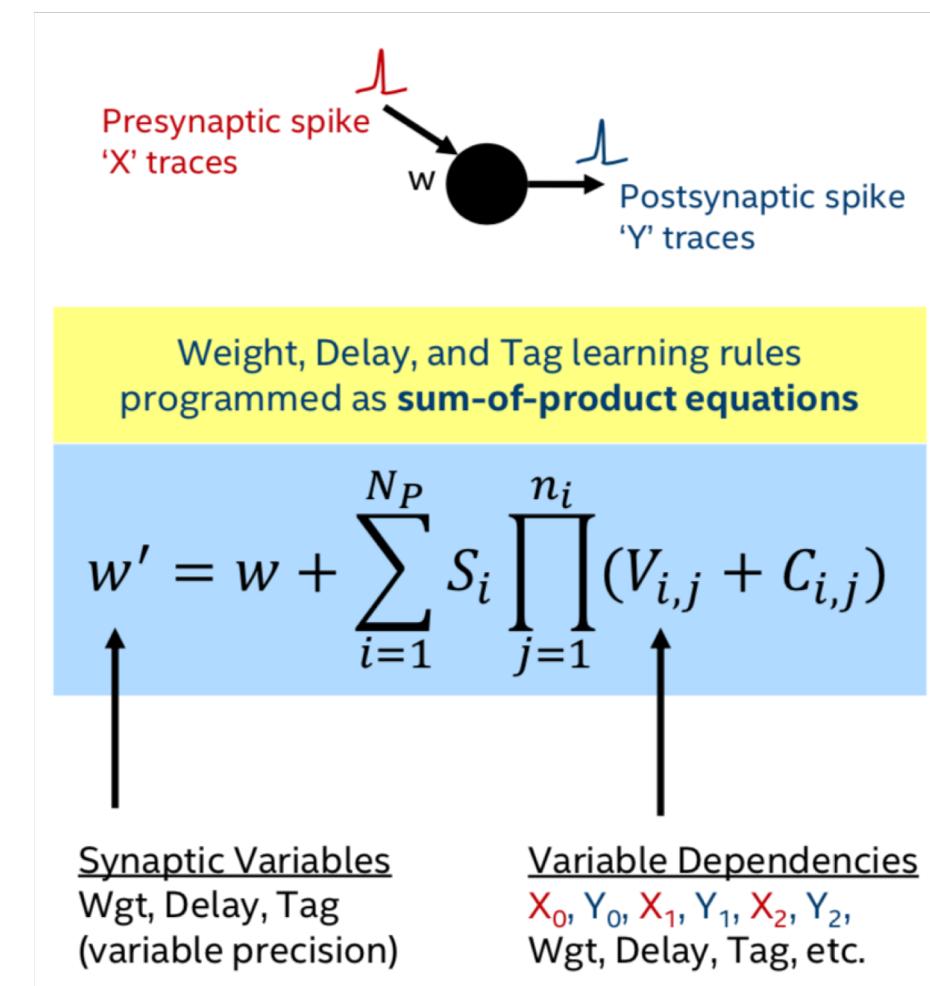
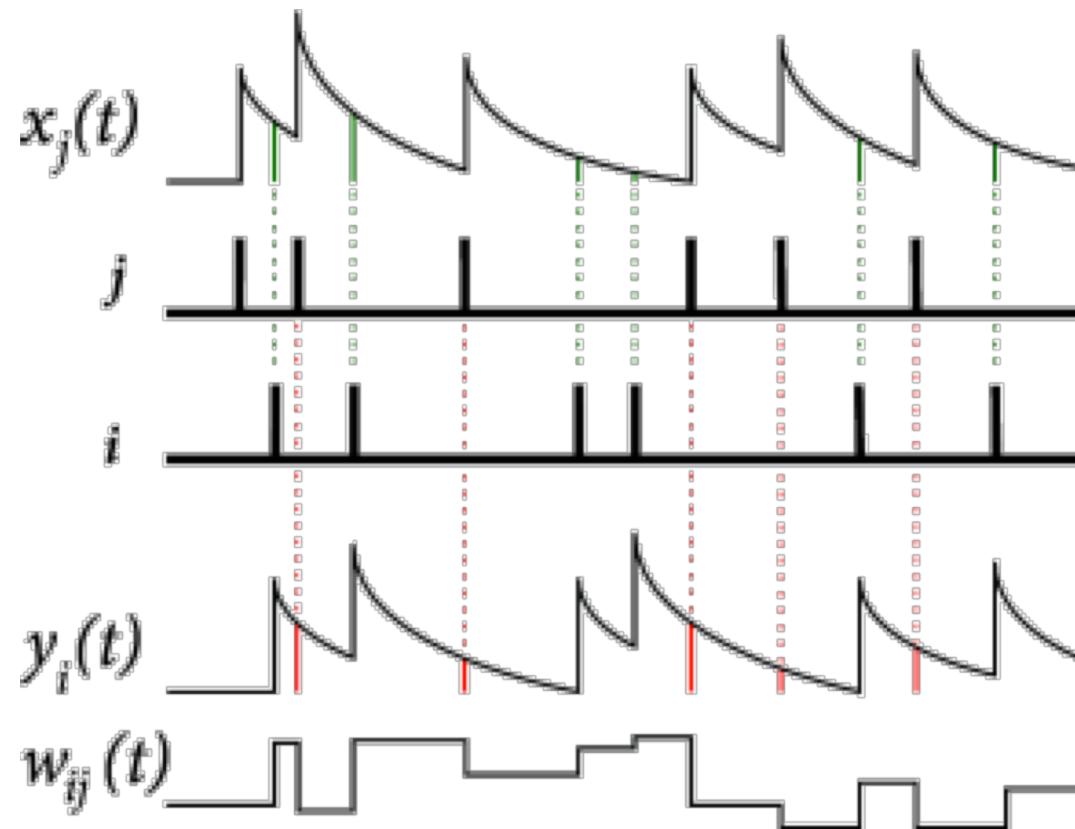
Learning Level 2: Reward-STDP



Learning Level 3: Delay Learning (Not for Today)

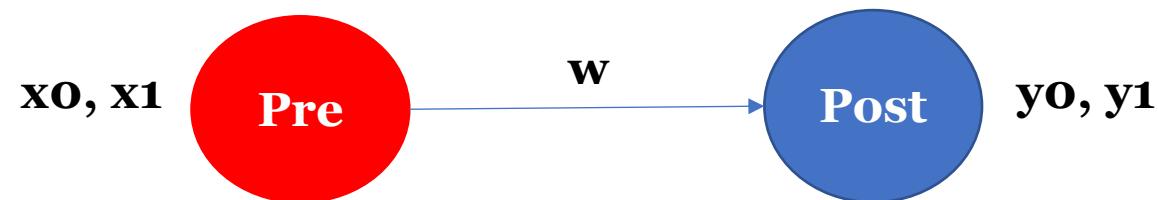


Trace-based Learning and Learning Rules

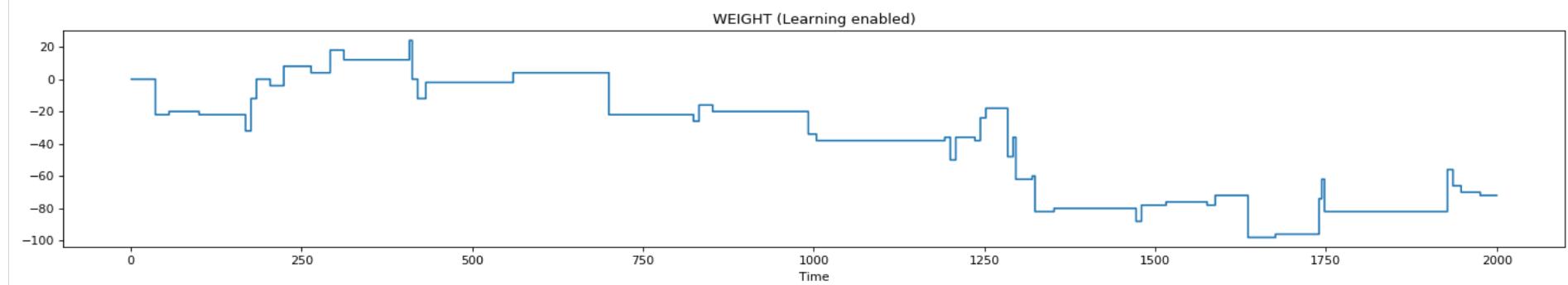
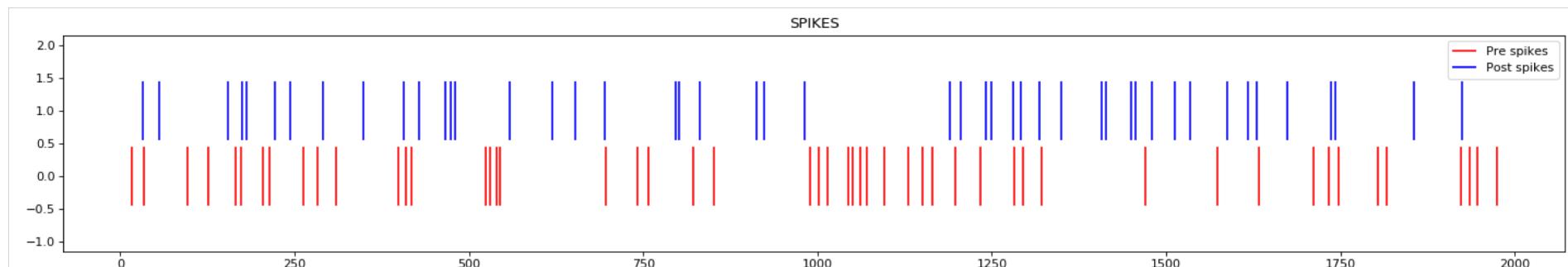
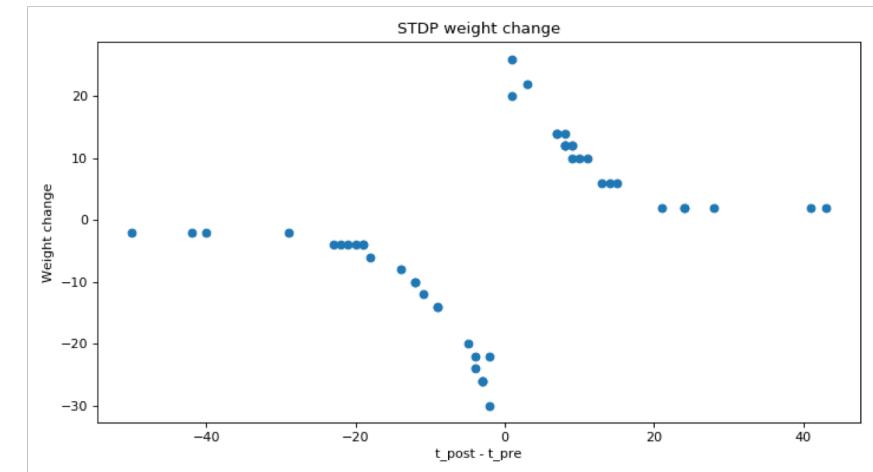




Learning Level 1: Vanilla STDP



$$dw = 2^{-2} * x_1 * y_0 - 2^{-2} * y_1 * x_0$$





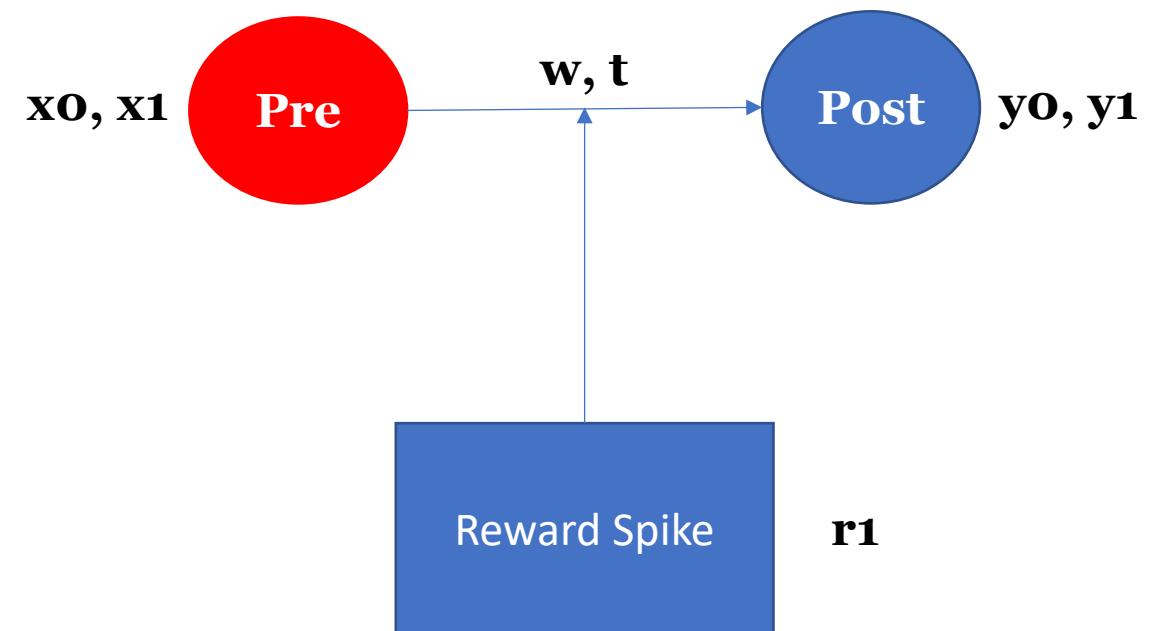
Learning Level 2: Reward-STDP

Tag Update with Decay

$$dt = x_1 * y_0 - y_1 * x_0 - 2^{-2} * t$$

Weight Update with Reward

$$dw = 2 * r_1 * t$$





Learning Level 2: Reward-STDP

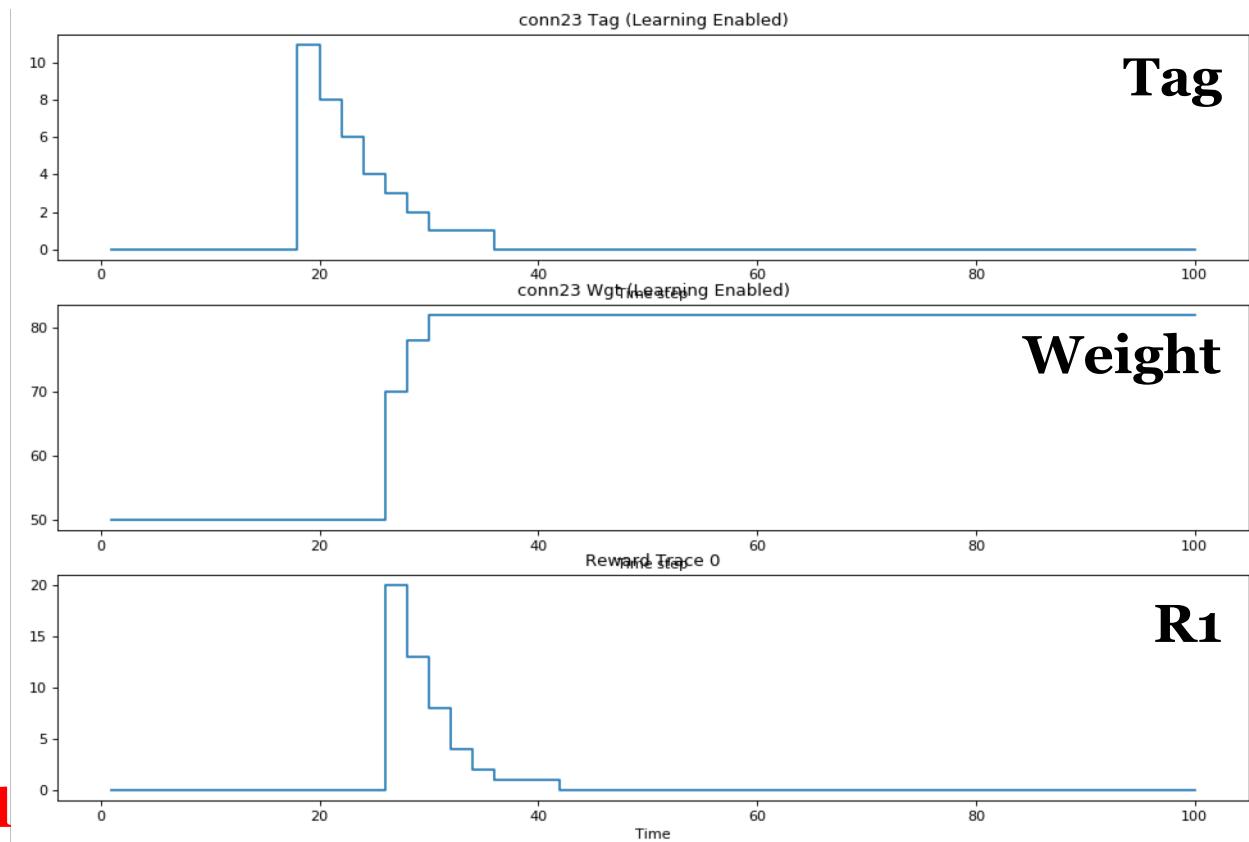
Tag Update with Decay

$$dt = x_1 * y_0 - y_1 * x_0 - 2^{-2} * t$$

Weight Update with Reward

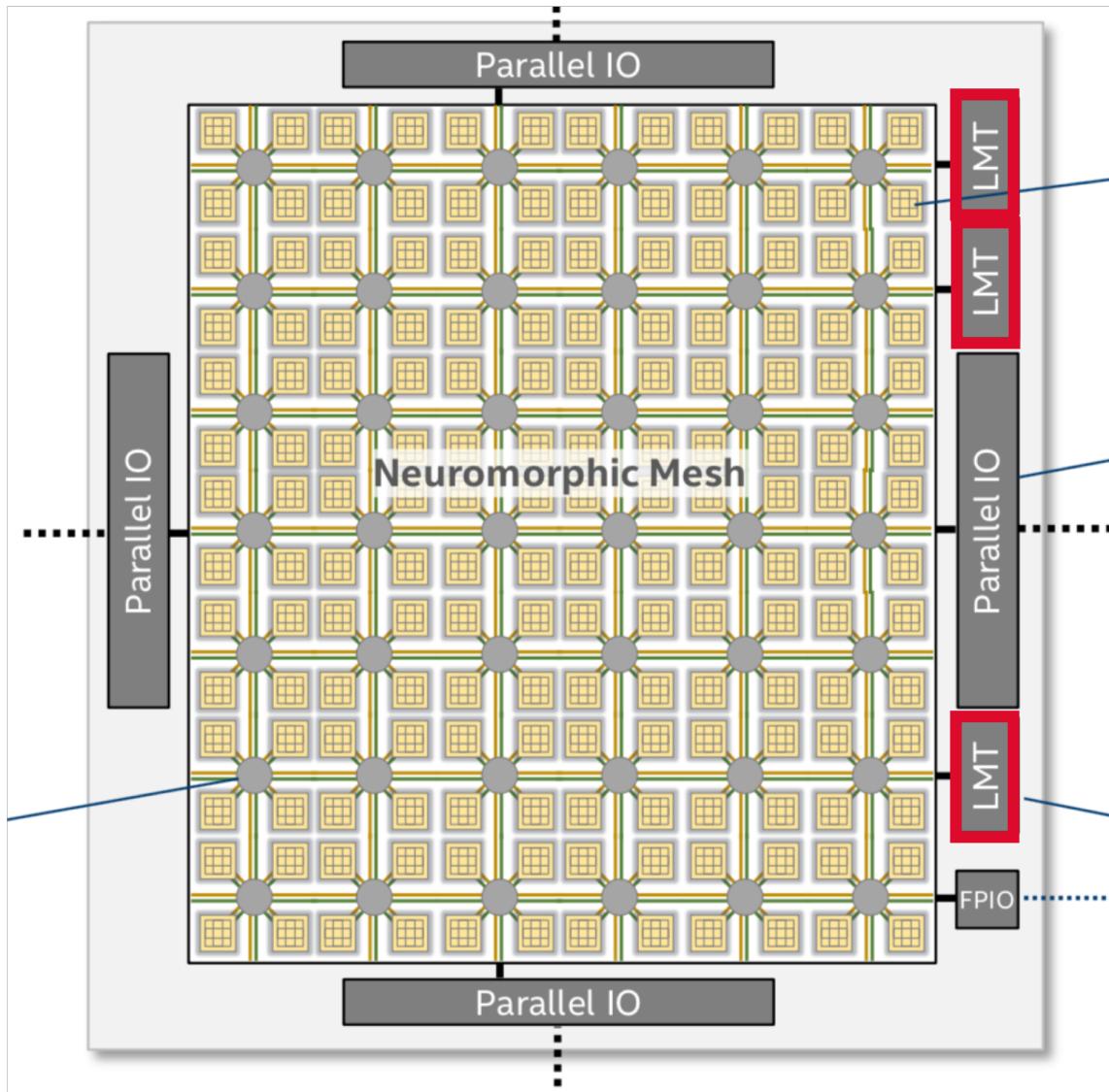
$$dw = 2 * r_1 * t$$

Delay Weight Updating with Reward Signal





Loihi Computation 4: SNIPs Level

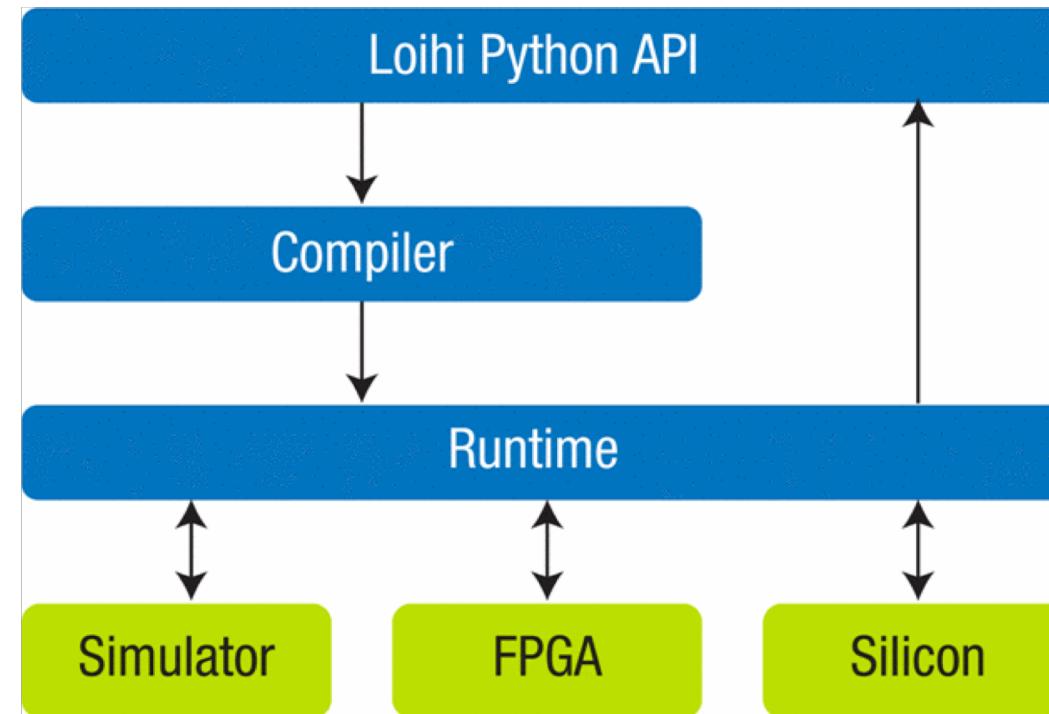


Sequential Neural Interaction Process (SNIP)

- Small C Programs on Embedded x86 CPUs
- Spike-based communication
 - Spike Generator to Compartments
 - Monitoring the Network using Probes
 - Customized Spike Encoder and Decoder
- Network Configuration
 - Change LIF Neuron Parameters
- Synchronous Design

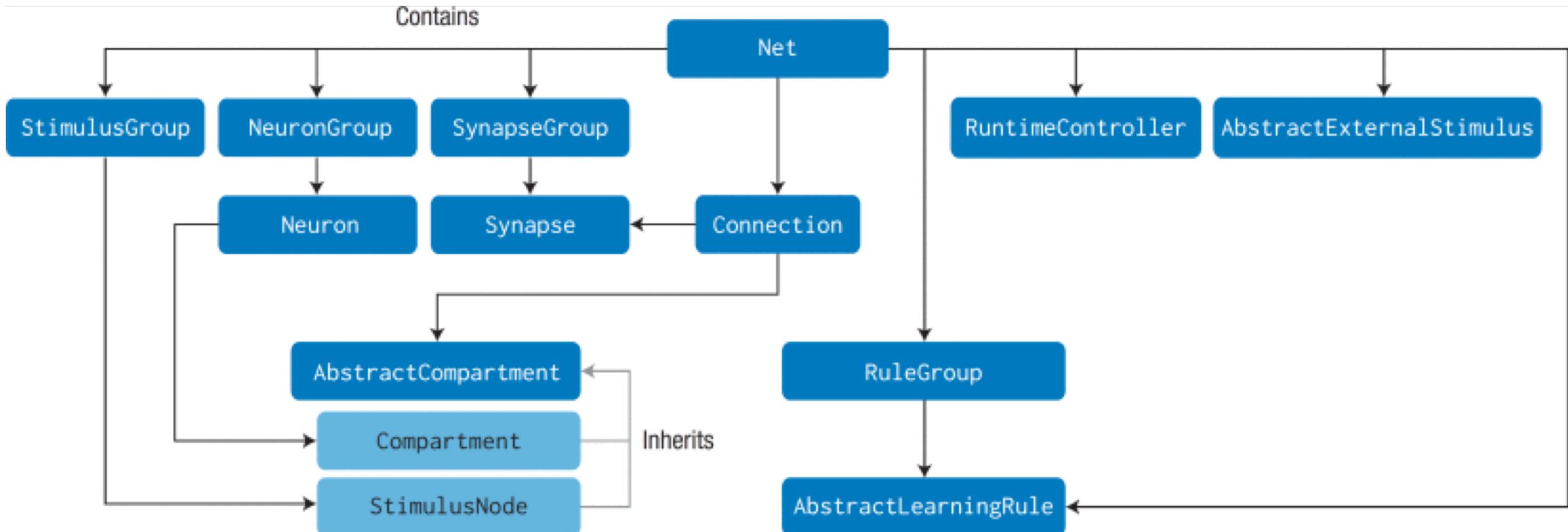


Programming for Loihi using NxSDK



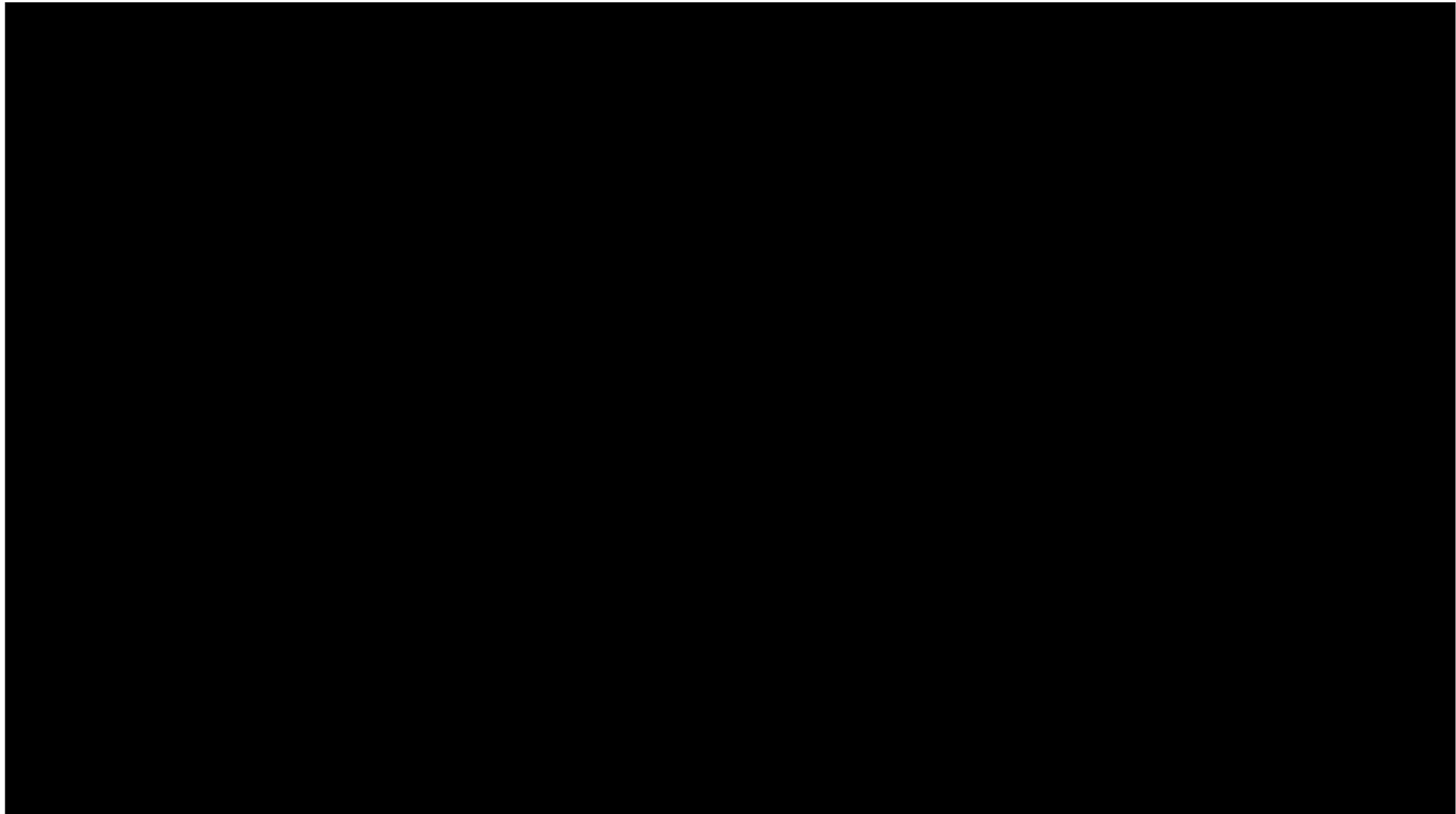


Programming for Loihi using NxSDK



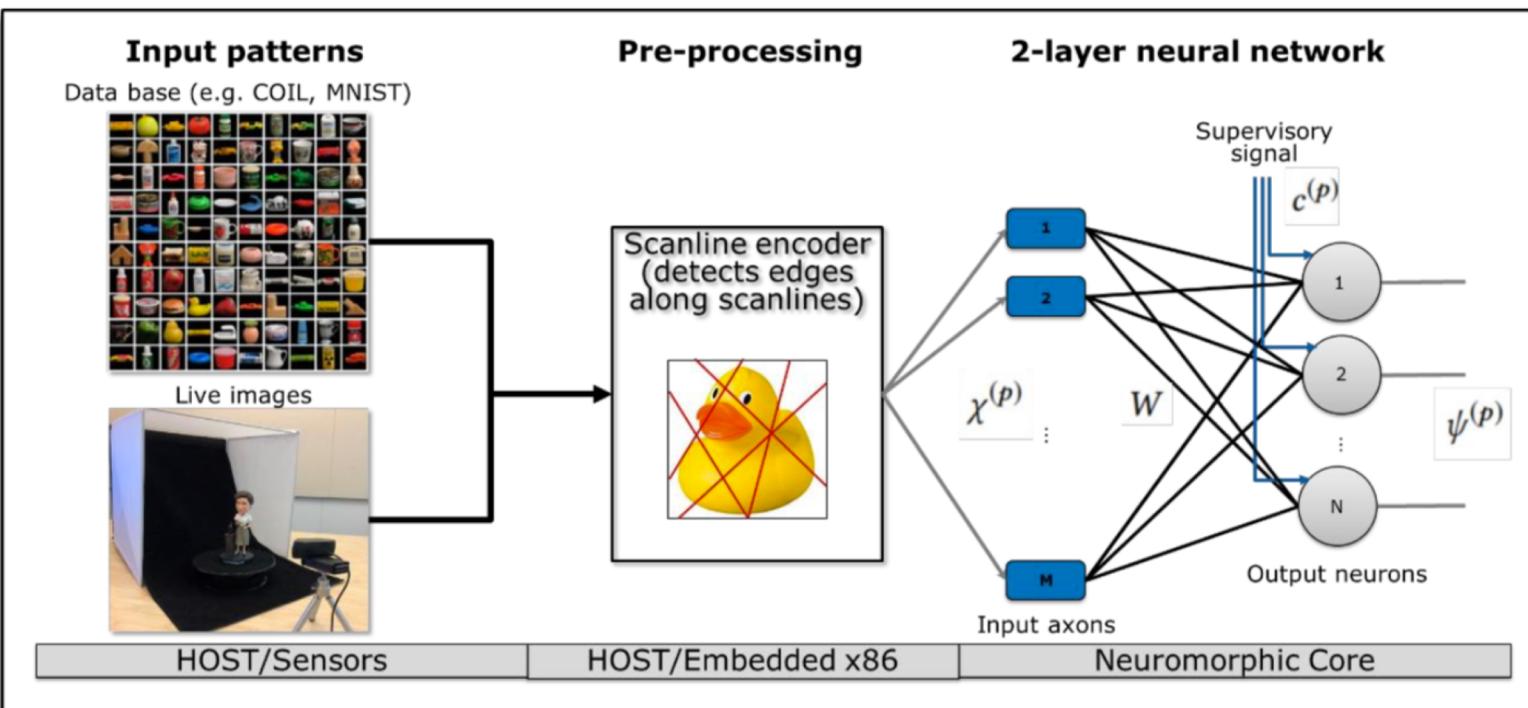


Example: Digit Classification



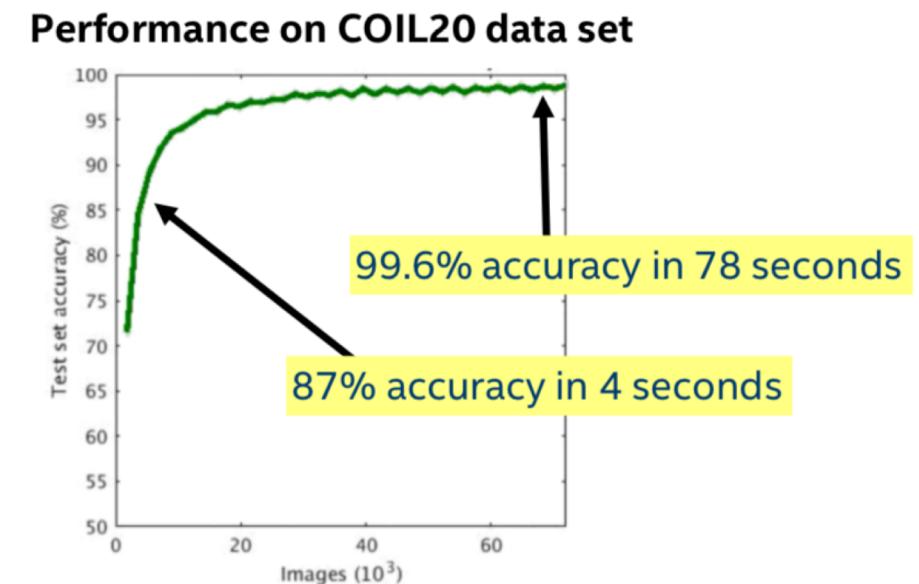


Example: Digit Classification



Resource Utilization	Count	Utilization
Neurons	20	0.02%
Synapses	38400	0.28%
SNN Cores	1	0.78%

Uses less than 1% of chip resources



	Training	Inference
Active energy per image (total)	553 uJ	128 uJ
Neuromorphic energy	322 uJ	13 uJ
Processing time per image	7.5 ms	1.8 ms
Chip power	74 mW	73 mW
Neuromorphic power	43 mW	7.4 mW