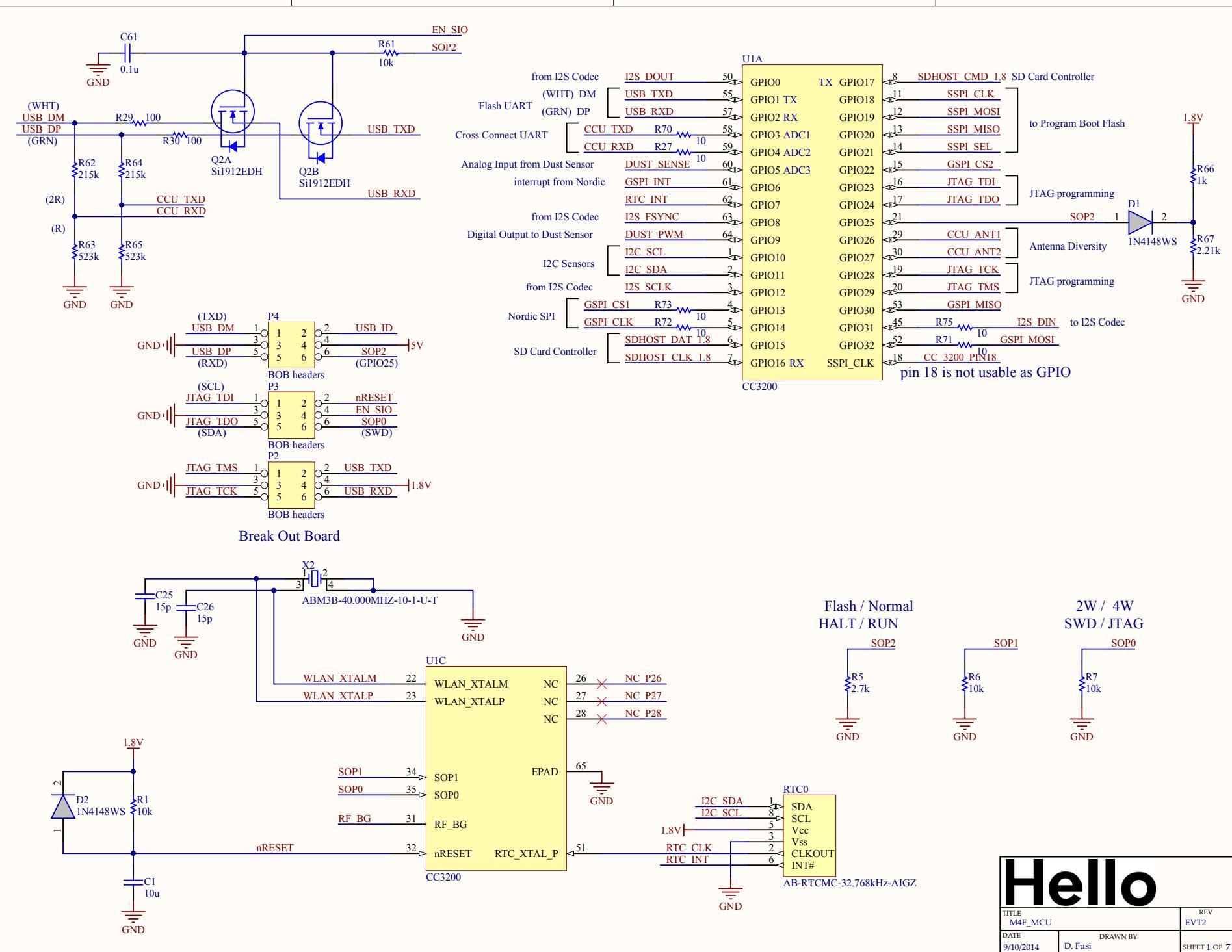
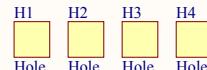
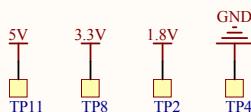


1 2 3 4

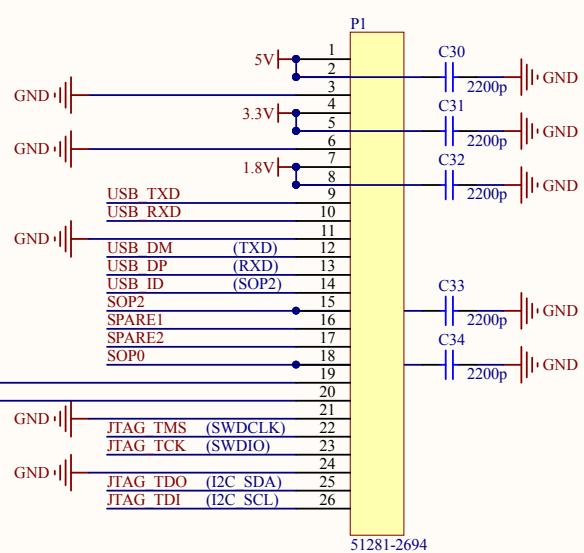




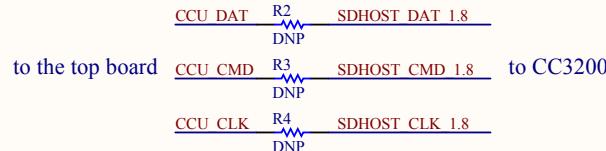
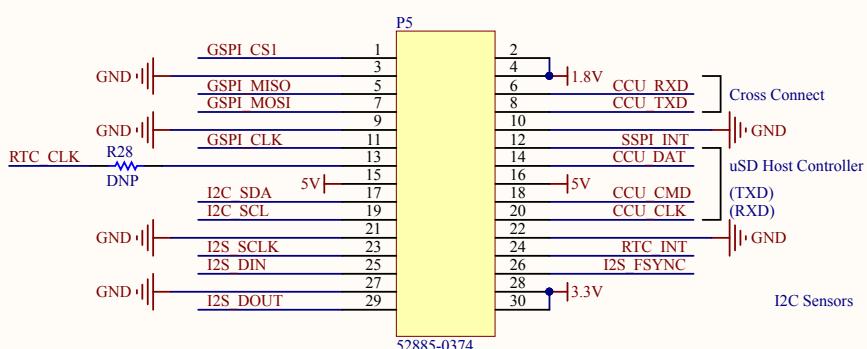
mounting holes



to the bottom board



to the top board

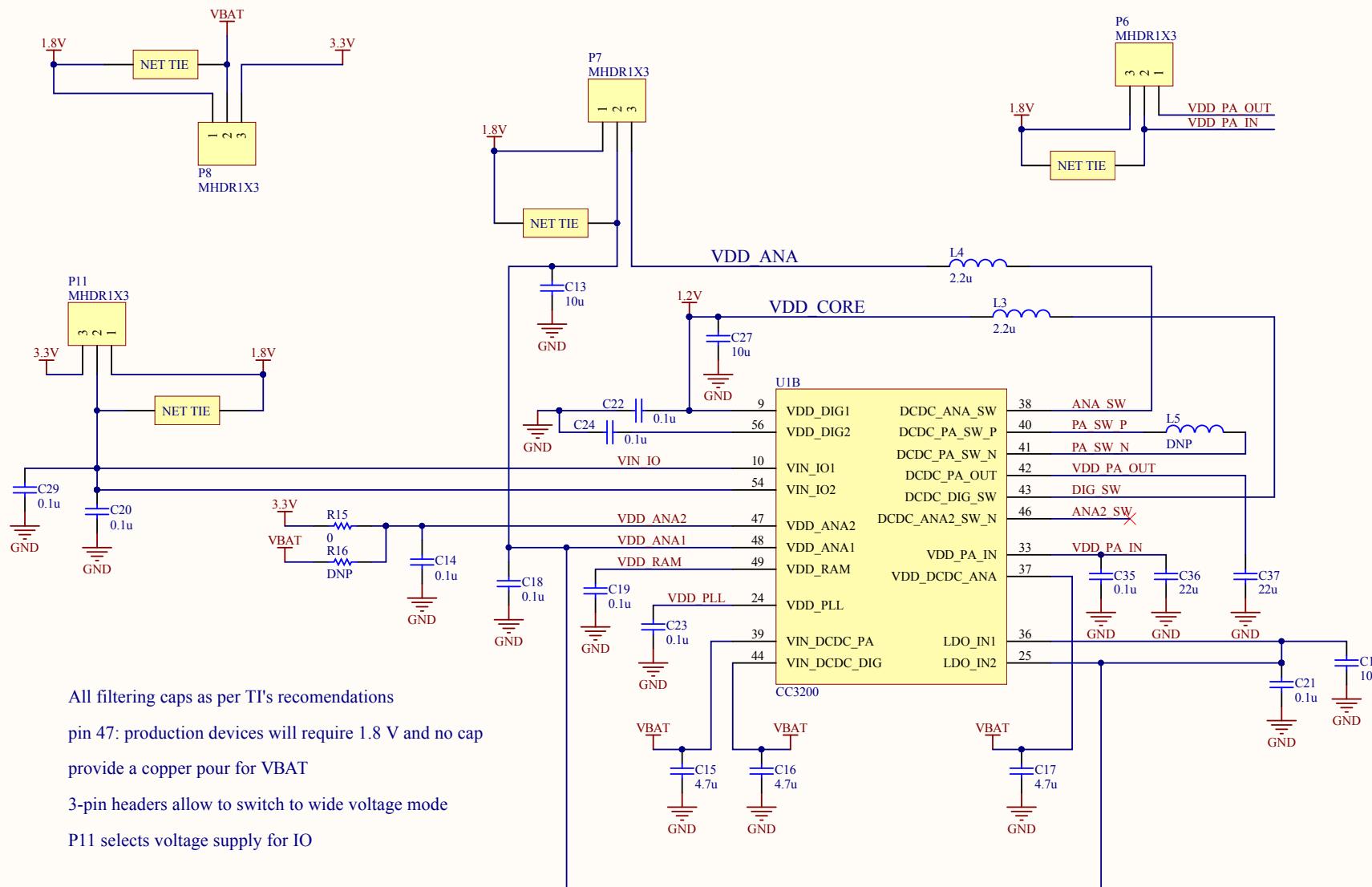


# Hello

TITLE	REV
Morpheus_middle	EVT2
DATE	Drawn By
9/5/2014	D. Fusi

SHEET 2 OF 7

## Pre Reg      Wide Volt



All filtering caps as per TI's recommendations

pin 47: production devices will require 1.8 V and no cap

provide a copper pour for VBAT

3-pin headers allow to switch to wide voltage mode

P11 selects voltage supply for IO

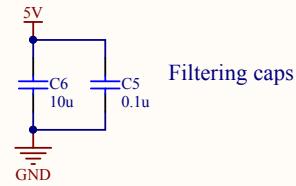
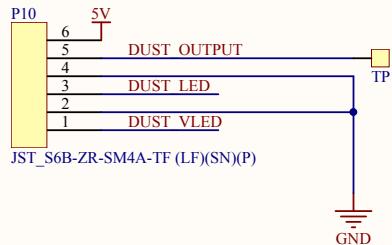
# Hello

TITLE	M4F MCU Power	REV	EVT2
DATE	9/3/2014	DRAWN BY	D. Fusi
SHEET 3 OF 7			

A

A

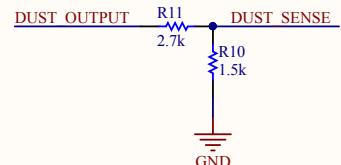
Connector for Sharp dust sensor GP2Y1010AU0F



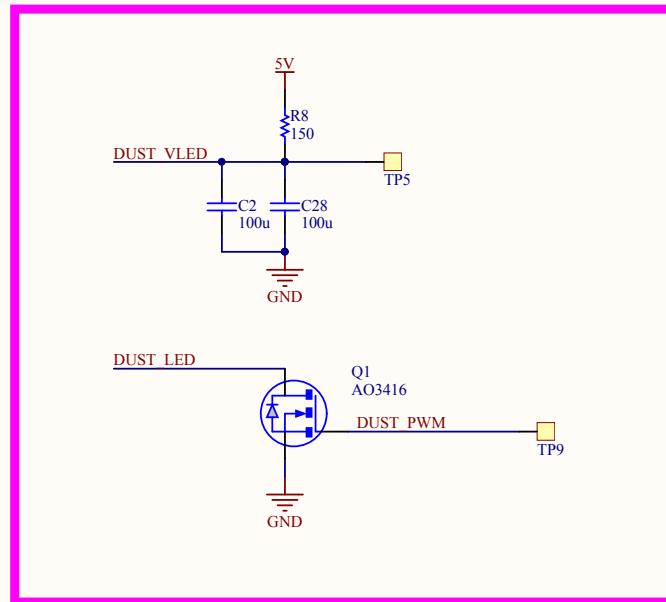
B

B

former level shifter from 4V to 1.8V



As on the GP2Y1010 datasheet



C

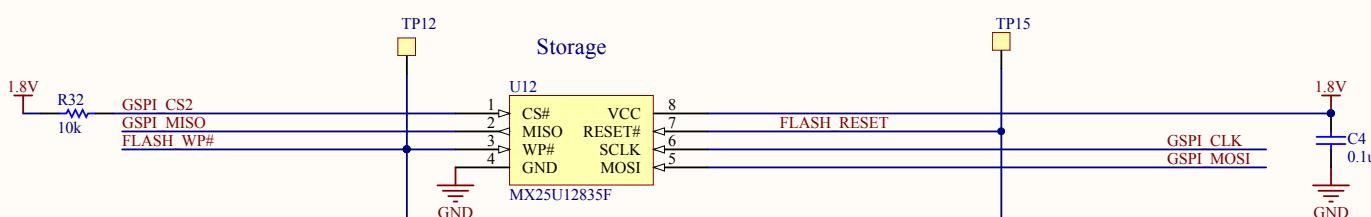
C

# Hello

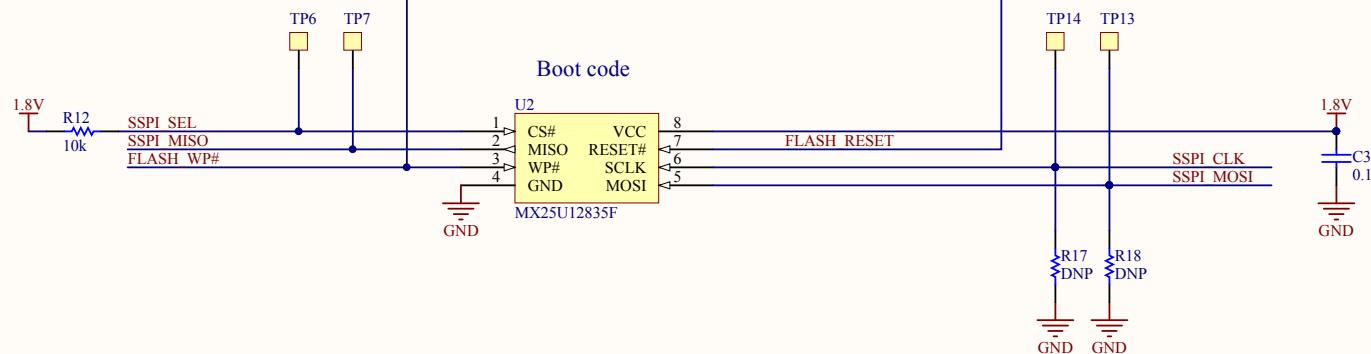
TITLE	REV
Air_quality	EVT2
DATE	DRAWN BY
9/3/2014	D. Fusi

D

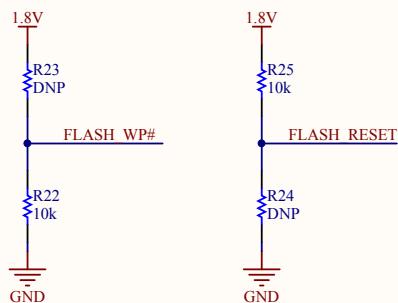
A



B



C



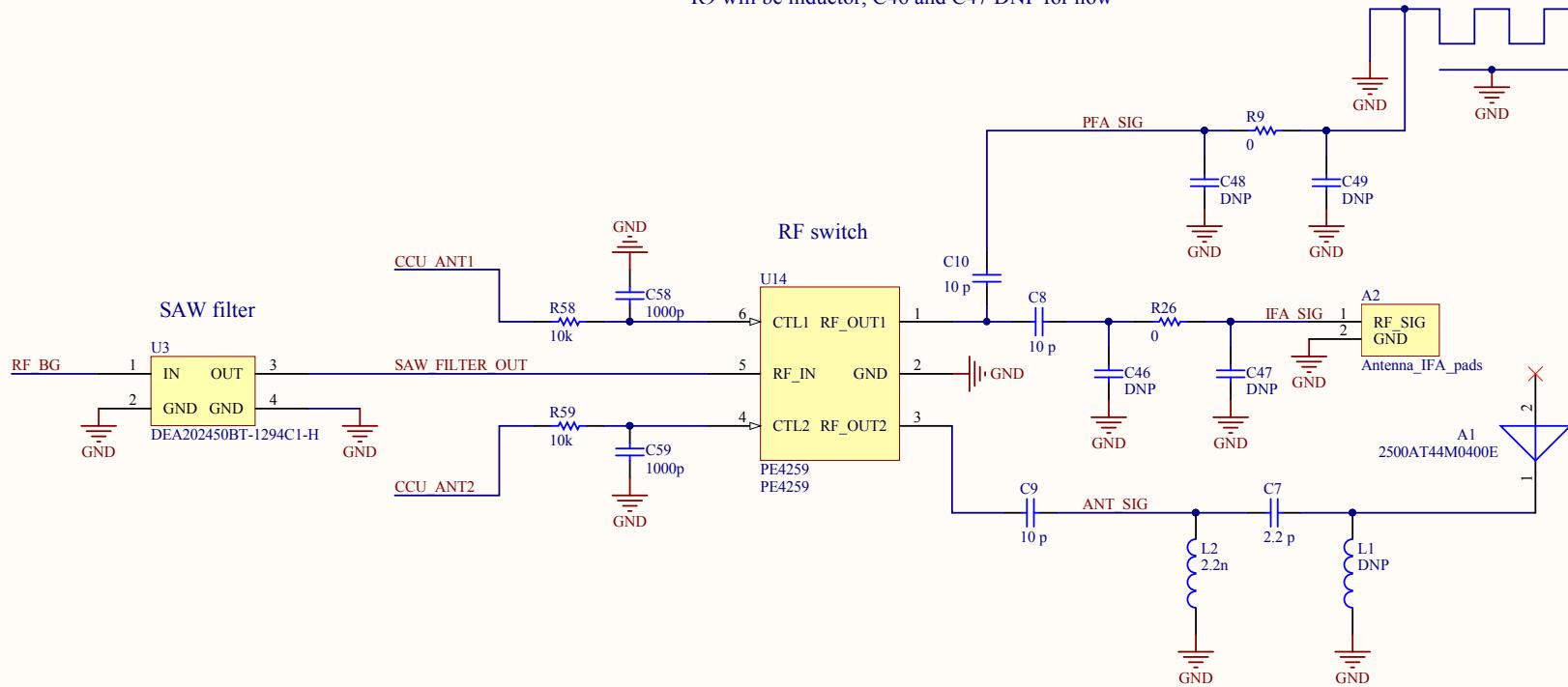
Datasheet is unclear, so for now we pull reset high and WP low



A

A

R9 will be inductor, C46 and C47 DNP for now

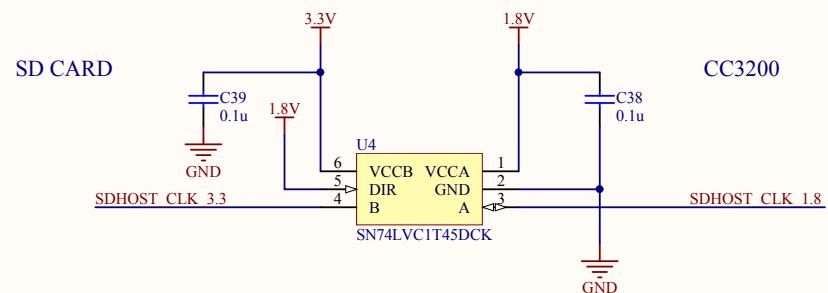


# Hello

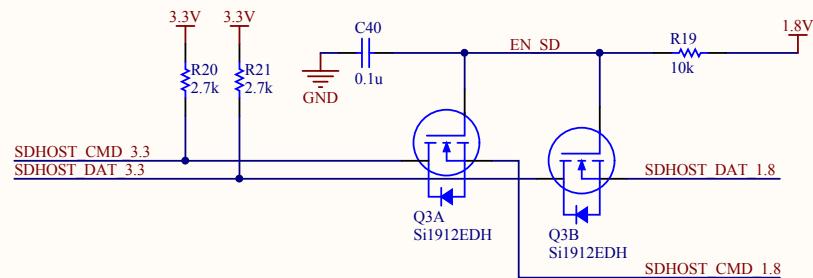
TITLE	REV
M4F MCU_Antennas	EVT2
DATE	DRAWN BY
9/3/2014	D. Fusi

A

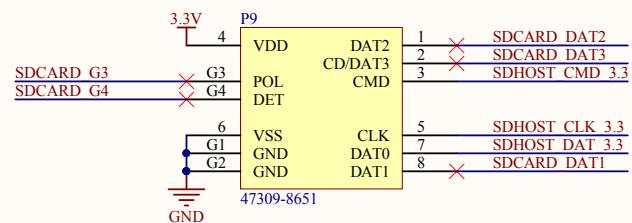
CLK needs a dedicated level shifter because of speed



B



C



SD Card connector

# Hello

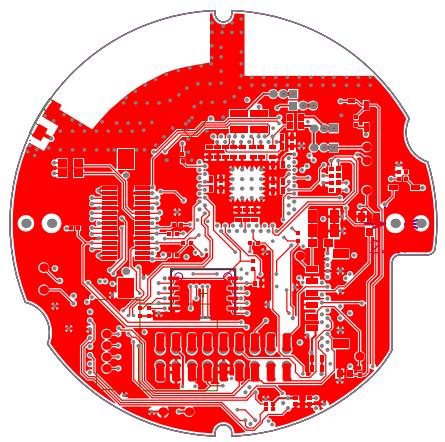
TITLE	REV
SD_Card	EVT2
DATE	DRAWN BY
9/4/2014	D. Fusi

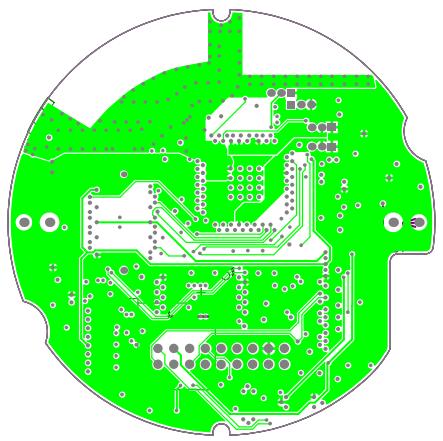
A

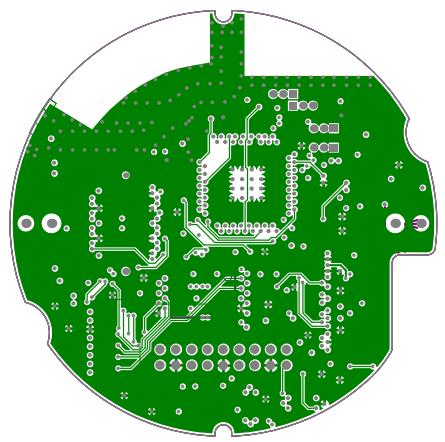
B

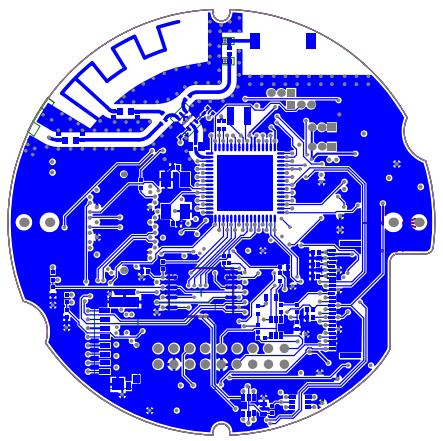
C

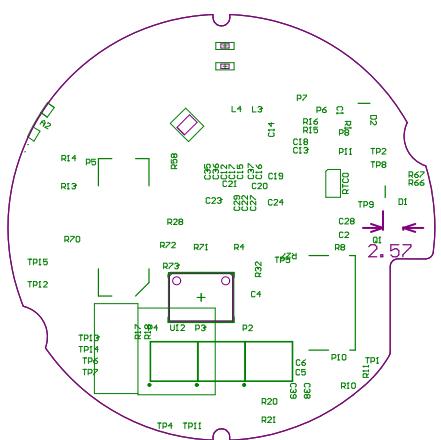
D

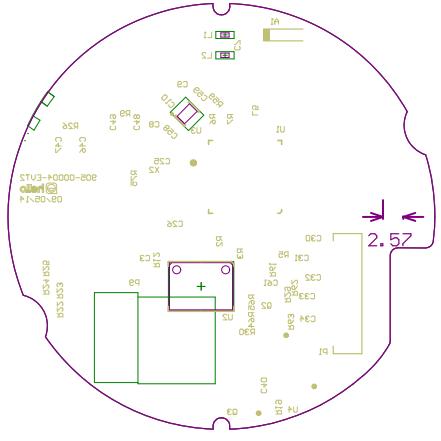


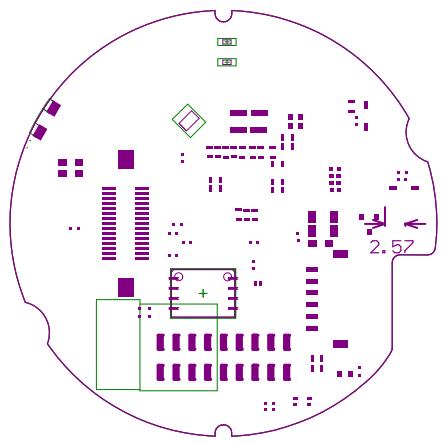


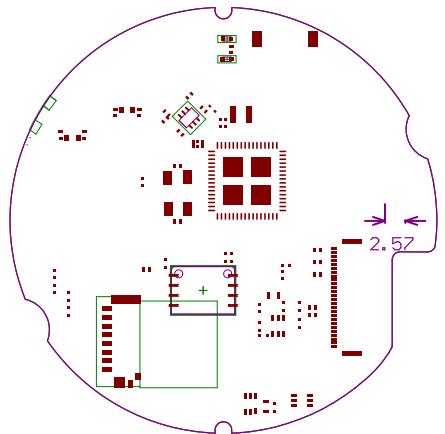


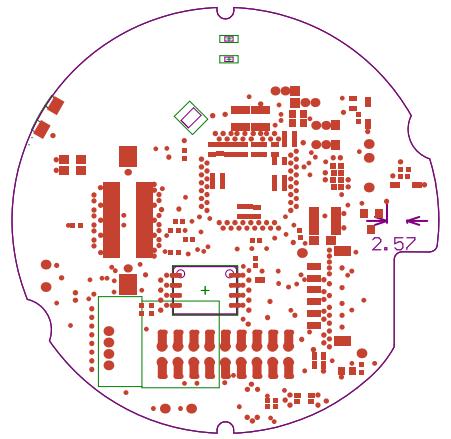


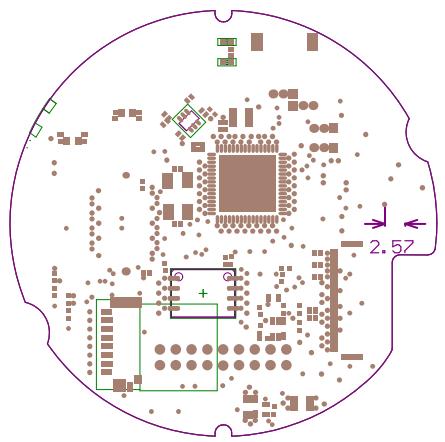


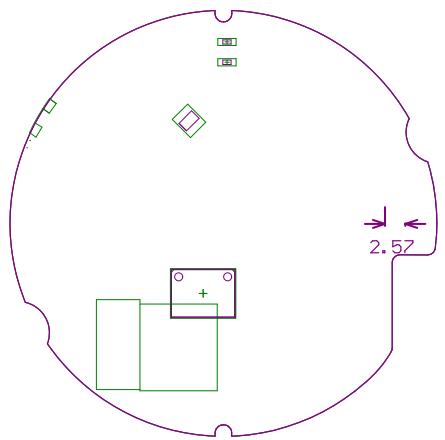


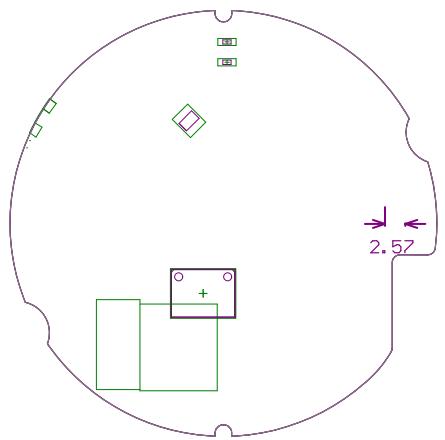


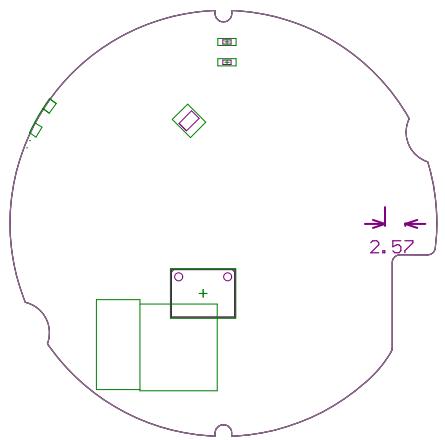


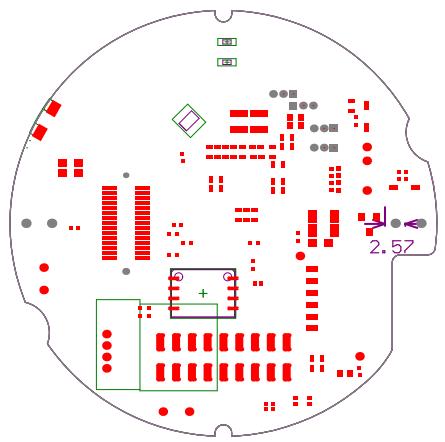


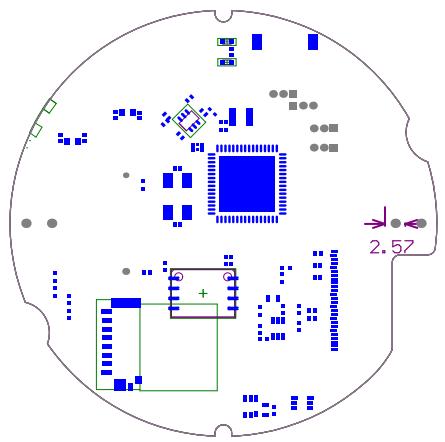




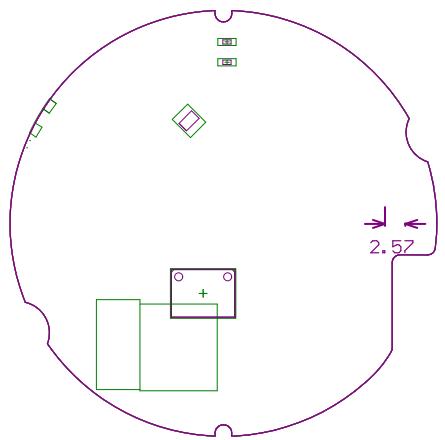








2.57



### Fabrication / Assembly Notes

1. Material: Rigid FR-4, RoHS compliant: material should meet or exceed requirements of IPC 4101/129
2. Number of electrical layers: 4
3. Trace / Space minimum: 5mil (all layers)
4. Thickness: 0.76mm (finished)
5. Finish: ENIG plating on exposed copper
6. Soldermask: per IPC-SM-840, color blue registration within +/- 50um of circuit layer
7. Silkscreen: do print silkscreen on top and bottom layers
8. Antenna trace from U1 pin 31 on bottom layer should be 50 ohm, (0.45mm) width.
9. Board must be lead free process compatible and able to withstand minimum of 5 cycles at 250 degrees celsius
10. All Test/QA/QC markings to be made on back side of PCB
11. x mousebites shall be no larger than 0.05 mm

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Paste				
2	Top Overlay				
3	Top Solder	Solder Resist	0.010mm	3.5	
4	Top Layer	Copper	0.036mm		
5	Dielectric1	FR-4	0.254mm	4.2	
6	GND	Copper	0.017mm		
7	Dielectric2		0.127mm	4.2	
8	PWR	Copper	0.017mm		
9	Dielectric3		0.254mm	4.2	
10	Bottom Layer	Copper	0.036mm		
11	Bottom Solder	Solder Resist	0.010mm	3.5	
12	Bottom Overlay				
13	Bottom Paste				

Symbol	Hit Count	Finished Hole Size	Plated	Hole Type
◊	1	0.900mm (35.43mil)	PTH	Round
■	2	1.800mm (70.87mil)	PTH	Round
○	2	2.200mm (86.61mil)	PTH	Round
*	3	0.600mm (23.62mil)	PTH	Round
×	10	0.700mm (27.56mil)	PTH	Round
○	18	0.813mm (32.00mil)	PTH	Round
▽	206	0.305mm (12.00mil)	PTH	Round
□	216	0.200mm (7.87mil)	PTH	Round
	458 Total			

