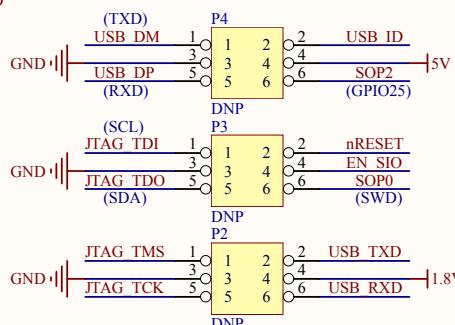
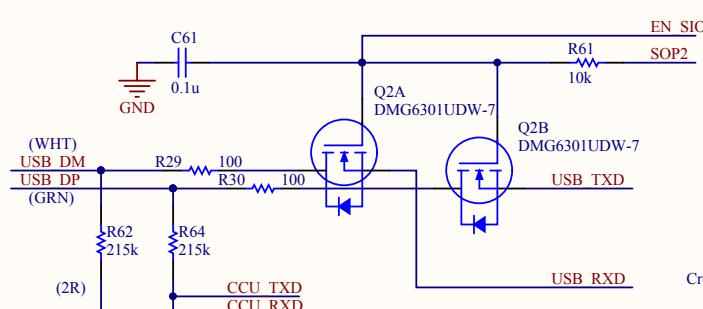
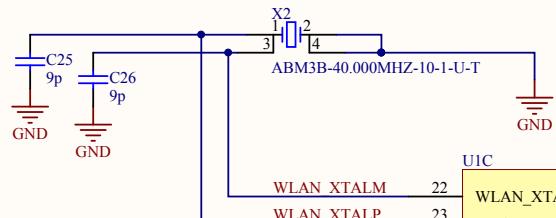
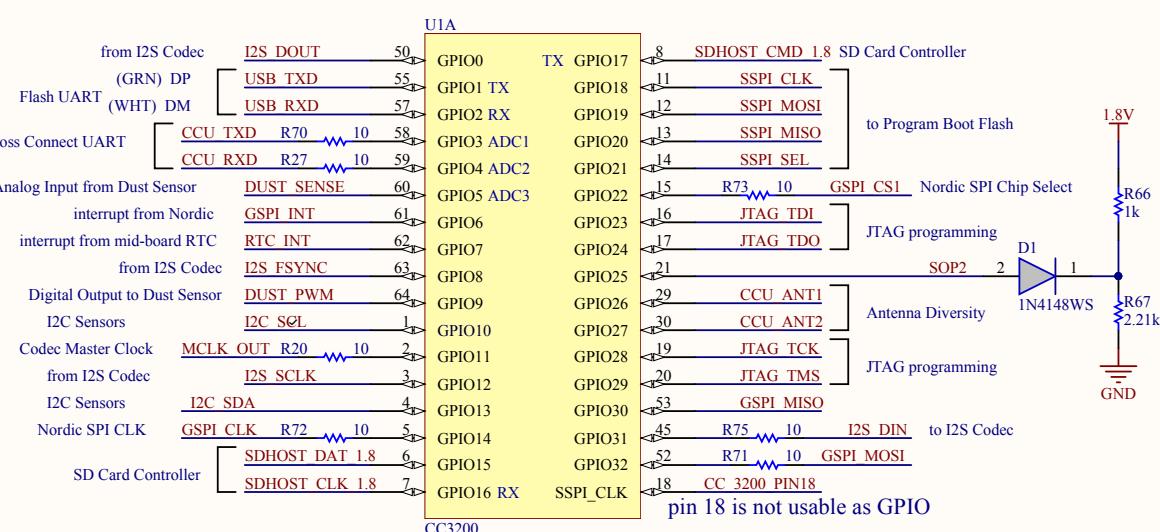
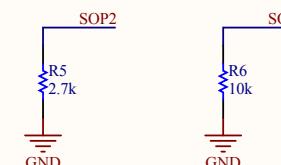
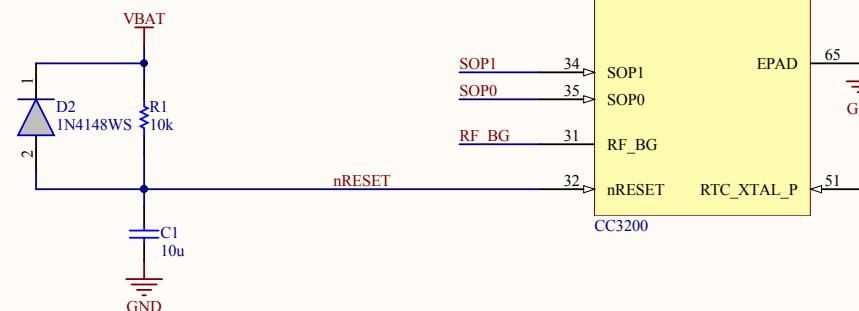
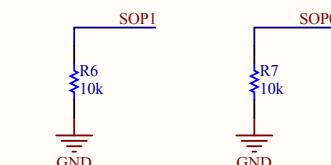


1 2 3 4



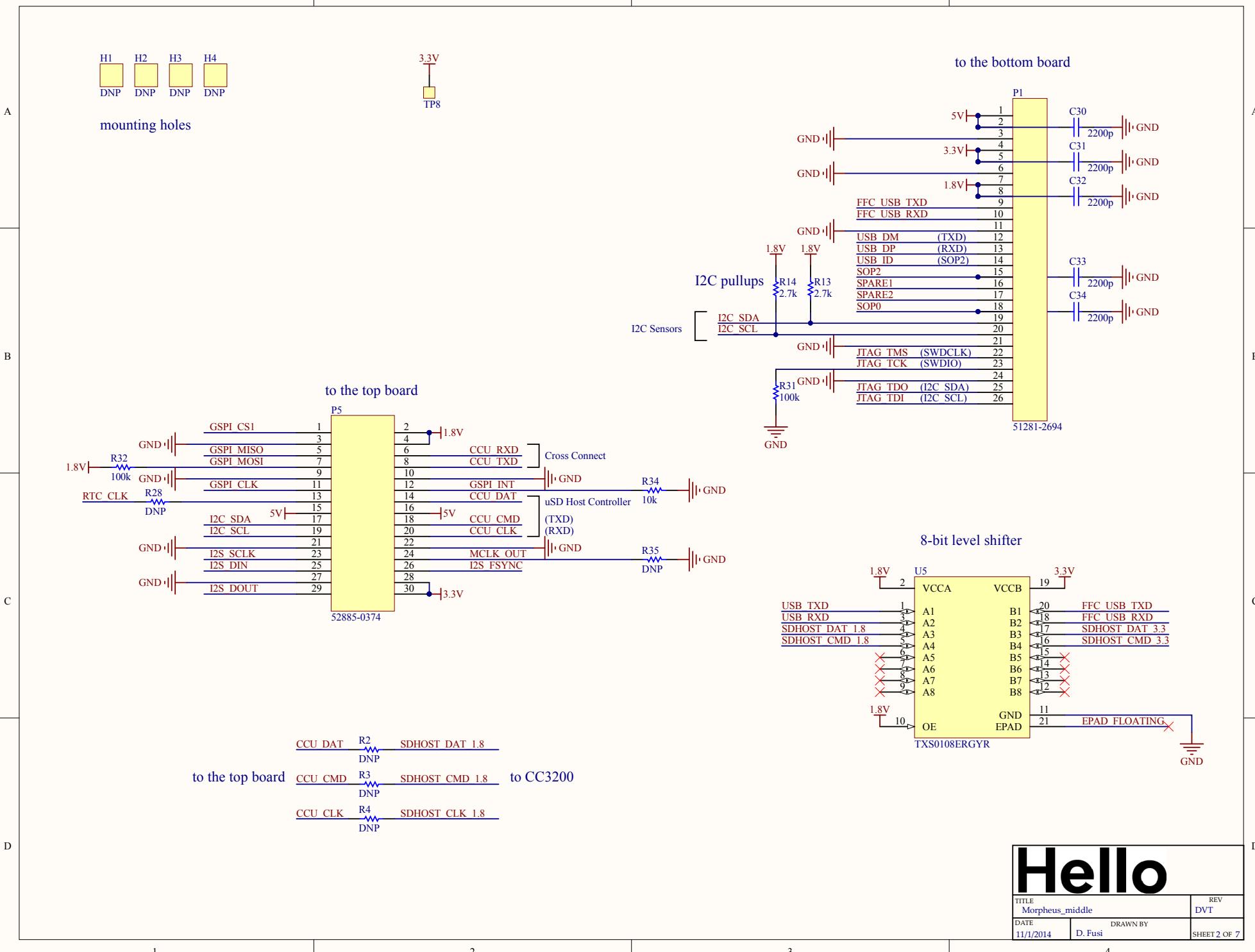
Break Out Board

Flash / Normal
HALT / RUN2W / 4W
SWD / JTAG**Hello**

TITLE	REV
M4F MCU	DVT
DATE 11/1/2014	D. Fusi DRAWN BY

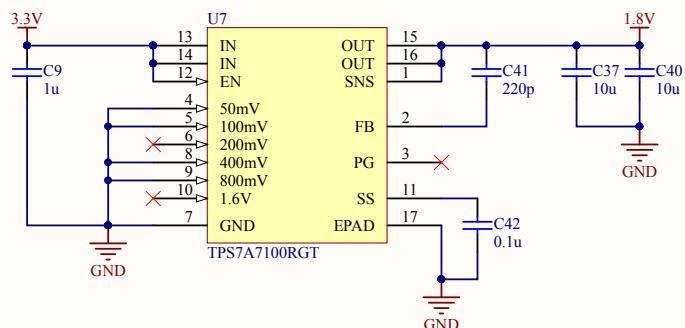
SHEET 1 OF 7

1 2 3 4



Hello

TITLE Morpheus_middle	REV DVT
DATE 11/1/2014	D. Fusi
DRAWN BY	
SHEET 2 OF 7	

LDO for 1.85V**Power scheme only for reference**

A

A

B

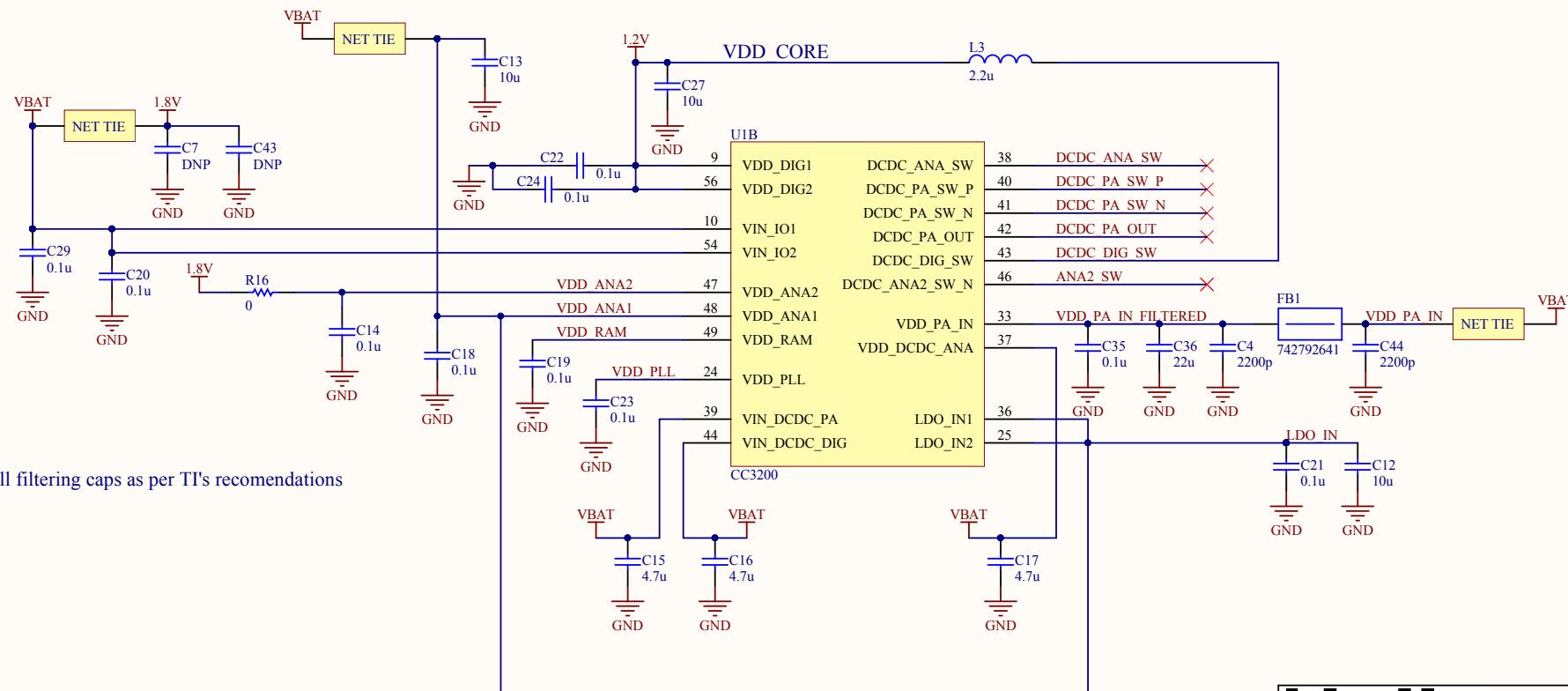
B

C

C

D

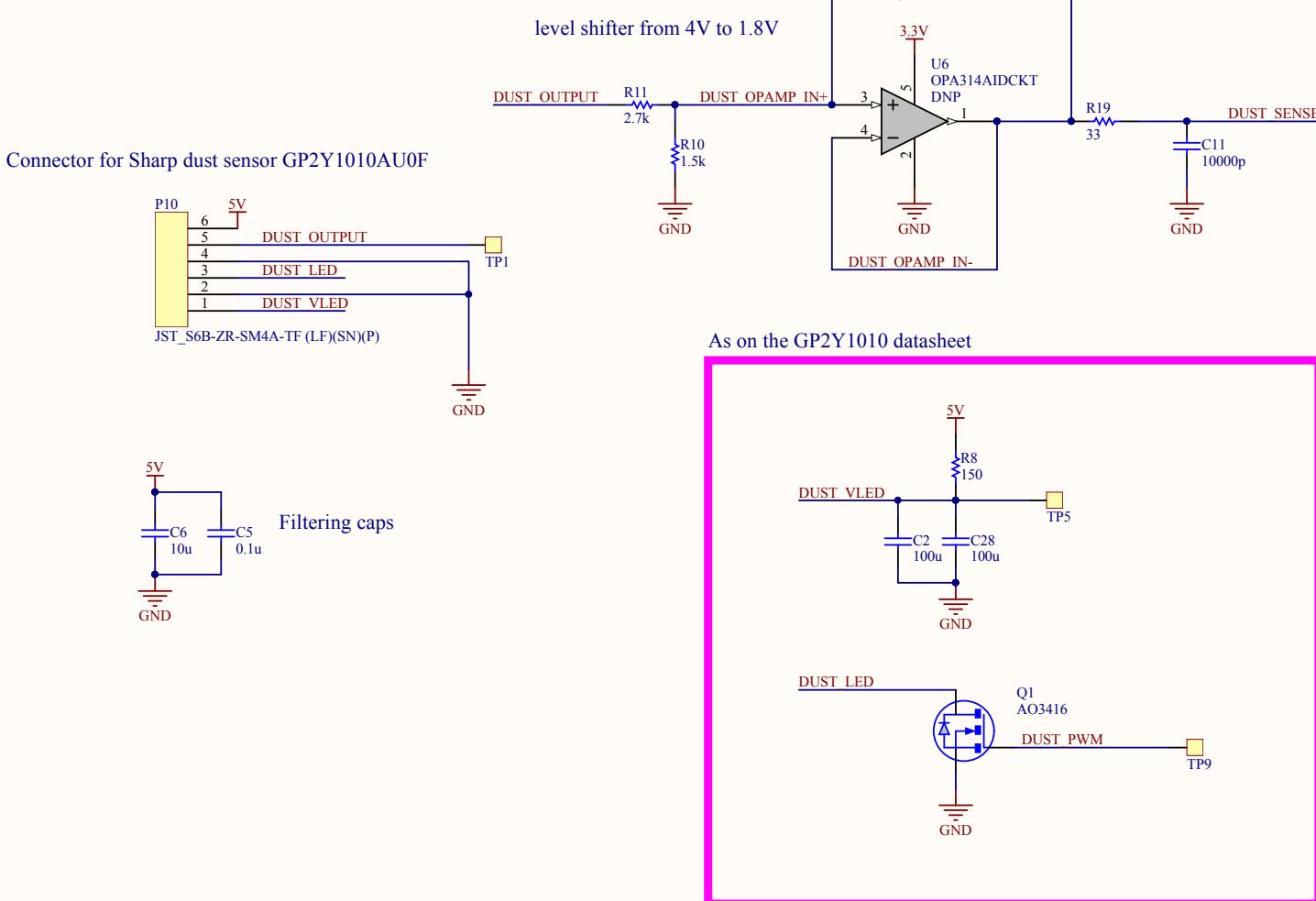
D



Route ground traces for C15, C16 and C17 to single vias on the EPAD. Isolate them from pours in inner layers

Hello

TITLE	REV
M4F MCU_Power	DVT
10/30/2014	D. Fusi



Hello

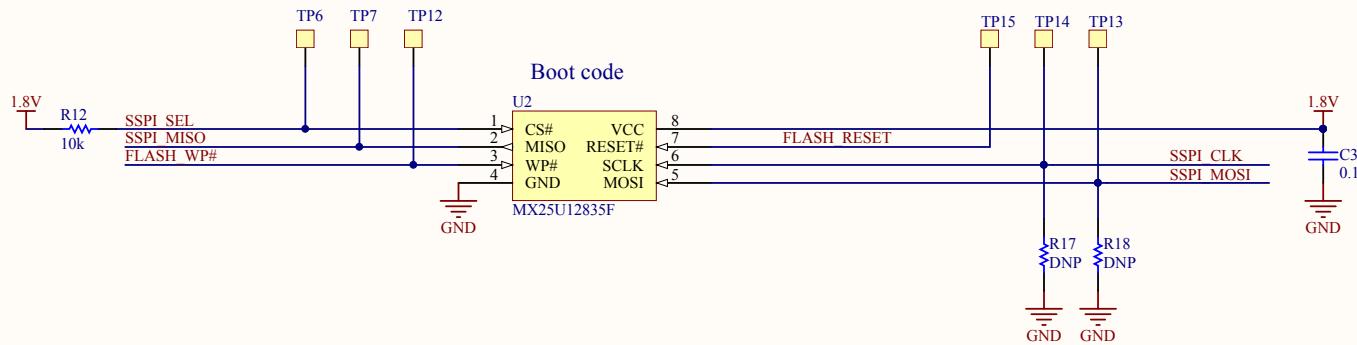
TITLE	REV
Air_quality	DVT
DATE	DRAWN BY
11/1/2014	D. Fusi

A

A

B

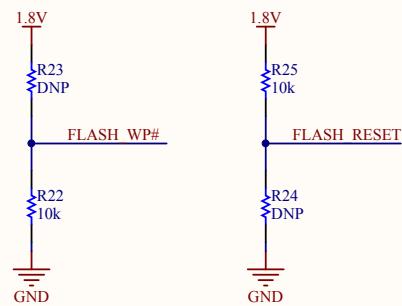
B



TI wants 17 and R18 to be installed but we've always been good without

C

C



D

D

Datasheet is unclear, so for now we pull reset high and WP low



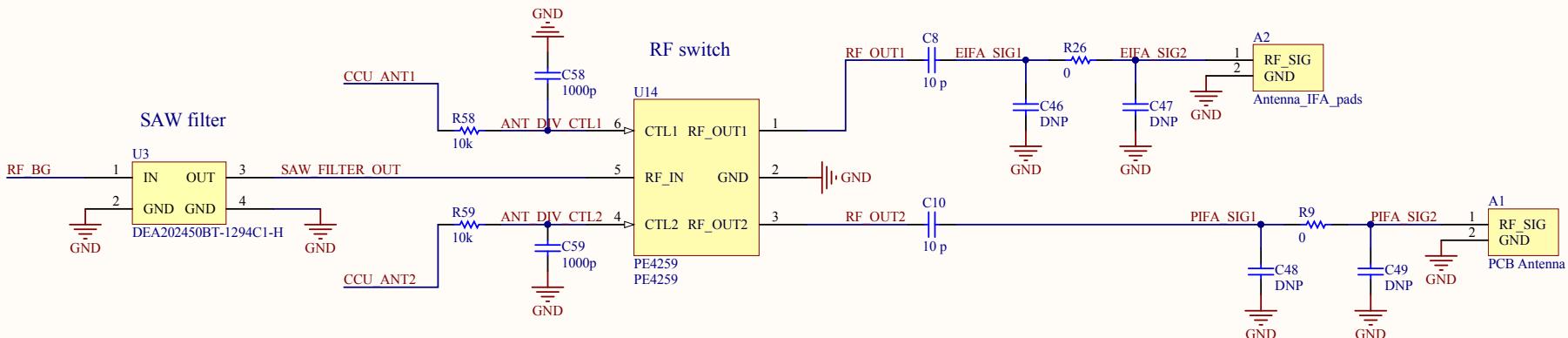
A

A

R9 and R26 will be inductors if needed. C46 and C47 DNP for now

B

B



C

C

RF components: Johanson 0201 L-05B0N6CV6S 250R05L0R2AV4S
 Murata 0201 GJM0335C1ER20WB01
 Murata 0402 GJM1555C1H100GB01D
 Murata 0402 LQP15MN1N0B02

GJM series is better than GRM for RF

D

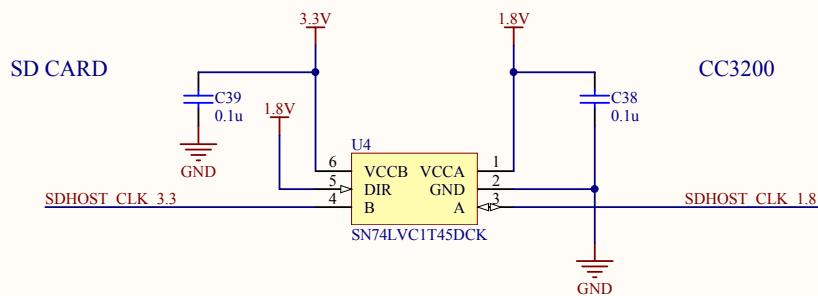
D

Hello		REV
TITLE	M4F MCU_Antennas	DVT
DATE	D. Fusi	DRAWN BY
10/30/2014		SHEET 6 OF 7

A

A

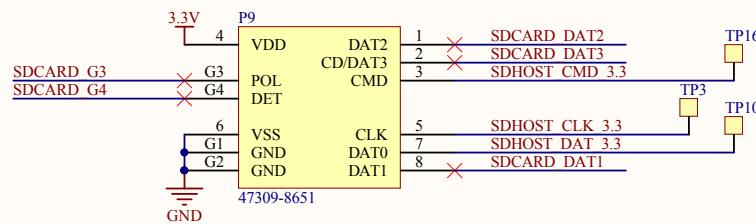
CLK needs a dedicated level shifter because of speed



B

B

CMD and DAT shifter on dedicated level shifter



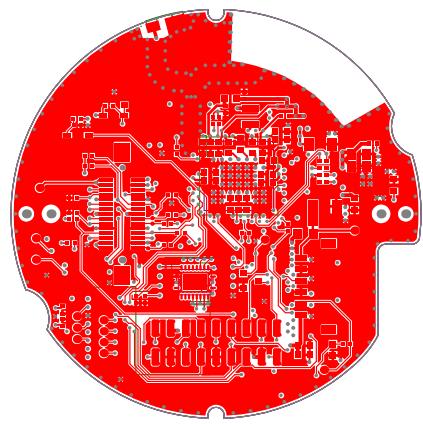
SD Card connector

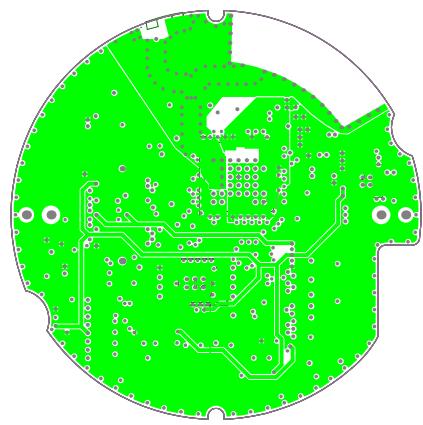
D

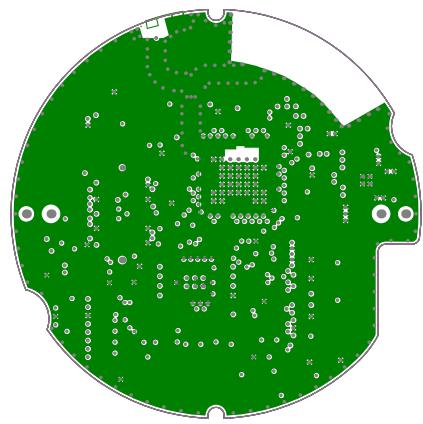
D

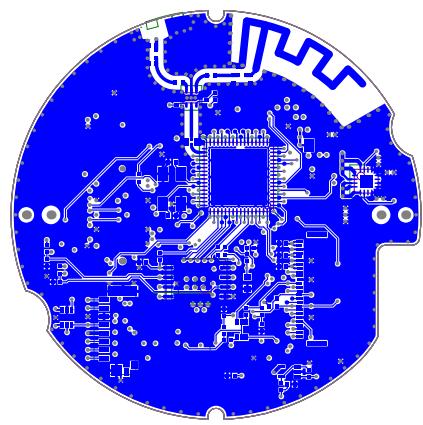
Hello

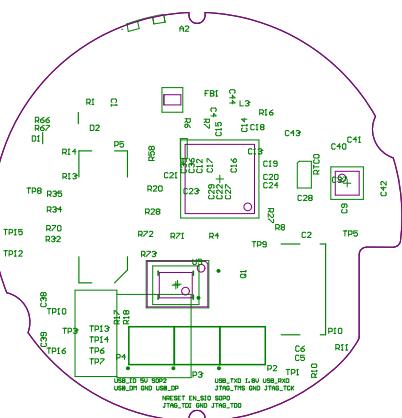
TITLE	REV
SD_Card	DVT
DATE	DRAWN BY
10/24/2014	D. Fusi

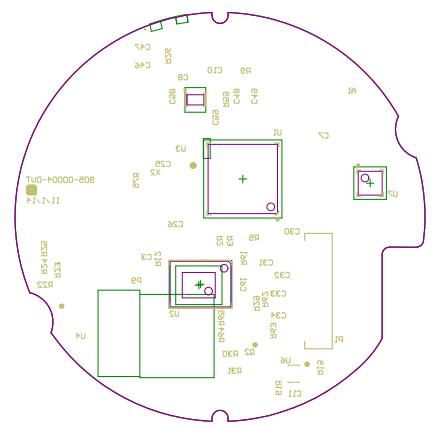


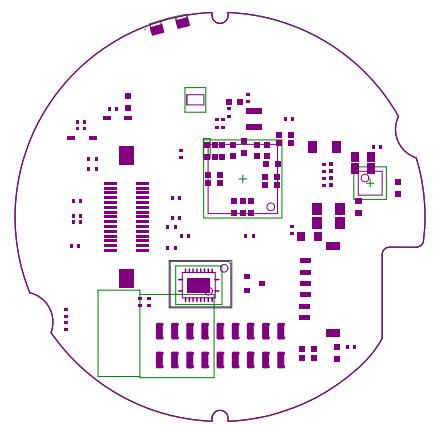


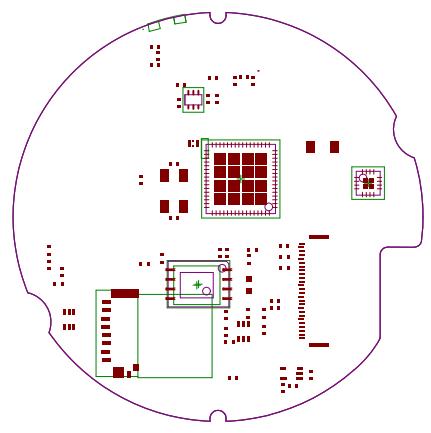


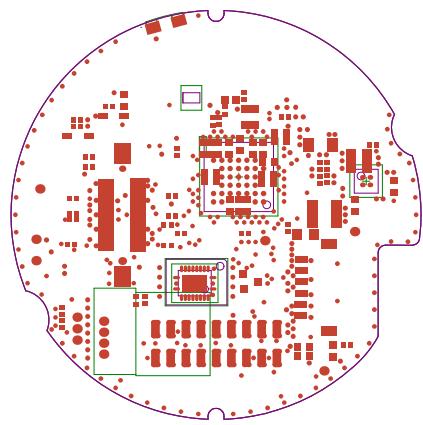


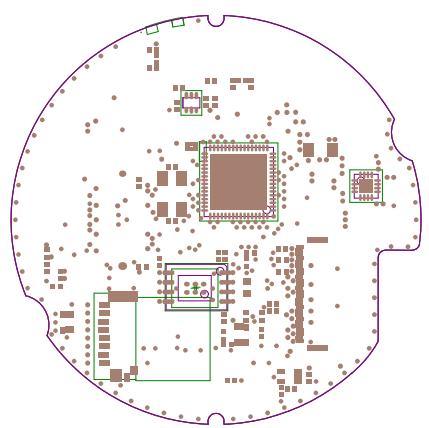


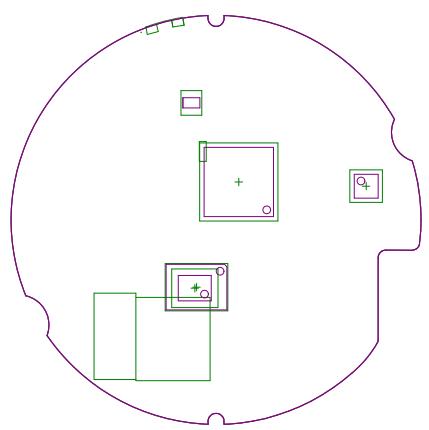


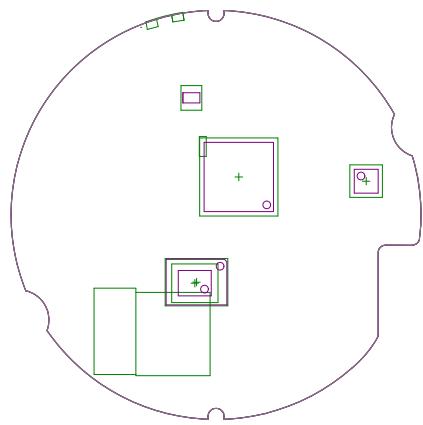


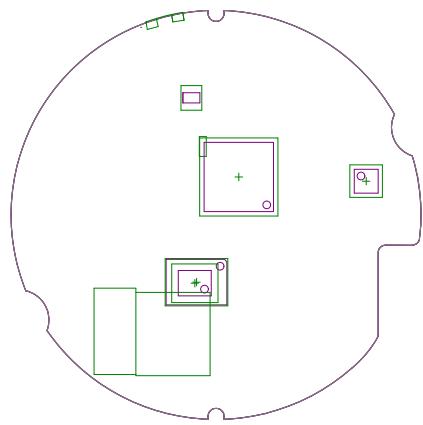


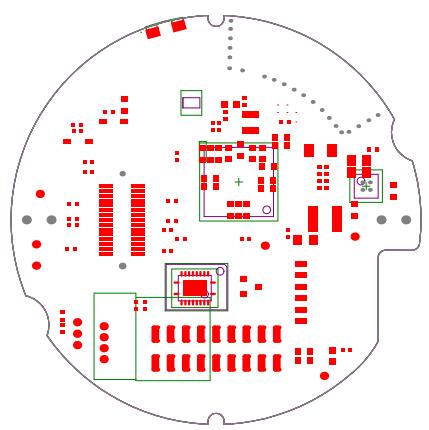


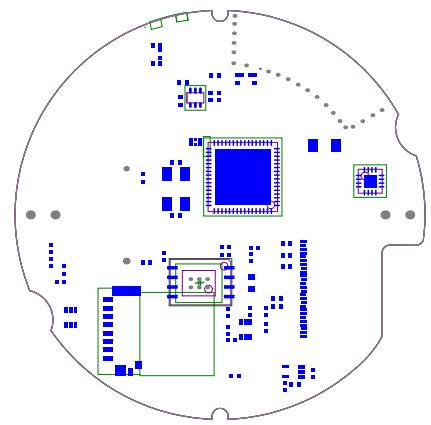


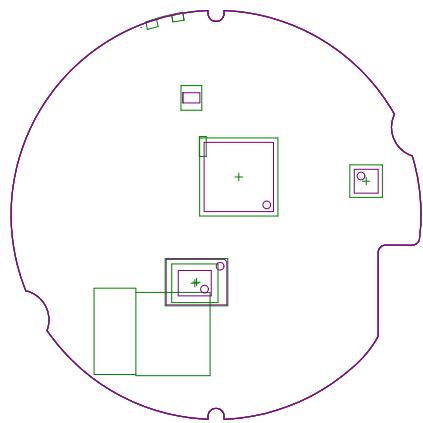












Fabrication / Assembly Notes

1. Material: Rigid FR-4, RoHS compliant: material should meet or exceed requirements of IPC 4101/129
2. Number of electrical layers: 6
3. Trace / Space minimum: 5mil (all layers)
4. Thickness: 0.76mm (finished)
5. Finish: ENIG plating on exposed copper
6. Soldermask: per IPC-SM-840, color black, registration within +/- 50um of circuit layer
7. Silkscreen: do printed silkscreen on top and bottom layers, color white.
8. .45mm traces on Bottom layer are 50 ohm +/- 5 Ohm controlled impedance traces.
9. Board must be lead free process compatible and able to withstand minimum of 5 cycles at 250 degrees celsius
10. All Test/QA/QC markings to be made on back side of PCB
11. x mousebites shall be no larger than 0.05 mm

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Paste				
2	Top Overlay				
3	Top Solder	Solder Resist	0.010mm	3.5	
4	Top Layer	Copper	0.025mm		
5	Dielectric1	FR-4	0.102mm	4.2	
6	Signal Layer 1	Copper	0.025mm		
7	Dielectric 5		0.203mm	4.2	
8	Signal Layer 2	Copper	0.025mm		
9	Dielectric 4		0.102mm	4.2	
10	GND	Copper	0.025mm		
11	Dielectric2		0.203mm	4.2	
12	PWR	Copper	0.025mm		
13	Dielectric3		0.102mm	4.2	
14	Bottom Layer	Copper	0.025mm		
15	Bottom Solder	Solder Resist	0.010mm	3.5	
16	Bottom Overlay				
17	Bottom Paste				

Symbol	Hit Count	Finished Hole Size	Plated	Hole Type
✖	1	0.700mm (27.56mil)	NPTH	Round
▼	1	0.900mm (35.43mil)	NPTH	Round
■	2	1.800mm (70.87mil)	PTH	Round
●	2	2.200mm (86.61mil)	PTH	Round
✿	33	0.300mm (11.81mil)	PTH	Round
○	117	0.305mm (12.01mil)	PTH	Round
□	304	0.200mm (7.87mil)	PTH	Round
460 Total				

