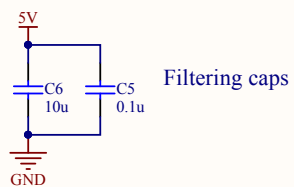
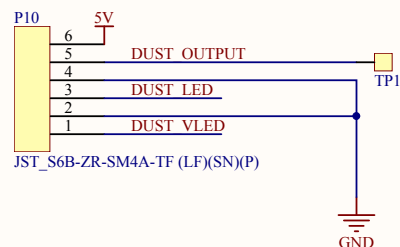


Route ground traces for C15, C16 and C17 to single vias on the EPAD. Isolate them from pours in inner layers

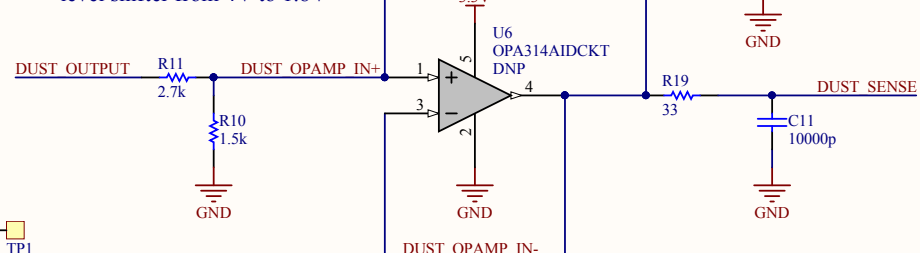
Hello

TITLE M4F_MCU_Power		REV DVT
DATE 11/17/2014	DRAWN BY D. Fusi	SHEET 3 OF 7

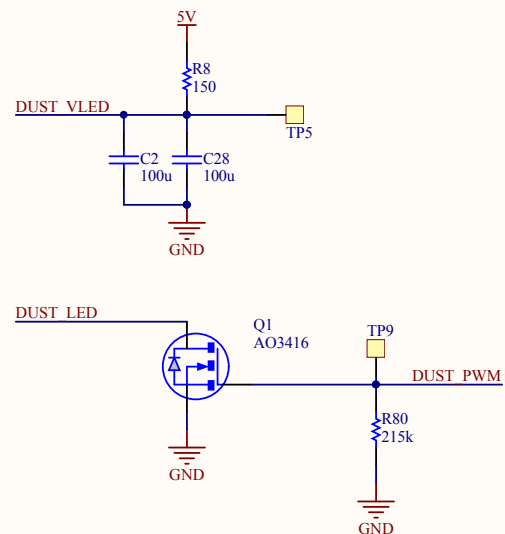
Connector for Sharp dust sensor GP2Y1010AU0F



level shifter from 4V to 1.8V

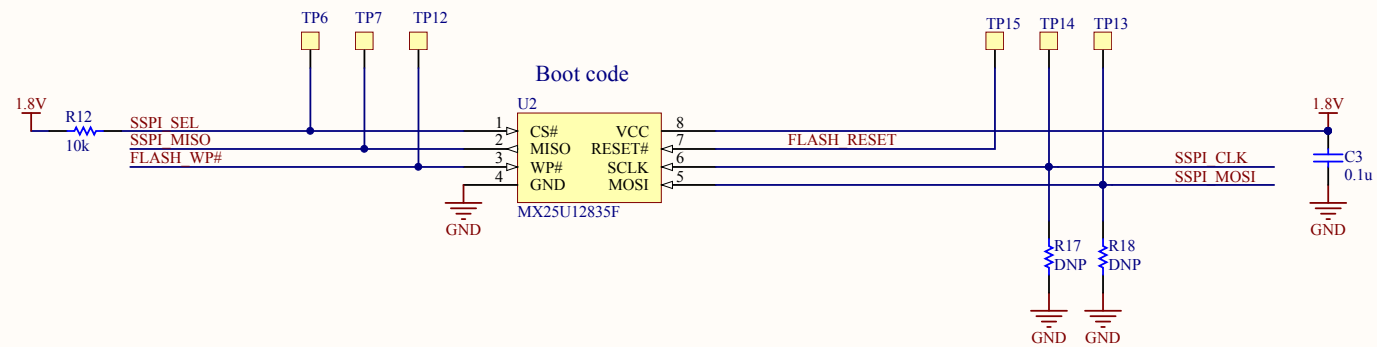


As on the GP2Y1010 datasheet

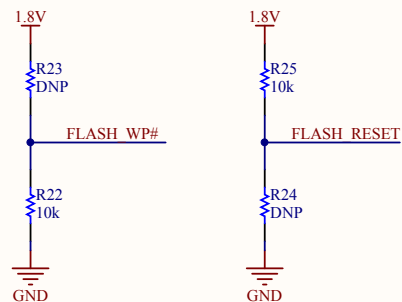


Hello

TITLE Air_quality		REV DVT
DATE 11/17/2014	DRAWN BY D. Fusi	SHEET 4 OF 7

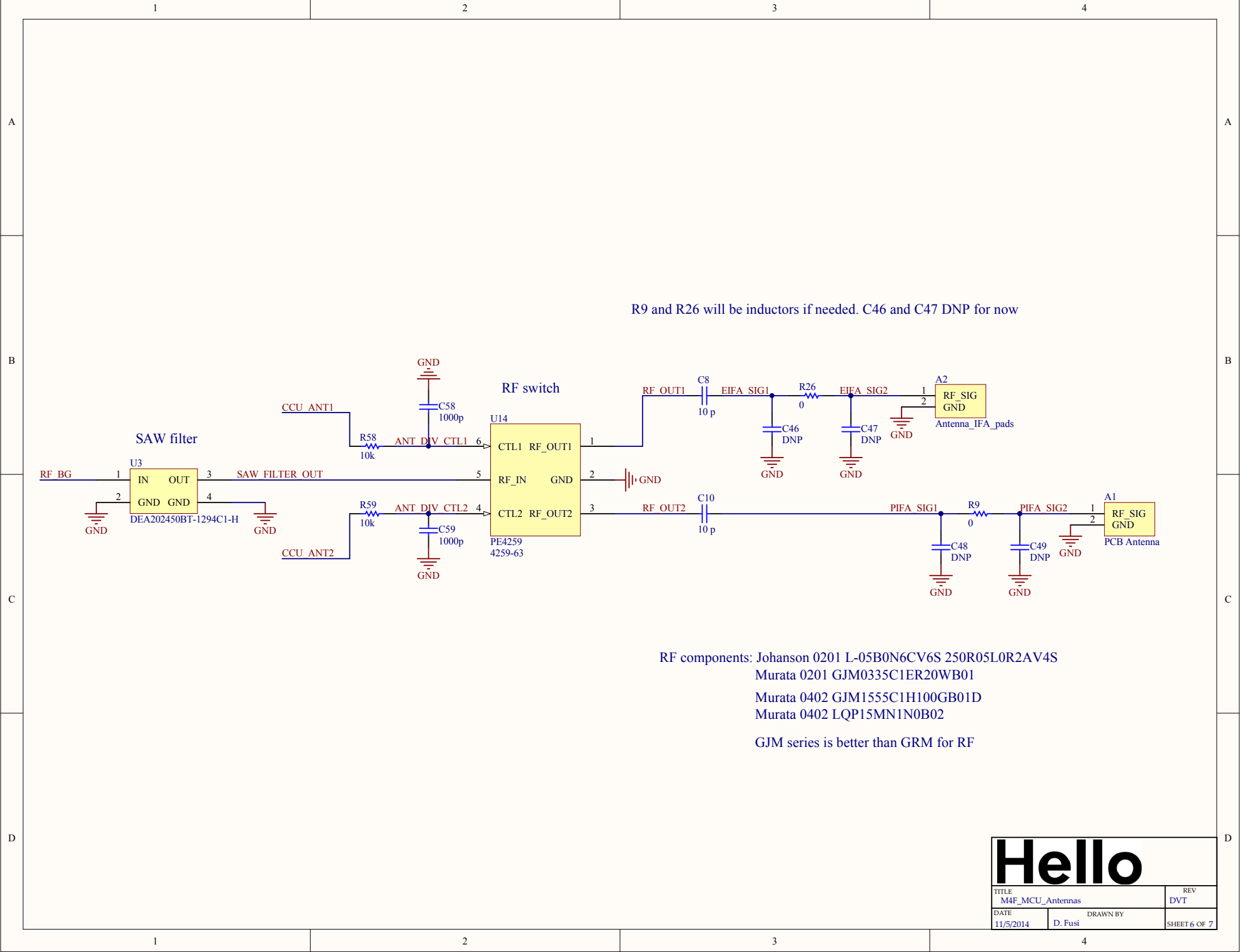


TI wants 17 and R18 to be installed but we've always been good without



Datasheet is unclear, so for now we pull reset high and WP low

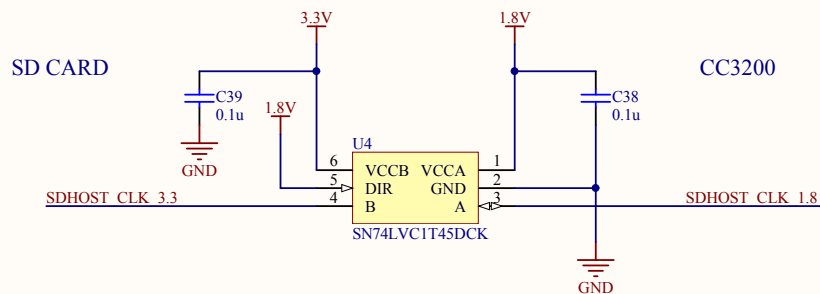
<h1>Hello</h1>		
TITLE Flash memory		REV DVT
DATE 10/30/2014	DRAWN BY D. Fusi	SHEET 5 OF 7



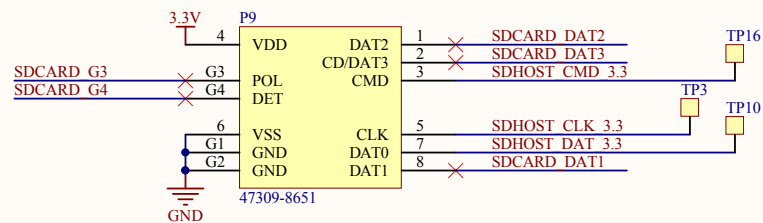
Hello

TITLE M4F_MCU_Antennas		REV DVT
DATE 11/5/2014	DRAWN BY D. Fusi	SHEET 6 OF 7

CLK needs a dedicated level shifter beacuse of speed



CMD and DAT shifter on dedicated level shifter



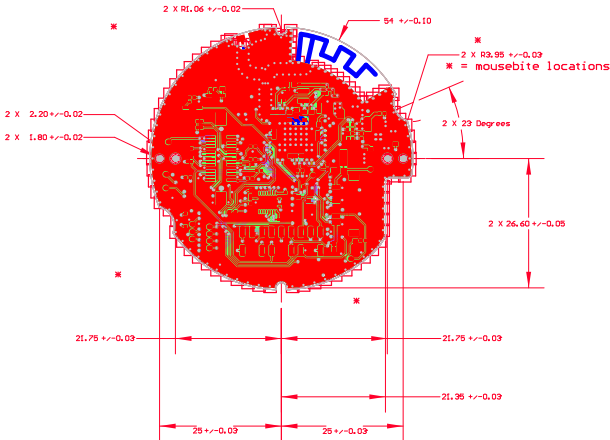
SD Card connector

Hello		
TITLE	REV	
SD_Card	DVT	
DATE	DRAWN BY	
10/24/2014	D. Fusi	SHEET 7 OF 7


Fabrication / Assembly Notes

- 1. Material: Rigid FR-4, RoHS compliant; material should meet or exceed requirements of IPC 4101/129
- 2. Number of electrical layers: 6
- 3. Trace / Space minimum: 5mil (all layers)
- 4. Thickness: 0.782mm (31mils) finished
- 5. Finish: ENIG plating on exposed copper
- 6. Soldermask: per IPC-SM-840, color matte black, registration within +/- 50um of circuit layer
- 7. Silkscreens: do printed silkscreen on top and bottom layers, color white. Clip on pads.
- 8. Board must be lead free process compatible and able to withstand minimum of 5 cycles at 250 degrees celsius
- 9. All Test/QA/QC markings to be made on back side of PCB
- 10. x mousebites shall be no larger than 0.05 mm
- 11. All Dimensions are after plating/finishing
- 12. All components must be placed within +/- 0.10mm
- 13. This is a controlled impedance board between Layers 5 and 6.
0.45mm traces on Bottom layer (layer 6) are 50 ohm +/-5 Ohm controlled impedance traces referenced to layer 5.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Paste				
2	Top Overlay				
3	Top Solder	Solder Resist	0.010mm	3.5	
4	Top Layer	Copper	0.025mm		
5	Dielectric1	FR-4	0.102mm	4.2	
6	Signal Layer 1	Copper	0.025mm		
7	Dielectric 5		0.152mm	4.2	
8	Signal Layer 2	Copper	0.025mm		
9	Dielectric 4		0.102mm	4.2	
10	GND	Copper	0.025mm		
11	Dielectric2		0.152mm	4.2	
12	PdR	Copper	0.025mm		
13	Dielectric3		0.102mm	4.2	
14	Bottom Layer	Copper	0.025mm		
15	Bottom Solder	Solder Resist	0.010mm	3.5	
16	Bottom Overlay				
17	Bottom Paste				



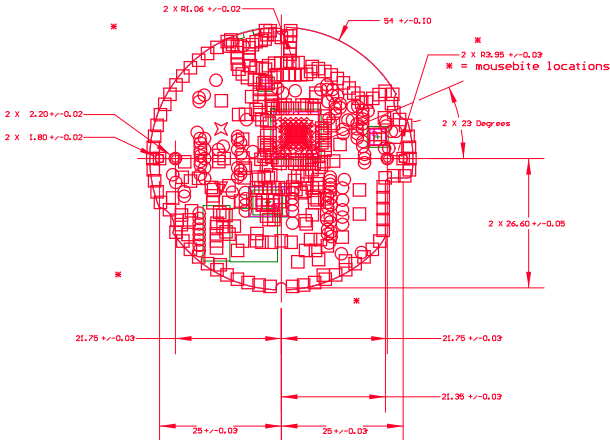
Symbol	Hit Count	Finished Hole Size	Plated	Hole Type
⌘	1	0.700mm (27.56mil)	NPTH	Round
▼	1	0.900mm (35.43mil)	NPTH	Round
■	2	1.800mm (70.87mil)	PTH	Round
●	2	2.200mm (86.61mil)	PTH	Round
⊙	33	0.300mm (11.81mil)	PTH	Round
○	122	0.305mm (12.01mil)	PTH	Round
□	309	0.200mm (7.87mil)	PTH	Round
	470 Total			

METRIC		DRAWER	DATE		
DIMENSIONS ARE IN MILLIMETERS		DESIGNER	DATE		
TOLERANCES		rsb/dfusi	11/17/14	TITLE: Morpheus Middle Board	
0 > - < 2 0.05		PROPRIETARY AND CONFIDENTIAL		THE INFORMATION CONTAINED IN THIS DRAWING IS THE SOLE PROPERTY OF HELLO INC.	
2 > - < 10 0.08					
10 > - < 50 0.10					
50 > - < 100 0.15					
100 > - < 200 0.20					
200 > - 0.20		ANY REPRODUCTION IN PART OR AS A WHOLE WITHOUT THE WRITTEN PERMISSION OF HELLO INC IS PROHIBITED.		SIZE B DWG. NO. 201-00004-04	
ANGLES 1.00				REV	
				SCALE: 1:1 WEIGHT: SHEET 1 OF 1	

Fabrication / Assembly Notes

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METRIC		DRAWER	DATE		
DIMENSIONS ARE IN MILLIMETERS		DESIGNER	DATE		
TOLERANCES		rsb/dfusi	11/17/14	TITLE: Morpheus Middle Board	
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2 > - < 10 0.08					
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100 > - < 200 0.20					
200 > - 0.20		ANY REPRODUCTION IN PART OR AS A WHOLE WITHOUT THE WRITTEN PERMISSION OF HELLO INC IS PROHIBITED.		SIZE B	
ANGLES 1.00				DWG. NO. 201-00004-04	
				REV	
				SCALE: 1:1	
				WEIGHT:	
				SHEET 1 OF 1	

