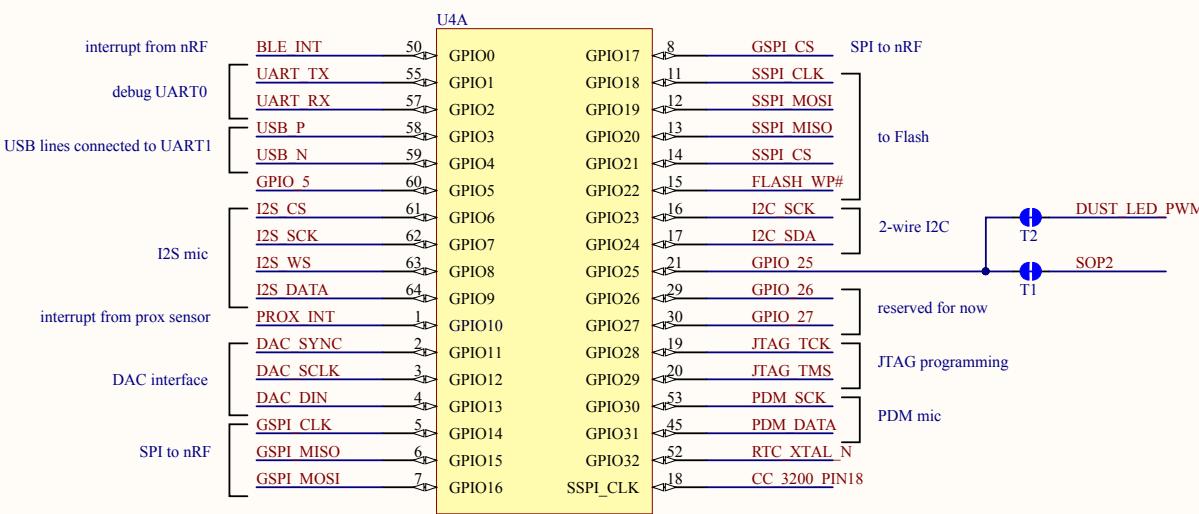
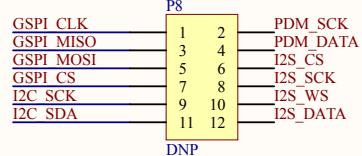
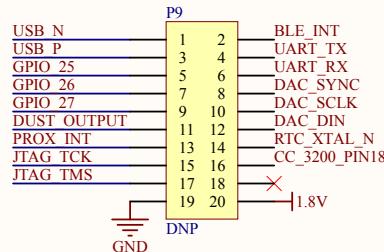
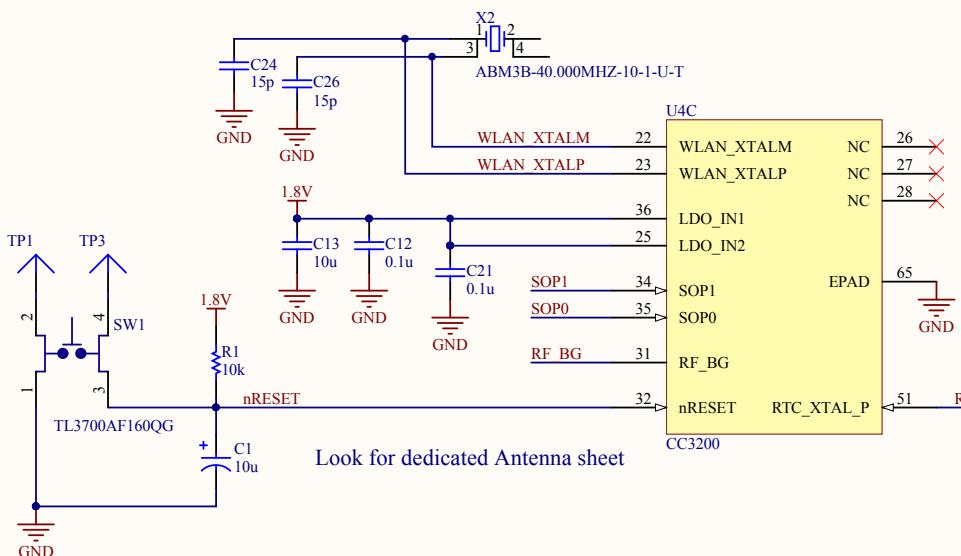
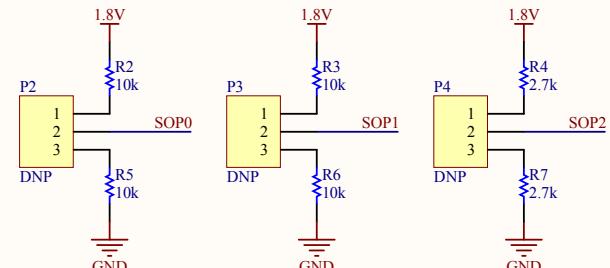


Debugging connectors



pin 52 can be used as GPIO when getting 32 kHz clk from another IC
pin 18 is not usable as GPIO

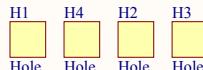
JTAG available to the developer via TMS and TCK pins
Defaults: P1 = 1-2, P2 = 2-3, P3 = 2-3



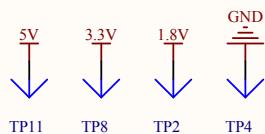
Look for dedicated Antenna sheet

Hello

TITLE	REV
M4F MCU	1
6/16/2014	D. Fusi

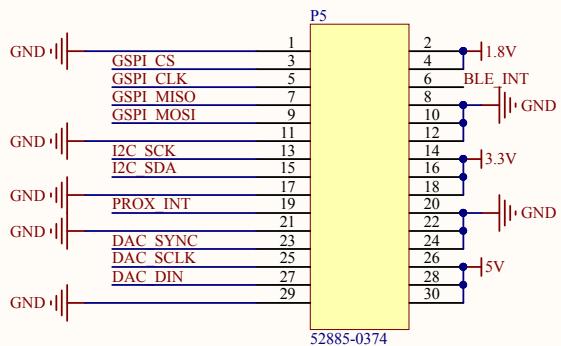


mounting holes

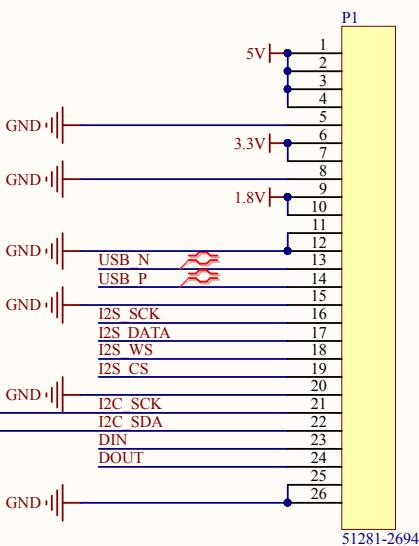


to the bottom board

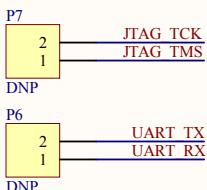
to the top board



I2C pullups



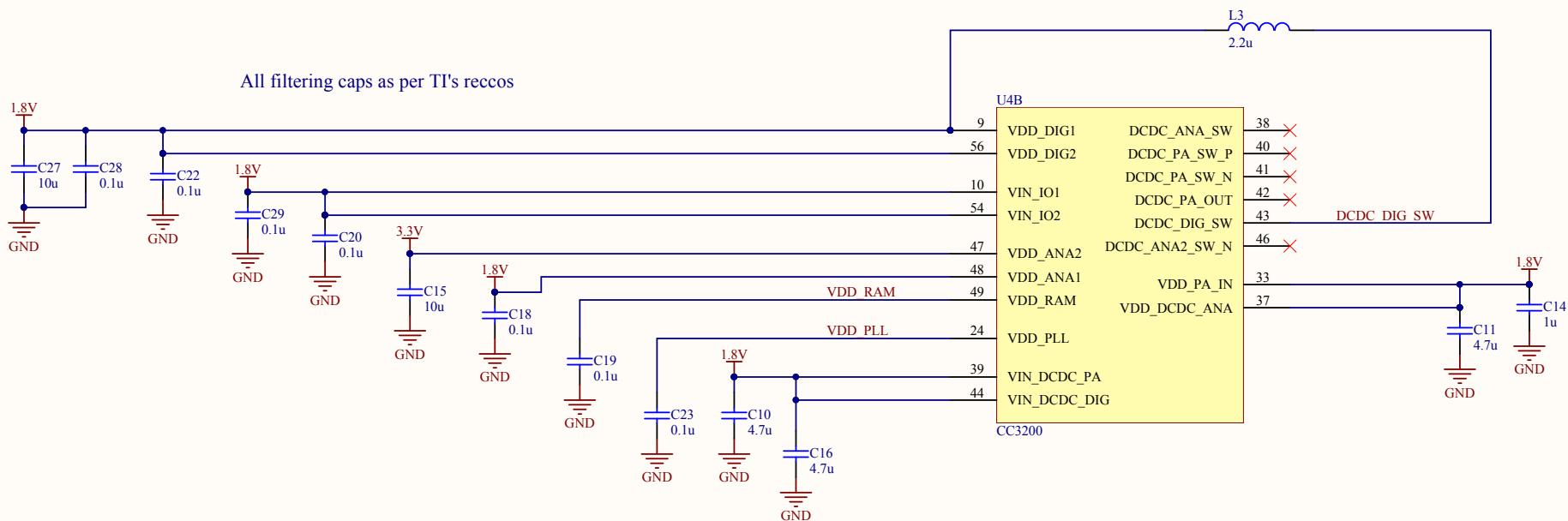
programming / debugging connectors



Hello

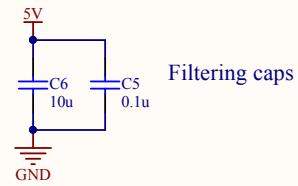
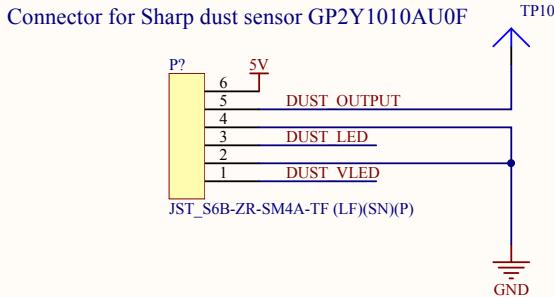
TITLE	REV
Morpheus_middle	1
DATE	DRAWN BY
6/13/2014	D. Fusi
SHEET 2 OF 6	

All filtering caps as per TI's reccos

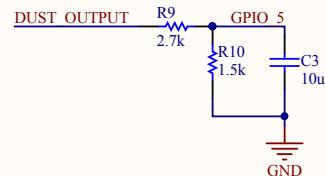


Hello

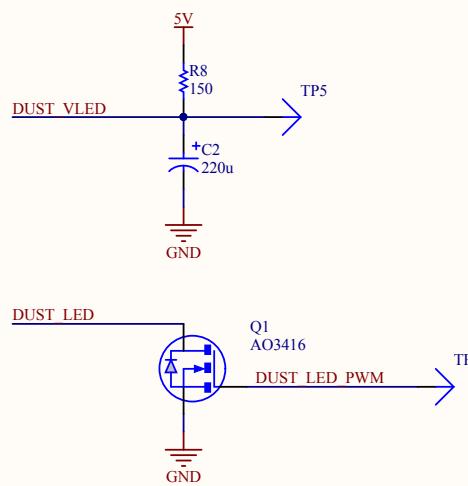
TITLE		REV
M4F MCU Power		1
DATE	DRAWN BY	
6/13/2014	D. Fusi	SHEET 3 OF 6



level shifting from 4V to 1.8V, plus anti-aliasing filter

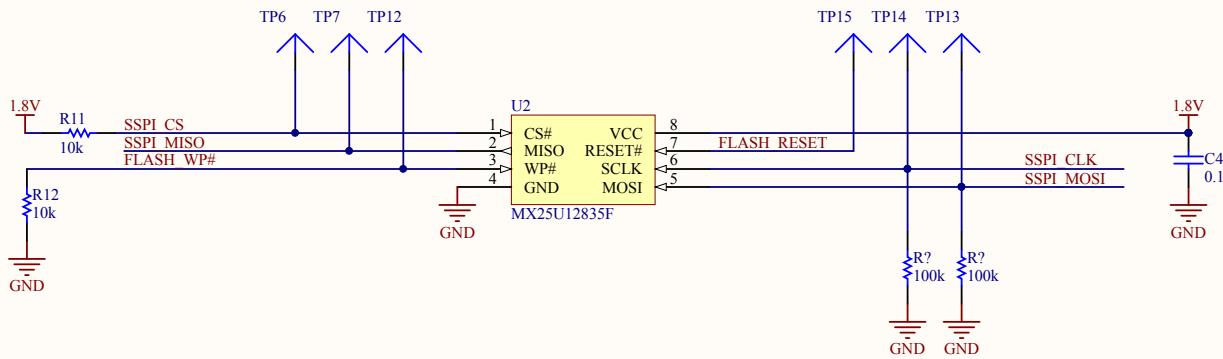


As on the GP2Y1010 datasheet



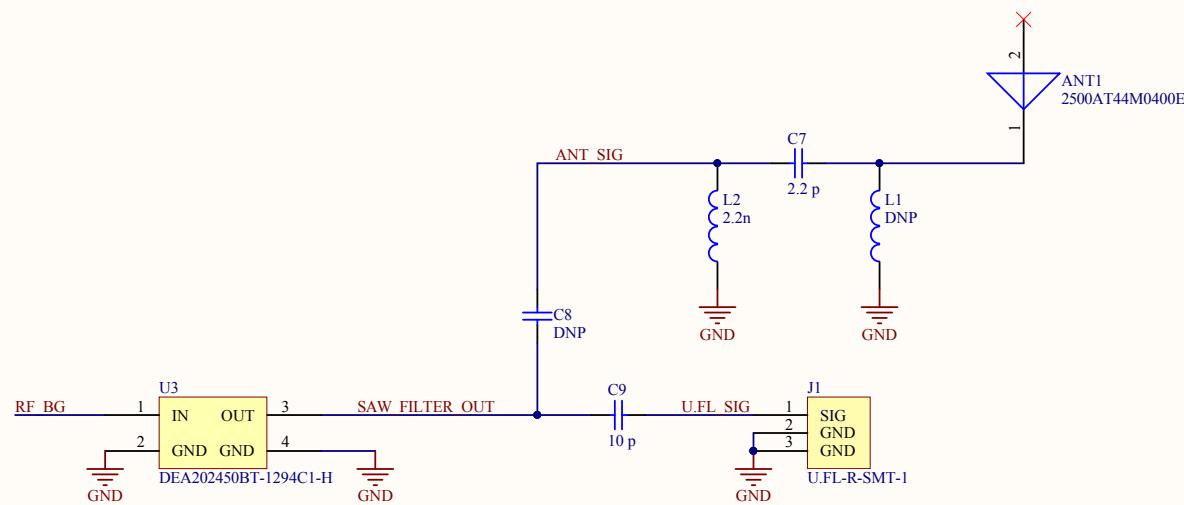
Hello

TITLE	REV
Air_quality	1
DATE	DRAWN BY
6/13/2014	D. Fusi
SHEET 4 OF 6	

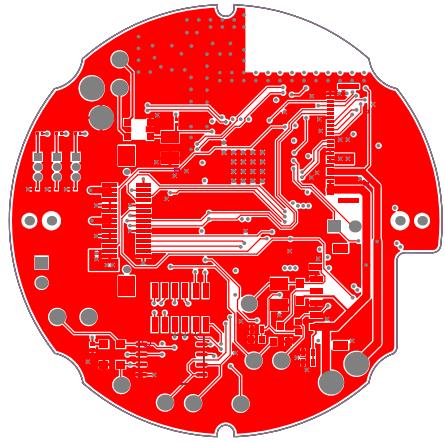


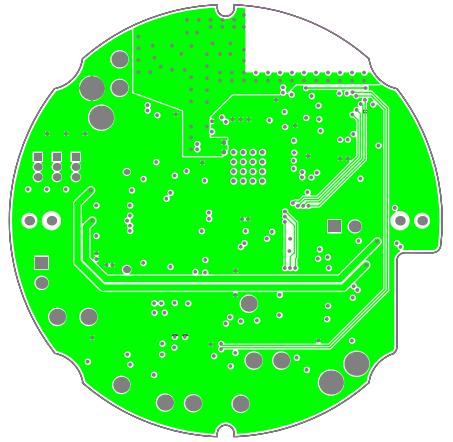
Hello

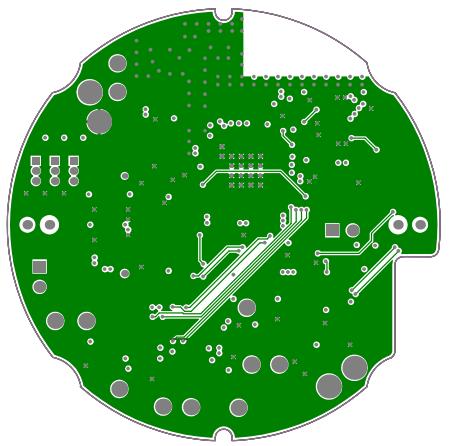
TITLE Flash memory	REV 1
DATE 6/10/2014	DRAWN BY D. Fusi
SHEET 5 OF 6	

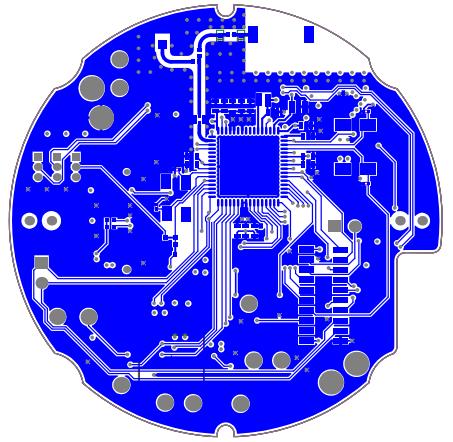


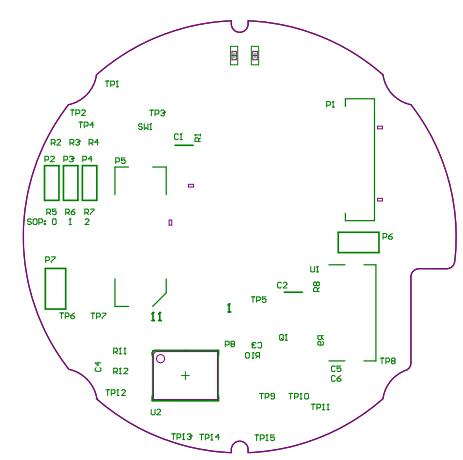
Hello	
TITLE M4F MCU_Antennas	REV 1
DATE 6/16/2014	DRAWN BY D. Fusi
SHEET 6 OF 6	

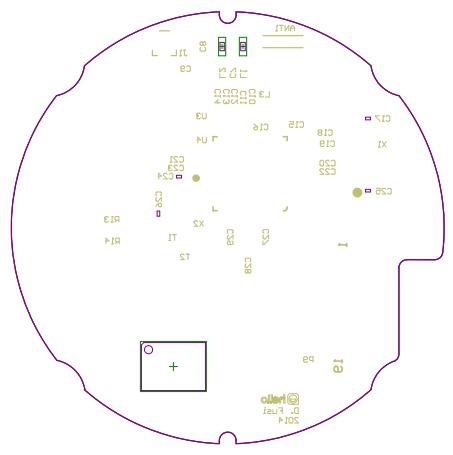


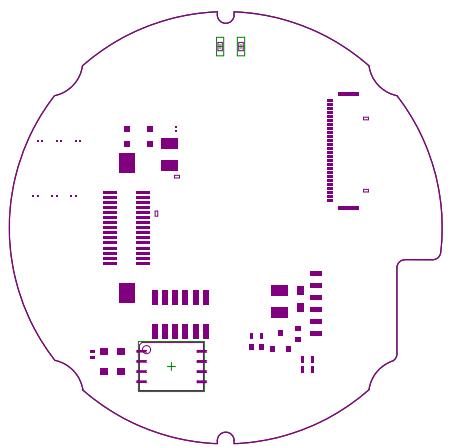


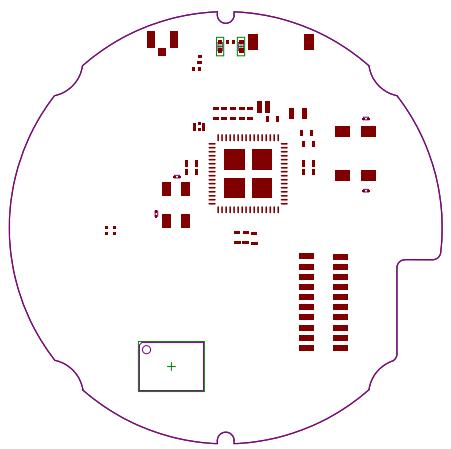


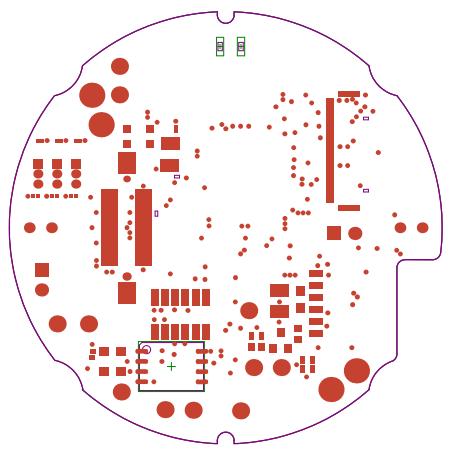


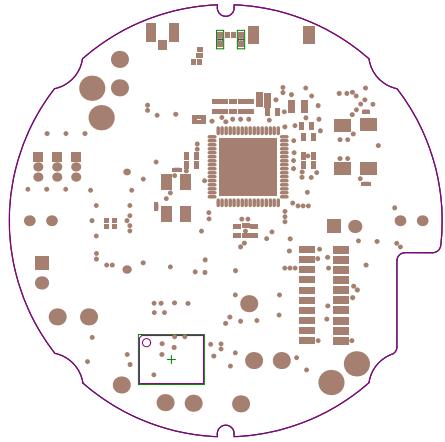


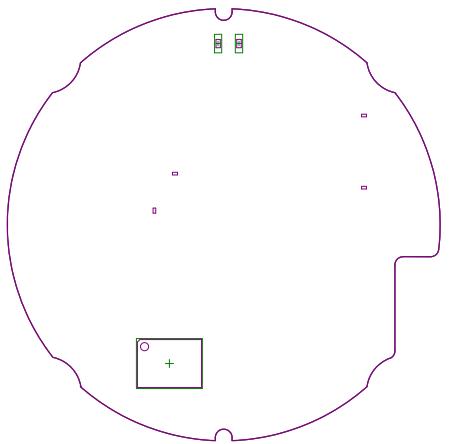


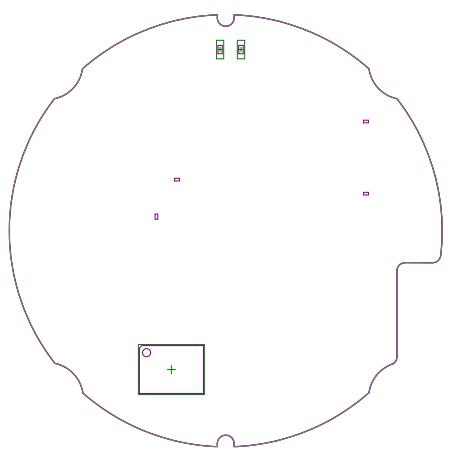


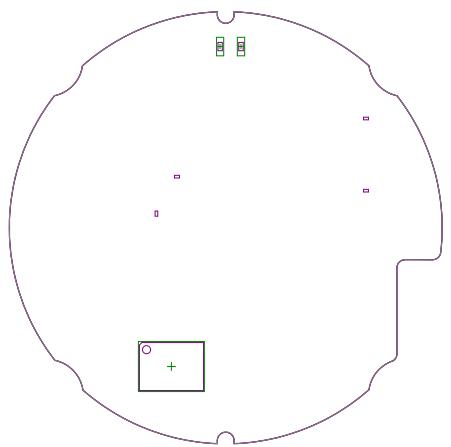


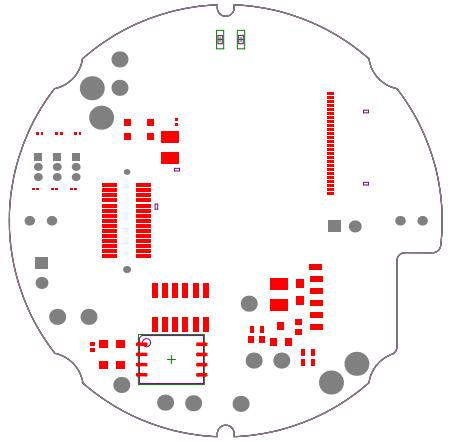


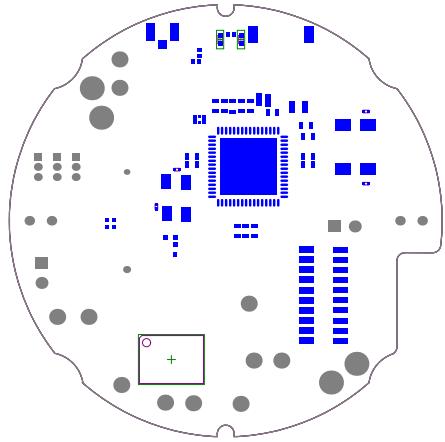


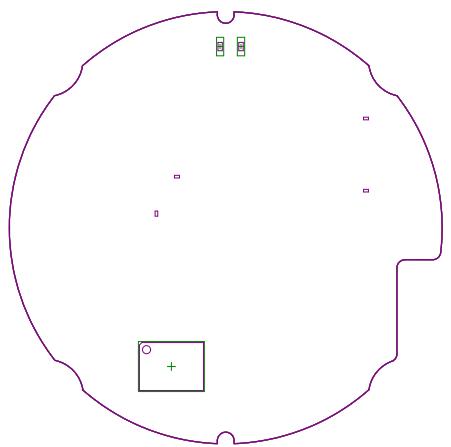












Fabrication / Assembly Notes

1. Material: Rigid
2. Number of electrical layers: 4
3. Trace / Space minimum: 5mil (all layers)
4. Thickness: 0.76mm (finished)
5. Finish: ENIG plating on exposed copper
6. Soldermask: per IPC-SM-840, color green registration within +/- 50um of circuit layer
7. Silkscreen: do print silkscreen on top and bottom layers
8. RoHS: parts shall be RoHS compliant as per European Union directive 2002/95/EC
9. Board must be lead free process compatible and able to withstand minimum of 5 cycles at 250 degrees celsius
10. All Test/QA/QC markings to be made on back side of PCB

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Paste				
2	Top Overlay				
3	Top Solder	Solder Resist	0.010mm	3.5	
4	Top Layer	Copper	0.036mm		
5	Dielectric 1	FR-4	0.254mm	4.2	
6	GND	Copper	0.017mm		
7	Dielectric 3		0.127mm	4.2	
8	PWR	Copper	0.017mm		
9	Dielectric 2		0.254mm	4.2	
10	Bottom Layer	Copper	0.036mm		
11	Bottom Solder	Solder Resist	0.010mm	3.5	
12	Bottom Overlay				
13	Bottom Paste				

Symbol	Hit Count	Finished Hole Size	Plated	Hole Type
◊	1	0.700mm (27.56mil)	NPTH	Round
☒	1	0.900mm (35.43mil)	NPTH	Round
○	2	1.700mm (66.93mil)	NPTH	Round
☒	2	2.100mm (82.68mil)	NPTH	Round
◊	4	0.900mm (35.43mil)	PTH	Round
☒	4	2.400mm (94.49mil)	PTH	Round
□	9	0.600mm (23.62mil)	PTH	Round
▽	11	1.700mm (66.93mil)	PTH	Round
▼	18	0.300mm (11.81mil)	PTH	Round
■	227	0.200mm (7.87mil)	PTH	Round
279 Total				

