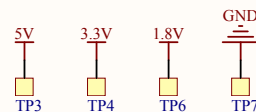
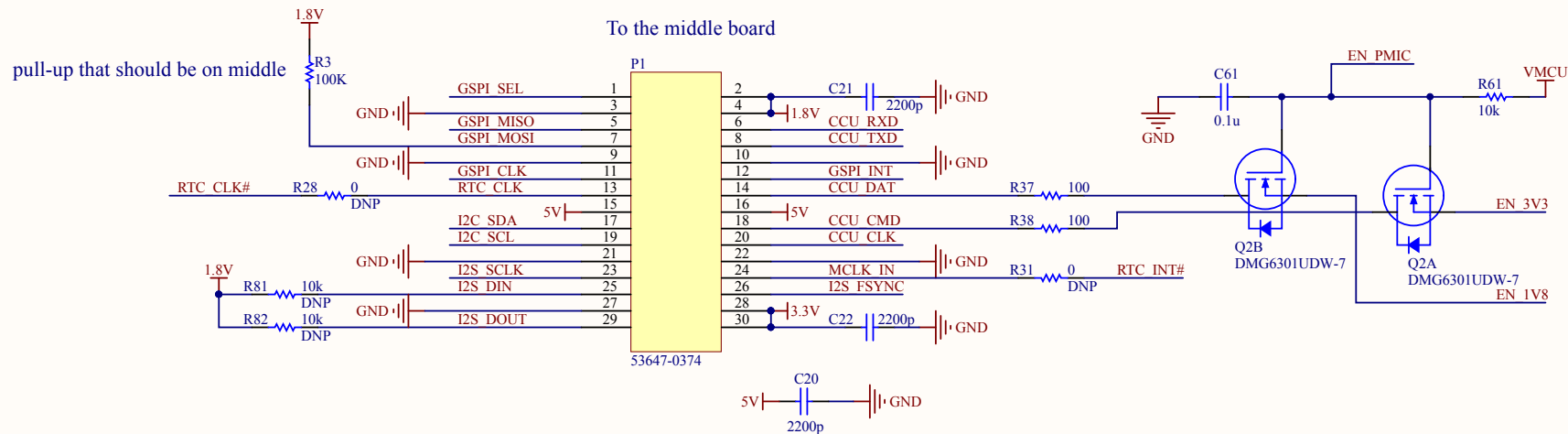
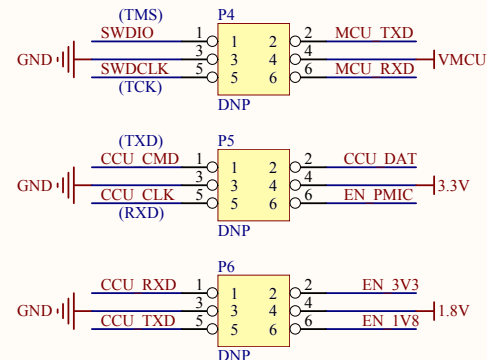




Mounting holes

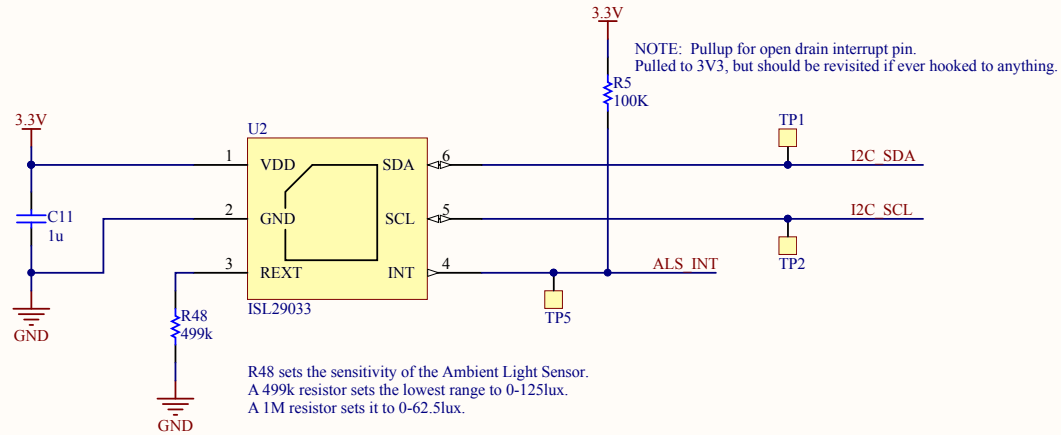


Break Out Board Development



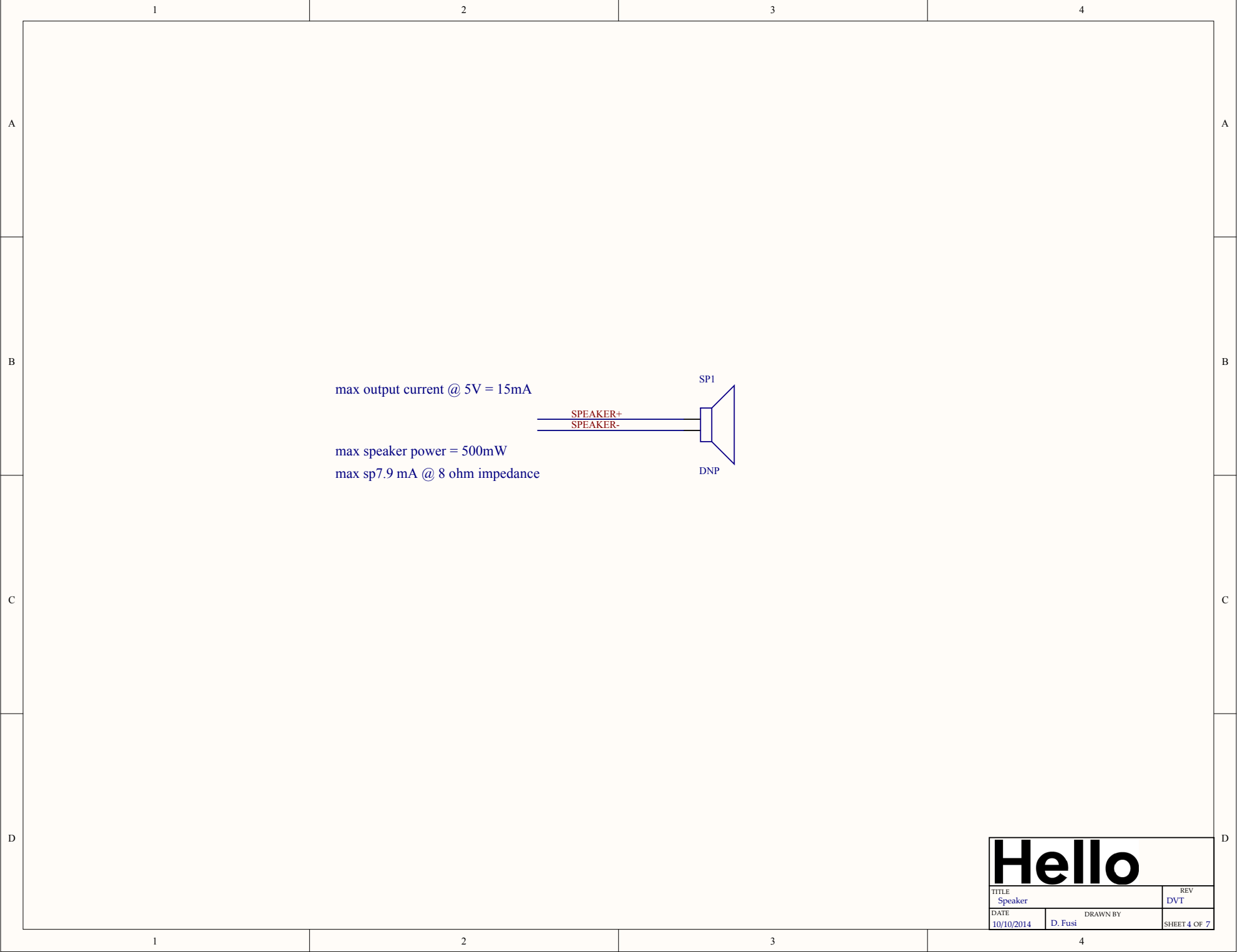
Hello

TITLE Morpheus top		REV DVT
DATE 11/13/2014	DRAWN BY D. Fusi	SHEET 1 OF 7



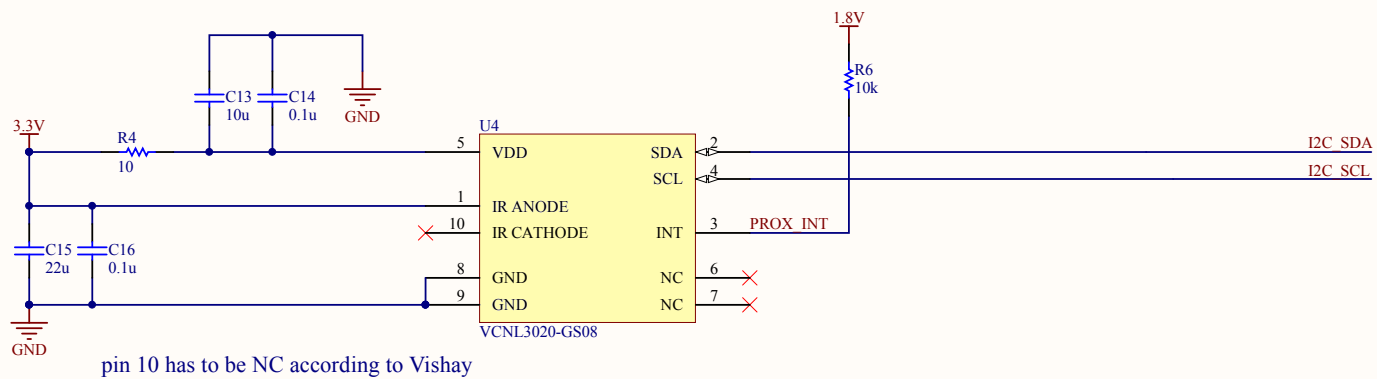
Hello	
TITLE ALS	REV DVT
DATE 11/13/2014	DRAWN BY D. Fusi
SHEET 2 OF 7	





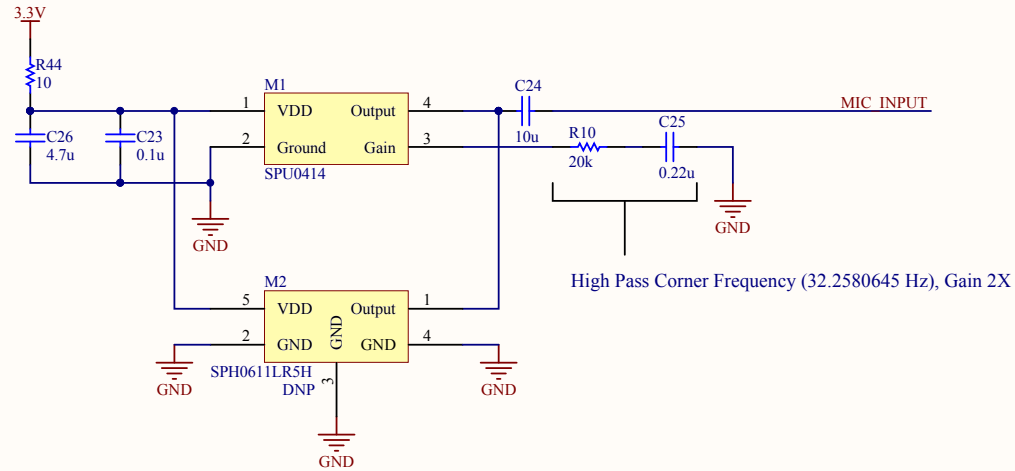
Hello

TITLE		REV
Speaker		DVT
DATE	DRAWN BY	
10/10/2014	D. Fusi	SHEET 4 OF 7

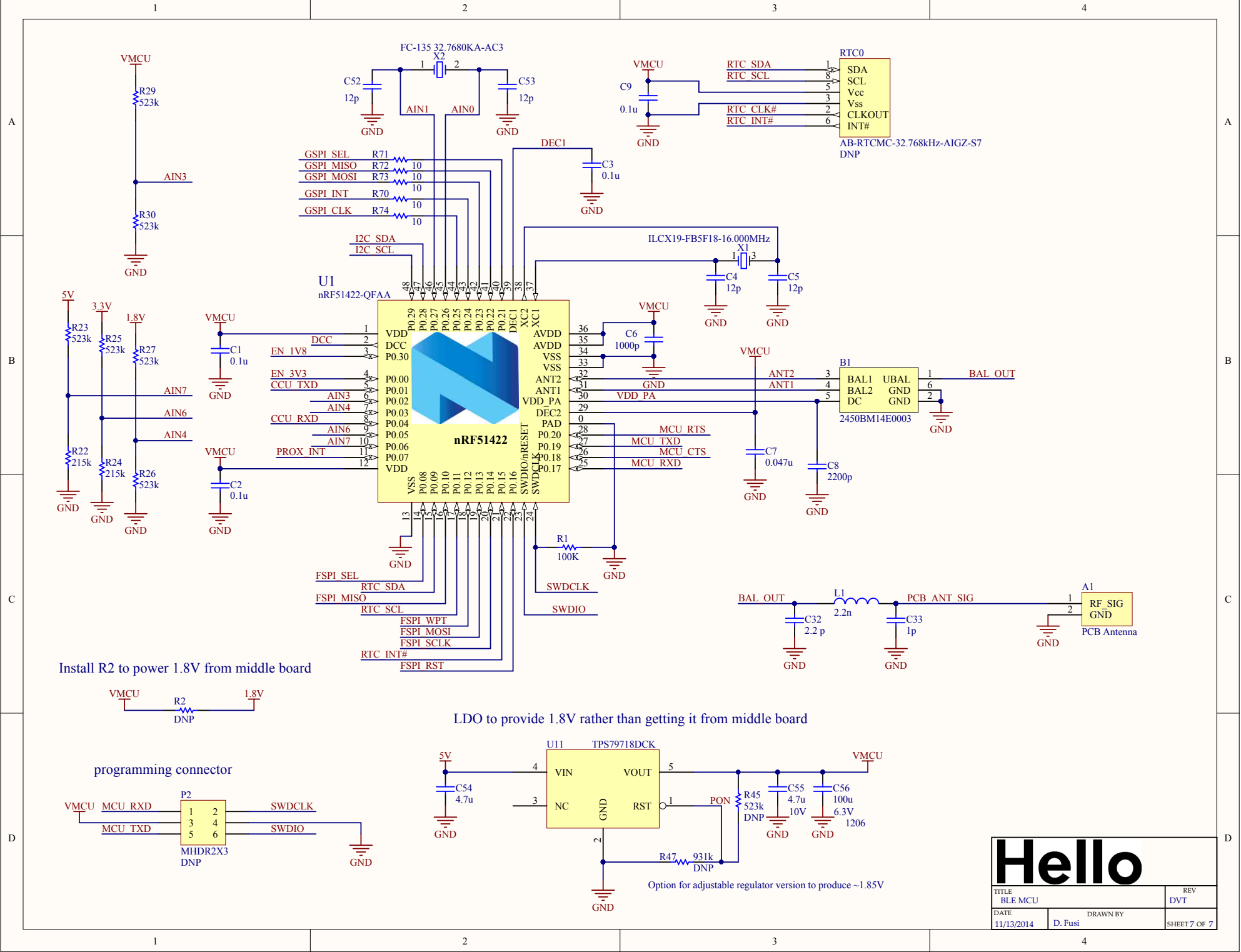


<h1>Hello</h1>		
TITLE	Proximity	REV
DATE	11/13/2014	DVT
DRAWN BY	D. Fusi	SHEET 5 OF 7

M1 is top port mic, M2 is bottom port mic. Only one can be installed at a time



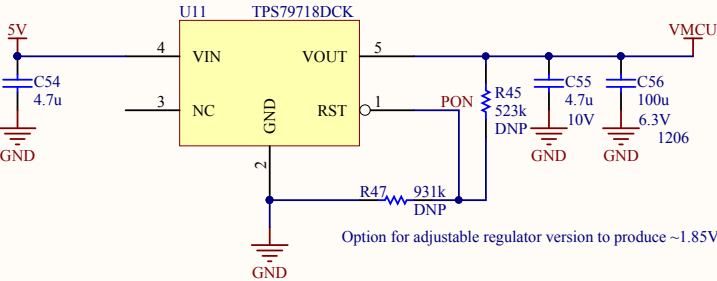
Hello		
TITLE	Microphone	REV
DATE	D. Fusi	DVT
11/13/2014		SHEET 6 OF 7



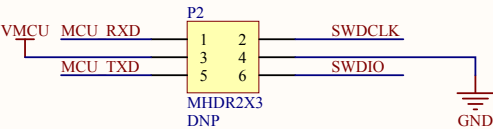
Install R2 to power 1.8V from middle board



LDO to provide 1.8V rather than getting it from middle board



programming connector



Hello

TITLE BLE MCU		REV DVT
DATE 11/13/2014	DRAWN BY D. Fusi	SHEET 7 OF 7

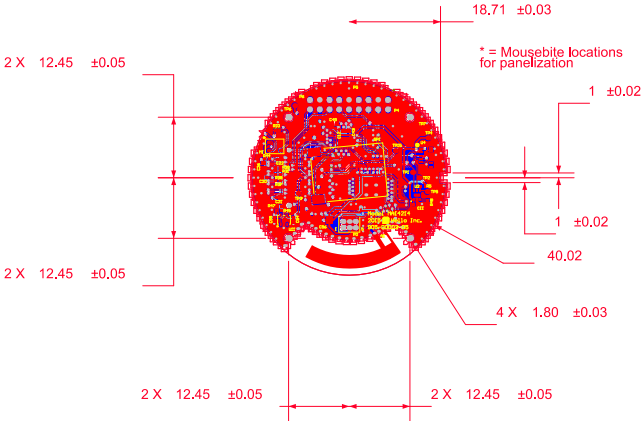
Fabrication / Assembly Notes


1. Material: Rigid FR-4, RoHS compliant; material should meet or exceed requirements of IPC 4101/126. ITEQ IT-180A Pre-approved.
2. Number of electrical layers: 4
3. Trace / Space minimum: 5mil (all layers)
4. Thickness: 0.786mm (finished)
5. Finish: ENIG plating on exposed copper
6. Soldermask: per IPC-SM-840, color matte black registration within +/- 76um of circuit layer
7. Silkscreens: use white silkscreen on top and bottom layers
8. Board must meet or exceed 94U-0
9. Board must be lead free process compatible and able to withstand minimum of 5 cycles at 250 degrees celsius
10. All Test/QA/QC markings to be made on back side of PCB
11. x mousebites shall be no larger than 0.05 mm
12. 0.25mm radius around sharp edges like the notch on the right side
13. All Dimensions are after plating/finishing
14. All components must be placed within +/- 0.10mm
15. This is a controlled impedance board between layers 3 and 4.
0.45mm traces on Bottom (Layer 4) are 50 Ohms +/- 5 Ohm controlled impedance traces referenced to layer 3.
Fab vendor to adjust trace width as needed but no smaller than .18mm without approval.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Paste				
2	Top Overlay				
3	Top Solder	Solder Resist	0.010mm	3.5	
4	TOP	Copper	0.036mm		
5	Dielectric1	FR-4	0.127mm	4.2	
6	SIG	Copper	0.017mm		
7	Dielectric3	FR-4	0.406mm	4.2	
8	GND	Copper	0.017mm		
9	Dielectric2	FR-4	0.127mm	4.2	
10	BOT	Copper	0.036mm		
11	Bottom Solder	Solder Resist	0.010mm	3.5	
12	Bottom Overlay				
13	Bottom Paste				

TOP Layer 1oz Cu
SIG Layer 5 mil Drilling 0.5oz Cu
GND Layer 16 mil Core 31 +/- 4 mils
BOT Layer 5 mil Drilling 0.5oz Cu
1oz Cu

Symbol	Hit Count	Finished Hole Size	Plated	Hole Type
o	1	0.325mm (12.80mil)	PTH	Round
x	1	0.700mm (27.56mil)	NPTH	Round
o	1	0.900mm (35.43mil)	NPTH	Round
v	4	0.381mm (15.00mil)	PTH	Round
⊗	4	1.800mm (70.87mil)	NPTH	Round
*	6	0.600mm (23.62mil)	PTH	Round
●	88	0.200mm (7.87mil)	PTH	Round
*	207	0.305mm (12.01mil)	PTH	Round
312 Total				



METRIC		DRAWN	DATE			
DIMENSIONS ARE IN MILLIMETERS		DESIGNER	DATE	TITLE: Morpheus Top Board		
TOLERANCES:		rsb/dyke/dfusi	12/30/14			
0 > - < 2 0.10		PROPRIETARY AND CONFIDENTIAL				
2 > - < 10 0.10						
10 > - < 50 0.10						
50 > - < 100 0.15						
100 > - < 200 0.20						
200 > - 0.20		THE INFORMATION CONTAINED IN THIS DRAWING IS THE SOLE PROPERTY OF HELLO INC.				
ANGLES 1.00		ANY REPRODUCTION IN PART OR AS A WHOLE WITHOUT THE WRITTEN PERMISSION OF HELLO INC IS PROHIBITED.				
SIZE	DWG.	NO.	REV			
B		201-00003-05				
SCALE: 2:1		WEIGHT:		SHEET 1 OF 1		