

# Yu-Fan (Bernie) Teng

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## RESEARCH INTEREST

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*Integrated Circuit (IC) Design; Architecture and Embedded Systems; Deep learning application in Computer Vision*

## EDUCATION

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### National Taiwan University (NTU)

Taipei, Taiwan

*Bachelor of Science in Electrical Engineering (NTUEE)*

09/2016 – 01/2021

- CGPA: 3.7/4.0; Last 60 GPA: 3.97/4.0
- Selected Courses: Integrated Circuit Design (A), Digital System Design (A), Digital Circuits Lab (A), Integrated Circuit Design Lab (A), Electronic Circuits (A), Electronic Circuits Experiment (A)

## RESEARCH EXPERIENCE

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### Microsystem Research Lab, NTU (Advisor: Prof. Tzi-Dar Chiueh)

Taipei, Taiwan

*Undergraduate Research Student*

02/2019 – 09/2020

Topic 1: Digital signal processor taped-out IC [\[link\]](#)

- Implemented the whole IC design process from simulation to **taped-out IC**, including Matlab simulation, RTL, P&R, and DRC/LVS.
- Designed an adaptive FIR filter chip as an equalizer to eliminate the noises (Accuracy: 99 percent)

Topic 2: FloatSD machine learning acceleration hardware solution [\[link\]](#)

- Designed an efficient dataflow of FloatSD to reduce memory access
- Developed hardware format of dropout and batch normalization to accelerate the training process of CNN

### Media IC and System Lab, NTU (Advisor: Prof. Shao-Yi, Chien)

Taipei, Taiwan

*Undergraduate Research Student*

09/2018 – 01/2020

Topic: Deep learning tracking algorithm for multiple object tracking

- Developed novel siamese deep learning tracking algorithm to track and tag multiple objects
- Applied it on **2019 CVPR Multiple Object Tracking Contest**

### Digital System Design Course (Instructor: Prof. An-Yeu Wu)

Taipei, Taiwan

*Teaching Assistant*

01/2020 – 06/2020

- Prepared MIPS/RISC V class materials for students and optimized student's MIPS baseline homework
- Wrote a script in Bash and Python to grade student's homework automatically

## WORK EXPERIENCE [\[link\]](#)

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### McKinsey & Company

Taipei, Taiwan

*Analyst Intern | Design to Value Team*

07/2020 – Present

- Analyze client's product using teardown analysis and cleansheet modeling
- Solved 11 client cases with global consultants

### DBS Bank

Taipei, Taiwan

*T&O Support Analyst | Technology and Operation Team*

02/2020 – 03/2020

- Analyzed data for business analysis team by developing automatic comparison program in Python and Qlikview SQL
- Developed strategy for Iserve system call issue with banking team and credit card team

### Intel Corporation

Taipei, Taiwan

*Hardware Engineer Intern | Non-Volatile Solutions Memory Team*

06/2019 – 01/2020

- Supported NVMe SSD system-level validation and integration for Client SSD
- Designed automated hardware validation tools in Python for SSD firmware and improved the efficiency of validation by 50 percent
- Cooperated with the top laptop brand and leading SSD controller companies to analyze SSD failure

### Ganzin Technology

Taipei, Taiwan

*Product Development Engineer Intern | Eye-tracker Development Team*

09/2018 – 06/2019

- Won second place at Taiwan Pitch Night
- Developed a light detection application project of eye-tracker, and exhibited on **COMPUTEX/INNOVEX 2019**

## PUBLICATION [\[link\]](#)

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### Under review (1<sup>st</sup> author)

- **Yu-Fan Teng\***, Yu-Sheng Ting\*, Tzi-Dar Chiueh, “Batch Normalization Processor Design for Convolution Neural Network Training and Inference” , *Submitted to 2021 IEEE International Symposium on Circuits and Systems (ISCAS)*

*\* Indicates equal contribution*

## CONTEST AND AWARD [\[link\]](#)

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### NTU Outstanding Performance Award

*Taipei, Taiwan*

*15 out of 7000+ Students at NTU (USD 3,300)*

*10/2020*

- Honored of academic and research excellence at National Taiwan University

### Undergraduate Innovation Award

*Taipei, Taiwan*

*Second Prize*

*07/2020*

- Proposed our research on Batch Normalization Processor Hardware Design

### National IC Design Contest

*Hsinchu, Taiwan*

*Third Place (Among 100+ teams)*

*07/2020*

- Represented NTU in the national competition held by the Ministry of Education and won the 3<sup>rd</sup> place

### MakeNTU (The largest nationwide hardware hackathon)

*Taipei, Taiwan*

*Cathay Financial Holding Business Award (USD 1,600)*

*05/2019*

- Used techniques such as RPI, CNN, SVM, and Azure (Microsoft) to create a Supermarket AI Assistant

## LEADERSHIP ROLES

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### Startup – GoGet [\[link\]](#)

*Taipei, Taiwan*

*Co-Founder & Web developer*

*11/2019 – Present*

- Founded with workers from McKinsey, BCG, Shopee, and Microsoft
- An online platform for college students and startup companies to find expertise to deal with their current project problems and find partners, and 1000+ users per week, still increasing
- Cooperated with Microsoft Taiwan to promote programming courses for interdisciplinary learning

### NTUEE Badminton Team

*Taipei, Taiwan*

*Captain*

*05/2018 – 05/2019*

- Managed the whole team with nearly 70 people and won the 2018 North Taiwan EE Cup Champion

### NTUEE Camp

*Taipei, Taiwan*

*Leader of the event planning department*

*08/2017*

- Organized the whole activities with 100 +workers; activities included visiting Google and NVIDIA headquarters

### Sea Group and Garena World Overseas Visit Program

*Singapore and Thailand*

*Delegate*

*09/2019*

- Selected as one of the 20 representatives of Taoyuan City from 1000+ candidates.
- Visited 7 startup companies; learned and exchanged ideas from CTO in Sea Group Singapore and PM in Garena Thailand.

## SELECTED PROJECTS

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### Automatic Musical Note Player on FPGA | *Digital Circuit Lab (EE3016)* [\[link\]](#)

- Designed an automatic music player in System Verilog on FPGA, which integrated image and audio processing to identify musical notes
- Integrated FPGA peripheral modules, such as Arduino joystick and VGA image display and TRDB-D5M camera.

### Distributed Training on Multi-GPUs Platform | *Independent project*

- Integrated GPipe’s pipeline using PipeDram’s algorithm for training process of ResNet and AlexNet
- Increased the largest training throughput by 133% on 8 GPUs

### Pipelined MIPS CPU | *Digital System Design (EE4010)* [\[link\]](#)

- Implemented 5-stage pipelined MIPS with branch prediction, layer-2 cache, and multiplier & divider unit
- Ranked 1<sup>st</sup> place in terms of area and timing in final project

## SKILLS

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**Programming Languages:** Python, C++, Verilog/System Verilog, Matlab, Assembly | **ISAs:** RISC-V, MIPS, Arm

**VLSI Design Tools:** NC-Verilog, Design Compiler, Innovus, Verdi, Virtuoso | **ML Frameworks:** PyTorch, Keras, TensorFlow