Tsang-Yung Wu

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OBJECTIVES

To explore myself in practical projects of world-leading industries., via over 2 months co-op/internship opportunity. To expand full potential of my versatile personalities and contribute my engineering skills in VLSI and Computer Architecture hardware design to industrial projects.

EDUCATION

National Taiwan University *Sep 2015 - Present*
Bachelor of Science in Electrical Engineering *Taipei, Taiwan*
Expected Graduation June 2019
GPA : Overall 3.84 / 4.0, **Major 3.97 / 4.0**

AWARDS

Second Place in Arm Design Contest (Cash Prize 3300 USD) *Nov 2018*
Sign Language Translation System, Prof. Chia-Hsiang Yang *Taiwan*

- Awarded with 2nd & Best Popularity award **among 50+ teams.**
- Developed gesture recognition algorithm on Arm embedded system using **only one 9-DOF IMU** to achieve real-time sign language translation.

Second Place in Undergraduate Innovation Award *Sep 2018*
LED Controller Chip, Prof. Tzi-Dar Chiueh *Dept. of Electrical Eng., NTU*

- Designed a programmable LED cubic displayer that integrated electronic materials with FPGA prototyping to showcase real-world visual effect.
- Tapped out a **controller ASIC** based on above FPGA design to be familiarized with Design Compiler and Innovus.

WORK EXPERIENCES

Hardware Engineering Co-op *Mar 2018 - Jan 2019*
Intel Inc., Managers: Jackie Wang and Tommy Li *Taipei, Taiwan*

- Automated circuit simulation reports generation process using hands-on Python framework to improve team efficiency **by 50 %**.
- Co-designed a schematic verification tool and standardized circuit net-list format to reduce effort on **chip debugging for clients' wireless product**.
- Managed parcel database and reduced parcel arrival latency **from 2 days to 1 day** by establishing a parcel auto-tracking system.

RESEARCH EXPERIENCES

SHA256-Efficient RISC-V CPU Design *Jul 2018 - Dec 2018*
Micro-System Laboratory, Prof. Tzi-Dar Chiueh *Dept. of Electrical Eng., NTU*

- Developed and designed enhanced RISC-V CPU to accelerate SHA256 operation used in current Blockchain application.
- Leveraged Chisel framework and RISC-V ISA to reduce CPU design cost with emulation results outperforming original RISC-V and x86 ISA **by 13%**.

Text-Based Machine Learning Multi-Labeling *Feb 2018 - Nov 2018*
Speech Processing Laboratory, Prof. Lin-Shan Lee *Dept. of Electrical Eng., NTU*

- Developed and designed a novel BERT-revised ML modeling with accuracy outperforming current RNN modeling **by 10%** on the text-based emotional multi-labeling to explore text emotion distribution.

TEACHING EXPERIENCES

Electrical Engineering Cornerstone Education *Sep 2017 - Jul 2018*
Lab Assistant *Dept. of Electrical Eng., NTU*

- Cultivated practical project experiences on **80+** freshman students by designing and executing lab teaching materials in person.
- Refined teaching materials by analyzing students feedback to further course implementation.

Signals and System *Feb 2018 - Jul 2018*
Teaching Assistant *Dept. of Electrical Eng., NTU*

- Assisted Prof. Lin-Shan Lee and helped **100+** sophomore students understand lecture materials by answering course questions.

SELECTED PROJECTS

EL-Wire Controlled Suits *Aug 2018*
NTU-EE Camp *Taipei, Taiwan*

- Leveraged engineering feats on practical projects by integrating electroluminescent-wire with Linkit embedded system in dancing performance.

CNN FPGA Accelerator *Jul 2018*
Digital Circuit Lab, Prof. Chia-Hsiang Yang *Dept. of Electrical Eng., NTU*

- Developed and designed CNN modeling **from RTL Verilog design to FPGA verification** to achieve real-time execution on speech recognition.

Suits Recommendation System *Apr 2018*
MakeNTU Hackthon *Taipei, Taiwan*

- Integrated speech and image recognition into RPI embedded system to improve experiences on choosing suits based on user's intentions.

TECHNICAL STRENGTHS

VLSI Technologies
NC-Verilog, Design Compiler, Innovus, Quartus II, Gem5, FPGA Prototyping, Embedded System Prototyping
Programming Languages
Verilog, C/C++, Python, Chisel(Scala) Assembly
English Abilities
TOFEL : 107/120 (Writing 28/30)
GRE : 327/340 (Verbal 157/170, Quantitative 170/170)

SELECTED COURSEWORK

VLSI Related
CMOS VLSI Design (A+)
Computer Architecture (A+)
Integrated Circuits Design Lab (A+)
Digital Circuit Lab (A+)
Computer-Aided VLSI System Design (A+)

EXTRA-CURRICULAR ACTIVITIES

Globe Leadership Organization Conference, *Attendee* Dec 2018
NTUEE-Camp, *Dancing Director* Aug 2018
Campus Proms for 350+ Students from 8 Departments, *Chief Director* Dec 2017

COMMUNITY SERVICE

After-school Tutor for Underprivileged Children *Sep 2016 - Jan 2017*