TSANG-YUNG (ERIC) WU

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EDUCATION

University of California, Berkeley — Berkeley, CA
M.Eng. in Electrical Engineering and Computer Science — *Aug. 2020 - May 2021 (Expected)*

- **Coursework:** Digital Integrated Circuits Design (ASIC Lab, EECS 151/251), Embedded System
- **Capstone Project:** TBD

National Taiwan University (NTU) — Taipei, Taiwan
B.S. in Electrical Engineering (GPA 3.98/4.00) — *Sep. 2015 - June 2019*

- **Coursework:** Digital Integrated Circuits Design, Computer-Aided VLSI Digital Systems Design, ASIC Lab, FPGA Lab, Computer Architecture, Graduate Computer Architecture, Electronics

SUMMARY OF QUALIFICATION

Hardware Design Tools NC-Verilog, VCS, Design Compiler, Innovus, Virtuoso, Quartus II, Gem5
Programming Tools C/C++, Python, Verilog, Assembly, Chisel, Matlab, Shell, Tcl, Vim Editor

WORK EXPERIENCE

MediaTek Inc. (MTK) — Singapore
Digital IC Design Intern | High-Performance Computing Team — *July 2019 - Oct. 2019*

- Pioneered research of ADB400-BIST (asynchronous bridge testing modules) in ARM CORTEX-A53 using *Verdi*.
- Constructed **ADB400-BIST Document** explaining architecture and data flow, and educated **7 CPU engineers**.
- Developed script to reduce RTL sign-off errors of ARM CORTEX-A53 **by 90%** using *Python* and *CAD tools*.

National Taiwan University — Taipei, Taiwan
Teaching Assistant | RISC-V Course Development advised by *Prof. An-Yeu (Andy) Wu* — *Apr. 2019 - July 2019*

- Collaborated with NTUST to design RISC-V Architecture, Simulator, Software and Implementation courses, implemented in Digital System Design/ Computer Architecture classes in NTU/NTUST.
- Sponsored by Ministry of Education in Taiwan with **TWD$2.5M.**

Intel Corp. — Taipei, Taiwan
Hardware Validation Intern | Wireless-Design Verification Team — *Mar. 2018 - Feb. 2019*

- Developed circuit-schematic tracing tool to locate improper pin connections between Wifi chip and CPU.
- Facilitated circuit validation process by generating the simulation reports automatically using *Python*.
- Improved Wifi chips' validation process efficiency with two tools **by 50%**.

PROJECT EXPERIENCE

Hybrid Cache in Multi-Core, 2GHz System — Taipei, Taiwan
Research Assistant advised by *Dr. Shih-Lien Lu*, Director, TSMC — *Apr. 2019 - Oct. 2019*

- Designed new cache replacement policy, NMRU, to allow efficient data allocation within L3 hybrid cache, which consisted of slower but cheaper XRAM with SRAM.
- Developed CPU simulator based on ZSim to model NMRU replacement policy data allocation mechanism.
- Achieved **1.2% better** IPC compared with normal cache with baseline LRU replacement policy in multi-core CPU.

32x16 16-Bit Image Displayer ASIC — Taipei, Taiwan
Computer-Aided VLSI System Design Class taught by *Prof. Chia-Hsiang Yang*, Dept. of EE, NTU — *Oct. 2018 - Dec. 2018*

- Constructed Image Displayer ASIC integrated with SRAM using *Verilog* and synthesized by *Design Compiler*.
- Drew schematic/layout using *Innovus* to achieve post-layout simulation.
- Accomplished the **second-best** design in Area/Timing performance out of 54 groups.

32-bit SHA256-Efficient RISC-V CPU — Taipei, Taiwan
Undergraduate Research Student advised by *Prof. Tzi-Dar Chiueh*, Dept. EE, NTU — *July. 2018 - Dec. 2018*

- Devised new instruction to accelerate SHA256 operations in RISC-V ISA using *Chisel* and *riscv-toolchain*.
- Outperformed baseline RISC-V and x86 ISA on IPC **by 13%** on *Gem5* emulation and *NC-Verilog* simulation.

AWARD

2019: **First Place in Synopsys ARC AIoT Design Contest [**link**]** — Taipei, Taiwan

2018: **Second Place in ARM Design Contest [**link**]** — Taipei, Taiwan

2018: **Second Place in Undergraduate Innovation Award [**link**]** — Taipei, Taiwan
*50MHz LED-Cube-Controller ASIC (*Taped-out-and-Tested ASIC using *Innovus*, *Virtuoso*)

EXTRACURRICULAR EXPERIENCE

2017: **President, NTU Student Prom** — Taipei, Taiwan

2016: **Dancer, NTU Pedestrian Dancing Club** — Taipei, Taiwan