TSANG-YUNG (ERIC) WU

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EDUCATION

University of California, Berkeley — Berkeley, CA
M.Eng. in EECS (Expected Graduation: May 2021) — *Aug. 2020 - Present*

- **Coursework:** Digital Integrated Circuits Design (ASIC Lab, EECS 151/251); Introduction to Embedded System
- **Leadership Training:** R&D Technology Management & Ethics; Communications for Engineering Leaders

National Taiwan University (NTU) — Taipei, Taiwan
B.S. in EE (CGPA 3.87/4.00; MGPA 3.98/4.00) — *Sep. 2015 - June 2019*

- **Coursework:** IC Design (A+); Computer-Aided VLSI System Design (A+); IC Design Lab (A+); Digital Circuits Lab (A+); Computer Architecture (A); Advanced Computer Architecture (A)
- **Teaching/Leadership:** TA of **RISC-V** (Pioneered RISC-V courses in Taiwan); President of NTU Campus Prom

SKILL

Circuit Design Technology Verilog; Design Compiler; Innovus; Verdi; Virtuoso; Altera Quartus II; Qsys; PSpice
Programming Technology C/C++; Python; Assembly; Chisel; Matlab; Vim

WORK EXPERIENCE

MediaTek Inc. (MTK) — Singapore
Digital IC Design Intern | High-Performance Computing Team — *July 2019 - Oct. 2019*

- Pioneered research of ADB400-BIST (asynchronous bridge testing modules) in ARM CORTEXA-53 using *Verdi*.
- Constructed **ADB400-BIST Document (20+ pages)** to explain architecture design and workflow within ARM CORTEXA-53.
- Held session to educate 7 CPU engineers on ADB400-BIST to advance team's project schedule **for 3 days**.
- Developed script to reduce RTL sign-off errors of ARM CORTEXA-53 **by 90%** using *Python* and *CAD tools*.

Intel Corp. — Taipei, Taiwan
Hardware Validation Intern | Wireless-Design Verification Team — *Mar. 2018 - Feb. 2019*

- Developed circuit-schematic verification tool to locate improper pin connections between Wifi chips and CPUs using depth first search algorithm.
- Initiated and developed automatic circuit-simulation-report generator to export Wifi chips' frequency response results from *ANSYS* into *Python* program automatically.
- Accelerated Wifi validation process with two tools **by 50%**.

PROJECT EXPERIENCE

Hybrid Cache in Multi-Core, 2GHz System — Taipei, Taiwan
Research Assistant advised by *Dr. Shih-Lien Lu*, Director, TSMC — *Apr. 2019 - Oct. 2019*

- Developed large L3 Hybrid Cache in 4,8,16-core CPU by integrating SRAM with XRAM (developed by TSMC) in ZSim (based on Intel Pin) to reduce production cost.
- Achieved **1.2% better** IPC on 4-core CPU, 16MB L3 Hybrid Cache system with self-design cache replacement policy, NMRU.

32x16 16-Bit Image Displayer ASIC — Taipei, Taiwan
Computer-Aided VLSI System Design Class taught by *Prof. Chia-Hsiang Yang*, Dept. of EE, NTU — *Oct. 2018 - Dec. 2018*

- Constructed Image Displayer ASIC integrated with SRAM using *Verilog*.
- Drew schematic/layout using *Design Compiler* and *Innovus* and achieved post-layout simulation.
- Achieved the **second-best** designs in Area/Timing performance out of 54 groups.

32-bit SHA256-Efficient RISC-V CPU — Taipei, Taiwan
Undergraduate Research Student advised by *Prof. Tzi-Dar Chiueh*, Dept. EE, NTU — *July. 2018 - Dec. 2018*

- Devised new instruction to accelerate SHA256 operations in RISC-V ISA using *Chisel*, *Gem5*, *Spike* and *riscv-toolchain*.
- Outperformed original RISC-V and x86 ISA on IPC **by 13%** on software emulation and Verilog simulation.

AWARD

Image-Segmentation using ResNet on ARC Embedded System [link] — Taipei, Taiwan
First Place in 2019 Synopsys ARC AIoT Design Contest — *Aug. 2019*

Sign Language Machine Recognition System on ARM Embedded System [link] — Taipei, Taiwan
Second Place in 2018 ARM Design Contest — *Oct. 2018*

50MHz LED-Cube-Controller ASIC (*Taped out using *Innovus* and *Virtuoso*) [link] — Taipei, Taiwan
Second Place in 2018 Undergraduate Innovation Award — *Aug. 2018*