TSANG-YUNG WU

Taichung, Taiwan +886 909 257 525 ericty.us13@gmail.com ericwu13.github.io

INTERESTS & ACHIEVEMENTS

Interests AIoT Computing; Application-Specific Computer Architecture/ASIC Design; Embedded Systems Design

2019 1st Place at Synopsys ARC AIoT Design Contest (Against **136** teams from China, Taiwan, India and Vietnam)

2018 2nd at Arm Design Contest (Against **130** teams from Taiwan, the only pure-undergraduate team to win)

2018 2nd at Undergraduate Innovation Award (Against **300** projects from Dept. EE at NTU)

EDUCATION

National Taiwan University (NTU)
Taipei, Taiwan

Bachelor of Science in Electrical Engineering (CGPA 3.87/4.00; MGPA 3.98/4.00) *Sep. 2015 - June 2019*

- **Honors:** Outstanding Performance Scholarship (15 out of 7,000 NTU students); Dean's List Award (**1**/243 in NTUEE)
- **EE Coursework:** IC Design; Computer-Aided VLSI System Design; IC Design Lab; Digital Circuits Lab
- **CS/AI Coursework:** Data Structure and Programming; Introduction to Computer Networks; Computer Architecture; Advanced Computer Architecture; Machine Learning
- **Teaching/Leadership:** TA of **RISC-V**/Cornerstone EE Education/Signals and Systems; President of Campus Prom

WORK EXPERIENCES

MediaTek Incorporation (MTK)
Singapore

Computer Engineer Intern, CAI1/High-Performance Computing *July 2019 - Oct. 2019*

- Researched architecture of Arm CORTEXA-53 with 3 CPU engineers using Verdi; guided MTK in-house features in Arm's ADB400 asynchronous bridge for **7 CPU engineers**.
- Developed script to reduce errors of Arm CORTEXA-53 RTL sign-off **by 90%** using Python and CAD tools.

Intel Corporation
Taipei, Taiwan

Hardware Engineer Intern, Wireless Design Team *Mar. 2018 - Feb. 2019*

- Developed automatic circuit-simulation report generator and circuit-schematic verification tool to reduce chip-debugging process for 3 hardware engineers **by up to 50%** with Python and ANSYS.
- Reduced 1 working day for each parcel in Custom Clearance by parcel tracking system using Python and MySQL.

RESEARCH EXPERIENCES

Independent Research
Taipei, Taiwan

Research Assistant (Advisor: Dr. Shih-Lien Lu, Director, TSMC) *Mar. 2019 - Present*

- Developing L3 Hybrid Cache using ZSim (based on Intel Pin) by integrating SRAM with XRAM (developed by TSMC) to reduce production cost
- Designing new replacement policy, NMRU, to provide better Instruction Per Cycle while using 3 times slower XRAM.

MicroSystem Research Lab NTU
Taipei, Taiwan

Undergraduate Research Student (Advisor: Prof. Tzi-Dar Chiueh, Dept. EE, NTU) *July. 2018 - Dec. 2018*

- **RISC-V ISA : ** Devised new instruction for enhanced RISC-V CPU to accelerate SHA256 operations by Chisel and riscv-tools; outperformed original RISC-V and x86 ISA on Instruction Per Cycle **by 13%**.
- **ASIC Controller:** Taped Choreographed ASIC using NC-Verilog, Design Compiler, Innovus and Virtuoso with UMC flow and won 2nd in Undergraduate Innovation Award.

Speech Processing Lab NTU
Taipei, Taiwan

Undergraduate Research Student (Advisor: Prof. Lin-Shan Lee, Dept., EE, NTU) *Feb. 2018 - Dec. 2018*

- Improved Text-Sentiment Multi-Labeling BERT model with TensorFlow and PyTorch; fine-tuned models on 60,000+ sentences with accuracy outperforming RNN modeling **by 10%**.

TECHNICAL & SIDE PROJECTS

Distributed Training on Multi-GPUs Platform
Advanced Computer Architecture (CSIE 5059)

- Integrated GPipe's pipeline with PipeDram's partitioning algorithm using C++ and Python for large ML models' (ResNet, VGG19 and AlexNet) training to increase training throughput **by up to 133%** on 8 GPUs.

Electroluminescent (EL)-Wire Lighting Suits
NTUEE High-School Student Camp

- Choreographed and integrated electronics dancing performance with EL-wire by Linkit Embedded Board.

CNN Accelerator on FPGA
Digital Circuits Lab (EE 3016)

- Implemented CNN accelerator for speech recognition using Quartus II and Altera DE2-115 FPGA.