TSANG-YUNG WU

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Interests: AIoT Computing | Application-Specific Computer Architecture/ASIC Design | Embedded Systems Design

ACHIEVEMENTS

DETAILS IN PERSONAL WEBSITE

2019 **1st** at Synopsys ARC AIoT Design Contest (Against **136** teams from China, Taiwan, India and Vietnam)
2018 **2nd** at Arm Design Contest (Against **130** teams from Taiwan, the only pure-undergraduate team to win)
2018 **2nd** at Undergraduate Innovation Award (Against **150+** projects from Dept. EE at NTU)
2018 **Open-Source Project:** Electroluminescence-Wire Dancing Performance attracting **350+** students in school

EDUCATION

National Taiwan University (NTU) — Taipei, Taiwan
Bachelor of Science in Electrical Engineering (CGPA 3.87/4.00; MGPA 3.98/4.00) — *Sep. 2015 - June 2019*

- **Honors:** Outstanding Performance Scholarship (15 out of 7,000+ NTU students); Dean's List Award (**1**/243 in NTU EE)
- **EE Coursework:** IC Design (A+); Computer-Aided VLSI System Design (A+); IC Design Lab (A+); Digital Circuits Lab (A+)
- **CS/AI Coursework:** Data Structure and Programming (A+); Intro to Computer Networks (A+); Computer Architecture (A+); Advanced Computer Architecture (A); Machine Learning (A)
- **Teaching/Leadership:** TA of **RISC-V** (Pioneered RISC-V courses for 3 EECS Prof.); President of NTU Campus Prom

WORK EXPERIENCES

MediaTek Inc. (MTK) — Singapore
Computer Engineer Intern | High-Performance Computing Team — *July 2019 - Oct. 2019*

- Pioneered research of MTK-inhouse ADB400 asynchronous bridge in Arm CORTEXA-53 using Verdi to publish **20+ pages** technical document for 7 CPU engineers.
- Developed script to reduce RTL sign-off errors of Arm CORTEXA-53 **by 90%** using Python and CAD tools.

Intel Corp. — Taipei, Taiwan
Hardware Engineer Intern | Wireless-Design Verification Team — *Mar. 2018 - Feb. 2019*

- Developed automatic circuit-simulation-report generator and circuit-schematic verification tool to accelerate chip-debugging process for 3 hardware engineers **by 50%** with Python and ANSYS.
- Reduced **1** working day for each parcel in Custom Clearance by parcel tracking system using Python and MySQL.

RESEARCH EXPERIENCES

DETAILS IN PERSONAL WEBSITE

Independent Research — Taipei, Taiwan
Research Assistant | Advisor: *Dr. Shih-Lien Lu*, Director, TSMC — *Mar. 2019 - Present*

- **Hybrid Cache**: Developing large L3 Hybrid Cache in multi-core CPU by integrating SRAM with XRAM (developed by TSMC) in ZSim (based on Intel Pin) to reduce production cost
- Designing new cache replacement policy, NMRU, to provide **2% better** IPC while using 3x slower XRAM.

NTU MicroSystem Research Lab — Taipei, Taiwan
Undergraduate Research Student | Advisor: *Prof. Tzi-Dar Chiueh*, Dept. EE, NTU — *July. 2018 - Dec. 2018*

- **RISC-V CPU: ** Devised a new instruction to accelerate SHA256 operations in RISC-V ISA by Chisel, Gem5, Spike and riscv-tools; outperformed original RISC-V and x86 ISA on Instruction Per Cycle **by 13%**.
- **ASIC Controller:** Taped out ASIC using NC-Verilog, Design Compiler, Innovus and Virtuoso with UMC flow and **won 2nd** in Undergraduate Innovation Award.

NTU Speech Processing Lab — Taipei, Taiwan
Undergraduate Research Student | Advisor: *Prof. Lin-Shan Lee*, Dept. EE, NTU — *Feb. 2018 - Dec. 2018*

- **Text-Sentiment Multi-Labeling: ** Improved BERT model with proposed classifier using TensorFlow and PyTorch; fine-tuned models on 60,000+ sentences with accuracy outperforming RNN modeling **by 10%**.

TECHNICAL PROJECTS

DETAILS IN PERSONAL WEBSITE

Distributed Training on Multi-GPUs Platform — Advanced Computer Architecture (CSIE 5059)

- Integrated GPipe's pipeline with PipeDram's partitioning algorithm using C++ and Python for large ML models' (ResNet, VGG19 and AlexNet) training to increase the largest training throughput **by 133% on 8 GPUs**.

CNN Accelerator on FPGA — Digital Circuits Lab (EE 3016)

- Implemented CNN accelerator for speech recognition using Verilog, C++, Quartus II and Altera DE2-115 FPGA.

SKILLS

Programming Languages: C/C++; Python; (System) Verilog; Assembly; Chisel | **ISAs:** RISC-V; MIPS; Arm; ARC
ML Frameworks: TensorFlow; PyTorch; Keras | **VLSI Tools:** NC-Verilog; Design Compiler; Innovus; Verdi; Virtuoso