TSANG-YUNG (ERIC) WU

Berkeley, CA | (341) 333-8211 | tywu13@berkeley.edu | LinkedIn | Personal Website

OBJECTIVE

Experienced in electrical engineering and ASIC/Computer Architecture Design, once taped out a chip in 2018. Seeking for a full-time job in 2021, with an emphasis on SoC/CPU Design.

EDUCATION

University of California, Berkeley — Berkeley, CA
M.Eng. in Electrical Engineering and Computer Science — *Aug. 2020 - May 2021*

- **Coursework:** Digital Integrated Circuits Design (ASIC Lab), Embedded Systems.

National Taiwan University (NTU) — Taipei, Taiwan
B.S. in Electrical Engineering (GPA 3.98/4.00) — *Sep. 2015 - Jun. 2019*

- **Coursework:** Digital Integrated Circuits Design, Computer-Aided VLSI Systems Design, ASIC Lab, FPGA Lab, Computer Architecture, Advanced Computer Architecture, Electronics.

WORK EXPERIENCE

MediaTek Inc. — Singapore
Digital IC Design Intern | High-Performance Computing Team — *July 2019 - Oct. 2019*

- Pioneered research of ADB400-BIST (asynchronous bridge testing modules) in the CPU using *Verdi*.
- Documented ADB400-BIST architecture and data flow and trained **7 CPU** engineers.
- Reduced errors in CPU **by 90%** by developing RTL sign-off checker using *Python* and *Synopsys SpyGlass*.

National Taiwan University — Taipei, Taiwan
Teaching Assistant | RISC-V Course Development advised by Prof. An-Yeu (Andy) Wu — *Apr. 2019 - Jul. 2019*

- Pioneered courses on RISC-V architecture, simulation, and usage in collaboration with NTUST (best VOC college in TW).
- Administered a team of three undergraduate students to break down RISC-V Simulator Software workflow for lab design.
- Won a **US$85,000** grant sponsored by the Ministry of Education.

Intel Corp. — Taipei, Taiwan
Hardware Validation Intern | Wireless Design Validation Team — *Mar. 2018 - Feb. 2019*

- Developed a circuit-schematic tracing tool in *Python* to detect disconnected ports between the WiFi chip and the CPU.
- Facilitated the circuit validation process by automating the generation of simulation reports using *Python*.
- Improved the time efficiency of the WiFi chip validation process **by 50%**.

PROJECT EXPERIENCE

Hybrid Cache in Multi-Core, 2GHz System — Taipei, Taiwan
Research Assistant advised by Dr. Shih-Lien Lu, Director, TSMC — *Apr. 2019 - Oct. 2019*

- Designed a new cache replacement policy to allow efficient data allocation within an L3 hybrid cache.
- Developed a CPU simulator based on ZSim in C++ to model the new replacement policy's data allocation mechanism.
- Improved IPC by **1.2%** compared to a normal cache using a baseline LRU replacement policy in a multi-core CPU.

32x16 16-Bit Image Displayer ASIC — Taipei, Taiwan
Computer-Aided VLSI System Design Class taught by Prof. Chia-Hsiang Yang, Dept. of EE, NTU — *Oct. 2018 - Dec. 2018*

- Constructed an Image Displayer ASIC integrated with SRAM in *Verilog* and synthesized using *Design Compiler*.
- Drew schematics/layouts in *Innovus* to achieve post-layout simulation.
- Awarded the **second-best** design in Area/Timing performance out of 54 groups.

32-bit SHA256-Efficient RISC-V CPU — Taipei, Taiwan
Undergraduate Research Student advised by Prof. Tzi-Dar Chiueh, Dept. EE, NTU — *Jul. 2018 - Dec. 2018*

- Devised a new instruction to accelerate SHA256 operations in RISC-V ISA implemented in *Chisel* and *riscv-toolchain*.
- Outperformed baseline IPC on RISC-V and x86 ISA by **13%** tested by *Gem5* emulation and *NC-Verilog* simulation.

AWARDS

First Place in Synopsys ARC AIoT Design Contest [link] (out of 136 teams from Asia) — *Aug. 2019*

Second Place in ARM Design Contest [link] (out of 130 teams from Taiwan) — *Oct. 2018*

Second Place in Undergraduate Innovation Award [link] (out of 150 projects from Dept. EE at NTU) — *Aug. 2018*
*50MHz LED-Cube-Controller ASIC (*Taped-out-and-Tested ASIC using *Innovus*, *Virtuoso*)

SKILLS

Circuit Design NC-Verilog, VCS, Design Compiler, Innovus, Virtuoso, Quartus II, Gem5, Synopsys SpyGlass (lint, CDC)
Programming C++ (OOP), Python, Verilog, Assembly, Chisel, Matlab, Shell, Tcl, Vim Editor