Luna Kim

Vancouver, Canada

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Education

University of British Columbia

Bachelor of Science in Computer Engineering

Sep 2018 – May 2022 | Vancouver, Canada

GPA: 3.9/4.0

Activities: IEEE Chapter Chair, Robotics Team Lead, Peer Tutor

Relevant Coursework: Embedded Systems, VLSI, FPGA, Robotics

Summer School: UC Berkeley 2021 (GPA: 3.9/4.0)

Work Experience

Hardware Design Engineer | AMD | Jun 2022 - Present | Santa Clara, CA, USA

- Designed RTL in Verilog for GPU datapath.

- Collaborated on ASIC verification with UVM.

- Optimized synthesis scripts for timing closure.

Skills

Languages: Verilog, VHDL, SystemVerilog

Tools: Synopsys, Cadence, ModelSim

Other: FPGA Design, Timing Analysis, RTL Verification

Certificates

Cadence Certified Digital IC Designer

Udemy: FPGA Development

Coursera: Hardware Design

Awards

AMD Innovation Award 2023

UBC Engineering Scholarship

First Place – North America FPGA Challenge