EASWARI ENGINEERING COLLEGE, CHENNAI-600 089 DEPARTMENT OF MECHANICAL ENGINEERING LESSON PLAN

SUBJECT CODE : CS 6201

SUBJECT TITLE : Digital Principles and System Design

HOURS DISTRIBUTION : (L T P C 3 0 0 3)

COURSE/ BRANCH : B.Tech (IT)

SEMESTER : II

ACADEMIC YEAR : 2014 - 2015

FACULTY NAME : L.BHAGYALAKSHMI / S.DEEPA

OBJECTIVE OF COURSE :

To learn how to design digital circuits

To learn how to simplify Boolean functions

To give an idea about designs using PLDs

To write codes for designing larger digital systems

OUTCOME OF COURSE :

At the end of this course, the student will be able to:

- · Perform arithmetic operations in any number system.
- · Simplify the Boolean expression using K-Map and Tabulation techniques.
- · Use boolean simplification techniques to design a combinational hardware circuit.
- · Design and Analysis of a given digital circuit combinational and

sequential.

PREREQUISTE

: To have knowledge in Number System with base 2, 8,16.

| S.No | Торіс | No. of Periods | Reference books | Page Nos |
|------|--|-------------------|--------------------|------------------------------|
| UNIT | BOOLEAN ALGEBRA AND LOGIC | GATES 9 | | |
| | Objective: To learn the concepts of | of Boolean Al | gebra and Logi | ic gates |
| 1 | Review of Binary Number Systems | 1 | T1 | 3 - 13 |
| 2 | Arithmetic Operations | 1 | T1 | 15 - 16 |
| 3 | Binary Codes | 1 | T1 | 17 - 22 |
| 4 | Boolean Algebra and Theorems | 1 | T1 | 34 - 41 |
| 5 | Boolean Functions | 1 | T1 | 42 - 46 |
| 6 | Simplifications of Boolean Functions using Karnaugh Map and Tabulation Methods | 2 | T1 | 46 - 53, 70 - 74, 84 - 87 |
| 7 | Logic gates | 1 | T1 | 57 - 60 |
| 8 | NAND and NOR Implementations | 1 | T1 | 87 - 94 |

OUTCOME: At the end of this unit, the student should understand arithmetic operations, simply Boolean expresions using K map and Tabulation techniques

UNIT II COMBINATIONAL LOGIC 9

Objective: To learn the concepts of Combinational circuits which includes adders, subtractors, multiplier, comparator and to learn the concepts of decoders, encoders, multiplexers and demultiplexers

| 9 | Combinational Circuits, Analysis and Design Procedure | 1 | T1 | 135 - 140 |
|----|---|---|----|-----------|
| 10 | Circuits for Arithmetic Operations | 2 | T1 | 143 - 161 |
| 11 | Code Conversion | 1 | T1 | 140 - 142 |

| 12 | Decoders | 1 | T1 | 162 - 165 |
|----|--|---|------------------|-----------|
| 13 | Encoders | 1 | T1 | 166 - 168 |
| 14 | Multiplexers | 1 | T1 | 168 - 174 |
| 15 | Demultiplexers | 1 | Internet (URL 1) | |
| 16 | Introduction to HDL, HDL Models for Combinational Circuits | 1 | T1 | 174 - 184 |

OUT COME: At the end of this unit, the student should be able to the basic concept of combination circuits with different applications

UNIT III SYNCHRONOUS SEQUENTIAL LOGIC 9

Objective: To learn the concepts of sequential logic which includes flip-flops, registers and counters. Sequential Circuits 1 T1 197 - 203 T1

| 18 | Latches and Flip Flops | 1 | | 203 - 210 |
|----|--------------------------------------|---|----|-------------------------|
| 19 | Analysis and Design Procedures | 1 | T1 | 210 - 221, 238 - 246 |
| 20 | State Reduction and State Assignment | 1 | T1 | 233 - 238 |

Registers and Counters

18

| 21 | Shift Registers | 2 | 11 | 255 - 267 |
|----|-----------------------------------|---|----|-----------|
| 22 | Counters | 2 | T1 | 268 - 293 |
| 23 | HDL for Sequential Logic Circuits | 1 | T1 | 293 - 298 |

OUT COME: At the end of this unit, the student should be able to the basic concept of Synchronous Sequential circuits with different applications like register and counter.

UNIT IV ASYNCHRONOUS SEQUENTIAL LOGIC 9

Objective: To learn the concepts of asynchronous sequential logic. Analysis and Design of Asynchronous Sequential Circuits 2 437 - 457

| 25 | Reduction of State and Flow Tables | 3 | T1 | 457 - 464 |
|----|------------------------------------|---|----|-----------|
| 26 | Race-Free State Assignment | 2 | T1 | 464 - 469 |
| 27 | Hazards | 2 | T1 | 469 - 474 |

OUT COME: At the end of this unit, the student should be able to the basic concept of ASynchronous Sequential circuits

UNIT V MEMORY AND PROGRAMMABLE LOGIC 9

Objective: To learn the concepts of memory and programmable devices

| 20 | | | - | 308 - 314, |
|----|--------------------------------|---|----|------------|
| 28 | RAM and ROM | 2 | | 322 - 325 |
| 29 | Memory Decoding | 1 | T1 | 314 - 319 |
| 30 | Error Detection and Correction | 1 | T1 | 319 - 322 |
| 31 | Programmable Logic Array | 1 | T1 | 328 - 332 |

| 32 | Programmable Array Logic | 1 | T1 | 332 - 336 |
|----|--|---|----------|-----------|
| 33 | Sequential Programmable Devices | 2 | T1 | 336 - 351 |
| 34 | Application Specific Integrated Cicruits | 1 | Handouts | |

OUT COME: At the end of this unit, the student should be able to the basic concept of Memory and it array applications

| SL.NO | ASSIGNMENT TOPICS | SUBMISSION DUE |
|-------|------------------------------|----------------|
| 1 | ASSIGNMENT PROBLEM SHEET I | Jan 30 2015 |
| 2 | ASSIGNMENT PROBLEM SHEET II | March 2 2015 |
| 3 | ASSIGNMENT PROBLEM SHEET III | April 1 2015 |

| | CONTENT BEYOND SYLLABUS | | | | | | | | |
|---|---|--|--|--|--|--|--|--|--|
| 1 | Solving Boolean Functions using K-Map and Tabulation Methods including Don't Care Conditions. | | | | | | | | |
| 2 | Parity Generator and Parity Checker | | | | | | | | |

TEXT BOOK

1. M.Morris Mano and Michael D. Ciletti, "Digital Design", 4th edition, Pearson Education, 2008.

REFERENCES

- 1. John F. Wakerly, "Digital Design Principles and Practices", Fourth Edition, Pearson Education, 2007.
- 2. Charles H. Roth Jr, "Fundamentals of Logic Design", Fifth Edition Jaico Publishing House, Mumbai, 2003.
- 3. Donald D. Givone, "Digital Principles and Design", Tata Mcgraw Hill, 2003.
- 4. Kharate G. K., "Digital Electronics", Oxford University Press, 2010.

URL

1. http://www.wisc-online.com/objects/ViewObject.aspx?ID=DIG5704

HOD FACULTY

Program Educational Outcomes

1. Graduates will be proficient in utilizing the fundamental knowledge of basic sciences and mathematics to the applications relevant to various streams of Engineering and Technology.

| UNITS | | | | | | | _ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|-------|----------------|---|----|--------|----|----|--------|---|---|---|---|---|---|----|---|---|---|---|----|
| | Course outcome | В | ОВ | U B | OB | OB | U B | С | С | С | С | С | С | Cg | С | С | С | С | CI |
| | course outcome | 1 | 2 | 3 | 4 | 5 | 6 | а | b | С | d | е | f | | h | i | j | k | |
| | | | | | | | | | | | | | | | | | | | |

- Graduates will possess core competencies necessary for application of knowledge of computers and telecommunications equipment to store, retrieve, transmit, manipulate and analyze data in the context of business enterprise.
- 3. Graduates will be capable of thinking logically, pursue lifelong learning and will have the capacity to understand technical issues related to computing systems and design optimal solutions.
- 4. Graduates will be able to develop hardware and software systems by understanding the importance of social, business and environmental needs in the human context.
- Graduates will gain employment in organizations and establish themselves as professionals by applying their technical skills to solve real world problems and meet the diversified needs of industry, academia and research.
- Graduates will be aware of professional ethics of the software industry and equip themselves with communication skills essential for working in community.

Program Outcomes

- (a) Ability to apply knowledge of computing and mathematics appropriate to Information Technology
- (b) Ability to analyze a problem, and identify computing requirements appropriate to its solution
- (c) Ability to design, implement, and evaluate a system, process, component, or program to meet requirements .
- (d) Ability to interpret and synthesis data to provide valid conclusions
- (e) Ability to function effectively as a team member to achieve a common goal
- (f) Ability to understand professional, ethical and social issues and responsibilities
- (g) Ability to communicate effectively with a diverse groups
- (h) Ability to analyze the local and global impact of Information Technology on society
- (i) Ability to recognize and engage in continuing professional development and life long learning
- (j) Ability to use current techniques, skills, and tools necessary to accomplish projects related to Information Technology.
- (k) Ability to understand the impact of the professional engineering solutions in societal and environmental contexts for sustainable development.
- (l) Ability to understand engineering and management principles to manage projects in multidisciplinary environment.

| BOOLEAN ALGEBRA AND LOGIC | To understand the concepts of Boolean Algebra and Logic gates | М | S | S | М | S | М | S | S | М | S | М | М | W | W | М | М | М | W |
|--|--|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| GATES | To realize the Boolean functions using logic gates | Μ | S | S | М | S | М | S | S | S | М | S | М | W | W | S | М | S | W |
| COMBINATI ONAL LOGIC | To understand the concept of combinational circuits using K-map | М | S | S | М | S | М | S | S | М | S | М | М | W | W | М | М | М | W |
| | To design various combinational circuits based on applications | М | S | S | М | S | М | S | S | S | S | S | М | W | М | S | S | S | W |
| SYNCHRON OUS SEQUENTIA L LOGIC | To understand the concept of sequential logic using flip-flops | М | S | S | М | S | М | S | S | S | S | S | М | М | М | S | S | S | W |
| | To design the sequential circuits for registers and counters | Μ | S | S | М | S | М | S | S | S | S | S | М | W | М | S | S | S | М |
| ASYNCHRO NOUS SEQUENTIA L LOGIC | To understand the concept and design of asynchronous sequential logic | М | S | S | М | S | М | S | S | S | S | S | М | М | М | S | S | S | W |
| MEMORY AND PROGRAMM ABLE LOGIC | To learn the concepts of memory and programmable logic devices | М | S | S | М | S | М | S | S | S | S | S | М | W | М | S | S | S | М |